HARDWARE DESIGN REVIEW

Vehicle Program:

Fiat 142 HL

Valeo

Review Location: Teams
Review Date: 11/05/2023

INSTRUCTIONS FOR COMPLETION

This template defines the structure of the presentation which the Hardware Design Review is based upon.

The supplier shall complete this document according to the requirements in TFO Standard CS.00010/02. Item numbering in this presentation corresponds to headings in the TFO, and this sequence must be maintained.

Information can be written directly in this document, inserted as OLE objects or as links to external documents. Any external items must be provided with this document so that the entire presentation may be viewed on STELLANTIS computers regardless of access to the Internet or to the supplier's private data servers.

The supplier shall eliminate none of the existing sections but can modify their format, if necessary.

This completed document shall be sent to STELLANTIS Core E/E, Software and Hardware Engineering no later than four weeks after the program 1A release date. The Hardware Design Review must be complete no later than 6 weeks prior to the 2A release. The supplier should contact the STELLANTIS Component engineer to obtain actual dates for these milestones.

REVISION HISTORY

Date	Authored by	Approved by	Description
12/05/2023	Valeo		HW Design Review
22/05/2023	Valeo		HW Review

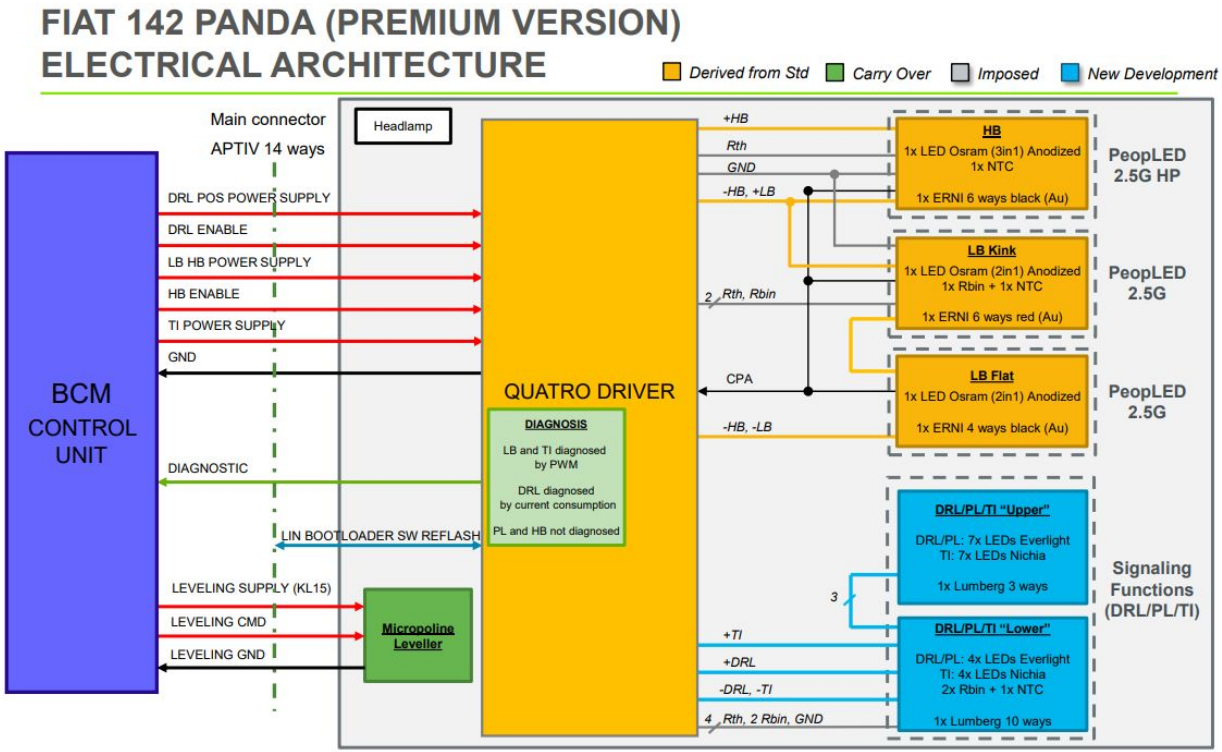
REQUIRED DESIGN DOCUMENTATION

Please send in advance of review:

- Functional Block Diagram;
- Schematics and BOM (may be presented by supplier);
- LED Selection Criteria;
- LED current limiting strategy (if present);
- Thermal Simulation or measurements;
- Optical Simulation or measurements;
- DFMEA (may be presented by supplier);
- LED fault strategy (one out, all out).

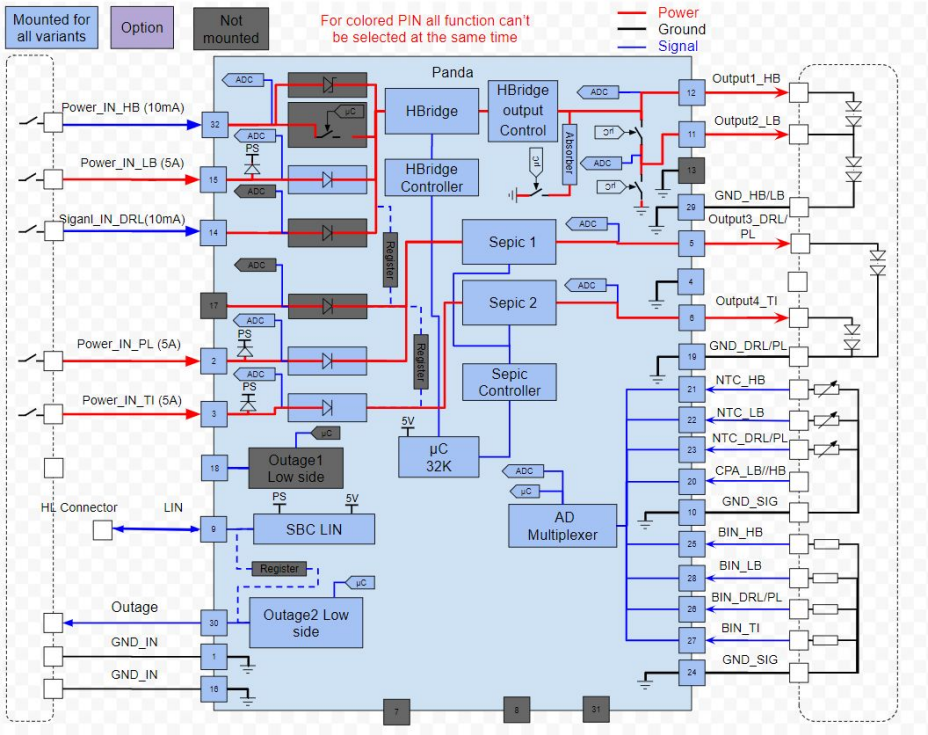
MODULE BLOCK DIAGRAM

Block diagram of the module, with detail of interactions between blocks.



MODULE BLOCK DIAGRAM

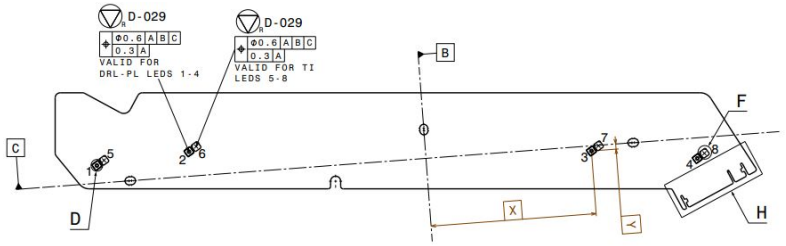
We can see that there are 3 DC-DC for Panda 142, one H Bridge + 2 SEPCI converter. H Bridge converter for LB and HB, and SEPIC-1 for DRL/PL, SEPIC for TI

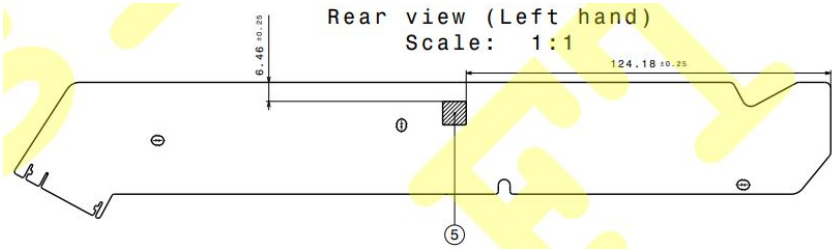


Present samples of (if available): FR4 black, 2 layer

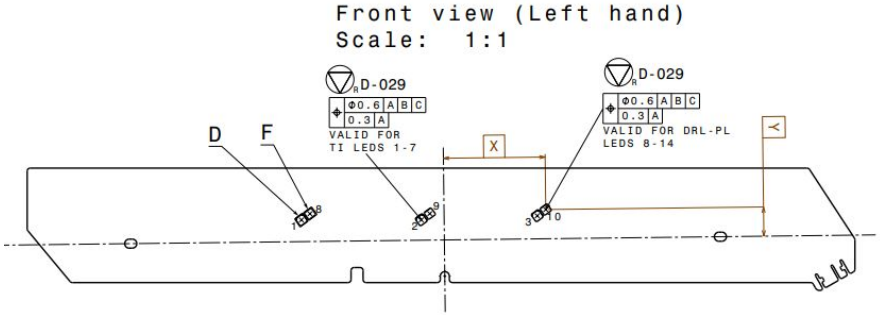
- A bare PCB from the module;

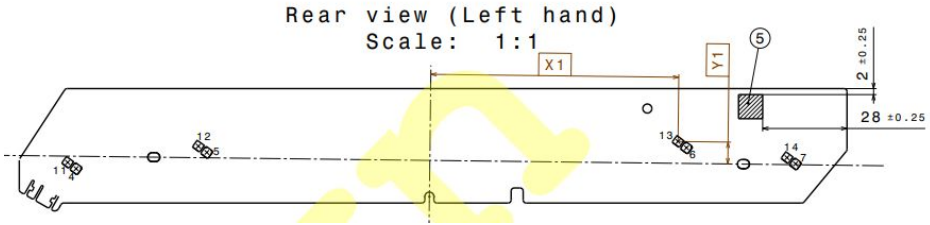
Lower





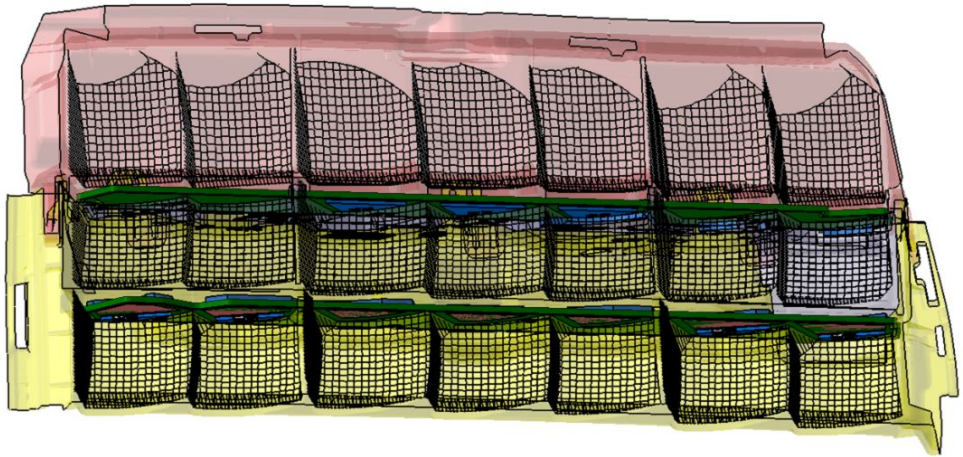
Upper

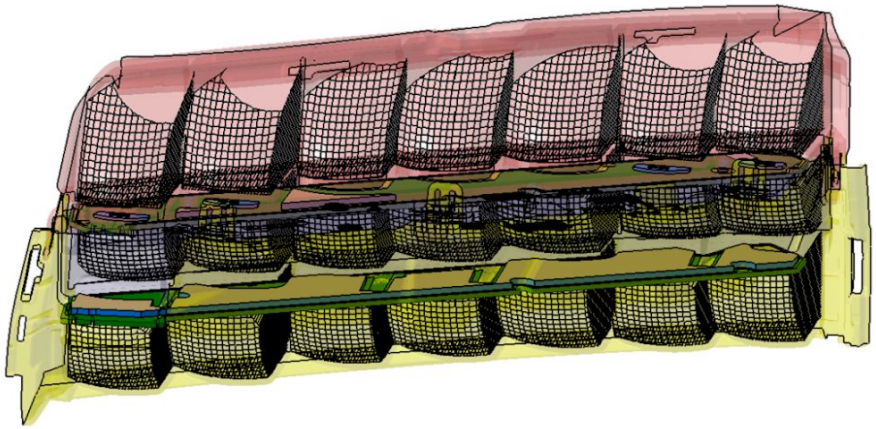




PC BOARD SAMPLES

- A complete PCB assembled with all components in final configuration





VEHICLE INTERFACES

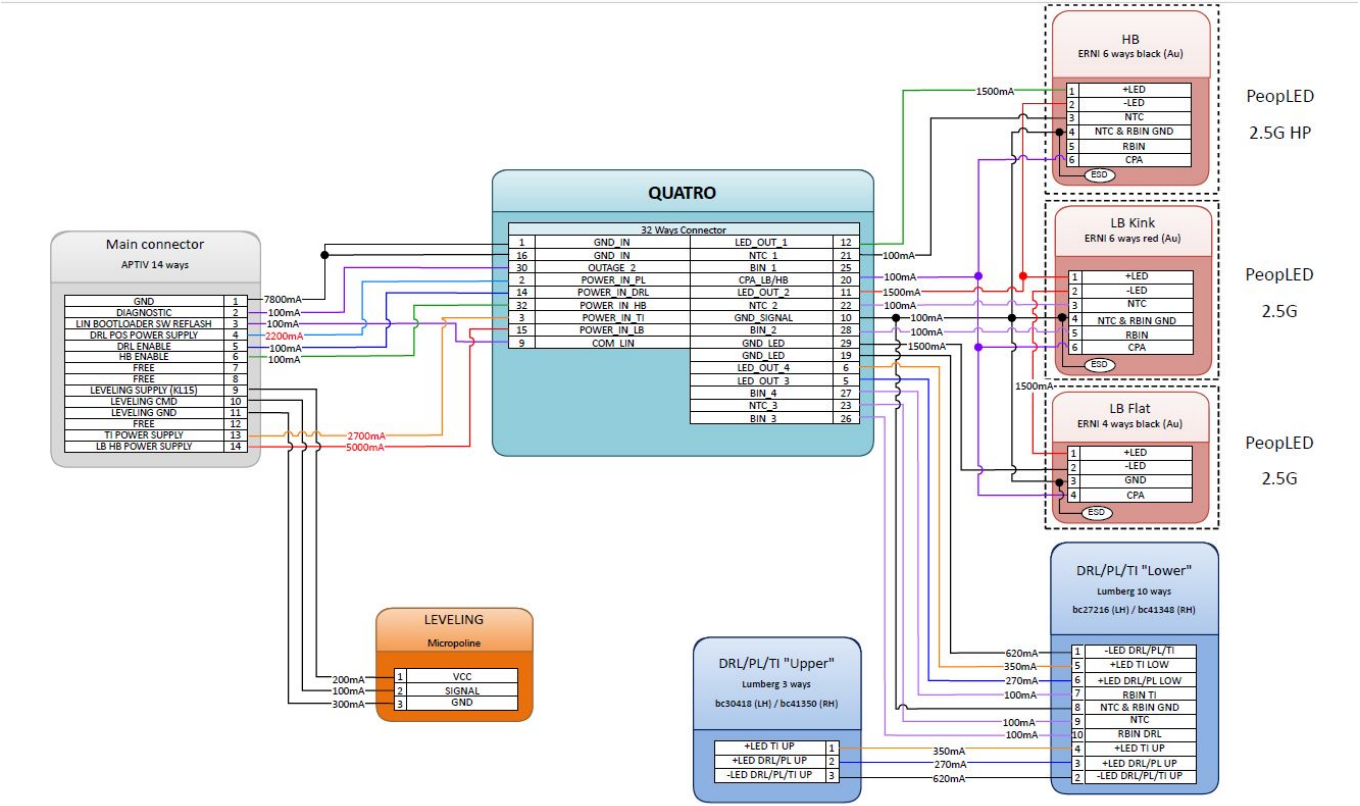
Present a schematic diagram including the hardware interfaces of all the connections of the subsystem with the vehicle and its own components.

The interface circuit(s) shall indicate all the relevant electric parameters and requirements for the circuit as concerns:

- Impedances;
- Voltages;
- Loads (operating current, inrush current, etc);
- Strategies affecting the parameters (e.g. PWM, Sleep conditions, Limp-Home circuits, etc.);
- Simulation results (in PSpice or SABER format);
- Any open interface issue that is not resolved.

Moreover, the schematic must show all optional components not present in the proposed design where mounting provisions are provided (“stuff options”) which can be incorporated at the request of STELLANTIS.

Schematic diagram of headlamp

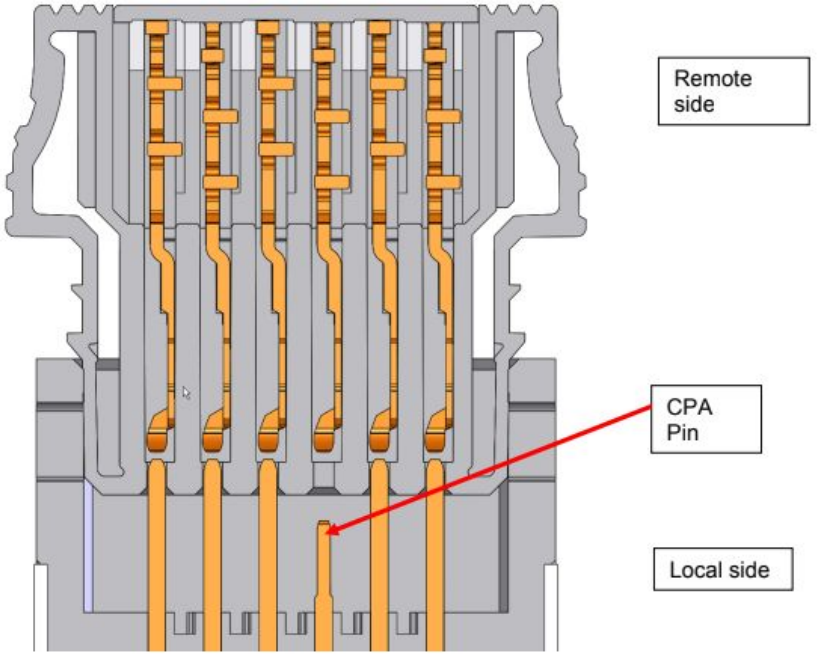


Details about the CPA connector

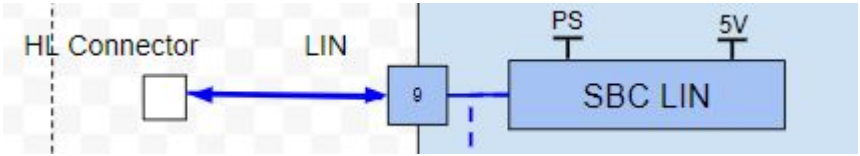
The MicroBridge connector system does have a feature that allows to ensure that plug and receptacle are always safely mated in applications.

This feature is called Connector Position Assurance (CPA).

The CPA feature is comprised of a dedicated short pin in the center of the connector and its pin field.



Software Reflash will be supported by the LIN interface for Panda 142. By connecting one HL wire (Depends on the harness definition of the HL) to the LIN interface of the driver (PIN 9) and Ground, and then using VN1611 and Valeo flash tools, SW can be upgraded by bootloader.

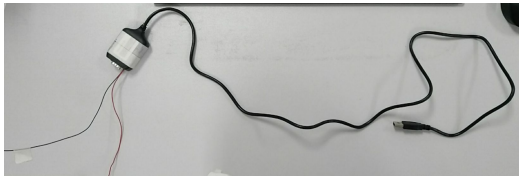


The Software Reflash time of Quatro driver by headlamp connector used to take around 12 minutes.

VEHICLE INTERFACES

The equipment needed to reflash the software is the following one:

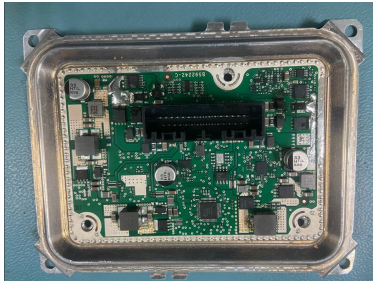
1. VN1611



2. Power supply

3. Computer

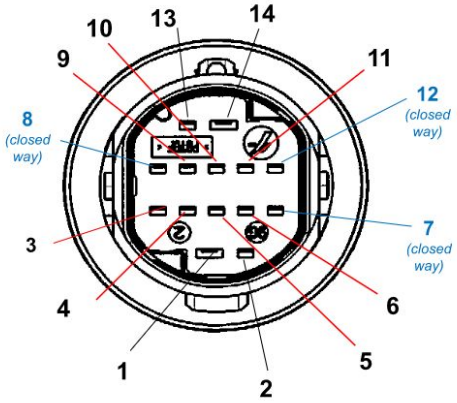
4. Quatro Driver with connector



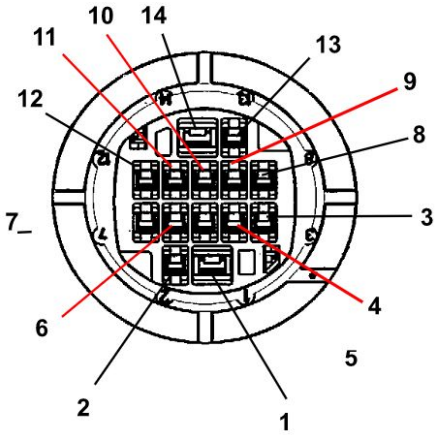
Headlamp main connector

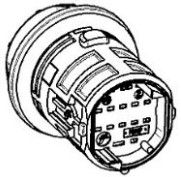
Part number FCA:	1/08740/93
Parte number supplier:	17261451
FCA Standard:	91349/41
Supplier:	APTIV
IMAN TCAE:	FJX33506
Configuration:	Male socket
Ways:	14
Environment:	No water proof
Link Ridbul:	

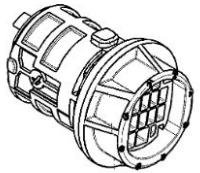
Connector view
(Connector mating)



Wire insertion view







ELECTRICAL ANALYSIS

Present electrical analysis of the design, and in particular:

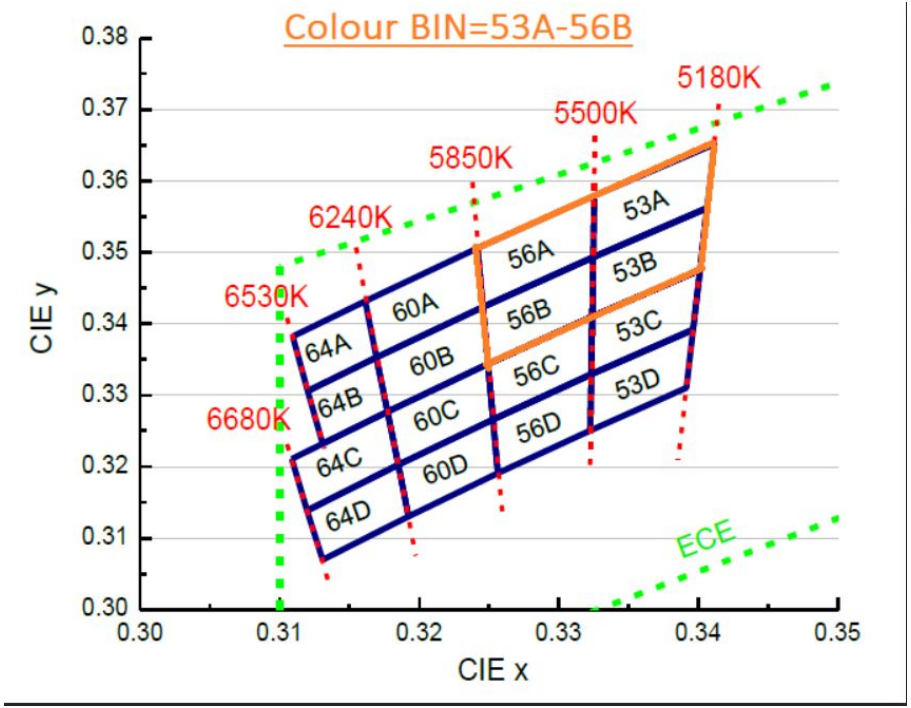
- Worst case analysis of critical areas of the design;
- Sneak circuit analysis (including paths in the system external to the module). Indicate if analysis on some paths is not possible due to lack of system information and identify these paths for follow up actions.
- LEDs specification (part number, quantity, color BIN, flux BIN, etc)

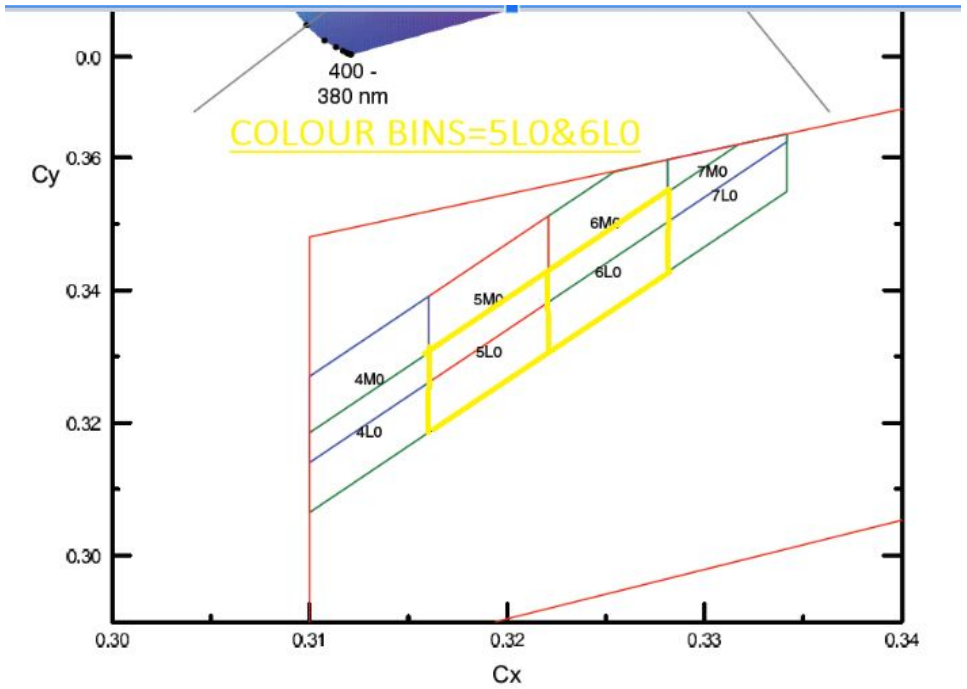
- **LEDs specification:**

Function	PCB	Nº LEDs	LED type	Flux BIN	Colour BIN
DRL	PCB 1(upper)	7	EVERLIGHT XI3030-C03501H-AM	J5 and J6	53A-56B
	PCB 2(lower)	4			
PL	PCB 1(upper)	7			
	PCB 2(lower)	4			
TI	PCB 1(upper)	7	NICHIA NJSA172CT	P18 and P19	L3
	PCB 2(lower)	4			
LB	KINK	1	OSRAM 2in1 KW C2L5L2.TK	D4, D5 and D6	5L0,6L0
	FLAT	1			
HB	-	1	OSRAM 3in1 KW C3L5L2.TK	T4, T5, T6	5L0,6L0

*NOTE: This information is for B3 mock-up

- **COLOUR BINS:**

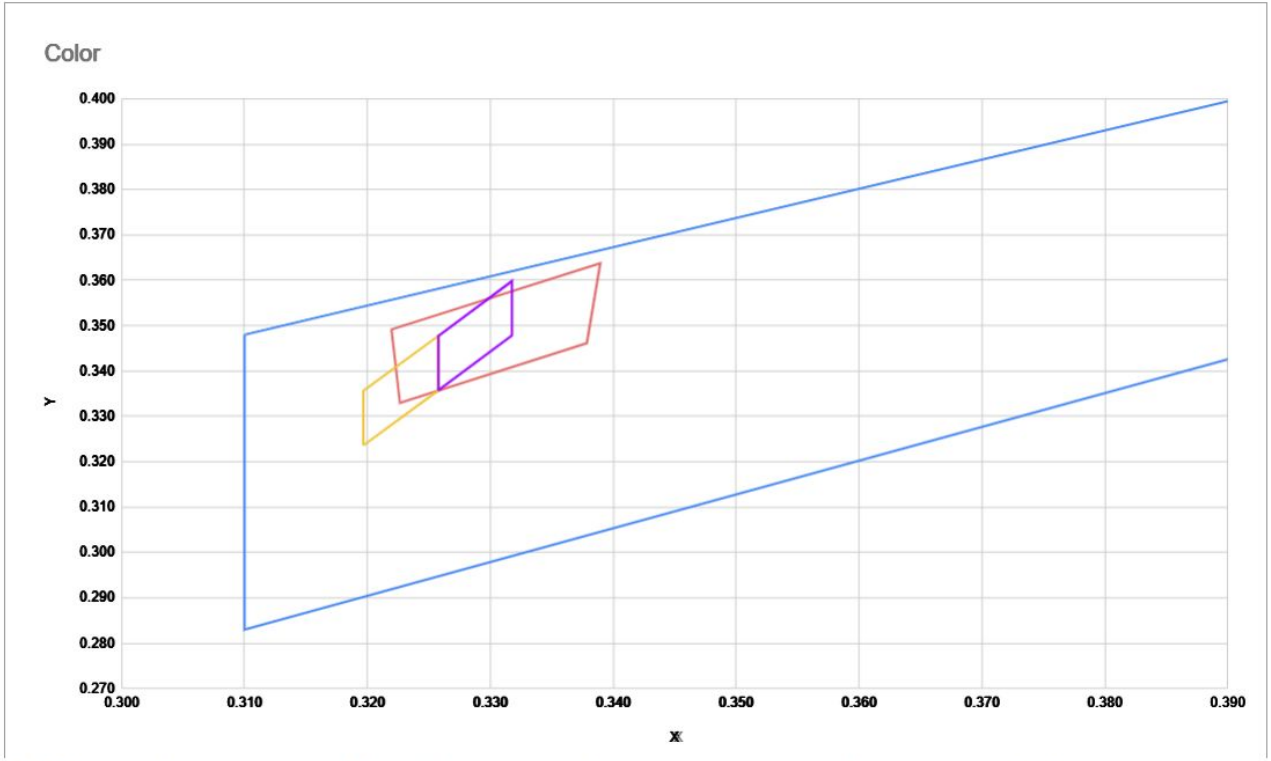




*NOTE: This information is for B3 mock-up

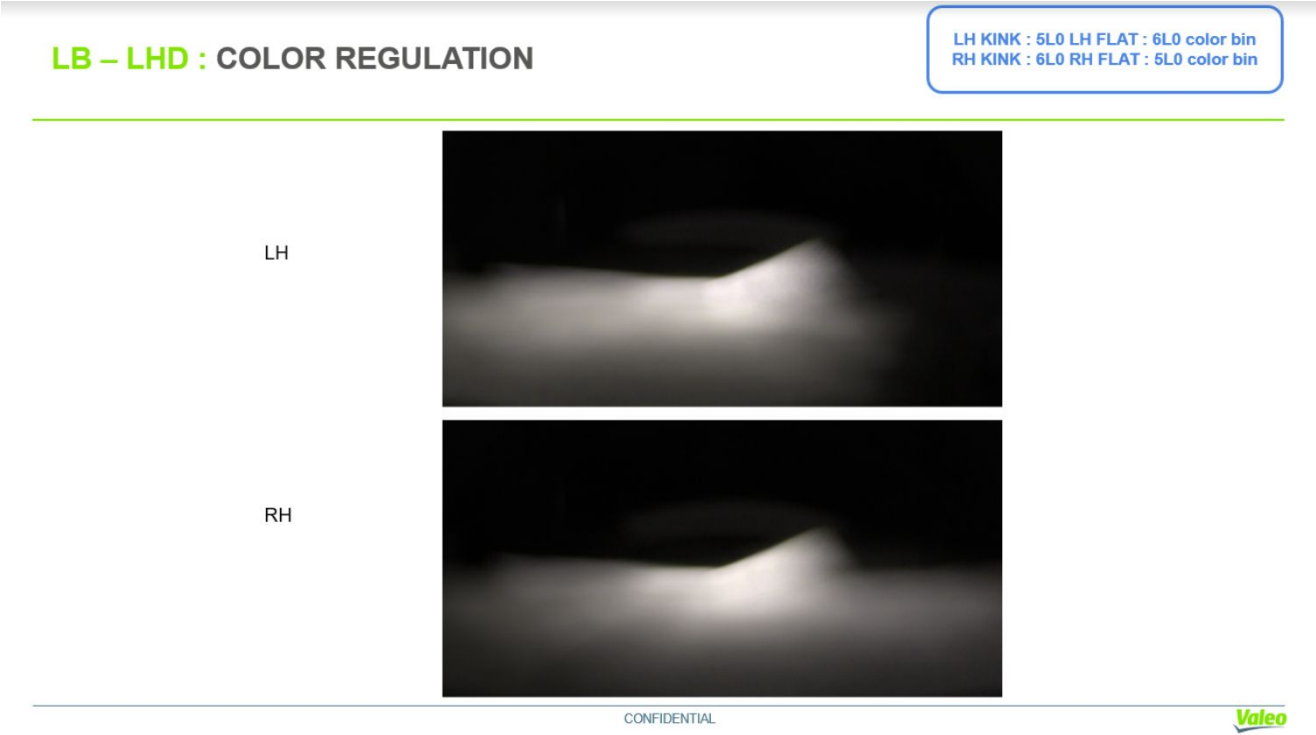
- **COLOUR BINS:**

LB&HB: 5L0
LB&HB: 6L0
DRL&PL: 53A-56B



*Estimate. For more precise information it is necessary to perform a simulation

- **COLOUR BINS:**



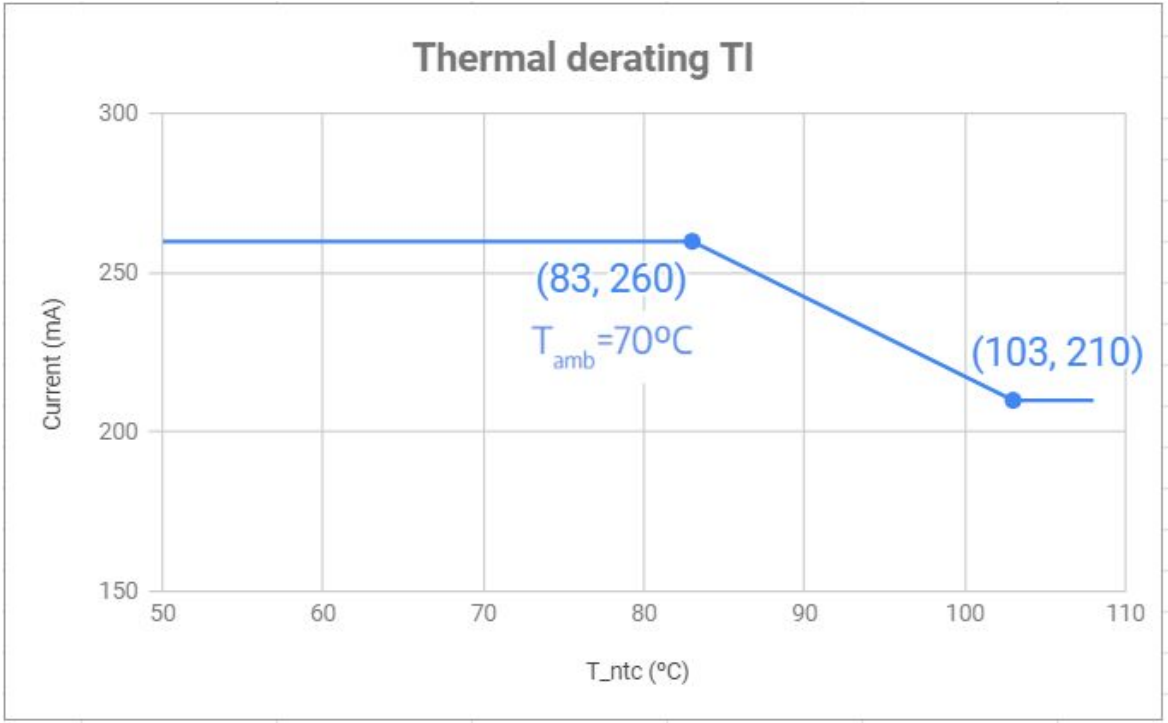
*NOTE: That's the simulation for the worst case scenario. Differences are not appreciable on the road

THERMAL ANALYSIS

- Present a thermal analysis of the design, limited to the power components.
- Derating strategy

Derating strategy

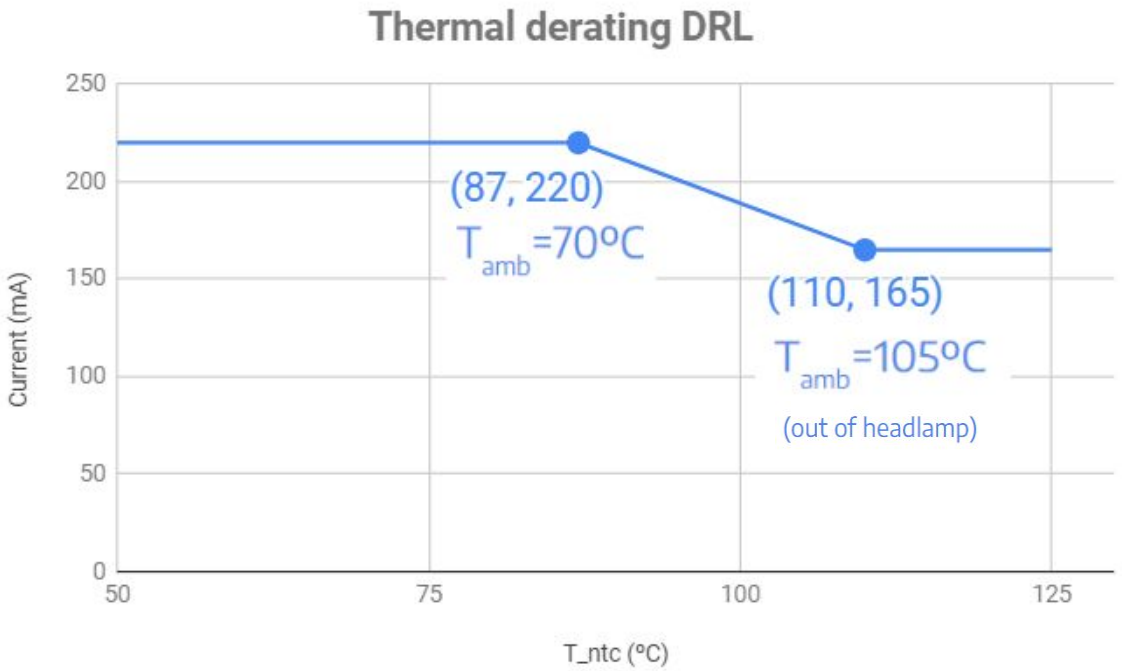
Turn indicator: The derating activation is necessary in the T_amb=70ºC scenario, but it could be earlier activated. The proposed derating activation is at T_ntc=83ºC, and the current goes down until 210mA. This protection protects the 90°C and 105°C scenarios.



*NOTE: This information is for B3 mock-up

Derating strategy

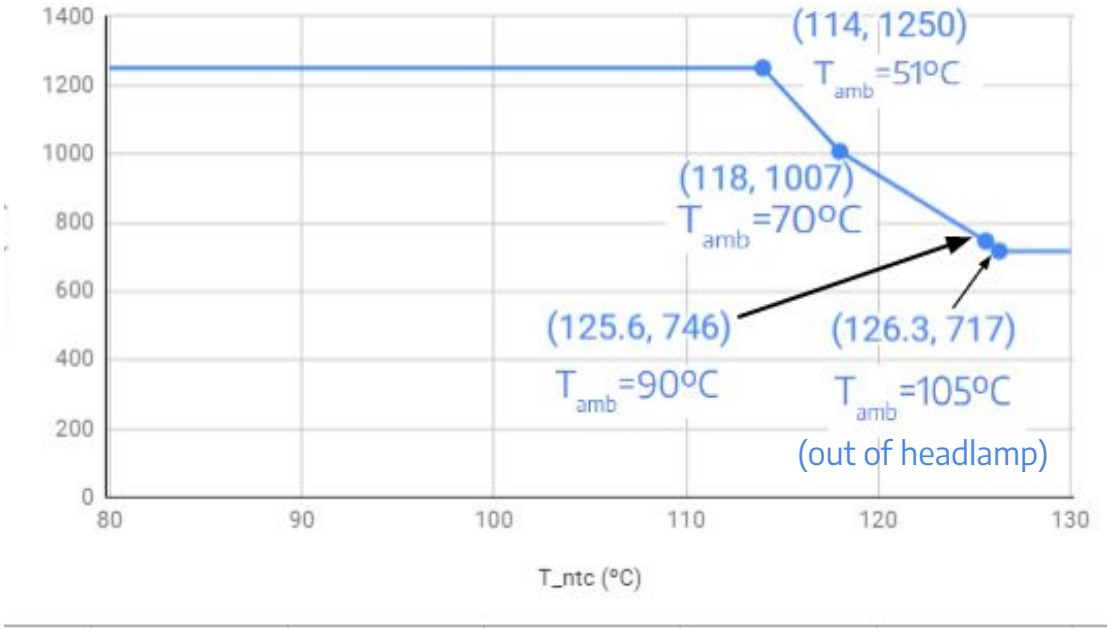
DRL: The derating activation is necessary in the T_amb=70ºC scenario, but it could be earlier activated. The proposed derating activation is at T_ntc=87ºC, and the current goes down until 165mA.



*NOTE: This information is for B3 mock-up

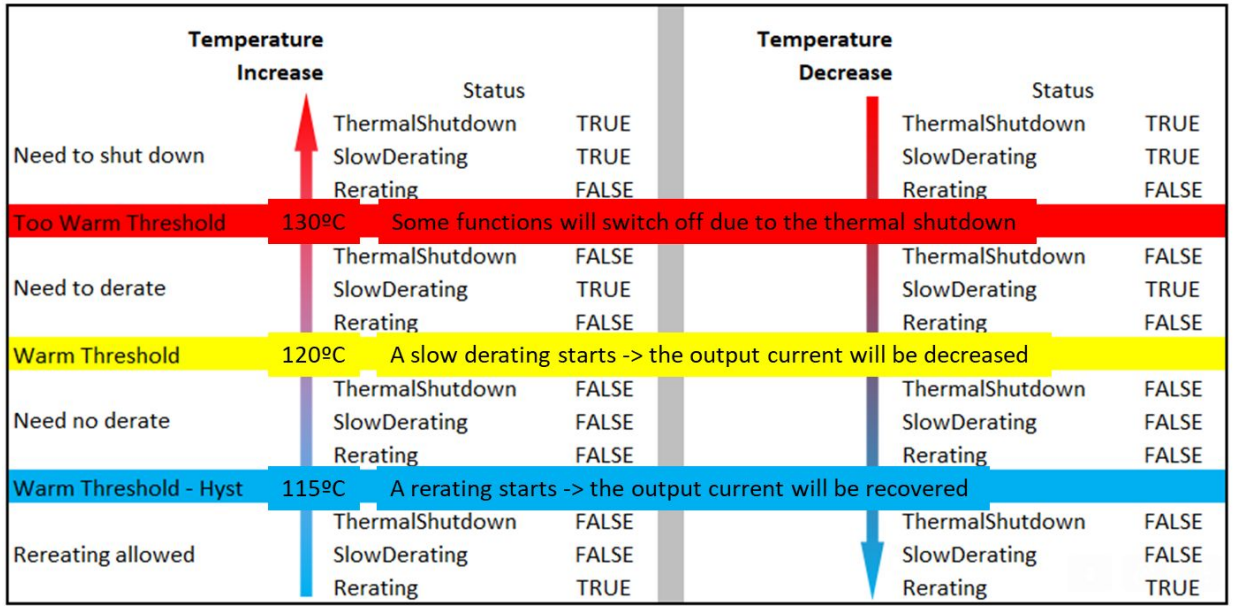
Derating strategy

LB and LB+HB: The derating activation is necessary in the T_amb=50ºC scenario. The proposed derating activation is at T_ntc=114ºC, and the current goes down until 717mA.



*NOTE: This information is for B3 mock-up

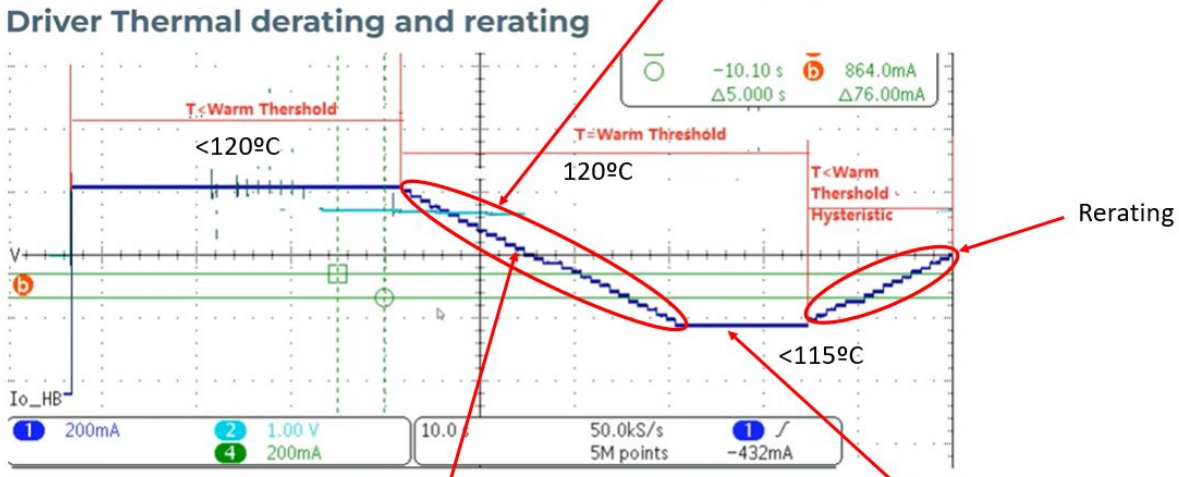
Quatro Driver Derating Strategy



Regarding the specific temperature, listed as below:

- Thermal shutdown: 130℃
- Thermal Derating: 120℃
- Hysterical：5℃

Quatro Driver Derating Strategy



RESULT SUMMARY

PERFORMANCE THERMAL SIMULATION

Objective :	To check the flux output of different functions in the FCA scenario. Predict the derating parameters.	Tools :	FloEFD 19.2 Selecto sheet AM [xi3030 using CUSTOM 20230215]
Context:	Previous DRL/TURN PCB layout was a draft. This is a real electronic layout. It is expected an additional loop of DRL TURN PCB with a Update of LB HB binning.	Customer specification document: Criteria :	ECE Regulations 1420 SSTS Headlamp-High rev00 6.1.3 Photometry according to the temperature Tj < Tj max Ts < Ts limit Flux > Flux target
Test Conditions :	**SIMULATED SCENARIOS** Scenario 1: 25°C&70°C LB Scenario 2: 25°C&70°C LB+HB Scenario 3: 25°C&70°C DRL Scenario 4: 25°C&70°C TI Scenario 5: 25°C PL		CONFORMITY :
Results and conclusion	LB HB: It is not possible to increase the current for lighting functions because of the derating forbidden at 50°C. DRL TURN: Similar performances than the previous study. PL: see recommendations		All functions are ok

Recommendations:

It is possible to reduce the DRL TURN pcb with a small impact with a thermal optimization of layout.
It is recommended to increase the PWM to change to PL function to 16%.

1/ SYNTHESIS

Flux performances of the different functions

LIGHTING FUNCTIONS

Function	Scenario	Current (mA)	LED Type	Bin	Tj (°C) Average	Ts (°C) Average	Flux (lm/led) Min (BIN only)	Flux (lm/led) Typ	Flux (lm/led) Max (BIN only)	Flux Target (lm/LED)	Other targets	Comments
LB	25°C (Steady)	1250	OSRAM KW	D4	108.3	95.9	758	775	792	700	Tj < 140°C Ts < 135°C	The derating is necessary at an outer temperature higher than 54°C (FCA request >50°C)
	25°C 1 minute				57.7	45.5	836	853	870	tbd		
	70°C (Steady)	*1066			135.8	125.4	603	617	630	550		

Function	Scenario	Current (mA)	LED Type	Bin	Tj (°C) Average	Ts (°C) Average	Flux (lm/led) Min (BIN only)	Flux (lm/led) Typ	Flux (lm/led) Max (BIN only)	Flux Target (lm/LED)	Other targets	Comments
HB	25°C (Steady)	1250	OSRAM KW	T4	109.6	96.3	1121	1146	1170	1000	Tj < 140°C Ts < 135°C	The derating starts at 54°C (FCA request >50°C) in the HB led The LB leds will start derating just at 50°C
	25°C 1 minute				59.4	46.2	1238	1263	1288	tbd		
	70°C (Steady)	*1007			134	123.5	861	880	899	700		

1/ SYNTHESIS

Flux performances of the different functions

SIGNALING FUNCTIONS

Function	Scenario	Current (mA)	LED Type	Bin	Tj (°C) Average	Ts (°C) Average	Flux (lm/led) Min (BIN only)	Flux (lm/led) Typ	Flux (lm/led) Max (BIN only)	Flux Target (lm/LED)	Other targets	Comments
DRL	25°C (Steady)	220	EVERLIGHT	J5	68.7	63.4	77.7	80.6	83.6	77.7	Tj < 140°C Ts < 125°C	
	25°C 1 minute				45.7	40.6	80.75	83.7	86.66	tbd		
	70°C (Steady)				111.5	106	70.8	73.5	76.2	64.8		

Function	Scenario	Current (mA)	LED Type	Bin	Tj (°C) Average	Ts (°C) Average	Flux (lm/led) Min (BIN only)	Flux (lm/led) Typ	Flux (lm/led) Max (BIN only)	Flux Target (lm/LED)	Other targets	Comments
TI	25°C (Steady)	260	NICHIA	P18	51.4	48.8	71.0	77.9	84.8	71.2	Tj < 140°C Ts < 125°C	
	25°C 1 minute				37.3	34.6	72.82	79.78	86.75	tbd		
	70°C (Steady)				92.4	89.7	64.1	70.4	76.9	59.3		

Function	Scenario	Current (mA)	PWM	LED Type	Bin	Tj (°C) Average	Ts (°C) Average	Flux (lm/led) Min (BIN only)	Flux (lm/led) Typ	Flux (lm/led) Max (BIN only)	Flux Target (lm/LED)	Other targets	Comments
PL	25°C (Steady)	220 mA	10%	EVERLIGHT	J5	32.3	31.8	8.4	8.7	9.0	13 lm (100 cd)	Tj < 140°C Ts < 125°C	
	25°C 1 minute					27.3	26.8	8.4	8.7	9.0	< 18.2 lm		

STELLANTIS

RESULT SUMMARY

PERFORMANCE THERMAL SIMULATION

Objective :	To check the components temperature in the FCA scenario. FCA NORM: CS.00056 "ENVIRONMENTAL SPECIFICATION FOR ELECTRICAL / ELECTRONIC (E/E) COMPONENTS"	Tools :	FloEFD 19.2 Selecto sheet AM (xi3030 using CUSTOM 20230215)
Context:	Previous DRL/TURN PCB layout was a draft. This is a real electronic layout. Update of LB HB binning.	Customer specification document:	CS.00056 (105ºC tests)
		Criteria :	Tj < Tj max Ts < Ts limit Flux > Flux target
Test Conditions :	**SIMULATED SCENARIOS** Scenario 1: 105C DRL Scenario 1: 105C TURN		CONFORMITY :
Results and conclusion	All the components are under the limit allowed for each one.		All functions are ok
Recommendations:			

Valeo

EMC ANALYSIS

Present analysis and reports of the design as concerns EMC aspects, and in particular:

- Availability of elements and tools to assess the EMC aspect and to describe how they apply during the system development process to forecast the EMC performances and to optimize the design parameters;
- Detailed information on the grounding concept, with particular attention for the current paths for the high-power devices, loads with PWM drive, and switching transients;
- Detailed information on the placement strategy of the system components and routing, in order to optimize the EMC performance and to make sure that the generation of interference between different systems is accurately avoided, with particular attention for audio interference, cross-talk and transient events;
- ESD:
  - Capacitors on strategic location (connector…);
  - Capacitors placement done close to the connector and EMC Layout review is done as per Valeo Process
- EMC:
  - Reduction of emitting paths surface;
  - Use of a DCDC driver architecture.

DESIGN STRATEGIES

Present descriptions concerning:

- Supply voltage fault detection and involved strategies.
- ECU protections (reverse polarity, over-voltage, over-current, N-1, one out - all out...)

Electrical/EMC identified risk

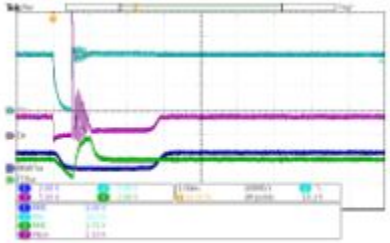
Test Case	Criteria	Results	Proposals
Supply voltage drop out	M1 < 500us M3 for all other points >=500us	DRL OK LB-HB-TI OK (short flicker 2.5ms for pulses > 100us)	Short light flicker 2.5ms as part as M1 performance
Supply voltage dips	F12: M1<=250uS,M3>250uS; F11/F10: M1<=1mS,M3>1mS;	DRL OK LB-HB-TI OK (short flicker 2.5ms for pulses > 100us)	
Engine cranking low voltage warm cranking / Stop-Start	M1(Reduce flux is allowed)	Based on JEEP516 DV. OK	

The DV results of Jeep 516 HL

Supply Voltage Drop Out-CS.00054, 5.3.2	COMPLIANT	
Power Supply Disconnection-CS.00054, 5.3.3	COMPLIANT	
Reset Behaviour at Voltage Drop-CS.00054, 5.3.4	COMPLIANT	
Supply Voltage Dips-CS.00054, 5.3.5	Accepted by PF90165 Deviation L1 is requested	According to PF90165 the behaviour the assessement can be L1
Engine Cranking Low Voltage – Resembling Cold Cranking-CS.00054, 5.3.6	COMPLIANT	
Engine Cranking Low Voltage – Warm Cranking / Stop – Start-CS.00054, 5.3.7	COMPLIANT	

Electrical/EMC identified risk

500us



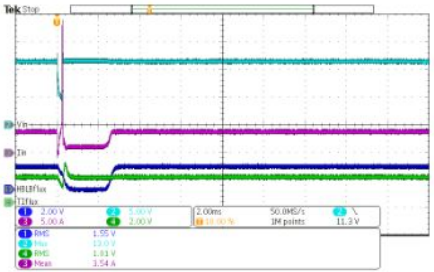
HBLB: The LED flicker
TI:No variable flux observed

Voltage drop up 500us
HBLB flux shuts down during 3ms

Flux variation below 20ms are not visible on the road

Video will be provide with at least 30f/s quality

0.25ms



HBLB: The LED flicker
TI:No variable flux observed

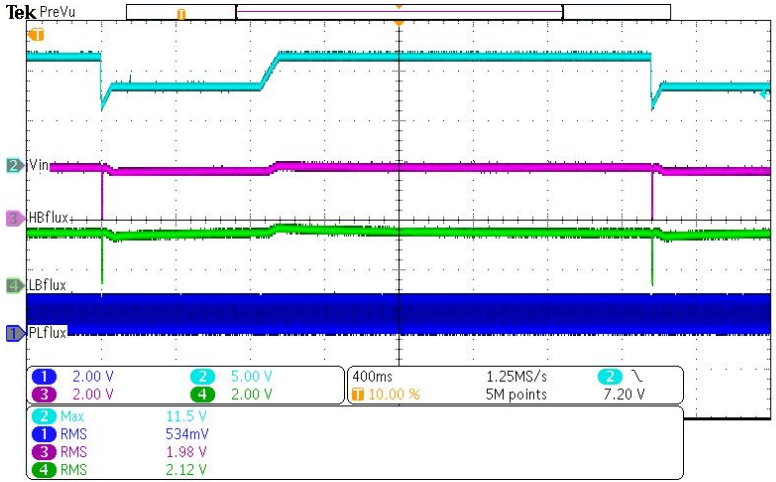
Voltage dips >1ms
HBLB flux shuts down during 3ms

Video will be provide with at least 30f/s quality

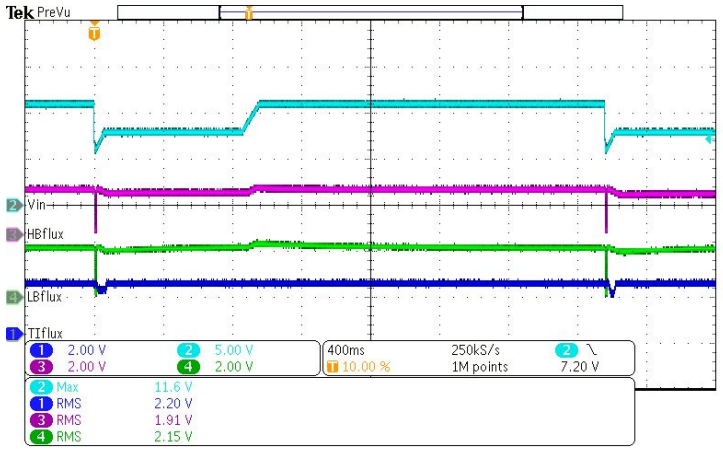
Engine cranking low voltage-warm

Table 13 – Warm Cranking Pulse Parameters								
Parameter	Vb	Vmin	Vstart	tf	t6	t7	t8	tr
Value	11V	6V	8V	5ms	5ms	50ms	800ms	100ms

HB+LB+PL mode



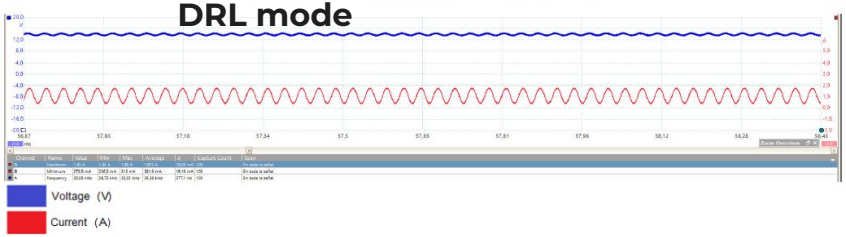
HB+LB+TI mode



Electrical/EMC identified risk

Test Case	Criteria	Result
Supply Voltage Ripple (Superimposed Alternating Voltage)	M1	M1 OK Risk of DRL input power line minimum consumption is not fulfilled during test application

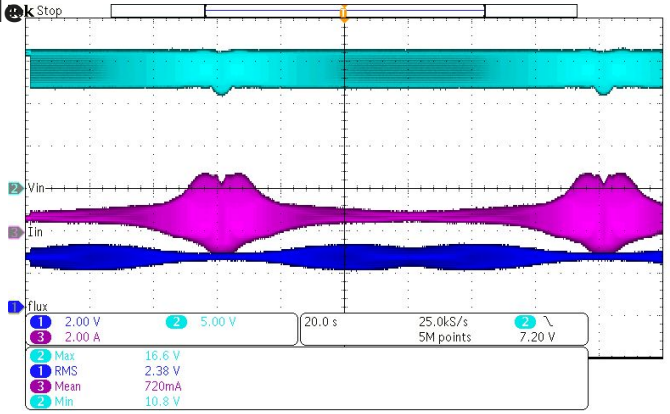
DRL mode



Consumption ok for 30Hz

Remarks: Ripple frequency depends of engine rpm when generator failure occurs
During Pre-DV phase, frequency threshold where consumption drops below 142mA will be measure

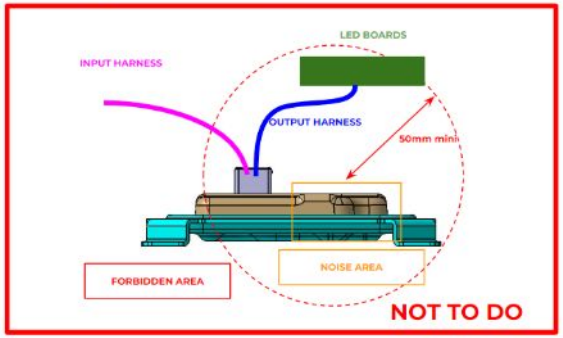
DRL mode

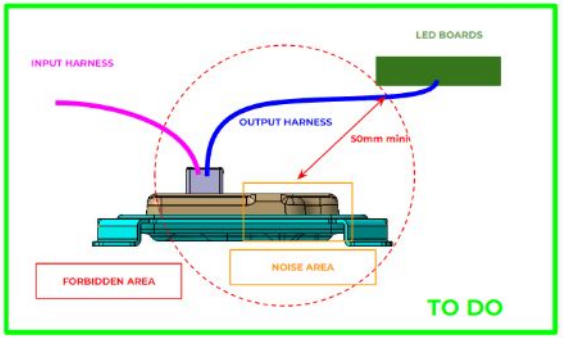


Consumption below failure detection threshold at 30KHz

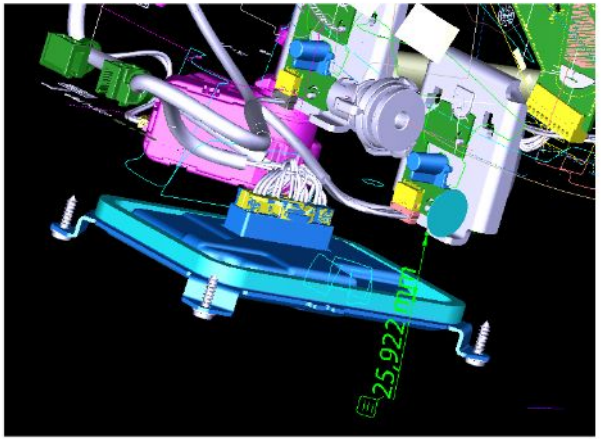
EMC identified risk

Integration in HL environment



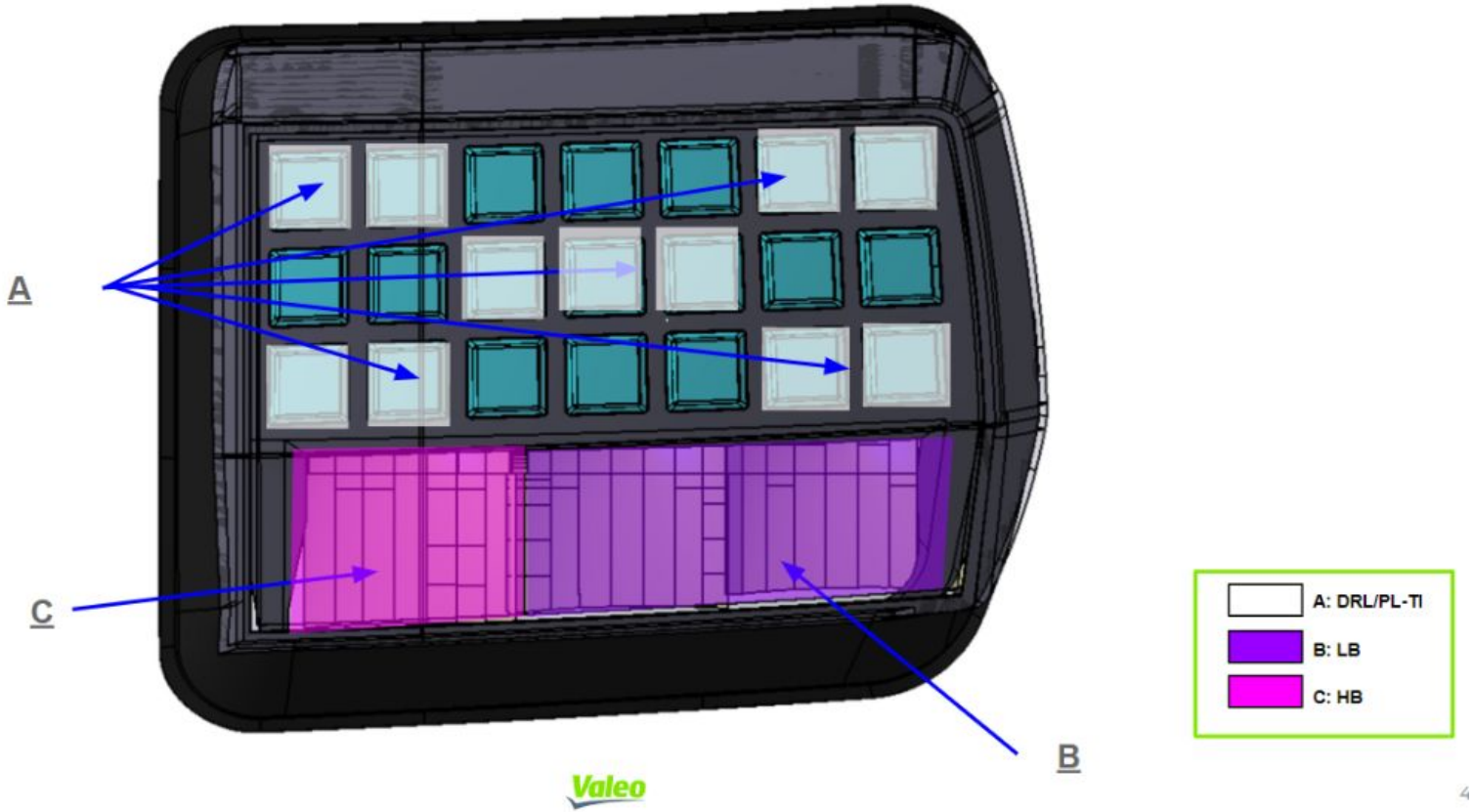


Not followed, warning



History of the subject in mail: Re: Estudio EMC Fiat 142 PANDA

GLOBAL OVERVIEW



- ECU protections (reverse polarity, over-voltage, over-current, N-1, one out - all out...)

Function	Active Chamber	Reaction of the component	Failure report
DRL	A	1 Light source off --> Function OFF	Reporting by current consumption. IIH_Default when there is failure = 55 mA
PL	A	1 Light source off --> Function OFF	No diagnosis
TI	A	1 Light source off --> Function OFF	Reporting by PWM diagnose protocol
LB	B	1 Light source off --> Function OFF	Reporting by PWM diagnose protocol
HB	C	1 Light source off --> Function OFF	No diagnosis

SCHEMATIC DETAILS

Present schematic details→ Not able to share

PCB LAYOUT

Present layout details, and in particular: → Not able to share

- Best practices and lessons learned application;
- Worst case analysis of critical areas of the layout;

CRITICAL COMPONENTS

- There are no critical components for PCBs
- For driver, we have the following list:

Supplier	MPN (Ordering number)1	Critical part (Y/N)	Status
ANALOG DEVICES	LT8391DJUFDM#WTRPBF	Y	Carry over parts, no shortage
INFINEON	TLD6098-2ES_/_SP005568816	Y	Carry over parts, no shortage
NXP SEMICONDUCTORS	935377352528_/_FS32K118LFT0MLFR	Y	Carry over parts, no shortage
TEXAS INSTRUMENTS	TMUX1308QDYYRQ1	Y	Carry over parts, no shortage
INFINEON	BTS3050EJ_/_SP001340336	Y	Carry over parts, no shortage
TEXAS INSTRUMENTS	TLIN10285DRBRQ1	Y	Carry over parts, no shortage
INFINEON	BTS4175SGA_/_SP000360279	Y	Carry over parts, no shortage
INFINEON	IPG20N06S4L-11_/_SP000705550	Y	Carry over parts, no shortage
NEXPERIA	934067038115_/_BUK9Y38-100E,115	Y	Carry over parts, no shortage
VISHAY	SQ2362ES-T1_GE3	Y	Carry over parts, no shortage
INFINEON	2N7002DW-H6327_/_SP000917596	Y	Carry over parts, no shortage
NEXPERIA	934064134115_/_2N7002PS-115	Y	Carry over parts, no shortage
NEXPERIA	934034210115_/_PUMX1-115	Y	Carry over parts, no shortage
ROHM	UMX1NFHA	Y	Carry over parts, no shortage

DFMEA

- PCB flatness: Controlled in production following DRW data
- Led current: checked with protos, controlled in production by driver
- Led flux: checked with simulations and protos, controlled in production by driver
- Led Orientation on PCB: Checked with protos, controlled in production following DRW data
- Led Position: checked with protos, controlled in production following DRW data

ENGINEERING VALIDATION PLAN

Present the engineering validation plan (including reliability, vehicle integration requirements, system safety activities, software validation, etc.)

- HWI verification (9 point check of inrush and operating current)
- Diagnose protocol verification
- Fault strategy verification (one out – all out, N-1, etc)
- Requirements verification (animation, truth table, etc)

TESTING & VALIDATION PLAN - B2 samples

- Electronic design validation plan.: Attached
- Include the input current consumptions and inrush measurements (9-Point-Check):
- Include the LEDs current consumptions measurements of each function, in order to guarantee the photometric requirements: Attached
- Include the PWM diagnose protocol validation: To be included after the implementation.

TESTING & VALIDATION PLAN - B2 samples

- Inrush measurements (each measurement has been made in the power supply pins)

	9-Point-Check INRUSH activation								
FUNCTIONS	-40ºC			25ºC			105ºC		
	8V (10us)	13.5V (13us)	16V (16us)	8V (10us)	13.5V (13us)	16V (16us)	8V (10us)	13.5V (13us)	16V (16us)
LB	9.7391A	19.98A	24.375A	10.625A	21.166A	25.802A	13.8534A	23.589A	28.332A
LB+HB	9.3794A	19.19A	23.684A	10.451A	20.419A	24.696A	13.613A	23.858A	28.332A
PL	9.8182A	20.585A	25.012A	9.581A	19.162A	23.431A	10.032A	17.905A	21.364A
DRL	11.083A	20.427A	24.696A	10.921A	19.783A	22.9A	10.1388A	17.806A	21.265A
TI	11.241A	20.901A	25.486A	11.083A	20.269A	24.221A	9.9723A	17.81A	21.486A
	slew rate: 1V/us								
	wire interface: APROX 250mOhms								
	Driver used: SW B2								

- Include the input current consumptions (9-Point-Check. Each measurement has been made in the power supply pins):

FUNCTIONS	9-Point-Check CURRENT consumption									
	25ºC			105ºC			-40ºC			
	8V	13.5V	16V	8V	13.5V	16V	8V	13.5V	16V	Expected
LB	2.3178A	1.3604A	1.1588A	2.1221A	1.3097A	1.1298A	2.3864A	1.4114A	1.214A	<5A
LB+HB	3.7564A	2.2430A	1.88A	3.74A	2.1826A	1.8193A	3.692A	2.3678A	1.9811A	<5A
PL	143.19mA	104.47mA	97.697mA	140.09mA	103.23mA	97.693mA	153.83mA	109.94mA	102.41mA	<2.2A
DRL	1.0762A	645.2mA	557.95mA	1.0635A	634.92mA	548.93mA	1.1237A	675.72mA	583.67mA	<2.2A
TI	1.1326A	668mA	572.98mA	1.1028A	649.38mA	557.46mA	1.186A	700.97mA	600.99mA	<2.7A