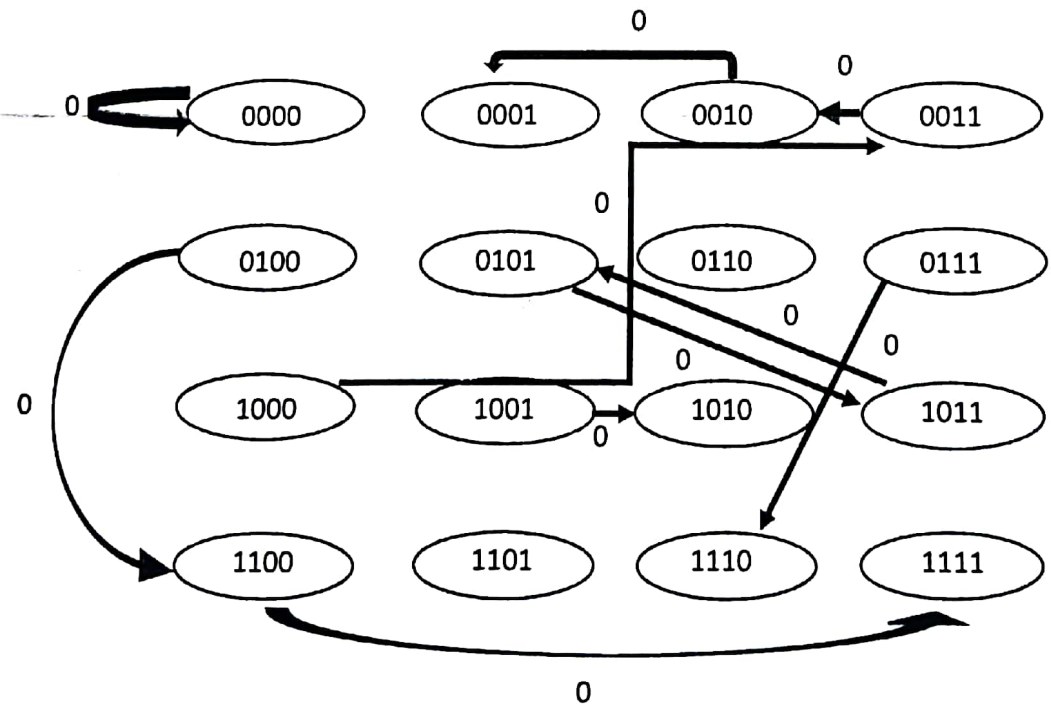
Cairo University	Computer Engineering Program		Program:	CCEC
	Academic Year:	2021/2022	Semester:	FALL 2021
	Course Code:	CMPN 111	Course Title:	Logic Design II
	Day:	Saturday	Date:	January 22nd, 2022
	Time:	8:30 – 10:30	Full Mark:	40

Question (1): [20]

- Given the state diagram below, design a synchronous sequential circuit using JK flip-flops with PAL technology to implement it. [Hint: When External input = "0, it will act normally, E = "1" it will reset]
- Define its functionality.
- Redesign using
  - D FF / PLA technology
- Calculate the following timing parameters; for each design;
  a. Propagation delay t_{PD}.
  b. Setup time t_s.
  c. Hold time t_H.
  d. Clock-to-output delay t_{OC}.
  e. Clock-to-output delay through the logic array t_{OC2}.
  f. System clock to system clock delay t_{SCS} (minimum frequency of operation)

[Assume the delay time for each gate is 1.5 ns & each F.F. is 3 ns, t_s=0.5ns]



Examiners Signature

Ihab Talkhan

For Students: Please write using a blue pen only