Computer Engineering Department		Program:	CCEC	
Academic Year:	2020	Semester:	FALL 20	
Course Code:	CMPN 111	Course Title:	Logic Design II	
Day:	Sunday	Date:	December 6th, 2020	
Time:	9:15 - 10:15	Full Mark:	20	

18.5 / 20

Name:	ID #:
علي سعيد البحار توفيق	1180036

Question (1): (15 point)

8 4 -2 -1

For the following circuit:

i. State its functionality.
ii. Redesign, using ;
    1. 3-input NOR gates (SC).
    2. 4x1 Multiplexers.
    3. PAL configuration.
    4. PLA configuration.
    5. PROM configuration
iii. Compare between all designs w.r.t. (# of gates / # of ICs / delay / expansion)

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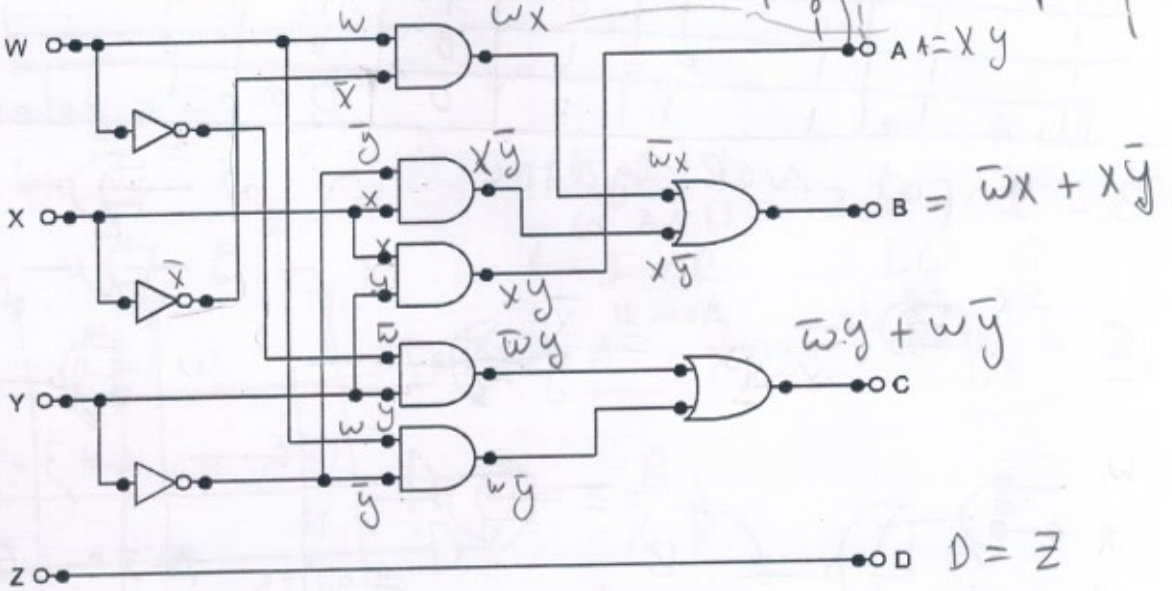

[Hint : all dots means connections not bubbles]

Z	Y	X	W	D	C	B	A
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0
0	0	1	0	0	0	1	0
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	1	1
0	1	1	1	0	0	0	0

Examiners Signature

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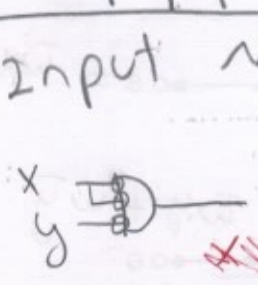
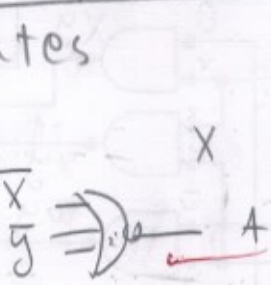
$A = xy$, $B = \bar{w}x + x\bar{y}$, $C = w\bar{y} + \bar{x}y$, $D = z$

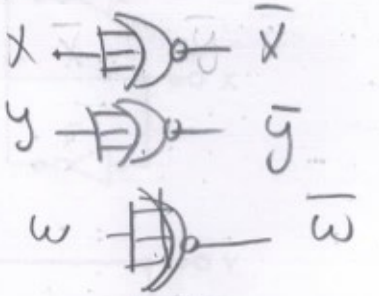
2	1	-2	-1	8	-4	+2	+1
w	x	y	z	A	B	C	D
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	1	1	1	0
0	1	1	1	1	1	1	1
1	0	0	0	0	0	1	0
1	0	0	1	0	0	1	1
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1
1	1	0	0	0	1	1	0
1	1	0	1	0	1	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	1

3-Input NOR gates



$\equiv$



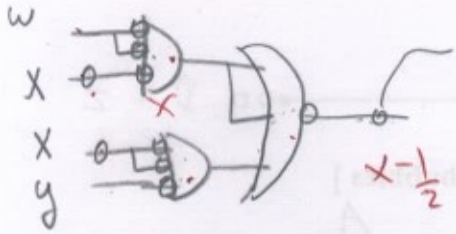


$\bar{w}$

4×3

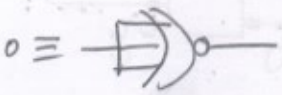
1

1+5+ 14×3



$x - \frac{1}{2}$

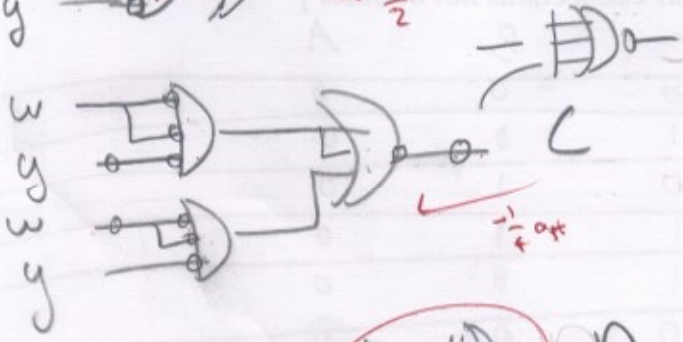
$\equiv$



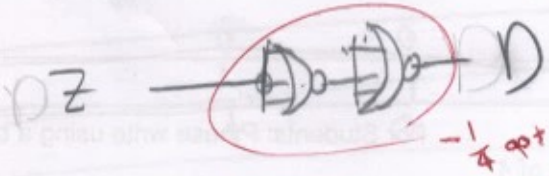
11

# gates	# Σc	# exp	delay
42 NOR	11	2	12

$x_{-\frac{1}{4}}$

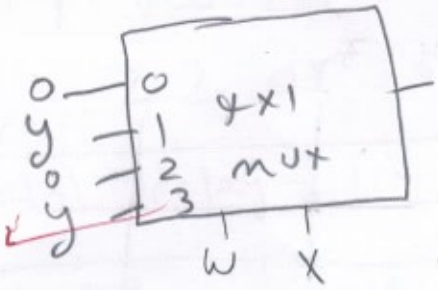


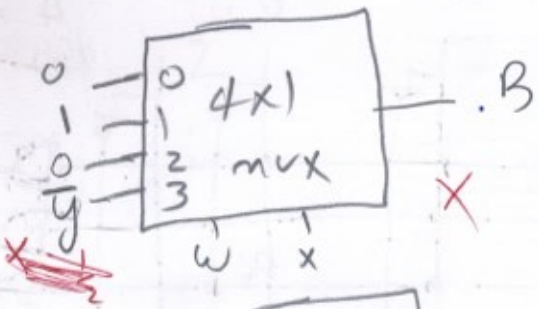
$-\frac{1}{4}$ opt

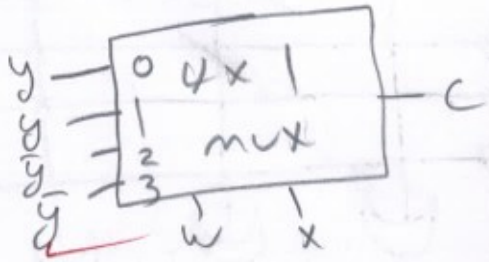


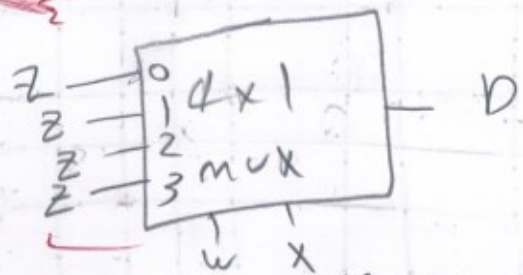
$-\frac{1}{4}$ opt

② 4x1 Multiplexer









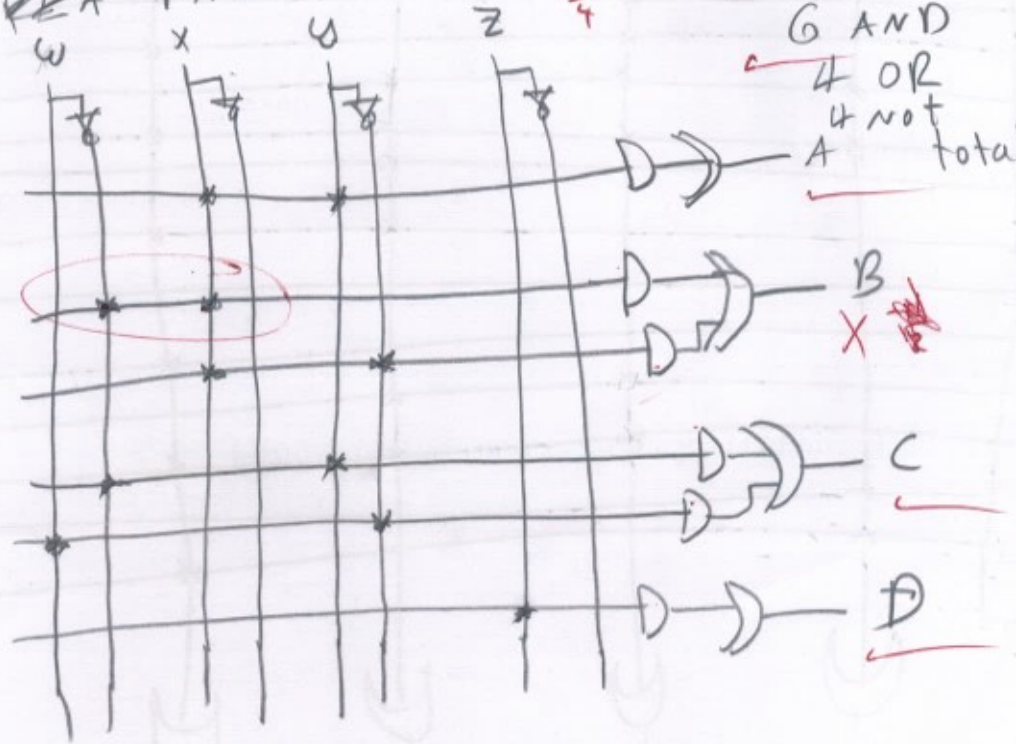
assume one IC

# gates	# IC	# exp	# delay
4 mux	4 IC	0	5
1 not	1 IC	5	12

total delay = zero ?? X -1/4

w, x, y, z

③ PLA PAL



# gates	# IC	# exp	# delay
6 AND	2 IC	2	1
4 OR	1 IC	0	1
4 not	1 IC	2	1

total delay = 3

PLA

w x y z

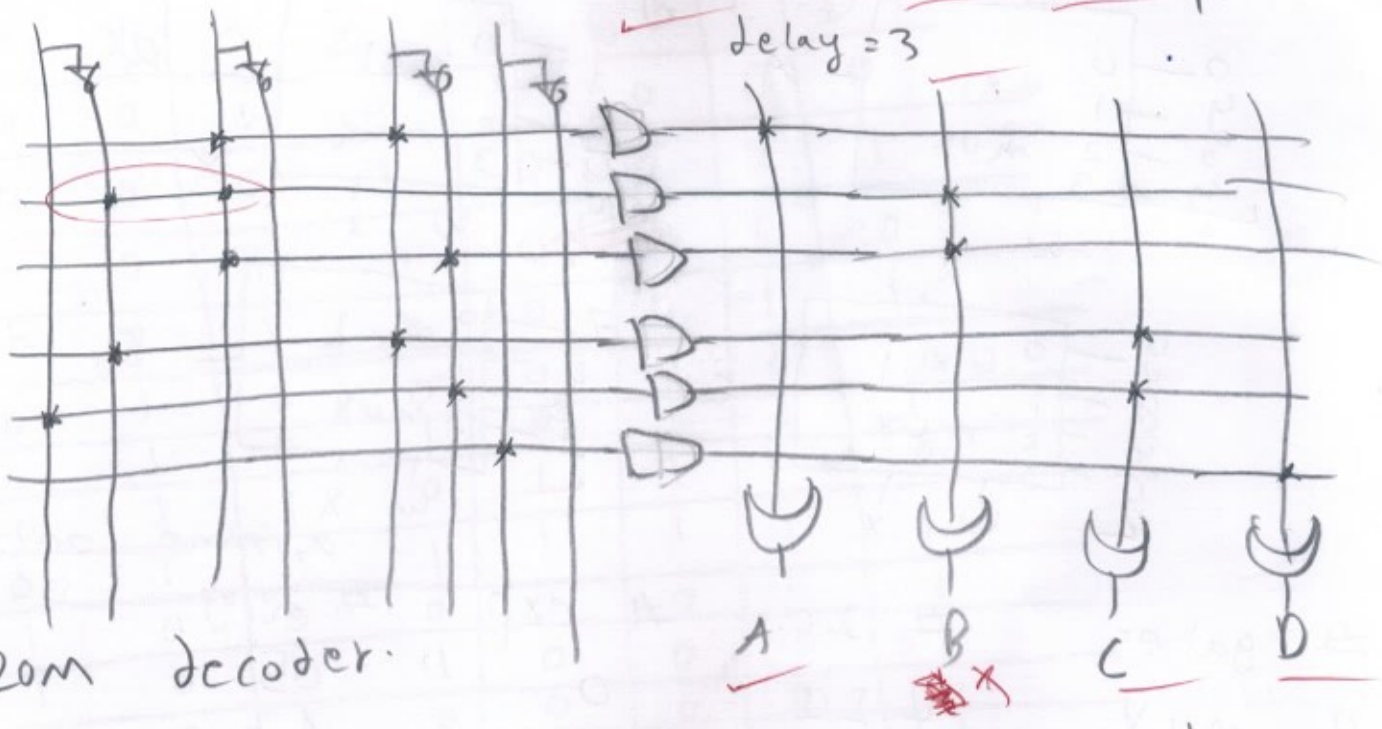
6 AND 2 IC 2

4 OR 1 IC 0

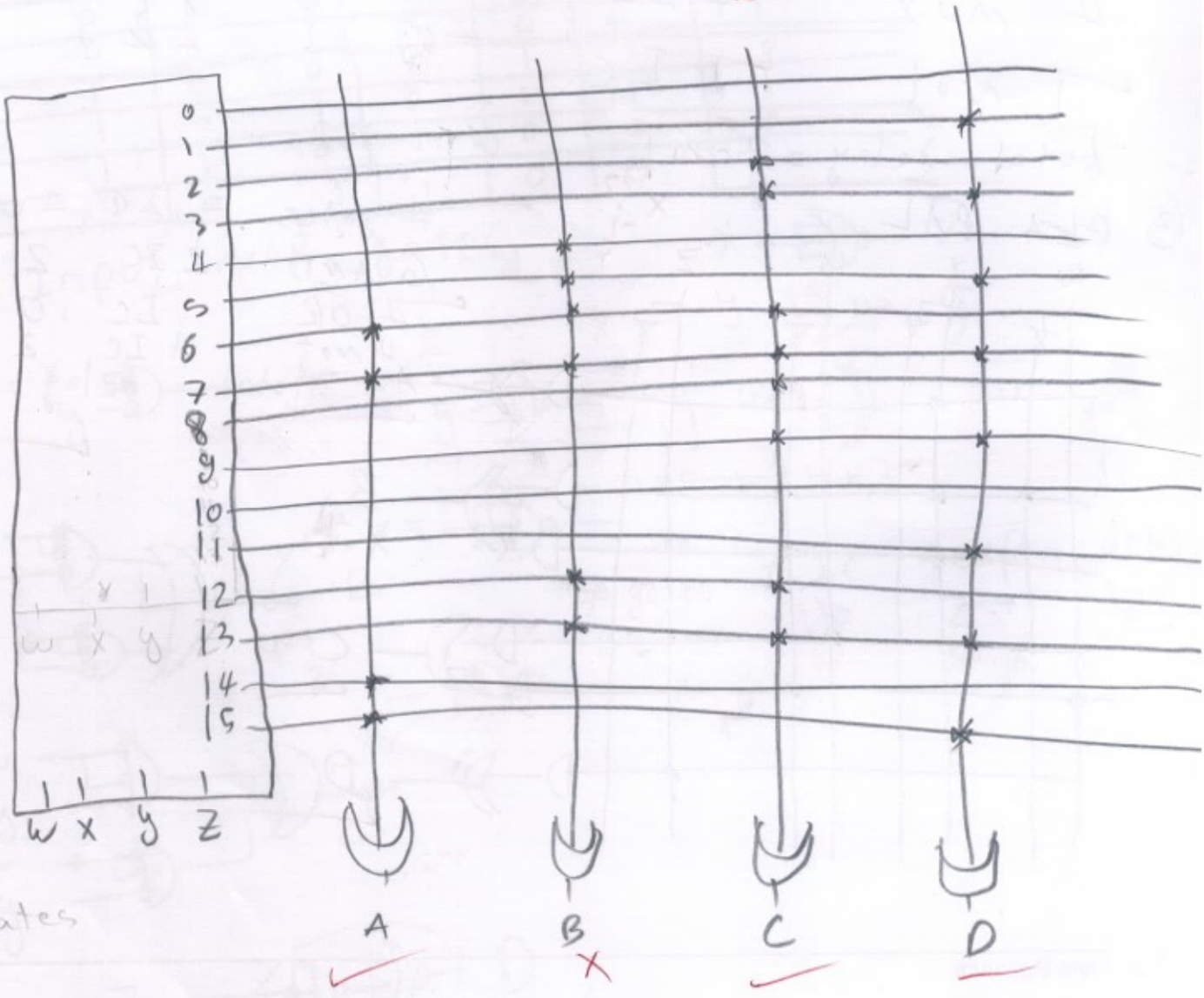
4 Not 1 IC 2

delay

delay = 3



PROM decoder.



gates

# gates	# IC	$ exp	# delay
1 decoder	1	0	3
22 or	6	2	7

total delay = 10

assume decoder 1 IC

Question (2): (5 points)

5

a) Given the Capacity of the following memory units
23M X 16

specify ;

i. Number of address lines
ii. Number of input & output lines
iii. Total Number of words and its width

b) Also, it is required to design a 4 x 6 Memory.

$23M * 16 \quad 23 * 2^{20} > 2^5 * 2^{20} \neq 2^{25}$

(a)

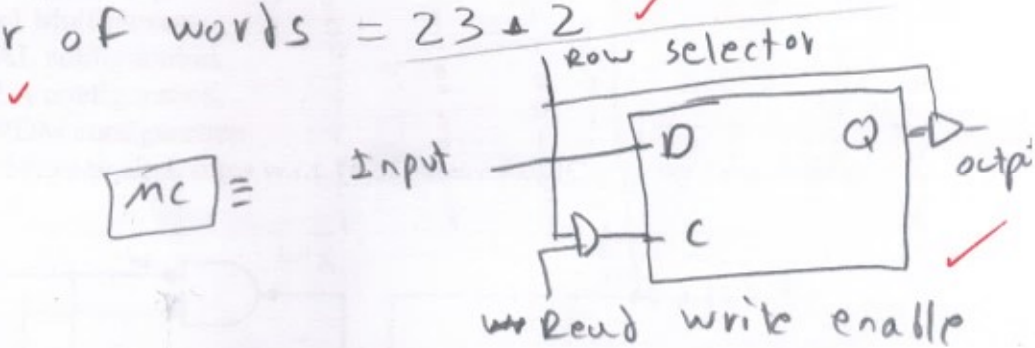
(i) address lines = 25 ✓

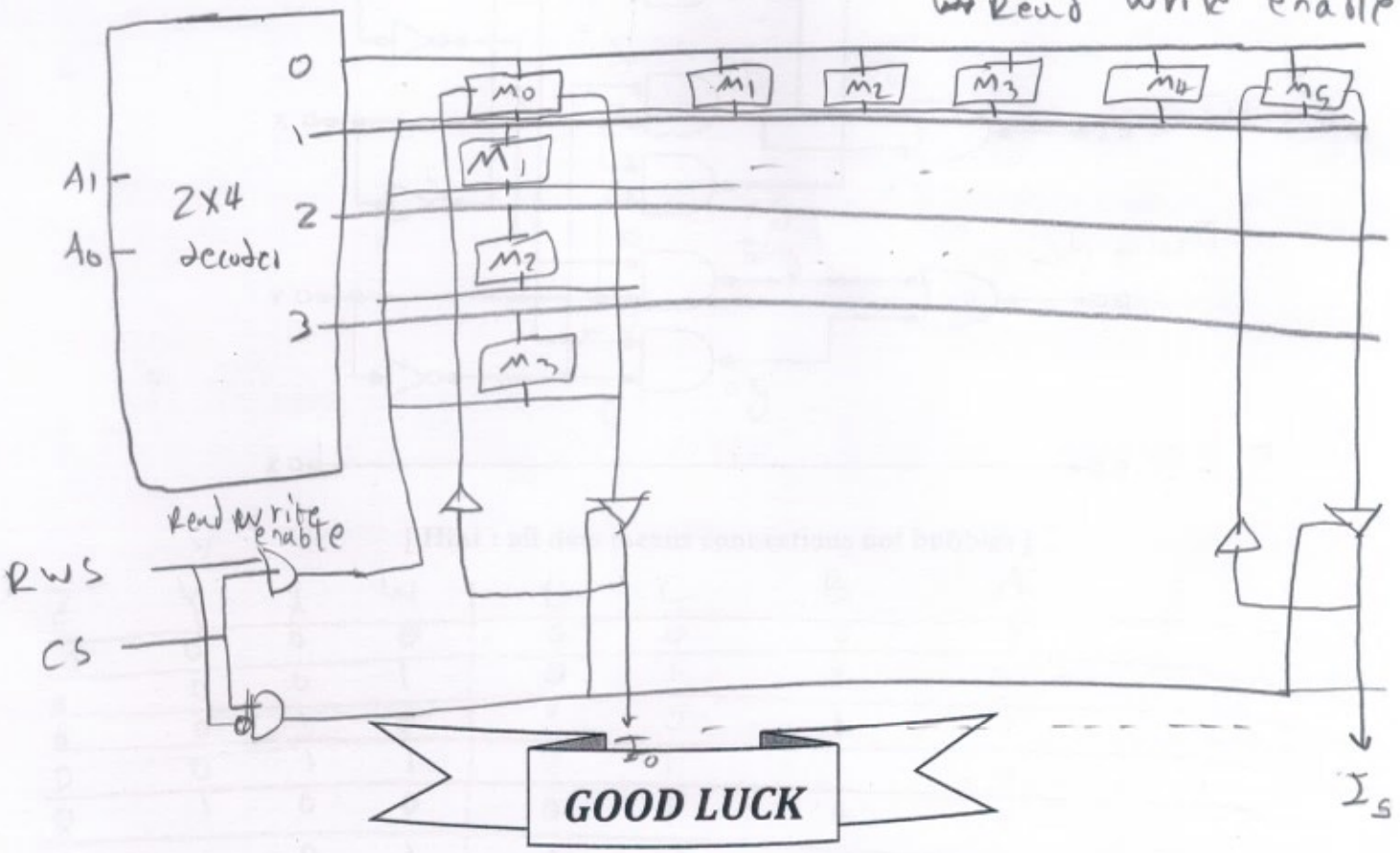
(ii) number of input lines = 16 ✓
number of output lines = 16 ✓

total number of words $= 23 * 2^{20}$ ✓
width = 16 ✓

(b)

MC ≡





GOOD LUCK

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