

# Nova34

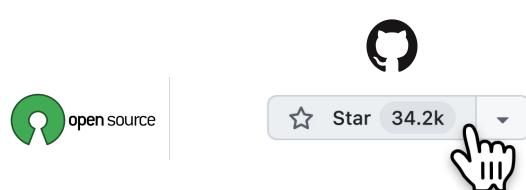
(Nova34 - Reference Board)

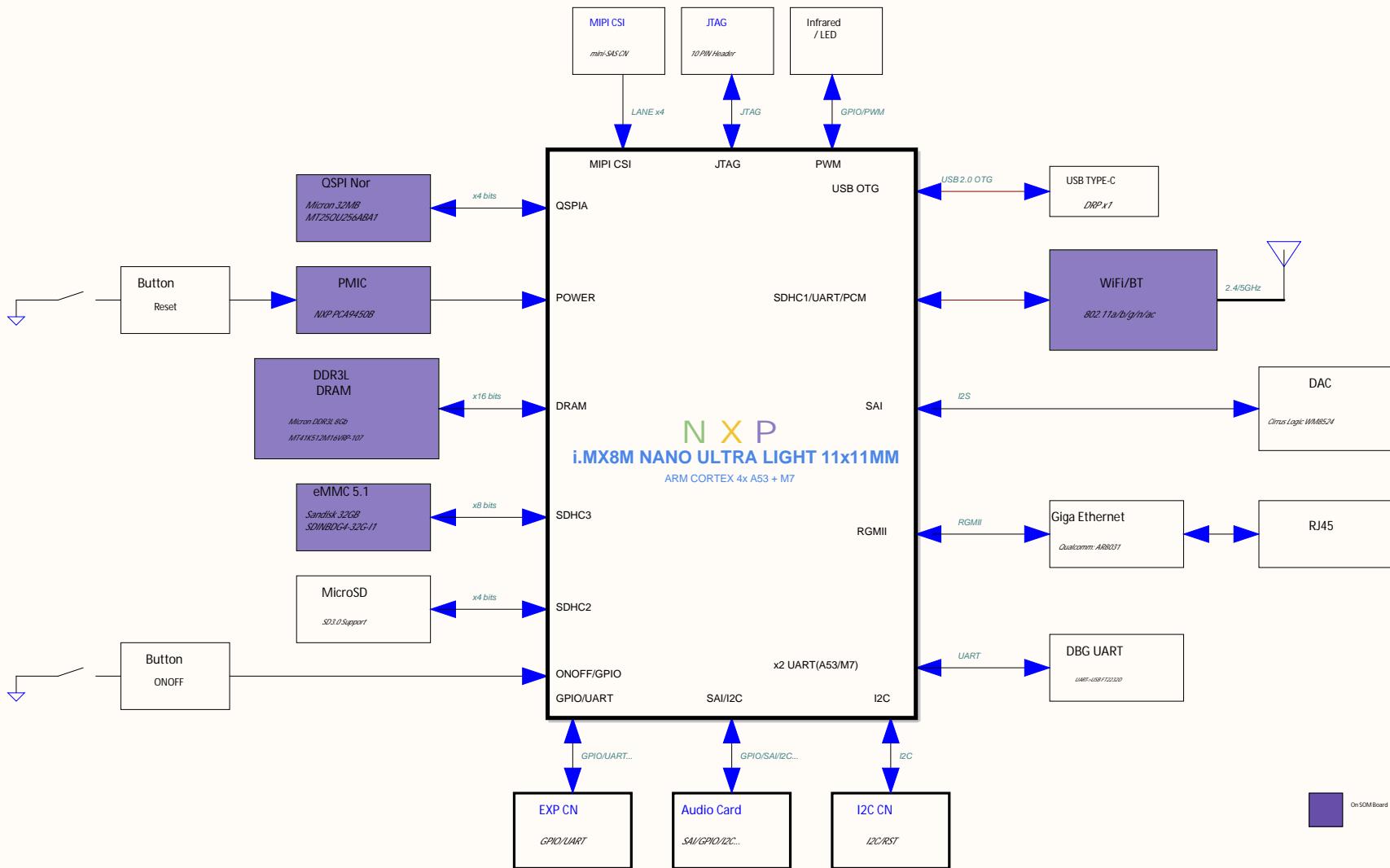
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## Revision History

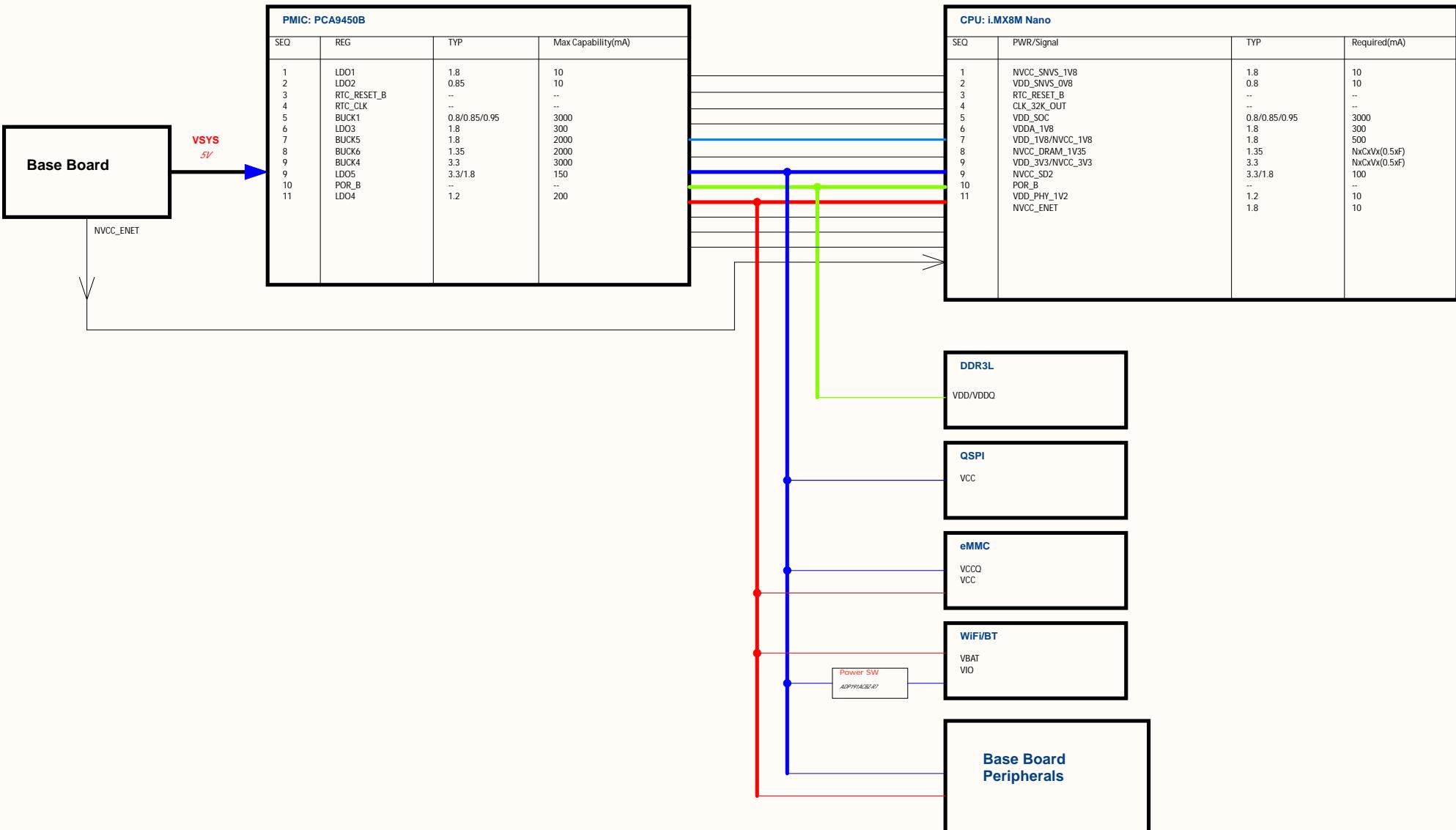
Rev. Code	Date	By	Description
A	2025-01-01	InnovativeBoards	Initial version release



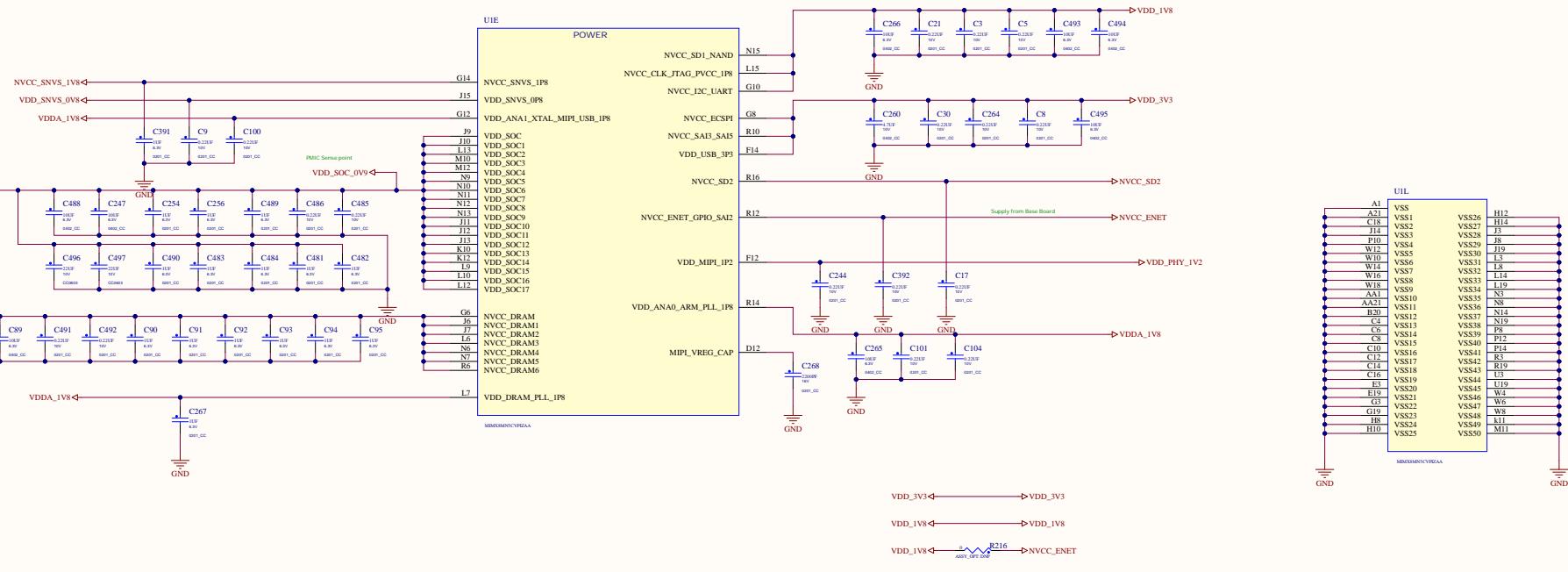


NOVA34		Nova34 - General Purpose Ultra Small Linux Board		
Designer: InnovativeBoards		Drawing Ref: Page 1 of 1		
Drawn by:				
Approved:	Date:	Document Number:	Rev:	

# 8MNANOD3L-EVK PWR TREE

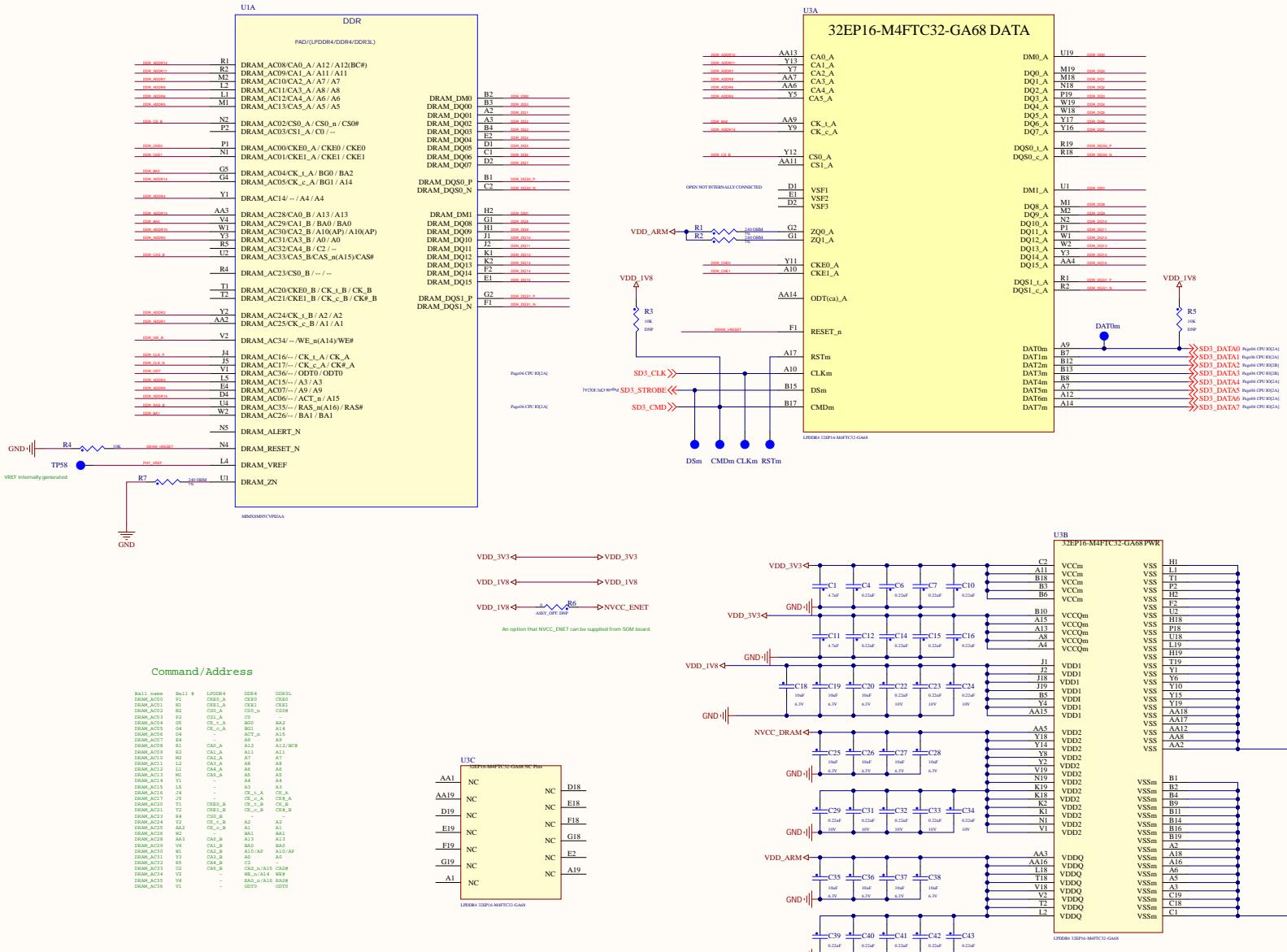


# i.MX8M Nano PWR

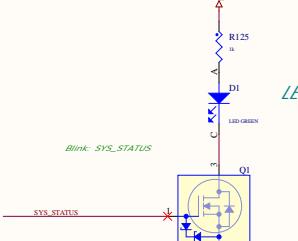
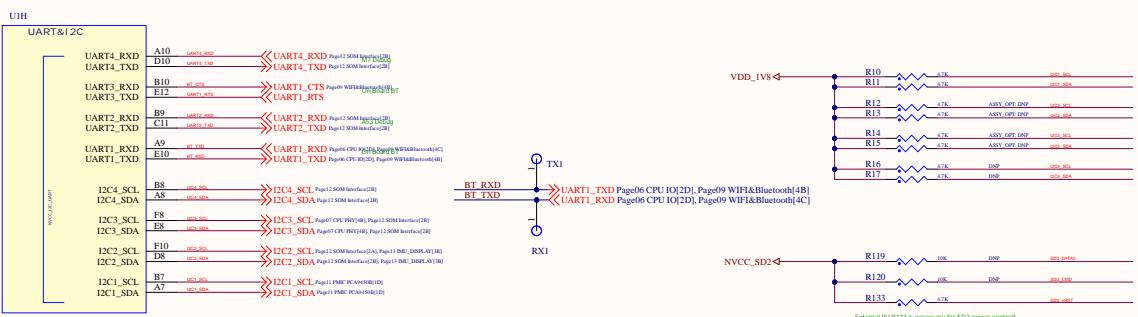
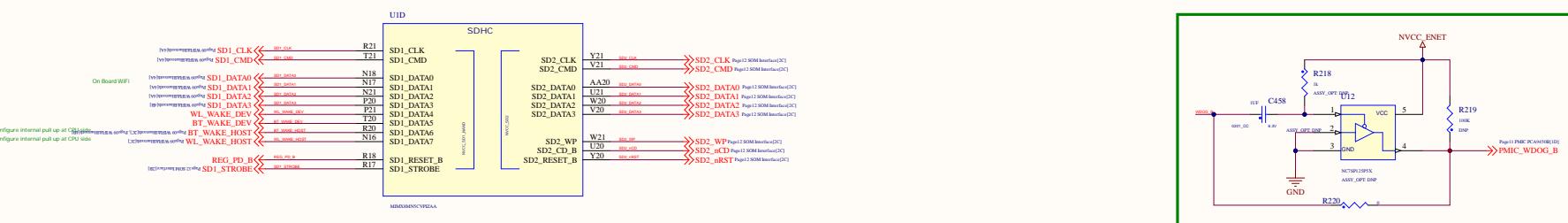
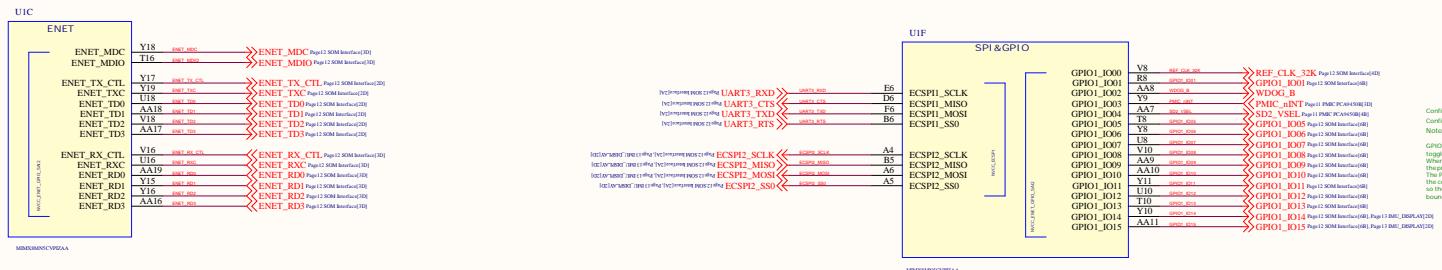
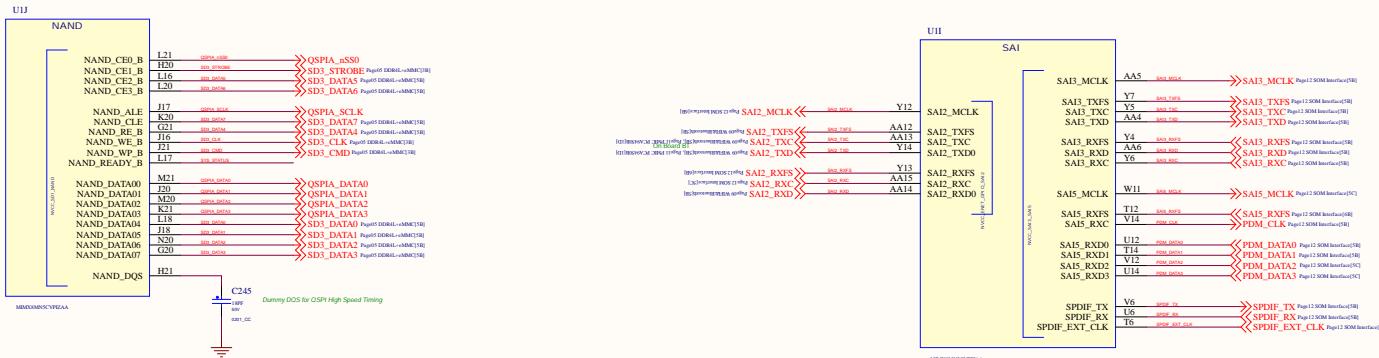


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Design:	Drawing Ref: X-IMXNANOD3L-CPU
Drawn by:	Page Ref: CPU PWR
Approved:	Date: Document Number: Rev: NC SC31-47569 PDF-SPE-47569 A. PLB: -
Date:	Sheet 1 of 10

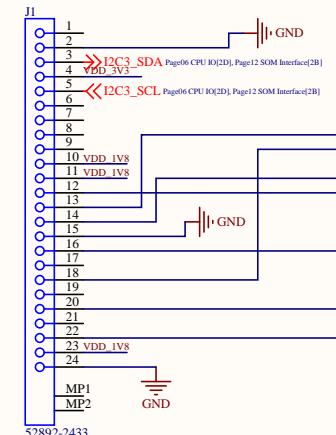
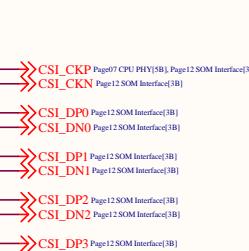
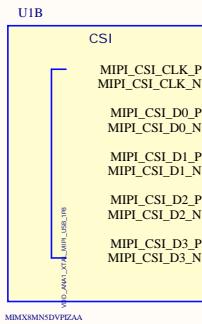
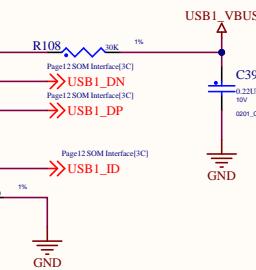
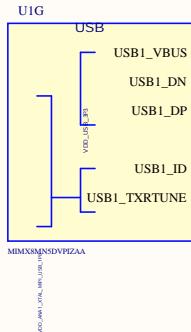
## EPOP LPDDR4X+eMMC



*i.MX8M Nano IO Interface*



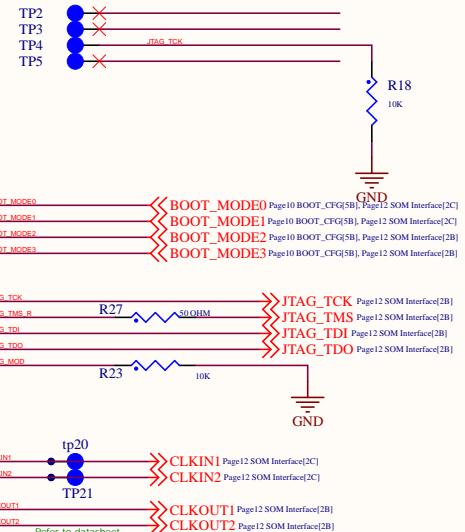
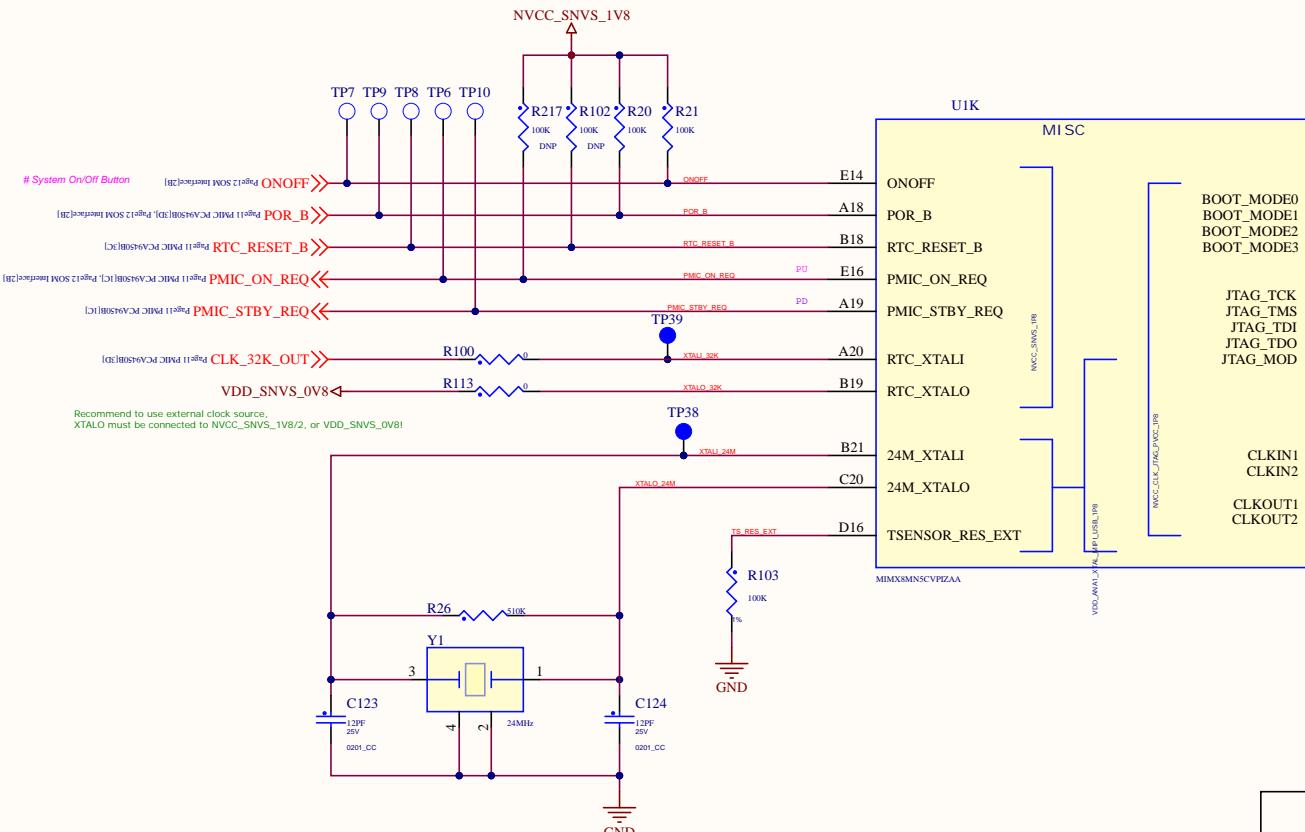
# i.MX8M Nano PHYS



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Drawn by: Vector Cheng	Page Title: <b>CPU PHY</b>
Approved: NC	Size Document Number SCH-47569 PDF: SPP-47569 Rev A2
Date: +	Date: Sheet 7 of 13

# i.MX8M Nano MISC

JTAG Debug



Signal Naming:

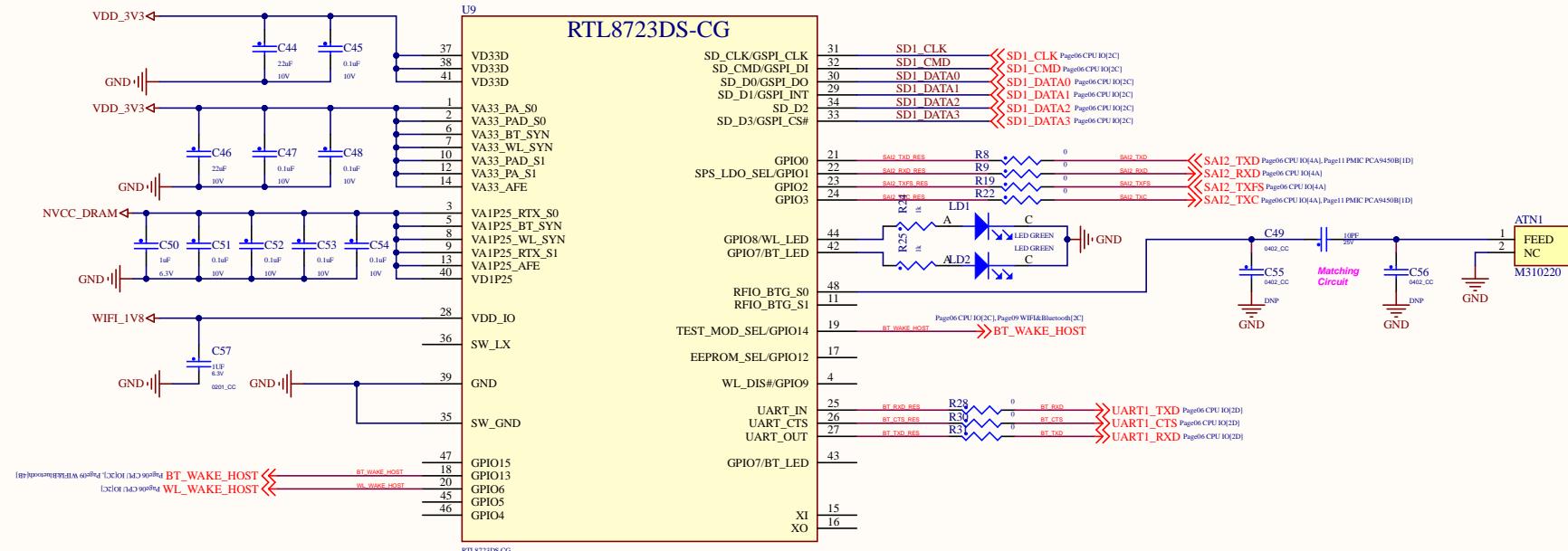
Net Name	i.MX8M Mini	i.MX8M Nano
JTAG_nTRST	JTAG_nTRST	BOOT_MODE2
TEST_MODE	TEST_MODE	BOOT_MODE3

JTAG\_TMS pin must be connected with a 50ohm series resistor near the component if used or fanout.

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ICAP Classification: CP: ___ IUO: ___ PUBL: ___				
Designer: Vector Cheng	Drawing Title: <b>X-8MNANOD3L-CPU</b>			
Drawn by: Vector Cheng	Page Title: <b>CPU MISC</b>			
Approved:	Size NC	Document Number SCH-47569 PDF: SPF-47569		
Date: ____	Rev A2		Sheet 8 of 13	



## 2.4G/5G WIFI/BT Module



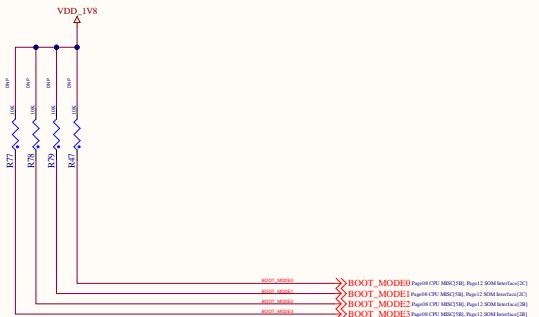
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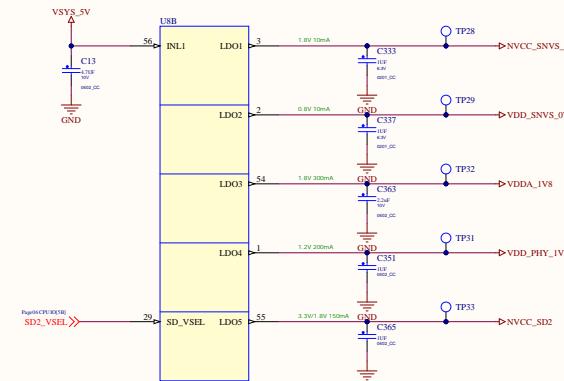
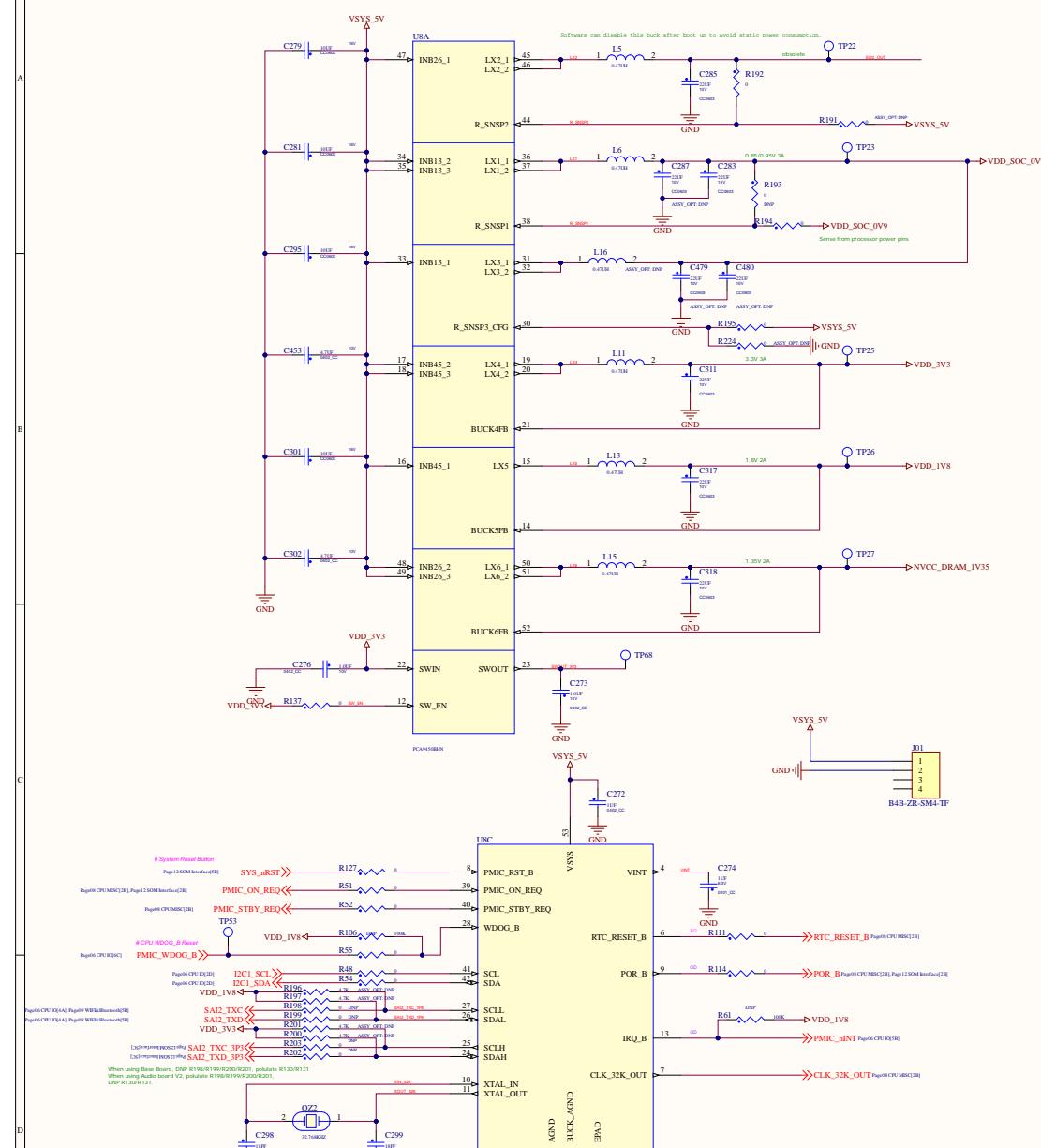
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Drawn by: Vector Cheng	Page Title: WIFI/BT Module			
Approved:	Size NC	Document Number SCH-47569 PDF-SPF-47569	Rev A2	Date: +
				Sheet 15 of 15

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<b>Boot Mode</b>																																																																																															
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<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr><th>BOOT_PIN[3]</th><th>BOOT_PIN[2]</th><th>BOOT_PIN[1]</th><th>BOOT_PIN[0]</th><th>Boot Modes</th></tr> </thead> <tbody> <tr><td><small>BOOT_MODE3 (TEST_MODE)</small></td><td><small>BOOT_MODE2 (JTAG_TRST_B)</small></td><td><small>BOOT_MODE1</small></td><td><small>BOOT_MODE0</small></td><td><small>Function</small></td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Boot From Internal Fuses</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>USB Serial Download</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>USDHC3 (eMMC boot only, SD3 8-bit)</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>USDHC2 (SD boot only, SD2)</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>NAND 8-bit single device 256 page</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>NAND 8-bit single device 512 page</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>QSPI 3B Read</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>QSPI Hyperflash 3.3V</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>eSPI Boot</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Reserved (Boot on I2C connected to BOOT PIN[3:2])</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Infinite Loop Mode</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Test Mode</td></tr> </tbody> </table>						BOOT_PIN[3]	BOOT_PIN[2]	BOOT_PIN[1]	BOOT_PIN[0]	Boot Modes	<small>BOOT_MODE3 (TEST_MODE)</small>	<small>BOOT_MODE2 (JTAG_TRST_B)</small>	<small>BOOT_MODE1</small>	<small>BOOT_MODE0</small>	<small>Function</small>	0	0	0	0	Boot From Internal Fuses	0	0	0	1	USB Serial Download	0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit)	0	0	1	1	USDHC2 (SD boot only, SD2)	0	1	0	0	NAND 8-bit single device 256 page	0	1	0	1	NAND 8-bit single device 512 page	0	1	1	0	QSPI 3B Read	0	1	1	1	QSPI Hyperflash 3.3V	1	0	0	0	eSPI Boot	1	0	0	1	Reserved	1	0	1	0	Reserved	1	0	1	1	Reserved	1	1	0	0	Reserved (Boot on I2C connected to BOOT PIN[3:2])	1	1	0	1	Reserved	1	1	1	0	Infinite Loop Mode	1	1	1	1	Test Mode
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 <p><b>Note:</b></p> <p>1. <small>BOOT_MODE0</small> J-signal are used for boot selections</p> <p>2. <small>BOOT_MODE</small> signals have internal ID before and after POR_B reset is asserted</p> <p>3. When using Board for Multi-boot selection, you must keep the resistors DNP on SCM board!</p>																																																																																															
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# SYS PMIC

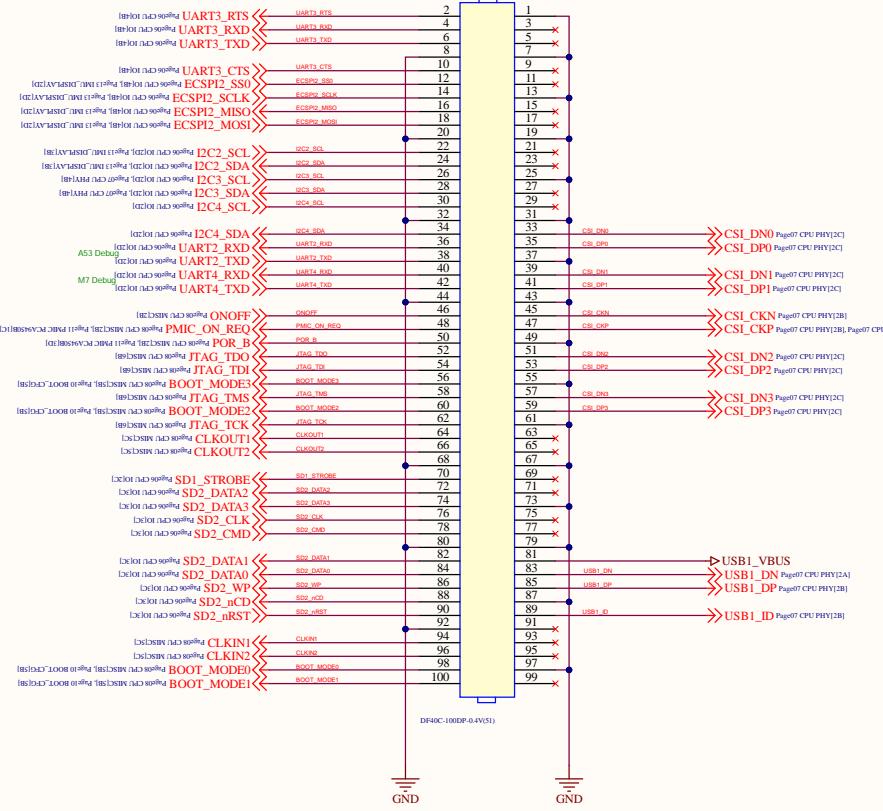


i.MX8M Nano DDR3L EVK Power Sequence						
SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.62	1.8	1.98	10
2	VDD_SNVS_0V8	LDO2	0.76	0.8	0.9	10
3	RTC_RESET_B	RTC_RESET_B	--	--	--	--
4	CLK_32K_OUT	RTC_CLK	--	--	--	--
5	VDD_SOC_0V9	BUCK1	0.76/0.805/0.9	0.8/0.85/0.95	0.9/0.95/1.0	3000
6	VDDA_1V8	LDO3	1.71	1.8	1.89	300
7	VDD_1V8/NVCC_1V8	BUCK5	1.65	1.8	1.95	2000
8	NVCC_DRAM_1V35	BUCK6	1.283	1.35	1.417	2000
9	VDD_3V3/NVCC_3V3	BUCK4	3	3.3	3.6	3000
10	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
11	POR_B	POR_B	--	--	--	--
	VDD_PHY_1V2	LDO4	1.14	1.2	1.26	200

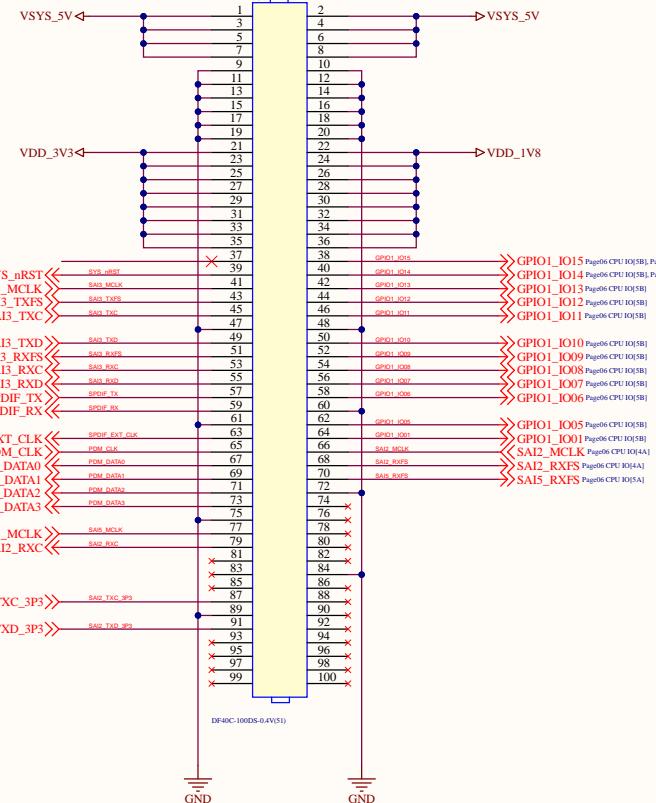
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Drawn by:	Wenlong	Page Title:
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	NC	SC847549-PB1-SPP-47549
Date:	Rev:	10
		Sheet 10 of 10

## B2B Connector for CPU Board

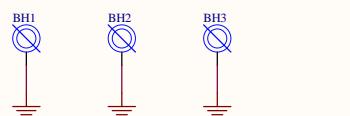
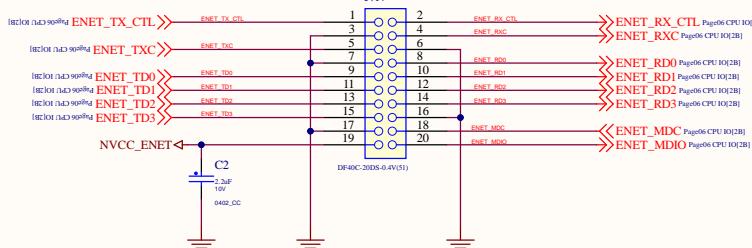
### Header



### Receptacle



### Receptacle



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Drawn by: Vector Cheng	Page Title: SOM Interface
Approved: NC	Document Number: SCH-4756 PDF: SPP-47569

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B

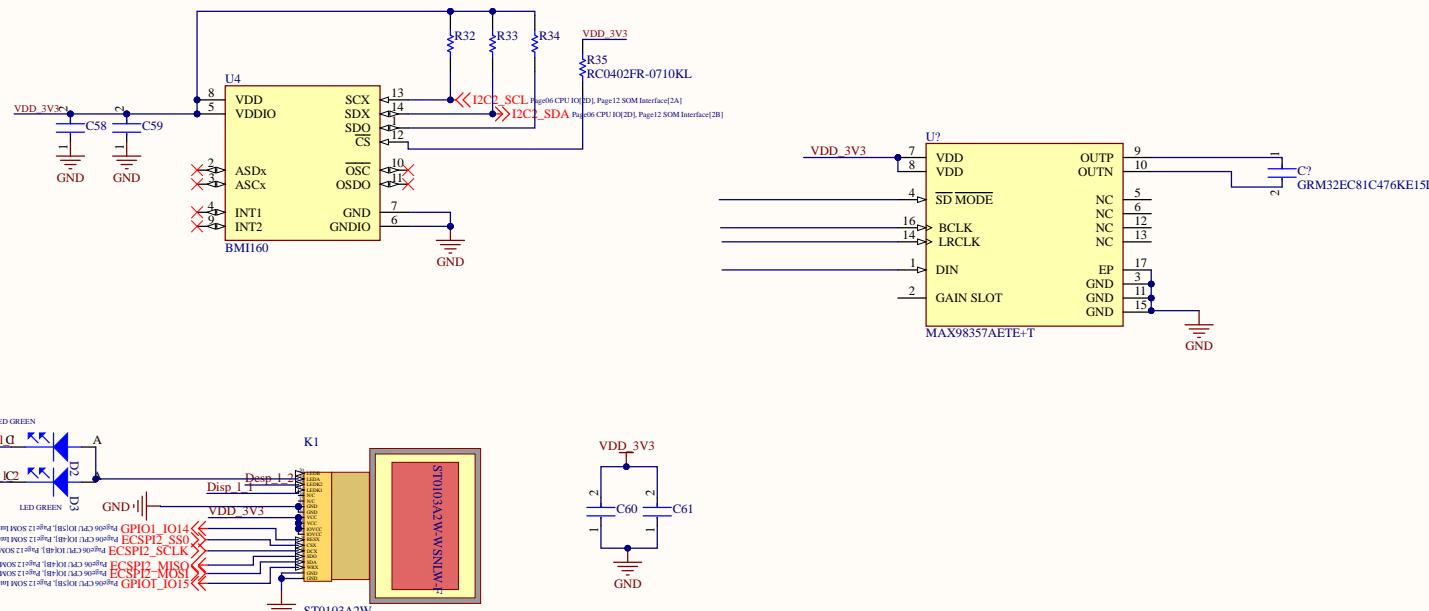
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C

C

D

D



Title		
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