8MNANOD3L-CPU

(i.MX8M Nano Reference Board)

Table of Content

Revision History

Rev. Code	Date	By	Description
A	2020-08-12	Vector	Initial version release
A1	2021-01-08	Vector	Remove CPU socket.
A2	2022-03-02	Vector	Remove WDOG note for ROHM PMIC.

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:

   _B Denotes - Active-Low Signal

   <> or [] Denotes - Vectored Signals

4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

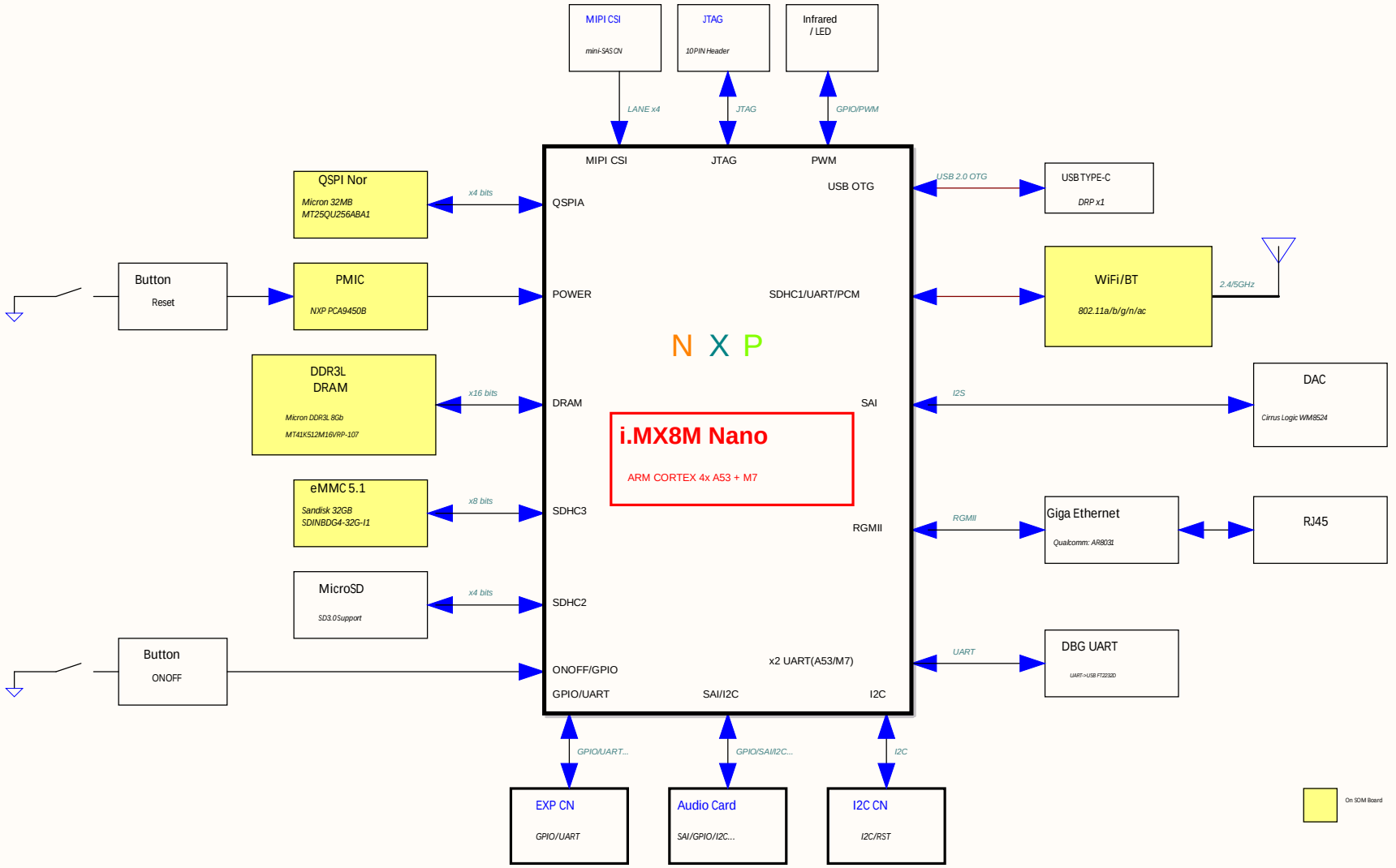
Microcontroller Product Group

6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: ___ IUO: _X_ PUBI: ___

Designer: Vector Cheng	Drawing Title: X-8MNANOD3L-CPU	
Drawn by: Vector Cheng	Page Title: Title and Rev History	
Approved:	Size: NC	Document Number: SCH-47569 PDF: SR-47569 Rev: A2
	Date: -	Sheet 1 of 13

8MNANOD3L-EVK Block Diagram



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Designer: Vector Cheng	Drawing Title: X-8MNANOD3LCPU
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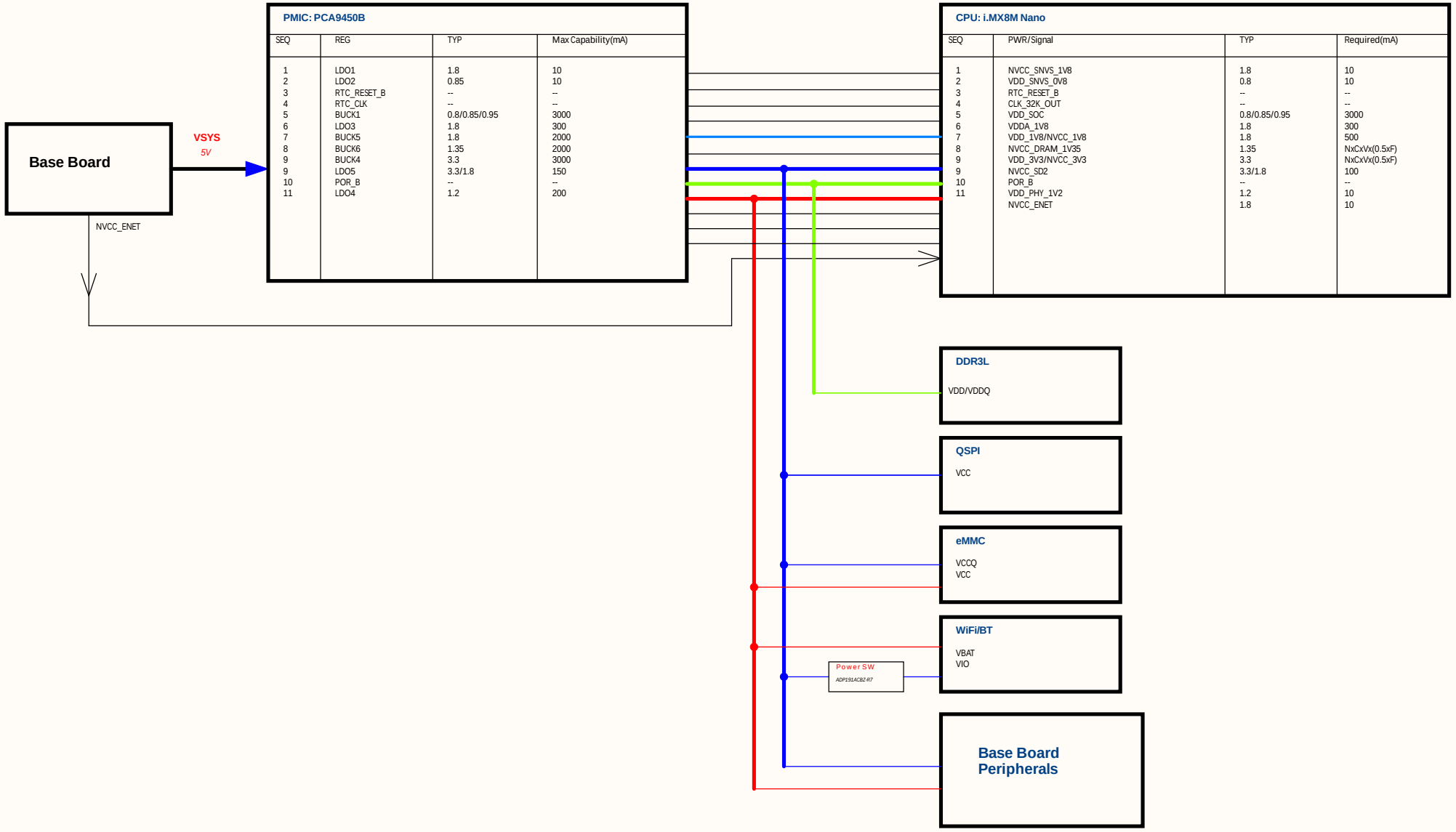
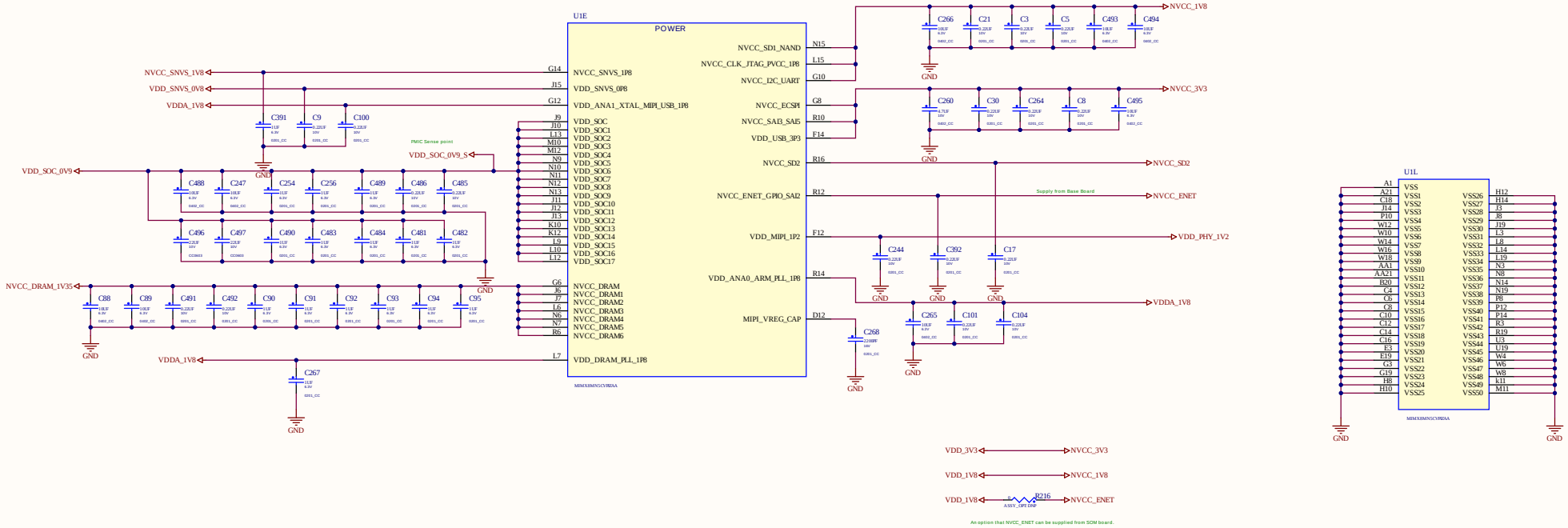
8MNANOD3L-EVK PWR TREE



i.MX8M Nano PWR



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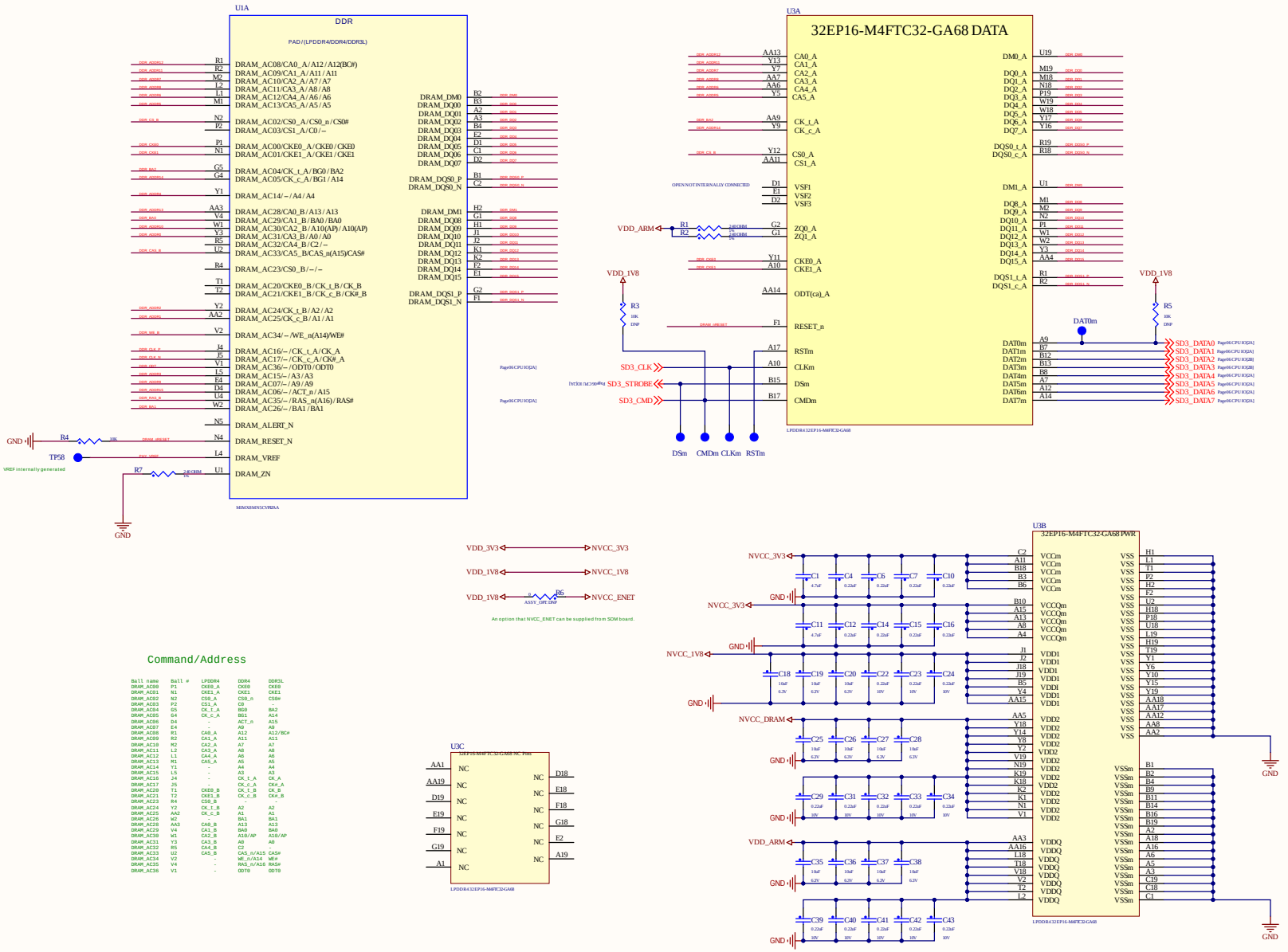
DDR4+eMMC



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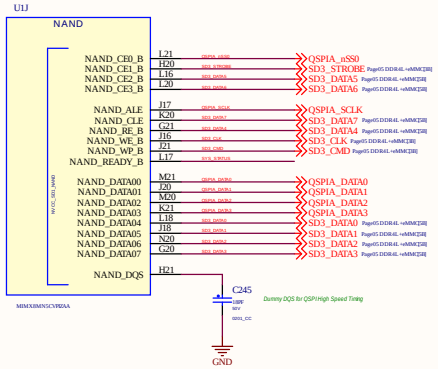
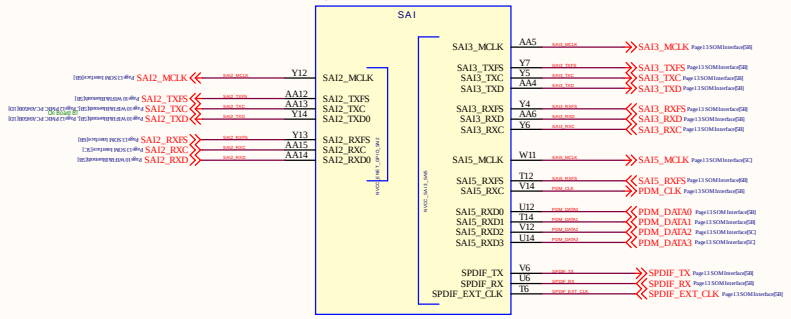
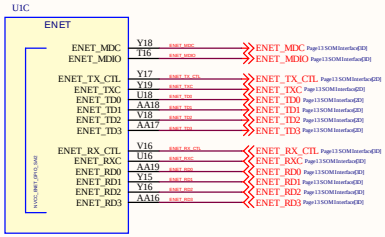
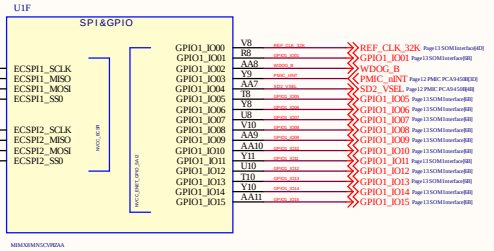
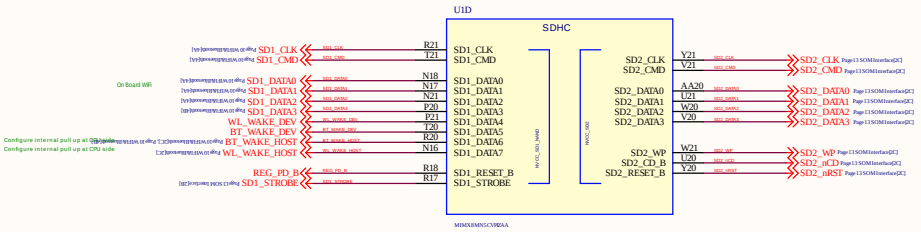
i.MX8M Nano IO Interface

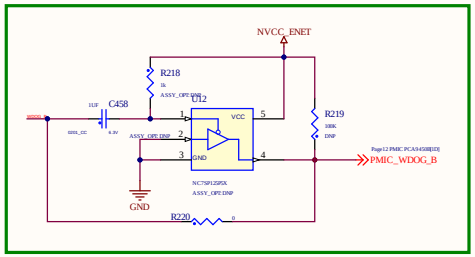


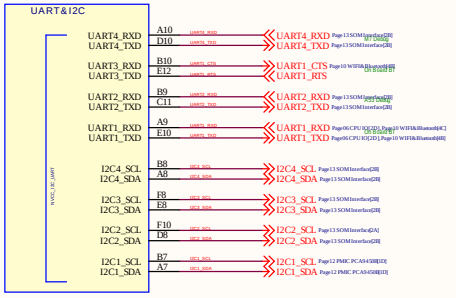


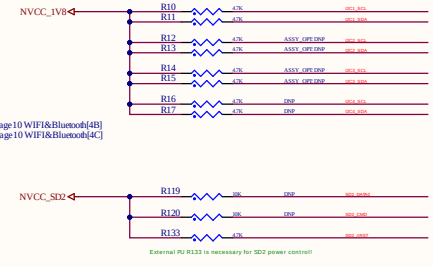


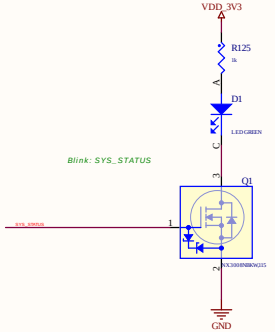












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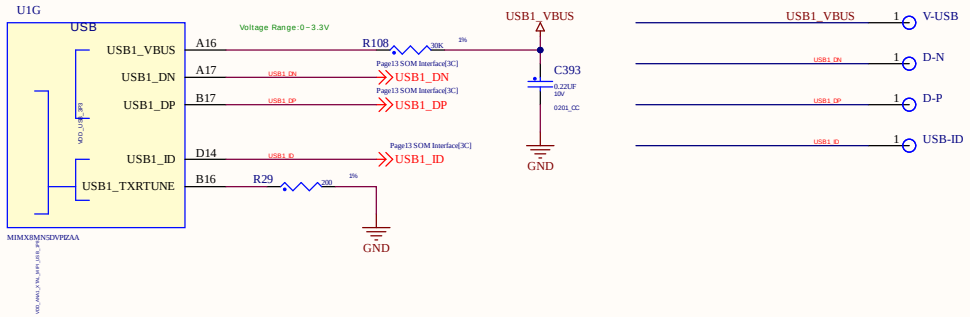
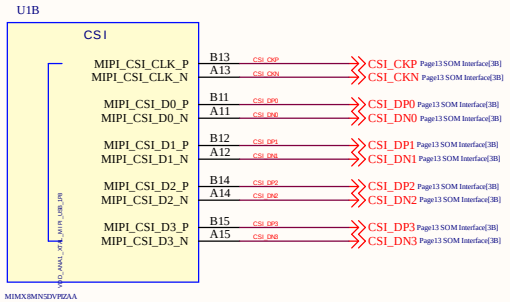
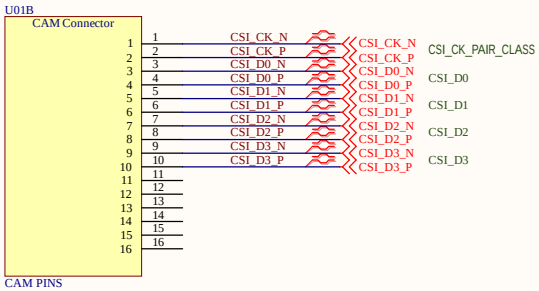
Designer: Vector Cheng	Drawing Title: X-8MNANOD3L-CPU
Drawn by: Vector Cheng	Page Title: CPU IO
Approved:	Size: NC; Document Number: SCH-47569 PDF-SR-47569; Rev: A2
	Date: -; Sheet: * of **

i.MX8M Nano PHYs







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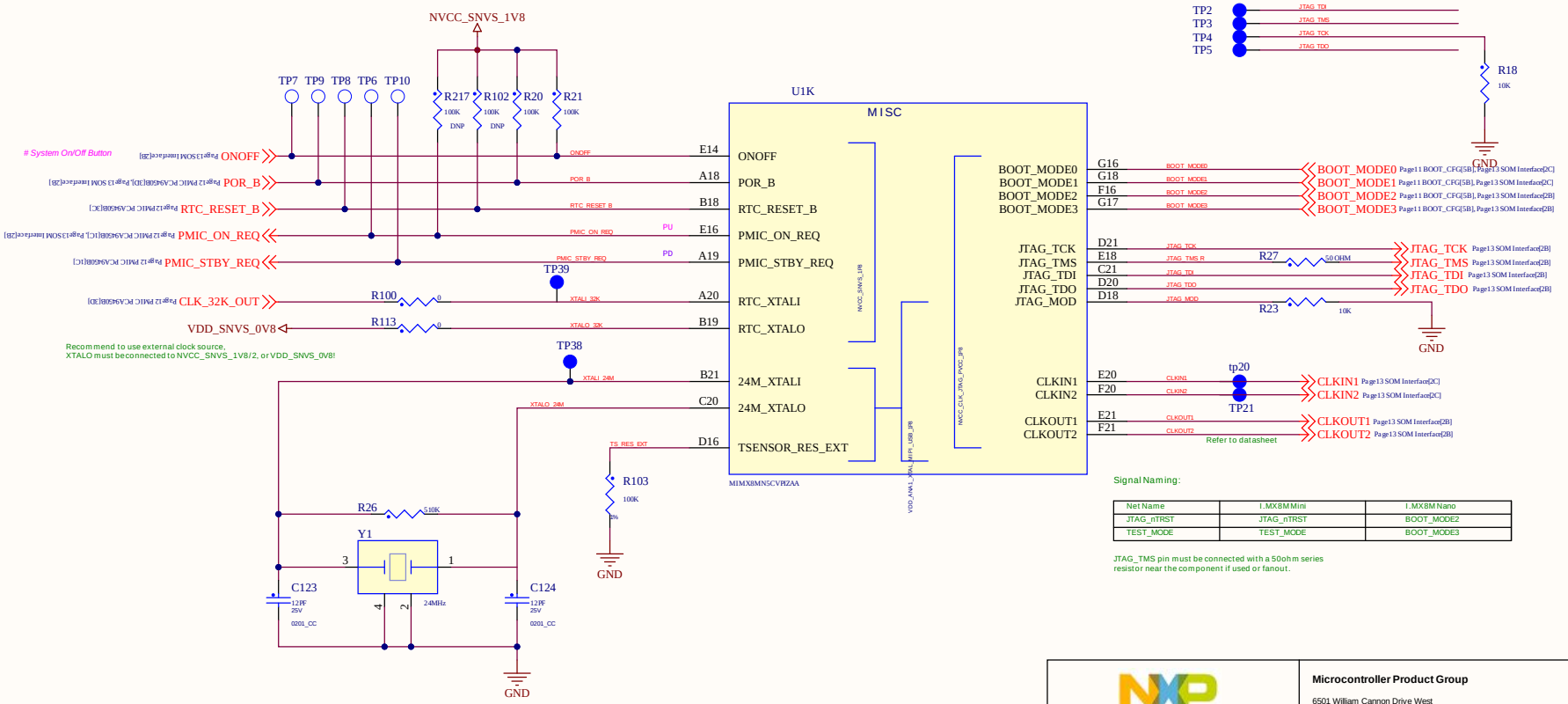
Approved:	Size: NC Document Number: SCH-47569 PDF: SPF-47569	Rev: A2
	Date: -	Sheet 7 of 13

i.MX8M Nano MISC



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Drawn by: Vector Chang	Page Title: **eMMC/QSPI**	
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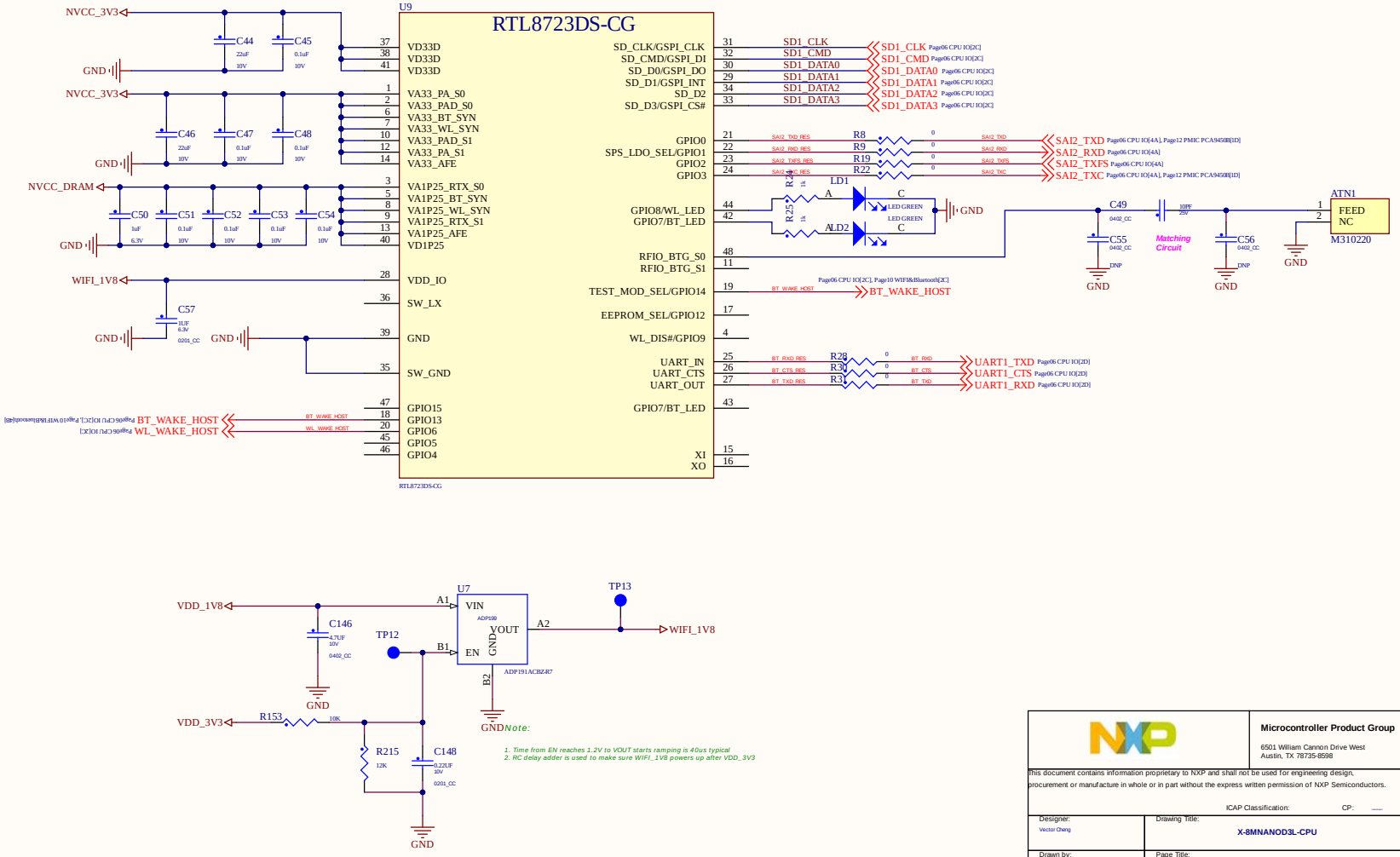
2.4G/5G WIFI/BT Module



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	Date: -; Sheet 10 of 13

Boot Mode

i.MX8M Nano Boot Mode

BOOT_PIN[3]	BOOT_PIN[2]	BOOT_PIN[1]	BOOT_PIN[0]	Boot Modes
BOOT_MODE3 (TEST_MODE)	BOOT_MODE2 (JTAG_TRST_B)	BOOT_MODE1	BOOT_MODE0	Function
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit)
0	0	1	1	USDHC2 (SD boot only, SD2)
0	1	0	0	NAND 8-bit single device 256 page
0	1	0	1	NAND 8-bit single device 512 page
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ecSPI Boot
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved (Boot on I2C connected to BOOT PIN[3:2])
1	1	0	1	Reserved
1	1	1	0	Infinite Loop Mode
1	1	1	1	Test Mode

Note:

1. BOOT_MODE0 -3 singals are used for boot selections

2. BOOT_MODE singals have internal PD before and after POR_B reset is deasserted!

3. When using Base Board for Multi boot selection, you must keep the resistors DNP on SOM board!

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Drawn by: Vector Cheng	Page Title: BOOT_CFG
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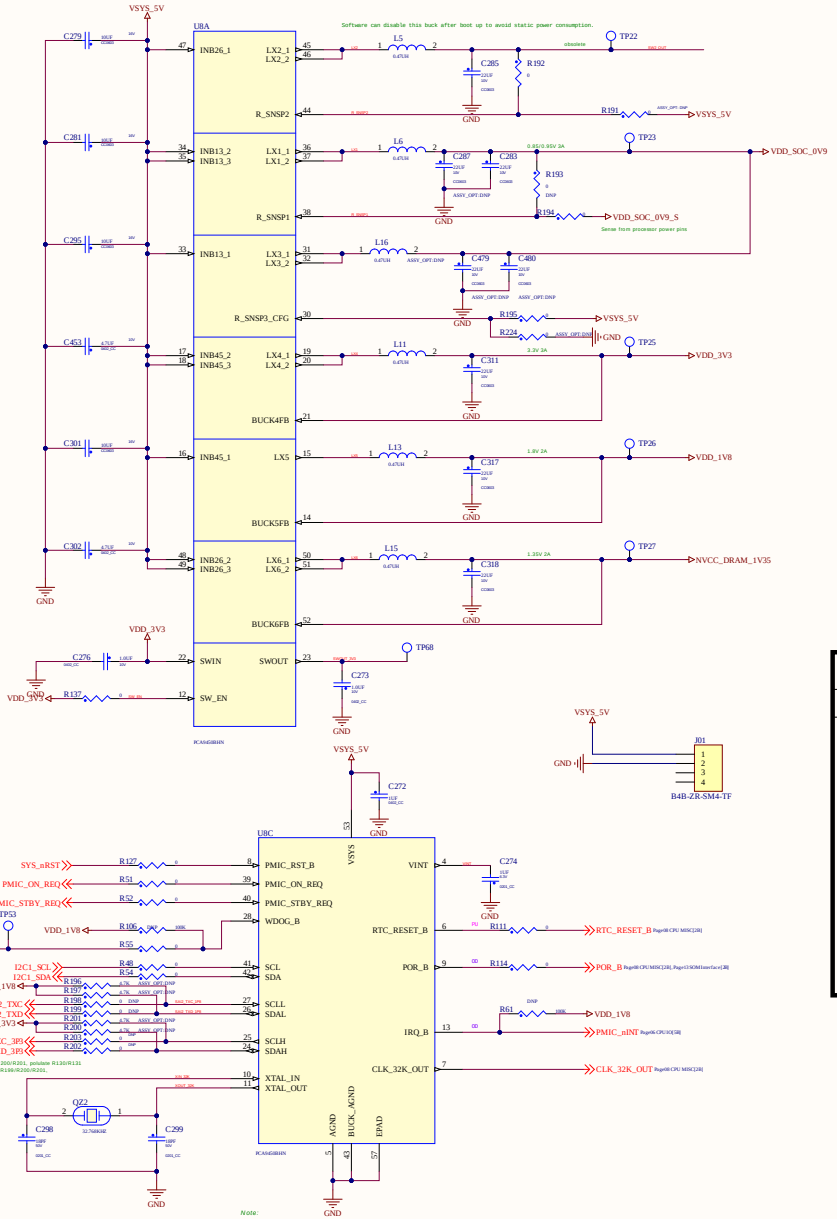
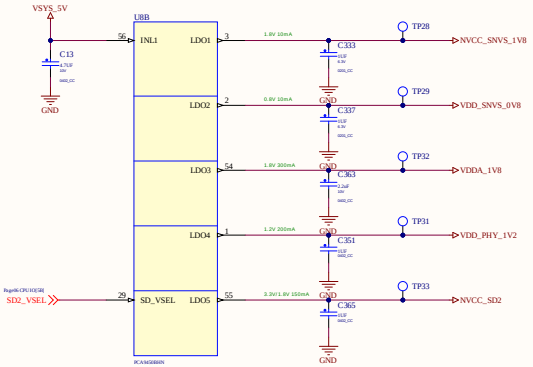
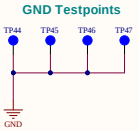
	Date: - / Sheet: 31 of 43

SYS PMIC







i.MX8M Nano DDR3L EVK Power Sequence

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.62	1.8	1.98	10
2	VDD_SNVS_0V8	LDO2	0.76	0.8	0.9	10
3	RTC_RESET_B	RTC_RESET_B	--	--	--	--
4	CLK_32K_OUT	RTC_CLK	--	--	--	--
5	VDD_SOC_0V9	BUCK1	0.76/0.805/0.9	0.8/0.85/0.95	0.9/0.95/1.0	3000
6	VDDA_1V8	LDO3	1.71	1.8	1.89	300
7	VDD_1V8/NVCC_1V8	BUCK5	1.65	1.8	1.95	2000
8	NVCC_DRAM_1V35	BUCK6	1.283	1.35	1.417	2000
9	VDD_3V3/NVCC_3V3	BUCK4	3	3.3	3.6	3000
9	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
10	POR_B	POR_B	--	--	--	--
11	VDD_PHY_1V2	LDO4	1.14	1.2	1.26	200

Note:

1. WDOG_B is used as Cold Reset, external pull up is needed. On EVK, R106 is not necessary, since WDOG_B/GPIO1_IO02 of CPU has internal pull up.
2. PMIC_nINT is open drain output, external pull up is needed. On EVK, R61 is not necessary, since PMIC_nINT/GPIO1_IO03 of CPU has internal pull up.
3. AGND/BUCK_AGND should be connected to ground plane through Via. Do not short to EP directly on top layer

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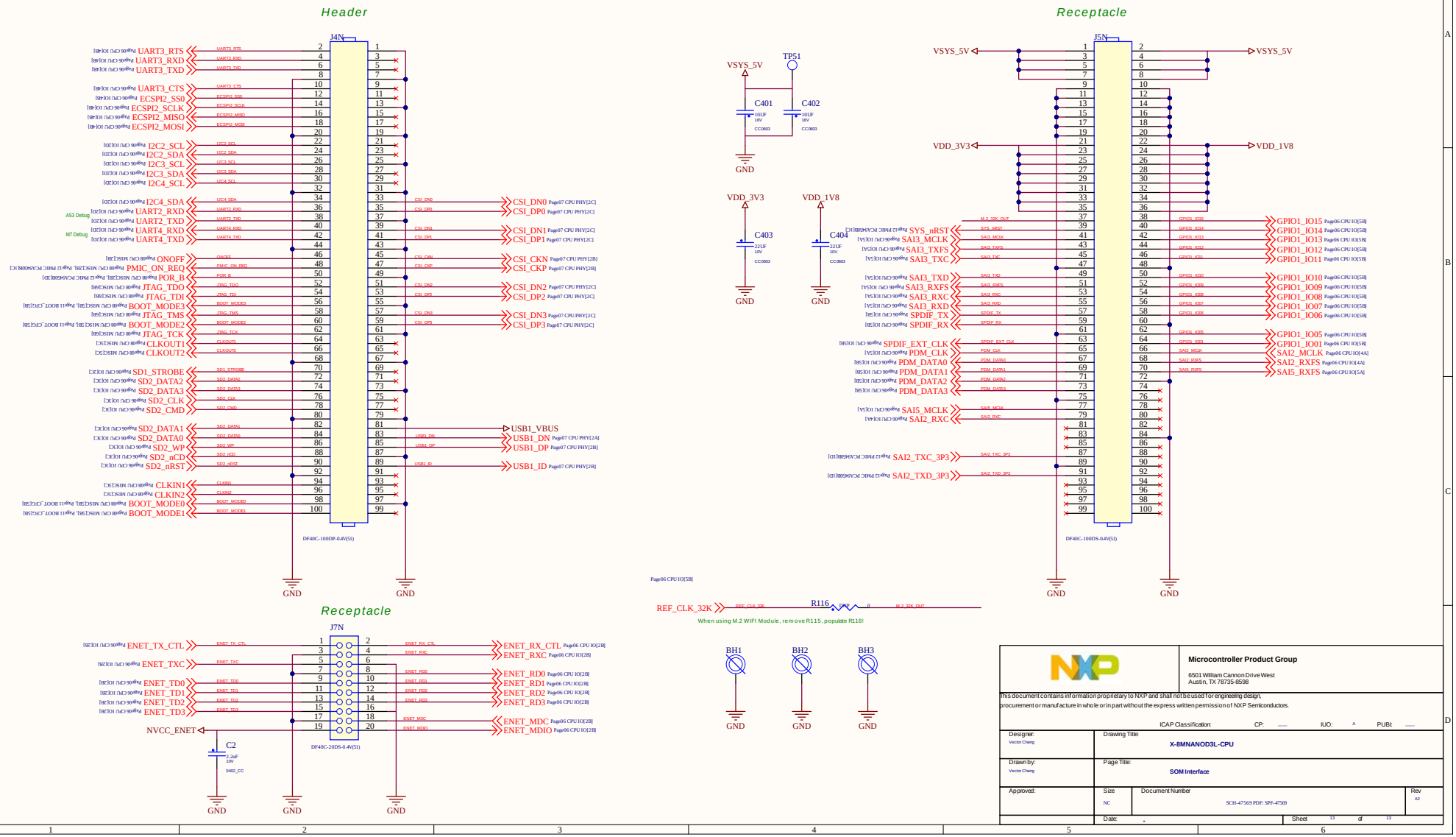
B2B Connector for CPU Board



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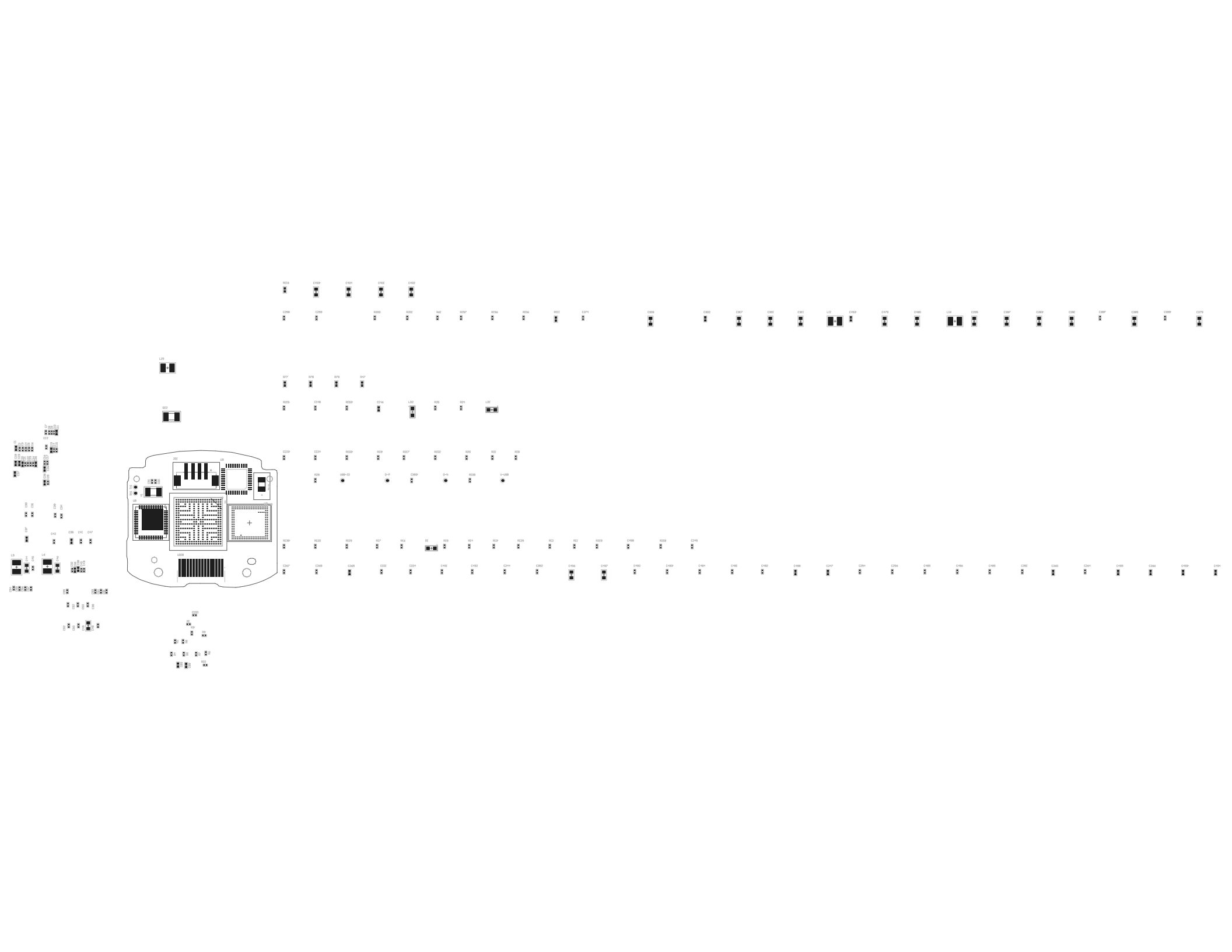

Board Stack Report