

8MNANOD3L-CPU

(i.MX8M Nano Reference Board)

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Revision History


Rev. Code	Date	By	Description
A	2020-08-12	Vector	Initial version release
A1	2021-01-08	Vector	Remove CPU socket.
A2	2022-03-02	Vector	Remove WDOG note for RCHM PMIC.

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.
2. Device type number is for reference only. The number varies with the manufacturer.
3. Special signal usage:
 _B Denotes -Active-Low Signal
 < or / Denotes - Vectored Signals
4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

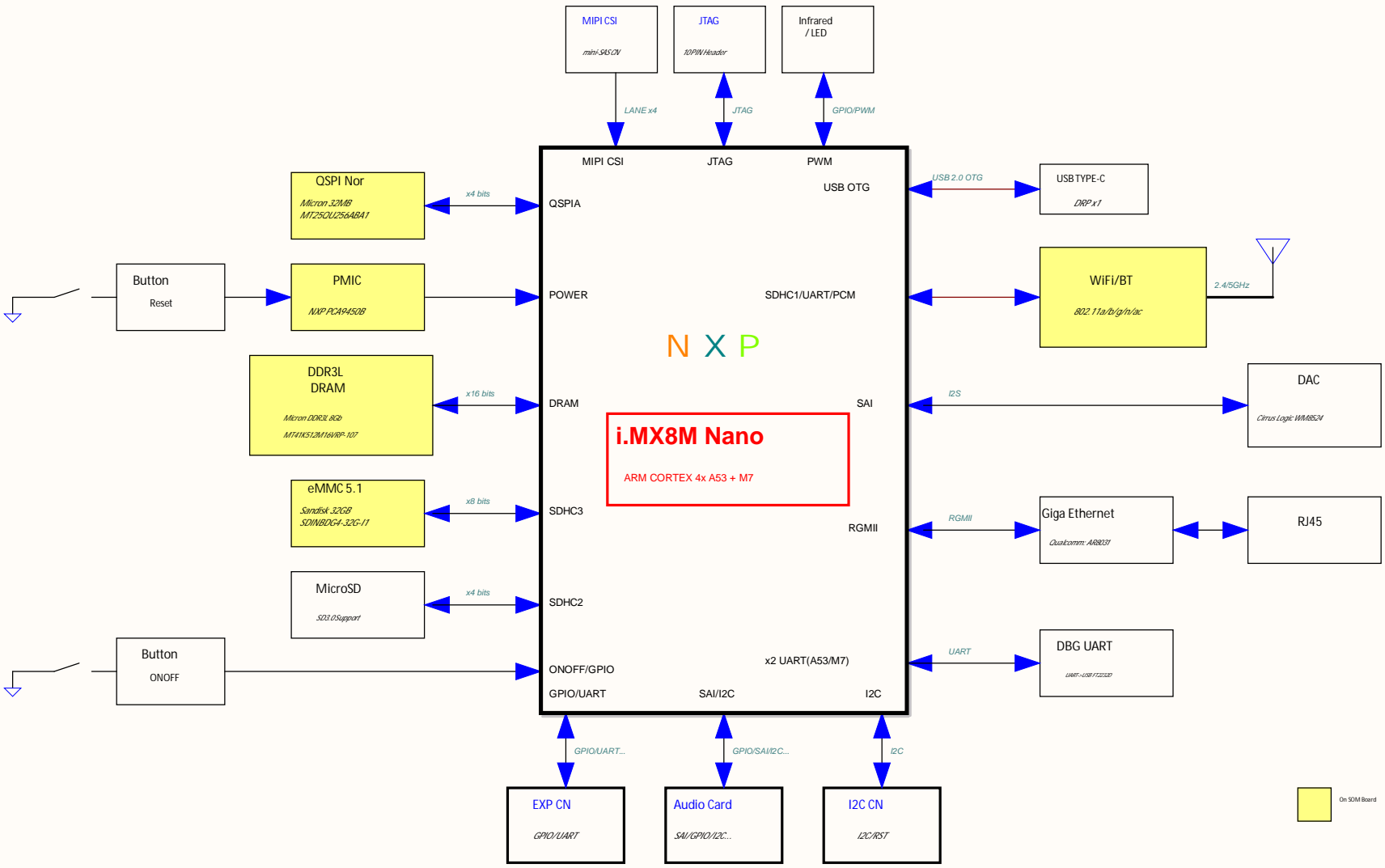
Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

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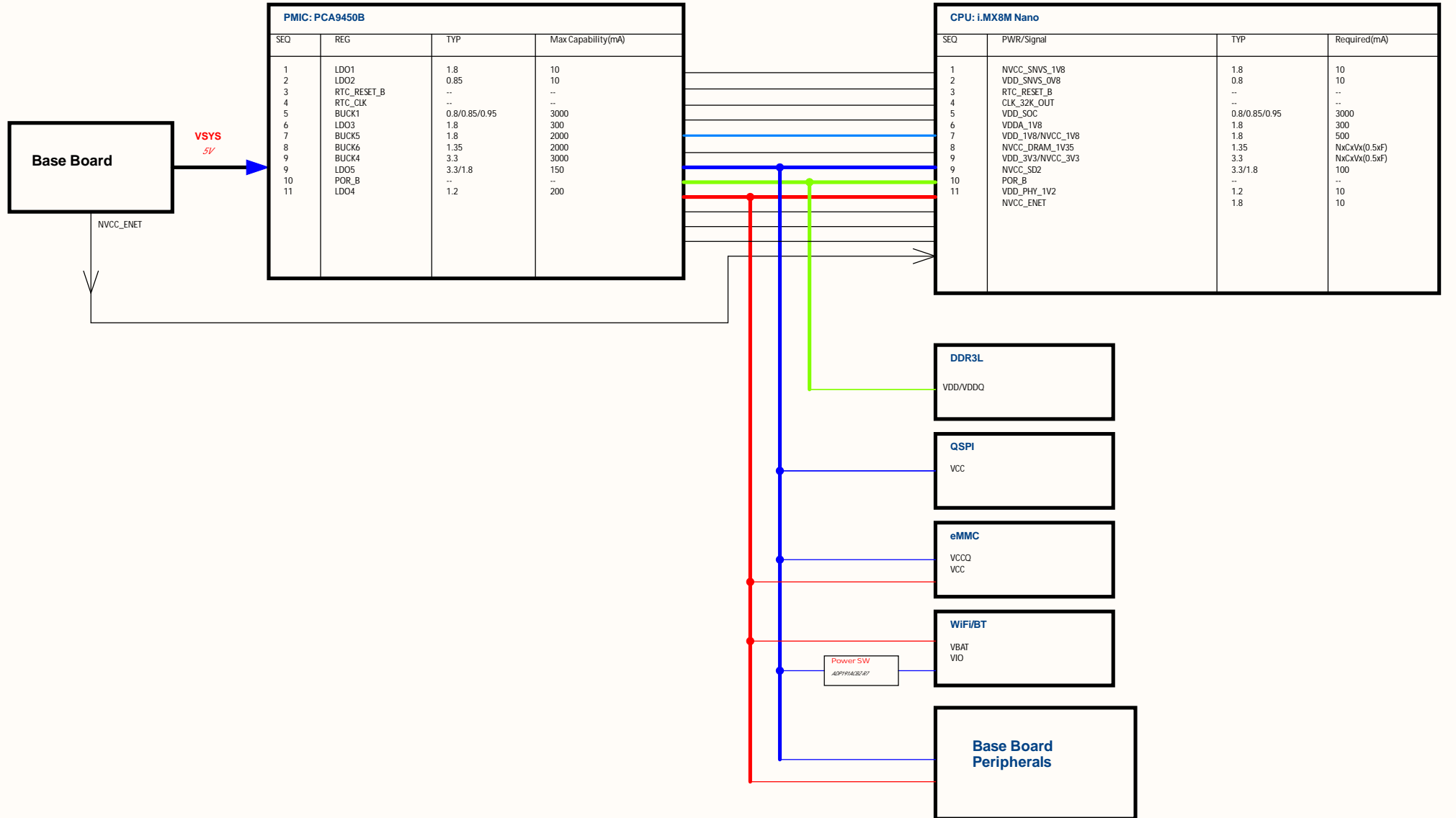
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Drawn by <small>name (line)</small>		Page Title: Title and Rev History	
Approved <small>signature</small>		Date <small>MM DD YY</small> Document Number 6578-47149 PDF 08-4750	
Author <small>name (line)</small>		Scale <small>1:1</small>	

8MNANOD3L-EVK Block Diagram



On SOM Board

8MNANOD3L-EVK PWR TREE





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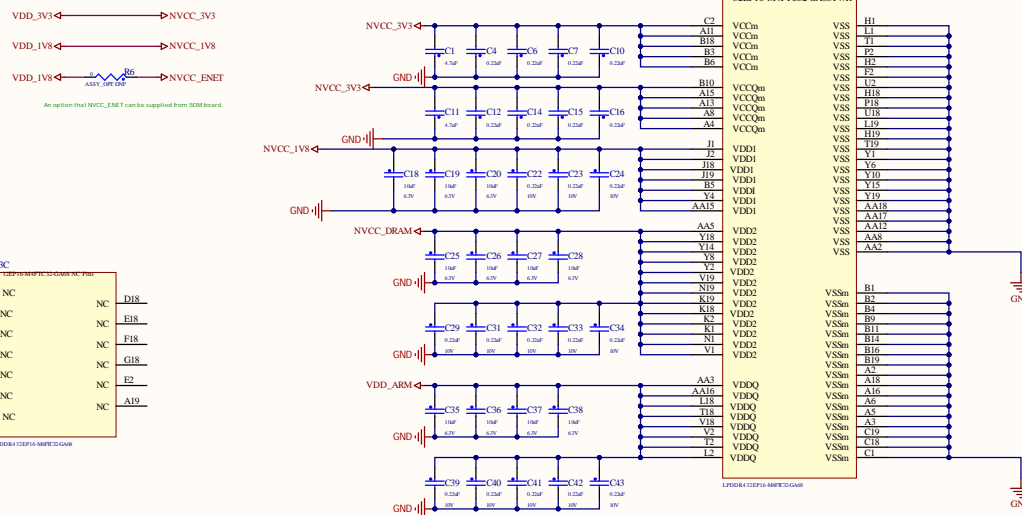
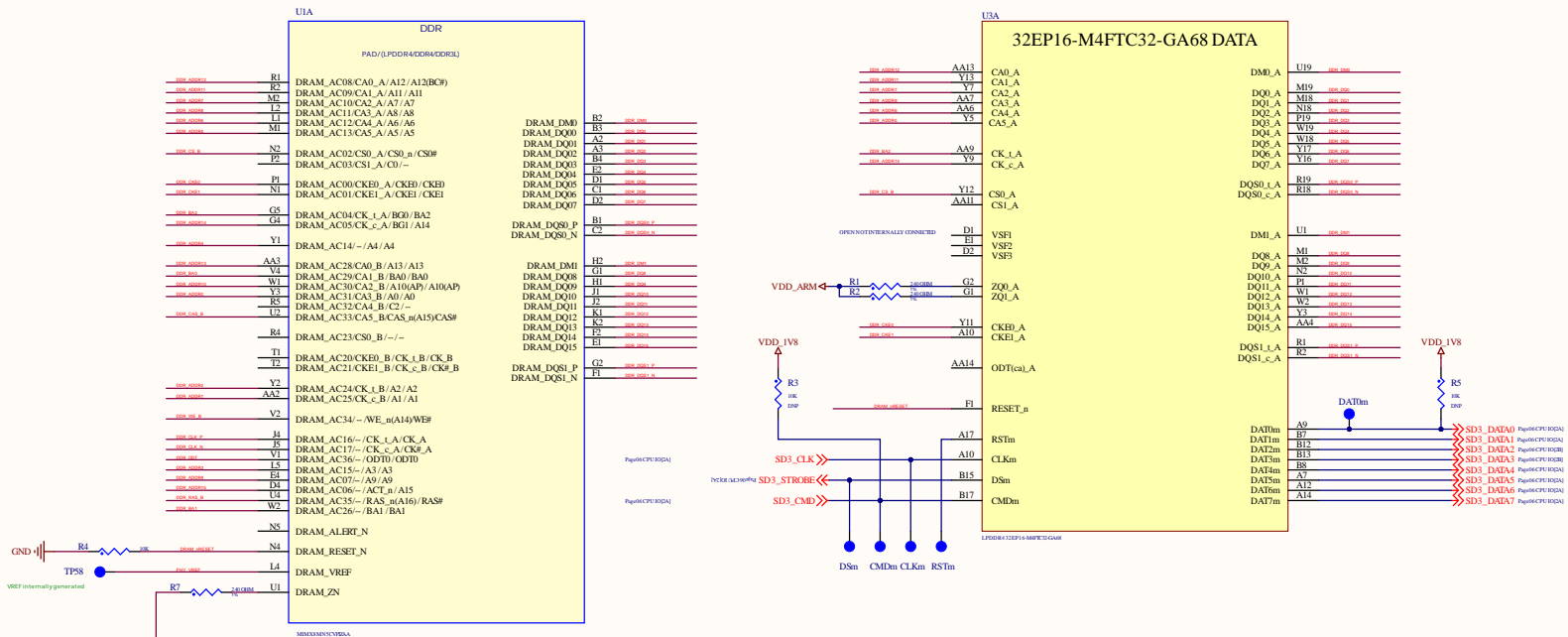
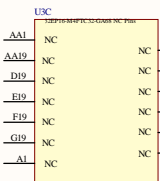
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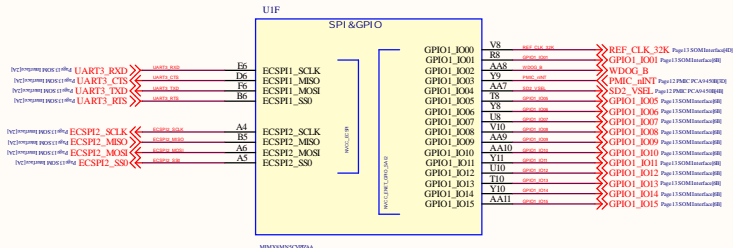
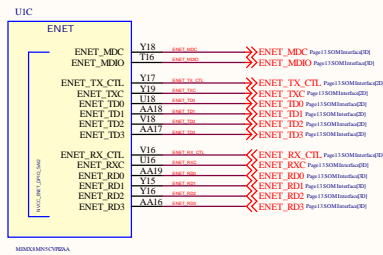
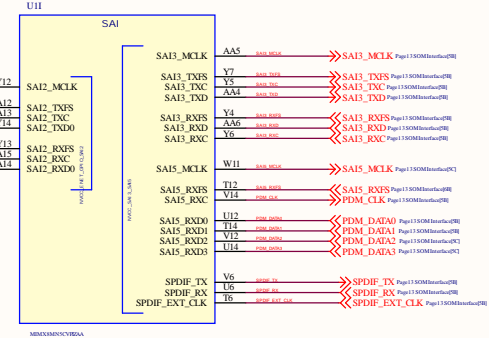
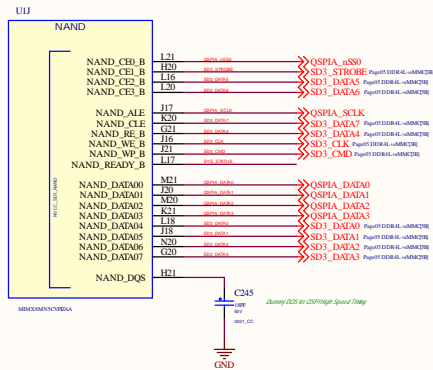
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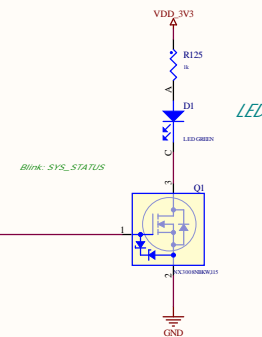
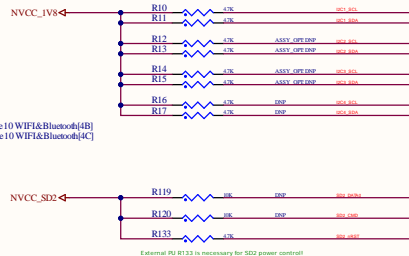
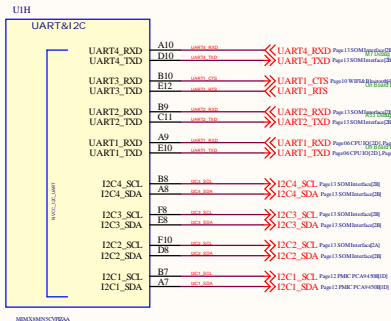
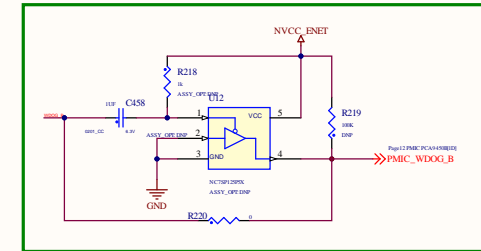
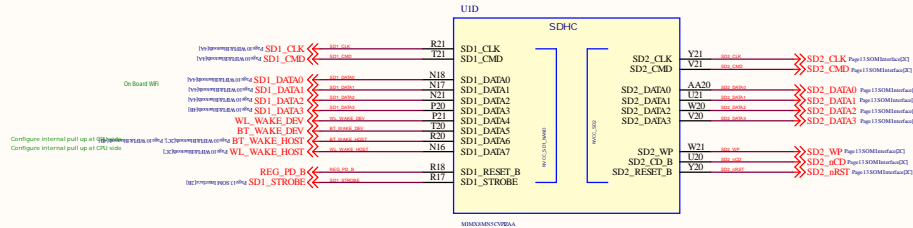
DDR4+eMMC


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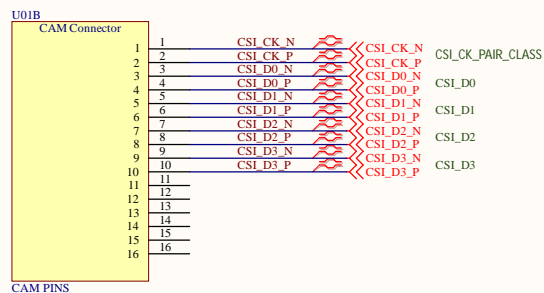
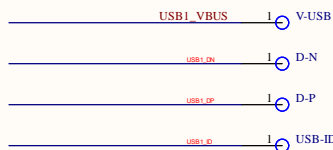
i.MX8M Nano IO Interface




Configure internal pull up at CPU side, open drain output
Configure internal pull up at CPU side
Note:
GPIO1_IO02 is the only pin can be used as WDOG_B to
loggle the PMIC.
When entering boundary-scan mode, this pin is set to lowby
the processor.
The PMIC PCA9450 default disables WDOG_B Reset and
the cold reset event is generated by WDOG_B falling edge,
so the WDOG_B is always low that will not impact to enter
boundary scan mode.



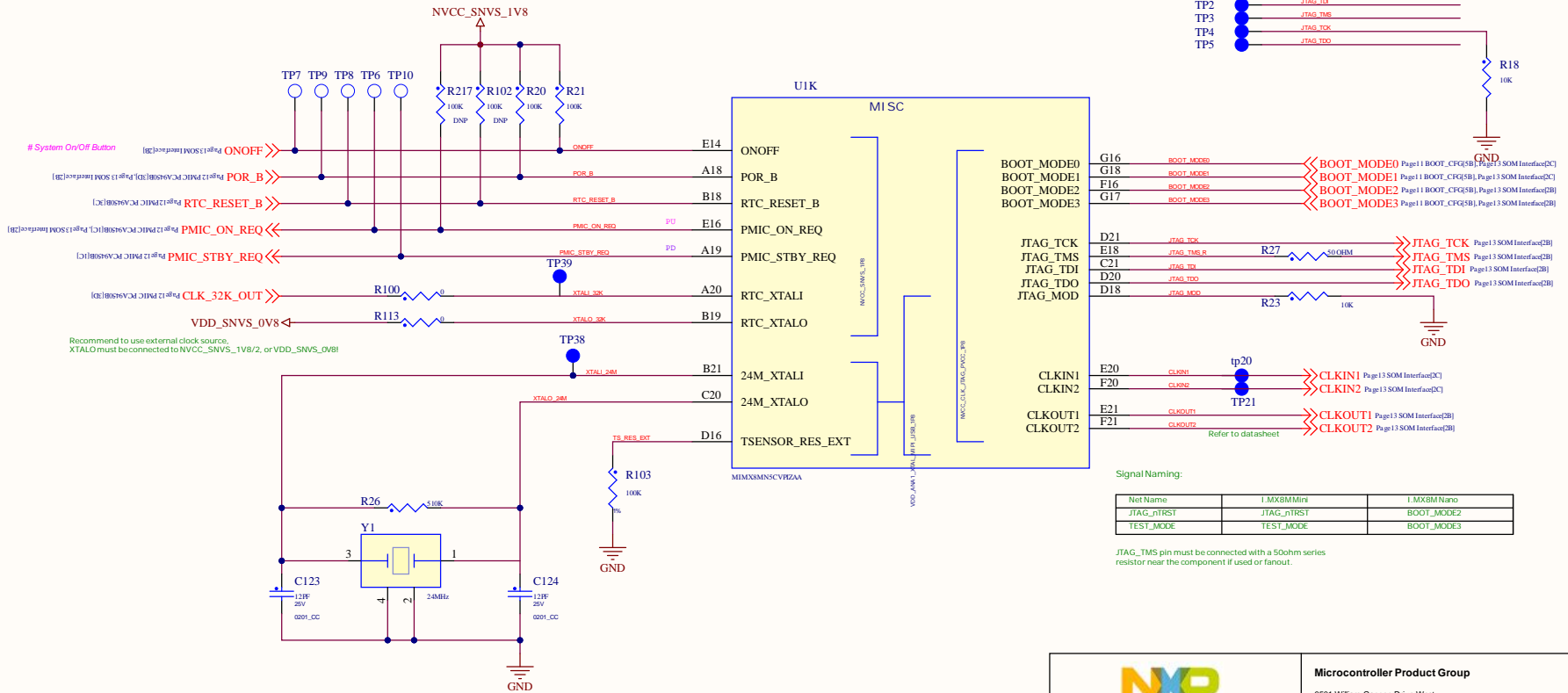
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Drawn by: <i>Vector Group</i>	Page Title: <div style="text-align: center;">CPU PHY</div>				
Approved:	Size NC	Document Number <div style="text-align: center;">SCH-47569 PDF: SPY-4750</div>			Rev A2
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i.MX8M Nano MISC

JTAG Debug

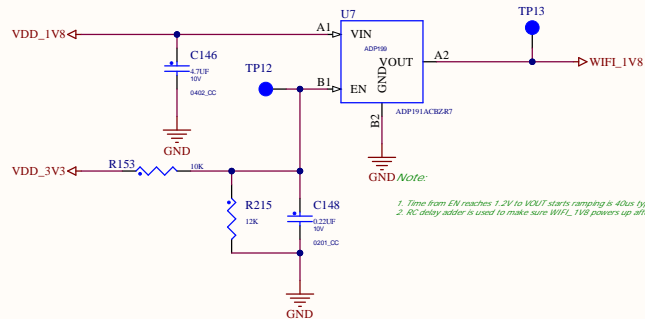
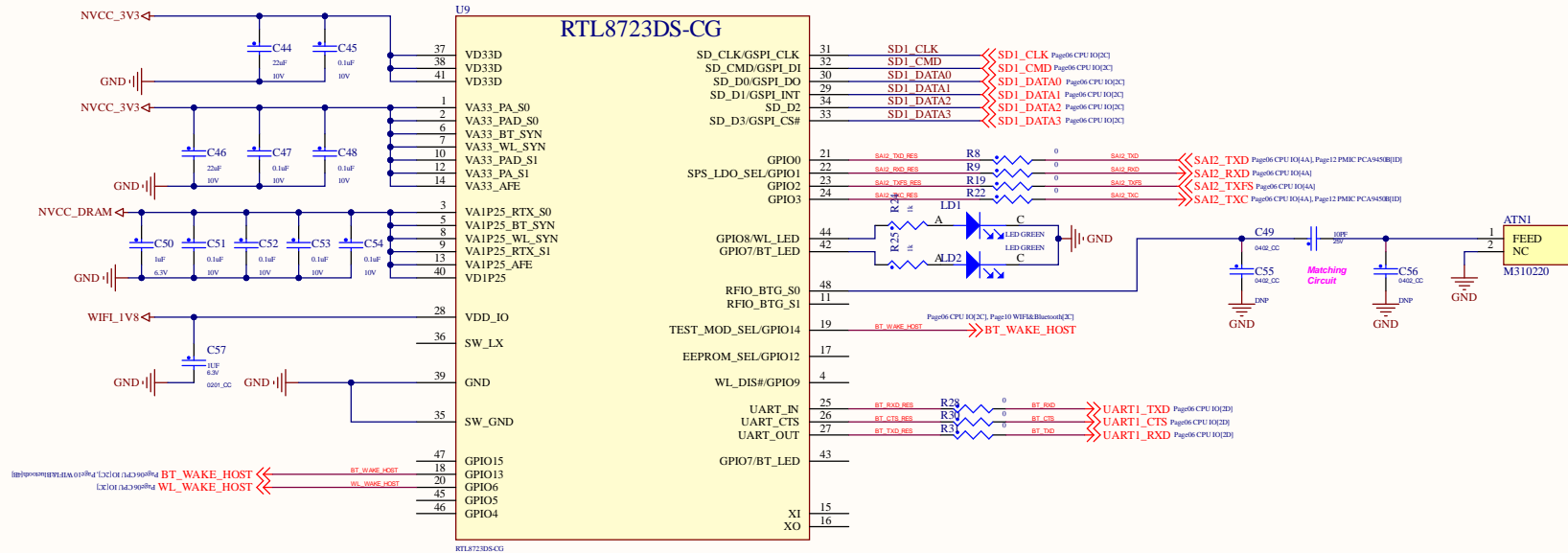


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1	2	3	4	5	6	
A						A
B						B
C						C
D						D
1	2	3	4	5	6	

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Drawn by: Vector Chang	Page Title: eMMC/QSPI				
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Date: 2014-05-01		Sheet 6 of 14			

2.4G/5G WIFI/BT Module



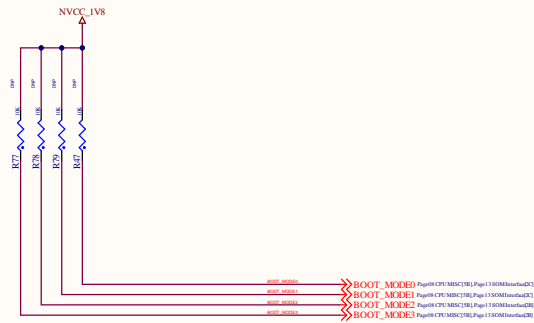
Note:
1. Time from EN reaches 1.2V to VOUT starts ramping is 40µs typical
2. AC delay adder is used to make sure WIFI_1V8 powers up after VDD_3V3

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Drawn by: Vector Chang	Page Title: WIFI/BT Module				
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Date:	1	Sheet	30	of	15

Boot Mode

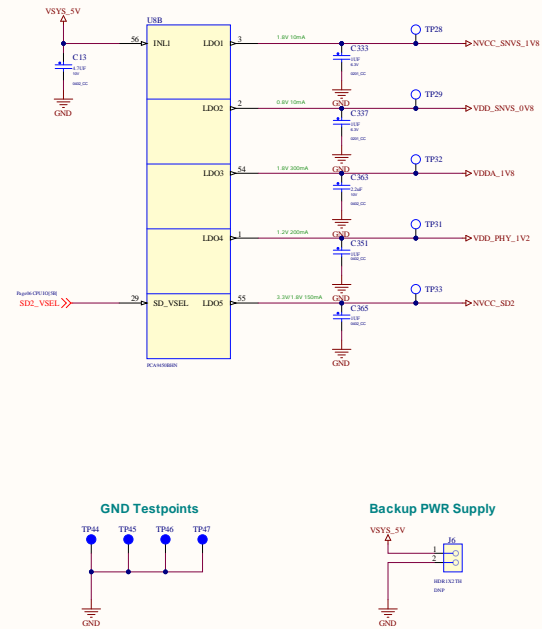
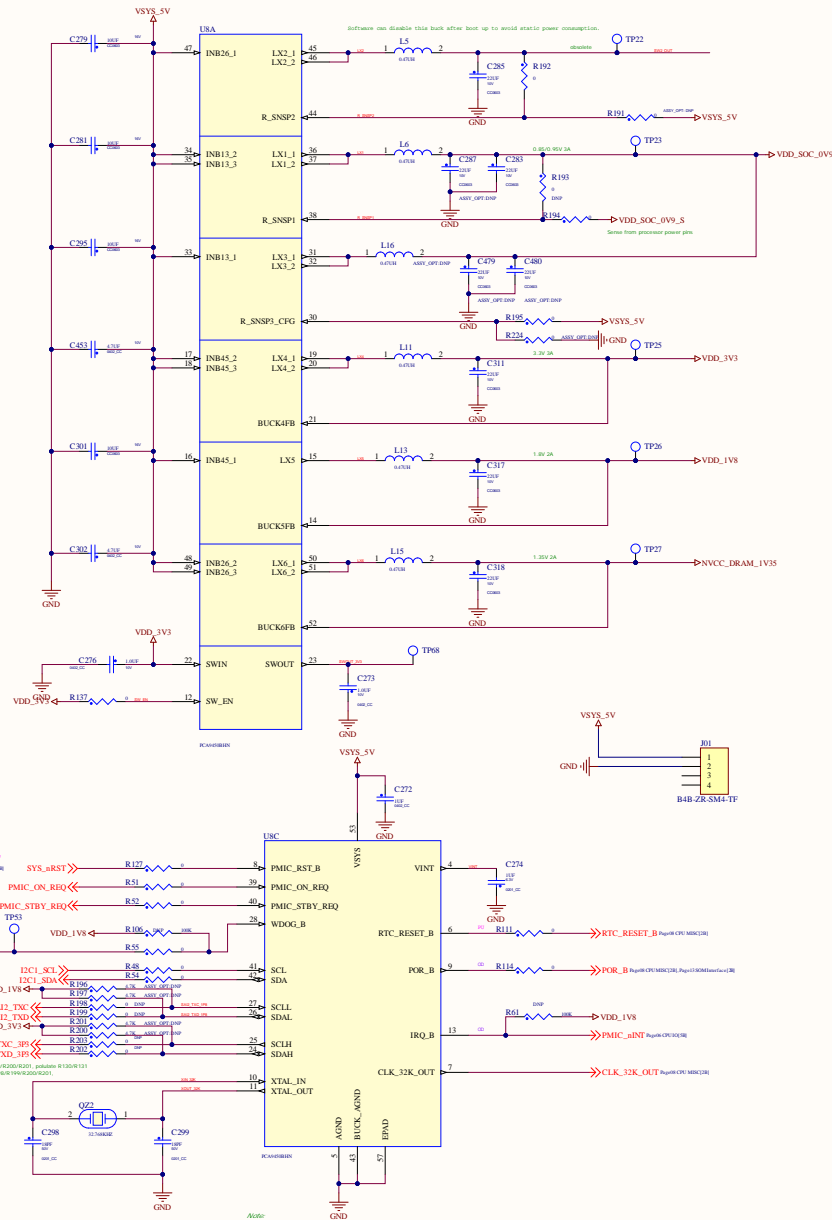
i.MX8M Nano Boot Mode

BOOT_PIN[3]	BOOT_PIN[2]	BOOT_PIN[1]	BOOT_PIN[0]	Boot Modes
BOOT_MODE3 (TEST_MODE)	BOOT_MODE2 (JTAG_TRST_B)	BOOT_MODE1	BOOT_MODE0	Function
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit)
0	0	1	1	USDHC2 (SD boot only, SD2)
0	1	0	0	NAND 8-bit single device 256 page
0	1	0	1	NAND 8-bit single device 512 page
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ecSPI Boot
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved (Boot on I2C connected to BOOTPIN[3:2])
1	1	0	1	Reserved
1	1	1	0	Infinite Loop Mode
1	1	1	1	Test Mode



- Notes:
- 1. BOOT_MODE0-3 signals are used for boot selections
 - 2. BOOT_MODE0 signals have internal RD buffers and after POR, B reset is deasserted
 - 3. When using Base Board for Multi boot selection, you must keep the resistors 20K or 50K board

SYS PMIC

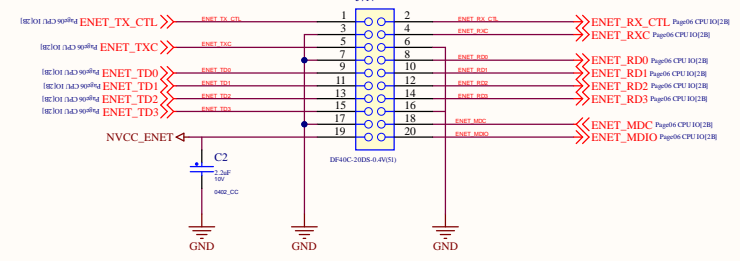
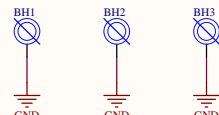
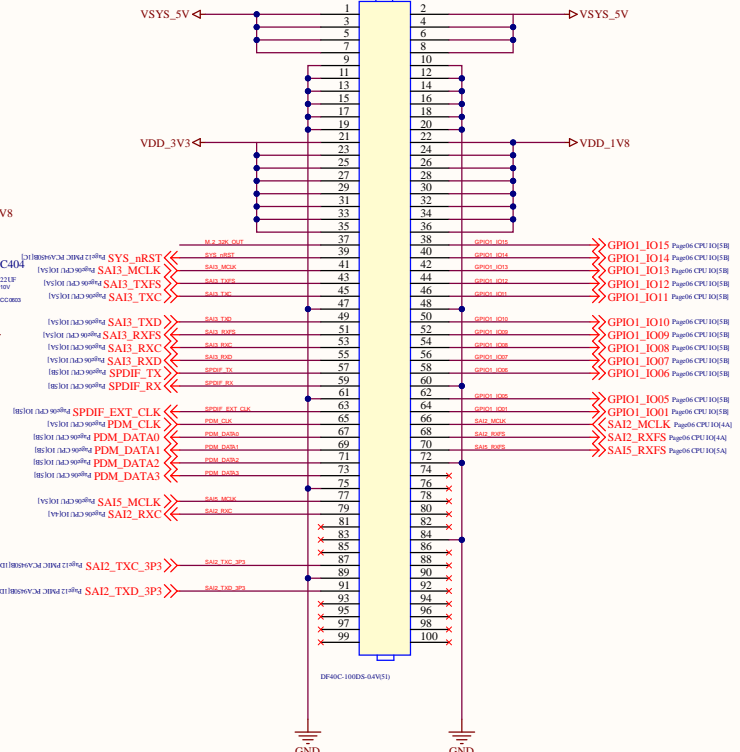
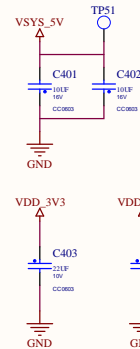



i.MX8M Nano DDR3L EVK Power Sequence						
SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.62	1.8	1.98	10
2	VDD_SNVS_0V8	LDO2	0.76	0.8	0.9	10
3	RTC_RESET_B	RTC_RESET_B	--	--	--	--
4	CLK_32K_OUT	RTC_CLK	--	--	--	--
5	VDD_SOC_0V9	BUCK1	0.76/0.805/0.9	0.8/0.85/0.95	0.9/0.95/1.0	3000
6	VDDA_1V8	LDO3	1.71	1.8	1.89	300
7	VDD_1V8/NVCC_1V8	BUCK5	1.65	1.8	1.95	2000
8	NVCC_DRAM_1V35	BUCK6	1.283	1.35	1.417	2000
9	VDD_3V3/NVCC_3V3	BUCK4	3	3.3	3.6	3000
9	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
10	POR_B	POR_B	--	--	--	--
11	VDD_PHY_1V2	LDO4	1.14	1.2	1.26	200

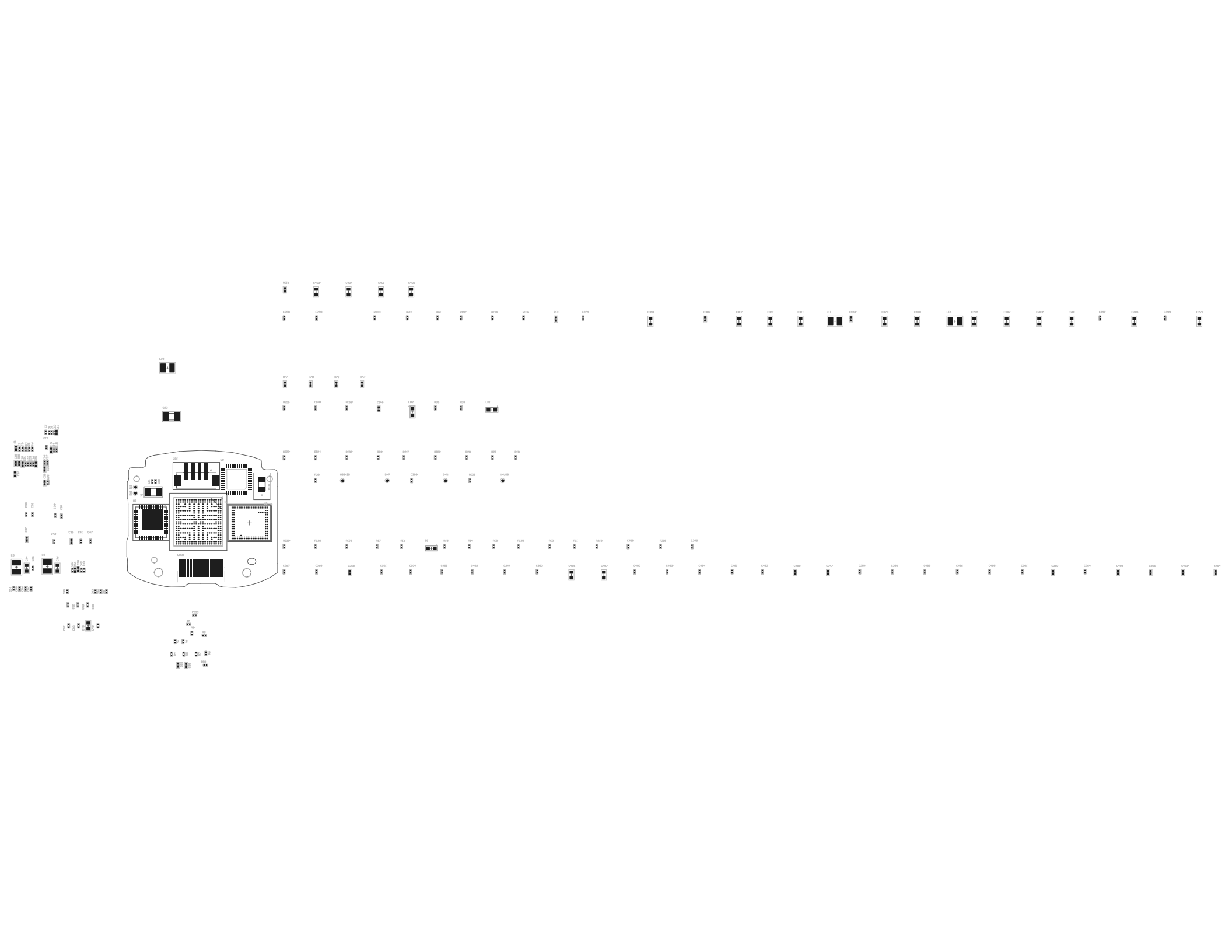
B2B Connector for CPU Board

Header

Receptacle



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Approved:	Size NC	Document Number SC31-47549 PDF: SPF-47549	Rev 02
Date:	Sheet		13 of 13



Board Stack Report