Project 10

Design of wideband matching circuits

This project focuses on the design of the wide-band matching circuits for input of an FET using both LC elements and microstrip transmission lines.

Choose one of the defined complex loads which model FET inputs (shown below) and design frequency bands. Using both the LC and microstrip matching structures, design wideband matching circuits transforming the load in question to a standard 50 Ω impedance with a resulting reflection coefficient lower than −10 dB. Show graphs with S_{11} (absolute values and Smith Chart) of both matching circuits and the layout of the microstrip matching circuit.

Loads and frequency bands:

Task No.	R_L (Ω)	C_L (pF)	Frequency band (GHz)
1	13	1,0	3 – 6
2	15	1,8	8 – 11
3	10	1,2	7 – 13
4	18	1,7	6 – 10
5	14	1,5	8 – 15
6	20	1,4	3 – 6
7	11	1,1	7 – 11
8	17	0,9	12 – 18
9	12	1,3	7 – 12
10	19	1,1	4 – 7
11	15	1,4	6 – 10
12	13	1,8	5 – 9
13	10	1,2	11 – 16
14	18	1,3	3,5 – 7
15	14	1,6	8 – 15
16	11	0,9	10 – 16
17	17	1,3	5 – 9
18	16	1,0	10 – 16
19	15	1,4	6 – 11
20	11	1,7	3 - 6
21	13	1,0	4 – 8
22	15	1,8	10 – 15
23	10	1,2	6 – 12
24	18	1,7	5 – 10
25	14	1,5	9 – 14
26	20	1,4	4 – 7
27	11	1,1	7 – 12
28	17	0,9	10 – 16
29	12	1,3	8 – 14
30	19	1,1	12 – 18
31	15	1,4	5 – 10
32	13	1,8	8 – 13
33	10	1,2	10 – 15
34	18	1,3	4 – 8
35	14	1,6	9 – 15
36	11	0,9	7 – 13
37	17	1,3	6 – 12
38	16	1,0	11 – 17
39	15	1,4	8 – 12
40	11	1,7	4 – 7

Project solution procedure

The recommended design steps are described in the following example:

- The complex Z_L load impedance can be approximated by a series combination of R_L = 17 Ω and C_L = 1.1 pF, see Fig. 1. This equivalent circuit corresponds, for example, to an FET input circuit.

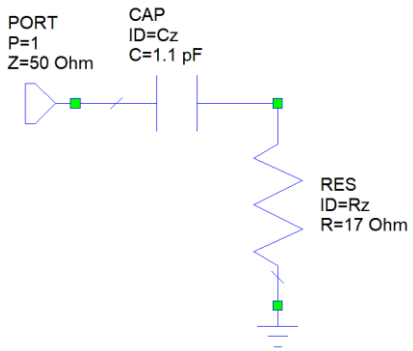

Fig. 1 Equivalent circuit of the input of an FET.

- In the frequency band from 6 to 12 GHz the load should be matched to 50 Ω. In practice, the obtained return loss should be higher than 10 dB ($|S_{11}| < -10$ dB).

Based on the recommended structures described in the Lectures, the following matching circuits can be used. In the first step, try to find optimum values using TUNE TOOL.

- Create a new schematic and draw the concerned matching structure shown in Fig. 2.
- Set the following initial values L1 = 1 nH, L2 = 1 nH, C1 = 1 pF.
- For tuning, activate L1, L2, C1
- Set the low limits of all variables used to 0. Set the high limits to 2 (nH, pF).
- Create a new Smith Chart graph and plot S_{11} of the whole circuit.

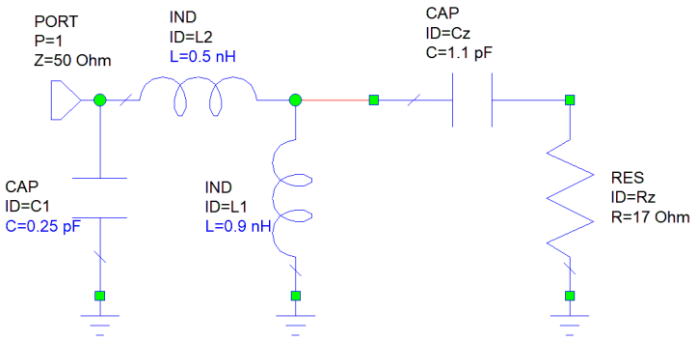

Fig 2. Recommended matching circuit for the input of an FET.

- When tuning L1, L2, C1, try to "curl" the S_{11} plot around the Smith Chart center which minimizes its absolute value. A suitable solution can be seen in Fig. 3.

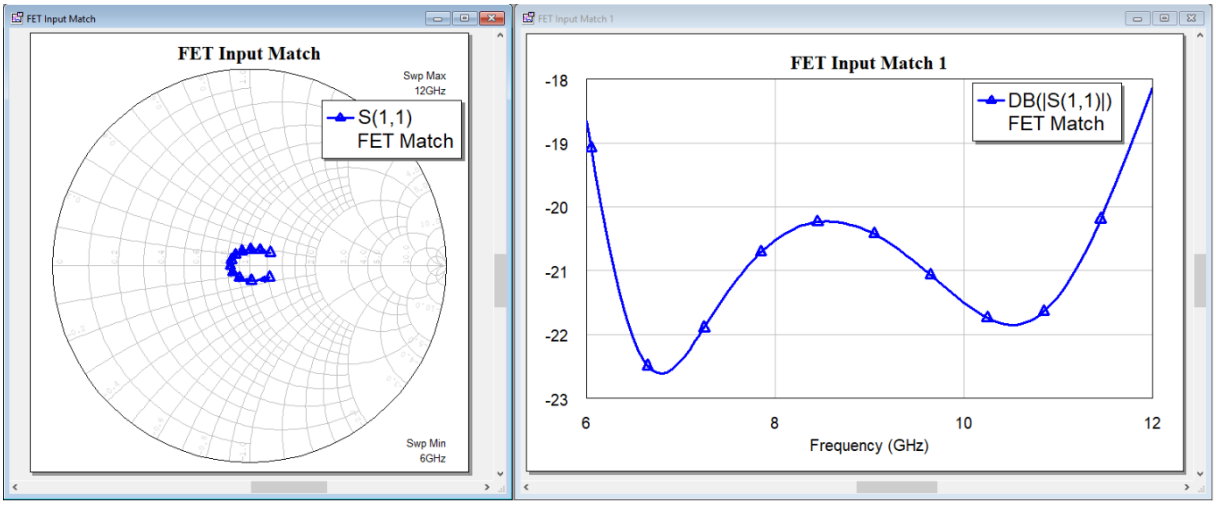

Fig. 3 Reflection of S_{11} of the tuned structure from Fig. 2.

- The resulting return loss is higher than 18 dB which is practically a suitable solution.

You can also try the structure shown in Fig. 4 with more elements. Theoretically, it should provide even better impedance matching.

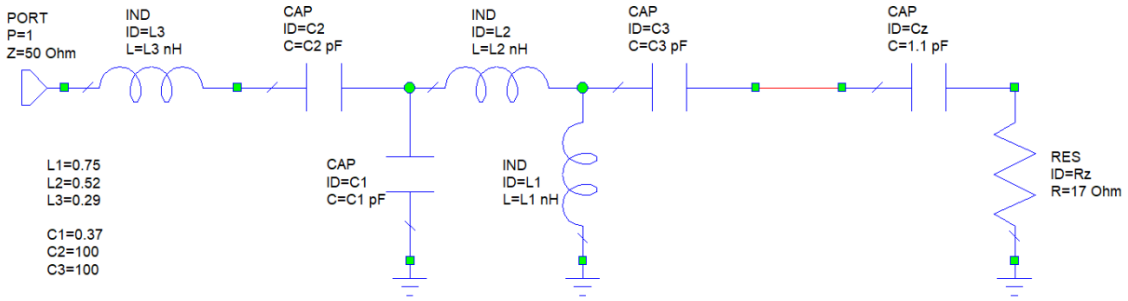

Fig. 4 Advanced matching circuit.

- The C3 capacitor enables the absorption of a definite part of the load capacitance.
- Due to the high number of variables, the usage of an optimization procedure can be beneficial. Using ADD EQUATION, set VARIABLES (L1, L2, L3, C1, C2, C3) and estimate their initial values to 1 (pF or nH).
- Create a rectangular graph, then add the absolute value of the S_{11} measurement in dB.
- By clicking on your right mouse, activate the OPTIMIZER GOALS – ADD OPTIMIZER GOAL function.
- Choose $|S_{11}|$, define MEAS. < GOAL, and GOAL = −30 dB.
- From the SIMULATE submenu, activate the OPTIMIZE function. In the bottom-left part of this window it is possible to switch between the optimizer and variable settings.
- Activate the VARIABLES function. At all variables used within the optimization process (L1−3, C1−3) mark the OPTIMIZE and CONSTRAINED options.
- CONSTRAINED means that the optimizer will choose variable values from the constrained ranges. Define the LOWER and UPPER fields to 0 and 1 (pF or nH), respectively. In the case of C2 and C3 set the UPPER limits to a higher value, *e.g.*, 100 pF, see Fig. 5.

Document	Element eqn	ID	Parameter	Value	✔Tune	✔Optimize	✔Constrain	Lower	Upper
FET Advanced Match	EQN		C1	0.37	☐	☑	☑	0	1
FET Advanced Match	EQN		C2	100	☐	☑	☑	0	100
FET Advanced Match	EQN		C3	100	☐	☑	☑	0	100
FET Advanced Match	EQN		L1	0.75	☐	☑	☑	0	1
FET Advanced Match	EQN		L2	0.52	☐	☑	☑	0	1
FET Advanced Match	EQN		L3	0.29	☐	☑	☑	0	1

Fig. 5 Definition of variables for optimization.

- Now activate OPTIMIZER and choose an optimization procedure.
- Try the SIMPLEX OPTIMIZER (or any other from the list).
- Start the optimization procedure using the START button. The RELATIVE GOAL COST graph should descend ideally to zero. The optimization process is stopped automatically, or manually, using the STOP button.
- Values of the optimized variables can be found in the VARIABLES table, or in the concerned schematic.
- Optimization results can be found in Fig. 6.

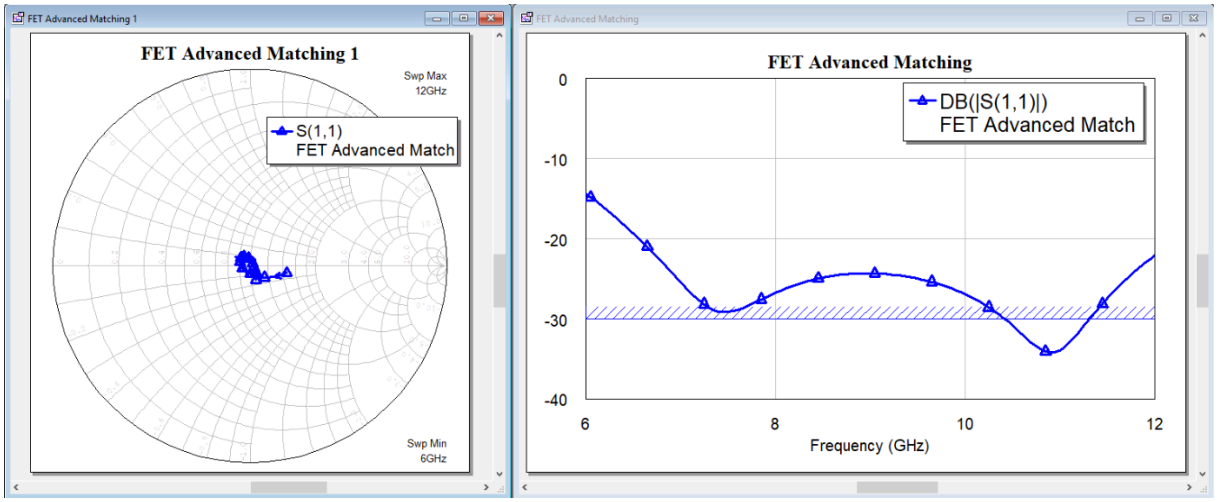

Fig. 6 Optimized reflection coefficient.

The above-designed wideband matching circuits show very good results. Unfortunately, at high RF or microwave frequencies, due to the parasitic properties of real L and C components, wideband matching circuits are difficult (often unable) to be constructed. This is why the following wideband matching structure based on sections of microstrip lines can be recommended:

- For the design, use the CuClad 217 substrate, its parameters (set in GLOBAL DEFINITIONS) are the following: $\varepsilon_r = 2{,}17$, $\mathrm{tg}\delta = 0.001$, $H = 0.508$ mm, $T = 30$ μm, copper metallization.
- Using TXLINE, calculate the width corresponding to 50 Ω and related λ_g.
- In the given example, the center frequency equals 9 GHz, $w_{50} = 1.54$ mm, $\lambda_g = 24.4$ mm.
- Connect a section of the 50 Ω microstrip line to the concerned R_L and C_L load, and using TUNE TOOL, set its length so that the center of the S_{11} frequency plot intersects the horizontal Smith Chart axis as shown in Fig. 7.

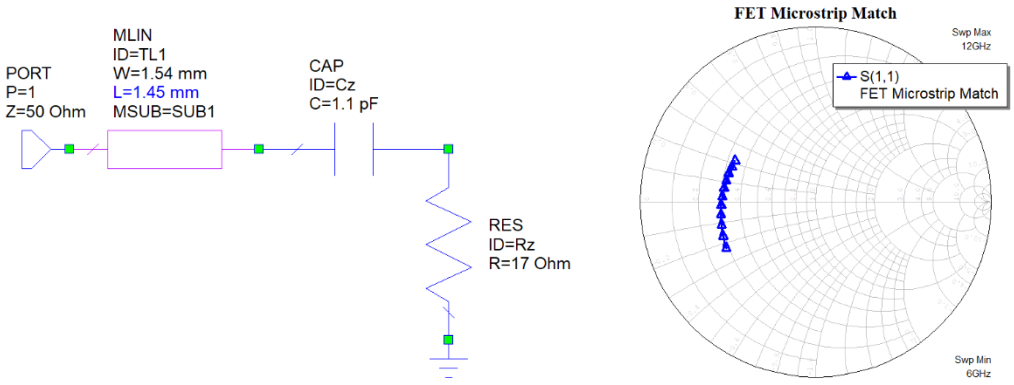

Fig. 7 Input circuit of an FET with microstrip line and resulting reflection.

- The shifted S_{11} frequency dependence can be "wrapped" using two in-parallel connected sections of microstrip line, approximately $\lambda_g/8$ long. Ends of these stubs are equipped with SHORT and OPEN terminations, see the schematic and graph in Fig. 8.

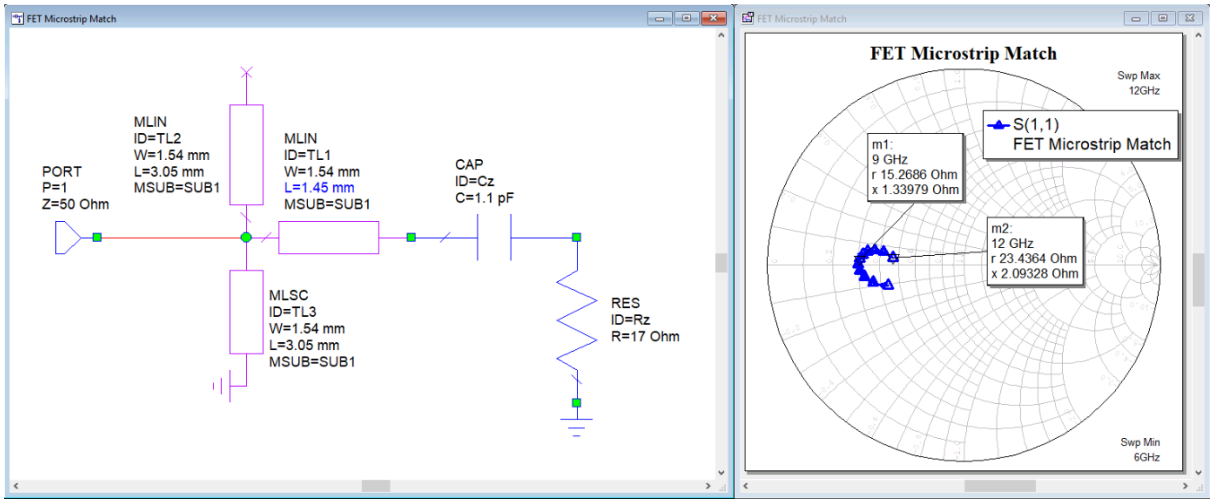

Fig. 8 Matching circuit with open and short microstrip line stubs and its resulting reflection coefficient.

- The frequency plot is relatively well "curled" but still far from the Smith Chart center.
- The shift to the Smith Chart center can be arranged using the $\lambda_g/4$ impedance transformer. An impedance of this section should be set to $Z_1 = \sqrt{Z_0 Z_L}$. In this equation, Z_L corresponds to an approximate impedance at the center of the curled frequency plot.
- In our case, $Z_L = 19\,\Omega$ leads to $Z_1 = \sqrt{19 \cdot 50} = 30.8\,\Omega$.
- TXLINES make it possible to calculate the corresponding microstrip width w_1 = 3.05 mm. The required 90º phase-shift can be ensured by a 5.96 mm microstrip line length. The schematic and resulting reflection coefficient is shown in Fig 9.

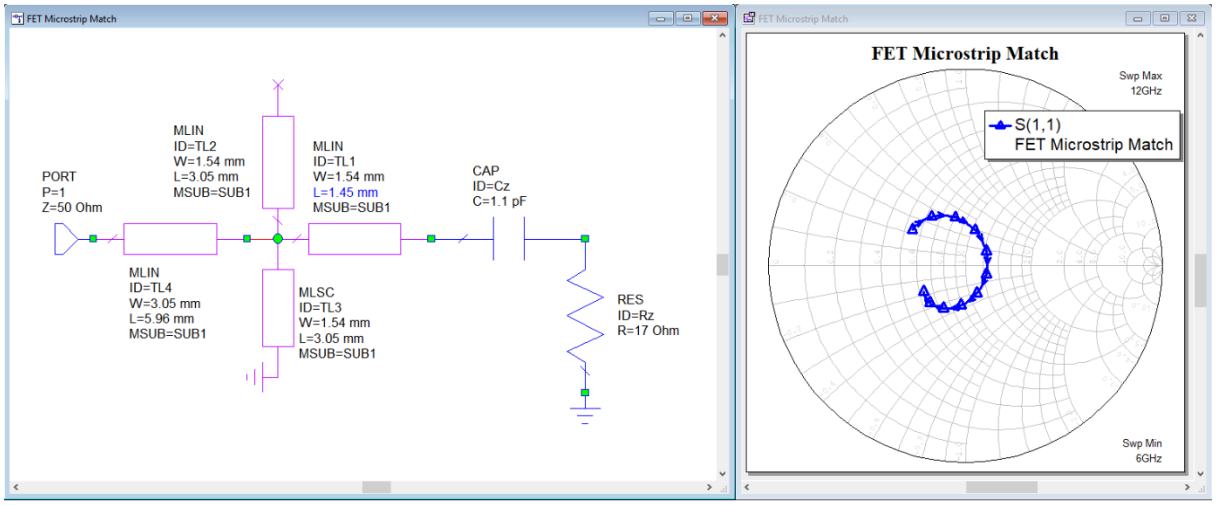

Fig. 9 Matching circuit with impedance transformer and its reflection coefficient.

- "Wrapping" of the frequency plot can be improved using TUNE TOOL or the optimization process. Prior to this, the schematic should be completed using discontinuity models. In the given case of the MCROSS$, MLEF, MVIA1P and MSTEP$ models, see Fig. 10.
- Using the optimization process, the reflection shown in Fig. 11 was obtained.

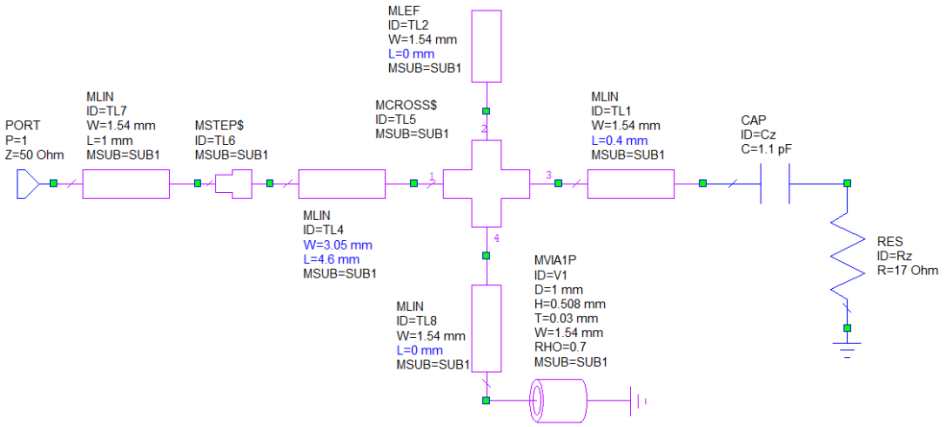

Fig. 10 Schematic of the matching circuit including discontinuities.

- An interesting result from the optimization is that the microstrip open stub and line connecting the via both have zero length.

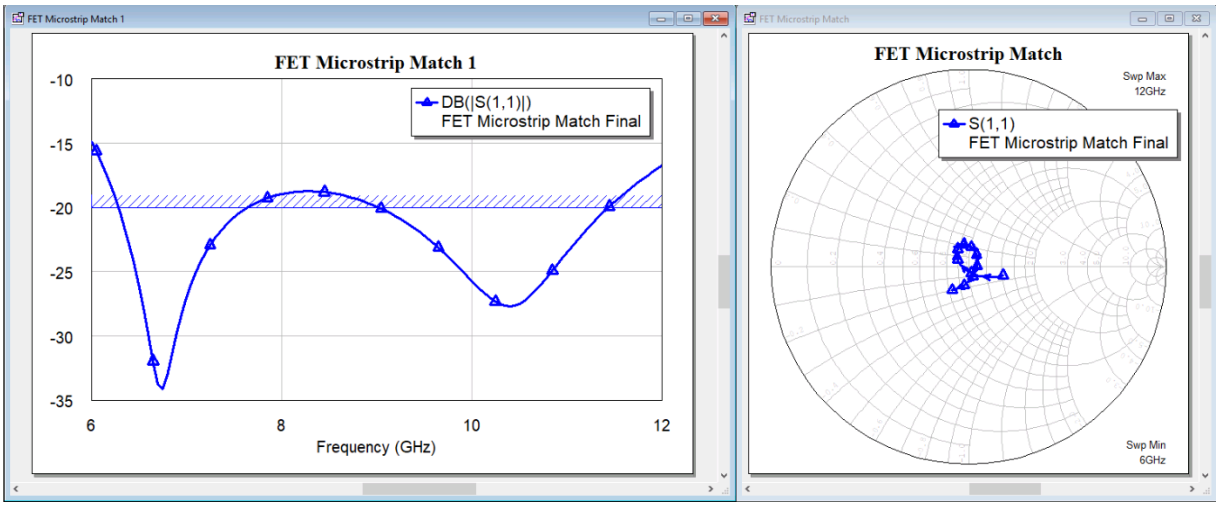

Fig. 11 The resulting reflection coefficient using microstrip lines.

- The resulting structure can also be viewed in a LAYOUT form.
- This can be displayed by right clicking the concerned SCHEMATIC and activating the VIEW LAYOUT function.
- Quite often, it is necessary to correct the layout. Activate the CTRL+A (select all) function, the concerned layout should change its color to yellow.
- Activate the SNAP TOGETHER function (upper horizontal bar). The resulting layout can be seen in the following figure.

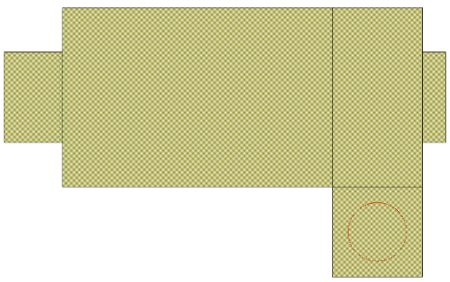

Fig. 12 Layout of the matching circuit.

- From the right side, the concerned complex load (*e.g.*, transistor input) can be connected. From the left side, the input 50 Ω line should be extended.