Application of FinFET technology in RF systems

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1 Introduction

Recent technological trends indicate a shift towards higher frequencies in the field of electronic engineering, which imposes new requirements on the radio-frequency (RF) capabilities of developed components. With the integration of additional components into LTE phones and the emergence of novel sub-6-GHz 5G bands, the need for area scaling becomes crucial to accommodate a variety of chipsets within compact cellphone designs, all while ensuring optimal power efficiency.

FinFET-based logic process technologies have risen as a favoured option for production, boasting significant advantages including exceptional scalability, minimal power consumption, and outstanding performance, especially evident at 14-nm and 16-nm nodes.

2 Performance

Working with the data provided in [1], we can make a direct performance comparison in the following three crucial RF figures of merit:

- f_t as the cutoff frequency, i.e., the frequency at which the magnitude of the current gain has dropped to unity (i.e., 0 dB);
- f_max as the maximum frequency of oscillation, i.e., the frequency at which the unilateral power gain equals unity (i.e., 0 dB);
- $G_\mathrm{m}/G_\mathrm{ds}$ as the self-gain, where G_m is the transconductance and G_ds is the output conductance.

For most RF applications, power gain and f_max are more important than current gain and f_t. However, that is not always the case, and we should inspect both parameters, as displayed in Figure 1. These plots are taken from [1], and they display the frequency performance using a minimum channel length (14 nm), 12-fin N-type and P-type FinFET devices. The measurements were taken using the open, short and through de-embedding technique for the elimination of the pad and the interconnect effects.

Furthermore, the 14 nm FinFET processing involves the creation of deep silicon cavities for subsequent growing of a boron-doped SiGe epitaxy stressor inside them. The compressive stress over the fin channel boosts the overall hole carrier mobility, hence significantly increasing in the transconductance G_m. This directly translates to much higher cutoff frequency and self-gain. The self-gain is further improved during the on-state operation, where a FinFET device experiences full channel depletion. This is thanks to better electrostatic gate control by suppressing the short-channel effects, i.e., the punchthrough and the drain-induced barrier lowering, resulting in lower output conductance G_ds.

All the results discussed above are summarized in Table 1 which serves as a good and standing-out comparison of key performance factors.[1]

[1] The data were taken for a 14 nm RF FinFET and a 28 nm planar FET with a high-K metal gate. The G_msat was measured at $V_\mathrm{dd} = 8\,\mathrm{V}$. The S_vg is measured at $f = 1\,\mathrm{kHz}$.

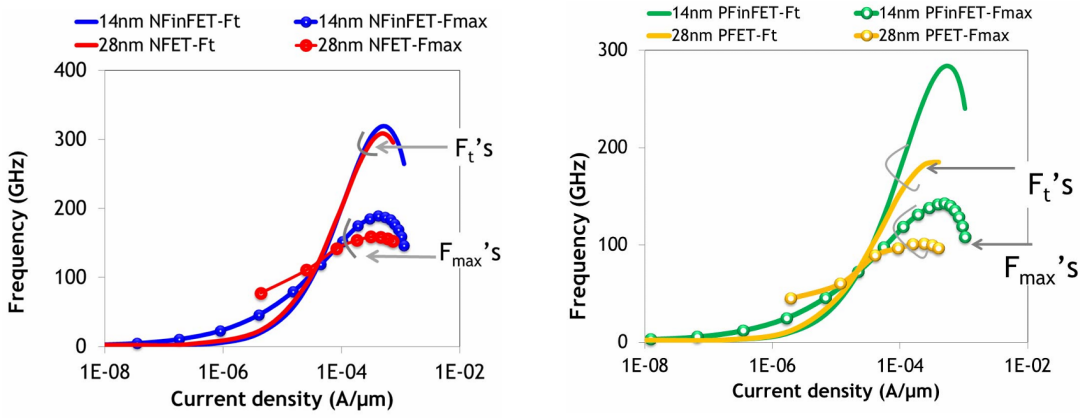

Figure 1: Cutoff and maximum oscillation frequencies over current density dependence

Device	NFinFET	PFinFET	NFET	PFET
f_t [GHz]	314	285	308	185
f_{max} [GHz]	180	140	159	102
G_{msat} [S m^{-1}]	3017	2748	985	395

Table 1: Comparison of key RF parameters between 14 nm FinFET and 28 nm planar FET

For more details on the performance differences between N-type and P-type FinFET devices, related work [3] serves as a good elaborate analysis of this topic.

3 Conclusion

The enhancement of FinFET technology's RF and analogue capabilities opens avenues to achieve RF + Logic system-on-chip (SoC) architectures, capitalizing on the technology's strides in logic power, performance, and area scaling.

Moreover, the trend towards digitally assisted analogue designs further highlights the appeal of the FinFET technology, given its scaled footprint and robust digital design portfolio. Consequently, optimized RF SoC designs based on the FinFET technology emerge as an appealing choice [2].

Bibliography

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