Project 9

Design of a low-noise amplifier based on a microwave FET and microstrip matching circuits

This project focuses on the design of a low-noise amplifier consisting of an FET and matching circuits from microstrip lines.

Design a low-noise amplifier (LNA) based on a microwave FET. Find its type and operating frequency in the appended table.

As a design protocol note, please include:

- choice of an FET and design frequency f_0,
- a utilized commercially available substrate,
- schematics of the input and output matching circuits,
- the schematic and reflection of a bias circuit,
- the final schematic of the amplifier,
- the final layout of the amplifier,
- a graph with S-parameters of the final amplifier in an approx. f_0 ±20% freq. band,
- a graph of the noise figure of the final amplifier and the NFMin of the transistor.

The transistor data can be found in LIBRARIES − AWR WEB SITE − PARTS OBSOLETED – AGILENT/FUJITSU. Transistors F1... are Agilent and transistors FHX… or FHR… are Fujitsu.

Task No.	FET file name	Design frequency (GHz)
1	F101352A	6
2	F102352A	7.2
3	F107352A	5.3
4	F133353A	10
5	FHR02FH	18
6	FHX13LG	8.8
7	FHX30X	14.5
8	FHX044	15.7
9	F101352A	7.7
10	F102352A	6.8
11	F107352A	6.3
12	F133353A	9.3
13	FHC30LG	5.1
14	FHX13LG	9.5
15	FHX30X	14.8
16	F101352A	7.4
17	F102352A	6.9
18	F107352A	7.3
19	F133353A	10.7
20	FHC30LG	6.8
21	FHR02FH	18.4
22	FHC30LG	7.4
23	FHX04LG	11.6
24	FHX13LG	8.9
25	F101352A	6.6
26	F102352A	5.8
27	F107352A	6.7
28	FHX04LG	12.0
29	FHC30LG	5.6
30	FHX13LG	11.2

Project solution procedure

As a demonstration task, the following amplifier has been designed:

- An ATF-34143 (Agilent) transistor with a 2V/20mA biasing point. Both the transistor's S-parameters and noise parameters can be found in the F341432A.S2P file which can be found in LIBRARIES − AWR WEB SITE − PARTS OBSOLETED – AGILENT – DATA − FET DATA FILES library.
- The S-parameters and noise parameters can be viewed by double-clicking the left mouse at the filename in the PROJECT – DATA FILES folder.
- Create a new schematic called Transistor, load your transistor and connect both ports.
- The design frequency of this example is 8 GHz. The goal is to design the LNA with optimum noise matching at the input and ideal impedance matching at the output.
- The RT/duroid 5880 substrate with h = 0.508mm and ε_r = 2.2 is utilized for the design of matching circuits using sections of microstrip lines including discontinuities.

Plot in the entire frequency band of the given FET and graph of stability coefficient k:

- Create a new rectangular graph.
- Add the measurement of stability factor k (Linear – Stability − K).
- Perform an analysis whose result is shown in Fig. 1.
- At the design frequency 8 GHz the stability factor is k = 1.1 which is sufficient stability.
- If your FET is potentially unstable (k < 1), contact your teacher.

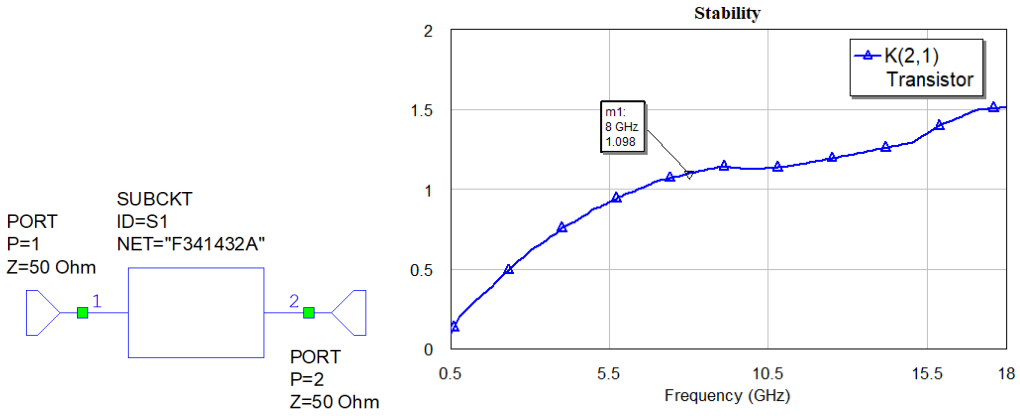

Fig. 1 Stability factor of the ATF-34143 transistor.

When designing the required optimum noise matching of any transistor, its input must "see" the optimum reflection coefficient in AWR described as GMN. All noise-related measurements can be found in LINEAR − NOISE.

- Create a new tabular graph and plot it into the table at the design frequency: NFMin in dB, magnitude of GMN and angle of GMN (source Transistor schematic). The result can be seen in Fig. 2.

Frequency (GHz)	DB(NFMin(2,1))[76] Transistor	|GMN(2,1)|[76] Transistor	Ang(GMN(2,1))[76] (Deg) Transistor
8	0.95	0.47	-86

Fig. 2 Minimal reachable noise-figure and optimal input reflection coefficient.

- Now, it is possible to design the input matching circuit (IMC) which transforms 50 Ω to GMN.
- To design the output matching circuit (OMC), it is necessary to calculate Γ_2 which is an output reflection coefficient of the transistor with GMN connected to the input. The output matching circuit should transform 50 Ω to $\Gamma_L = \Gamma_2^*$.

- The Γ_2 value can be calculated, for example, by using the LTUNER element (General – Passive – Other). Create a new schematic and connect the LTUNER to the input of the transistor and set its reflection coefficient to GMN. The actual Γ_2 value is equal to S_{22} of the schematic shown in Fig. 3.

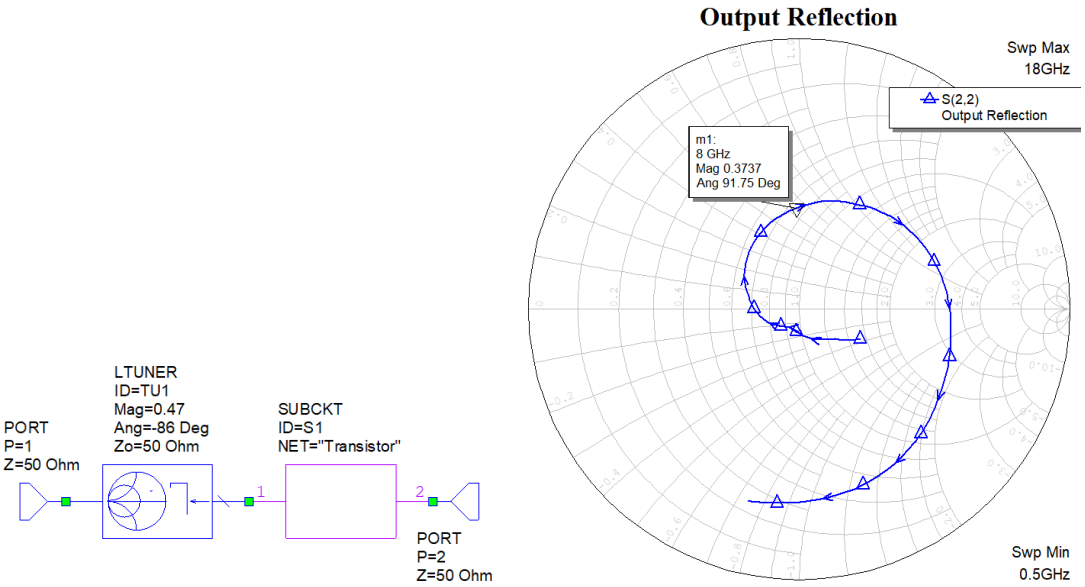

Fig. 3 Optimal input reflection coefficient connected to the transistor and S_{22} measurement.

- In our example, Γ_2 =0.3737∠91.75° at the design frequency of 8 GHz.

Now, it is possible to design the input matching circuit, which transforms 50 Ω to GMN, and the output matching circuit, which transforms 50 Ω to Γ_2. Both IMC and OMC should be formed by sections of microstrip lines and should include influences of discontinuities.

- Define the substrate parameters into GLOBAL DEFINITIONS parameters of the microstrip substrate MSUB.
- Using the TXLINE procedure calculate width *w* corresponding to a 50 Ω microstrip line and corresponding λ_g.
- In our example, at 8 GHz: *w* = 1.51 mm and λ_g = 27.37 mm, as shown in Fig. 4. All line lengths should be shorter than $\lambda_g/2$ which means < 13.69 mm.

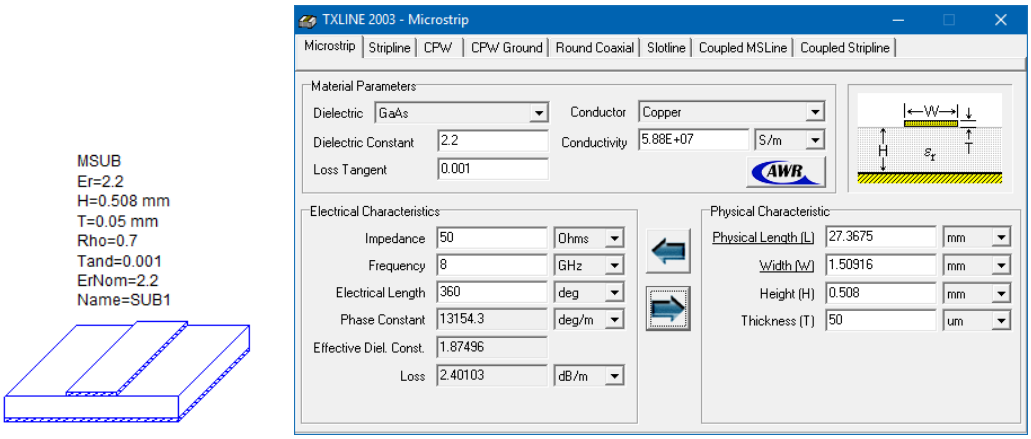

Fig. 4 Definition of the substrate and parameters of a 50 Ω-microstrip line.

- It is necessary to design the IMC separately. The LTUNER element can be utilized as one of the design possibilities.

- Create a new schematic called Input Match, insert from the right LTUNER there and set the GMN* value to 0.47∠86°. Also add both ports.
- Create a new Smith Chart and plot S_{11} and match reflection on the design frequency by connecting microstrip transmission lines.
- The IMC schematic and design procedure is shown in Fig. 5.

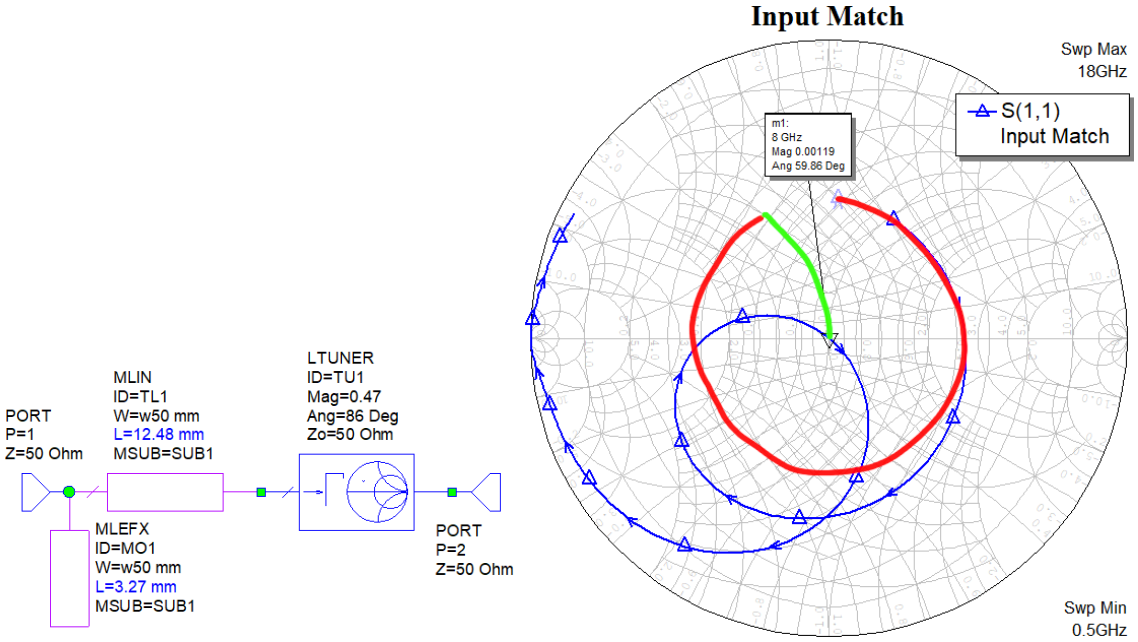

Fig. 5 IMC schematic and design procedure.

- First, the GMN* point must be transformed to the $g = 1$ circle using a TL1 microstrip section. That can be performed using TUNE TOOL by varying its length (red curve).
- Now, it is possible to transform the input impedance to the center of the Smith Chart connecting parallel section MO1 (green curve).
- Up to now, influences of the major discontinuity (T-junction), have not been included.
- Connect the MTEE element to the circuit. Set all widths W_i corresponding to the 50 Ω transmission line.
- When the MTEE element is connected, the S_{11} value shifts from the Smith Chart center. The correction can be performed using TUNE TOOL. Usually, approx. a 10% shortening of TL1 and a prolongation of MO1 is necessary.
- The IMC, after correction, can be seen in Fig. 6.

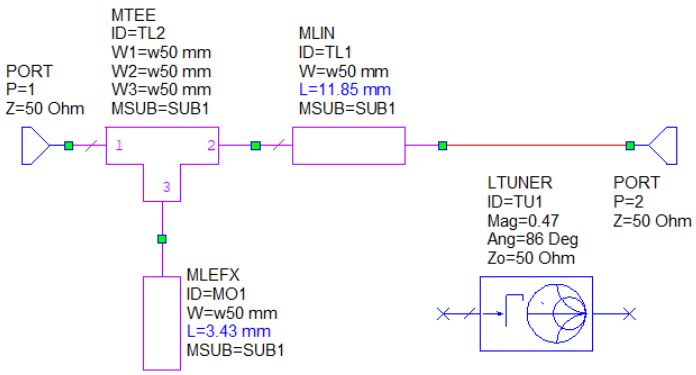

Fig. 6 Schematic of the IMC.

- Before connecting the IMC into the amplifier, do not forget to remove the LTUNER. To check the IMC design, plot the magnitude and angle of S_{22} values into the tabular graph. Check if S_{22} is approx. equal to GMN as shown in Fig. 7.

Frequency (GHz)	|S(2,2)|[76] Input Match	Ang(S(2,2))[76] (Deg) Input Match	|GMN(2,1)|[76] Transistor	Ang(GMN(2,1))[76] (Deg) Transistor
8	0.46343	-86.206	0.47	-86

Fig. 7 Check of S22 of IMC, which should be approx. the same as GMN.

- In a similar way, it is possible to design the OMC. The resulting circuit corresponding to our example can be seen in Fig. 8.

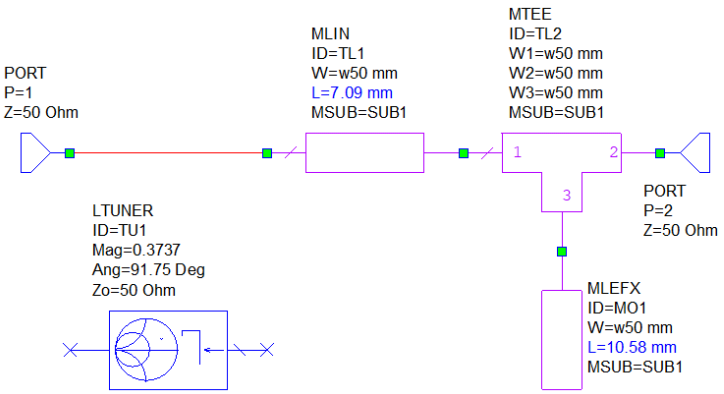

Fig. 8 Schematic of the OMC. The LTUNER utilized had a reflection as S_{22} as shown in the schematic from Fig. 3.

Each microwave amplifier must contain biasing circuits. Their main function is to bring biasing voltages to the FET. At the same time, they must not influence, in any way, the matching circuits at the design frequency. To accomplish this behavior, the impedance of the connecting point must be close to ∞. This can be ensured by using a $\lambda_g/4$-long section of high-impedance line shortened at one end. The $\lambda_g/4$ transformer transforms short to open, but the short cannot be galvanic short. That is why another section of a low-impedance (approx. 30 Ω), $\lambda_g/4$ open-ended line can be utilized. This low-impedance line transforms open to short. The high-impedance line transforms short to the required open. The biasing voltage can be connected to the MSTEP point because the impedance of this point is zero.

- Create a new schematic called Bias Filter and insert an open section of microstrip line MLEF with width 4 mm and length $\lambda_g/4$ in it. Tune its length to produce a short circuit at design frequency as shown in Fig. 9.

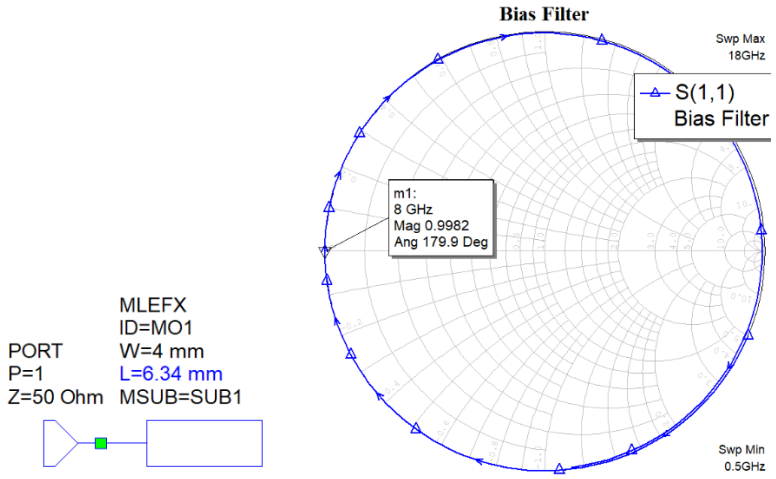

Fig. 9 Open stub with $\lambda_g/4$ length to produce a short circuit at design frequency.

- Add discontinuity MSTEP and MLIN with W = 0.2 mm and length $\lambda_g/4$. Tune TL2's length to produce an open circuit at the design frequency as shown in Fig. 10.

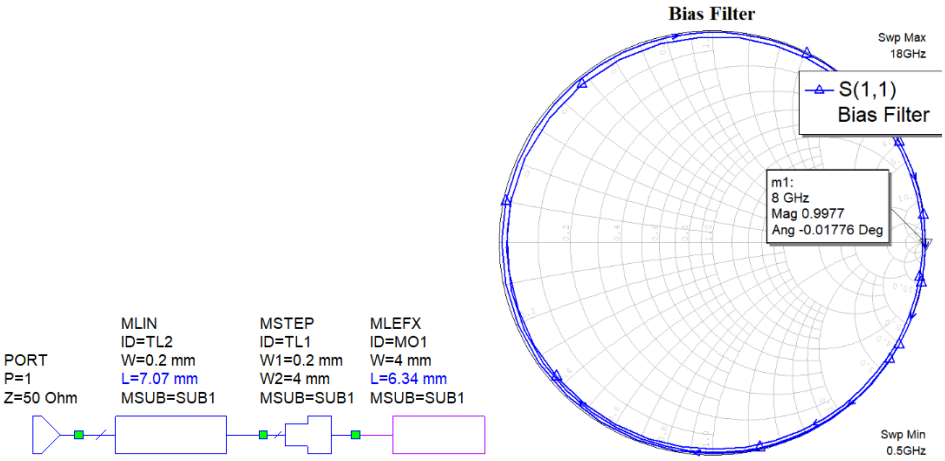

Fig. 10 Bias filter schematic and its reflection coefficient corresponding to an infinite impedance at f_0.

Now, it is possible to compile the whole amplifier:

- Move aside or delete the LTUNERs from both the IMC and OMC schematics.
- The final amplifier can be compiled using SUBCIRCUITS in a new schematic called Amplifier, see Fig. 11.
- The 10 mm section of microstrip lines is connected at both the input and output.

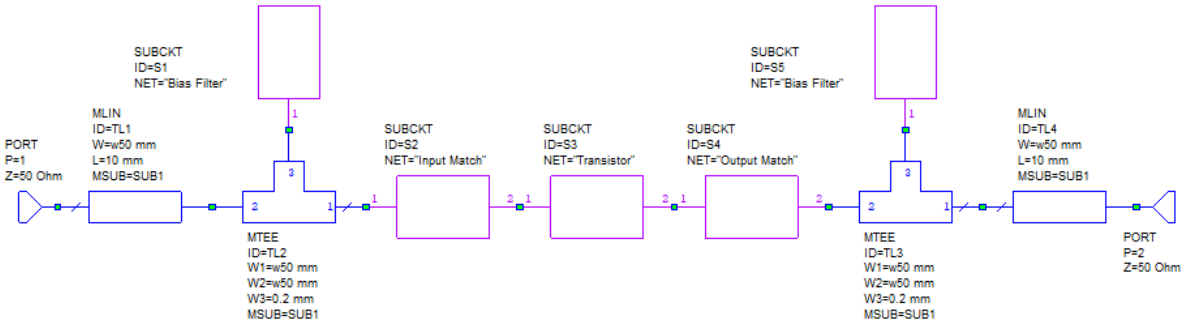

Fig. 11 Schematic of the whole LNA.

- Perform an analysis of the final amplifier in a frequency band equal to the design frequency ± approx. 20% (6 – 10 GHz in our example).
- Plot the magnitude of all S-parameters in dB into the first rectangular graph as shown in Fig. 12. Into the second rectangular graph plot noise figure NF (Linear – Noise – NF, Amplifier schematic as a source) and NFMin (Transistor schematic as a source), both in dB, as shown in Fig. 13.

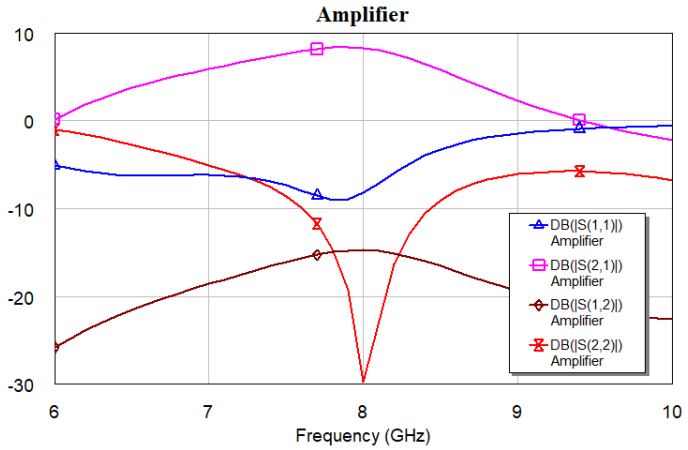

Fig. 12 S-parameters of the final LNA.

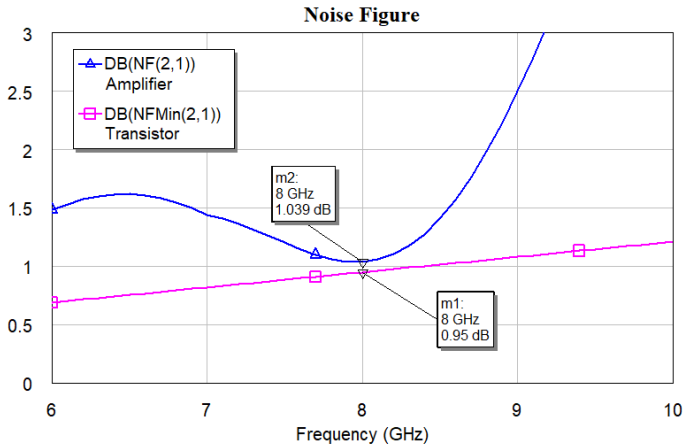

Fig. 13 Minimal reachable noise figure of the transistor alone and of the whole amplifier.

- The final amplifier is very well matched at the output; the input reflection corresponds to the applied noise matching. Its noise figure is NF = 1.04 dB, which is only slightly higher than NFMin = 0.95 dB. The noise figure increase is caused by IMC losses.

The layout describes the physical arrangement of microstrip lines at the substrate. It can be used for the manufacturing of a mask used for manufacturing a printed circuit board. The layout can be viewed from the resulting Amplifier schematic:

- At first, a package must be assigned to the transistor. Switch to the LAYOUT folder (in the basic PROJECT − ELEMENTS level), click to CELL LIBRARIES and, using the right mouse, activate IMPORT CELL LIBRARY and load the PACKAGES.GDS file (in MOODLE next to this task).
- Open the Transistor schematic and assign the package. Click the right mouse button on the transistor and activate the PROPERTIES – LAYOUT function. Open LIBRARY NAME and load the Packages.gds file. Use the EPA018 package.
- It is almost always necessary to arrange the layouts of all amplifier subcircuits first. By activating CTRL+A (select all), all layout components should change in color to yellow.
- Then activate the SNAP TOGETHER function (situated at the upper bar).
- The layout can be displayed by right clicking the resulting Amplifier schematic and clicking on VIEW LAYOUT option. A new Amplifier:2 window with the layout will open.
- The final layout of the Amplifier schematic can be seen in Fig. 14.

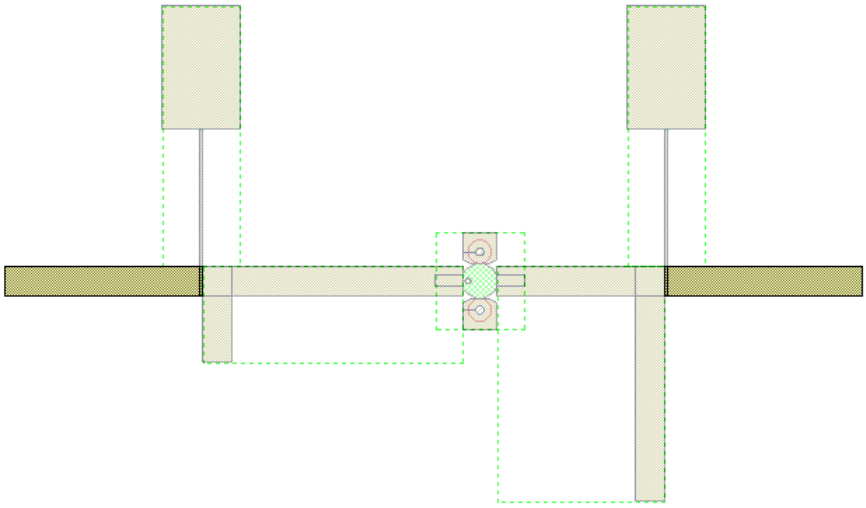

Fig. 14 Layout of the LNA.