Chapter 11

Millimeter-Wave Flip-Chip Transitions

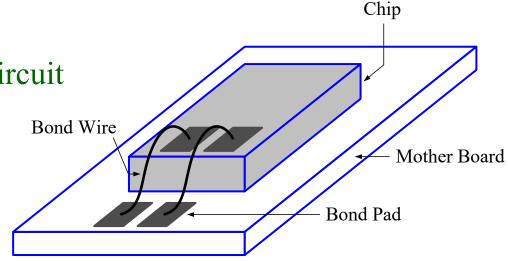
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Outline

- Introduction
- Conventional Flip-chip Transition
- Resonant Flip-chip Transition
- Inductive Compensation Flip-chip Transition
- Locally Matching Flip-chip Transition
- On Chip Design and Measurement Correction
- Conclusions

- Bonding Wire → Inductive
 - Multiple Bonding Wires [1]
 - Ribbon Wire [1]-[2]
 - Up to 40 GHz
 - Capacitive Matching Circuit[3]-[4]
 - Sacrifice of chip areas
 - Requirement of precise fabrication

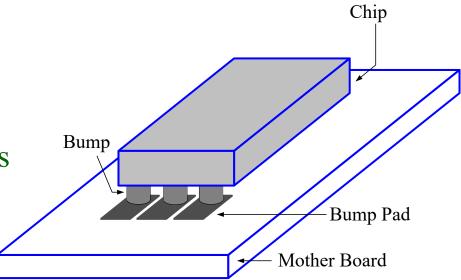


- [1] J. Y. Kim et al., IEEE APMC'00, pp. 1265-1268.
- [2] A. Sutono et al., IEEE Advanced Packaging-24, pp. 595-603, 2001.
- [3] U. Goebel, IEEE EPEP'94, pp. 182-185.
- [4] T. P. Budka, IEEE MTT-49, pp. 715-718, 2001.

- Why Flip-chip over Bonding Wire
 - Short and Stable Electrical Interconnection [5]
 - Lower insertion loss
 - Good Power Distribution Fidelity [6]
 - Good Heat Sinking Ability [7]
 - Good Surface Wave Immunity [8]
 - Available Fabrication in Millimeter-wave Frequencies[9]

- [5] T. Krems et al., IEEE MTT-S'96, pp. 247-250.
- [6] H. Hashemi et al., IEEE EPEP'96, pp. 24-26.
- [7] E. Wolf, Proc. Semiconductor Packaging Symposium, 2000.
- [8] T. Krems et al., IEEE MTT-S'97, pp. 987-990.
- [9] Y. Arai et al., IEEE MTT-45, pp. 2261-2266, 1997.

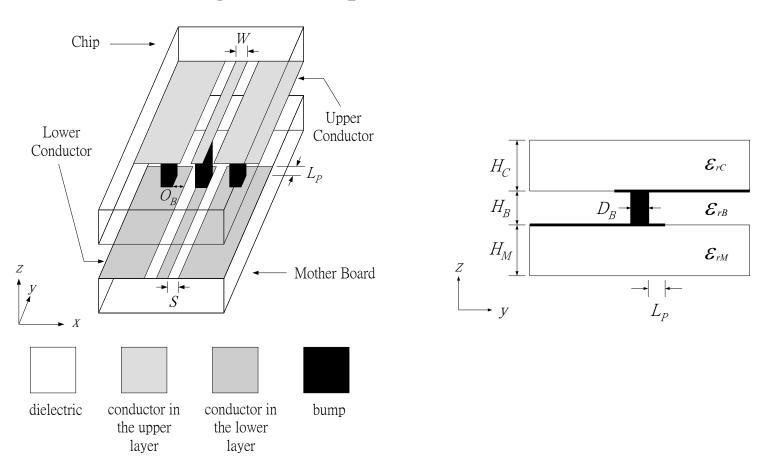
- Flip-chip → Capacitive
 - Geometry of the Bumps
 - e.g. Bump pad and height [10] Bump cross section [11]
 - Structure of the Transitions
 - e.g. Staggered structure [12] Resonant structure [13]
 - Impedance Matching
 - e.g. Compensated structure [11]
 Locally matching structure [14]



- [10] W. Heinrich et al., IEEE MTT-S'98, p. 1083.
- [11] A. Jentzsch et al., IEEE MTT-S'99, pp. 637-640.
- [12] H. H. M. Ghouz et al., IEEE MTT-44, p. 2550, 1996.
- [13] C. L. Wang et al., IEEE MTT-S'99, pp. 1423-1426.
- [14] C. L. Wang et al., IEEE MTT-S'02, pp. 1397-1400.

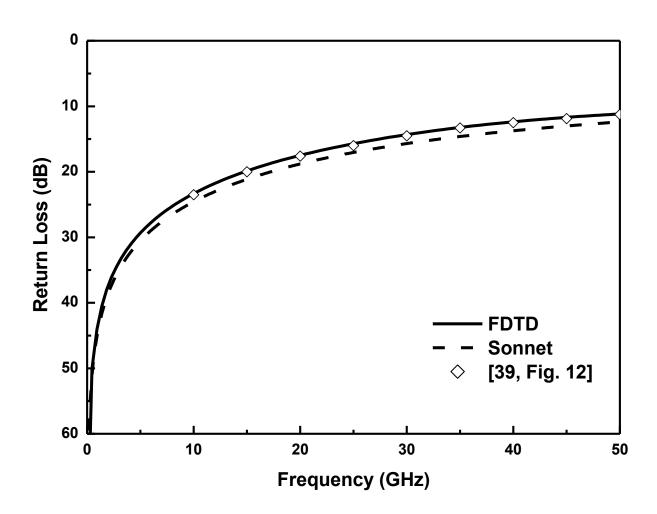
- Various Structure Achievement
 - Two Resonant Designs
 - Control of the large return loss region
 - Optimization up to millimeter-wave frequencies
 - Inductive Compensation Design
 - A systematic design rule for implementing the inductive circuit
 - Locally Matching Technique
 - Enhancement of the frequencies above millimeter-wave
 - On Real Chip Design
 - Consideration of the conductor thickness.
 - A procedure for acquiring the correct return loss level

- Configuration
 - Use Rectangular Bump Cross Section [10]

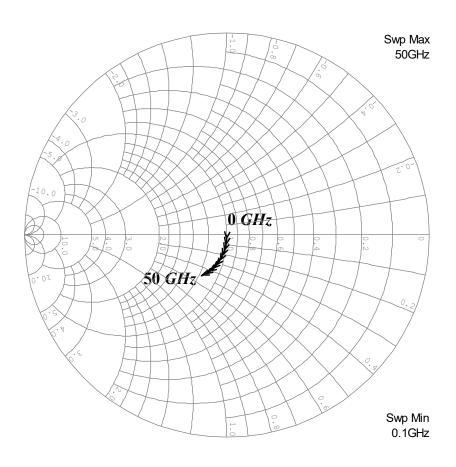


 $H_{C}\!\!=\!\!H_{M}\!\!=\!\!0.36\mathrm{mm},\ W\!\!=\!\!S\!\!=\!\!0.12\mathrm{mm},\ H_{B}\!\!=\!\!D_{B}\!\!=\!\!0.12\mathrm{mm},\ L_{P}\!\!=\!\!O_{B}\!\!=\!\!0\mathrm{mm}\ ,\ \varepsilon_{rM}\!\!=\!\!12.9,\ \varepsilon_{rB}\!\!=\!\!1,\ \varepsilon_{rC}\!\!=\!\!12.9.$

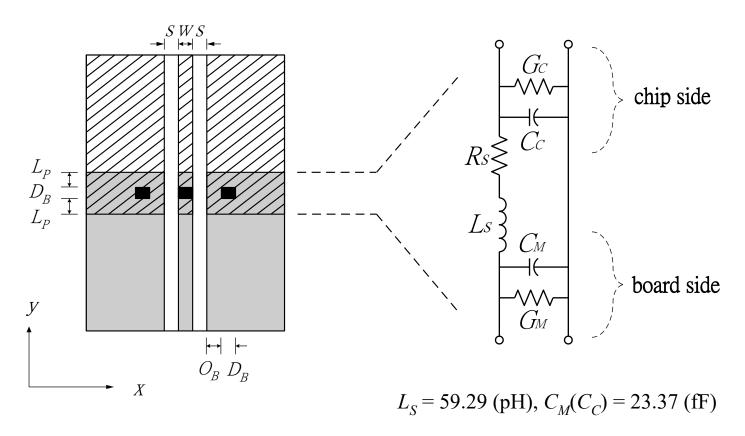
Comparison between Different Methods



• S_{11} Plotted on the Admittance Smith Chart

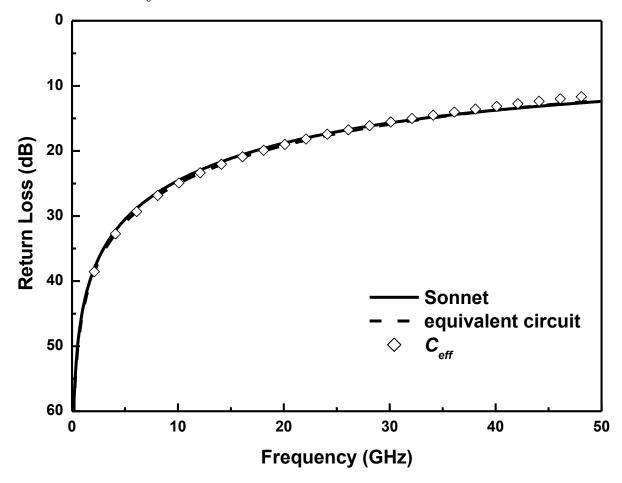


- Equivalent Circuit Model [12]
 - Extracted Using ABCD Matrix by Least Square Method



• Return Loss of Equivalent Circuit Model [11]

$$C_{eff} = (C_M + C_C) - \frac{L_S}{Z_0^2} = 29.11 \text{ (fF)}$$



• The Influence of Bump Diameter D_B on L_S and $C_M(C_C)$

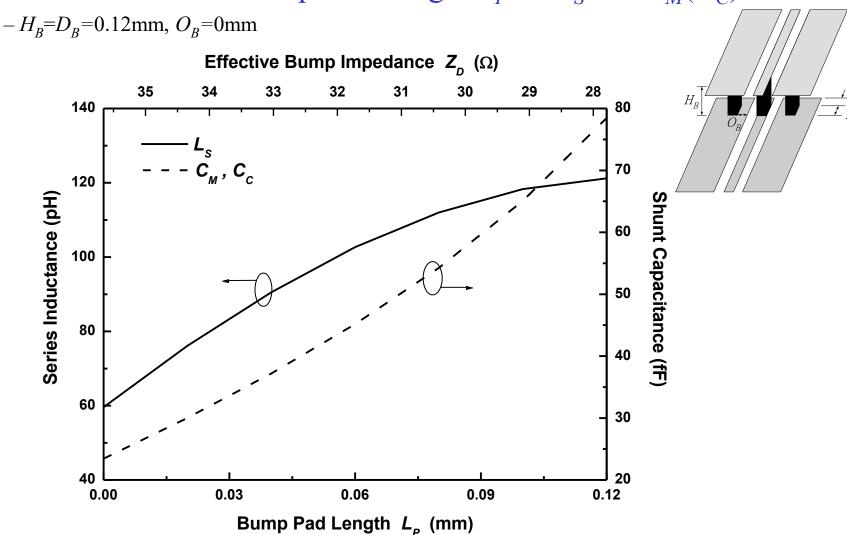
$$-H_{B}=0.12 \text{mm}, L_{p}=O_{B}=0 \text{mm} \qquad Z_{D}=\sqrt{L_{S}/(C_{M}+C_{C})}$$
 Effective Bump Impedance Z_{D} (Ω)
$$-L_{S}$$

$$---C_{M}, C_{C}$$
Shunt Capacitan C

• The Influence of Bump Height H_B on L_S and $C_M(C_C)$

 $-D_B = 0.12$ mm, $L_P = O_B = 0$ mm Effective Bump Impedance Z_{p} (Ω) Series Inductance (pH) Shunt Capacitance (fF) 0.1 0.2 0.3 Bump Height H_{R} (mm)

• The Influence of Bump Pad Length L_P on L_S and $C_M(C_C)$



• The Influence of Bump Offset O_B on L_S and $C_M(C_C)$

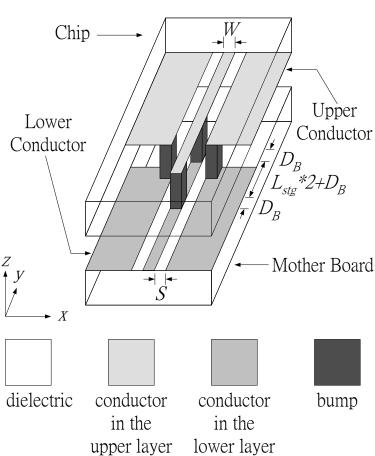
 $-H_B = D_B = 0.12$ mm, $L_P = 0$ mm Effective Bump Impedance Z_{n} (Ω) 46 48 36 38 40 42 44 120 30 110 28 Series Inductance (pH) Shunt Capacitance (fF) 100 26 90 80 70 22 60 50 20 0.06 0.12 0.18 0.00 0.24 0.30 0.36 Bump Offset O_R (mm)

Summary

- Three methods are in a good agreement.
- The equivalent circuit resembles a low pass prototype
- The conventional flip-chip possesses a capacitive effect
- Ways to lower down the capacitive effect:
 - Reduce the Bump Diameter
 - Lengthen the Bump Height
 - Minimize the Bump Pad Length
 - Maximize the Bump Offset

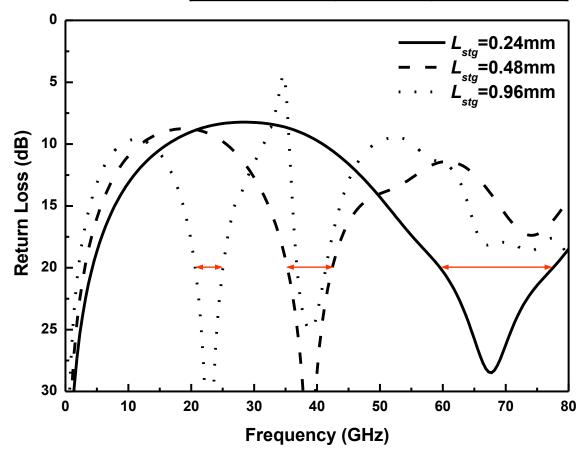
- Single Resonance Design
 - Simulated via FDTD
 - Control of Resonant Length $(L_{stg}*2+D_B)$
 - Sacrifice of Chip Areas

 $W=S=D_B=0.12$ mm, other parameters are the same as conventional

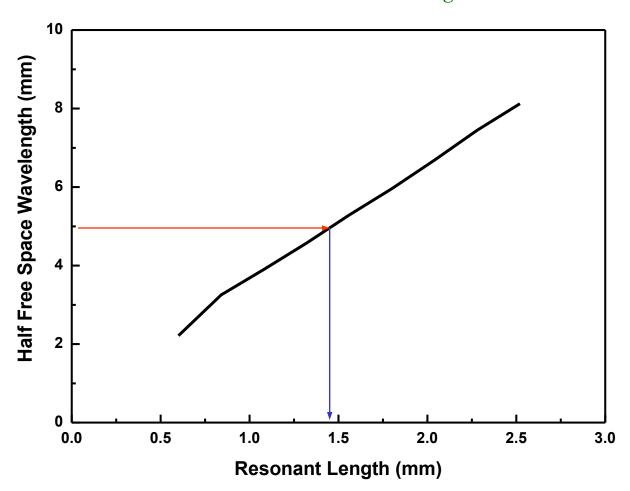


Return Loss

	f_0 (GHz)	20dB BW (%)
$L_{stg} = 0.24 \text{ mm}$	68.21	26.17
$L_{stg} = 0.48 \text{ mm}$	38.91	17.65
$L_{stg} = 0.96 \text{ mm}$	22.89	18.67

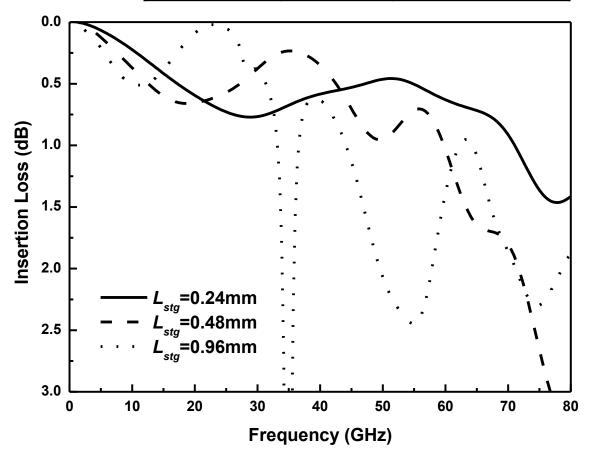


- Design Chart
 - $-\lambda_0/2$ versus Resonance Length $(L_{stg}*2+D_B)$

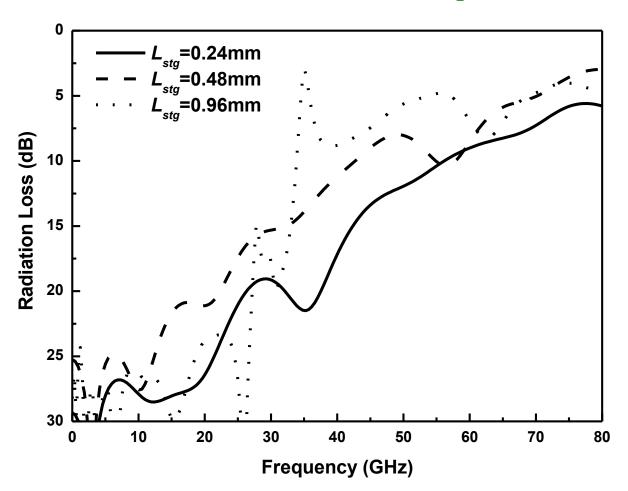


• Insertion Loss

	IL at $f_0(dB)$	IL in 20dB BW (dB)
$L_{stg} = 0.24 \text{ mm}$	0.81	<1.46
$L_{stg} = 0.48 \text{ mm}$	0.30	< 0.47
$L_{stg} = 0.96 \text{ mm}$	0.02	< 0.06

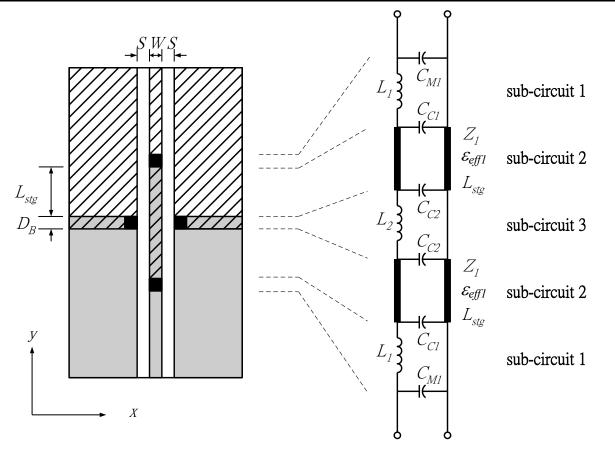


- Radiation Loss
 - Severe above Millimeter-wave Frequencies

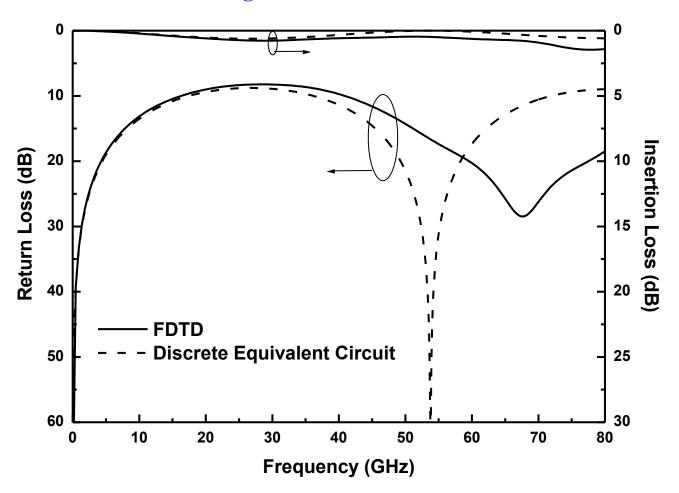


- Discrete Equivalent Circuit
 - Simulated by Sonnet and Extracted via LSM

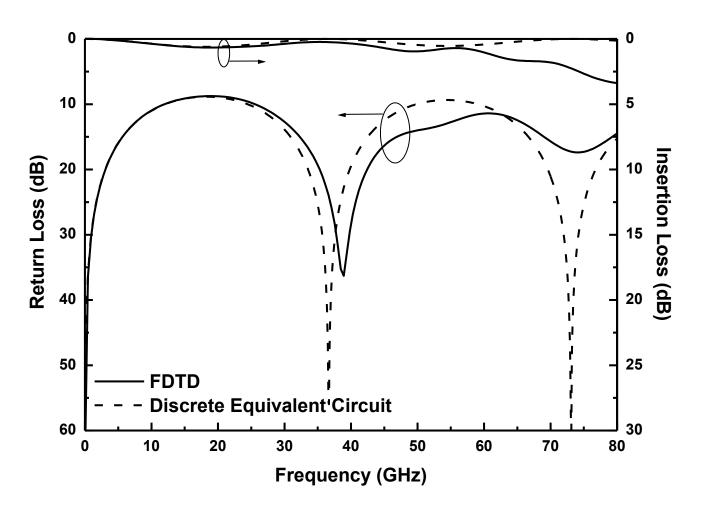
C_{MI} (fF)	$L_I(pH)$	C_{CI} (fF)	$Z_{I}\left(\Omega\right)$	$\mathcal{E}_{e\!f\!fl}$	C_{C2} (fF)	L_2 (pH)
21.01	48.04	14.42	40.07	7.70	22.83	65.17



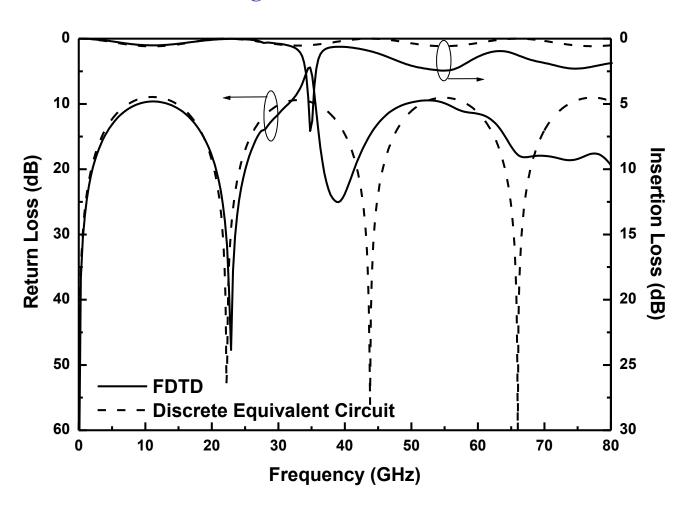
• Comparison for L_{stg} =0.24mm



• Comparison for L_{stg} =0.48mm

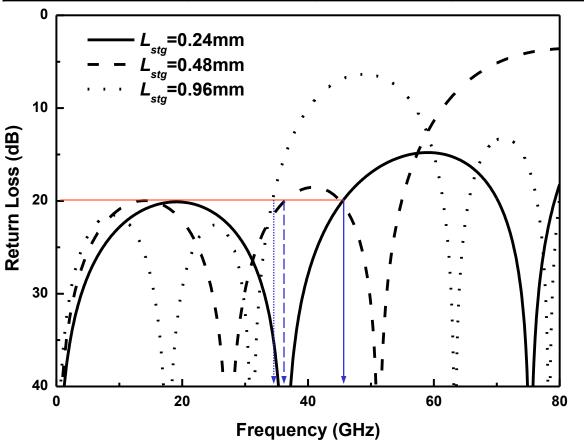


• Comparison for L_{stg} =0.96mm



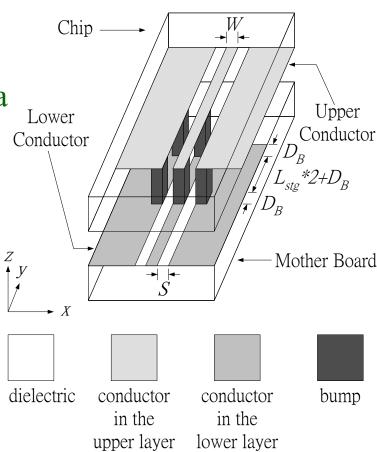
• Optimum Results

	$L_{stg} = 0.24 \text{ mm}$	$L_{stg} = 0.48 \text{ mm}$	$L_{stg} = 0.96 \text{ mm}$
$Z_{I}(\Omega)$	67.50	59.10	56.60
20dB Bound (GHz)	45.50	36.30	34.30



- Transformer Design
 - Simulated via FDTD
 - Impedance Transformer Idea
 - Sacrifice of Chip Areas
 - Better Field Confinement

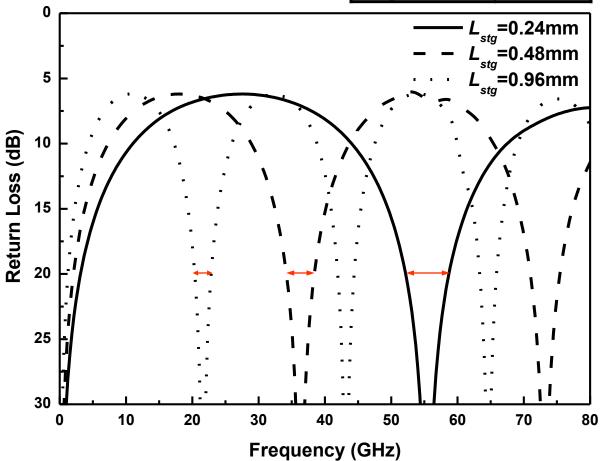
 $W=S=D_B=0.12$ mm, other parameters are the same as conventional



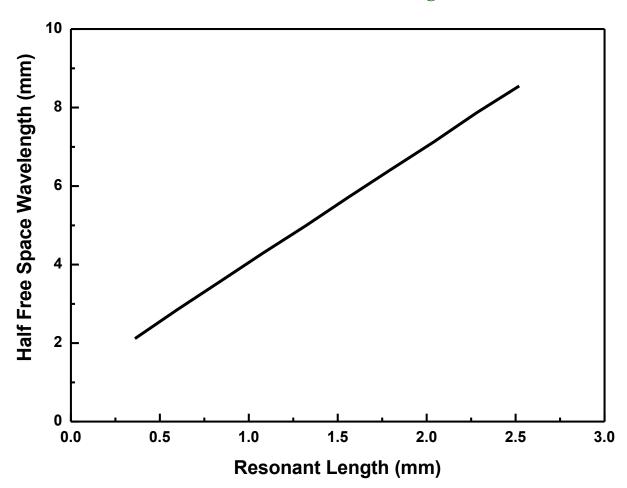
• Return Loss

- 20 dB Bandwidth: 11.5%

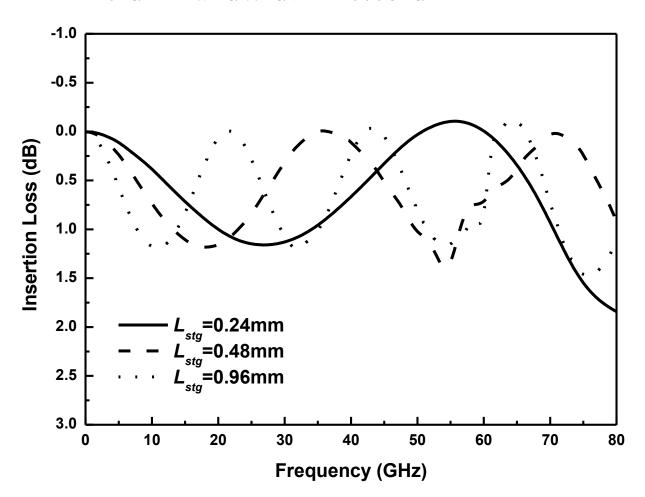
	f_0 (GHz)
L_{stg} =0.24 mm	55.54
$L_{stg} = 0.48 \text{ mm}$	36.32
$L_{stg} = 0.96 \text{ mm}$	21.67



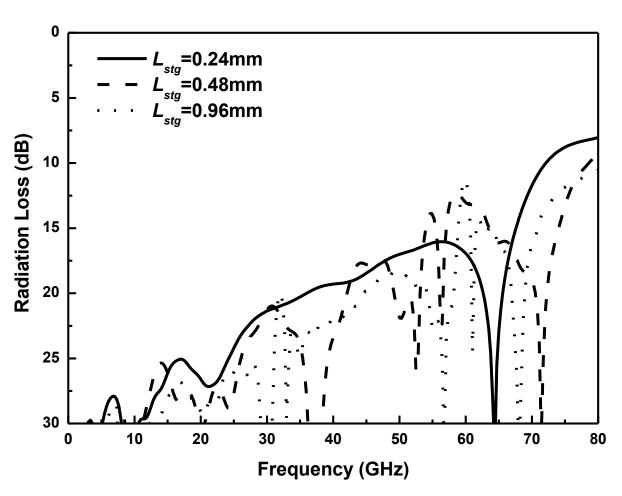
- Design Chart
 - $-\lambda_0/2$ versus Resonance Length $(L_{stg}*2+D_B)$



- Insertion Loss
 - IL in 20 dB Bandwidth > 0.05 dB

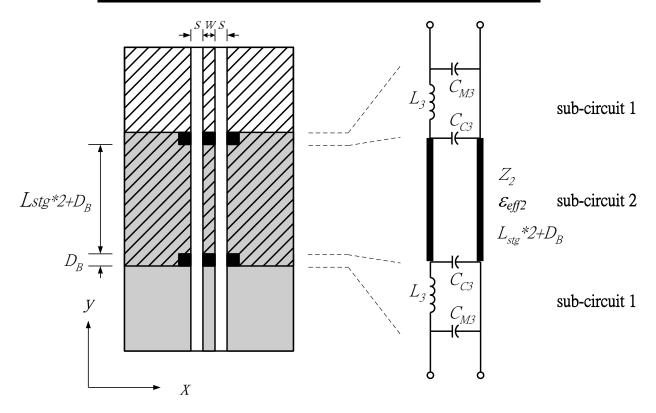


- Radiation Loss
 - Severe above 60 GHz

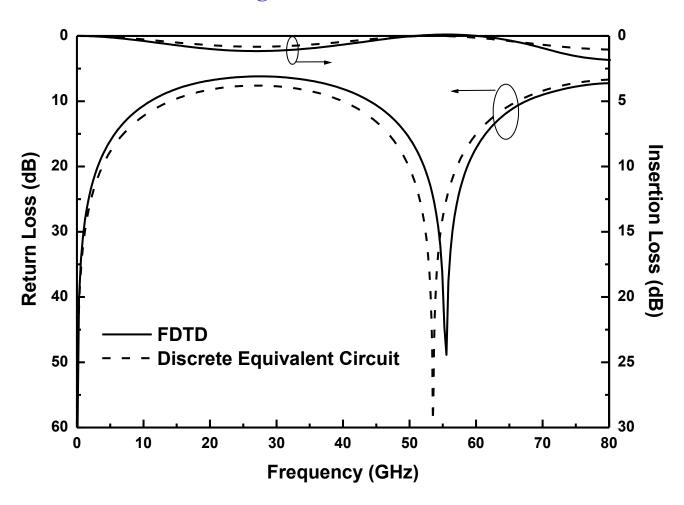


- Discrete Equivalent Circuit
 - Simulated by Sonnet and Extracted via LSM

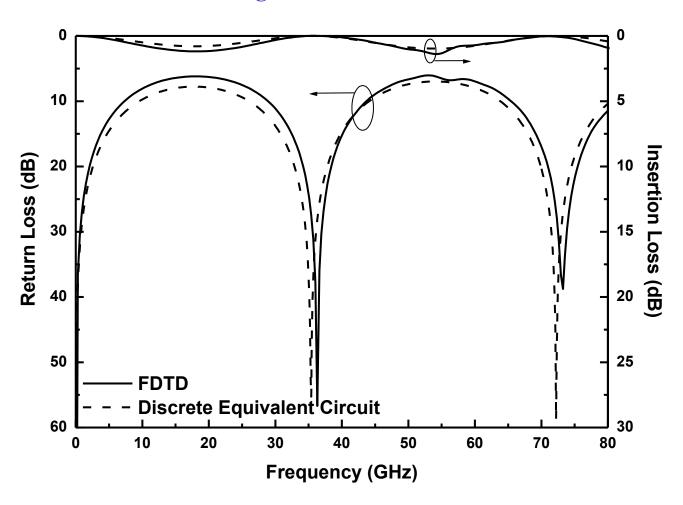
C_{M3} (fF)	$L_3(\mathrm{pH})$	C_{C3} (fF)	$Z_2(\Omega)$	$\mathcal{E}_{e\!f\!f2}$
23.05	41.42	18.32	37.78	8.45



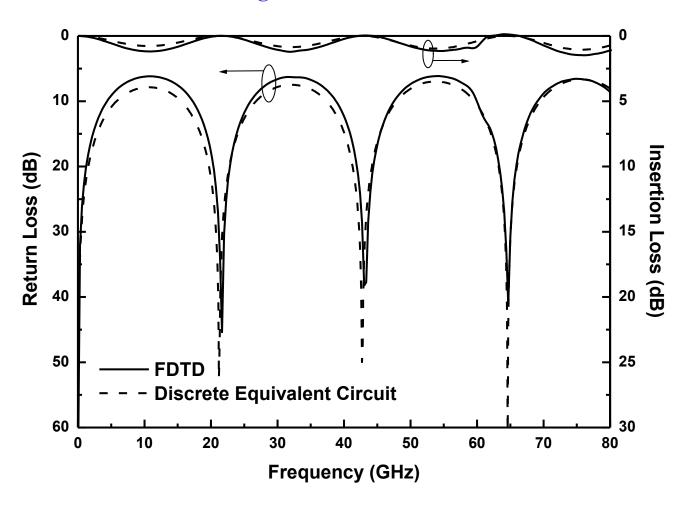
• Comparison for L_{stg} =0.24mm



• Comparison for L_{stg} =0.48mm

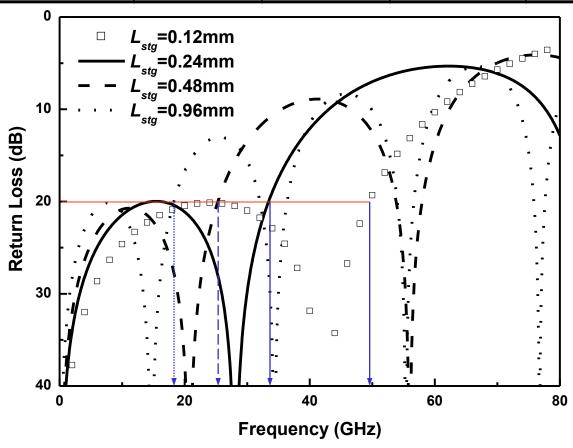


• Comparison for L_{stg} =0.96mm



• Optimum Results

	$L_{stg} = 0.12 \text{ mm}$	$L_{stg} = 0.24 \text{ mm}$	$L_{stg} = 0.48 \text{ mm}$	$L_{stg} = 0.96 \text{ mm}$
$Z_{I}(\Omega)$	96.80	58.00	55.60	53.50
20dB Bound (GHz)	49.60	33.40	25.30	18.20



Resonant Flip-chip Transition

Summary

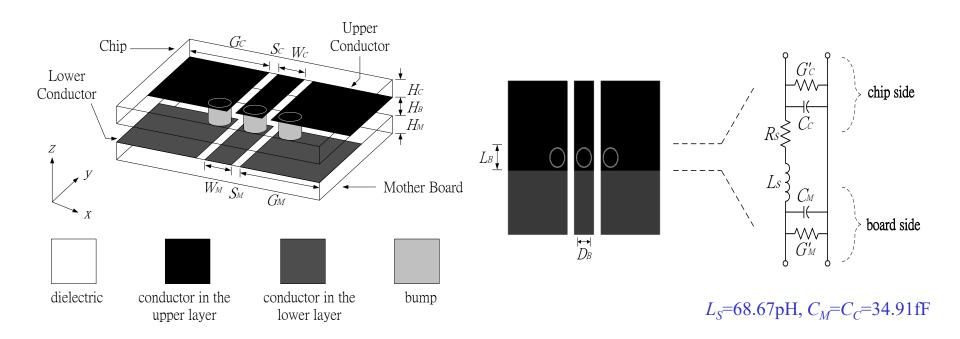
- Single Resonance Design
 - 20 dB Bandwidth: 17.5 ~ 26 %
 - Insertion Loss in 20 dB BW: 1.5 dB
 - Optimum Design

	L_{stg} =0.24 mm	$L_{stg} = 0.48 \text{ mm}$	$L_{stg} = 0.96 \text{ mm}$
20dB Bound (GHz)	45.50	36.30	34.30

- Transformer Design
 - 20 dB Bandwidth: 11.5 %
 - Insertion Loss in 20 dB BW: 0.05 dB
 - Optimum Design

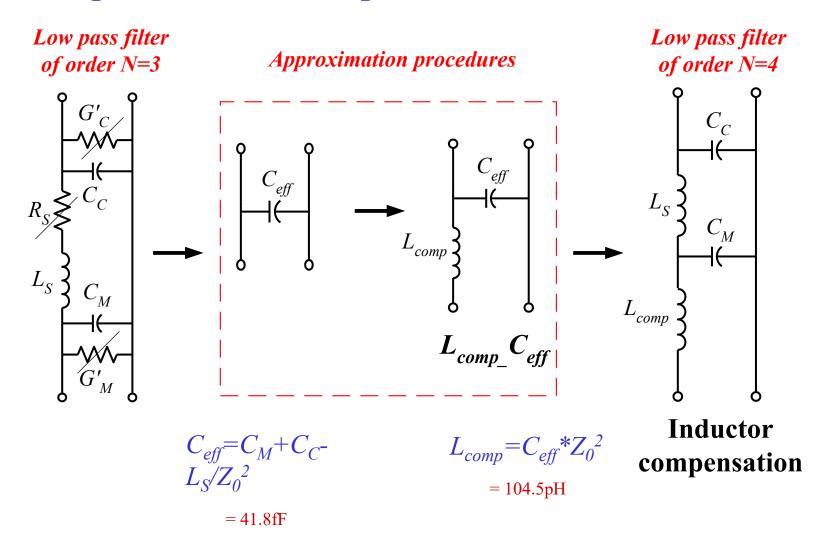
	$L_{stg} = 0.12 \text{ mm}$	$L_{stg} = 0.24 \text{ mm}$	$L_{stg} = 0.48 \text{ mm}$	$L_{stg} = 0.96 \text{ mm}$
20dB Bound (GHz)	49.60	33.40	25.30	18.20

- Structure Parameters
 - Introduce an Inductive Element to Compensate the Capacitive Effect

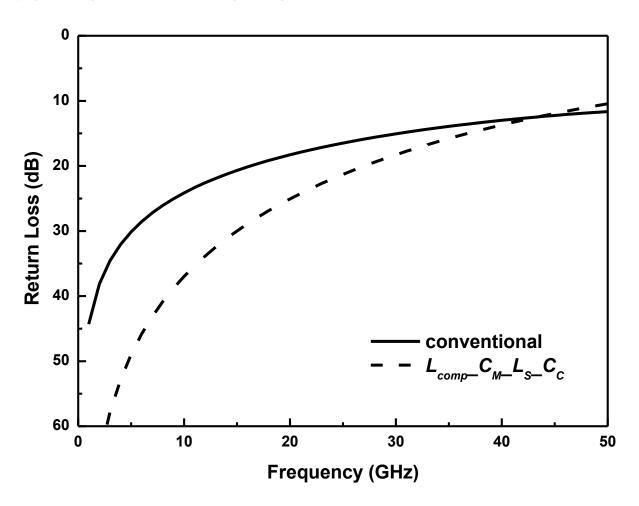


$$W_{C} = W_{M} = 200 \mu \text{m}, \ S_{C} = S_{M} = 70 \mu \text{m}, \ G_{C} = G_{M} = 600 \mu \text{m}, \ H_{C} = H_{B} = H_{M} = 127 \mu \text{m}, \ \varepsilon_{r} = 10.2.$$

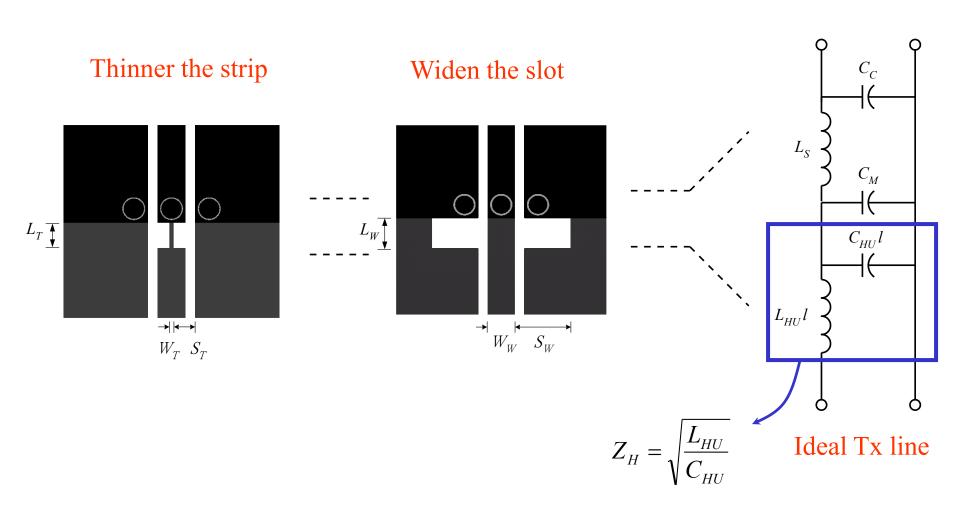
• Lumped Element Compensation



 Comparison between Inductance Compensation and Conventional Transition



• High Impedance Transmission Line Compensation [11]



- High Impedance Transmission Line Compensation
 - Matching Condition

$$\sqrt{\frac{L_{HU}l}{C_{HU}l + C_{eff}}} = Z_0 \longrightarrow l = (\frac{\omega_H}{\beta_H})(\frac{Z_H Z_0^2 C_{eff}}{Z_H^2 - Z_0^2})$$

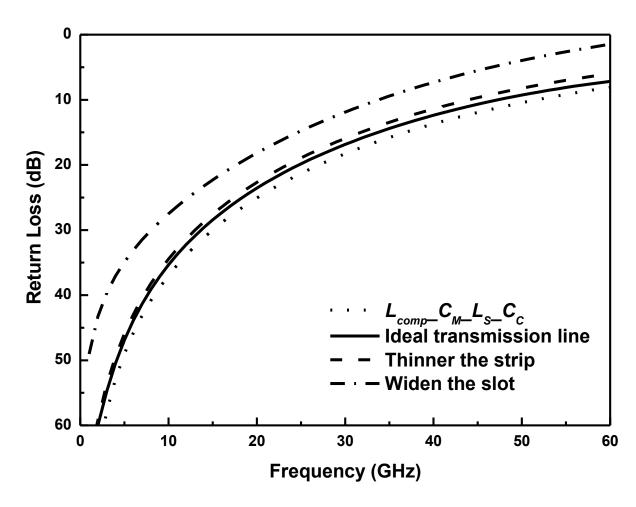
$\bullet Z_H = 100\Omega$

βl _{30GHz} (°)	$W_T(\mu m)$	$S_T(\mu m)$	$L_T(\mu \mathrm{m})$	$W_W(\mu \mathrm{m})$	$S_W(\mu \mathrm{m})$	$L_W(\mu \mathrm{m})$
15.048	30	155	185	200	410	230

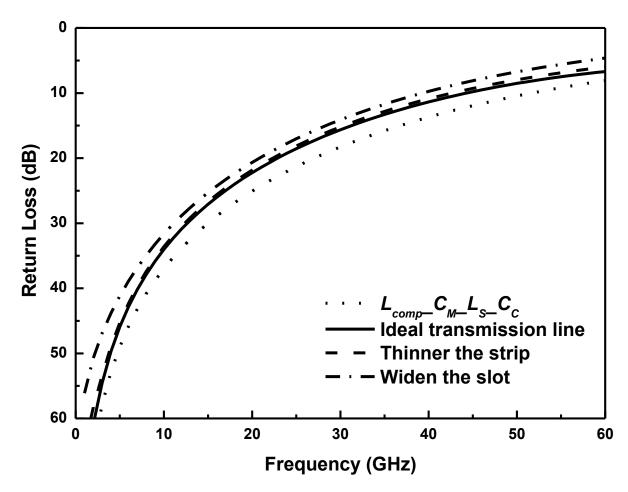
$\bullet Z_H = 76\Omega$

βl _{30GHz} (°)	$W_T(\mu m)$	$S_T(\mu m)$	$L_T(\mu m)$	$W_W(\mu \mathrm{m})$	$S_W(\mu m)$	$L_W(\mu\mathrm{m})$
25.554	30	130	315	200	240	340

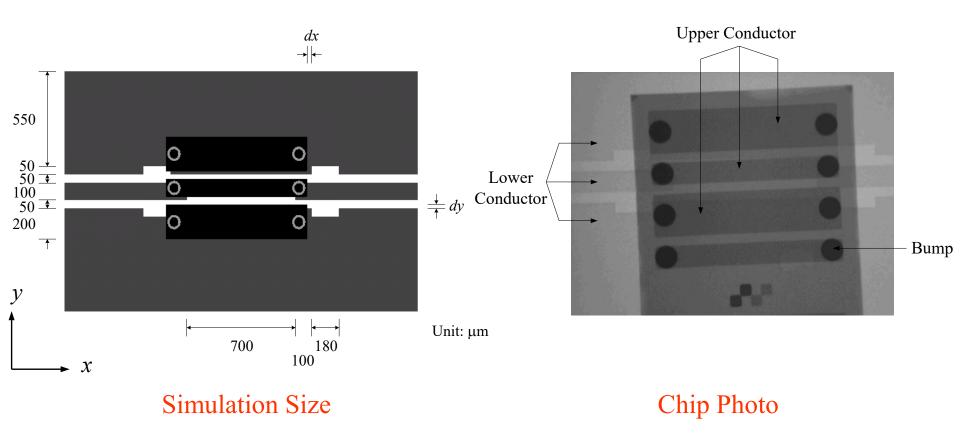
• $Z_H = 100\Omega$



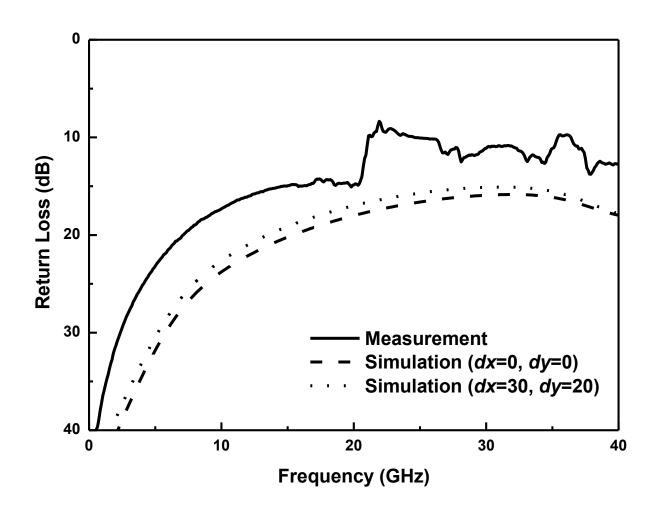
• $Z_H = 76\Omega$



Experiment



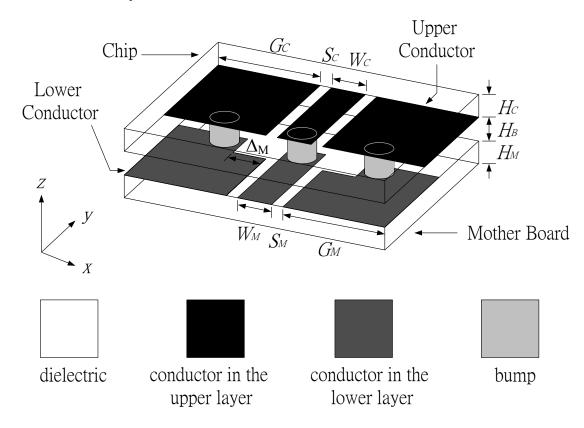
Comparison between Simulation and Measurement



- Summary
 - Lumped Inductance
 - This can well compensate the capacitive effect at low frequencies
 - Ideal High Impedance Transmission Line
 - Higher impedance results in smaller length
 - Higher impedance can better represent the inductance
 - High Impedance Compensation
 - Thin strip has little discontinuity effect than wide slot
 - The Best Choice is to Adopt
 - higher impedance implemented with thin strip
 - Experiment
 - Return Loss is better than 15dB up to 20 GHz

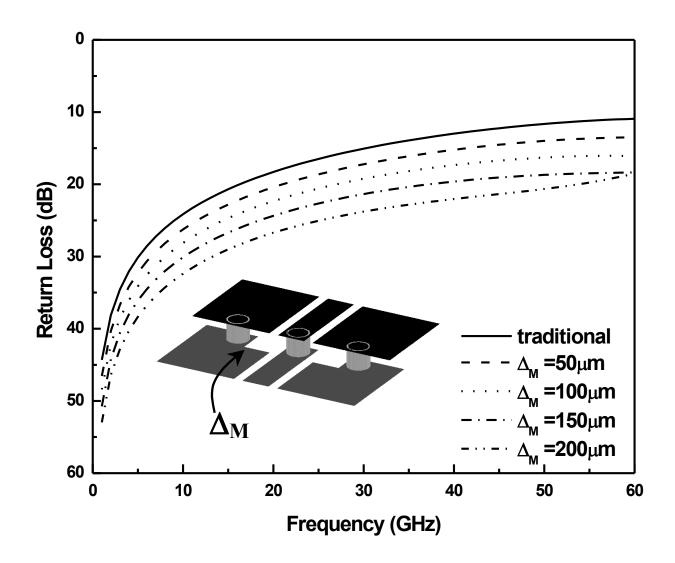
• Ground Retreat on Mother Board [15]

- Make
$$Z_D = \sqrt{L_S/(C_M + C_C)}$$
 Close to 50 Ω

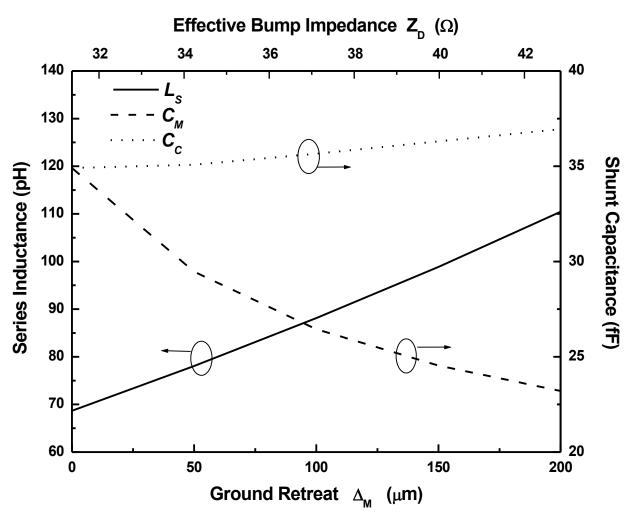


$$W_C = W_M = 200 \mu \text{m}, \ S_C = S_M = 70 \mu \text{m}, \ G_C = G_M = 600 \mu \text{m}, \ H_C = H_B = H_M = 127 \mu \text{m}, \ \varepsilon_r = 10.2.$$

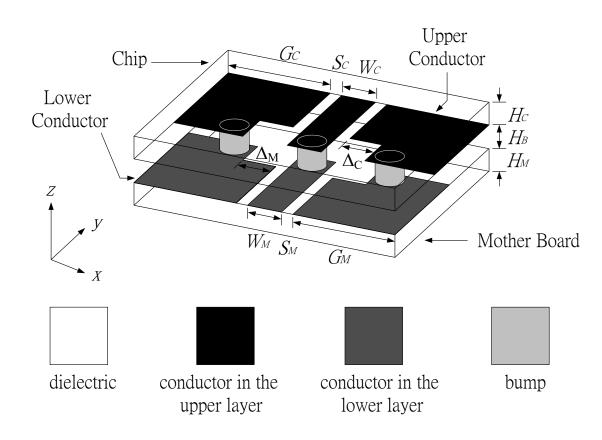
Return Loss



• Equivalent Circuit Values versus Δ_{M}

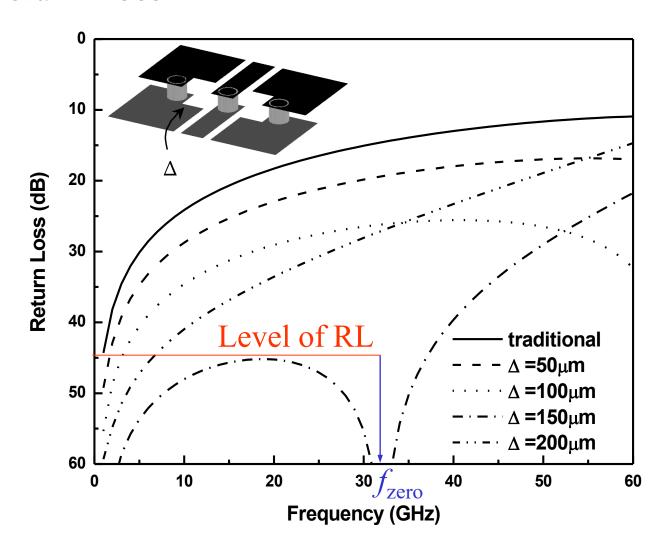


Ground Retreats Both on Mother Board and Chip

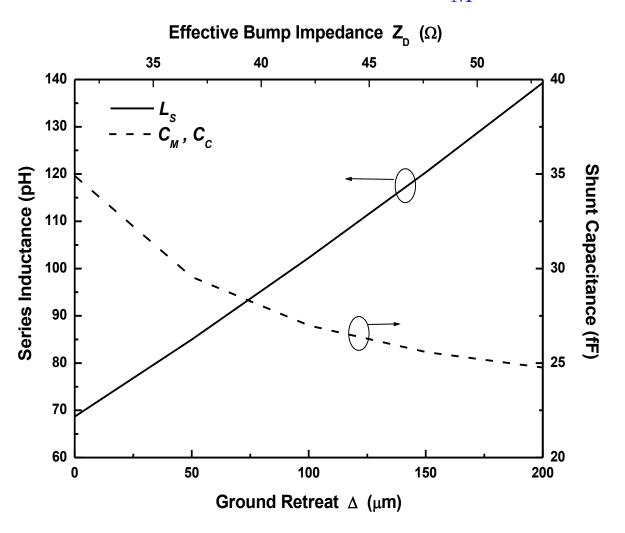


$$W_C = W_M = 200 \mu \text{m}, S_C = S_M = 70 \mu \text{m}, G_C = G_M = 600 \mu \text{m}, H_C = H_B = H_M = 127 \mu \text{m}, \varepsilon_r = 10.2.$$

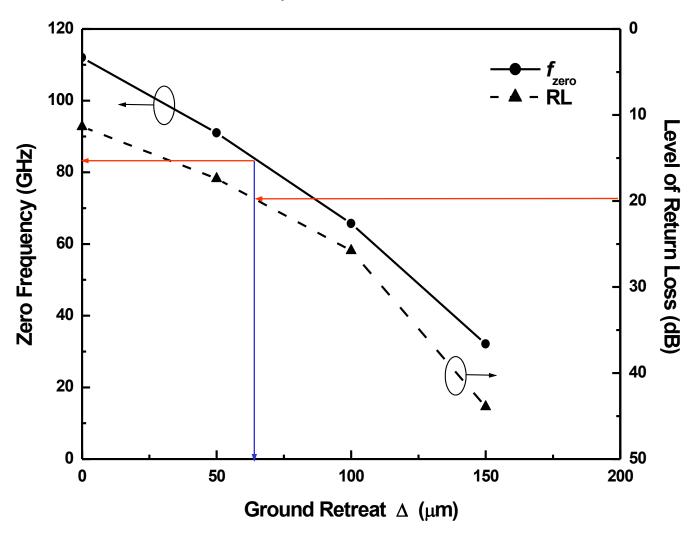
• Return Loss



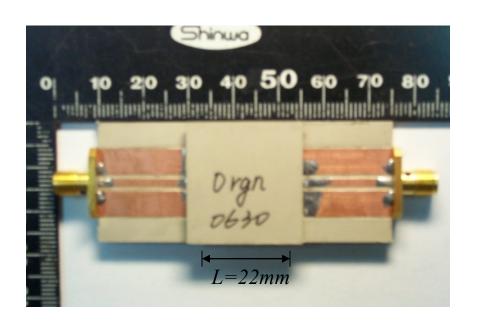
• Equivalent Circuit Values versus Δ_{M}



• Design Chart $f_{zero} = \frac{1}{2\pi} \sqrt{\frac{1}{L_s C_c^2}} (2C_C - \frac{L_s}{Z_o^2})$



- 10 times Scaled up Circuit
 - Fabricated on RT/Duroid6010 of ϵ_r =10.2, and Measured with TRL Calibration.



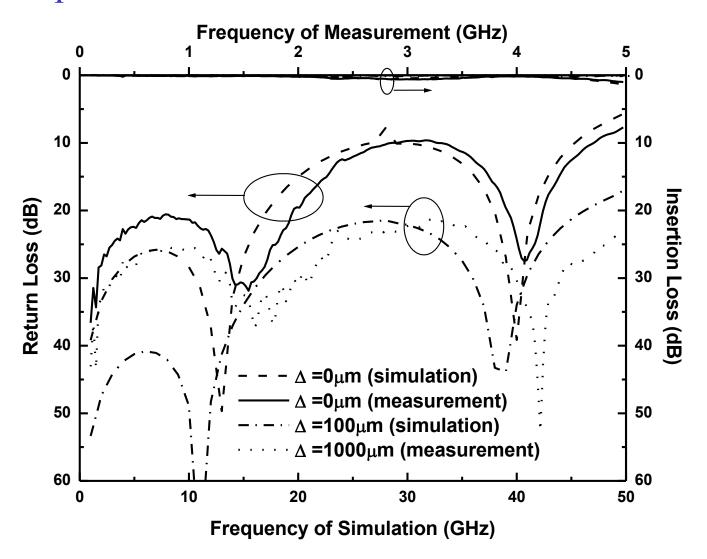


Top view of the whole circuit

Local view of the bump area

Many thanks to Mr. Shih-Chieh Yen and Shih-Je Yang for helps on the fabrication. Many thanks to Mr. Wen-Hua Tu for the suggestions in the measurement.

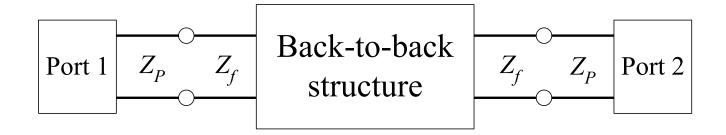
Comparison between Simulation and Measurement



Summary

- Ground Retreat on Mother Board
 - The response of return loss does not change severely with $\Delta_{\rm M}$
 - The performance is still restricted by C_C on the chip side
- Ground Retreats on Mother Board and Chip
 - This structure exhibits good transition when Δ is chosen well to match the impedance.
 - The area occupied is in the transverse direction of propagation and the frequency band is wide.
 - A design graph built with four simulated points can be used to design the return loss level validated up to the resonant frequency.
 - Measurement results of the ten-times scaled up circuit show good agreement with the simulation results.

- Design Consideration
 - Simulated with Zero Conductor Thickness
 - $Z'_f = Z'_P = 52\Omega$
 - Measured with Real Conductor Thickness
 - $Z_P = 50\Omega$

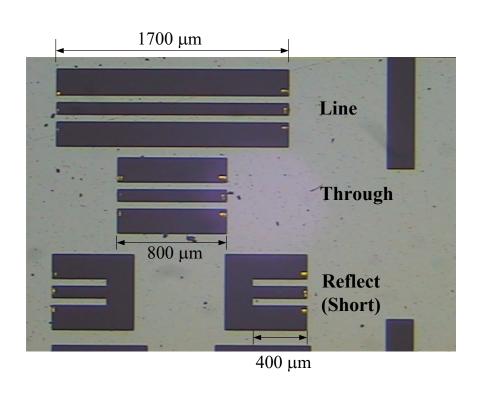


 Z_f : characteristic impedance of feed line

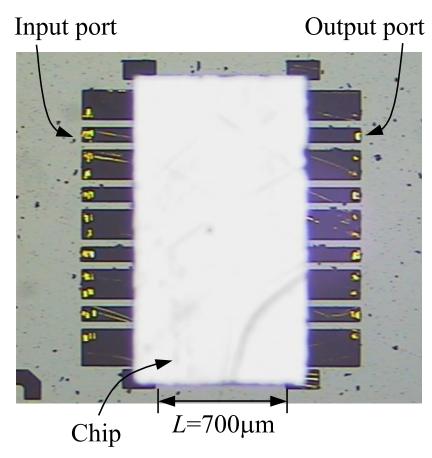
 Z_P : characteristic impedance of port

Many thanks to Airwave Inc. for fabricating the real flip-chip circuits, and Mr. Kun-You Lin and Ping-Yu Chen for doing the on wafer measurements.

Chip Photo



TRL Calibration Kit

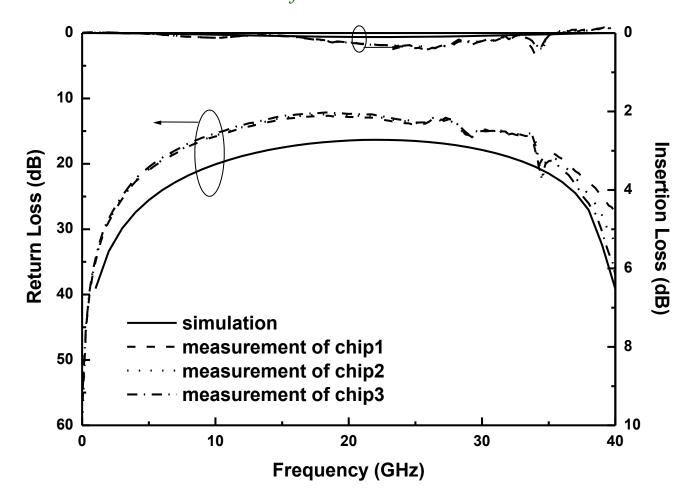


Back to Back Circuit

Bump: H_{R} =35µm, D_{R} =80µm

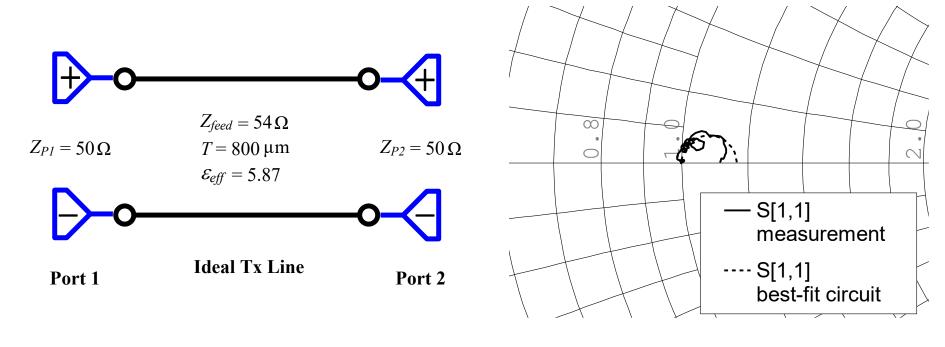
Mother Board (GCPW): H_M =381 μ m, ε_r =9.9, Chip (CPW): H_C =635 μ m, ε_r =12.9

- Ground Retreat on Mother Board Only $\Delta_M = 50 \mu m$
 - Measured Based on $Z_f = Z_p = 50\Omega$



Mother Board: W_M =100 μ m, S_M =50 μ m, G_M =200 μ m. **Chip:** W_C =100 μ m, S_C =50 μ m, G_C =200 μ m.

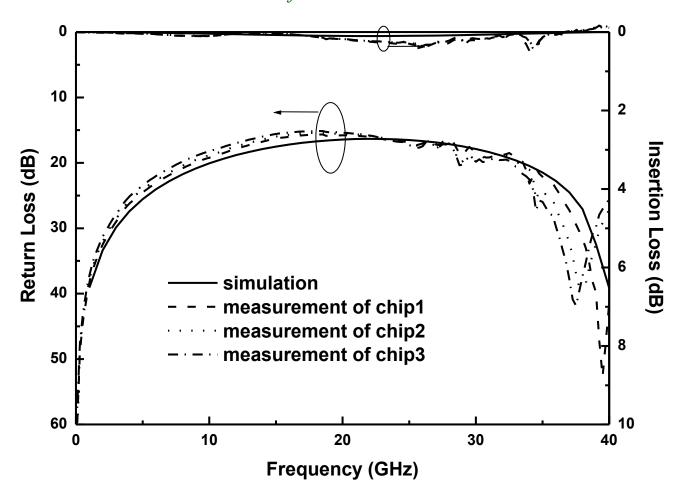
- Circuit for Acquiring the Correct Feedline Impedance
 - $-Z_f$ is Estimated to be 54 Ω



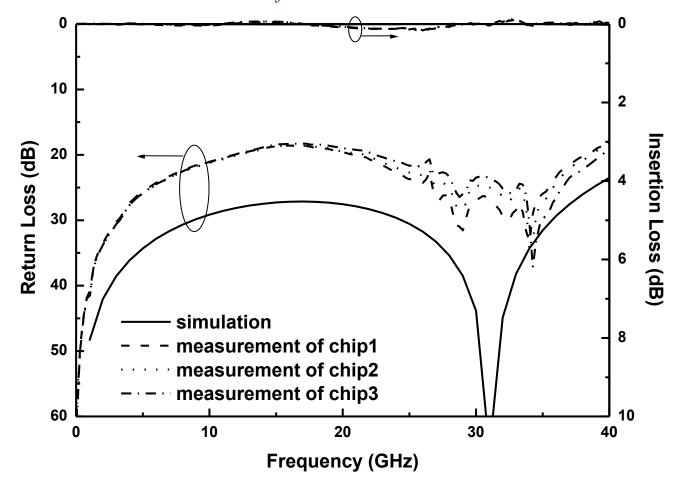
Equivalent Circuit

Comparison Result

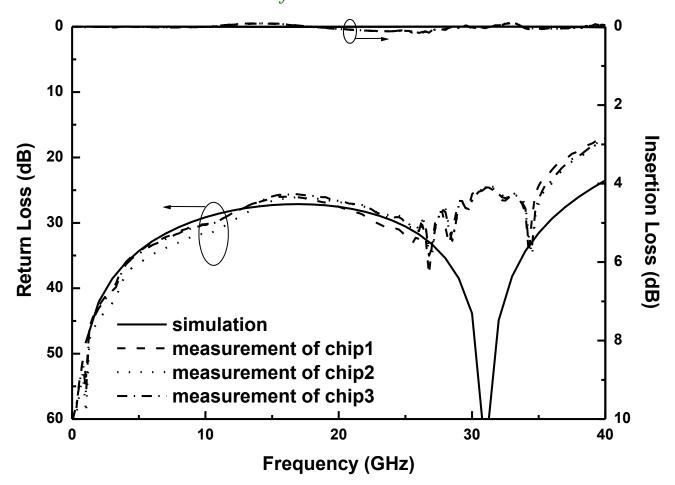
- Ground Retreat on Mother Board Only $\Delta_M = 50 \mu m$
 - Measured Based on $Z_f = Z_p = 54\Omega$



- Ground Retreat on Both Sides $\Delta_M = 75 \mu m$, $\Delta_C = 50 \mu m$
 - Measured Based on $Z_f = Z_p = 50\Omega$



- Ground Retreat on Both Sides $\Delta_M = 75 \mu m$, $\Delta_C = 50 \mu m$
 - Measured Based on $Z_f = Z_p = 54\Omega$



- Summary
 - Simulation
 - zero conductor thickness based on $Z'_f = Z'_P = 52\Omega$ is adopted
 - Measurement
 - Original measurement based on $Z_f = Z_P = 50\Omega$ is calibrated to $Z_f = Z_P = 54\Omega$
 - 4 to 10 dB error in RL is corrected
 - Ground Retreat on Mother Board Only
 - 15 dB RL up to 35 GHz
 - Ground Retreats on Both Sides
 - 25 dB RL up to 35 GHz

Conclusions

Conclusions

- Conventional Flip-chip Transition
 - This possesses a capacitive effect
- Resonant Flip-chip Transition
 - The resonant length is controlled to result in a resonant dip in the desired frequency band
 - Discrete equivalent circuit could be optimized up to millimeterwave frequencies
 - Chip areas are sacrificed in the longitudinal direction
- Inductive Compensation Flip-chip Transition
 - Lumped inductance could well compensate the capacitive effect
 - High impedance line with higher impedance and thin strip could result in the best performance and smallest size
 - This saves chip areas
 - This could only enhance the performance up to millimeter-wave frequencies

Conclusions

Conclusions

- Locally Matching Flip-chip Transition
 - Ground retreat on mother board could substantially improve the performance
 - Ground retreat on both sides could greatly improve the performance
 - Wide band performance are obtained with chip areas sacrificed in the transverse direction
- On Chip Design
 - Simulation considering conductor thickness with zero conductor thickness and somewhat higher impedance is adopted
 - Measurement correction procedures are required to calibrate the return loss level due to fabrication error