## *Chapter 2*

# Ideal Transmission Line Fundamentals

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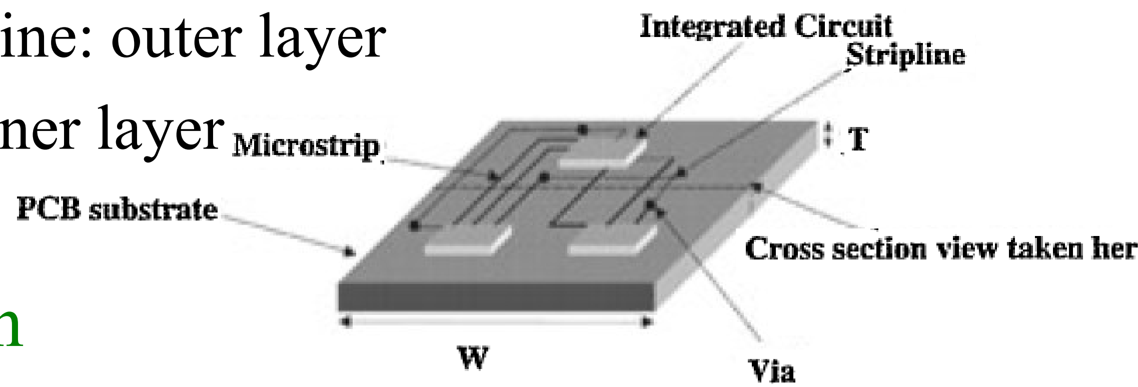
# Outline

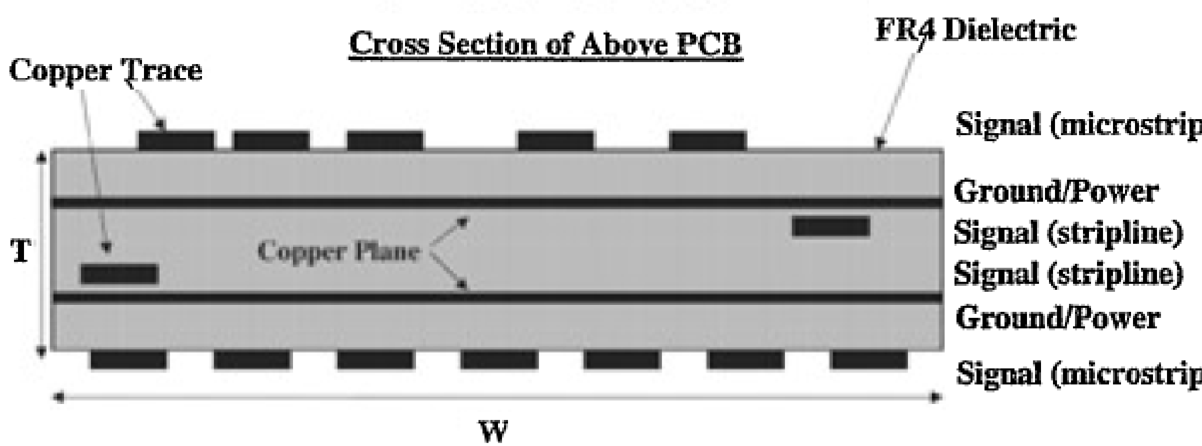
- Transmission Line Structures on a PCB or MCM
- Wave Propagation
- Transmission Line Parameters
- Launching Initial Wave and Transmission Line Reflections
- Additional Examples

# Transmission Line Structures on a PCB or MCM

- Typical Design Built on a PCB
  - 3D View
    - Microstrip line: outer layer
    - Stripline: inner layer



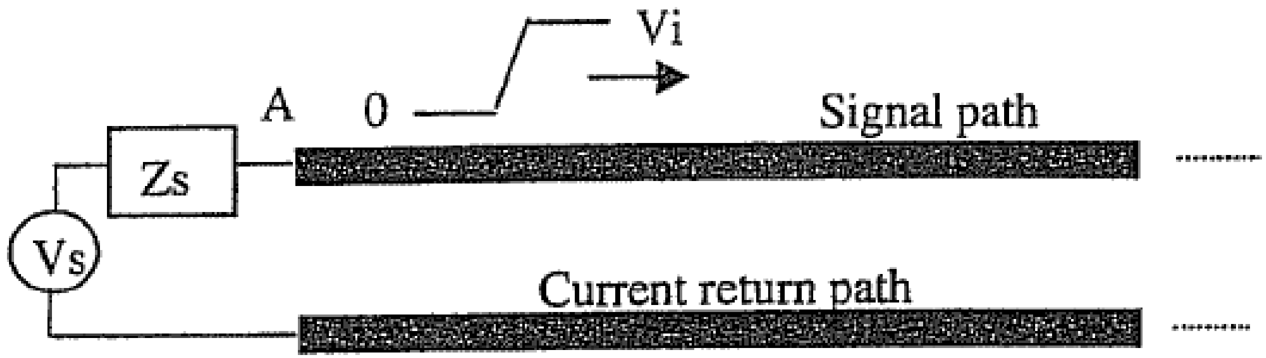

  - Cross Section
    - For *ac* signal: Ground/Power could be viewed as *ac* ground.




Typical conductor: copper
Typical dielectric: FR4

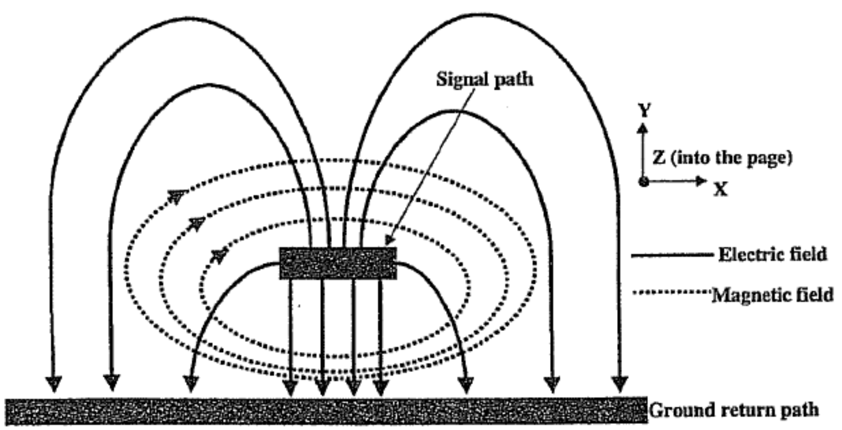
# Wave Propagation

- Transmission Line Propagation
  - Typical Method of Portraying a Digital Signal
    - When the rise time or fall time is small compared to the propagation delay down the trace.
    - Wave propagation is like the waterfront.
      - Voltage: height of the water
      - Current: flow of the water
    - $V_s$ and $Z_s$: source or driver (output buffer)



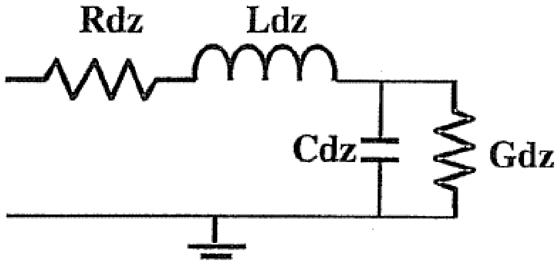
# Transmission Line Parameters

- Introduction
  - Characteristic Impedance
    - *V*/*I* for a matched load (the impedance for the wave)
  - Propagation Velocity
    - The speed of the wave
  - Relationship between (*V*, *I*) and (*E*, *H*)
    - Actually, transmission lines transfer energy using (*E*, *H*).



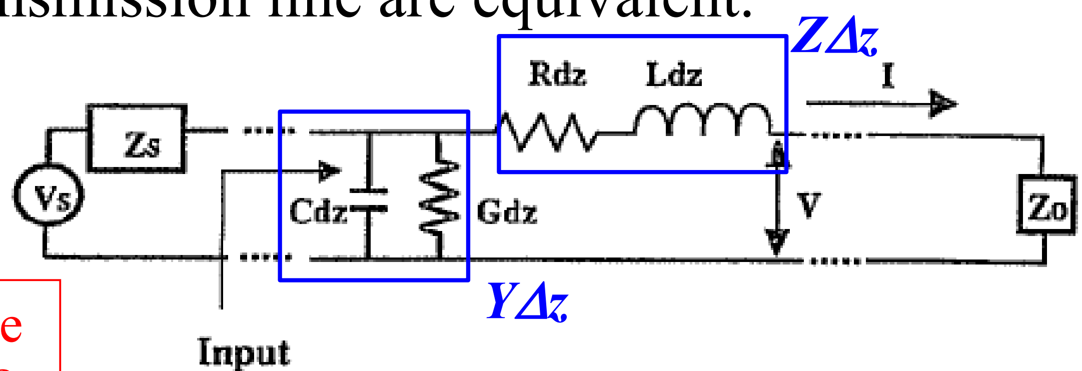
# Transmission Line Parameters

- Introduction
  - Equivalent Circuit
    - TEM: When no components of the $E$ or $H$ fields propagate in the $z$-direction.
    - $R$: the losses due to the finite conductivity of the conductor
    - $L$: the energy stored in the magnetic field
    - $C$: the energy stored in the electric field
    - $G$: the losses due to the finite resistance of the dielectric separating the conductor and the ground plane



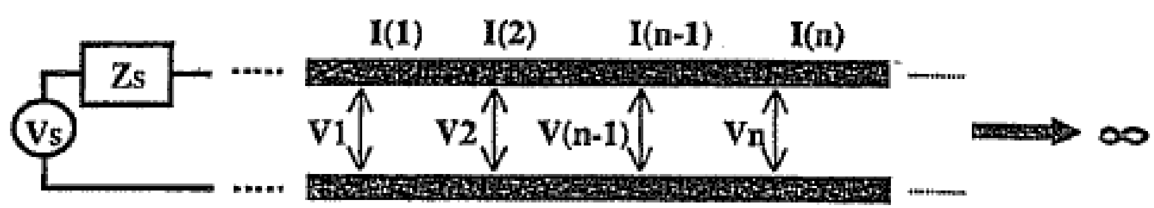
# Transmission Line Parameters

- Derivation and Detailed Descriptions
  - Characteristic Impedance
    - The following two circuit representations of a transmission line are equivalent.




(a)

How small the value of dz is reasonable?




(b)

Equivalent representation ($Z_0$ and $\gamma$) ⟹ Lossless ($Z_0$ and $\beta$)

# Transmission Line Parameters

- Derivation and Detailed Descriptions
  - Characteristic Impedance
    - With a short length of $\Delta z$, the derivation is as follows:

$jwL(\Delta z) + R(\Delta z) = Z\Delta z$ (series impedance for length of line $\Delta z$)

$jwC(\Delta z) + G(\Delta z) = Y\Delta z$ (parallel admittance for length of line $\Delta z$)

$Y\Delta z$ in parallel with $Z\Delta z + Z_0$.

$$Z(\text{input}) = Z_o = \frac{(Z_o + Z\,\Delta z)(1/Y\,\Delta z)}{Z_o + Z\,\Delta z + 1/Y\,\Delta z}$$ (assuming the load is equal to the characteristic impedance)

$$\rightarrow Z_o\left(Z\,\Delta z + Z_o + \frac{1}{Y\,\Delta z}\right) = (Z_o + Z\,\Delta z)\frac{1}{Y\,\Delta z}$$

$$\Rightarrow Z_o Z\,\Delta z + Z_o^2 + \cancel{\frac{Z_o}{Y\,\Delta z}} = \cancel{\frac{Z_o}{Y\,\Delta z}} + \frac{Z\,\Delta z}{Y\,\Delta z}$$

$$\Rightarrow Z_o(Z\,\Delta z + Z_o) = \frac{Z}{Y}$$

$$\Rightarrow Z_o Y(Z\,\Delta z + Z_o) = Z$$

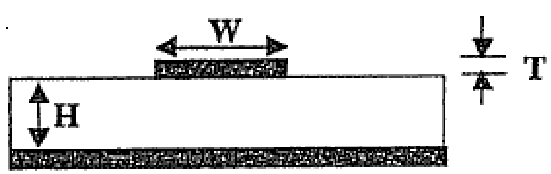
$$\Rightarrow \lim_{\Delta z \to 0}[Z] = Z_o^2 Y$$

# Transmission Line Parameters

- Derivation and Detailed Descriptions
  - Characteristic Impedance

$$Z_o = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

    - When the line is lossless, we have $Z_o = \sqrt{L/C}$
    - Only at very high frequencies, or with very lossy lines, do the *R* and *G* components of the impedance become significant.
  - Approximations for Typical TX lines
    - Microstrip line

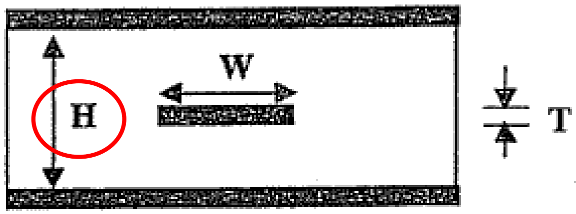



$$Zo \approx \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) \quad \text{Ohms}$$

(*Valid when* $0.1 < W/H < 2.0$ *and* $1 < \varepsilon_r < 15$)

# Transmission Line Parameters

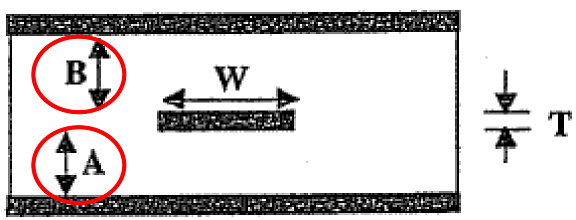
- Derivation and Detailed Descriptions
  - Approximations for Typical TX lines
    - Stripline




$$Zo_{sym} \approx \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4H}{0.67\pi(T+0.8W)}\right) \text{ Ohms}$$

(Valid when $W/H < 0.35$ and $T/H < 0.25$)

(b)




$$Zo_{offset} \approx 2\frac{Zo_{sym}(2A,W,T,\varepsilon_r)\cdot Zo_{sym}(2B,W,T,\varepsilon_r)}{Zo_{sym}(2A,W,T,\varepsilon_r)+Zo_{sym}(2B,W,T,\varepsilon_r)}$$

(c)

Average by using the equation in (b)

# Transmission Line Parameters

- Derivation and Detailed Descriptions
  - Propagation Velocity, Time, and Distance

$$v = \frac{c}{\sqrt{\varepsilon_r}}$$

$v$ = propagation velocity, in meters/second

$c$ = speed of light in a vacuum ($3 \times 10^8$ m/s)

$$\mathrm{PD} = \frac{1}{v} = \frac{\sqrt{\varepsilon_r}}{c}$$

$$\mathrm{TD} = \frac{x\sqrt{\varepsilon_r}}{c}$$

$\varepsilon_r$ = dielectric constant

PD = propagation delay, in seconds per meter

TD = time delay for a signal to propagate down a transmission line of length $x$

$x$ = length of the transmission line, in meters

- The time delay could also be expressed as $\mathrm{TD} = \sqrt{LC}$
- where $L$: total series inductance of length $x$
- and $C$: total shunt capacitance of length $x$

$$PD = \sqrt{L_{unit} C_{unit}}$$

# Transmission Line Parameters

- Derivation and Detailed Descriptions
  - Propagation Velocity, Time, and Distance
    - TD depends on the dielectric constant of the dielectric material, the line length, and the geometry of the transmission line cross section.
    - For the same FR4 board:
      - Stripline: the effective dielectric constant is larger → the speed of the signal is slower → TD is larger
      - Microstrip line: the effective dielectric constant is smaller → the speed of the signal is faster → TD is smaller
    - Formula for calculating the effective dielectric constant of a microstrip line:

$$F = \begin{cases} 0.02(\varepsilon_r - 1)\left(1 - \frac{W}{H}\right)^2 & \text{for } \frac{W}{H} < 1 \\ 0 & \text{for } \frac{W}{H} > 1 \end{cases}$$

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{12H}{W}\right)^{-1/2} + F - 0.217(\varepsilon_r - 1)\frac{T}{\sqrt{WH}}$$

# Transmission Line Parameters

- Derivation and Detailed Descriptions
  - Equivalent Circuit Models for SPICE Simulation
    - Since it is not practical to model a transmission line with an infinite number of elements, a sufficient number can be determined based on the minimum rise or fall time.
    - TD is no larger than one-tenth of the minimum system rise or fall time.
    - Rise times are typically measured between the 10 and 90% values of the maximum swing.

# Transmission Line Parameters

- Derivation and Detailed Descriptions
  - Equivalent Circuit Models for SPICE Simulation
    - How many segments should be chosen? $\text{segments} \geq 10\left(\frac{x}{T_r v}\right)$
    - The circuit parameters for a single segment must be

(x/v)/(Tr/10)

$$C_{\text{segment}} = \frac{(x)(C/\text{meter})}{\text{segments}}$$

$$L_{\text{segment}} = \frac{(x)L/\text{meter}}{\text{segments}}$$

$$R_{\text{segment}} = \frac{(x)R/\text{meter}}{\text{segments}}$$

$$G_{\text{segment}} = \frac{(x)G/\text{meter}}{\text{segments}}$$

$$\text{TD}_{\text{segment}} = \sqrt{L_{\text{segment}} C_{\text{segment}}} \leq \frac{T_r}{10}$$

# Transmission Line Parameters

- Derivation and Detailed Descriptions
  - Example 2.1 Creating a TX Line Model
    - $Z_0$=50Ω, line length $x$=5 in., $\tau_r$=2.5 ns, $\varepsilon_r$=4.5.
    - First, using the equations mentioned previously


$$Z_o \approx \frac{60}{\sqrt{\varepsilon_r}} \ln \frac{4H}{0.67\pi(T+0.8W)} = \frac{60}{\sqrt{\varepsilon_r}} \ln \frac{4(14.7)}{0.67\pi[0.7+0.8(5)]} = 50\ \Omega$$

$$\mathrm{TD} = \frac{x\sqrt{\varepsilon_r}}{c} = 5\ \mathrm{in.}(0.0254\ \mathrm{m/in.})\frac{\sqrt{4.5}}{3\times10^8\ \mathrm{m/s}} = 898\ \mathrm{ps}$$

$$v = \frac{c}{\sqrt{\varepsilon_r}} = \frac{3\times10^8\ \mathrm{m/s}}{\sqrt{4.5}} = 1.41\times10^8\ \mathrm{m/s}$$

- The total inductance and capacitance are

$$\mathrm{TD} = \sqrt{LC}$$

$$Z_o = \sqrt{L/C}$$

$$L_{\mathrm{total}} = (\mathrm{TD})(Z_o) = (898\times10^{-12})(50\ \Omega) = 44.9\ \mathrm{nH}$$

$$C_{\mathrm{total}} = \frac{\mathrm{TD}}{Z_o} = \frac{898\times10^{-12}\ \mathrm{s}}{50\ \Omega} = 17.9\ \mathrm{pF}$$

# Transmission Line Parameters

- Derivation and Detailed Descriptions
  - Example 2.1 Creating a TX Line Model
    - The segments needed are

$$\text{segments} \geq 10\left(\frac{X}{T_r v}\right) = 10\left[\frac{5\ \text{in.}(0.0254\ \text{m/in.})}{2.5\ \text{ns}(1.41\times 10^8\ \text{m/s})}\right] = 3.6$$

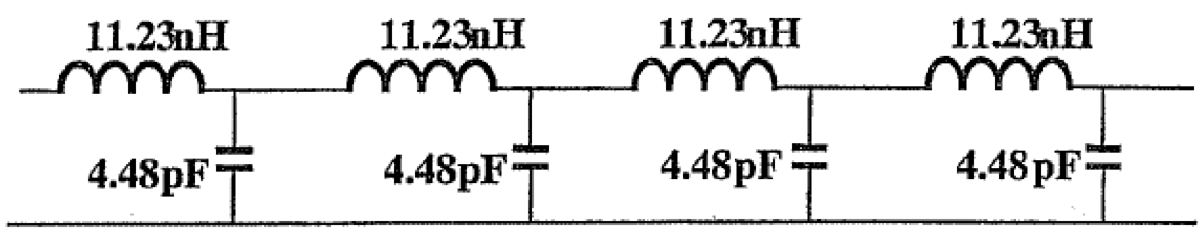
    - The capacitance and inductance for a single segment are

$$C_{\text{segment}} = \frac{C_{\text{total}}}{\text{segments}} = \frac{17.9\ \text{pF}}{4} = 4.48\ \text{pF}$$

$$L_{\text{segment}} = \frac{L_{\text{total}}}{\text{segments}} = \frac{44.9\ \text{nH}}{4} = 11.23\ \text{nH}$$

    - For checking

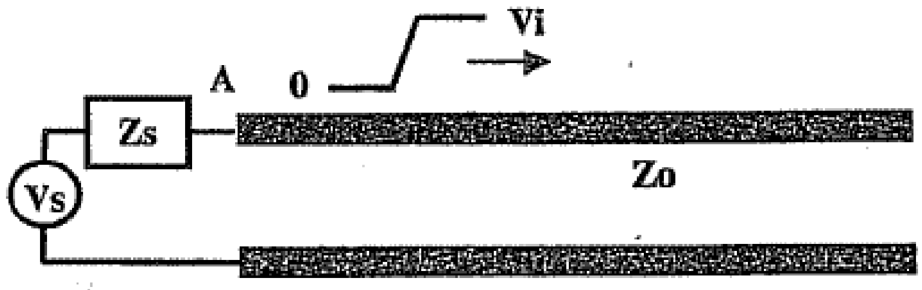
$$\text{TD}_{\text{segment}} = \sqrt{L_{\text{segment}}C_{\text{segment}}} = \sqrt{(4.48\ \text{pF})(11.23\ \text{nH})} = 0.224\ \text{ns} \leq \frac{T_r}{10}$$



# Launching Initial Wave and TX line Reflections

- Initial Wave
  - Launching a Wave onto a Long TX Line
    - The magnitude of $V_i$ is determined by the voltage divider between the source and the line impedance:

$$V_i = V_s \frac{Z_o}{Z_o + Z_s}$$




    - When $Z_L = Z_0$, the voltage $V_i$ is the dc steady-state value.

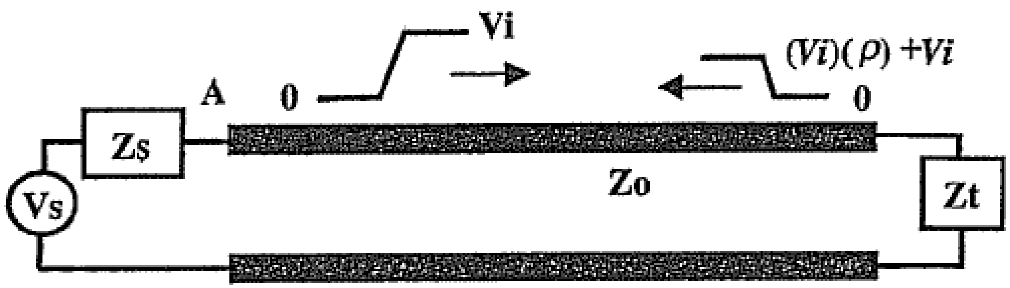
How long does it take? A time delay: TD

# Launching Initial Wave and TX line Reflections

- Initial Wave
  - Incident Signal Being Reflected from an Unmatched Load
    - ***Junction***: impedance discontinuity on a TX line
    - The reflection coefficient is calculated as:

$$\rho = \frac{V_{\text{reflected}}}{V_{\text{incident}}} = \frac{Z_t - Z_o}{Z_t + Z_o}$$

    - This reflection and counter-reflection continues until the line has reached a stable condition.




$$Vi = Vs\frac{Zo}{Zo + Zs}$$

$$\rho = \frac{Zt - Zo}{Zt - Zo}$$

# Launching Initial Wave and TX line Reflections

- Initial Wave
  - Matched, Shorted and Open Loads


$$\rho = \frac{Zo - Zo}{Zo + Zo} = 0$$

(a)


$$\rho = \frac{0 - Zo}{0 + Zo} = -1$$

(b)

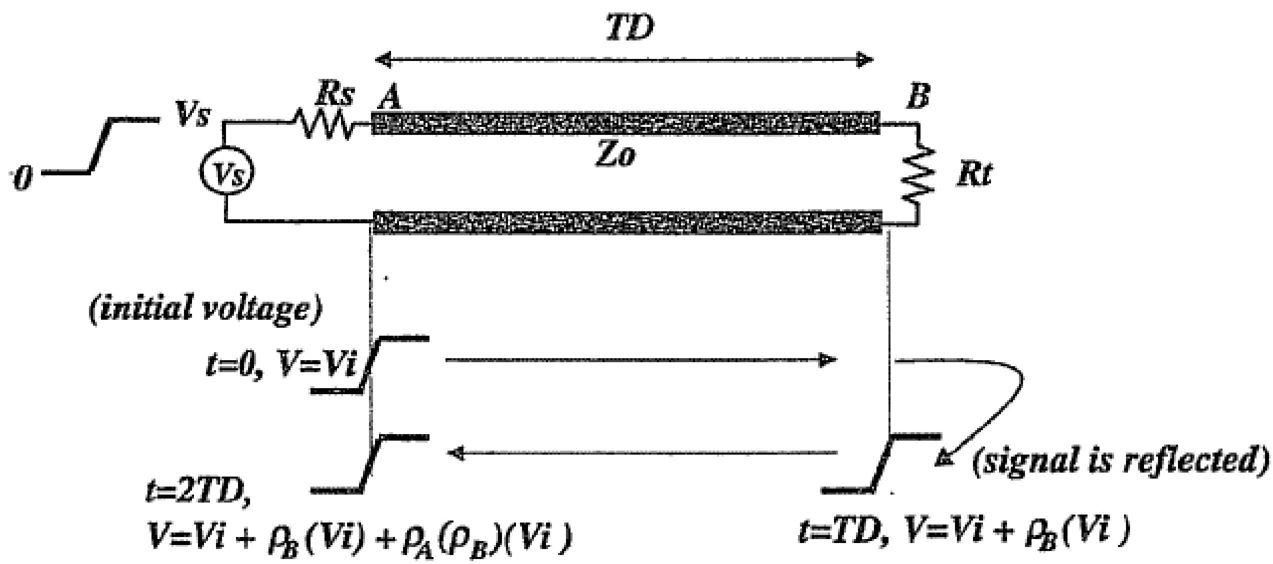

$$\rho = \frac{\infty - Zo}{\infty + Zo} = 1$$

(c)

# Launching Initial Wave and TX line Reflections

- Multiple Reflections
  - Descriptions

$V_i = V_s Z_o / (Z_o + R_s)$

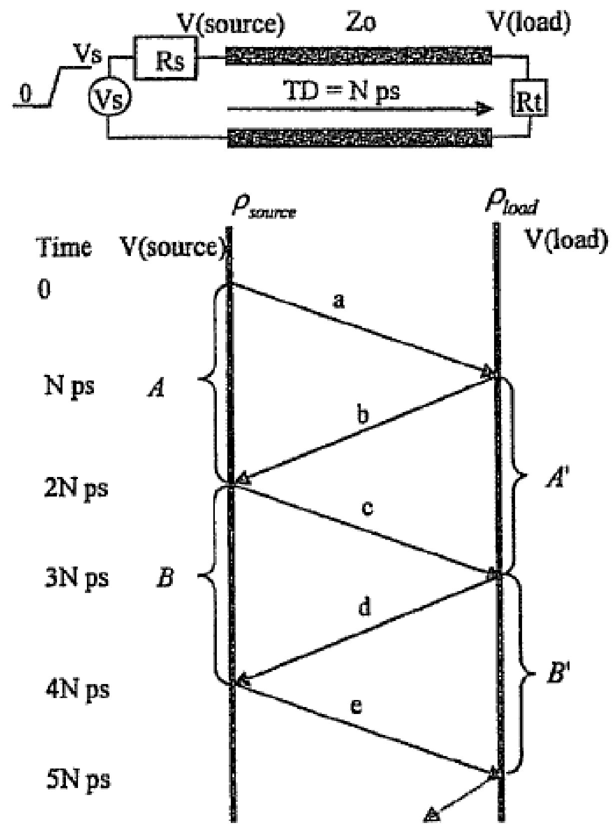



- The reflections could take a long time to settle out if the termination is not matched and can have some significant timing impacts.

# Launching Initial Wave and TX line Reflections

- Multiple Reflections
  - Lattice Diagrams
    - A bounce diagram
    - Diagonal lines: waves
    - Increasing time: ↓
    - Time increment: TD
    - The steady state *V*:

$$V_s \frac{R_t}{R_t + R_s}$$




$a = V_{initial}$

$b = a\ \rho_{load}$

$c = b\ \rho_{source}$

$d = c\ \rho_{load}$

$e = d\ \rho_{source}$

$f = e\ \rho_{load}$

$A = a$

$B = a + b + c$

$C = a + b + c + d + e$

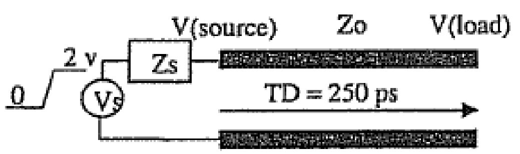
$A' = a + b$

$B' = a + b + c + d$

$C' = a + b + c + d + e + f$

# Launching Initial Wave and TX line Reflections

- Lattice Diagrams and Over- and Underdriven TX Lines
  - Example 2.2 Underdriven TX Line ($Z_0<Z_S$)

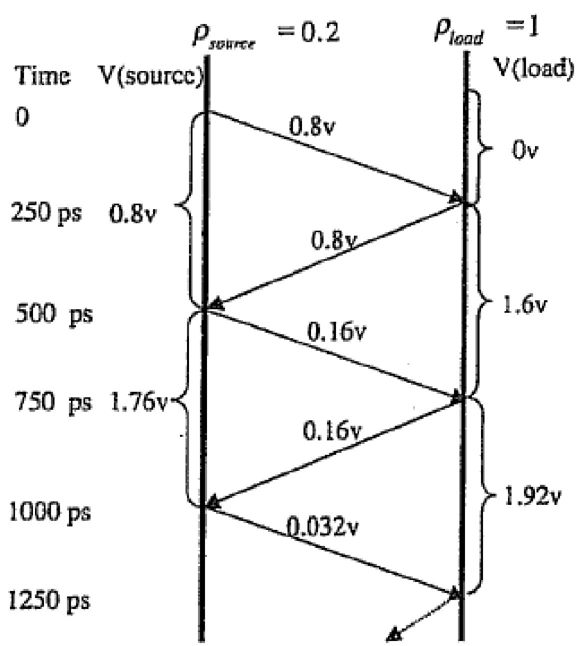


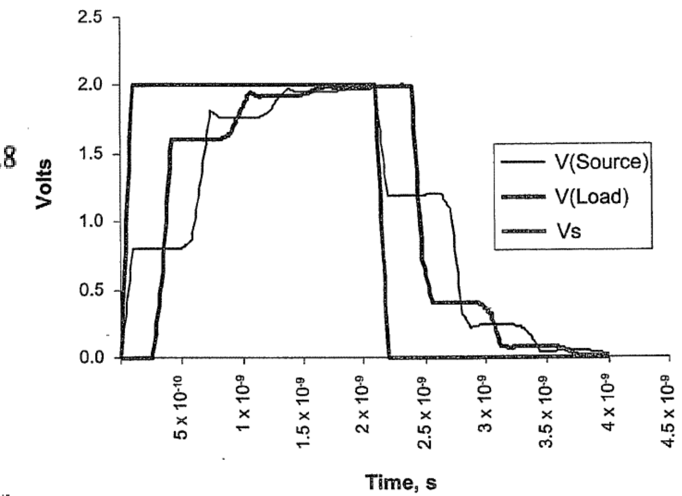

Assume Zs=75 ohms
Zo=50 ohms
Vs=0-2 volts

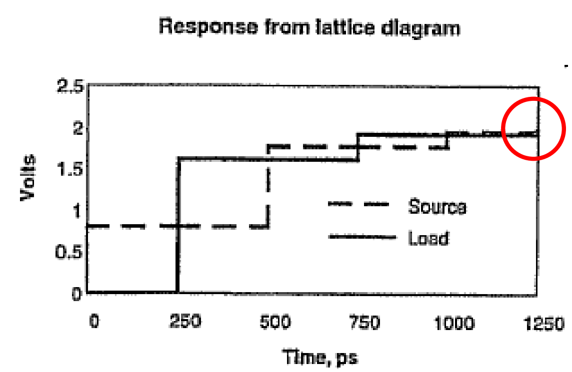
$$V_{initial}=Vs\frac{Zo}{Zs+Zo}=(2)\left(\frac{50}{75+50}\right)=0.8$$

$$\rho_{source}=\frac{Zs-Zo}{Zs+Zo}=\frac{75-50}{75+50}=0.2$$

$$\rho_{load}=\frac{Zl-Zo}{Zl+Zo}=\frac{\infty-50}{\infty+50}=1$$

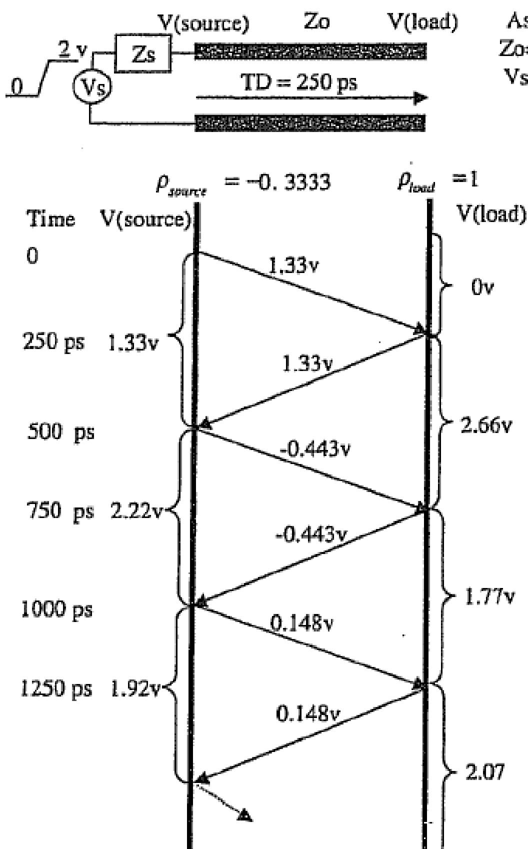


# Launching Initial Wave and TX line Reflections

- Lattice Diagrams and Over- and Underdriven TX Lines
  - Example 2.2 Overdriven TX Line ($Z_0 > Z_S$)

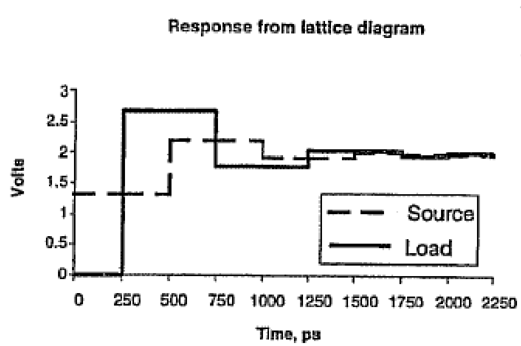


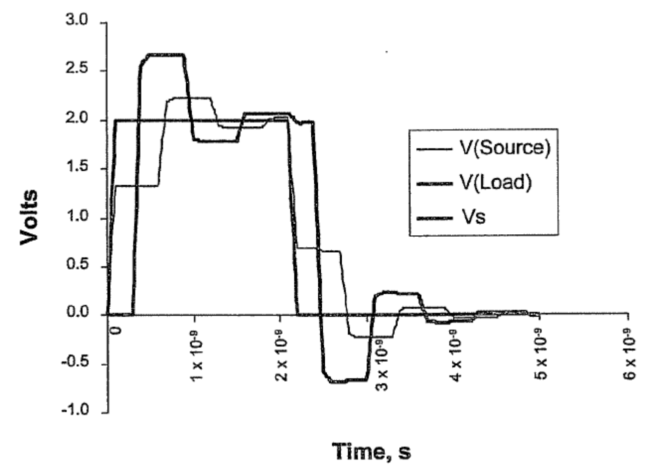

Assume Zs=25 ohms
Zo=50 ohms
Vs=0-2 volts

$$V_{initial} = V_S \frac{Zo}{Zs+Zo} = (2)\left(\frac{50}{25+50}\right) = 1.3333$$

$$\rho_{source} = \frac{Zs-Zo}{Zs+Zo} = \frac{25-50}{25+50} = -0.33333$$

$$\rho_{load} = \frac{Zl-Zo}{Zl+Zo} = \frac{\infty-50}{\infty+50} = 1$$

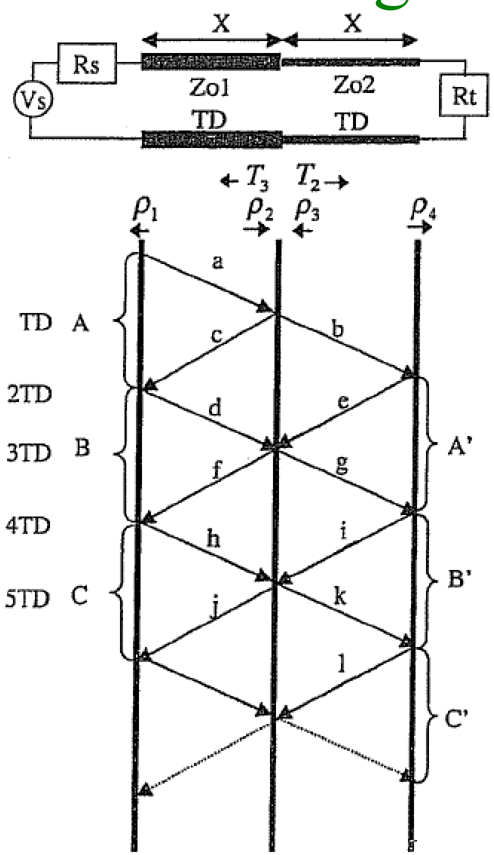



Ringing effect

# Launching Initial Wave and TX line Reflections

- Lattice Diagrams and Over- and Underdriven TX Lines
  - Two Segments of TX Lines




$A = a$    $A' = b + e$

$B = a + c + d$    $B' = b + e + g + i$

$C = A + c + d + f + h$    $C' = b + e + g + i + k + l$

$$v_i = V_s \frac{Z_{o1}}{Rs + Z_{o1}} \qquad a = v_i$$

$$b = aT_2$$

$$\rho_1 = \frac{Rs - Z_{o1}}{Rs + Z_{o1}} \qquad c = a\rho_2$$

$$d = c\rho_1$$

$$\rho_2 = \frac{Z_{o2} - Z_{o1}}{Z_{o2} + Z_{o1}} \qquad e = b\rho_4$$

$$f = d\rho_2 + eT_3$$

$$\rho_3 = \frac{Z_{o1} - Z_{o2}}{Z_{o1} + Z_{o2}} \qquad g = e\rho_3 + dT_2$$

$$h = f\rho_1$$

$$\rho_4 = \frac{Rt - Z_{o2}}{Rt + Z_{o2}} \qquad i = g\rho_4$$

$$T_2 = 1 + \rho_2 \qquad j = h\rho_2 + iT_3$$

$$T_3 = 1 + \rho_3 \qquad k = i\rho_3 + hT_2$$

At the junction of $Z_{01}/Z_{02}$, part of the signal will be reflected ($\rho$) and part of the signal will be transmitted ($T$=1+$\rho$)

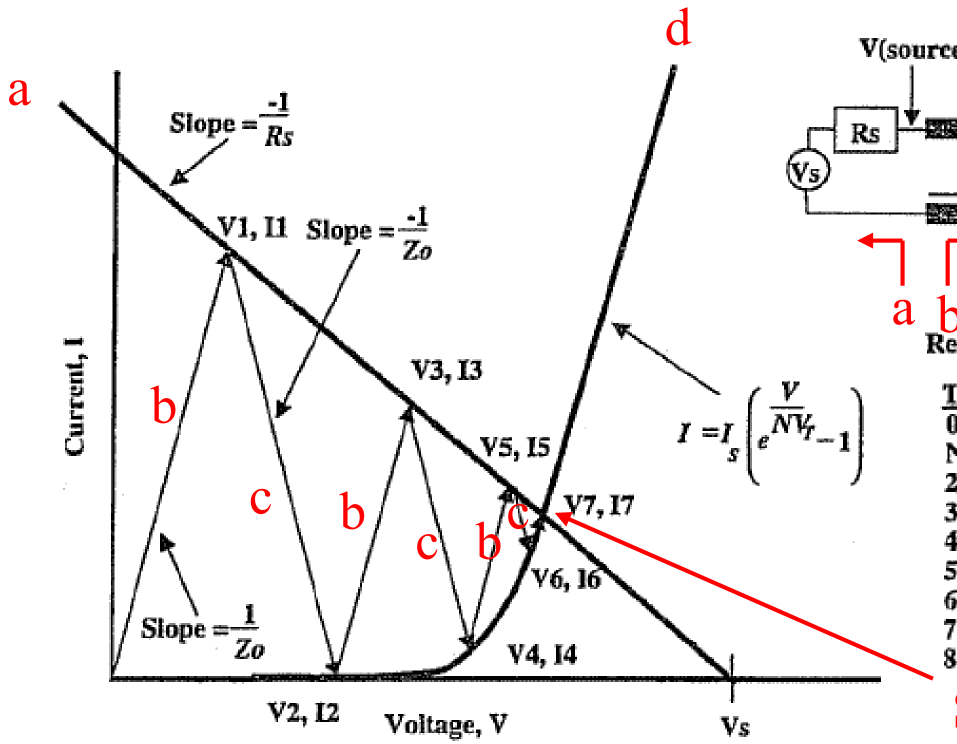
How about the signal at the junction $Z_{01}/Z_{02}$?

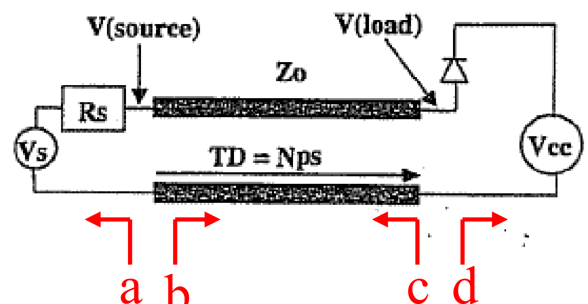
# Launching Initial Wave and TX line Reflections

- Bergeron Diagrams and Reflections from Nonlinear Loads
  - Bergeron Diagrams
    - When nonlinear loads and sources exist.

Solve for the intersections of the source (a, b)
Solve for the intersections of the load (c, d)

V1=?



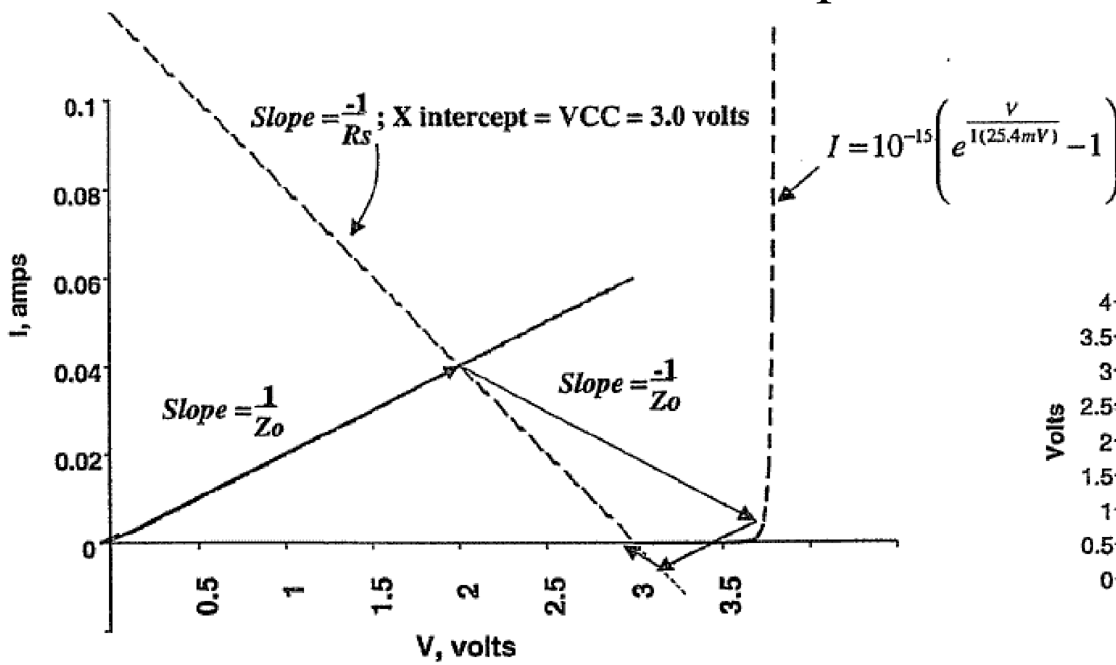



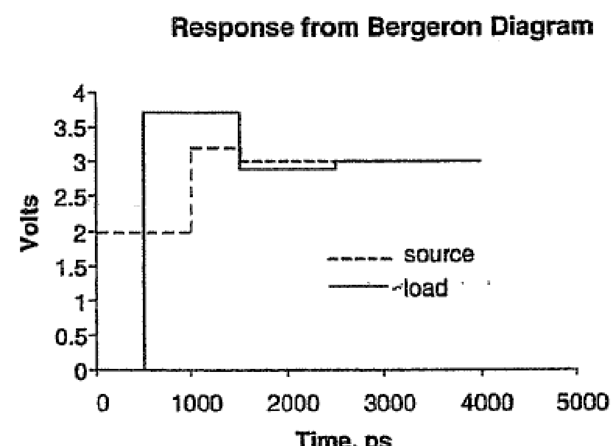

Response from Bergeron Diagram

| Time | V(source) | V(load) |
|---|---|---|
| 0 | V1 | 0 |
| N | V1 | V2 |
| 2N | V3 | V2 |
| 3N | V3 | V4 |
| 4N | V5 | V4 |
| 5N | V5 | V6 |
| 6N | V7 | V6 |
| 7N | V7 | V7 |
| 8N | V7 | V7 |

# Launching Initial Wave and TX line Reflections

- Bergeron Diagrams and Reflections from Nonlinear Loads
  - Example of Bergeron Diagrams
    - $V_S$=3V, TD = 500ps, $Z_0$=50Ω, $R_S$=25Ω, and the diode behaves with the equation shown.

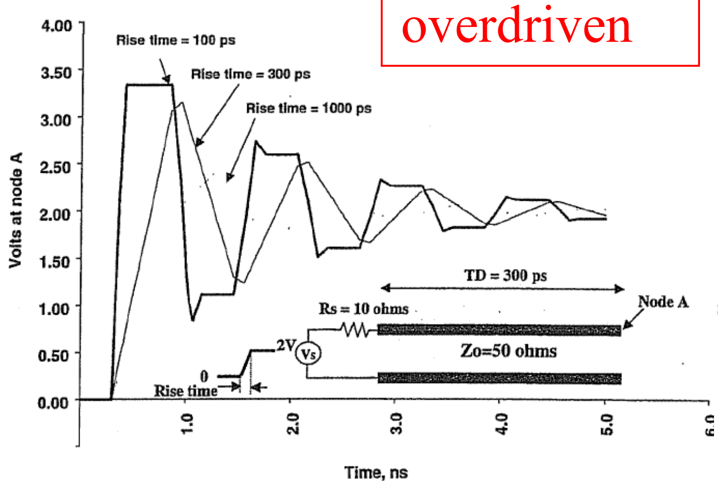


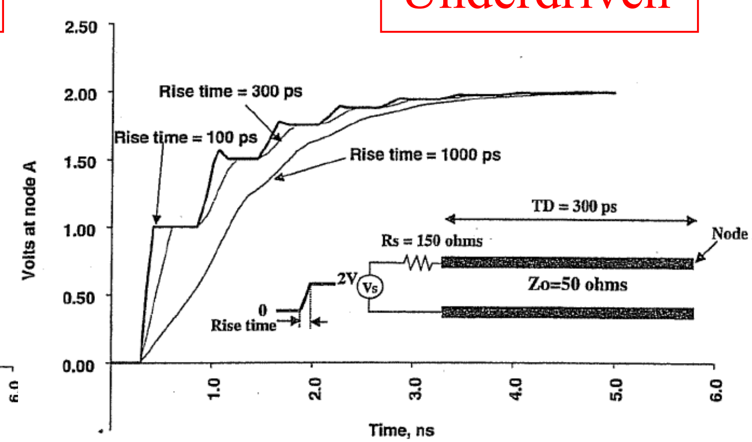
# Launching Initial Wave and TX line Reflections

- Effect of Rise Time on Reflections
  - Criterion
    - The rise time will begin to have a significant effect on the waveform when : $\tau_r < 2TD$.
    - When $\tau_r > 2TD$, reflection from the source will occur at a time in the transition region, which will not affect the steady state value.

overdriven




Underdriven



# Launching Initial Wave and TX line Reflections

- Reflections from Reactive Loads
  - Reflections from Capacitive Loads-No Loss
    - The capacitor will initially look like a short circuit when the signal reaches the capacitor and will look like an open circuit after the capacitor is fully charged.

What is the effect of $t_r$ on the waveform?

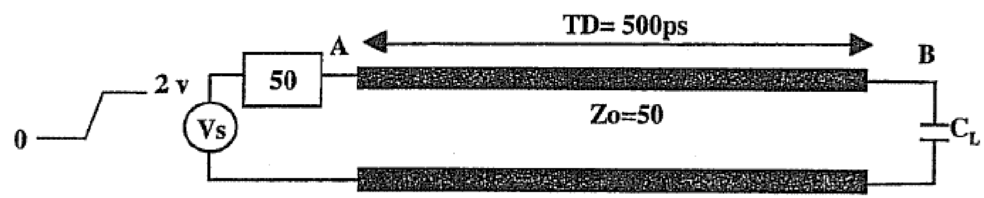
The signal data rate is slow down by adding $C_L$.

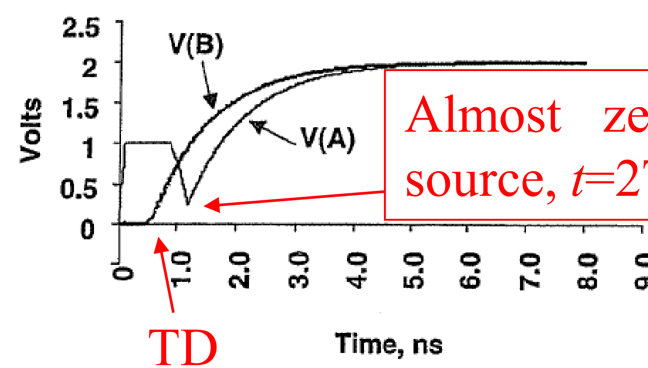
The voltage at the capacitor is

$$V_{\text{capacitor}} = 2V_i(1 - e^{-(t-\text{TD})/\tau}), \qquad t > \text{TD}$$

$$\tau = CZ_o$$

$$v(t) = V_{\text{oc}} + (v(0) - V_{\text{oc}})e^{-t/(R_t C)}$$




Almost zero at the source, $t$=2TD

# Launching Initial Wave and TX line Reflections

- Reflections from Reactive Loads
  - Reflections from Capacitive Loads-Lossy
    - If the line is terminated with a parallel resistor and capacitor, the voltage at the capacitor will be

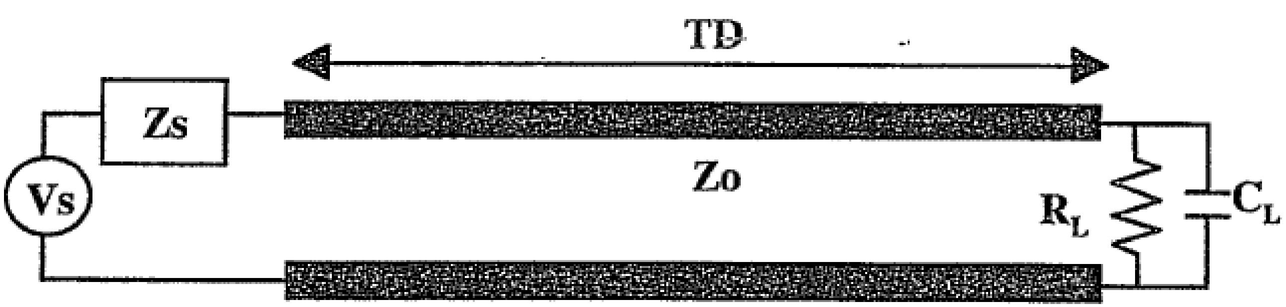
$$V_{\text{capacitor}} = 2V_i \frac{R_L}{R_L + Z_o}\left(1 - e^{-(t-\mathrm{TD})/\tau_1}\right), \qquad t > \mathrm{TD}$$

With $Z_S = Z_0$

$$\tau_1 = \frac{C_L Z_o R_L}{R_L + Z_o}$$

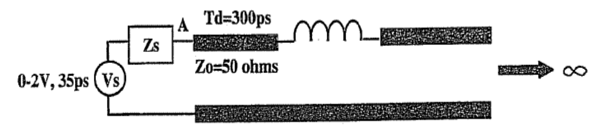
The time constant depends on $C_L$ and the parallel combination of $R_L$ and $Z_0$.

By adding $R_L$, $\tau_1$ could be made smaller.

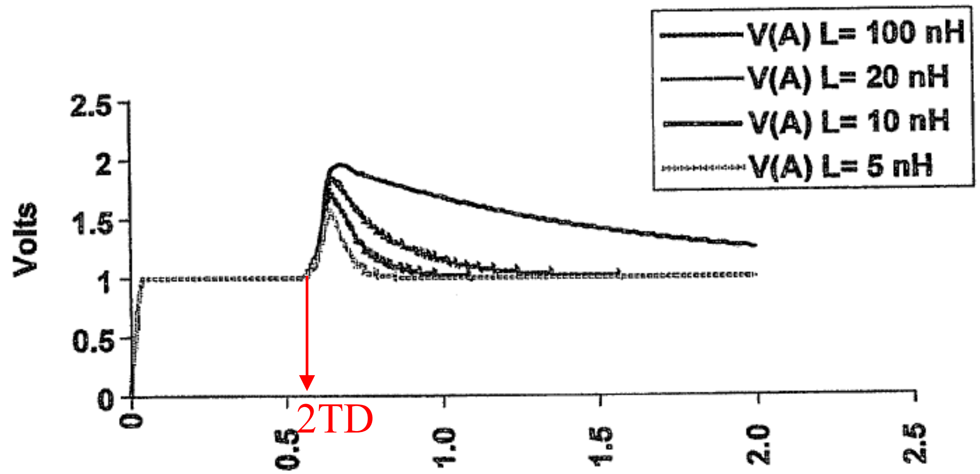


# Launching Initial Wave and TX line Reflections

- Reflections from Reactive Loads
  - Reflections from Inductive Loads




    - Initially, at time = 0, the inductor will resemble on open circuit. This produces a reflection coefficient of 1.
    - Eventually, the inductor will discharge its energy at a rate that depends on the time constant $\tau$ of $L/Z_0$.



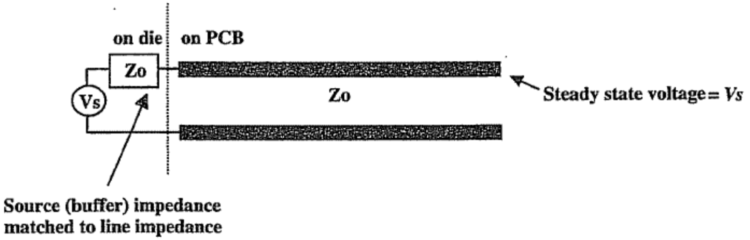

What if the series $L$ was replaced with an parallel $C$?

# Launching Initial Wave and TX line Reflections

- Termination Schemes to Eliminate Reflections
  - Two Impractical and One Practical Methods
    - Method 1: to decrease the frequency of the system so that the reflections on the TX line reach steady state before another signal is driven onto the line
    - Method 2: to shorten the PCB traces so that the reflections will reach steady state in a shorter time.
    - **Method 3**: to terminate the TX line with an impedance equal to the characteristic impedance of the line.
      - Source termination
      - Load (Parallel) termination

# Launching Initial Wave and TX line Reflections

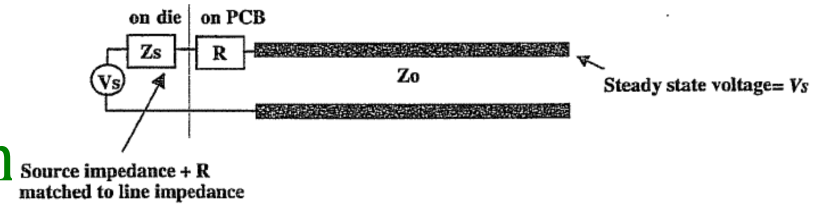
- Termination Schemes to Eliminate Reflections
  - On-Die Source Termination




    - This method requires that the *I-V* curve of the output buffer be very linear and yield an *I-V* curve with an impedance very close to the TX line impedance.
    - *Advantages*: this does not require any additional components that increase cost and consume area on the board.
    - *Disadvantages*: since there are numerous variables, it is difficult to achieve a good match. Some of them are silicon fabrication process variations, voltage, temperature, power delivery factors, and simultaneous switching noise.

# Launching Initial Wave and TX line Reflections

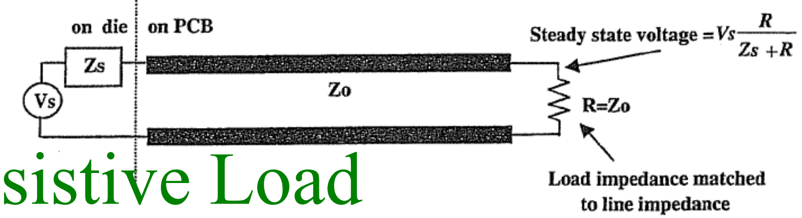
- Termination Schemes to Eliminate Reflections
  - Series Source Termination




    - This method requires that a resistor be added in series with the output buffer to match the characteristic impedance of the TX line.
    - Designing the *I-V* curve of the output buffer to yield a very low impedance so that the matching mechanism is dominated by the series resistor.
    - *Advantage*: the total variation in impedance is small.
    - *Disadvantage*: the resistors add cost to the board, and it consumes significant board area.

# Launching Initial Wave and TX line Reflections

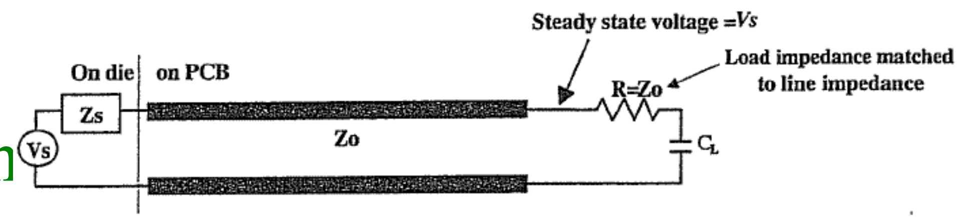
- Termination Schemes to Eliminate Reflections




  - Load Termination with Resistive Load
    - Load termination with a resistive load eliminates the unknown variables associated with the buffer impedance because a precision resistor can be used.
    - *Advantage*: low-impedance output buffers may be used.
    - *Disadvantage*: a large portion of the dc current will be shunted to ground, which exacerbates power delivery and thermal problems. As power consumption increases, cost also increases.

# Launching Initial Wave and TX line Reflections

- Termination Schemes to Eliminate Reflections
  - AC Load Termination



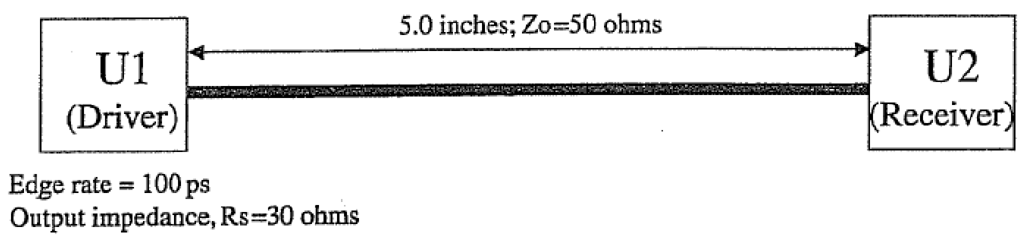

- AC load termination uses a series capacitor and resistor at the load end. $R=Z_0$, $RC_L=1\sim2\tau_r$.
- *Advantage*: the power is only dissipated during the transition region. Thus, no dc power dissipation.
- *Disadvantage*: the capacitive loading will increase the signal delay by slowing down the rising or falling times at the load. Furthermore, additional resistors and capacitors consume board area and increase cost.

# Launching Initial Wave and TX line Reflections

- Termination Schemes to Eliminate Reflections
  - Common Termination Problems
    - *Fabrication Variation*: the characteristic impedance of the trace tends to vary significantly, due to PCB production variations. This tends to have a bigger impact on source termination.
    - *Crosstalk*: will introduce additional variations in the impedance.
    - Different line lengths:
      - For short lines, source termination is desirable. Since DC levels are prolonged, we don't want to consume them.
      - For long lines, load termination is preferable. Since we don't want the wave to be reflected toward the source.

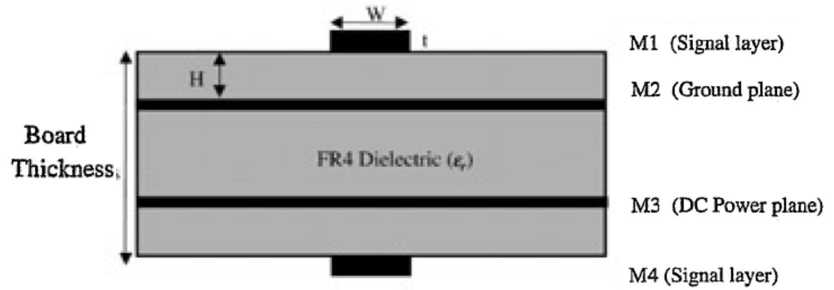
# Additional Examples

- Design of a Trace
  - Problem
    - The driving buffers on component U1 have an impedance of 30 Ω, an edge rate of 100 ps, and a swing of 0 to 2 V.
    - The traces on the PCB are required to be 50 Ω and 5 in. long.
    - The relative dielectric constant of the board ($\varepsilon_r$) is 4.0, the transmission line is assumed to be a perfect conductor, and the receiver capacitance is small enough to be ignored.

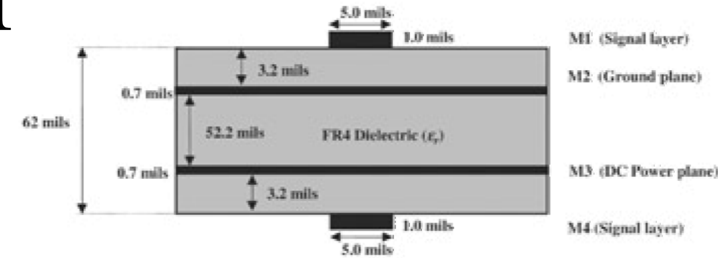


# Additional Examples

- Design of a Trace
  - Goals
    - 1. Determine the correct cross-sectional geometry of the PCB trace in microstrip form that will yield an impedance of 50 Ω.
    - 2. Calculate the time it takes for the signal to travel from the driver, U1, to the receiver, U2.
    - 3. Determine the wave shape seen at U2 when the system is driven by U1.
    - 4. Create an equivalent circuit of the system.



# Additional Examples




- Design of a Trace
  - Calculating the Cross-Sectional Geometry of the PCB
    - For the purpose of transmission line design, a dc power plane will act like an ac ground.
    - The trace impedance in microstrip form is

$$Z_{o_{\text{microstrip}}} = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \frac{5.98H}{0.8W + t}$$

    - Since the standard $t$=1.0mil and $W$=5mil, thus we have

$$50 = \frac{87}{\sqrt{4.0 + 1.41}} \ln \frac{5.98H}{0.8(5.0) + 1.0} \longrightarrow H = 3.2 \text{ mils}$$

    - Since the internal metal layers are only 0.7 mil thick and a typical PCB board thickness requested by industry is 62 mils thick, 52.2 mil is determined.

# Additional Examples

- Design of a Trace
  - Calculating the Propagation Delay
    - The effective dielectric constant is

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{12H}{W}\right)^{-1/2} + F - 0.217(\varepsilon_r - 1)\frac{t}{\sqrt{WH}}$$

    - Since $W/H = 5/3.2 > 1.0$, then $F = 0$. Therefore,

$$\varepsilon_e = \frac{4.0 + 1}{2} + \frac{4.0 - 1}{2}\left[1 + \frac{12(3.2)}{5.0}\right]^{-1/2} + 0 - 0.217(4.0 - 1)\frac{1.0}{\sqrt{5.0(3.2)}}$$

$$= 2.84$$

    - The propagation velocity is

$$v = \frac{c}{\sqrt{\varepsilon_r}} = \frac{3.0 \times 10^8 \text{ m/s}}{\sqrt{2.84}} = 1.78 \times 10^8 \text{ m/s}$$

    - The time delay is

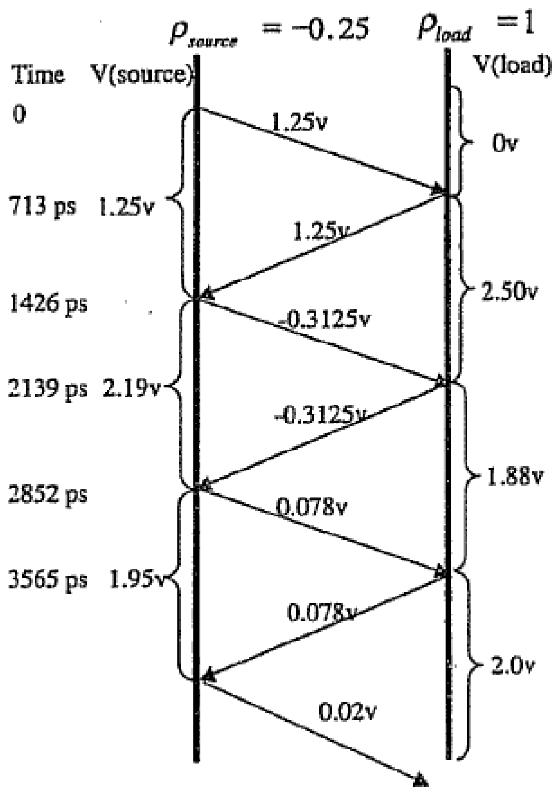
$$\text{TD} = \frac{\text{length}\sqrt{\varepsilon_r}}{c} = \frac{5.0 \text{ in.}}{1.78 \text{ m/s}}\left(\frac{0.0254 \text{ m}}{1.0 \text{ in.}}\right) = 713 \text{ ps}$$

# Additional Examples

- Design of a Trace
  - Determining the Wave Shape Seen at the Receiver

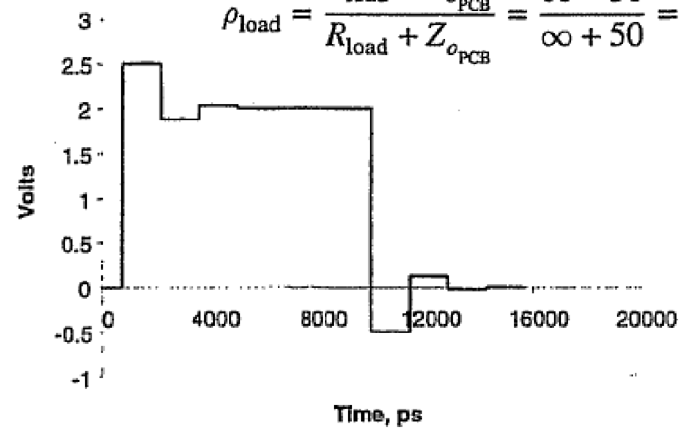
$$V_{\text{initial}} = V_{\text{in}} \frac{Z_{o_{\text{PCB}}}}{Z_{o_{\text{PCB}}} + R_s} = 2.0\left(\frac{50}{50+30}\right) = 1.25\ \text{V}$$

- Assuming $R_{Load}=\infty$ and using the lattice diagram,




$$\rho_{\text{source}} = \frac{R_s - Z_{o_{\text{PCB}}}}{R_s + Z_{o_{\text{PCB}}}} = \frac{30-50}{30+50} = -0.25$$

$$\rho_{\text{load}} = \frac{R_{\text{load}} - Z_{o_{\text{PCB}}}}{R_{\text{load}} + Z_{o_{\text{PCB}}}} = \frac{\infty-50}{\infty+50} = 1.0$$



# Additional Examples

- Design of a Trace
  - Creating an Equivalent Circuit
    - The minimum of 72 segments is required.

$$\text{velocity (in./ps)} = \frac{5.0\text{ in.}}{713\text{ ps}} = 0.0070\text{ in./ps}$$

$$\text{segments} \geq 10\left(\frac{\text{length}}{T_r v}\right) = 10\left[\frac{5\text{ in.}}{(100\text{ ps})(0.0070\text{ in./ps})}\right] = 71.4$$

    - Since $Z_o = \sqrt{L/C}$ and $\text{TD} = \sqrt{LC}$ , we have

$$C = \frac{\text{TD}}{Z_o} = \frac{\sqrt{LC}}{\sqrt{L/C}} = \frac{142.6\text{ ps}}{50} = 2.85\text{ pF}$$

TD per inch

$$L = (\text{TD})(Z_o) = \sqrt{LC}\sqrt{\frac{L}{C}} = 7.130\text{ nH}$$

    - The inductance and capacitance per segment are

$$C_{\text{segment}} = \frac{(\text{length})(C/\text{in.})}{\text{segment}} = \frac{5.0\text{ in.}(2.85\text{ pF/in.})}{72} = 0.198\text{ pF/segment}$$

$$L_{\text{segment}} = \frac{(\text{length})(L/\text{in.})}{\textit{segment}} = \frac{5.0\text{ in.}(7.13\text{ nH/in.})}{72} = 0.495\text{ nH/segment}$$

# Additional Examples

- Design of a Trace
  - Creating an Equivalent Circuit
    - Check the calculations with

$$\text{delay/segment} = \frac{713 \text{ ps}}{72} = 9.9 \text{ ps} \approx \sqrt{(0.198 \text{ pF})(0.495 \text{ nH})} = 9.9 \text{ ps}$$

$$\text{impedance/segment} = \sqrt{\frac{0.495 \text{ nH}}{0.198 \text{ pF}}} = 50\ \Omega$$

    - The equivalent circuit is shown below with the open circuit at the end of the line approximated with a very large resistor.