Project 7

Design of an amplifier with an absolutely stable FET and matching circuits based on microstrip TL sections

This project focuses on the design of a narrow-band amplifier consisting of an FET and matching circuits from microstrip lines.

Design an amplifier based on a microwave FET. Find its type, operating frequency and bias point in the appended table.

As a design protocol note, please include:

- choice of a FET and design frequency f_0,
- stability coefficient k ,
- calculate GM1 and GM2 values,
- choose a commercially available substrate,
- schematic of matching circuits,
- analysis of the resulting amplifier in the f_0 ± 20% frequency band, *i.e.*, plot the absolute values of parameters S_{11}, S_{21}, S_{12} and S_{22},
- layout of the whole amplifier.

List of transistors:

Task No.	FET s-par. file	Design frequency f_0 (GHz)	Bias Point
1	ATF58143	8	4 V, 30 mA
2	ATF58143	6.5	3 V, 60 mA
3	ATF35143	9.5	3 V, 30 mA
4	ATF35143	8.5	4 V, 60 mA
5	ATF34143	12	3 V, 40 mA
6	ATF34143	9.5	3 V, 20 mA
7	ATF33143	6	3 V, 40 mA
8	ATF33143	8.8	3 V, 40 mA
9	ATF36163	13	2 V, 20 mA
10	ATF36163	14	2 V, 10 mA

Project solution procedure

As a demonstration task, the following amplifier has been designed:

- We utilized the ATF-34143 (Agilent) transistor with a 2 V, 20 mA biasing point. The data file can be found in the following AWR library: Libraries − AWR Web Site – Parts by Vendor – Avago – Data − FET – ATF34143 − MDIF. This folder contains an *.mdf file which aggregates sets of Touchstone files for all available bias points.
- Create a new schematic called Transistor, load your transistor and connect both ports.
- Create a new rectangular graph called Stability and add the measurement of stability factor *k*. The data source is directly from the S-parameters file.
- Perform an analysis.
- Check if $k > 1$ at your design frequency. If not, contact a teacher. The stability of the ATF-34143 transistor is shown in Fig. 1.

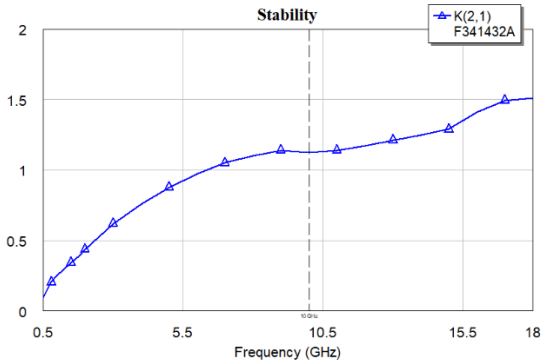

Fig. 1 Stability factor of the ATF-34143 transistor.

When your FET is absolutely stable, it is possible to calculate the GM1 and GM2 optimum reflection coefficients of the generator and load:

- Set the project to have a single frequency of 10 GHz in this example.
- Calculate GM1 and GM2 at the design frequency (set source as the Transistor schematic).
- Create a new tabular graph called GM.
- Add the measurements: mag(GM1), angle(GM1), mag(GM2) and angle(GM2). The result is shown in Fig. 2.

Frequency (GHz)	|GM1(1,1)| Transistor	Ang(GM1(1,1)) (Deg) Transistor	|GM2(1,1)| Transistor	Ang(GM2(1,1)) (Deg) Transistor
10	0.82699	-35.942	0.4975	-84.943

Fig. 2 Reflections GM1 and GM2 of the ATF-34143 transistor at 10 GHz.

- Verify GM1 and GM2 values using the AWR model based on 2 LTUNERs as shown in Fig. 3.

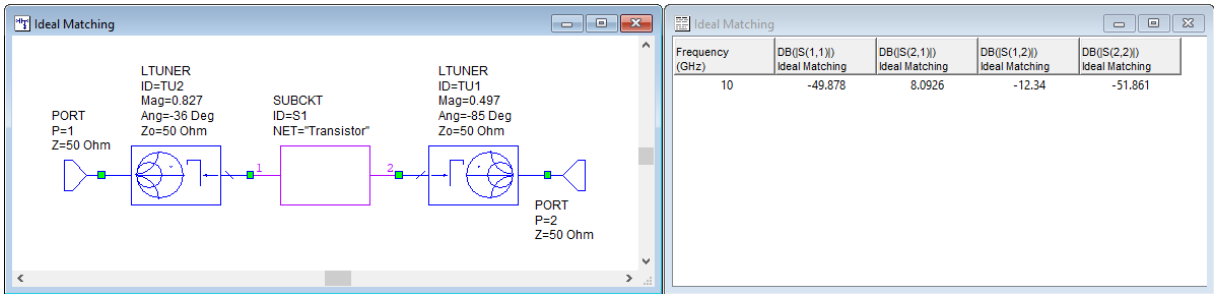

Fig. 3 Schematic of the ideally matched transistor using two LTUNER elements and resulting S-parameters.

It is now possible to design both the input and output matching circuits. Both should employ sections of microstrip transmission lines including discontinuities:

- Set the substrate parameters into GLOBAL DEFINITIONS: Rogers RT/Duroid: $\varepsilon_r = 2.2$, $\tan\delta = 0.001$, $H = 0.508$ mm, $T = 50$ µm, Rho = 0.7.
- Using TXLINE, calculate 50 Ω width W and its corresponding λ_g line wavelength.
- For the demo task at 10 GHz: $W = 1.51$ mm, $\lambda_g = 21.87$ mm. All line sections MUST be shorter than $\lambda_g/2$ which means < 11 mm.
- Create a new schematic Input Match, place the LTUNER in it and set its value to GM1*. Connect the two ports as shown in Fig. 4.
- Create a new Smith Chart graph and show S_{11}. Change the curves in the Smith Chart to admittances (right click on graph – Options... – Grid – Admittance grid).

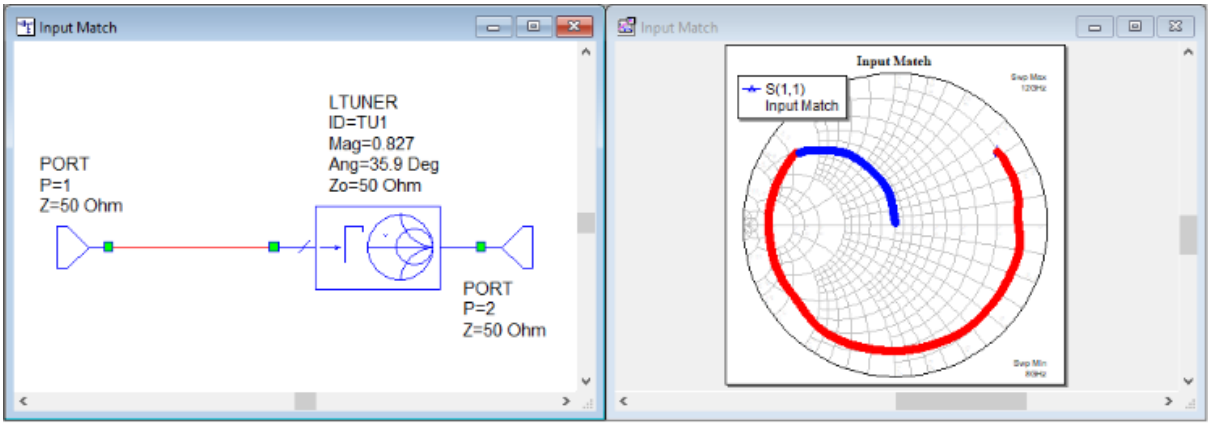

Fig. 4 Schematic with LTUNER with GM1 reflection and Smith Chart with intended matching.*

- Add section MLIN with a 50 Ω impedance between the LTUNER and Port 1 and set its length to 0.
- Using TUNE TOOL set TL1's length to transform S_{11} to the g = 1 circle (red curve in the admittance Smith Chart in Fig. 4).
- Add element MLEF to Port 1 and set its length using TUNE TOOL to transform S_{11} to the Smith Chart's center (blue curve in Fig. 4). The final matching circuit is shown in Fig. 5.

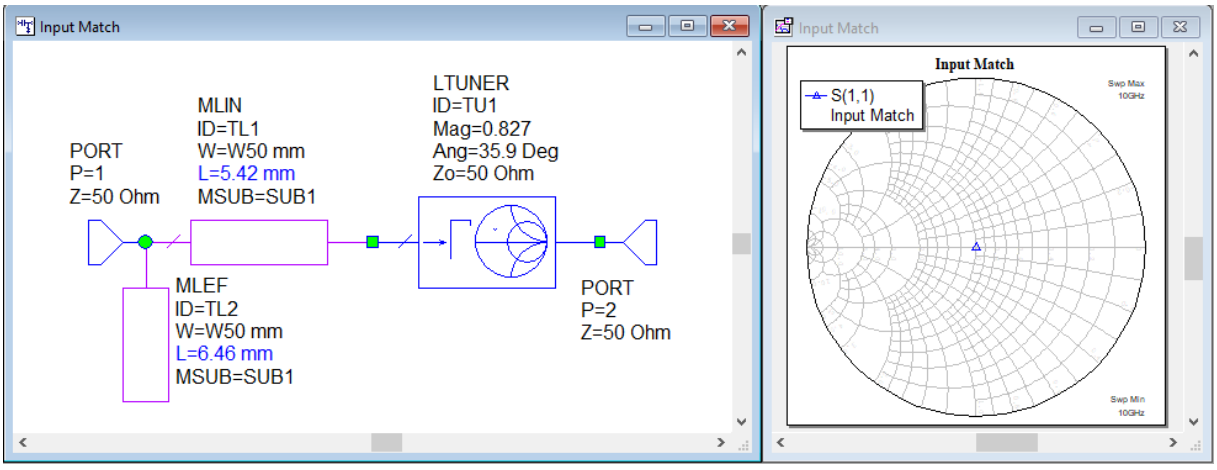

Fig. 5 Input matching circuit and resulting reflection coefficient.

- To complete the design, add the influence of discontinuities. Between TL1 and TL2 insert the MTEE discontinuity. Using TUNE TOOL, adjust TL1's and TL2's lengths as shown in Fig. 6. Usually, approx. a 10% reduction of TL1 and a very short lengthening of TL3 is necessary.
- The resulting S_{11} must, again, fall in the Smith Chart's center.

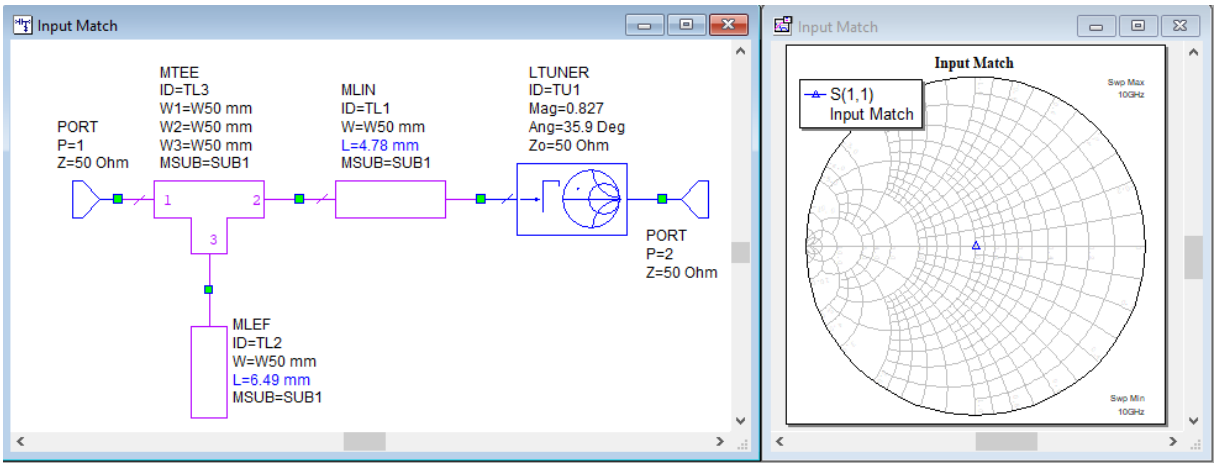

Fig. 6 Input matching circuit with discontinuity and resulting reflection coefficient.

- Afterwards, move the LTUNER away from the schematic.
- The output matching circuit can be designed in a similar way. The resulting structure can be seen in Fig. 7.

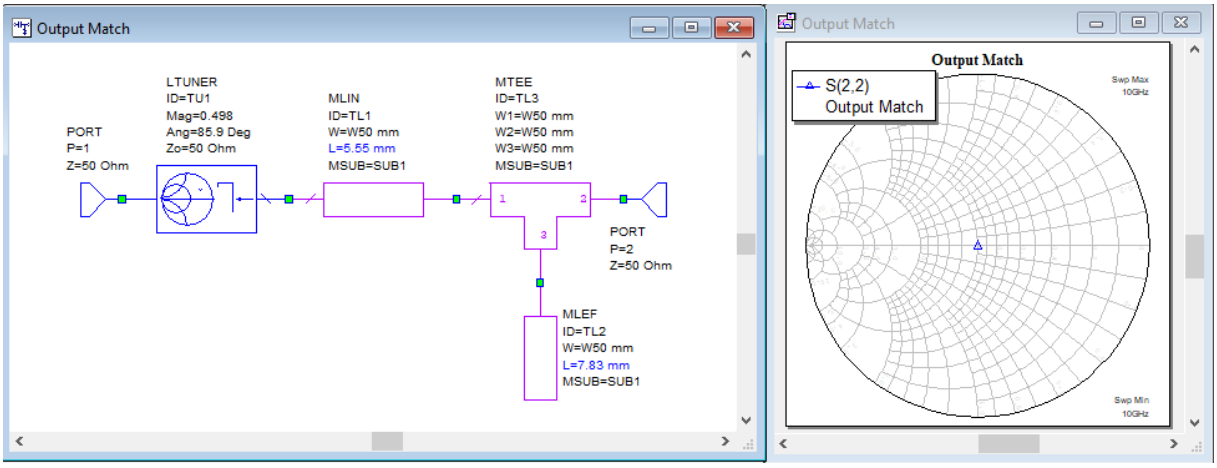

Fig. 7 Output matching circuit with discontinuity and resulting reflection coefficient.

The design should also include the bias circuits. They must enable the connection of the negative Gate bias and the positive Drain bias. But, at the same time, they must not influence the RF circuit in any way. This can be achieved if the impedance of the connecting point is close to ∞. An infinite impedance (open) can be obtained from 0 impedance (short) by a $\lambda_g/4$ impedance transformation. Such a transformer is formed by a $\lambda_g/4$-long TL section. Suitable TL impedance should be 100-120 Ω. Another $\lambda_g/4$ transformer can be used to create the short impedance without the necessity of using a via-hole (a via-hole would short the biasing voltage). Using the transformer in question, the short can be created from an open circuit while TL's impedance should be around 30 Ω in this case. To design such a biasing circuit:

- Create a new schematic called Bias Filter and insert an open section of microstrip line MLEF with width 4 mm and length $\lambda_g/4$ in it. Tune its length to produce a short circuit at the design frequency as shown in Fig. 8.

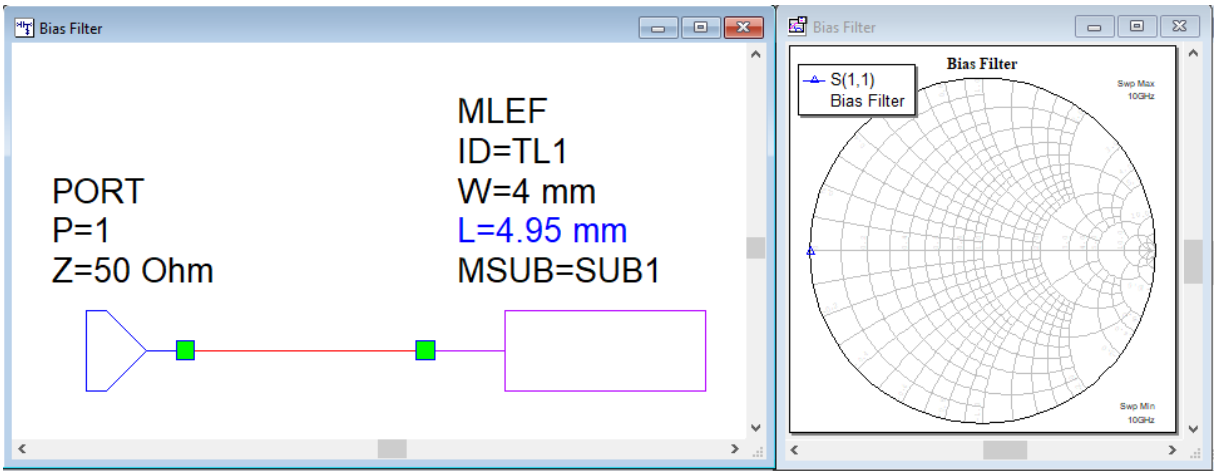

Fig. 8 Open microstrip stub acting as a short circuit at design frequency.

- Add discontinuity MSTEP and MLIN with W = 0.2 mm and length $\lambda_g/4$. Tune TL3's length to produce an open circuit at design frequency as shown in Fig. 9.

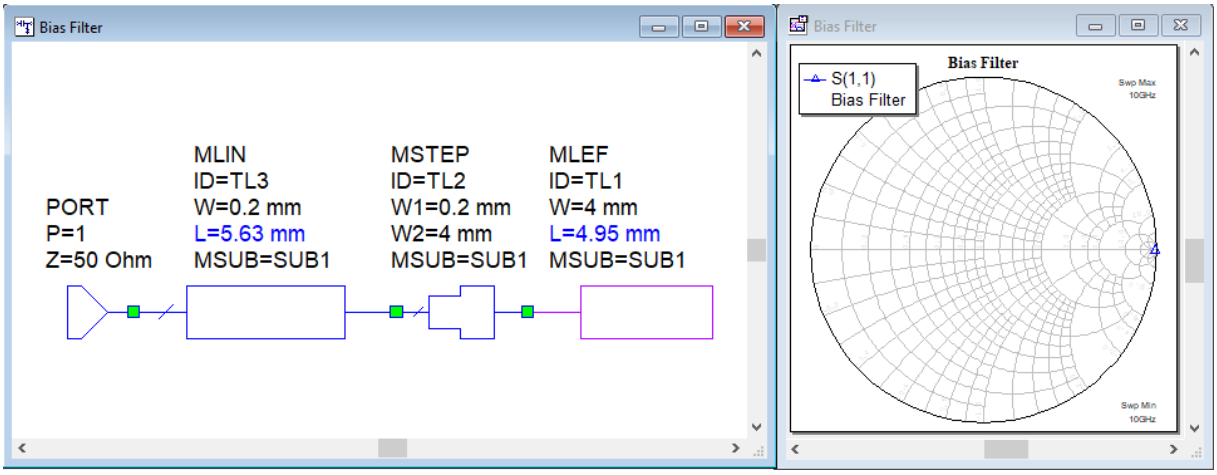

Fig. 9 Series combination of high- and low-impedance transmission line sections forming a bias filter acting as an open circuit at design frequency.

- The biasing voltage can be connected to the MSTEP plane where the impedance is equal to 0 Ω = short.

Assemble the complete amplifier. In the first step without the biasing circuits:

- Do not forget to exclude all LTUNERs.
- Compile the amplifier using SUBCIRCUITS. Create a new schematic Amplifier and place (from the left) schematics Input Match – Transistor − Output Match and connect ports there, as shown in Fig. 10.

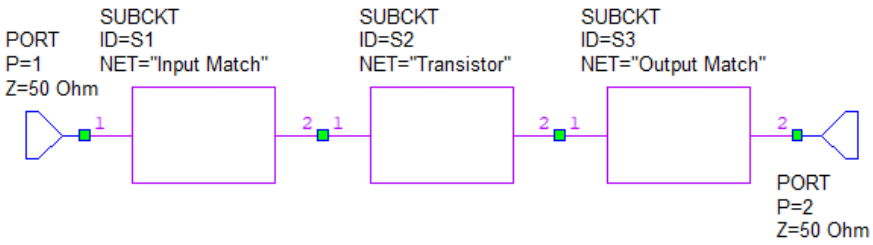

Fig. 10 Schematic of the complete amplifier without bias filters.

- Create a new graph of rectangular type and add measurements from the Amplifier schematic dB(abs(S11)), dB(abs(S21)), dB(abs(S12)) and dB(abs(S22)). Perform an analysis in the f_0 ± 20% frequency band of the resulting amplifier. The demo task leads to the results shown in Fig. 11.

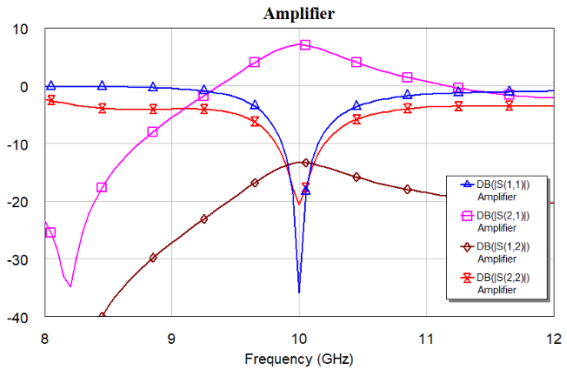

Fig. 11 Resulting S-parameters of the amplifier without bias circuits.

- Add biasing circuits to the Amplifier schematic. Use the MTEE discontinuity models and add 10-mm-long 50 Ω microstrip line sections (to connectors) at both sides as shown in Fig. 12.

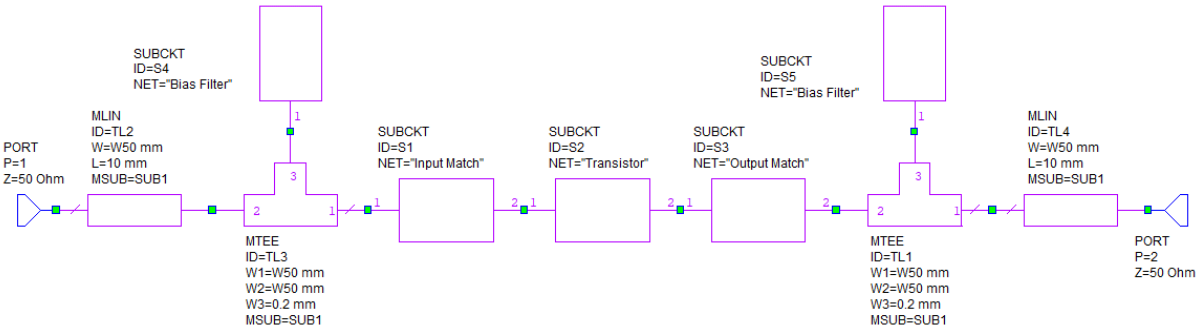

Fig. 12 Schematic of the amplifier including both bias circuits and connecting 50 Ω lines.

- Properly designed and connected biasing circuits must not worsen amplifier RF parameters in any way, as shown in Fig. 13.

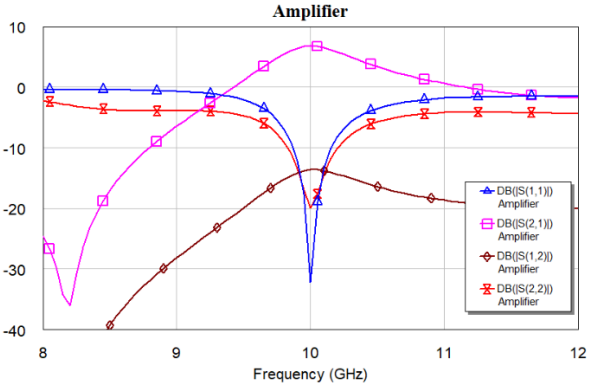

Fig. 13 S-parameters of the final amplifier.

Layout is a physical distribution of microstrip line sections on the substrate. From it, the manufacturing mask can be produced. It can be obtained from the final schematic Amplifier.

- At first, a package must be assigned to the transistor. By drag and drop the *.mdf file from the library to the schematic, the transistor package should be automatically loaded.

- It is almost always necessary to arrange the layouts of all amplifier subcircuits first. Activating CTRL+A (select all), all layout components should change in color to yellow.
- Then activate the SNAP TOGETHER function (situated at the upper bar).
- The layout can be displayed by right clicking the resulting Amplifier schematic and activation of VIEW LAYOUT. A new Amplifier:2 window with the layout will open.
- The final layout of the Amplifier schematic can be seen in Fig. 14.
- In this case, the 50 Ω transmission lines should be narrower for better connection to small pins of gate and drain. It is also necessary add vias to both sources connecting them to the ground.

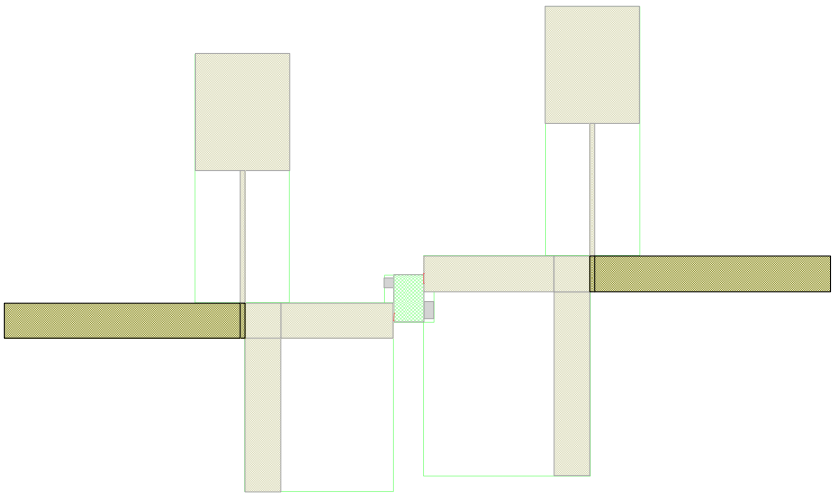

Fig. 14 Layout of the final amplifier.