Chapter 10

Connectors, Packages, and Vias

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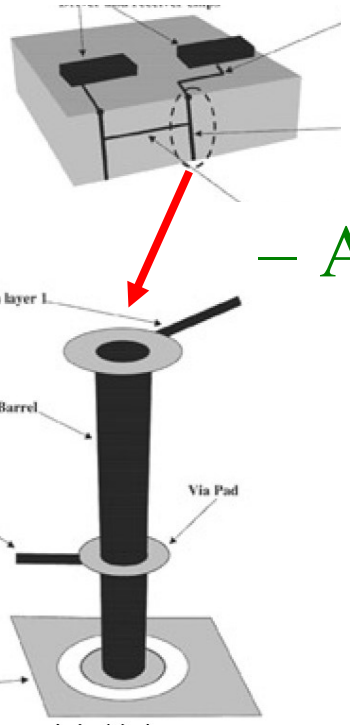
Outline

- Vias
- Connectors
- Chip Packages

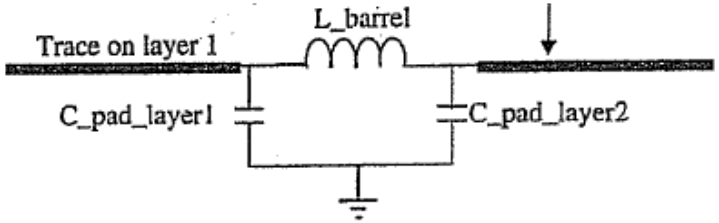
Vias

- Components of Vias
  - Barrel
    - The *barrel* is a conductive material that fills the hole to allow an electrical connection between layers.
  - Pad
    - The *pad* is used to connect the barrel to the component or trace.
  - Antipad
    - The *antipad* is a clearance hole between the pad and the metal on a layer to which no connection is required.



Vias

- Equivalent Circuit of Vias
  - π Network
    - This is valid when delay of the via is smaller than one-tenth of the edge rate.
    - The capacitors represent the via pad capacitance on layers 1 and 2.
    - The series inductance represents the barrel.
    - The via capacitance will slow down the signal edge rate.
    - If several consecutive vias are placed in close proximity it will lower the effective characteristic impedance.



Vias

- Equivalent Circuit of Vias
  - π Network
    - The approximate value of the pad capacitance is

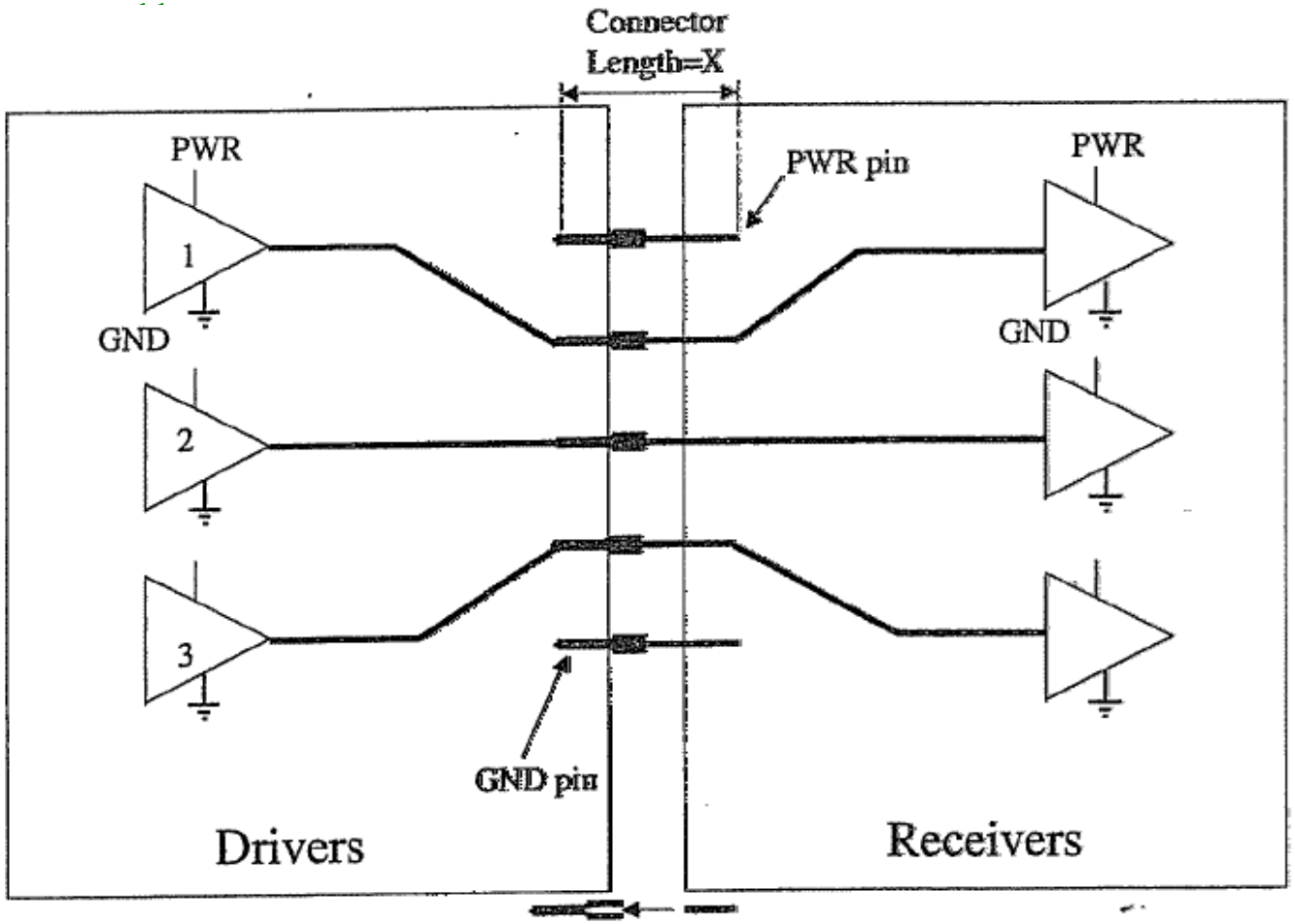
$$C_{\text{via}} \approx \frac{1.41\varepsilon_r D_1 T}{D_2 - D_1} \quad \text{picofarads}$$

    - where D_2 is the diameter of the antipad, D_1 the diameter of the via pad, T the thickness of the PCB.
    - The inductance of the vias is usually more important than the capacitance, which will degrade the signal integrity and decrease the effect of decoupling capacitors.
    - The via inductance can be approximated by

$$L \approx 5.08h\left[\ln\left(\frac{4h}{d}\right) + 1\right] \quad \text{nanohenries}$$

Connectors

- Equivalent Circuit
  - Series Inductance, Shunt Capacitance, Cr



Connectors

- Equivalent Circuit
  - Series Inductance
    - A series inductance can be estimated to a first-order level with the use of simple straight-wire formulas.
    - Estimates for the series inductance of round and rectangular wire, respectively, are

$$L \approx \frac{\mu_0}{2\pi} l \left[\ln\left(\frac{2l}{r}\right) - \frac{3}{4} \right] \quad \text{nanohenries} \quad \text{for} \quad r \ll 1$$

$$L \approx \frac{\mu_0}{2\pi} l \left[\ln\left(\frac{4l}{p}\right) + \frac{1}{2} \right] \quad \text{nanohenries}$$

    - where l the length, r the radius of the wire, and p the perimeter.

Connectors

- Equivalent Circuit
  - Shunt Capacitance
    - It can usually be ignored in the initial design.
    - It will slow down the system edge rate.
    - The addition of extra capacitance is sometimes used to mitigate the impedance discontinuity seen at the connector.
    - Extra capacitance can be added by using a wider pad, adding a small tab or widening out the connector pins.

Connectors

- Equivalent Circuit
  - Connector Crosstalk
    - Typically, the mutual inductance plays a larger role than mutual capacitance.
    - The mutual inductance between two connector pins can be can be approximated as

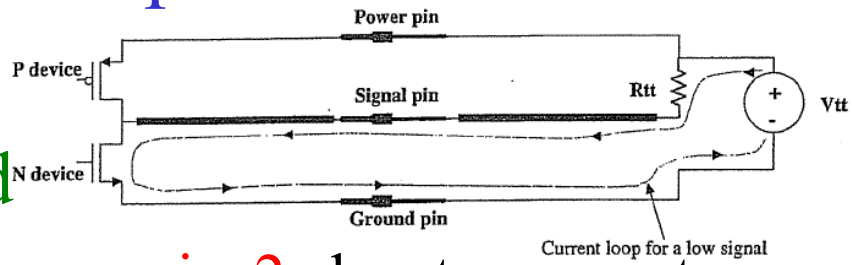
$$L_M \approx \frac{\mu_0}{2\pi} l \left[\ln\left(\frac{l}{s} + \sqrt{1 + \left(\frac{l}{s}\right)^2} \right) - \sqrt{1 + \left(\frac{s}{l}\right)^2} + \frac{s}{l} \right] \quad \text{nanohenries} \quad (5.$$

$$L_M \approx \frac{\mu_0}{2\pi} l \left[\ln\left(\frac{2l}{s}\right) - 1 \right] \quad \text{nanohenries} \quad \text{for} \quad s \ll l \quad (5.$$

    - where l the length, and s the center-to-center spacing between the wires
    - The mutual inductance is largely independent on the cross-sectional area and the shape of the conductor.

Connectors

- Effects of Inductively Coupled Connector Pin Fields
  - Ground Effects Excluded



    - The total induced voltage on pin 2 due to current changes in itself and pins 1 and 3 is

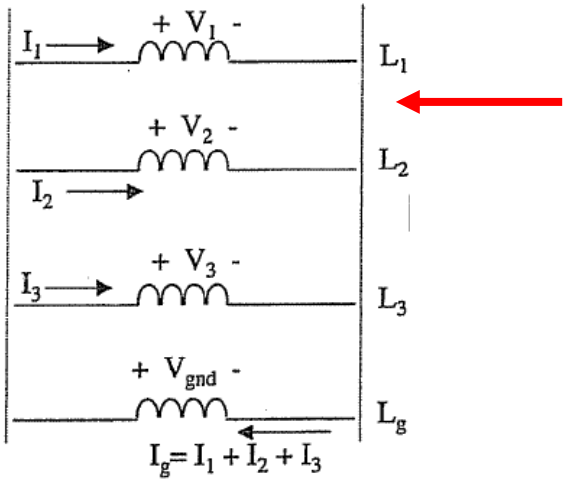
$$v_2 = L_{22}\dot{I}_2 + L_{21}\dot{I}_1 + L_{23}\dot{I}_3$$

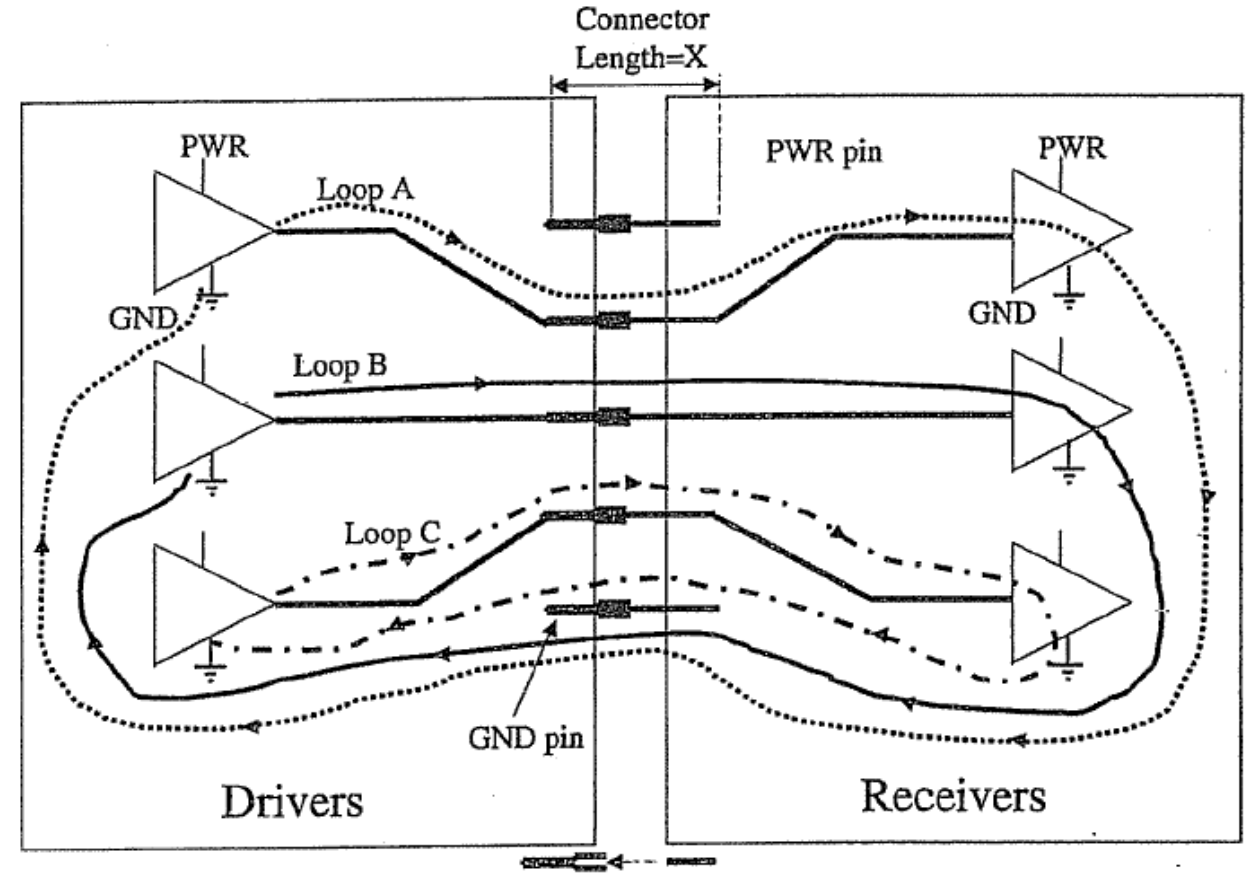
    - Assuming that the currents and the slew rates for each buffer are the same, a single-line equivalent model can be created

$$v_2 = \begin{cases} (L_{22} + L_{21} + L_{23})\dot{I} & \text{(all bits switching in phase)} \\ (L_{22} - L_{21} - L_{23})\dot{I} & \text{(bit 2 switching out of phase with bits 1 and 3)} \end{cases}$$

Connectors

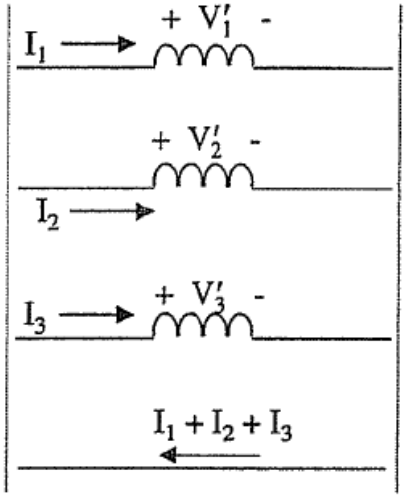
- Effects of Inductively Coupled Connector Pin Fields
  - Ground Effects Included





Connectors

- Effects of Inductively Coupled Connector Pin Fields
  - Ground Effects Included
    - The response of the system is shown as



$$V_2 = L_{22}\dot{I}_2 + L_{21}\dot{I}_1 + L_{23}\dot{I}_3 + L_{2g}\dot{I}_g$$

$$V_{gnd} = L_{gg}\dot{I}_g + L_{g1}\dot{I}_1 + L_{g2}\dot{I}_2 + L_{g3}\dot{I}_3$$

$$\dot{I}_g = -(\dot{I}_1 + \dot{I}_2 + \dot{I}_3) \rightarrow V_2' = V_2 - V_{gnd}$$

$$V_2' = \dot{I}_1(L_{21} - L_{2g} - L_{g1} + L_{gg}) + \dot{I}_2(L_{22} - L_{2g} - L_{g2} + L_{gg}) + \dot{I}_3(L_{23} - L_{2g} - L_{g3} + L_{gg})$$

$$\rightarrow V_2' = L_{22}'\dot{I}_2 + L_{21}'\dot{I}_1 + L_{23}'\dot{I}_3$$

- For a group of *n* conductors with a single current return path: $L_{ij}' = L_{ij} - L_{ig} - L_{gj} + L_{gg}$

Connectors

- Effects of Inductively Coupled Connector Pin Fields
  - Ground Effects Included
    - The equations above are valid only for a coupled array of pins.
    - The total loop inductance of loop *A* has the largest total inductance, and loop *C* is the smallest.
    - Ways to reduce crosstalk effects:
      - maximize the total number of power and ground pins to decrease the total inductive path. It will effectively decrease L_{gg}.
      - place power and ground pins adjacent to each other because the currents flows in opposite directions.

Also, the area of the loop is proportional to the emission radiated.

Connectors

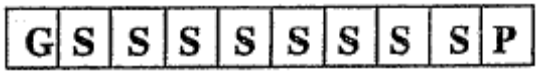
- Connector Design Guidelines
  - Non-Differential Signals
    - Minimize the physical length of the connector pins to reduce the total series inductance.
    - Maximize the power and ground to signal pin ratio.
    - Each signal pin should be placed in close proximity to a power and a ground pin.
  - Differential Signals
    - The number of power and ground pins required will probably be far less than those for a similar single-ended system.
    - Without power or ground pins separating them.

Connectors

- Connector Design Guidelines
  - Conclusions
    - Each signal pin should be tightly coupled to a current return pin.
    - The power and ground pins should be placed adjacent to each other.
    - The ratio of power pins to signal pins and the ratio of ground pins to signal pins are greater or equal to 1.
    - To use the shortest connector.
    - To increase the connector pin capacitance. But connector capacitance tends to slow the edge rates.

Connectors

- Connector Design Guidelines



  - Example 5.1 Choosing a Connector Pin Pattern
    - This will exhibit the worst performance because the power and ground pins are physically very far apart from the signal pins.
    - This pin-out will maximize the inductive noise since the return current will travel through a single power or ground pin.
    - Large current loops can exacerbate connector-related EMI and increase series inductance.
    - Since all the signal pins are adjacent to each other, pin-to-pin crosstalk noise will be maximized.

Connectors

- Connector Design Guidelines
  - Example 5.1 Choosing a Connector Pin Pattern
    - An increased number of power and ground pins will provide for lower-inductance current return paths and provide better power delivery.
    - Pin-to-pin crosstalk is also reduced.
    - The crosstalk between pairs, however, can still be quite high.
    - Notice that the connector size has increased by 30%.

    - This is the optimal for the differential signaling but not the optimal for a single-ended signaling.

Connectors

- Connector Design Guidelines
  - Example 5.1 Choosing a Connector Pin Pattern
    - Both a power and a ground pin surround each signal pin. This minimizes the return current path inductance through both the power and ground pins.
    - Pin-to-pin crosstalk between signals is reduced.
    - The size of the connector has increased by 70%.

G	S	P	S	G	S	P	S	G	S	P	S	G	S	P	S	G

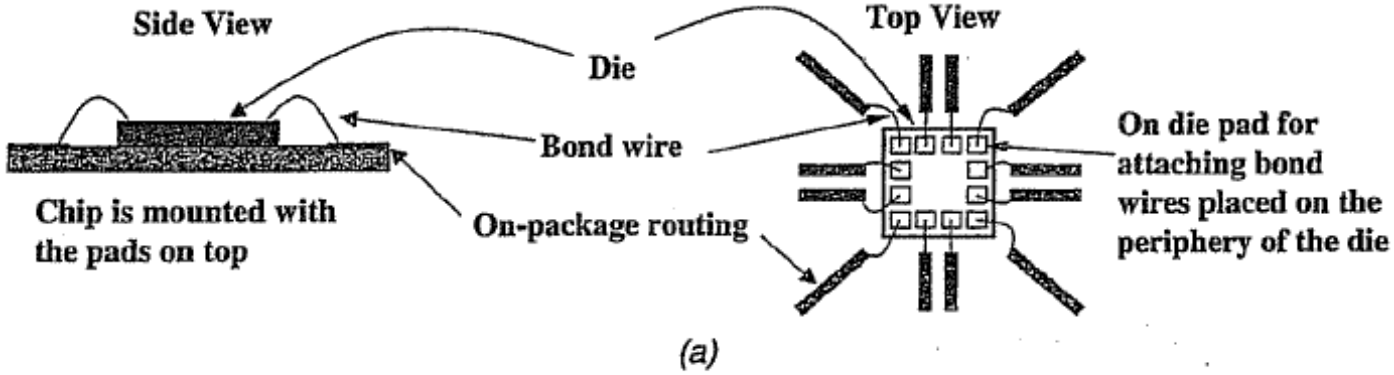
    - The power and ground pins are always adjacent to each other.
    - The best one is

G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P

    - where the power/ground-to-signal ratio is 9 : 8.

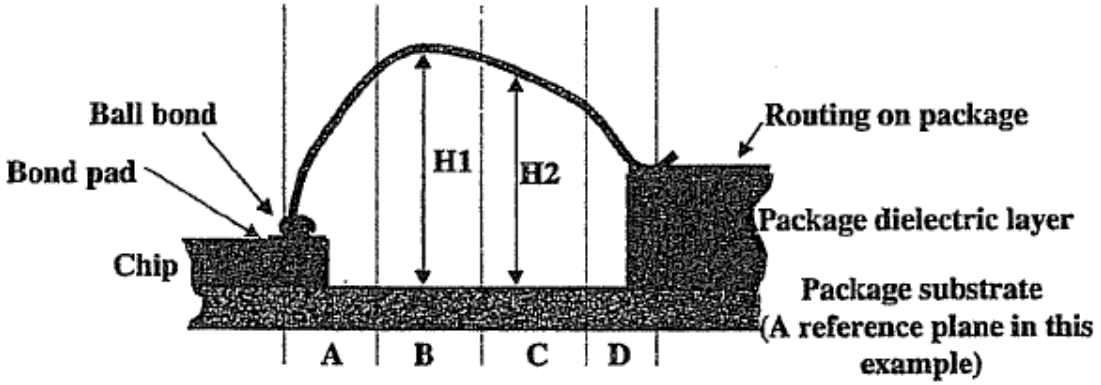
Chip Packages

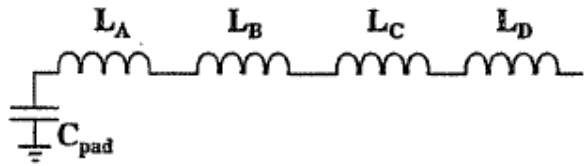
- Common Types of Packages
  - Attachment of the Die to the Package
    - Wire bond and flip chip attachments



Chip Packages

- Common Types of Packages
  - Attachment of the Die to the Package—Wire Bond
    - A wire bond is simply a very small wire with a diameter on the order of 1 mil.
    - Bond wire lengths vary from approximately 50 to 500 mils.





Chip Packages

- Common Types of Packages
  - Attachment of the Die to the Package—Wire Bond
    - Section *A* is roughly perpendicular to the reference plane; subsequently, the reference plane will have a minimal effect.
    - Section *B* is roughly parallel to the reference plane with an approximate height of H_1. Subsequently, the inductance L_B must be calculated using the inductance of a straight wire in the presence of a ground plane. $L = l(5.08 \times 10^{-9}) \ln \frac{4h}{d}$ nanohenries
    - where l is the length in inches, h the height above the ground plane, and d the wire diameter.

Chip Packages

- Common Types of Packages
  - Attachment of the Die to the Package—Wire Bond (Disadvantages)
    - Wire bonds also exhibit a large amount of crosstalk, which will cause pattern-dependent inductance values and ground return path problems.
    - The mutual inductance for two bond wires above a local ground plane is

$$L_M = L\frac{1}{1+(s/h)^2} \quad \text{nanohenries}$$

    - where L is the self-inductance of the two bond wires, s the center-to-center spacing, and h the height above the ground plane.

Chip Packages

- Common Types of Packages
  - Attachment of the Die to the Package—Wire Bond (Advantages)
    - They are inexpensive, mechanically simple, and allow for some changes in the bonding pad location and package routing.
    - Furthermore, since the back of the chip is attached directly to the package substrate, it maximizes heat transfer out of the die.
    - (Disadvantage) The I/O pads tend to be limited to the periphery of the die, which will inflate the die size for a large number of I/O.

Chip Packages

- Common Types of Packages
  - Attachment of the Die to the Package—Flip Chip (Advantages)
    - Flip-chip technology is also said to be *self-aligning*.
    - The series inductance of a flip-chip connection is much lower. The typical inductance is on the order of 0.1 nH.
    - Furthermore, the effect of crosstalk in a flip-chip connection can be ignored at low frequencies.
    - The bonding pads for a flip-chip connection can be placed over the entire die, not just on the periphery. This will help to minimize die size when a large number of I/O cells are required.

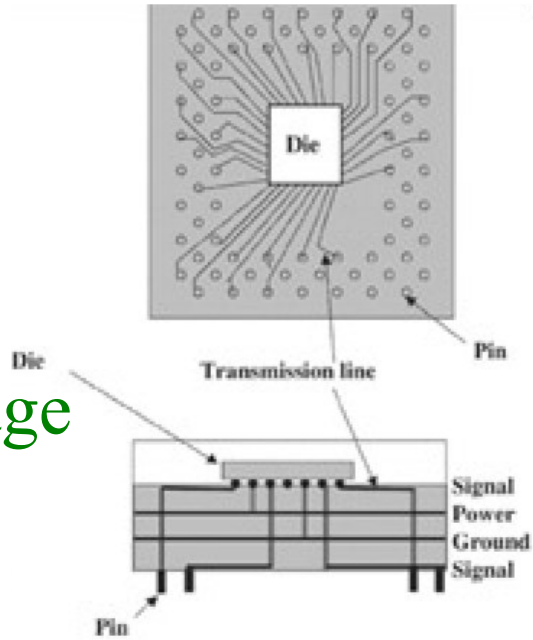
Chip Packages

- Common Types of Packages
  - Attachment of the Die to the Package—Flip Chip (Disadvantages)
    - Mechanically and thermally, however, flip-chip technology is dismal.
    - The thermal coefficient of expansion must be very close between the die and the package substrate.
    - Furthermore, the physical tolerances must be very tight.
    - Cooling is also more difficult with flip-chip technology.

Table 5.1: Comparison of Wire Bond and Flip-Chip Technology

	Series Inductance (nH)	Minimum Pitch (mils)	I/O Placement	Cooling
Wire bond	1–5	4–6	Periphery only	Easy
Flip chip	0.1	2–3	Entire surface	Difficult

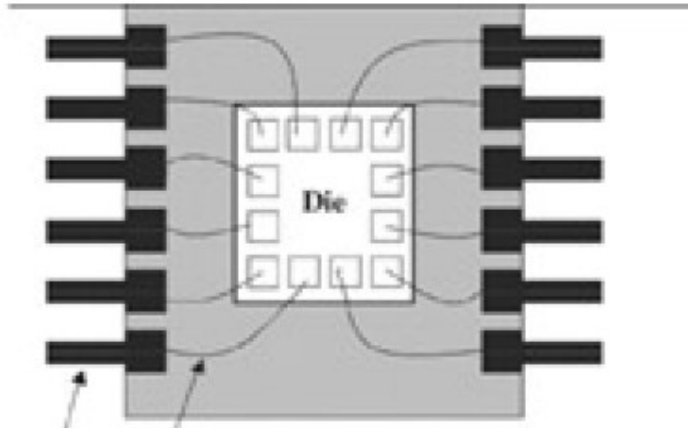
Chip Packages

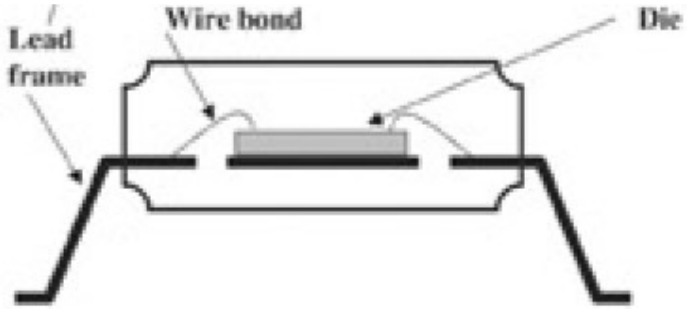


- Common Types of Packages
  - Routing of the Signals on the Package
    - *Controlled Impedance:*
    - For high-speed digital designs
    - This package typically resembles a miniature PCB board with different layers and power and ground planes with a centered cavity used for die placement.
    - The chip is usually attached with flip-chip bonding, although short wire bonds are often used.
    - Small-dimensioned transmission lines are used to route the signals from the bond pad on the package to the board attachment.

Chip Packages

- Common Types of Packages
  - Routing of the Signals on the Package
    - *Noncontrolled Impedance:*
    - Noncontrolled-impedance packages usually wire bond the die directly to a lead frame, which is then soldered to the board.
    - This creates a series inductance that can wreak havoc on the signal integrity.



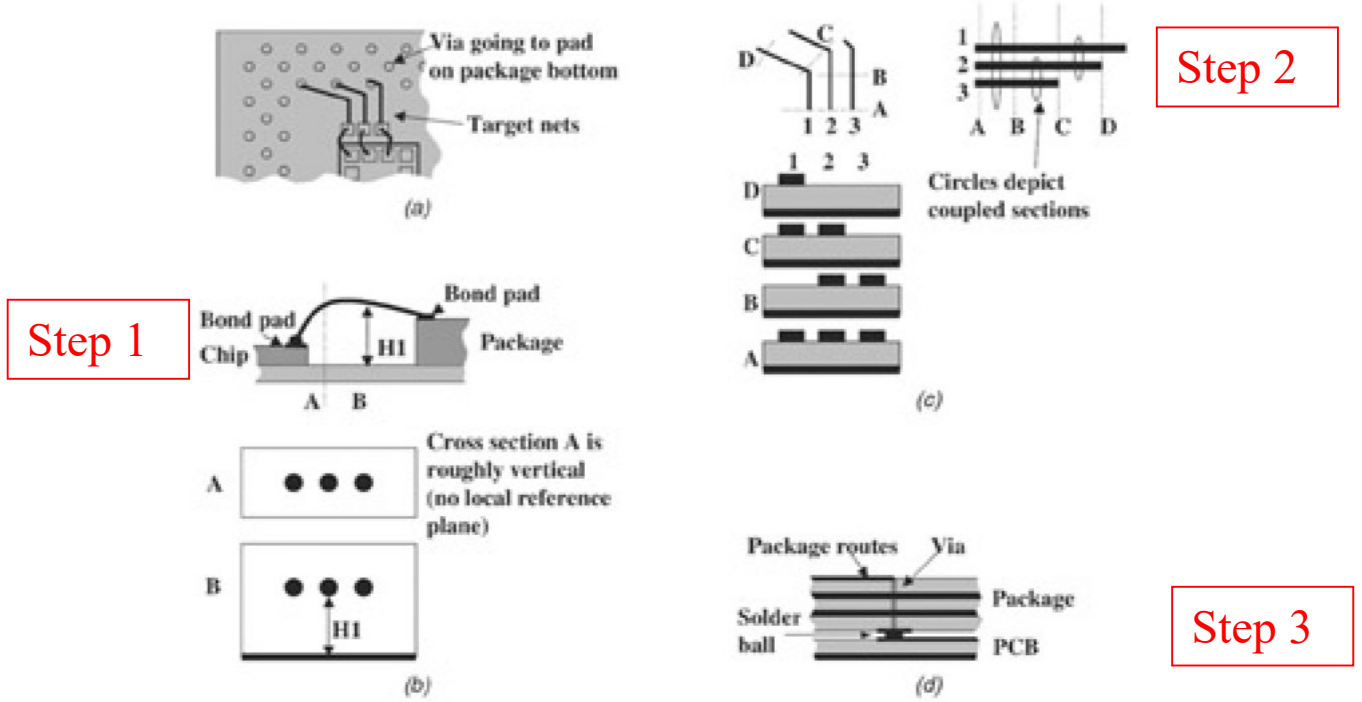


Chip Packages

- Common Types of Packages
  - Attachment of the Package to the Board
    - *A Lead Frame:*
    - A *lead frame* is simply a metal frame that is integral to the package, which provides an electrical connection between the wire bonds and the PCB.
      - A through-hole mount is achieved by drilling a hole through the PCB, inserting the lead frame pins through the hole, and re-flowing solder.
      - A surface-mount attachment is achieved by soldering the lead frame pins onto pads on the surface layer of the PCB.
    - A *pin-grid array*:
    - A *pin-grid array* (PGA) consists of an array of pins that stick out of the bottom part of the package.

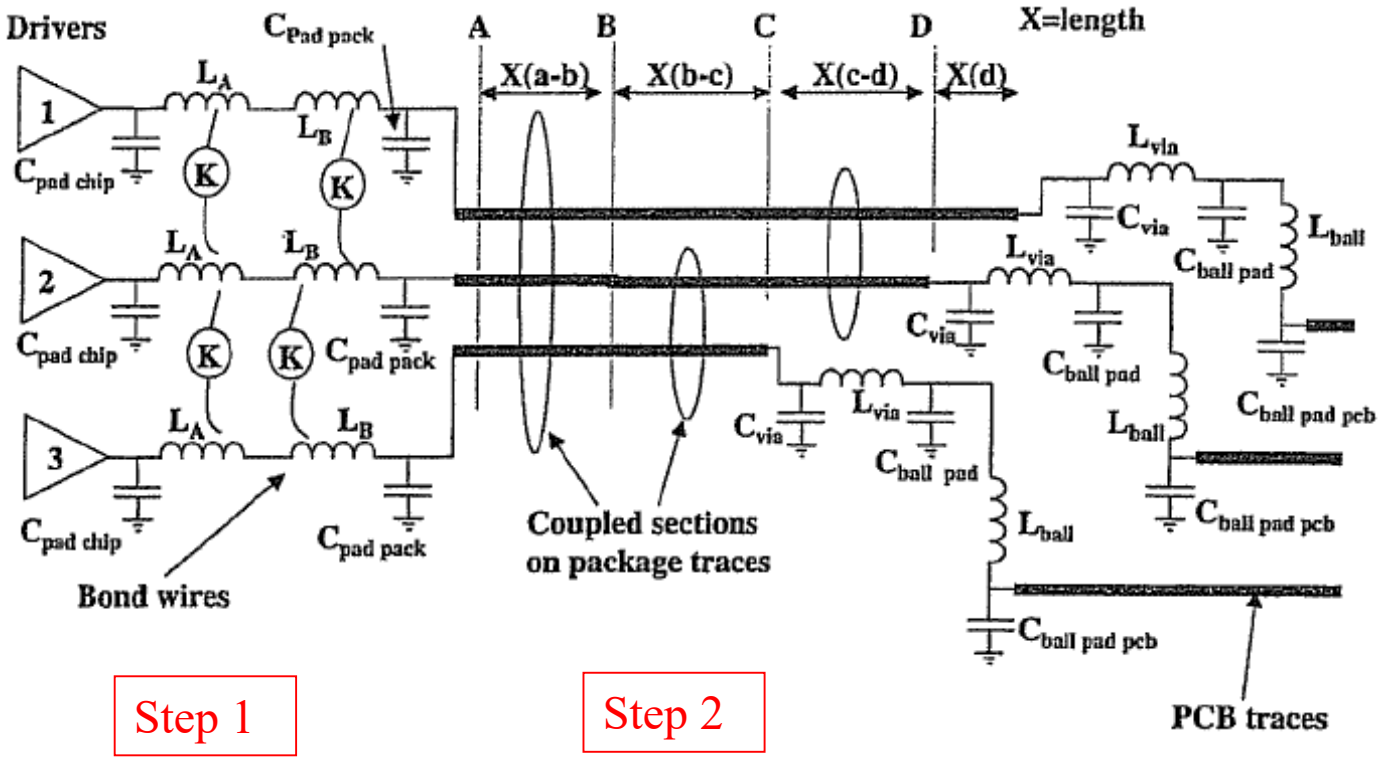
Chip Packages

- Creating a Package Model
  - Example 5.2 Controlled-Impedance Package
    - Step 1: Attachment of the die to the package
    - Step 2: Routing of the signals on the package
    - Step 3: Attachment of the package to the PCB



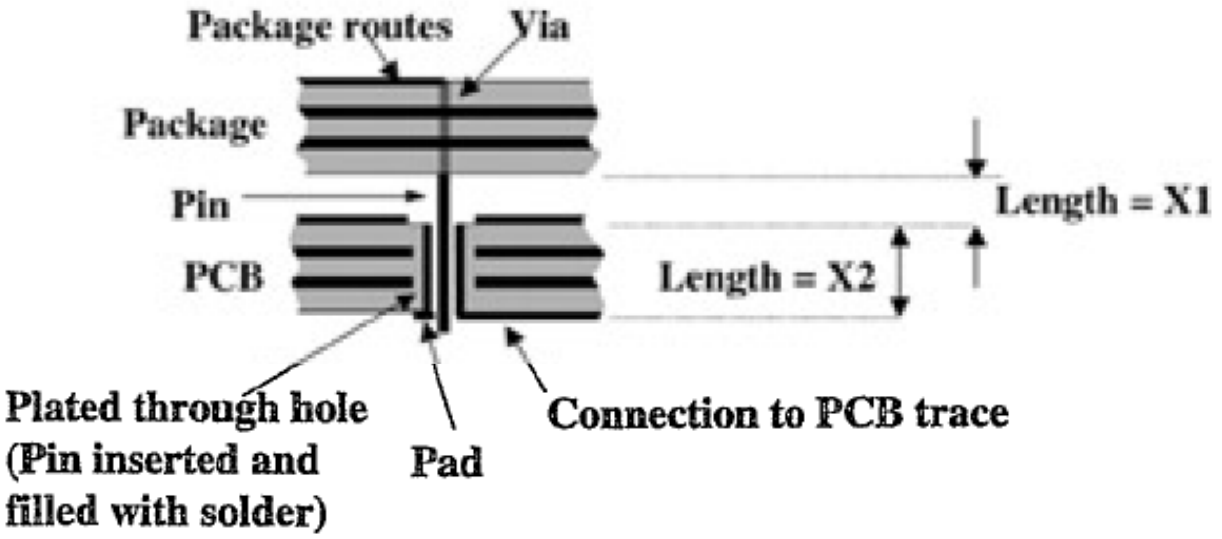
Chip Packages

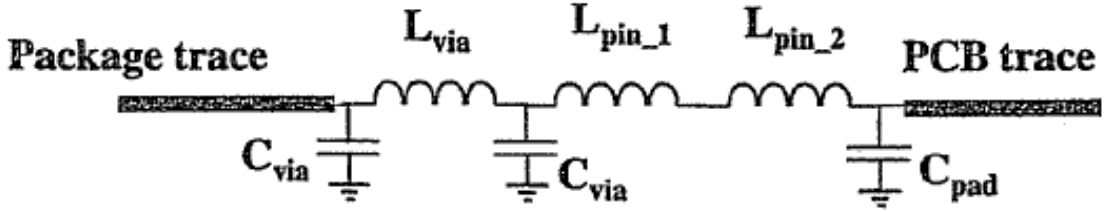
- Creating a Package Model
  - Example 5.2 Controlled-Impedance Package
    - The equivalent circuit is shown below.



Chip Packages

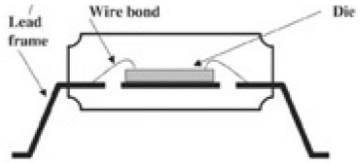
- Creating a Package Model
  - Example 5.2 Pin-Grid-Array Attachment



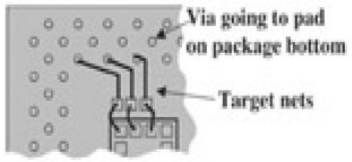


Chip Packages

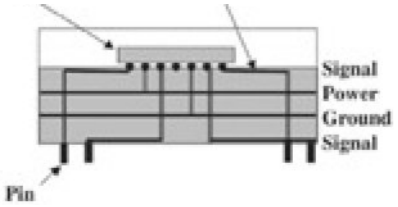
- Effect of a Package
  - Point-to-Point Bus Topology



- *Case 1*: noncontrolled-impedance package with a total bond length (bond wire plus lead frame) of 0.75 in.



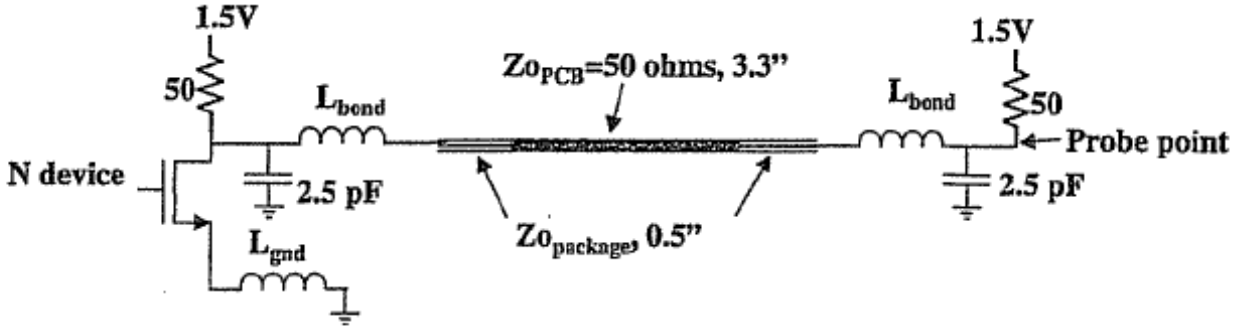
- *Case 2*: controlled-impedance package with 0.25-in. bond wires and a 40-Ω transmission line on the package.

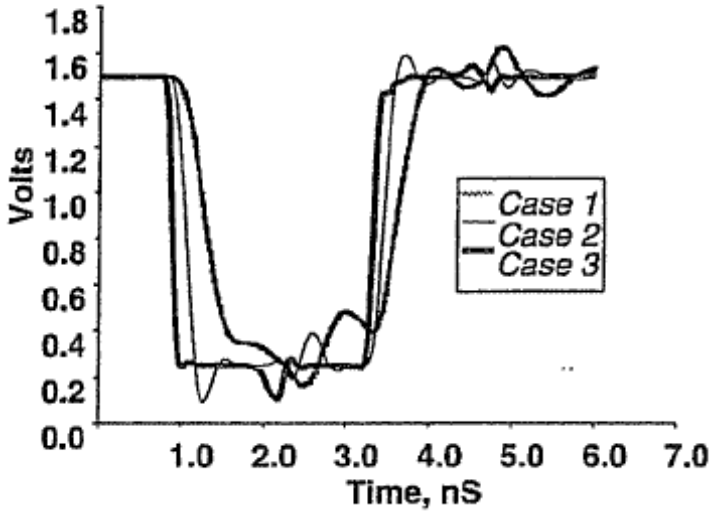


- *Case 3*: controlled-impedance package with die flip-chip attached to the package and 40-Ω package routing.

Chip Packages

- Effect of a Package
  - Point-to-Point Bus Topology





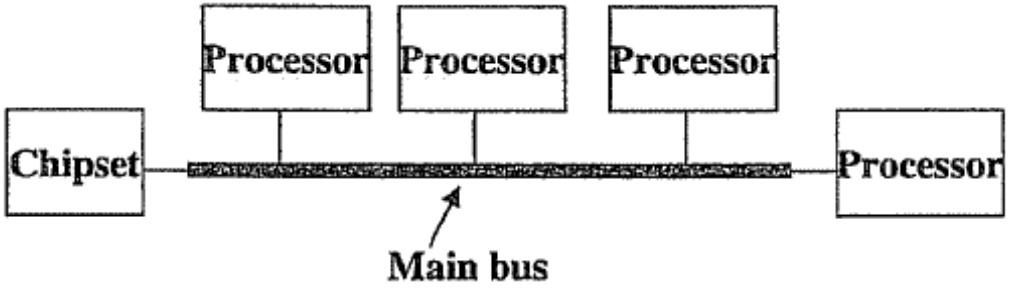
	$Zo_{package}$	L_{bond}	L_{gnd}
Case1	50 ohm	15nH	1.5nH
Case2	40 ohm	5nH	0.5nH
Case3	40 ohm	0.1nH	0.01nH

Chip Packages

- Effect of a Package
  - Point-to-Point Bus Topology
    - The edge rate has been slowed significantly due to the extra inductance. This is because the inductance will act as a low-pass filter, which will attenuate the high-frequency components.
    - Case3 is the best one, case 2 is the secondary one and case 1 is the worst one. ($L_{case3}<L_{case2}<L_{case1}$)
    - Also, the crosstalk between bond wires and leads in case 1 cause significant pattern-dependent inductance values (due to the mutual inductance), which will cause edge-rate differences and degrade timing margins further.

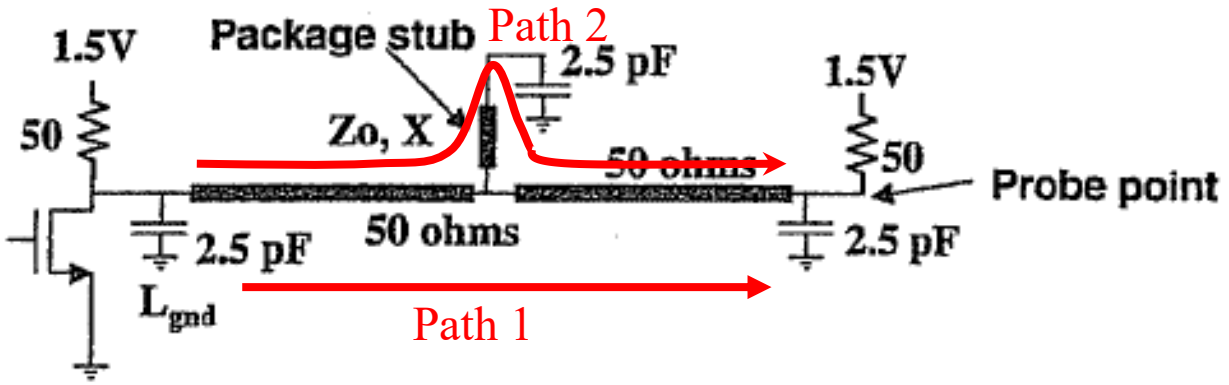
Chip Packages

- Effect of a Package
  - Multidrop or Daisy Chain Topologies
    - The effect of packaging on such bus topologies is largely dependent on the package stub length:
      - If the package stub is long, it will induce transmission line reflections that degrade the signal quality.
      - If the package length is short, it will produce significant filtering effects that degrade the edge rate and change the effective characteristics of the transmission line.



Chip Packages

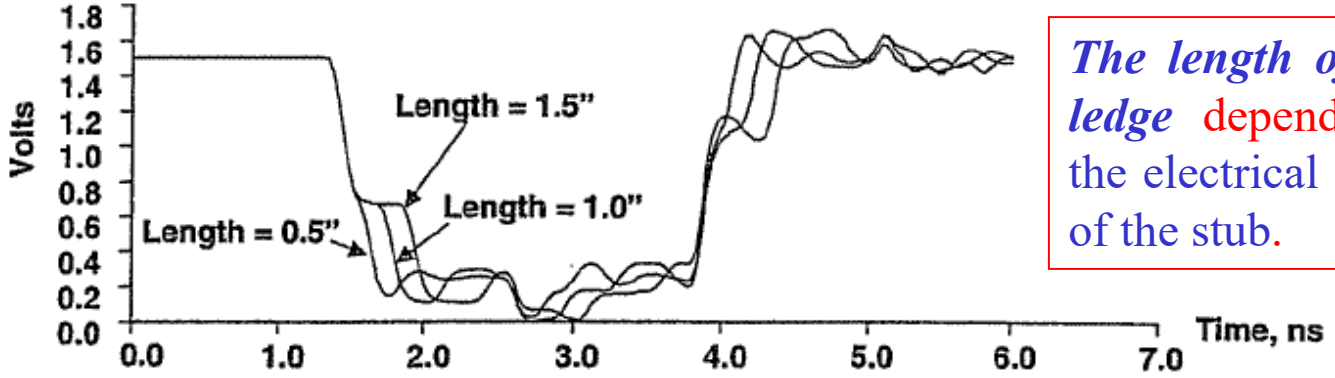
- Effect of a Package
  - Long Package Stub Effect
    - A package stub is considered to be long if $TD_{stub} > \frac{1}{2}T_{10-90\%}$
    - where TD_{stub} is the electrical delay of the unloaded package stub and $T_{10-90\%}$ is the rise or fall time of the signal edge.



Chip Packages

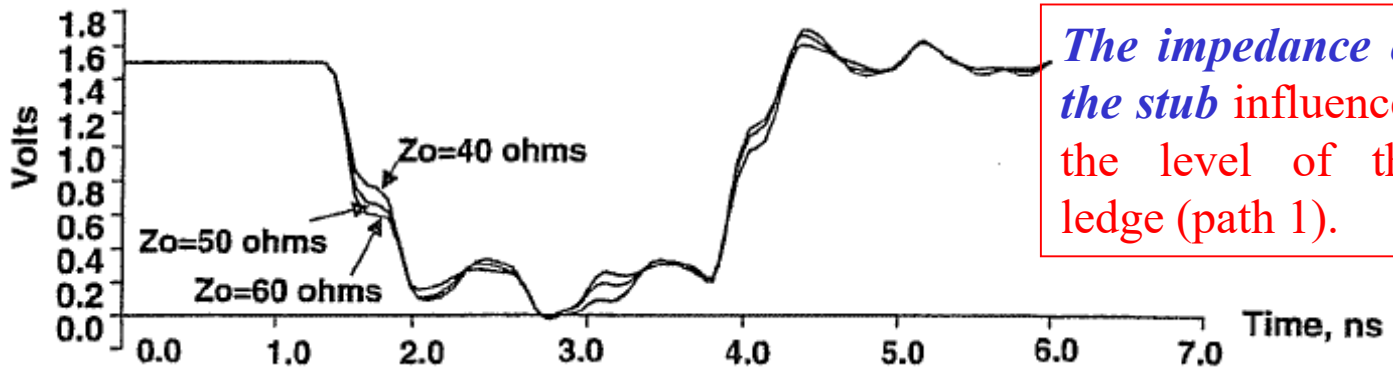
- Effect of a Package
  - Long Package Stub Effect
    - Effect of package stub length:

The capacitive loading at the end of the stub will increase the effective electrical delay of the stub by approximately 1 time constant (Z_0C).



The length of the ledge depends on the electrical delay of the stub.

- Effect of package stub impedance



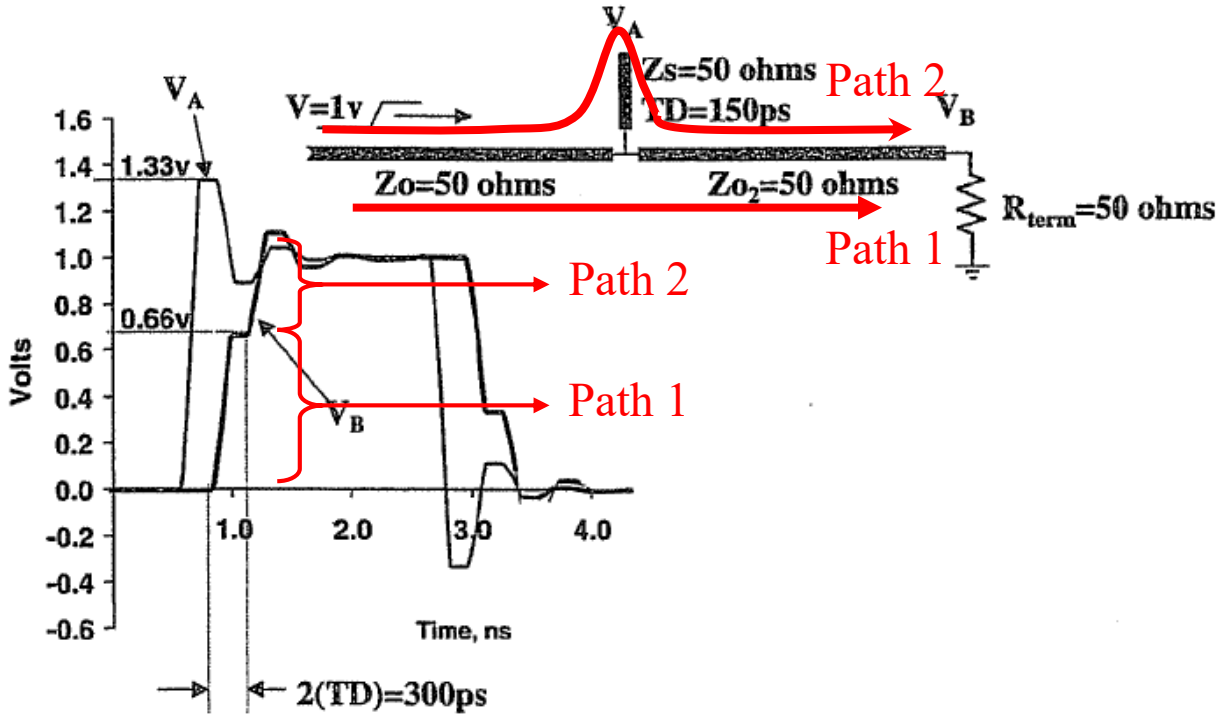
The impedance of the stub influences the level of the ledge (path 1).

Chip Packages

- Effect of a Package
  - Example 5.4 Effects of a Long Package Stub
    - The reflection coefficient looking into the stub junction is

$$\rho_{\text{at stub}} = \frac{Z_s \| Z_{o_2} - Z_o}{Z_s \| Z_{o_2} + Z_o} = -\frac{1}{3}$$

$T=1+\rho_{\text{at stub}}=2/3$



Chip Packages

- Effect of a Package
  - Example 5.4 Effects of a Long Package Stub
    - The transmission coefficient down the stub and the second half of the trunk is

$$T = 1 + \rho_{\text{at stub}} = 1 + \frac{Z_s \| Z_{o_2} - Z_o}{Z_s \| Z_{o_2} + Z_o} = \frac{2}{3}$$

    - Subsequently, the voltage arrived first at node *B* (path 1) is

$$V_B = VT = 1.0\left(\tfrac{2}{3}\right) = 0.666 \text{ V}$$

    - The voltage arrived secondly at node *B* (path 2) is

0.66V*(2/3)=0.44 V

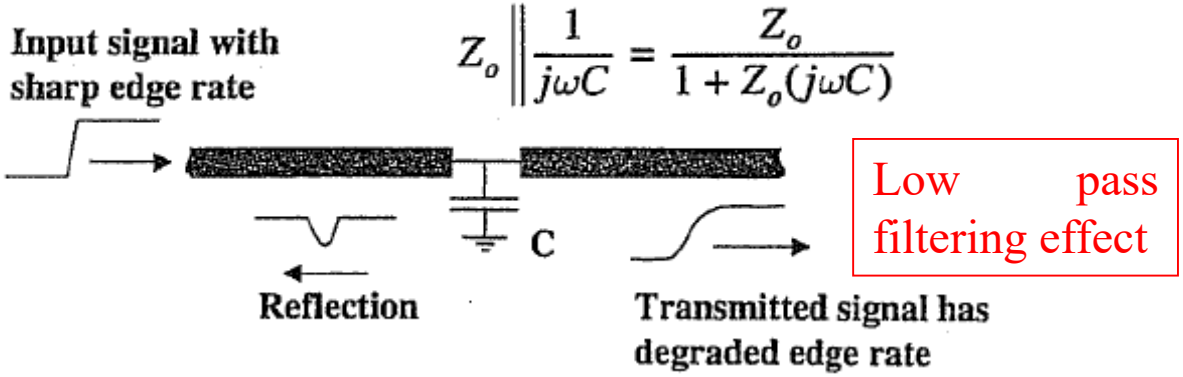
    - The voltage from the first reflection at node *A* is

$$V_A = 2VT = 1.33 \text{ V}$$

The timing push-out caused by the stub at node B depends on twice the total delay of the stub.

Chip Packages

- Effect of a Package
  - Widely Spaced Short Package Stub Effect
    - A package stub is considered to be short if $\mathrm{TD}_{\mathrm{stub}} < \frac{1}{2} T_{10\text{–}90\%}$
    - where $\mathrm{TD}_{\mathrm{stub}}$ is the electrical delay of the unloaded package stub and $T_{10\text{–}90\%}$ is the rise or fall time of the signal edge.
    - When a package stub is sufficiently short, the load will look like a capacitor.



Chip Packages

- Effect of a Package
  - Widely Spaced Short Package Stub Effect
    - The reflection and transmission coefficients are

$$\rho_{cap} = \frac{Z_o \| (1/j\omega C) - Z_o}{Z_o \| (1/j\omega C) + Z_o} = \frac{-Z_o(j\omega C)}{2 + Z_o(j\omega C)} \approx \frac{-Z_o(j\omega C)}{2}$$

$$T_{cap} = 1 + \rho_{cap} \approx 1 - \frac{Z_o(j\omega C)}{2}$$

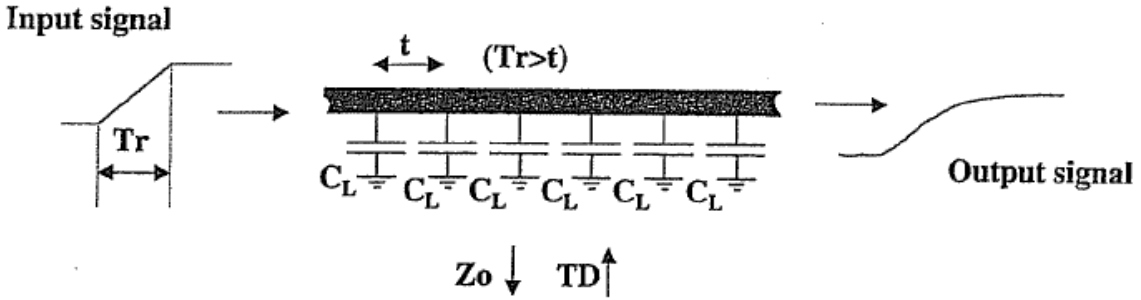
    - As the capacitance increases, the transmission coefficient decreases for a given frequency.
    - Assuming a very fast input edge rate, the transmitted edge will have an edge rate approximately equal to

$$T_{edge} \approx \frac{2.2(Z_o C)}{2}$$

    - The rise or fall time of the signal after it passes though the capacitive load is $T_{system} \approx \sqrt{T_{edge}^2 + T_{input}^2}$

Chip Packages

- Effect of a Package
  - Distributed Capacitive Loading on a bus (Narrow Spacing)
    - RIMM memory module:



    - The equivalent impedance and delay parameters for a uniformly capacitive loaded are

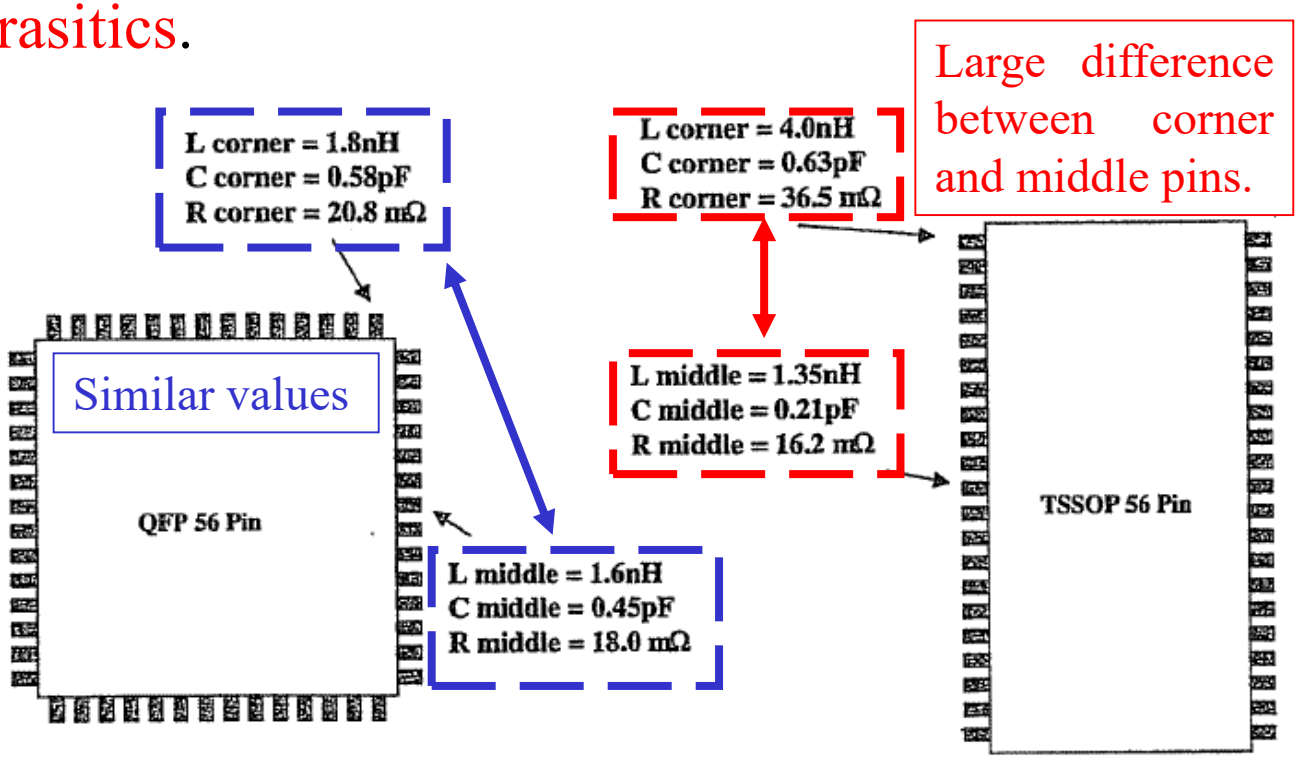
$$Z_o' = \sqrt{\frac{L}{C + NC_L/X}} \downarrow \qquad TD' = \sqrt{L\left(C + \frac{NC_L}{X}\right)} \uparrow$$

Per unit length delay

    - where L and C are the distributed transmission line parasitics, N the number of loads, and X the line length.

Chip Packages

- Optimal Pin-Outs
  - Square v.s. Rectangular Shape
    - In some applications, pin-to-pin parasitic matching is more important than minimizing total pin parasitics.



Chip Packages

- Package Design
  - Rules of Thumb
    - Use controlled packaging for a high-speed design.
    - Minimize inductance by using flip-chip or the shortest possible bond wire lengths for die attachment.
    - Follow all the same pin-out rules of thumb as described for connector design when choosing power and ground pin ratios.
    - Use the shortest possible package interconnect lengths to minimize impedance discontinuities and stub effects.

Chip Packages

- Package Design
  - Rules of Thumb
    - On a multidrop bus, stub length is often the primary system performance inhibitor.
    - In a multidrop bus design, never use long stubs that are narrowly spaced.
    - Pin-to-pin package parasitic mismatch, which is strongly affected by the physical aspect ratio of the package, should be considered.