CE721 Electronics Design Coursework
Second Assignment Report

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Abstract: This report will discuss the design, simulation, and analysis of a digital dice circuit using standard integrated circuits. In this design, the circuit will generate a pseudo-random number between one and six using a clock-based counter. A 555 timer IC will be used in astable mode as a pulse generator. This will generate a continuous clock signal. A decade counter IC will then convert the clock pulses into sequential digital signals. These signals will then be used as output to display the dice using an LED. A push-button switch will be used as a reset/enable mechanism. This will allow the final output of the counter to be held and then read as the output of the dice. This circuit can then be implemented using a breadboard or PCB. This project will cover various concepts such as clock generation, digital counters, timing control, and output decoding using simple ICs.

Keywords: digital dice, 555 timer, CD4017 decade counter, CMOS logic, astable pulse generation, clock signal, LED display mapping, diode logic, push-button control, Multisim simulation.

GitHub: https://github.com/simaygoktug/embedded_programming_stm32

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1 Introduction

In modern electronic systems, digital logic circuits play important roles in counting, sequencing, timing, and state control. The design and development of a digital dice circuit may provide an effective example to illustrate fundamental digital design principles.

This assignment describes the design and development of a digital dice system using a NE555 timer as the clock and CD4017 as the sequential state machine. The system will generate a sequence of numbers from 1 to 6, represented by LED displays arranged in the traditional dice configuration. The system will increment the counter by exactly one step with each press of the push button. The selected output will be latched and will remain valid until the next button press.

This design follows the classical 555-4017 dice configuration as presented in various literature on digital electronics **[1]**. The final design has been optimized to meet the requirements of stable simulation behavior, absence of switch bounce effects, and proper state machine operations. The component selection has been done carefully too:

- Ensure proper and stable transient simulation behavior
- Completely eliminate the effects of switch bounce
- Allow proper and visible LED output transitions
- Meet proper CMOS logic conditions at 5V supply

The system will use a regulated 5V supply and will use RC timing networks to generate proper clock pulses. The timing capacitor value has been selected as large as 220µF in the final design to eliminate any effects of switch bounce and to ensure proper and clean transitions.

This design demonstrates the use of analog timing circuits and digital logic circuits and how they interact with each other.

1.1 555 Timer Operation in the Digital Dice Circuit

In this configuration, the 555 IC will function as a controlled timing pulse generator that will provide clock pulses to the CD4017 decade counter. Unlike the previous energy burst monostable configuration implemented in the photopopper circuit, in this configuration, the 555 IC will generate well-defined trigger pulses when the push button is pressed.

The 555 IC will charge and discharge the timing capacitor connected to it through an RC network. The voltage at the timing capacitor will always be monitored by the internal comparators. The output will change when the capacitor voltage reaches the 2/3 Vcc threshold. The clean and crisp transition produced by this configuration will generate a pulse that will function well with CMOS logic. **[3]**

For the final configuration, a large timing capacitor of 220 μF will be connected to the 555 IC. The large capacitor will slow down the voltage transition and prevent any unwanted switching caused by mechanical switch bounce.

As mentioned above, the pulse generated by the 555 IC will function as the clock pulse that will advance the state of the dice by one step. Therefore, the 555 IC will function as the analog timing interface between the mechanical switch and the digital counter logic.

2 Principle of Operation of the Digital Dice (Explanation of Operation)

The digital dice works on the principle of clock pulses. Instead of using an energy storage device, this circuit relies on a stable clock pulse generated by a 555 timer IC connected in astable mode. The clock pulses are then used to drive a CD4017 decade counter IC. The IC has 10 outputs. The outputs are connected to light up one output at a time. The logic circuit connected to the outputs of the IC uses diodes to light up LEDs connected to them. The LEDs are connected to display dice points ranging from 1 to 6. **[2]**

When you press the push-button switch connected to pin 4 of the IC, it starts sending clock pulses. The IC then starts to count rapidly. The outputs are connected to light up LEDs to create a rolling effect. When you press the switch again, it stops counting. The output remains steady.

The CD4017 IC has been connected to work as a MOD-6 counter. The output at pin 6 has been connected to pin 10 to restrict it to six states. The IC then has six states corresponding to dice points ranging from 1 to 6. There are four phases involved in this digital circuit:

1. Clock generation: The clock pulses are generated by an RC circuit connected to a 555 IC.
2. Sequential counting: The IC counts rapidly by sending pulses to the output pin.
3. LED decoding: The output pin is connected to a logic circuit using diodes to light up LEDs.
4. Hold state: The IC stops counting when you press the switch.

2.1 Justification for Choice of Circuit

The project design chose a digital dice circuit because it was simple, reliable, and well-suited for teaching the basics of digital electronics in a compact form. The 555 timer, running in astable mode, will give a steady clock pulse with a variable frequency, which you can control by choosing simple values for an RC circuit, avoiding a complex oscillator circuit. It's also a very popular, rugged, cheap, and well-understood part, making it a great choice for simulation and actual implementation.

The CD4017 decade counter was also a natural choice because it includes a set of decoded outputs. You don't have to worry about binary counting and then having to decode the result with extra logic; with a 4017, you have a set of sequential high outputs (Q0-Q9). By connecting Q6 to the reset pin, you make a MOD-6 counter, which is exactly what you need for a die with six faces. **[6]**

The diode network will be used for a combination logic circuit that will control which LEDs will be on at any time. This will involve multiple outputs from the counter, but you won't need extra logic chips because a diode network will do the trick. This will also be an OR circuit, which will keep things simple while still allowing you to keep the digital circuit properties.

The current-limiting resistors will be useful for keeping the LEDs running at a safe current, which will keep them running reliably and also keep the CMOS outputs loaded properly.

So, we have a design that includes:

1. An analog RC circuit for timing purposes
2. CMOS logic for a Johnson decade counter
3. Combinational logic with a diode network
4. LEDs and interfacing

This circuit will meet the requirements for a "circuit of your choosing" while still being simple, easy to make, and suitable for theoretical and experimental exploration.

3 System-Level Design Overview and Evidence of Operation

The digital dice circuit has five primary subsystems, which work in unison to perform the functions of clock generation, sequential counting, and visual output decoding as follows:

1. Power Supply and Regulation
2. Clock Generation (555 Timer Stage)
3. Sequential Counting (CD4017 Decade Counter)
4. Output Decoding and LED Mappings (Diode Logic Network)
5. User Control Interface (Push Button Input)

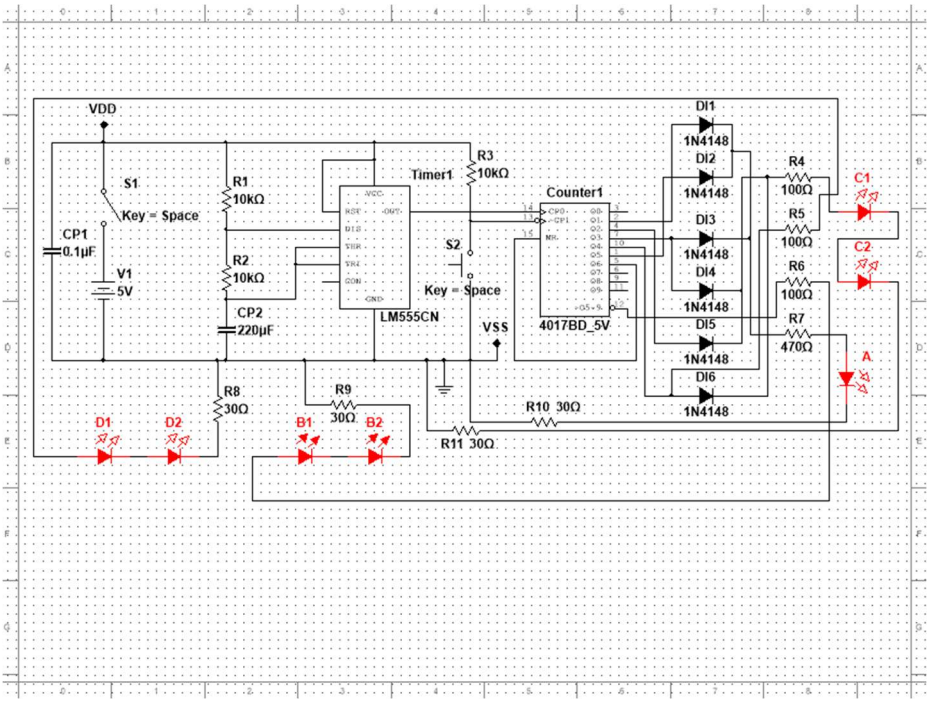

Figure 3.1 MULTISIM Circuit Schematic

3.1 PCB Layout

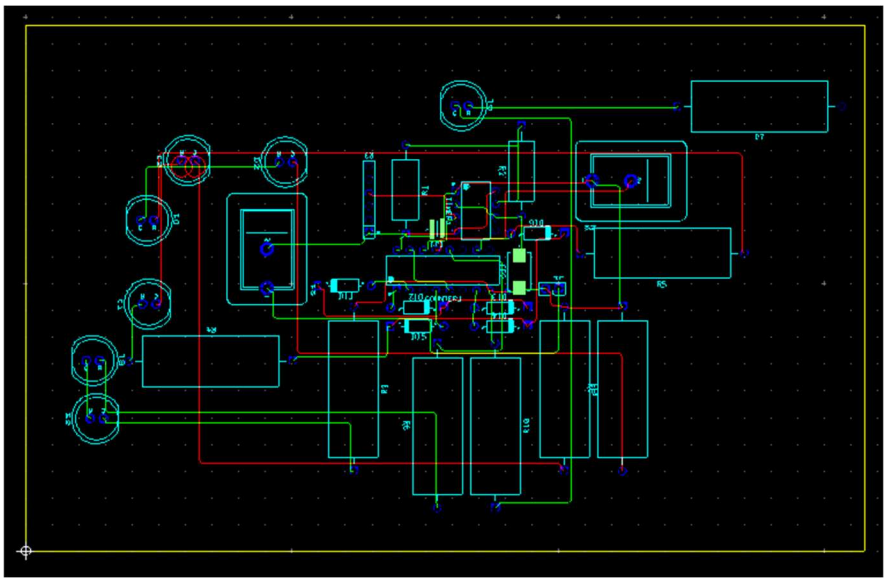

Figure 3.1.1 Final 2D PCB layout of the digital dice circuit generated in Ultiboard, showing component placement, copper routing (both layers), and board outline prior to manufacturing export.

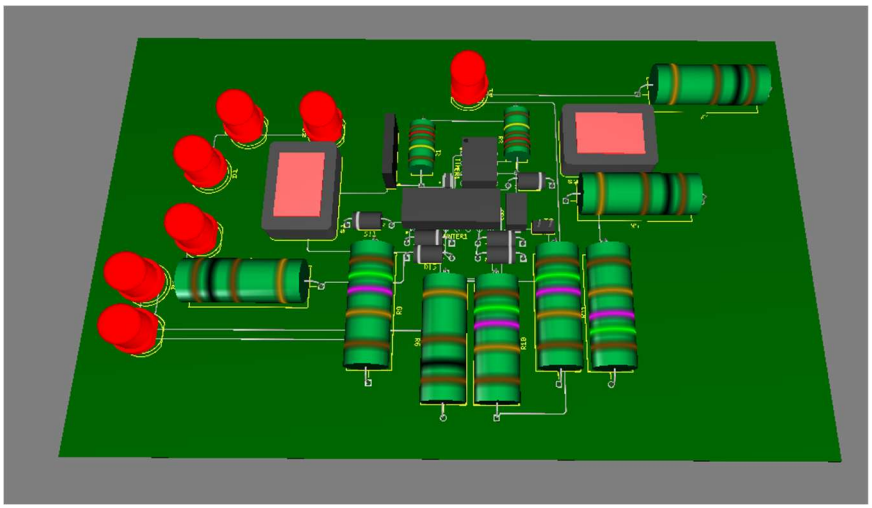

Figure 3.1.2 3D rendered view of the completed PCB design illustrating component placement, through-hole packaging (DIP ICs, resistors, LEDs), and overall mechanical arrangement before fabrication. (with HDR1X2 for Vcc and GND)

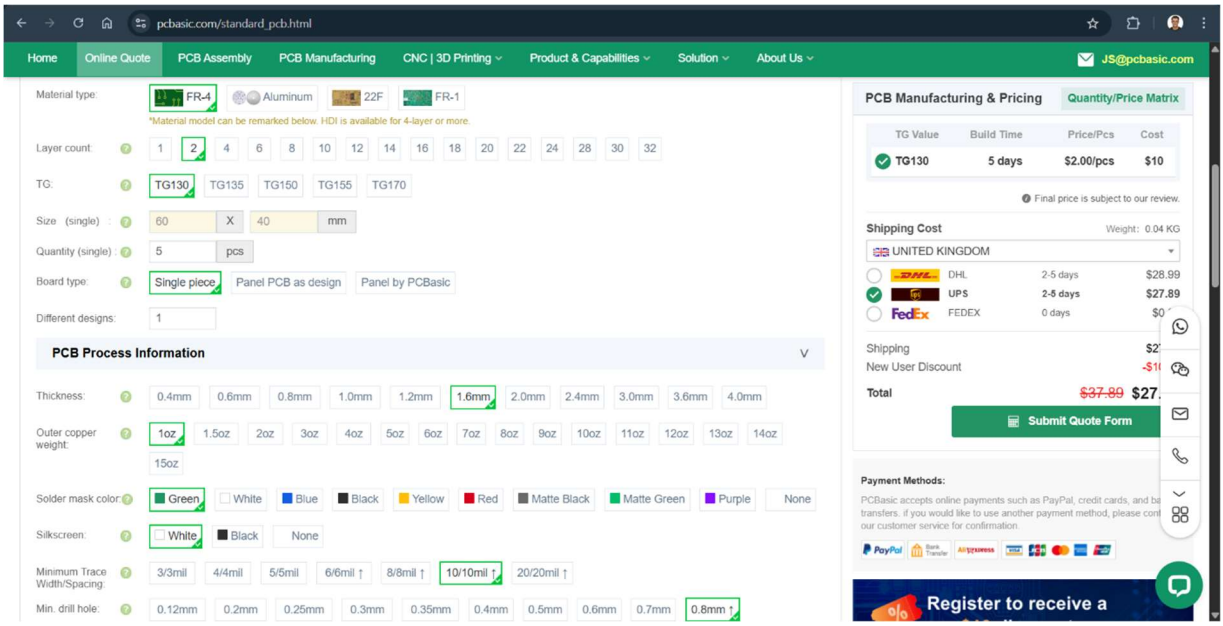

Figure 3.1.3 For the manufacturing configuration and cost estimation of the PCB, the PCBasic online quotation tool was used. In the context of the digital dice circuit, a standard FR4 substrate with 2-layers, 1.6mm board thickness, and 1 oz copper weight has been selected. These values represent standard specifications for digital logic circuits, which ensure the mechanical robustness of the board as well as the reliability of the routing. Additionally, a minimum trace width and spacing of 10/10 mil were selected, which ensures the manufacturability of the board, providing margins beyond the actual requirements of the traces, since wider traces are used in the actual implementation. The quotation results validate the practical feasibility of the proposed design, confirming that it can be manufactured using standard manufacturing processes, which are cost-effective. The selected configuration ensures optimal performance, robustness, and cost-effectiveness. **[8]**

3.2 Bill of Materials

Updated Bill of Materials - Digital Dice Circuit

Item No.	Component Description	Specification / Value	Qty	Unit Cost (£)	Total Cost (£)
1	Timer IC	LM555CN (DIP-8)	1	£0.60	£0.60
2	Decade Counter IC	CD4017BD (CMOS, 5V)	1	£0.80	£0.80
3	Timing Resistors	10 kΩ	3	£0.05	£0.15
4	Timing Capacitor (CP2)	220 µF Electrolytic	1	£0.80	£0.80
5	Control Capacitor (CP1)	0.1 µF Ceramic	1	£0.10	£0.10
6	Logic Isolation Diodes	1N4148	6	£0.10	£0.60
7	LED Current Resistors	100 Ω	3	£0.05	£0.15
8	LED Current Resistor	470 Ω	1	£0.05	£0.05
9	LED Series Resistors	30 Ω	4	£0.05	£0.20
10	Indicator LEDs	Red 5mm	7	£0.15	£1.05
11	Push Button Switches	SPST (Momentary)	2	£2.20	£4.40
12	Power Supply	5V DC Source	1	–	–
13	PCB / Prototyping Board	Single sided PCB	1	£2.00	£2.00
			Approximate Total Cost (excluding PSU):		£10.90

Figure 3.2.1 BoM Table by Amazon UK **[7]**

The Bill of Materials for the Digital Dice circuit includes conventional and inexpensive components to ensure reliable operation under 5V CMOS. The timing circuit is provided by an LM555CN timer, which operates in astable mode to generate clock pulses. The RC timing circuit comprises three 10kΩ resistors and a 220µF electrolytic capacitor, used to set the rolling speed, with an additional 0.1µF capacitor for stability and noise immunity. A CD4017BD decade counter is used to generate sequential logic (Q0 to Q5), implementing a Mod-6 counter suitable for use with the dice circuit. A diode logic matrix is implemented using six 1N4148 diodes to logically combine the counter outputs to drive the LEDs correctly. The LED display circuit comprises seven 5mm diameter red LEDs, with 100Ω, 470Ω, and 30Ω used as the current-limiting resistors to ensure the LEDs are brightly illuminated. The roll and reset circuit uses two SPST momentary push-button switches. **[7]**

Item	Component	Specification / Manufacturer	Farnell Order Co	Qty Require	MOQ
1	Timer IC	Texas Instruments LM555CN (DIP-8)	3121177	1	1
2	Decade Counter IC	Texas Instruments CD4017BE (DIP-16)	3006265	1	1
3	Timing Capacitor	Panasonic EEU-FR1E221 – 220µF 25V Radial	2217563	1	1
4	Control Capacitor	Vishay 0.1µF 50V Ceramic Radial	1759013	1	1
5	Timing Resistors (10kΩ)	Yageo CFR-25JR-52-10K 0.25W	4063928	3	10
6	Logic Diodes (1N4148)	Diotec 1N4148 DO-35	4555436	6	5
7	LED Current Resistors (220Ω)	Yageo CFR-25JR-52-220R	4063873	3	10
8	LED Current Resistor (470Ω)	Yageo CFR-25JR-52-470R	4063885	1	10
9	LED Series Resistors (30Ω)	Yageo CFR-25JR-52-30R	4063844	4	10
10	Indicator LEDs (5mm Red)	Multicomp Pro 703-0100	2112111	7	5
11	Push Button Switches	SPST Momentary Through-Hole	2448617	2	1
12	Power Connector	2-Pin Terminal Block 3.81mm	2828340	1	1

Figure 3.2.2 BoM Table by Farnell UK **[9]**

3.3 Real-Time Breadboard Demonstration

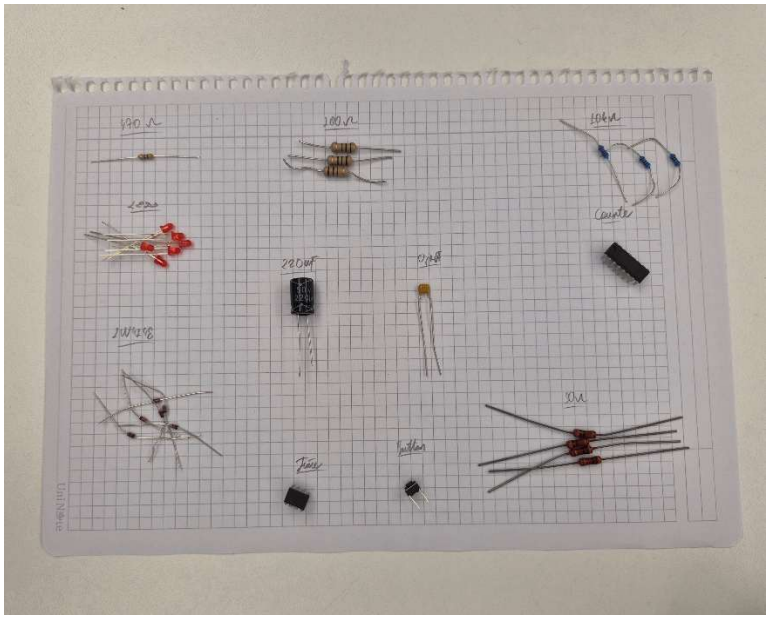

Figure 3.3.1 Component List for Digital Dice Circuit Demonstration (28 pieces)

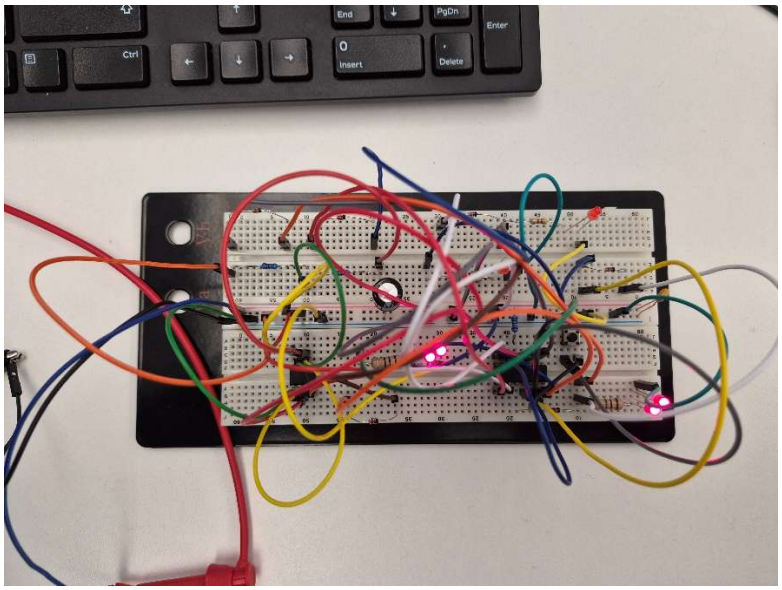

Figure 3.3.2 Real-Time Breadboard Demonstration (I fed the circuit with 5V, 3A by voltage generator)

4. Power Source Modelling

4.1 Supply Representation

Unlike the original reference photopopper, which utilizes a BP2433 solar panel as a low current energy source, the Digital Dice circuit implemented here is designed to utilize a regulated 5V DC supply in both simulation and intended laboratory implementation. In Multisim simulation, the power supply is an ideal DC voltage source of 5V that is connected directly to the LM555CN timer and the CD4017BD CMOS decade counter.

Since the circuit will not utilize energy harvesting as its power source, there is no requirement to include resistance in series with the DC supply voltage source to limit the maximum current from the source. The main requirement is to ensure that the DC supply voltage is within the recommended operating range of the CMOS switches and LEDs, which is between 3V and 15V for the CD4017BD and between 4.5V and 15V for the LM555CN.

To ensure maximum stability and prevent possible noise in the switches, a decoupling capacitor of 0.1μF is included in the circuit.

4.2 Available Power Estimation

With a tightly controlled 5V supply, the maximum limit of the power available in theory is determined by the load, not what the supply is able to drive out. The principal power consumption is due to:

- The current in the LEDs,
- The switching of the 555 timer,
- The outputs of the CMOS counter.

If each of the LEDs has an operating current of 10 to 15mA at 5V, then the instantaneous power available to an active LED is:

$$P\_LED \approx V \times I = 5V \times 0.01A = 50mW$$

5. Timing and Pulse Control Subsystem

In contrast to the operation of the photopopper circuit discussed in Assignment 1, the operation of the Digital Dice circuit does not rely on the principle of energy storage or the phenomenon of burst discharge. The operation of the system is governed by the timing and pulse generation capability through the use of the RC network connected to the LM555 working as an astable timer.

5.1 Timing Capacitor Selection

In this design, the primary timing capacitor is:

$$C_{p2} = 220\ \mu\text{F}$$

A fairly large capacitor has been used intentionally to accomplish the following: reduce the oscillation frequency of the 555-timer, produce the rolling effect for the LEDs, reduce switch bounce, and maintain the transient behavior in MULTISIM stable. This large capacitor reduces the likelihood of premature switching of the 555-timer, which might be caused by the bounce in the push-button switch, as it reduces the rate of charging and discharging the internal node of the 555-timer. An additional decoupling is used for supply stability and noise suppression near the timer IC:

$$C_{p1} = 0.1\ \mu\text{F}$$

5.2 Clock Frequency Estimation

The 555 timer, in astable configuration, will produce a clock frequency given by with Ra=10kΩ, Rb=10kΩ, C=220μF:

$$f = \frac{1.44}{(Ra + 2Rb)C} \approx 0.22\text{Hz}$$

This will produce a period of approximately: T ≈ 4.5s

This gentle, slow oscillation will ensure that the dice face remains in view long enough to see, record, and demonstrate it in simulation and in the real world.

5.3 RC Time Constant Behaviour

The dominant RC time constant is:

$$\tau = R \cdot C$$

$$\tau = 10 \times 10\text{^}3 \times 220 \times 10\text{^}\text{-}6 = 2.2 \text{ s}$$

In a nutshell, charging in RC circuits is slow and is done exponentially. Once we reach one time constant (1τ), the capacitor is at 63% of its final voltage value. Once we reach five-time constants (5τ), the capacitor is almost fully charged, about 99%. This slow charging allows us to have smooth and clean transitions between two digital states and prevents us from having unwanted multiple increments due to a single button press.

5.4 Duty Cycle Analysis

$$D = \frac{(R1 + R2)}{(Ra + 2R2)} \approx 66.7\%$$

This means that the output remains HIGH for approximately two-thirds of the cycle and LOW for one-third. Since the CD4017 advances on the rising clock edge, the exact duty ratio does not critically affect counting accuracy.

5.5 Step Rate and Dice Behaviour

$$\text{Step Rate} = f = 0.22 \text{ steps/sec}$$

Since the CD4017 counts on the rising edge of the clock signal, the sequence of the dice will count once per clock pulse. The entire count cycle takes about 27 seconds, with each number visible for a few seconds. This makes the circuit useful for observing it in a lab and for oscilloscope use. The speed was reduced because the initial simulations showed that using smaller capacitors would cause the transitions to be so fast that they would be difficult to see.

6. Sequential Counting Subsystem

The sequential state generation in the Digital Dice circuit is achieved by using the CD4017 decade counter IC. The CD4017 is a CMOS Johnson counter that provides 10 decoded outputs Q0 to Q9. Only one output is HIGH at any given time. **[4]**

6.1 Basic Operating Principle

The counter increases its active output on every rising edge of the clock signal applied to the CP0 input. Internally, a logic HIGH propagates through a 10-stage register chain, where each register is decoded directly onto an output pin. Essentially, it counts through a modulo 10 sequence by default. Its behavior can be summarized as:

- On power-up → Q0 = HIGH
- First clock pulse → Q1 = HIGH
- Second clock pulse → Q2 = HIGH
- …
- After Q9 → sequence returns to Q0

6.2 Mod-6 Configuration for Dice Operation

Since the actual dice only has six possible outcomes (1 through 6), the counter should actually be treated as a modulo 6 counter rather than the modulo 10 counter it currently is. Q6→MR (Reset input)

This can be done by wiring the counter such that when Q6 goes high, the counter resets instantly to Q0. This will result in exactly six distinct states, corresponding to the faces of the actual dice. The output sequence will therefore be: Q0→Q1→Q2→Q3→Q4→Q5→Q0

6.3 Clock Enable and Controlled Stepping

The CD4017 has a clock enable input (CP1 or CKE). If the clock enable input is HIGH, the pulses do not get through; when it's LOW, the pulses get through as normal. The 555 circuit here generates the clock pulses, and the button operates the enable/reset circuitry. The button only generates one pulse at a time, meaning the dice will move step by step rather than racing through the states.

6.4 Output Characteristics

The CD4017 outputs are:

- CMOS level
- Rail-to-rail (0 V to VDD)
- Capable of directly driving logic networks

As a result of this diode-mapped structure for the dice LEDs, current-limiting resistors are provided to prevent any output from being over-driven. Each output is held HIGH for a single clock cycle. The LED mapping network then converts that single output to the correct visual representation of a dice.

6.5 State Sequence Interpretation for Dice Faces

Each output state corresponds to one dice number:

- Q0 → Dice face 2
- Q1 → Dice face 3
- Q2 → Dice face 4
- Q3 → Dice face 5
- Q4 → Dice face 6
- Q5 → Dice face 1

This ordering was selected to simplify diode routing and reduce component count, as described in the logic mapping section.

4017 counter outputs high	Dice no.	LEDs ● = LED on			
		A	B1/2	C1/2	D1/2
Q0 and ÷10	2		● ●		
Q1 and ÷10	3	●	● ●		
Q2 and ÷10	4		● ●	● ●	
Q3 and ÷10	5	●	● ●	● ●	
Q4 and ÷10	6		● ●	● ●	● ●
Q5	1	●			

Figure 6.5.1 State Sequence Logic Table for Dice Faces

7. Diode Logic Mapping Network Analysis

The Digital Dice circuit has the requirement of converting a single active counter output into a combination of LED lights in order to mimic the visual output of a physical dice. Since the output of the CD4017 is HIGH individually, a logic mapping network is required in order to map the required output combinations. This is done by using a diode logic network.

7.1 Diode OR Configuration and Advantages

Each group of LEDs is connected to several counter output lines through individual signal diodes (1N4148). This configuration implements a wired OR logic using the diodes. If one of the counter output lines is HIGH, the current flows through the associated diode and activates the respective group of LEDs. In other words, the point at which the LEDs are activated is like a node where the V_{Qi} (active counter output) is the input, and the V_D is approximately 0.7V because it is a silicon diode. Since only one output from the Q counter is high at a given time, there is no output contention. **[5]**

$$V_{\text{LED}} = \max(V_{Qi} - V_D)$$

Compared to other alternatives, such as microcontrollers or combinational logic ICs, this implementation has the advantages of not requiring programming, illustrating the fundamental concepts of digital logic, being composed of discrete parts, and being rugged and easy to simulate.

7.2 Current Limiting and Load Protection

The series resistors for each LED branch are selected to be 100 ohms, 470 ohms, or 30 ohms depending upon the grouping of the LEDs. This establishes the equation where V_F is equal to the forward voltage of the LED and V_D is the forward drop of the diode, which is approximately 0.7 volts. This controls the current from the CMOS output stage:

$$I_{\text{LED}} = \frac{V_{DD} - V_D - V_F}{R}$$

8. Evidence of Operation and Observations

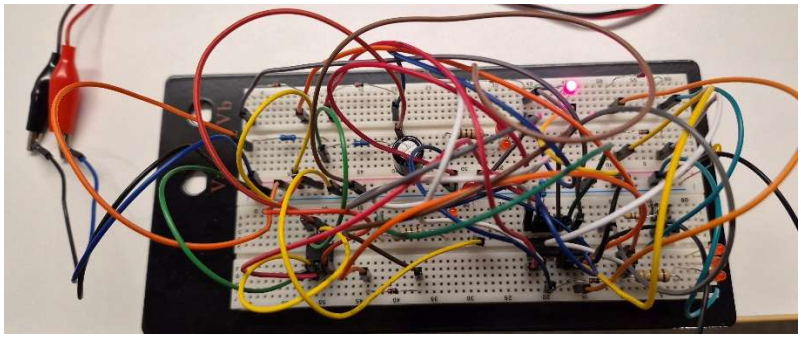

Figure 8.1 Dice Face 1 Demonstration Proof (1 LED)

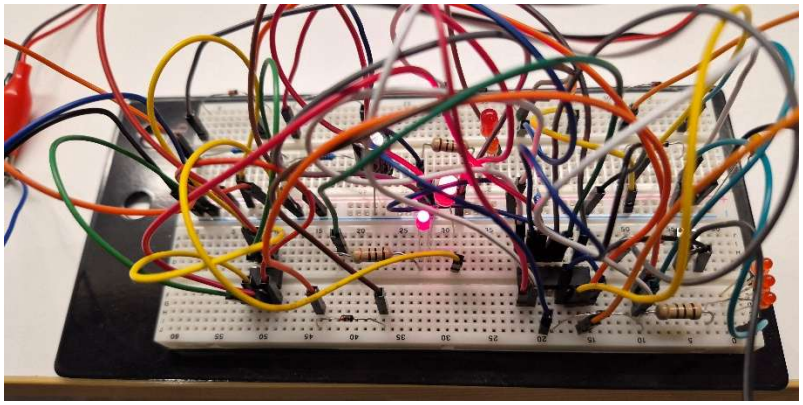

Figure 8.2 Dice Face 2 Demonstration Proof (2 LEDs)

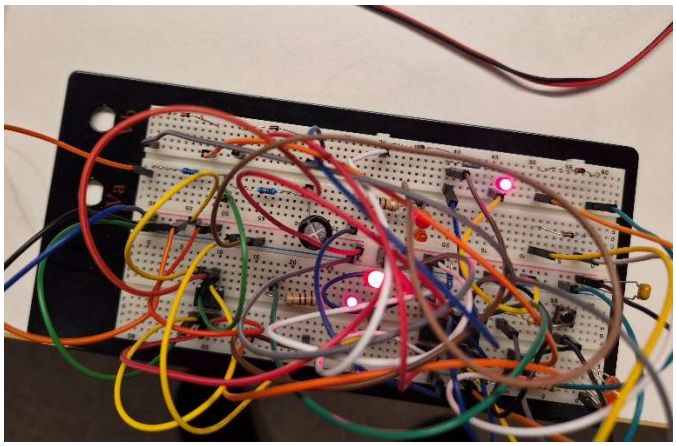

Figure 8.3 Dice Face 3 Demonstration Proof (3 LEDs)

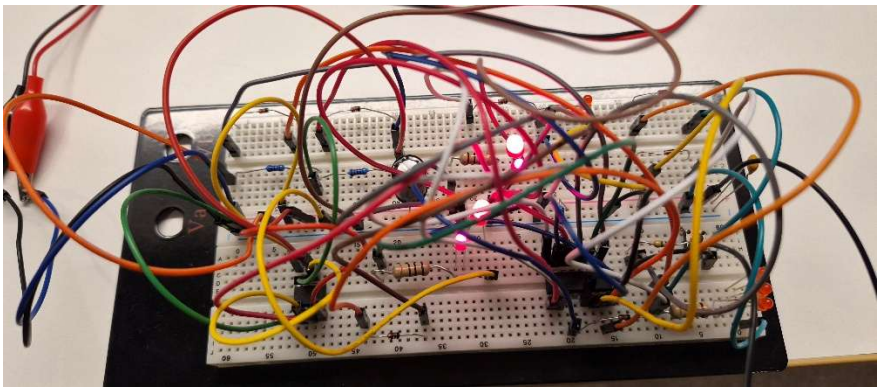

Figure 8.4 Dice Face 4 Demonstration Proof (4 LEDs)

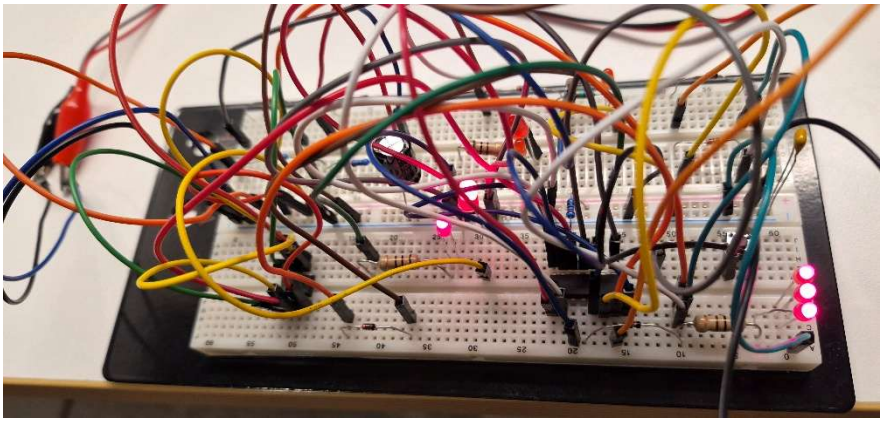

Figure 8.5 Dice Face 5 Demonstration Proof (5 LEDs)

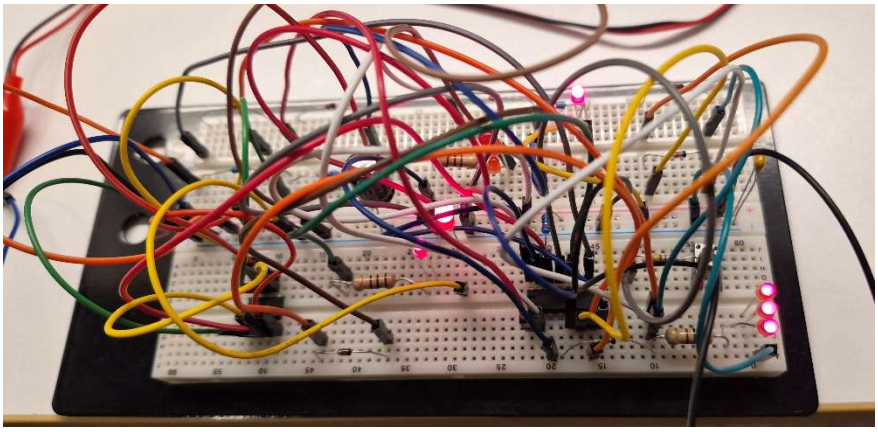

Figure 8.6 Dice Face 6 Demonstration Proof (6 LEDs)

9. Simulation and Measurement Setup

9.1 Logic Analyzer and Oscilloscope Configuration

The digital oscilloscope was employed within MULTISIM to verify the correctness of the clock signal generated by the LM555 timer. The probe is taped directly to the timer output pin, pin 3. The oscilloscope is set as follows:

- Time base: 50 ms/div
- Voltage scale: 5 V/div
- Coupling: DC

Nine horizontal divisions of the oscilloscope screen display a full cycle of the waveform, allowing precise verification of the amplitude and timing of the clock signal as it drives the CD4017 counter.

9.2 Observed Outputs

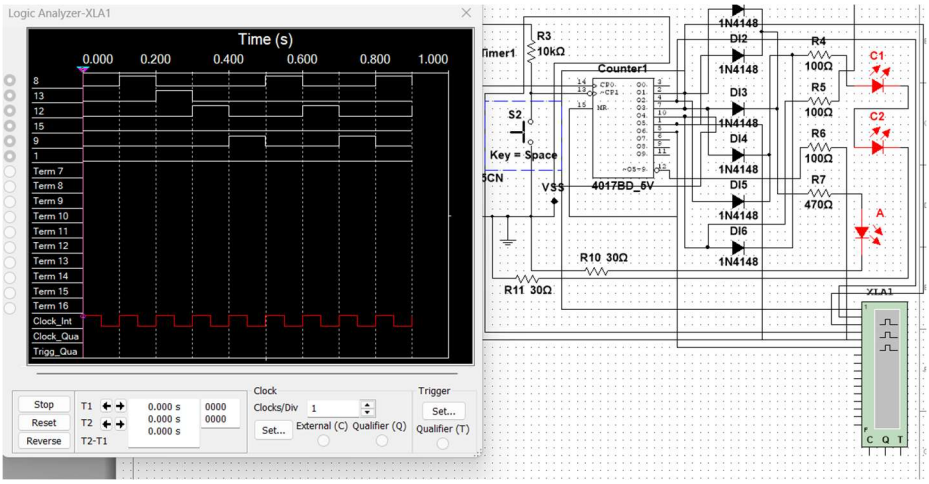

Figure 9.2.1 Sequential logic analyzer capture showing Q0-Q5 outputs transitioning in mod-6 sequence, confirming correct dice state progression. The logic analyzer verifies a correct sequence of one-hot values for the CD4017 output lines. The sequence advances with each rising clock edge, wrapping back to Q5 to confirm the correctness of the mod-6 dice operation.

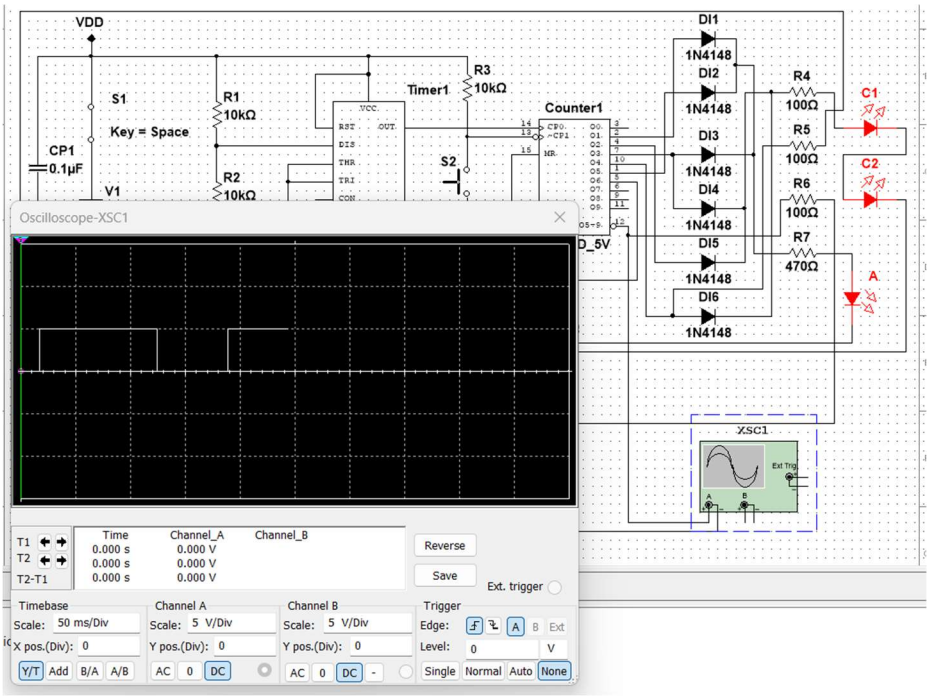

Figure 9.2.2 The scope is set to 50 ms/division, showing nine divisions horizontally. The trace indicates that one clock cycle is 4.5 seconds, which is consistent with the calculated frequency of about 0.22 Hz. This consistency confirms that the astable timing network is correct and that the clock for the dice sequence is being generated properly.

10. Conclusion and Critical Discussion

The design, simulation, and verification of the Digital Dice circuit were all successful, using a combination of analog timing and CMOS logic. The LM555 IC, when put into astable mode, provided a stable clock signal, which was then fed into the CD4017 decade counter, designed to operate as a mod 6 state machine. The logic analyzer and oscilloscope results verified the proper operation of the state machine, matching the theoretical calculations. The period of 4.5 seconds also agreed with the theoretical frequency, derived from the astable configuration equations.

Several technical issues arose during the development of the project. One of the major issues was obtaining stable and observable transitions without excessive switching speed. Lower capacitance settings for the timing capacitor made it difficult to observe the state transitions on the logic analyzer and oscilloscope, as the state transitions were very fast. By increasing the capacitance of the timing capacitor to 220 µF, the state transitions were more easily observable, but this also led to longer state transitions. Another important aspect was properly setting up the reset signal between Q6 and MR, as this could easily lead to incorrect mod 6 counting behavior if the wiring or IC pins were incorrectly interpreted on the CD4017 IC.

Another factor to be considered is the diode logic mapping network used to create the dice LED display. Although the use of an OR circuit with diodes offered a simple and educationally effective solution, the relatively high number of diodes used introduced complexity and voltage drop variability. While in a real-world application, forward voltage drop differences among diodes could affect LED brightness uniformity, in a simulation environment, the circuit is functionally correct. Although a more optimized solution would minimize component count and maximize electrical robustness, the selected architecture is effective in illustrating the interrelationship between analog timing, sequential logic, and combinational logic in a clear and effective manner.

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