





On the Impact of Asynchronous I/O on the Cube re-mapper at HPC Scale

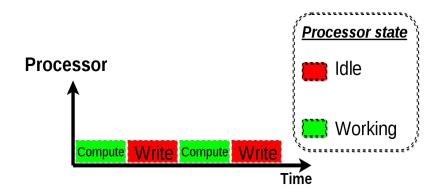
Presented by Riyane SID LAKHDAR, Supervised by Dr. Pavel SAVIANKOU







#### Motivation: avoid idle write time

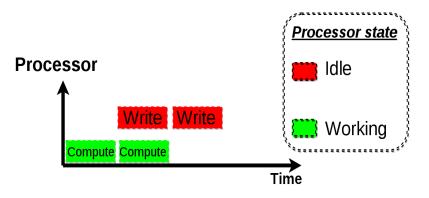








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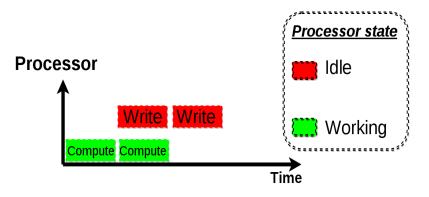








#### Motivation: avoid idle write time



## Target software optimization

The Cube re-mapper







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Basis of the custom solution The POSIX-based asynchronous I/O

Modelling the solution's gain

Improving the *Cube re-mapper*Basic asynchronous implementation

Custom enhancements

Conclusion and future work







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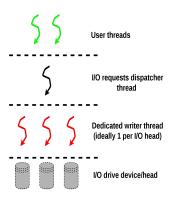
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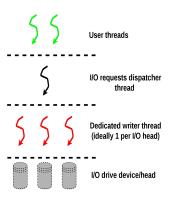
# Asynchronous I/O library (AIO.h)

- POSIX standard library
- Distributed on most UNIX OS: GNU-Linux, MacOsX
- Emulated for windows









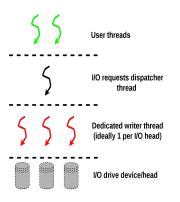
#### Limitations of the AIO.h

- Memory footprint might explode ⇒ RAM swap
- Possible contention on I/O device









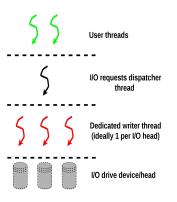
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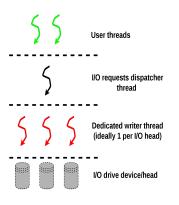
### Why this choice?

- Minimize the engineering effort
- Tuned to fit
  - I/O access pattern
  - Hardware specification









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- Minimize the engineering effort
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# The *Cube re-mapper*

```
void mainCubeRemapper
{
    Cube * inCube = new Cube(input);
    for (int i=0; i<nbMetric;++i)</pre>
         File* result = openFile("w");
         compute(inCube, i, &bufer);
         write(buffer, result);
```







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    wait_asynchronous_write();
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```
void mainCubeRemapper
                           The asynchronous choice
    Cube * inCube = new ( Reduce processor stall
    for (int i=0; i<nbMe
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void mainCubeRemapper
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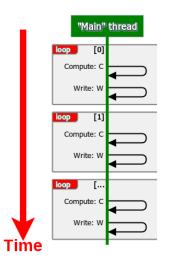
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### **Current synchronous model**



### Synchronous I/O model

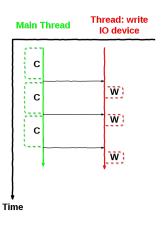
- Current version of the Cube re-mapper
- Benchmark for the study
- $T_{synchronous} = n*(C+W)$







## Simplified asynchronous I/O model



## Asynchronous I/O model

#### Assumptions:

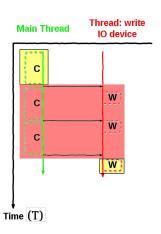
- Constant writing time W of each buffer
- Constant computation time C

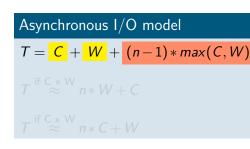






## Simplified asynchronous I/O model



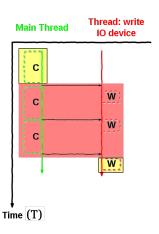


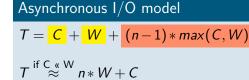






## Simplified asynchronous I/O model





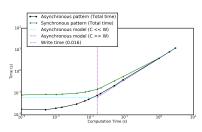
 $T \stackrel{\mathsf{if C}}{\approx} N \times C + W$ 



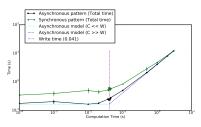




## Simplified model assessment



(a) Intel Core CPU i7-6700 (Workstation)



(b) Intel Xeon CPU E52680v3 (HPC JURECA)

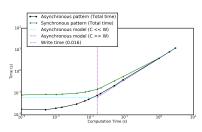
- Experimental improvement brought by asynchronous I/O
- Maximum improvement for  $C \sim W$



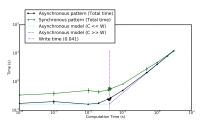




### Simplified model assessment



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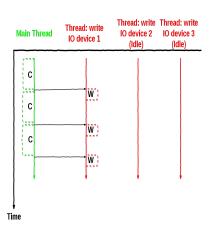
- Experimental improvement brought by asynchronous I/O
- Maximum improvement for  $C \sim W$
- Potential inaccuracy ⇒ model 2 (cf report)







### Multiple I/O devices: case C >> W



#### Theoretical model

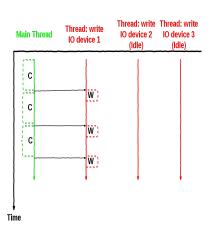
- $T(N_{io}) \stackrel{\text{if C} \gg W}{\approx} n * C + W$
- Useless additional I/C







## Multiple I/O devices: case C >> W



#### Theoretical model

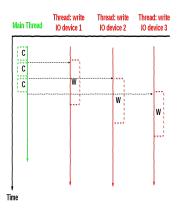
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## Multiple I/O devices: case C << W



### Theoretical model

$$T(N_{io}) \stackrel{\text{if } C \ll W}{pprox} C + W + (n-1) * max(\frac{W}{N_{io}}, C)$$

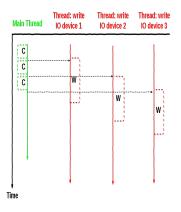
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### Multiple I/O devices: case C << W



#### Real-life execution

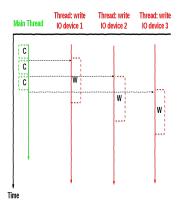
- Relevant additional I/O
- Complicated implementation







## Multiple I/O devices: case C << W



#### Real-life execution

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### **Experimental set-up**

Evaluation of custom implementations of *Cube re-mapper* using:

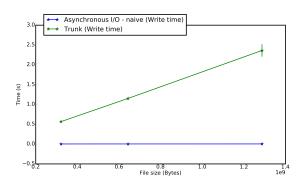
- Real-life input file (NAS parallel benchmark):
  - 65535 threads, 0.38 GiB
  - · 131071 threads, 0.62 GiB
  - · 262143 threads, 1.28 GiB
- Real metrics (ex: CPU time, MPI communication) from HPC execution
- Realistic ratio  $\frac{C}{W} \equiv 2$







# Basic asynchronous I/O implementation



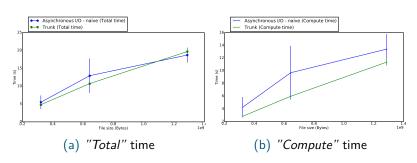
- Significant improvement in the "write" time
- Are we done?







# Basic asynchronous I/O implementation



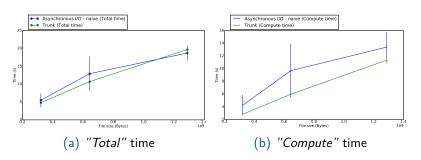
- Performance loss (due to "Compute")
- Uncertainty increase (due to "Compute"







# Basic asynchronous I/O implementation



- Performance loss (due to "Compute")
- Uncertainty increase (due to "Compute")







## Thread-scheduling issue

Threads belong to the same process  $\Rightarrow$ 

- scheduled mostly on same CPU core (for cache proximity)
- Delay the "compute" thread execution

**Solution:** to pin threads on different CPU-cores







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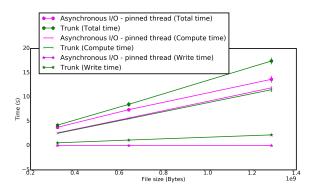
Solution: to pin threads on different CPU-cores







# Thread scheduling solution: pin threads



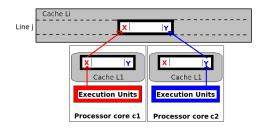
- Lighten interference with "Compute" thread
- Reduce "Compute" time







## False-sharing issue



### Consequence

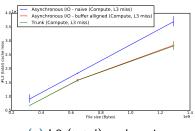
- Back and forth invalidation at each address access
- High occurrence frequency ⇒ significant impact

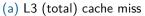


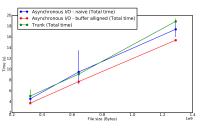




## Lighten the impact of false-sharing







(b) Cube re-mapper "Total" time

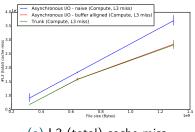
- Align buffer address to cache line
- Reduce cache-miss rate

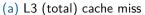


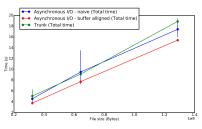




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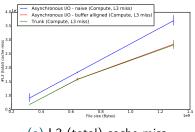
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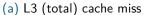


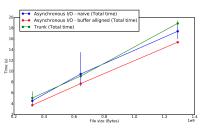




## Lighten the impact of false-sharing







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# Improve dynamic memory allocation usage

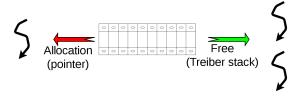


Figure: Free dynamic memory pool

## Custom memory allocator

- User-level managed heap
- Independent "allocation" (Compute) and "free" (Write)
- Reduced contention on "Free" pool ("Treiber" stack)







## Improve dynamic memory allocation usage

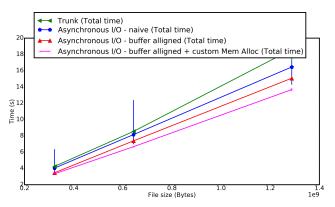


Figure: Cube re-mapper full-fledged assessment







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- Implemented prototype version (candidate for production) of the Cube re-mapper
  - Identified runtime perturbation created by AIC
  - Suggested and evaluated solutions







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#### **Future work**

#### Full parallelization of the pattern:

- Multiple concurrent "compute" threads
- Expected fit with our current solution:
  - Optimal data distribution/synchronization
  - Allows further scalability evaluation of current solution



# Thanks for your attention!