Comparison of Rectifier Circuits for Energy Harvesting Systems

Comparación de Circuitos Rectificadores para Sistemas de Energy Harvesting

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Abstract

Recent developments in the design of low-power circuits have allowed Energy Harvesting (EH) systems to be able to feed electronic circuits that execute complex processes, permitting that such systems play an important role in different application areas (e.g. Wireless Sensor Networks (WSN), biomedical devices, Internet of things (IoT), among others). Due to the low power output presented by these systems (in the range of μW to mW), the reduction of any potential losses presented in the circuits that form the EH system is a mayor issue, therefore a careful selection of the circuits and its components may improve the performance. In this work a comparison of various rectifier circuits found in the EH literature are presented. Some techniques that improve the performance of those circuits are also introduced. Finally, the simulation results of the considered circuits are presented with the aim to measure parameters, like the efficiency, and perform a quantitative comparison.

Keywords: Rectifiers, Energy harvesting, Power dissipation, AC-DC power converters.

Resumen

Los avances dados en los últimos años en el diseño de circuitos de bajo consumo de energía han permitido que los sistemas de Energy Harvesting (EH) tengan la capacidad de alimentar circuitos electrónicos que ejecuten procesos complejos, jugando así un papel fundamental en una gran variedad de aplicaciones, tales como Wireless Sensor Networks (WSN), dispositivos biomédicos, Internet of things (IoT), entre otras. Debido a que estos sistemas de EH generan potencias de salida en el rango de los mW es necesario reducir cualquier pérdida presente en los circuitos que

conforman el sistema, lo cual hace necesario una selección apropiada tanto de dichos circuitos como de los elementos que los conforman. En este trabajo se presenta una comparación de los circuitos rectificadores presentados en la literatura relacionada con EH, junto con algunas técnicas reportadas que brindan una mejora en el desempeño de estos circuitos. Finalmente, se presentan los resultados obtenidos de la simulación de algunos de los circuitos considerados con el fin de medir parámetros tales como la eficiencia y realizar una comparación cuantitativa de los circuitos presentados.

Palabras Clave: Rectificadores, Energy Harvesting, Disipación de potencia, AC-DC power converters.

Introduction

The advances presented in the development of electronic devices of low and very low power consumption have permitted the construction of smaller and more complex systems, owed to the relaxation of requirements related to the heat extraction or ventilation of the system. The creation, design and use of such systems have allowed the development of applications and techniques that only show a theoretical progress, for example IoT, development of Smart-Dust, implementation of WSN, among others. Each of these applications offer interesting benefits in different areas, e.g. materials engineering, bioengineering, medicine, communications, among others.

One application that has taken a lot of attention is the development of EH systems, because of the ability of such systems to provide its load (e.g. a WSN node) with the energy that it needs to operate during a certain period, through the extraction of the energy in the surrounding environment. This can enhance the autonomy of the entire system and reduces the expenses related to maintenance and battery changes [1].

Given the low power output presented by most EH systems, and the identification of the power requirements of a WSN as critical factors in the design and implementation of such networks [2],

the amount of power extracted by the EH system, and how much of this power reach the load, are of mayor importance for an adequate performance of the application system. This sets the two mayor problems to be solved in the implementation of a EH system: optimum extraction of the available energy present in the surrounding environment and low-loss processing of this power in order to presented it to the load.

Common electronic circuits that constitute the load of the EH system require a DC regulated voltage, which should be kept under a specific range in order to assure a correct load function. This dependence contrast with the fact that most of the transducers, used to convert the energy in the environment to an electrical form, produce an alternating power at their terminals. From this difference emerge the need of rectifier circuits, which led to obtain a DC component from an AC signal. This DC component can be processed to meet the power requirements presented by the load.

In this work different rectifier circuits reported in the EH literature will be presented. The operation of each circuit will be explained and its advantages and disadvantages will be discussed. This qualitative analysis will be presented in the section 2. In the section 3 different techniques with the potential to enhance the performance of rectifier circuits will be presented, such as Floating Gate Transistors (FGT), feedback techniques (Bootstrapping), among others. In section 4, the simulation results of the mayor rectifiers will be presented. Finally, in sections 5 and 6, a quantitative comparison based on the previously shown results will be realized and conclusions will be presented.

Problem statement

A common EH system has to present three basic functionalities: extraction of the power developed by the source, storage of some part of the energy generated and processing of the input power in order to meet the requirements imposed by the load. Because of the limited power

budget available in EH applications, each of the aforementioned functions must be realized as efficient as possible. This in order to assure that most of the generated power will be available to be used by the load of the EH system.

The mentioned power restriction plays an important role in the design of a functional EH system, due to the impossibility of using processing circuits available in the medium and high power range, where the allowed power losses may range between one to several tens of watts. This arise the need to develop new circuits able to operate as low as the μW range. In this work the power losses of different rectification circuits are studied. Which arises from the identification of the losses developed by these type of circuits as the most significant power losses inside a power processing circuit.

Rectifier circuits

As mentioned in the previous section, the commonly used electronic systems need specific voltage levels to guarantee a correct performance. Due to this requirement, the alternating power signal coming from the transducer must be transformed to the prescribed shape and values that the load requires. Such transformation requires a rectification stage, which produces a signal with a DC voltage level, which will be processed by a later stage to meet the voltage values required by the load.

The rectification stage should perform the transformation of the coming AC signal as efficient as possible. This in order to loss the minimum amount of power in the process that, in other way, would reach the load or a capacitor reservoir. The high efficiency requirement is of special interest in EH applications due to the low power available, therefore any unconstrained loss inside the power processing circuitry may severely impact the overall performance of the EH system and the load behavior. In the equations (1) and (2) two definitions of the power loss are presented.

(1)

(2)

Where is the power consumed by the rectifier circuit, is the circuit efficiency (output power over input power), is the input power and and are the power dissipated by the high and low side device inside the rectification circuit, respectively. Also, the triangular brackets represent the average value or DC value of the enclosed variable.

In the next sections various circuits reported in the EH literature will be presented. Some of the advantages and disadvantages of each circuit will be discussed through the modeling of the power loss developed by each rectifier

A. Diode bridge rectifier

The diode bridge rectifier is shown in the Fig 1. This is the most used rectification circuit in high and medium power applications, e.g. alimentation circuits connected to the electrical network, Uninterruptible Power Supply (UPS), etc. This circuit was widely used in EH applications due to its simple operation and implementation, for this reason it is denominated the standard circuit [3] and is used as a reference before which other circuits are compared.

Fig. 1. Diode bridge rectifier or standard circuit.

The operation of the circuit can be explained through the voltage values at the input and output ports and , respectively. When the input voltage is greater than , the diodes and are forward biased and provide a path that allows the current flow and connects the input and the output ports. The circuit operates in the same way when is greater than , but the forward biased diodes, that provide the current path, are and . When is smaller than no diode is forward biased, so there is no current flow and no energy exchange between the input and output ports.

A big disadvantage of this circuit is its low efficiency, which is due to the voltage presented by the diodes when a forward polarization is obtained. This voltage follows the exponential I-V

relation of the diode but, for simplicity, it is assumed as a constant value (so, is a constant). Taking into account that two diodes must conduct to obtain a current flux, and assuming that all diodes in the rectifier have an equal voltage drop, the power consumed by the rectification circuit can be calculated as shown in (3).

(3)

Where is the forward voltage drop on the diode and is the current that flows in it. Should be noted that the power consumption presented in (3) can be obtained by the calculation of the power consumed by the high and low side devices in (2). Commonly, the voltage drop of silicon devices lies around the 0.7 V. If lower voltage drop diodes are used (Schottky diodes) the efficiency is increased, however this is achieved at the expense of a higher implementation cost.

B. MOSFET bridge rectifier

An alternative to the diode bridge rectifier, commonly used in integrated circuits, is the circuit shown in the Fig. 2a, where the diodes of the rectifier circuit are replaced by diode-connected MOSFETs (DMOS). The DMOS are realized by short-circuiting the gate and the drain terminals of the transistor, thus maintaining the transistor in the saturation region of operation [3-5].

Fig. 2. Full-wave rectifier circuits: (a) MOSFET bridge rectifier, (b) Gate Cross-Coupled Rectifier (GCCR), (c) Negative Voltage Converter (NVC).

The operation of the MOSFET bridge rectifier is similar to the diode bridge rectifier, with the difference that the voltage developed by each conducting DMOS is as presented in (4). This leads to the power loss shown in (5).

(4)

(5)

Where is the voltage between the drain and source terminals, is the current through the transistor, is the process transconductance parameter, and are the width and length of the device

and is the threshold voltage. The equation (5) is obtained by the calculation of the power dissipation of each transistor under the assumption that all the transistors inside the rectifier have exact equal values of , , and . Note that at any conduction time, only one high side and one low side transistor are conducting, depending on the input voltage value. Therefore and only model the power loss of one transistor each, which explains the two factor in (5).

Although this circuit presents significant improvements, specially in the frequency response of the rectifier, which enables it to be used in radio-frequency applications, the rectifier still presents the efficiency related disadvantages shown by the diode bridge rectifier due to the developed voltage between the drain and source terminals of each device (higher than). Another problem presented by this rectifier emerge from the fact that the DMOS transistors operate in the saturation region of operation (), therefore each transistor is never fully on or fully off [6]. This is modeled with the first term of (4) and may increment the voltage on the transistors, thus reducing the efficiency of the circuit.

A solution presented in [4] and [5] proposes the use of active diodes, which are formed by a comparator controlled MOSFET, as shown in the Fig. 3a. The advantage presented by this circuit is the significant reduction of the voltage drop on the used transistors, increasing the overall efficiency of the rectifier. The main problem is the power consumption of the used comparators, given that this power has to be delivered by the EH system. Thereby the comparators act as a parallel load of the system and their power consumption may not justify their implementation [5]. Other parameter that should be considered during the design and implementation of these comparators is their slew-rate, due to the possible appearance of reverse currents (from the output to the input port) that surge because of switching delays when a low slew-rate is achieved [7].

Fig 3. (a) Active diode, (b) Low-drop Diode Equivalent (LDDE), (c) Active Gate Cross-Coupled Rectifier, (d) Bulk regulation transistors.

Another solution presented by Karthikeyan *et al.* [8] propose a circuit that emulates the behavior of a low voltage drop diode. This circuit is denominated *low-drop-diode equivalent* (LDDE) and is shown in the Fig. 3b, where a PMOS transistor is used. When a forward voltage is applied (the A terminal has a greater potential than the K terminal) the voltage of is positive, which generates a current flux through its collector terminal and turning-on the transistor . The commutation of charge the gate capacitance of and turns it on in the triode region of operation, thus providing a current path between A and K. Finally, an external circuit denominated *Current Reverse Sensing Circuit* (CRSC) activates the transistor when the input current reaches cero, thus turning off .

C. Gate Cross-Coupled Rectifier (GCCR)

A topology widely used in high-frequency inductive coupling devices is shown in the Fig. 2b. This circuit, named *Gate Cross-Coupled Rectifier* and proposed by Ghovanloo *et al.* [9], presents a great reduction of the voltage drop presented by the rectifier, due to the connection of the upper transistor gates directly to the input voltage. This sets a higher voltage at the gate terminals of the transistors [10], therefore reducing the voltage of the device. The reported efficiency of this circuit lies between 70-75% [11].

Considering the circuit operation for the positive interval of , when the input voltage is lesser than the voltage threshold of (i.e.), there is no current flow and the input and output port are isolated from each other. When the input voltage exceeds the output voltage (i.e.), the is turned on, thereby connecting the node to the output node. When the input voltage exceeds the output voltage by more than the threshold voltage of (i.e.), a current flow is established by the commutation of the DMOS transistor . The transistor prevents the establishment of a current flow when , because this current would flow from the output to the input port, degrading the

circuit efficiency. The circuit operation for negative voltage intervals is very similar to the described above, but the transistors and provide the path for current flow instead of and .

The voltage between the drain and the source terminals on the upper transistors is presented in (6) and the power loss of the rectifier is shown in (7).

(6)

(7)

Where is the input voltage and the subscripts and represents the parameter relation to the P or N type transistor. Should be noted that the first three terms inside the parenthesis correspond to the voltage developed by a high side transistor (PMOS transistor) and the third term is related to the voltage developed by a DMOS transistor (NMOS transistor).

The advantage presented by this circuit is the reduction of the voltage developed by the high side transistors due to the term inside the square root of (7). The great disadvantage of this circuit is that it still uses DMOS transistors, which has the aforementioned problems. The use of active diodes, mentioned in the previous section, may further improve the circuit performance [6] [12] [13]. This circuit is shown in Fig. 3c. Several alternatives to the use of active diodes are presented in [10] and [8], which propose a transistor arrangement that emulates the diode behavior. Another disadvantage of this circuit is the need for the input voltage to exceed the threshold voltage of the used transistors, which limits the employment of this circuit with very low voltage generators.

D. *Negative Voltage Converter*

An alternative derived from the GCCR, and proposed by Peters *et al.* [4], [14], is shown in the Fig. 2c. This circuit, denominated *Negative Voltage Converter* or *differential self cancellation rectifier* (DSVC) [15], allows to perform the rectification process with very low voltage drops in the current path. This is achieved by the use of a *full gate cross-coupled* topology.

The operation is very similar to the presented by the high side transistors (and) in the GCCR. Assuming all the threshold voltages are equal and for the positive interval of the input signal, when the input voltage is lesser than the voltage threshold () neither of the transistors is on, therefore there is no current flux towards the load. When the input voltage exceeds the threshold voltage of the transistors (), both and conduct, allowing the current flow. The circuit operation for negative intervals of the input voltage is very similar to the described above, but the transistors and provide the current path.

The voltage on the devices of the rectifier is the same of the high side transistors of the GCCR, which is shown in (6). This leads to an overall power loss as shown in (8) thanks to the replacement of the DMOS transistors in the GCCR topology.

(8)

It is of notice that the commutation of this circuit does not depend on the relation of the input and output voltages, as the other circuits presented, but only on the input voltage. Due to this characteristic and to the fact that the MOSFETs are bidirectional devices, currents from the output to the input port are developed when the voltage at the output port is higher than the magnitude of the input voltage. This may lead to a diminished rectifier efficiency if the input current is not controlled.

E. Bulk Regulation Transistors

The diodes formed in the transistors used in circuits like the GCCR or the MOSFET bridge rectifier, generated by the permanent connection of the bulk and the terminal with the lowest potential (for N-type transistors, for P-type transistors the bulk is connected to the terminal with the highest potential), allow the conduction of high inverse currents that flow from the output to the input of the rectifier. This currents, as the ones presented in the NVC circuit, may degrade the power obtained from the power source and the efficiency of the rectifier circuit.

A solution to this issue is presented in [16], where the use of two additional transistors is proposed to dynamically connect the substrate terminal (bulk) to the terminal with the highest or lowest potential, depending on the transistor type. The dynamic commutation avoids the generation of the diode and makes the transistor state only dependent on the gate terminal. This circuit is shown in the Fig. 3d. The used transistors can present a low relation due to the low current needed to perform the commutation.

In order to perform an early comparison between the presented rectifiers, a plot of the power losses presented by each rectifier with respect to the rectifier input current () is shown in Fig. 4a. It was assumed that the PMOS and NMOS transistors have equal , W, L and (i.e. , , and). The assumed values were: V, , V, mA/V^2 and, for the GCCR and the NVC, an input DC voltage (of the conducting transistors) of 0.6 V. In Fig. 4b, the plot of the NVC power losses with different DC input voltage values is presented.

Fig 4. Calculated power losses vs input current for: (a) diode bridge rectifier (1), MOSFET bridge rectifier (2), GCCR (3) and NVC (4), (b) NVC for V (1), V (2), V (3), V (4).

Enhancement techniques

As it was shown in the previous sections, the greatest disadvantage presented by the rectifier circuits, due to its impact on the efficiency of the circuit, is the voltage developed on the terminals of the commutation devices that form the rectifier. With the aim of improving the performance of these circuits, and due to the wide use of MOSFET devices for switching purposes, different techniques that allow the reduction of the threshold voltages have been developed. These techniques allow an increasing of the efficiency presented by the circuit and a reduction of the minimum voltage required to start the circuit operation. In this section some of these techniques, founded in the EH literature, will be presented.

A. *External Cancellation* (EVC)

This technique, proposed by Umeda *et al.* [17], uses additional and external circuits that produce a voltage with a magnitude proximate to the threshold voltage of the used devices, denominated . This with the aim of compensating the threshold voltage of the device and produce a near cero voltage at the terminals of the transistors. This may be developed by a reference circuit, commonly externally energized.

A great disadvantage of this circuit, reported in [18], is the use of external circuitry. This impacts not only on the rectifier power consumption but on the operation as well, which depends on the requirements imposed by the application and the environment where the circuit operates, leading to the impossibility to add additional circuitry.

B. *Internal Cancellation* (IVC)

With the aim of solving the problems presented by the EVC, the *internal cancellation* circuit was developed. This circuit was proposed by Nakamoto *et al.* [19] and is shown in Fig 5a. It uses a MOSFET together with an RC circuit to provide the required voltage to the switching transistor . This circuit is connected directly to the output voltage, so it is necessary to reduce their leakage currents, therefore high value resistances are commonly used.

Fig 5. (a) Internal Circuit (IVC), (b) Floating gate transistor in CMOS technology, (c) Bootstrapping circuit.

The output voltage of the IVC circuit is shown in (9), where the equivalent threshold voltage of the device correspond to the factor inside the parenthesis. This reduction obtained through the factor introduced by the threshold voltage of must be lesser, but close, than . This in order to avoid inverse currents.

(9)

Where is the input voltage, is the threshold voltage presented by the transistor and is the threshold voltage presented by the transistor.

This circuit presents important advantages in comparison to the EVC technique, because it allows tracking of the changes on the threshold voltage of the switching device without the use of external circuitry. One of the disadvantages presented by this circuit is due to the lack of stored energy at the start of the operation, which impose a certain settlement time in order to observe the aforementioned reduction of the threshold voltage. In addition, the need of highly pared transistors and large value resistors may increase the implementation cost of this circuit.

C. Floating gate transistors

The use of floating gate transistors to improve the performance of rectifier circuits was proposed in [20] and [21]. These transistors, regularly used as EPROM and EEPROM memories, base their operation on the incorporation of a floating gate, which, through the injection of electric charge, can change the threshold voltage of the arrangement. In the Fig. 5b is shown a functional diagram of the implementation of such transistor for CMOS technology. This circuit behaves as one unique transistor, where the control terminal acts as the gate terminal of a normal device.

This technique presents the advantage that it can be used with the majority of the rectifier circuits without the need to perform big changes in their basic structure. The main disadvantage is the need to programming the cell, which is carried out through *hot electron injection* or *Fowler-Nordheim tunneling* [22]. This programming and erasing process should be carried out only once, due to the low charge loss presented by the floating gate (0.1% in 10 years @100°C [20]).

D. Bootstrapping

The bootstrapping technique bases its operation on the commutation of capacitors, this in order to obtain the gate voltages that allow a reduction of the voltage drop presented on a switching device. This is achieved through charging of the capacitors, normally when the switching device is off, and connect them to the gate terminal of the switching transistor.

Hashemi *et al.* [23] propose the use of the commutation circuit presented in [5] with a GCCR topology, where the DMOS transistors were replaced by the circuit shown in the Fig. 5c. This circuit has a similar impact to the achieved by other techniques like the EVC or the IVC, because it aggregates a term to the output voltage equation similar to (9), which compensates the effect of the voltage developed on the terminals of the switching device. Additionally, a commutation circuit which makes use of a capacitor to provide the of the switching MOSFET was presented in [24]. This capacitor is directly charged by the rectifier input voltage, thus allowing greater voltage values driving the gates of the switching transistors.

This type of circuits present an easy implementation due to the low number of involved components, which impacts on the efficiency and the speed of the circuit. The parameters of these circuits, such as the size of the transistors and the capacitances involved, must be optimized accordingly to the requirements imposed by the input signal. This in order to avoid prohibitively long charging periods that may affect the starting and the operation of the circuit.

Experimentation

In order to compare the different rectifier topologies implemented in CMOS technology, through the computation of parameters such as efficiency, a computer simulation of the topologies shown in Fig. 2 was carried out. The simulated topologies are: the MOSFET bridge rectifier, the GCCR and the NVC. These simulations were made using the TSMC 0.18 μm process SPICE model, provided by [25], and the simulation package *LTspice IV*, from Linear Technology. Each circuit was simulated using transistors with a channel length μm, a channel width μm and μm, for P and N type MOSFETs, respectively, and a sinusoidal input voltage with a frequency of 10 Hz and amplitudes of 1 and 2 V. The operation of each circuit was probed using a pure resistive (KΩ) and a RC (KΩ, mF) load.

Results and discussion

The simulation results, in terms of the efficiency, input and output power, are shown in the Table 1. Additionally the output voltage obtained from the three simulated circuits is presented in Fig. 6 and Fig. 7, for an input voltage amplitude of 2 V and 1 V, respectively.

Circuit	V_{in}	Load	P_{in}	P_{out}	η
MOSFET bridge rectifier	2 V	R_L = 3 KΩ	315.89 µW	158.21 µW	0.50083
		R_L = 3 KΩ, C_L = 3.3mF	623.57 µW	306.01 µW	0.49074
	1 V	R_L = 3 KΩ	27.938 µW	5.5998 µW	0.20044
		R_L = 3 KΩ, C_L = 3.3mF	49.554 µW	8.0352 µW	0.16215
GCCR	2 V	R_L = 3 KΩ	479.56 µW	350.29 µW	0.73044
		R_L = 3 KΩ, C_L = 3.3mF	949.1 µW	692.77 µW	0.7299
	1 V	R_L = 3 KΩ	83.832 µW	44.31 µW	0.5285
		R_L = 3 KΩ, C_L = 3.3mF	166.83 µW	86.373 µW	0.5177
NVC	2 V	R_L = 3 KΩ	664.06 µW	662.54 µW	0.9977
		R_L = 3 KΩ, C_L = 3.3mF	34.601 mW	783.55 µW	0.024
	1 V	R_L = 3 KΩ	162.63 µW	160.96 µW	0.98973
		R_L = 3 KΩ, C_L = 3.3mF	1.9979 mW	239.51 µW	0.11988

Table 1. Circuit simulation results.

Fig. 5. Output voltages from the NVC (1), GCCR (2) and MOSFET bridge rectifier (3) for a 2 V input amplitude: (a) resistive load, (b) RC load.

Fig. 6. Output voltages from the NVC (1), GCCR (2) and MOSFET bridge rectifier (3) for a 1 V input amplitude: (a) resistive load, (b) RC load.

It should be pointed out the high efficiency displayed by the NVC rectifier, higher than 98% for the two input voltage values, when a pure resistive load is presented at its output. This efficiency is drastically reduced when a reactive element is added to the load, which is due to the inverse current generated from the output to the input port of the rectifier. This inverse current is produced because of the stored charge inside the output capacitor, which keeps the output voltage higher than the input voltage, and the MOSFET's bidirectional characteristic.

Unlike the NVC rectifier, the MOSFET bridge rectifier and the GCCR maintain a relatively constant efficiency for both considered loads (around the 50% for the MOSFET bridge rectifier and 70% for the GCCR when a 2 V input amplitude is applied). Additionally, both circuits present a high dependency of their efficiency with respect to the input voltage. This is visualized

in the high efficiency drop between the simulation carried out using with different input voltage amplitudes (higher than 30% and 20% for the MOSFET bridge rectifier and the GCCR, respectively).

Conclusions

In this work, a small review on topologies and commonly employed techniques used for EH rectifier circuits was presented. Where the results obtained from a SPICE simulation of three of the most common rectifier circuits were presented as well.

From the simulated circuits, the performance of the NVC rectifier can be highlighted due to its high efficiency while handling purely resistive loads, and good performance for low input values. This high efficiency is diminished when a reactive element is added to the load. Such problem may be solved by controlling the energy flow between the input and output ports of the rectifier. This approach may require additional circuits and its implementation should be further studied.

The GCCR presented very low efficiency changes when a filtering capacitor is added to the load. This suits this rectifier as a low cost alternative when highly stable output voltage and low EH system complexity is demanded by the application. The low efficiency displayed by this rectifier for low input voltages does not allow its use in very low voltage EH applications.

The MOSFET bridge rectifier displayed the lowest performance between the considered rectifiers. This rectifier presented high efficiency drops for changes in the load and the input amplitude, lower efficiency values compared with the GCCR and the resistive loaded NVC and requires the use of bulk transistor regulation. This prevents the implementation of this circuit when a high efficiency EH system is required.

It was observe that different topologies and improvement techniques are available from the EH literature. The selection of a particular topology or enhancement technique highly depends on the performance and characteristics imposed on the system by the application and the designer. This

due to the efficiency related differences observed between the simulated rectifiers to varying conditions, i.e. load and input voltage.

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Figure 1

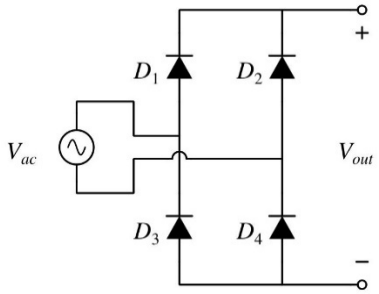

Figure 2

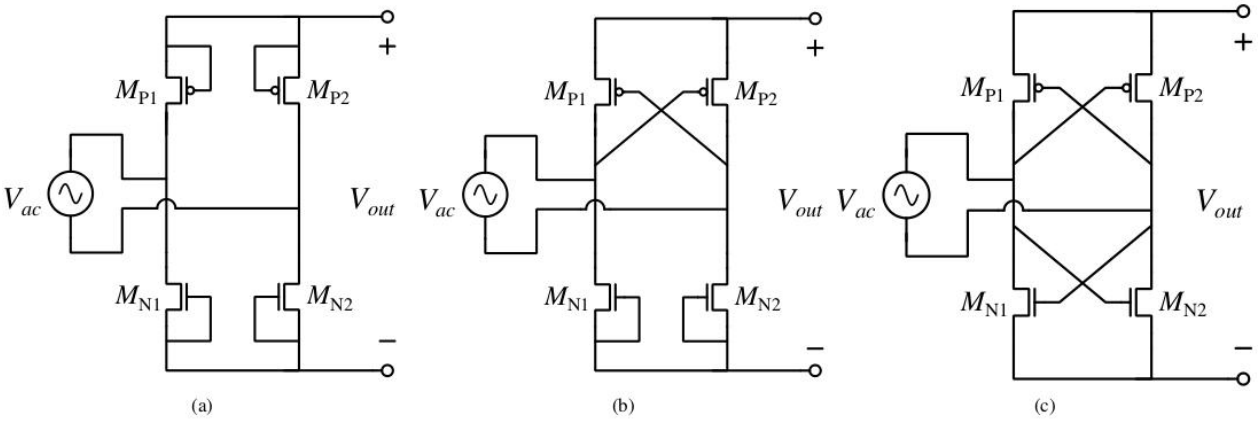

Figure 3

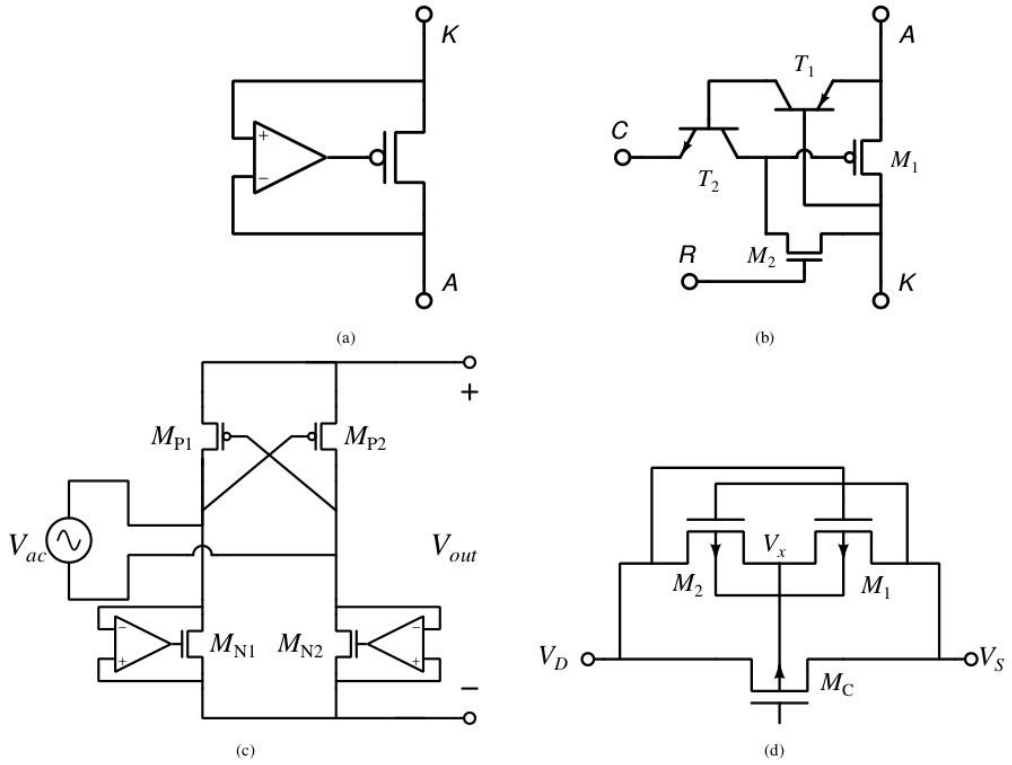

Figure 4

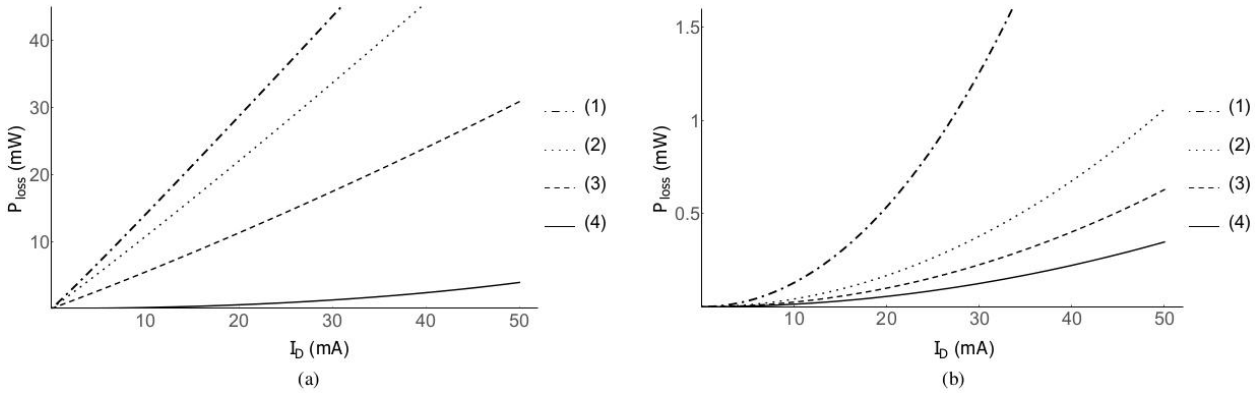

Figure 5

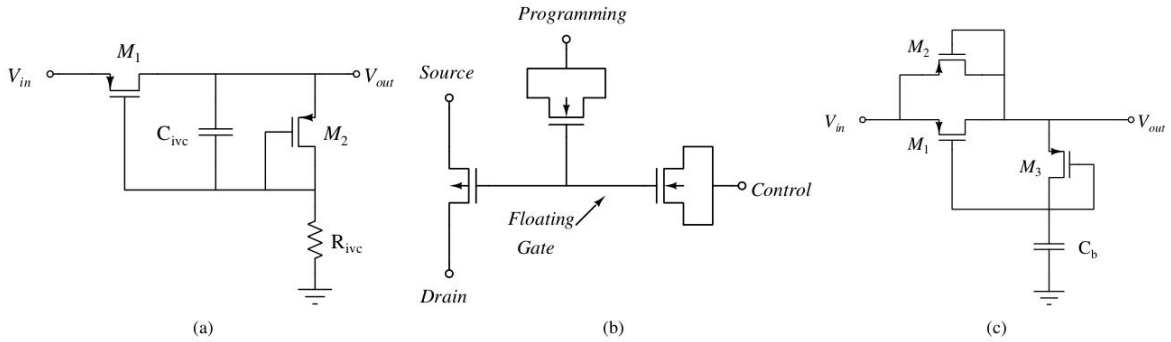

Figure 6

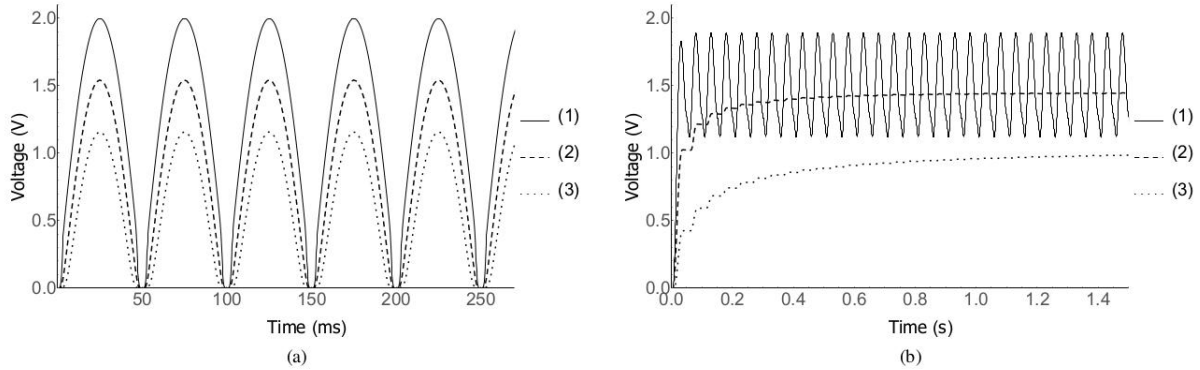

Figure 7