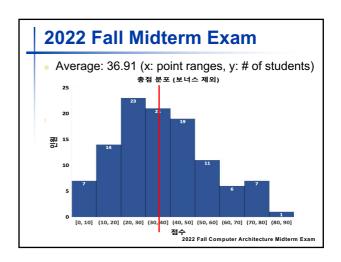
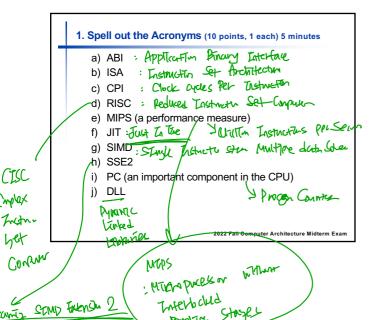
2022 Fall Midterm Exam

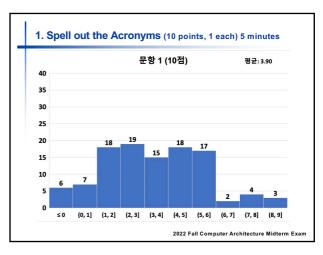
- Write in PEN!!!
 - name, student #, and then sign
 - number the sheets handed out
- Answers may be written either in pen or

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SUR



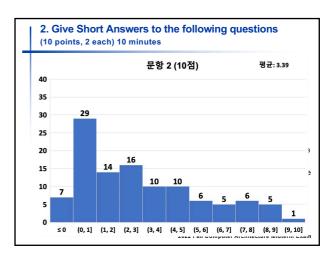


2. Give Short Answers to the following questions (10 points, 2 each) 10 minutes

(2) Give the names (the first and last names) of the authors of the textbook that we are using for this is course. Give the full name of the professor (either in English or Korean) who is teaching this course. David A- Patterson. John. L. Hennessy

(2) Explain how the overflow for integer and floating point operations are different.

- (1) Explain what the instruction 'mfhi rd' does.
- d) (1) lwc1 and swc1 are instructions that, respectively, load and store floating point words. Where does the c1 part of the instruction name come from?
- (4) Consider a program that you have written with an execution time of 10 seconds. With multicores, you have the choice to improve 10% of your code by 5 times or to improve 40% of your code by 2 times. Which would you choose? You need to clearly justify your



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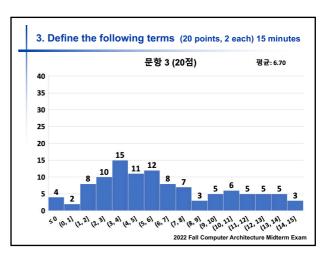
CISC

: Cmplex

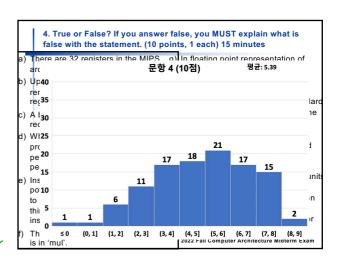
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3. Define the following terms (20 points, 2 each) 15 minutes

a) Yield (in the context of manufacturing IC chips)
b) Response time pandwidth
c) Throughput fotal amount of work done in Sten time
d) Clock Frequency Investe of done care time.
e) Amdahl's law
f) Benchmark
g) Pseudoinstruction
h) Activation record = freedule frame
i) Data race
j) Alignment restriction
A requirement that data be atgred in

menon on Natural boundaries
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4. True or False? If you answer false, you MUST explain what is false with the statement. (10 points, 1 each) 15 minutes here are 32 registers in the MIPS In floating point representation of architecture numbers, the exponent is the component that determines the Upon MIPS division, the quotient and precision of the number. remainder are placed in the HI and LO registers, respectively. Most computers today use a standar A benefit of dynamic linking is that it reduces CPU cycles. format defined by ACM, which is the most prestigious compactorization in the world. The d) While the instruction count of a program is not a good indicator of i) performance, the CPI is an excellent performance indicator of performance. To improve precision, the so-c guard, round, and sticky bits are specified as standards. They are implemented in all floating points unit Instead of simple instructions, Instead of simple instructions, powerful instructions are a good way as they are part of the standard. ARM is the most popular instruction to improve performance as more set architecture for embedded things can be done with a single devices, whose acronym stands for Advanced RISC Machine. The accent for the word 'multiplical Advised Her Moch

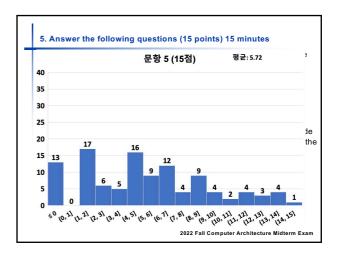


a) (2) What does it mean when we say that, at the assembly language level, that a read or write instruction is atomic?
b) (2) Two instruction II and sc are available in MIPS to handle synchronization of memory access. What does II and sc stand for?
c) (2) II and sc need to be used in combination to support synchronization. Does this mean that there can be no instructions between these two instructions being called?
d) (9) Write the MIPS assembly code to implement the following C code as an atomic "set max" operation using the II/sc instructions. Here, the argument shvar contains the address of a shared variable, which should be replaced by x if x is greater than the value it points to:

void setmax(int* shvar, int x) {

if (x > *shvar)

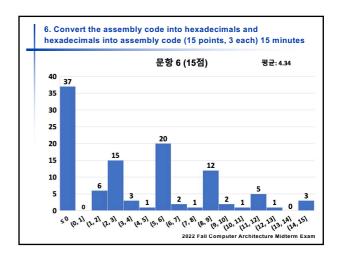
*shvar = x;
}



6. Convert the assembly code into hexadecimals and hexadecimals into assembly code (15 points, 3 each) 15 minutes

a) j 0x2000000
b) add \$t1, \$s7, \$t1
c) sw \$t0, 4(\$t8)
d) 0x15402000
e) 0x01100080

** Make use of the MIPS reference data sheet
** You may choose to just write the final answer, but showing the calculation may help you get partial credit



7. Answer the following questions (20 points) 20 minutes * Use the diagrams on the back sheet of the MIPS reference data (3) Fill in (a), (b), and (c) of Figure 1. b) (1) Specifically, what operation is performed by the ALU in Figure 1? (3) Assuming that operations performed with the multiplicand, the multiplier, and the ALU each take 1 cycle, roughly how many cycles does it take to multiply two 32-bit integers? Show your calculations. d) (2) Figure 2 shows an optimized version of Figure 1. Fill in (d) and (e) of Figure 2. (4) In the optimized version, what happened to the multiplier? Explain how the multiplier is involved in this multiplication. (4) In the same optimized version, we observe that the ALU is now a 32-bit ALU instead of a 64-bit one. Explain how this is possible. (3) This optimized version also performs better due to parallelism. Explain using specific descriptions what this parallelism is referring to (*bonus 3) Calculate the cycles needed to execute a 32-bit multiplication in this optimized version. State your assumption and show your calculations. 2022 Fall Computer Architecture Midterm Exam

