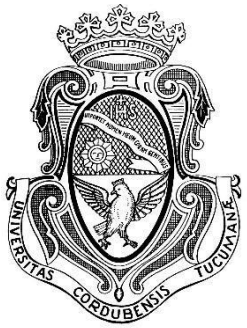

UNIVERSIDAD NACIONAL DE CÓRDOBA

FACULTAD DE CIENCIAS EXACTAS, FÍSICAS Y NATURALES

CÁTEDRA DE ELECTRÓNICA DIGITAL I

TRABAJO PRÁCTICO Nº 1

“DECODIFICADOR HEXADECIMAL A 7 SEGMENTOS”

Grupo Nº 3

Alumnos:
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Vera, Violeta

NOTA:

Profesor:
Ing. Vrech, Ruben

Comisión: Viernes 9:30 hs

Marzo / 2022

Consigna

El objetivo de este Trabajo Práctico es diseñar y construir en plaqueta tipo “Protoboard” un circuito combinacional decodificador hexadecimal con compuertas NAND y NOR de 2 entradas.

El circuito debe tener 3 entradas que formarán los números 0 al 7 en números binarios de 3 bits y a su salida un display de 7 segmentos mediante el uso de un transistor.

Con la secuencia a la entrada de los números 1-2-3-4-5-6-7 (decimales), cada grupo debe mostrar 7 números en el display en hexadecimal en forma ascendentes y del "mismo par", comenzando con el número del grupo (en nuestro caso el 3). Entonces la secuencia a mostrar será: 3-5-7-9-b-d-F.

Bajo consigna del profesor, la salida del display al tener 0-0-0 no será tomada en cuenta, permitiendo mayor flexibilidad en los cálculos.

Desarrollo

1. Tabla de Verdad

Teniendo en cuenta que para realizar el trabajo debemos transformar una entrada de 3 bits en base binaria a una salida de 7 bits en base hexadecimal, entonces los posibles números a mostrar en el display de 7 segmentos son del 0 al 9 más los números que corresponden al 10,11,12,13,14 y 15 de la base hexadecimal mostrados como A,b,C,d,E, F. Pero al tener una entrada de 3 bits solo podemos lograr 2^3 - 1 = 7 salidas, ya que al 000 lo tomamos como "valores sin cuidado".

Entonces desarrollamos la *tabla de verdad* con las entradas y salidas pautadas, aclarando que *A, B y C* son los interruptores del circuito que indican "0" si están abiertos y "1" si están cerrados, también *a,b,c,…,h,* corresponden a los segmentos de LED del display, que indican "0" si están apagados, "1" si están prendidos y "X" si son “Valores sin cuidado”.

Número	A	B	C	Display	a	b	c	d	e	f	g	h
0	0	0	0	-	x	x	x	x	x	x	x	x
1	0	0	1	3	1	1	1	1	0	0	1	0
2	0	1	0	5	1	0	1	1	0	1	1	0
3	0	1	1	7	1	1	1	0	0	0	0	0
4	1	0	0	9	1	1	1	1	0	1	1	0
5	1	0	1	b	0	0	1	1	1	1	1	0
6	1	1	0	d	0	1	1	1	1	0	1	0
7	1	1	1	F	1	0	0	0	1	1	1	0

Cuadro 1: Tabla de Verdad

2. Mapas de Karnaugh

Posteriormente de realizar la tabla de verdad, procedimos a realizar los mapas de Karnaugh para cada segmento del Display.

*tabla LED **a***

A\BC	00	01	11	10
0	X	1	1	1
1	1	0	1	0

*tabla LED **b***

A\BC	00	01	11	10
0	X	1	1	0
1	1	0	0	1

*tabla LED **c***

A\BC	00	01	11	10
0	X	1	1	1
1	1	1	0	1

*tabla LED **d***

A\BC	00	01	11	10
0	X	1	0	1
1	1	1	0	1

*tabla LED **e***

A\BC	00	01	11	10
0	X	0	0	0
1	0	1	1	1

*tabla LED **f***

A\BC	00	01	11	10
0	X	0	0	1
1	1	1	1	0

*tabla LED **g***

A\BC	00	01	11	10
0	X	1	0	1
1	1	1	1	1

*tabla LED **h***

A\BC	00	01	11	10
0	X	0	0	0
1	0	0	0	0

Cuadro 2: Mapas de Karnaugh

Cálculos

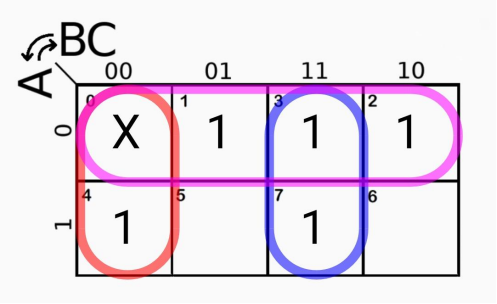
1. Simplificación y armado de Ecuaciones Lógicas

Luego de obtener los Mapas de Karnaugh, seguimos con la agrupación y simplificación de las funciones booleanas de cada diagrama, bajo las siguientes pautas:

- Solo se pueden armar grupos de tamaño 2^n.
- Cada grupo debe ser de mayor tamaño posible, teniendo la posibilidad de superponerse con otro grupo para lograrlo.
- Los valores X (sin cuidado) pueden tomar tanto valor 0 como 1 dependiendo de la utilidad al cálculo algebráico.

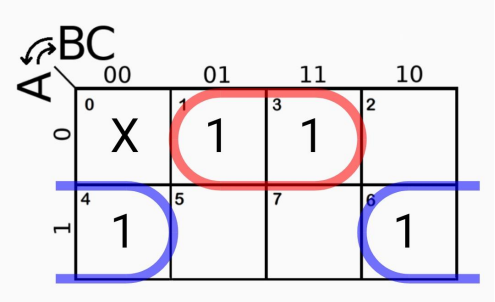
También, ya que la pauta del trabajo práctico consiste en solo utilizar compuertas NAND y NOR de 2 entradas, los cálculos se harán para lograr dicha pauta.

- ***Segmento a:***



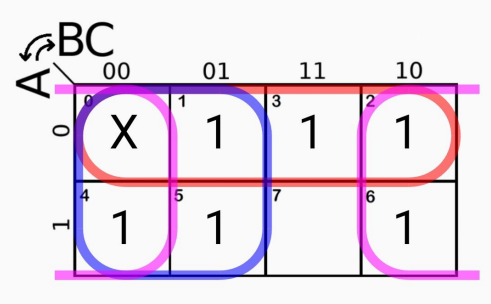
$$a = \overline{A} + \overline{B}.\overline{C} + BC = \overline{A} + (\overline{B + C}) + BC = \overline{\overline{\overline{A} + (\overline{B} + \overline{C})} + BC} = \overline{(\overline{A} + (\overline{B} + \overline{C}))} \cdot \overline{BC}$$

- ***Segmento b:***



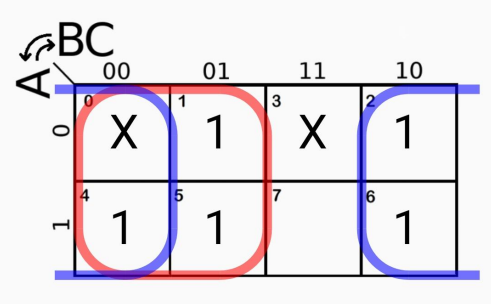
$$b = \overline{A}C + A\overline{C} = (A + C)(\overline{A} + \overline{C}) = (A + C)(\overline{AC}) = \overline{\overline{(A + C)(\overline{AC})}} = \overline{(\overline{A + C}) + AC}$$

- ***Segmento c:***



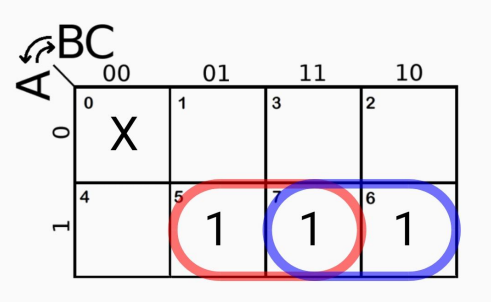
$$c = \overline{B} + \overline{C} + \overline{A} = \overline{\overline{(B.C)} + \overline{A}} = \overline{\overline{(B.C)}.A}$$

- ***Segmento d:***



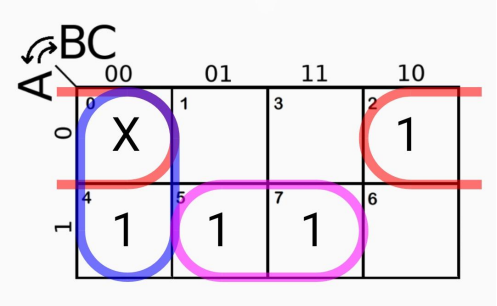
$$d = \overline{B} + \overline{C} = \overline{B.C}$$

- ***Segmento e:***



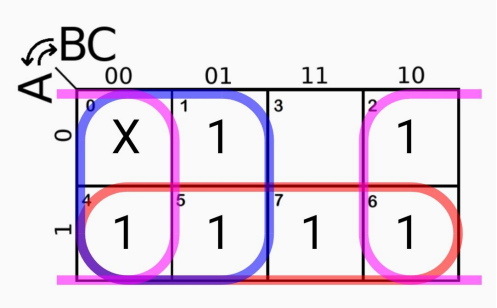
$$e = AC + AB = \overline{\overline{A(C + B)}} = \overline{\overline{A} + \overline{(C + B)}}$$

- ***Segmento f:***



$$f = \overline{A}.\overline{C} + A\overline{B} + AC = \overline{\overline{\overline{A}.\overline{C} + A(\overline{B} + C)}} = \overline{\overline{(A + C)} + A(\overline{B} + C)} = \overline{(\overline{\overline{A + C}}).(\overline{A} + (\overline{\overline{B} + C)}}$$
$$= \overline{(\overline{A + C}) + (\overline{A} + (\overline{\overline{B} + C}))}$$

- ***Segmento g:***



$$g = \overline{B} + \overline{C} + A = \overline{\overline{BC} + A} = \overline{\overline{BC}}.\overline{A} = \overline{BC}.\overline{A}$$

- ***Segmento h:***

En el caso del segmento h no hay ecuación porque no se utiliza el "punto" en ninguna salida del display.

2. Resistencias Colector y Base

De los componentes físicos comprados, obtuvimos los valores necesarios para el cálculo de las resistencias de colector y de base necesarias para lograr que cada segmento tenga 20mA de corriente y 2 V de tensión.

$\beta = 260$

Vcc = 6,3 [V]

Cálculo de resistencias usadas en los transistores:

$$R_c = \frac{V_{CC} - V_{CE} - V_D}{I_C} = \frac{6{,}3\ V - 0{,}4\ V - 2\ V}{20\ mA} \Rightarrow R_c = 195\ \Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{20\ mA}{260} \Rightarrow I_B = 77\ \mu A$$

$$R_b = \frac{V_{CC} - V_{BE} - V_D}{I_B} = \frac{6{,}3\ V - 0{,}2\ V - 2\ V}{77\ \mu A} \Rightarrow R_b = 53\ K\Omega$$

Se aclara que al no contar con las resistencias calculadas para R_c y R_b se utilizaron las más cercanas en valor que teníamos a disposición: 220 Ω y 47 KΩ respectivamente.

3. Resistencias Pull-Down

Para evitar que el PIN de entrada sea considerado de alta impedancia o flotante (quiere decir que cualquier perturbación o interferencia puede producir cambios de estado en la entrada o salida del PIN), por lo tanto es necesario el uso de las resistencias Pull-Down. La configuración Pull-Down permite que en el circuito se mantenga un nivel lógico 0 mientras el circuito se encuentra en reposo. Debido a que en nuestro circuito no se considera sensible a la potencia de entrada o a la velocidad de entrada, tomaremos un valor general de resistencia, siendo este 10KΩ. También se verifica la desigualdad:

$$V_{IL}/I_F = 1{,}5V/\text{0,77µA} = 19{,}5K\Omega > R_{PULL\ DOWN}$$

77microA

Diagrama Circuital

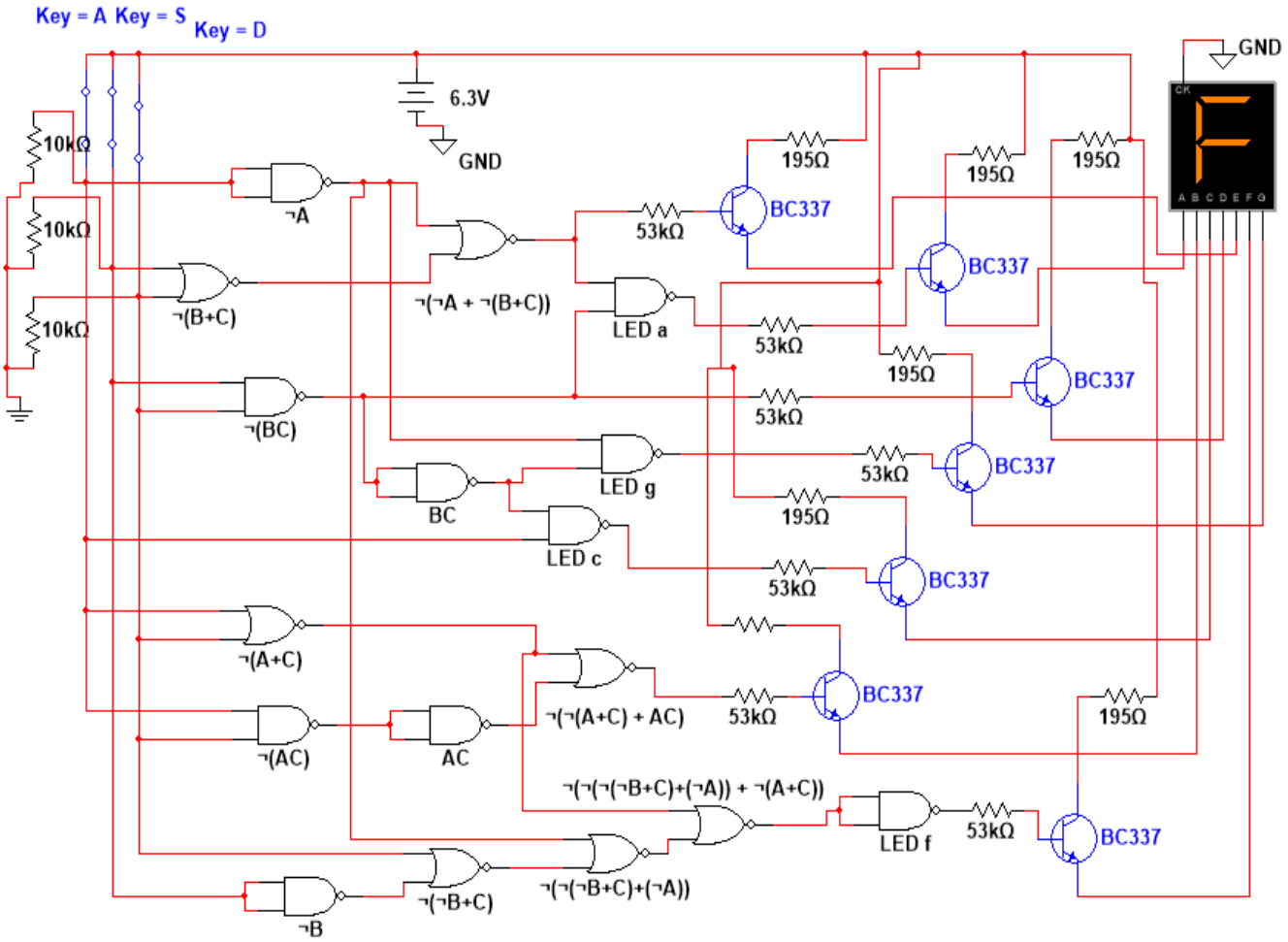


Imagen 1: Diagrama Circuital funcional simulado en Multisim.

Materiales

- Fuente de alimentación de 6,3 V (4 pilas de 1,5 V)
- Interruptor DIP switch de 4 posiciones (del cual solo usamos 3)
- 3 resistencias de 10 KΩ (Resistencias Pull-Down)
- 7 resistencias de 220 Ω (Resistencias de colector usadas en los transistores)
- 7 resistencias de 50 KΩ (Resistencias de base usadas en los transistores)
- 3 chips NAND de 4 compuertas (CD4011BC)
- 2 chips NOR de 4 compuertas (CD4001BC)
- 7 transistores NPN (BC337B)
- Display de 7 segmentos de cátodo común (REC-S5121CSR)
- 2 Placas Protoboard

(Data sheets adjuntados al final del informe)

Gráficos Topológicos

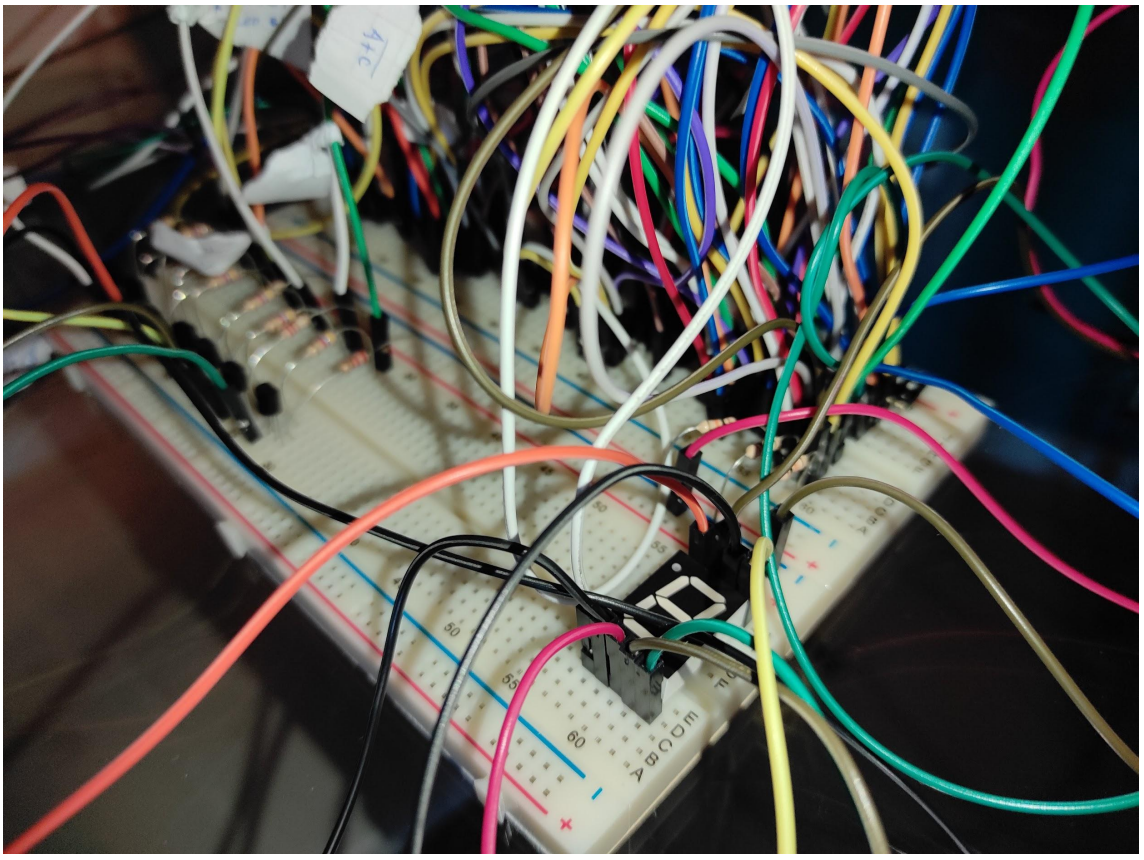


Imagen 2: Fotografía General del Circuito Armado en Protoboard, con Display visible.

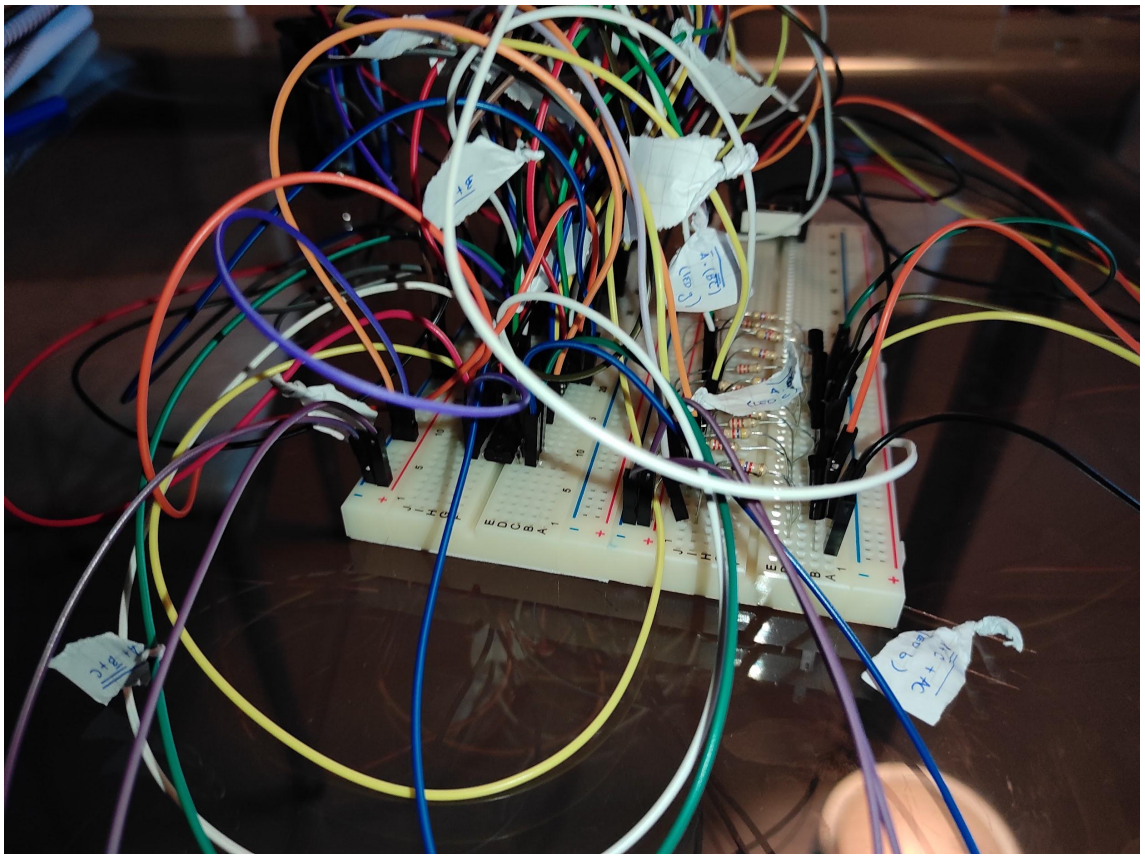
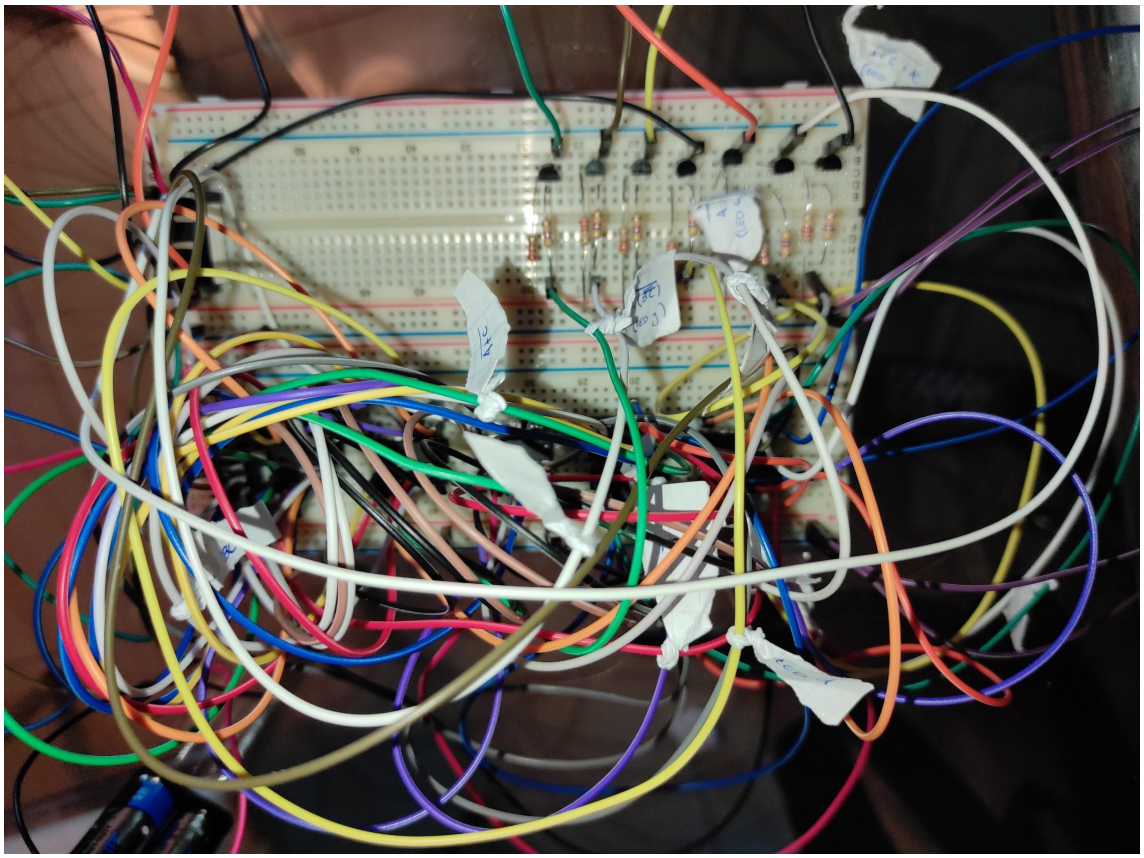


Imagen 3 e Imagen 4: Vistas Lateral y Dorsal del Circuito.



Conclusiones

En este primer trabajo práctico se logró construir un decodificador hexadecimal de siete segmentos, poniendo en juego conocimientos básicos sobre el álgebra de Boole y sistemas combinacionales, nos permitió adquirir y mejorar conocimientos prácticos sobre el armado de circuitos utilizando placas protoboard (conocimientos que no se tenían previamente).
A la hora de armar el circuito se destaca la importancia de que su diseño sea tan simple como sea posible, a modo de evitar un circuito tedioso de armar y difícil de estudiar.

Bibliografía y referencias

- [1] Página Web Zona Maker - Resistencias Pull-Up y Pull-Down https://www.zonamaker.com/electronica/intro-electronica/teoria/resistencias-de-pull-up-y-pull-down
- [1] Página Web Programar Facil - Resistencia Pull-Up y Pull-Down https://programarfacil.com/blog/arduino-blog/resistencia-pull-up-y-pull-down/
- [1] All Data Sheets https://www.alldatasheet.es

Hojas de Datos

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised March 2002

CD4001BC/CD4011BC
Quad 2-Input NOR Buffered B Series Gate • Quad 2-Input NAND Buffered B Series Gate

General Description

The CD4001BC and CD4011BC quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Low power TTL:
  Fan out of 2 driving 74L compatibility: or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

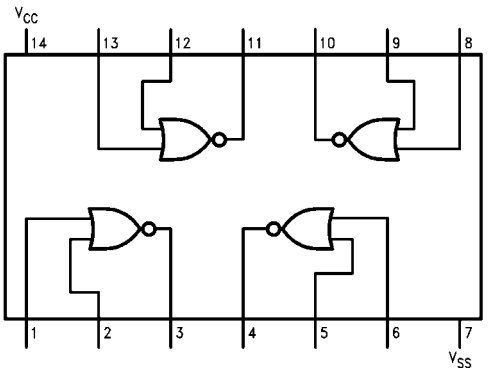
Ordering Code:

Order Number	Package Number	Package Description
CD4001BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4001BCSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4001BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4011BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4011BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

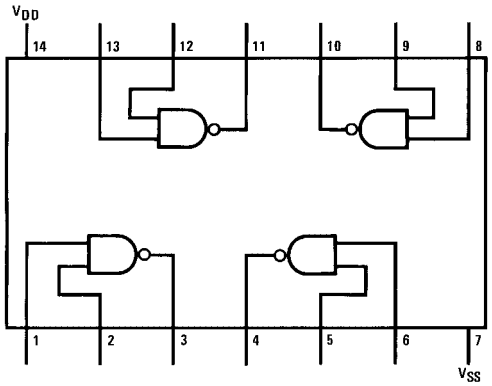
Connection Diagrams

Pin Assignments for DIP, SOIC and SOP
CD4001BC



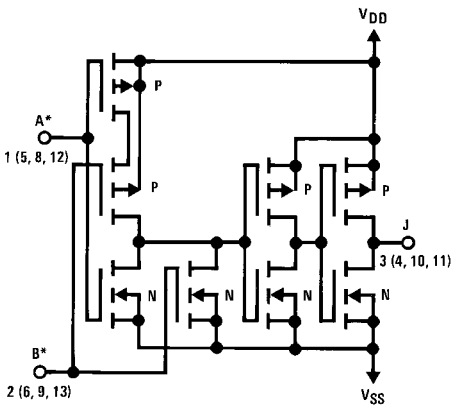
Top View

Pin Assignments for DIP and SOIC
CD4011BC

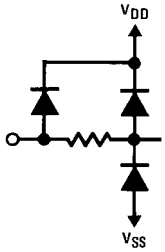


Top View

Schematic Diagrams



CD4001BC



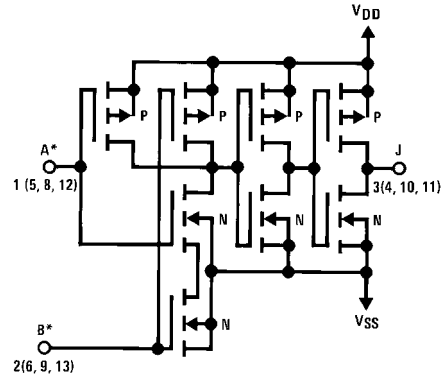
$^1/_4$ of device shown

$J = \overline{A + B}$

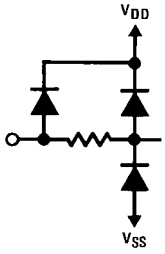
Logical "1" = HIGH

Logical "0" = LOW

All inputs protected by standard CMOS protection circuit.



CD4011BC



$^1/_4$ of device shown

$J = \overline{A \bullet B}$

Logical "1" = HIGH

Logical "0" = LOW

All inputs protected by standard CMOS protection circuit.

Absolute Maximum Ratings(Note 1)

(Note 2)

Voltage at any Pin	−0.5V to V_{DD} +0.5V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
V_{DD} Range	−0.5 V_{DC} to +18 V_{DC}
Storage Temperature (T_S)	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions

Operating Range (V_{DD})	3 V_{DC} to 15 V_{DC}
Operating Temperature Range	
CD4001BC, CD4011BC	−55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics tables provide conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		0.5		0.005	0.50		15	
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		1.0		0.006	1.0		30	
V_{OL}	LOW Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	
		V_{DD} = 15V		0.05		0	0.05		0.05	
V_{OH}	HIGH Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V $\lvert I_O \rvert$ < 1 μA	9.95		9.95	10		9.95		
		V_{DD} = 15V	14.95		14.95	15		14.95		
V_{IL}	LOW Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	
V_{IH}	HIGH Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		
I_{OL}	LOW Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		
I_{OH}	HIGH Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.10		1.0	

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics (Note 4)

CD4001BC: T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical temperature coefficient is 0.3%/°C.

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	
		V_{DD} = 15V	35	70	
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level	V_{DD} = 5V	110	250	ns
		V_{DD} = 10V	50	100	
		V_{DD} = 15V	35	70	
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	
		V_{DD} = 15V	40	80	
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Note 5)

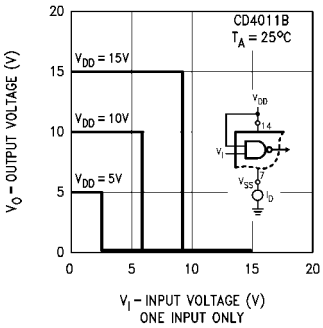
CD4011BC: T_A= 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical Temperature Coefficient is 0.3%/°C.

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay,	V_{DD} = 5V	120	250	
	HIGH-to-LOW Level	V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	
t_{PLH}	Propagation Delay,	V_{DD} = 5V	85	250	
	LOW-to-HIGH Level	V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

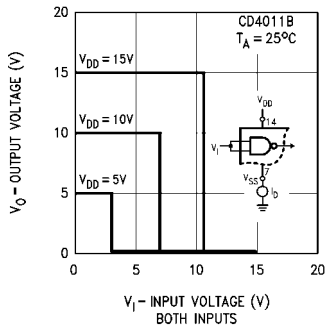
Note 5: AC Parameters are guaranteed by DC correlated testing.

Typical Performance Characteristics

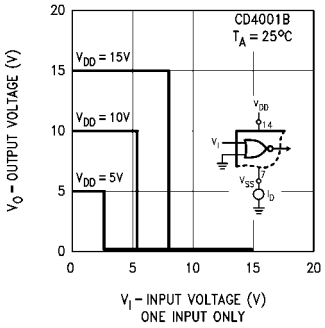
Typical Transfer Characteristics



Typical Transfer Characteristics

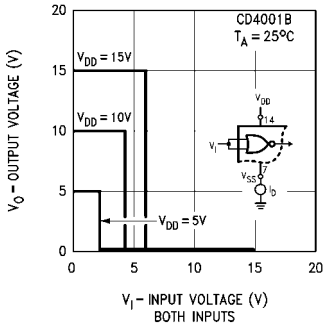


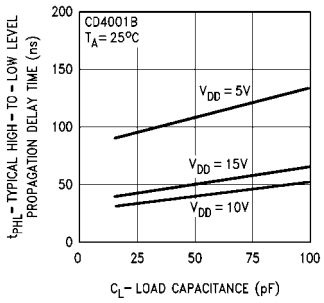
Typical Transfer Characteristics

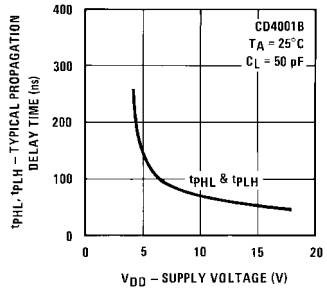


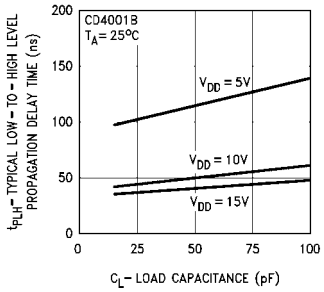
Typical Performance Characteristics (Continued)

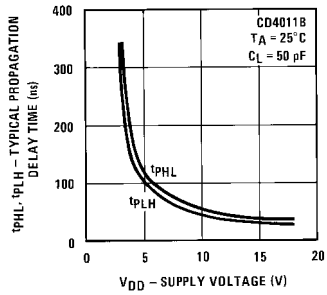
Typical Transfer Characteristics

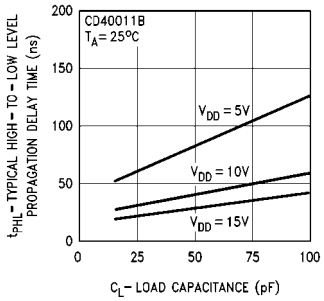




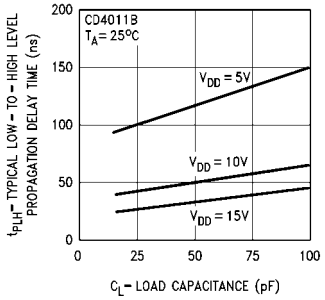


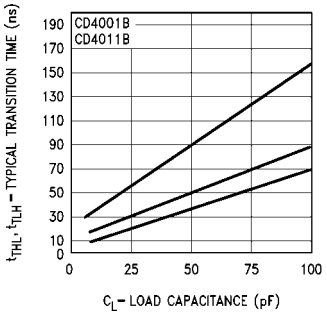


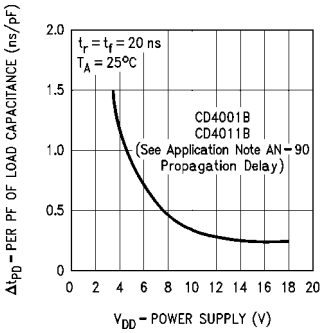


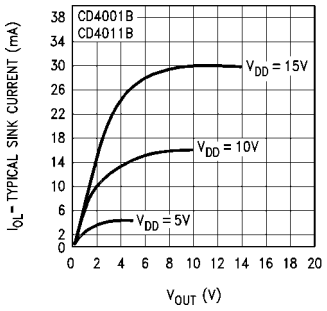


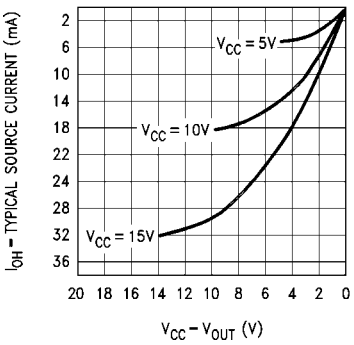
Typical Performance Characteristics (Continued)



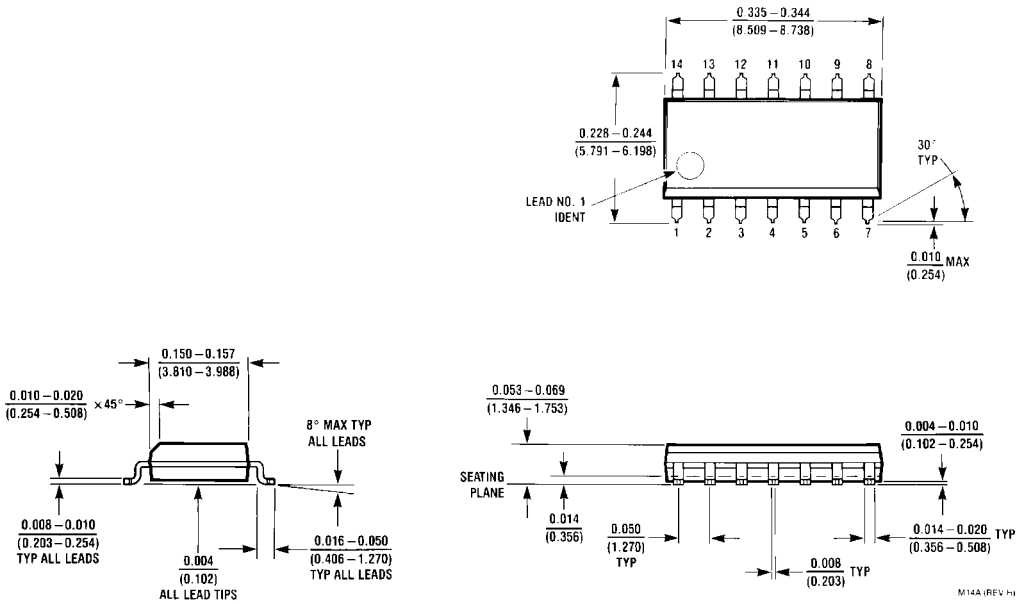






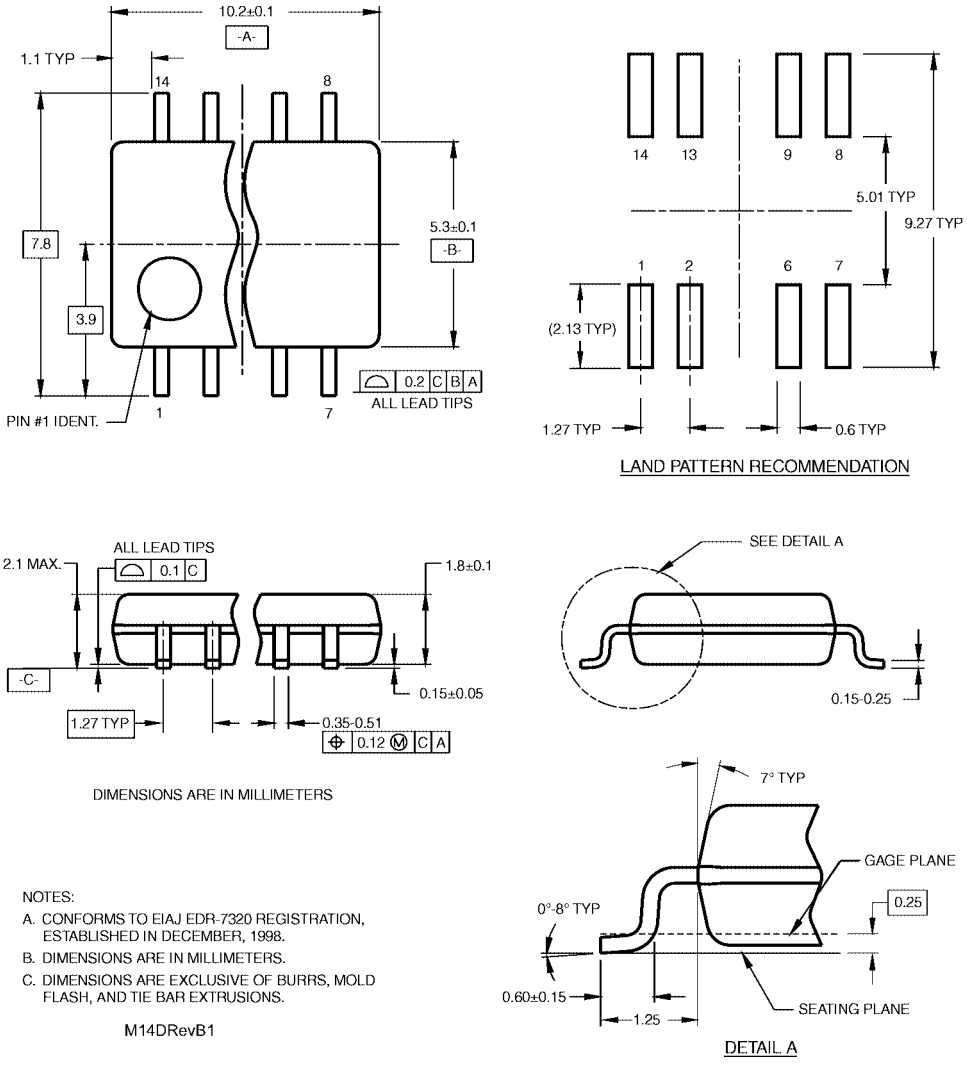


Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

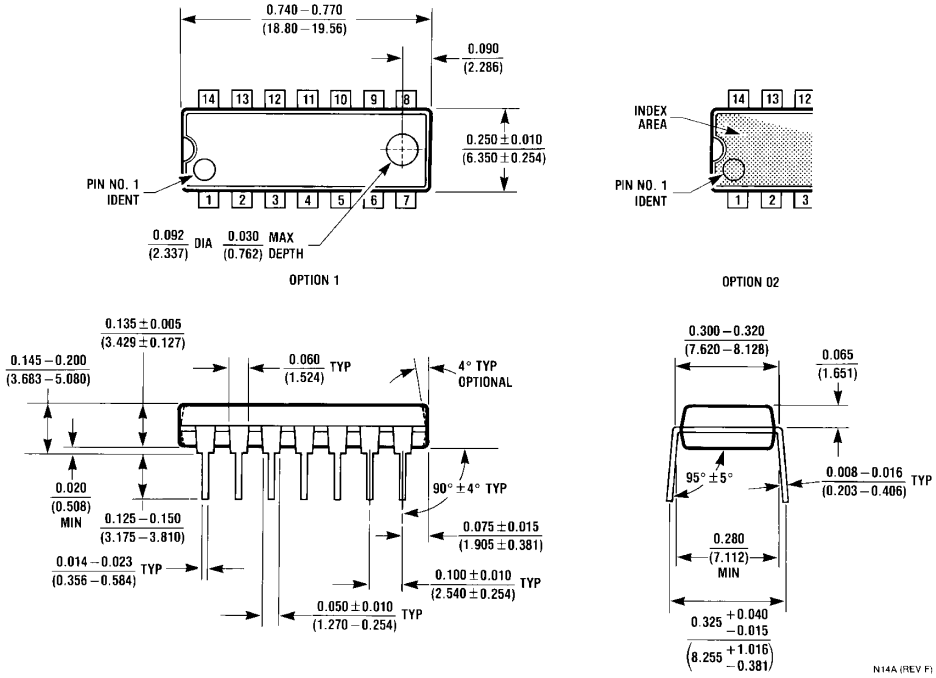
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



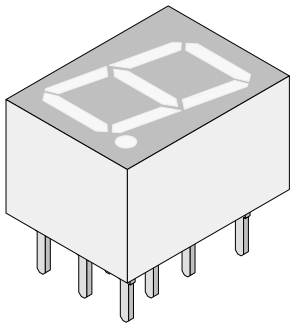
14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

Standard 7– Segment Display 7 mm

Color	Type	Circuitry
Red	TDSR115.	Common anode
Red	TDSR116.	Common cathode
Orange red	TDSO115.	Common anode
Orange red	TDSO116.	Common cathode
Yellow	TDSY115.	Common anode
Green	TDSG115.	Common anode
Green	TDSG116.	Common cathode

Description

The TDS.11.. series are 7 mm character seven segment LED displays in a very compact package.
The displays are designed for a viewing distance up to 3 meters and available in four bright colors. The grey package surface and the evenly lighted untinted segments provide an optimum on-off contrast.
All displays are categorized in luminous intensity groups. That allows users to assemble displays with uniform appearence.
Typical applications include instruments, panel meters, point-of-sale terminals and household equipment.



96 11506

Features

- Evenly lighted segments
- Grey package surface
- Untinted segments
- Luminous intensity categorized
- Yellow and green categorized for color
- Wide viewing angle
- Suitable for DC and high peak current

Applications

Panel meters
Test- and measure- equipment
Point-of-sale terminals
Control units

Absolute Maximum Ratings

T_{amb} = 25°C, unless otherwise specified

TDSR115. /TDSR116. , **TDSO115. /TDSO116.** , **TDSY115. TDSG115. /TDSG116.** , **/**

Parameter	Test Conditions	Type	Symbol	Value	Unit
Reverse voltage per segment or DP			V_R	6	V
DC forward current per segment or DP		TDSR115./116.	I_F	25	mA
		TDSO115./116.	I_F	17	mA
		TDSY115.	I_F	17	mA
		TDSG115./116.	I_F	17	mA
Surge forward current per segment or DP	$t_p \leq 10$ µs (non repetitive)	TDSR115./116.	I_{FSM}	0.5	A
		TDSO115./116.	I_{FSM}	0.15	A
		TDSY115.	I_{FSM}	0.15	A
		TDSG115./116.	I_{FSM}	0.15	A
Power dissipation	$T_{amb} \leq 45$˚C		P_V	400	mW
Junction temperature			T_j	100	˚C
Operating temperature range			T_{amb}	–40 to + 85	˚C
Storage temperature range			T_{stg}	–40 to + 85	˚C
Soldering temperature	t ≤ 3 sec, 2mm below seating plane		T_{sd}	260	˚C
Thermal resistance LED junction/ambient			R_{thJA}	140	K/W

Optical and Electrical Characteristics

T_{amb} = 25°C, unless otherwise specified

Red (**TDSR115.** , **TDSR116.**)

Parameter	Test Conditions	Type	Symbol	Min	Typ	Max	Unit
Luminous intensity per segment (digit average) 1)	I_F = 10 mA	TDSR1150/1160	I_V	180			µcd
Dominant wavelength	I_F = 10 mA		λ_d		645		nm
Peak wavelength	I_F = 10 mA		λ_p		660		nm
Angle of half intensity	I_F = 10 mA		φ		±50		deg
Forward voltage per segment or DP	I_F = 20 mA		V_F		1.6	2	V
Reverse voltage per segment or DP	I_R = 10 µA		V_R	6	15		V
1) I_{Vmin} and I_V groups are mean	values of segments a to g						

Orange red (**TDSO115.** , **TDSO116.**)

Parameter	Test Conditions	Type	Symbol	Min	Typ	Max	Unit
Luminous intensity per segment (digit average) 1)	I_F = 10 mA	TDSO 1150/1160	I_V	450			µcd
Dominant wavelength	I_F = 10 mA		λ_d	612		625	nm
Peak wavelength	I_F = 10 mA		λ_p		630		nm
Angle of half intensity	I_F = 10 mA		φ		±50		deg
Forward voltage per segment or DP	I_F = 20 mA		V_F		2	3	V
Reverse voltage per segment or DP	I_R = 10 µA		V_R	6	15		V
1) I_{Vmin} and I_V groups are mean values of segments a to g							

Yellow (**TDSY115.**)

Parameter	Test Conditions	Type	Symbol	Min	Typ	Max	Unit
Luminous intensity per segment (digit average) 1)	I_F = 10 mA	TDSY1150	I_V	450			µcd
Dominant wavelength	I_F = 10 mA		λ_d	581		594	nm
Peak wavelength	I_F = 10 mA		λ_p		585		nm
Angle of half intensity	I_F = 10 mA		φ		±50		deg
Forward voltage per segment or DP	I_F = 20 mA		V_F		2.4	3	V
Reverse voltage per segment or DP	I_R = 10 µA		V_R	6	15		V
1) I_{Vmin} and I_V groups are mean values of segments a to g							

Green (**TDSG115.** , **TDSG116.**)

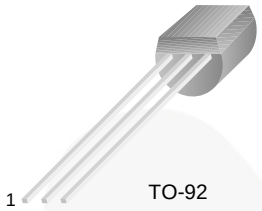
Parameter	Test Conditions	Type	Symbol	Min	Typ	Max	Unit
Luminous intensity per segment (digit average) 1)	I_F = 10 mA	TDSG 1150/1160	I_V	450			µcd
Dominant wavelength	I_F = 10 mA		λ_d	562		575	nm
Peak wavelength	I_F = 10 mA		λ_p		565		nm
Angle of half intensity	I_F = 10 mA		φ		±50		deg
Forward voltage per segment or DP	I_F = 20 mA		V_F		2.4	3	V
Reverse voltage per segment or DP	I_R = 10 µA		V_R	6	15		V
1) I_{Vmin} and I_V groups are mean values of segments a to g							

October 2014

BC337 / BC338
NPN Epitaxial Silicon Transistor

Features

- Switching and Amplifier Applications
- Suitable for AF-Driver Stages and Low-Power Output Stages
- Complement to BC327 / BC328



TO-92

1. Collector 2. Base 3. Emitter

Ordering Information

Part Number	Top Mark	Package	Packing Method
BC33716BU	BC33716	TO-92 3L	Bulk
BC33716TA	BC33716	TO-92 3L	Ammo
BC33716TFR	BC33716	TO-92 3L	Tape and Reel
BC33725BU	BC33725	TO-92 3L	Bulk
BC33725TA	BC33725	TO-92 3L	Ammo
BC33725TAR	BC33725	TO-92 3L	Ammo
BC33725TF	BC33725	TO-92 3L	Tape and Reel
BC33725TFR	BC33725	TO-92 3L	Tape and Reel
BC33740BU	BC33740	TO-92 3L	Bulk
BC33740TA	BC33740	TO-92 3L	Ammo
BC33825TA	BC33825	TO-92 3L	Ammo

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Value	Unit
V_{CES}	Collector-Emitter Voltage	BC337	50	V
		BC338	30	
V_{CEO}	Collector-Emitter Voltage	BC337	45	V
		BC338	25	
V_{EBO}	Emitter-Base Voltage		5	V
I_C	Collector Current (DC)		800	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-55 to 150	°C

Thermal Characteristics[1]

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Power Dissipation	625	mW
	Derate Above 25°C	5.0	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	200	°C/W

Note:

1. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

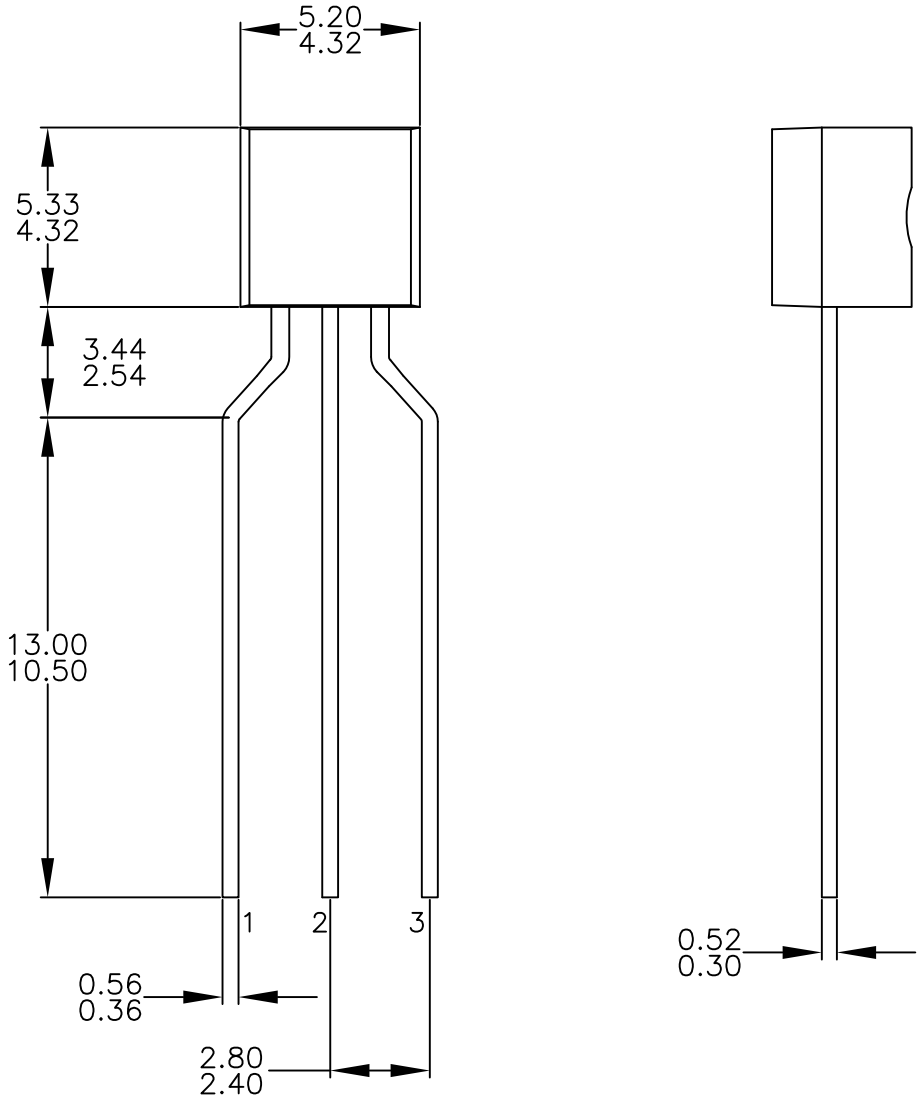
Electrical Characteristics

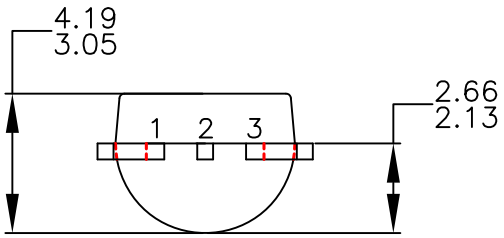
Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
BV_{CEO}	Collector-Emitter Breakdown Voltage	BC337	I_C = 10 mA, I_B = 0	45			V
		BC338		25			
BV_{CES}	Collector-Emitter Breakdown Voltage	BC337	I_C = 0.1 mA, V_{BE} = 0	50			V
		BC338		30			
BV_{EBO}	Emitter-Base Breakdown Voltage		I_E = 0.1 mA, I_C = 0	5			V
I_{CES}	Collector Cut-Off Current	BC337	V_{CE} = 45 V, I_B = 0		2	100	nA
		BC338	V_{CE} = 25 V, I_B = 0		2	100	
h_{FE1}	DC Current Gain		V_{CE} = 1 V, I_C = 100 mA	100		630	
h_{FE2}			V_{CE} = 1 V, I_C = 300 mA	60			
V_{CE}(sat)	Collector-Emitter Saturation Voltage		I_C = 500 mA, I_B = 50 mA			0.7	V
V_{BE}(on)	Base-Emitter On Voltage		V_{CE} = 1 V, I_C = 300 mA			1.2	V
f_T	Current Gain Bandwidth Product		V_{CE} = 5 V, I_C = 10 mA, f = 50 MHz		100		MHz
C_{ob}	Output Capacitance		V_{CB} = 10 V, I_E = 0, f = 1 MHz		12		pF

h_{FE} Classification

Classification	16	25	40
h_{FE1}	100 ~ 250	160 ~ 400	250 ~ 630
h_{FE2}	60 ~	100 ~	170 ~





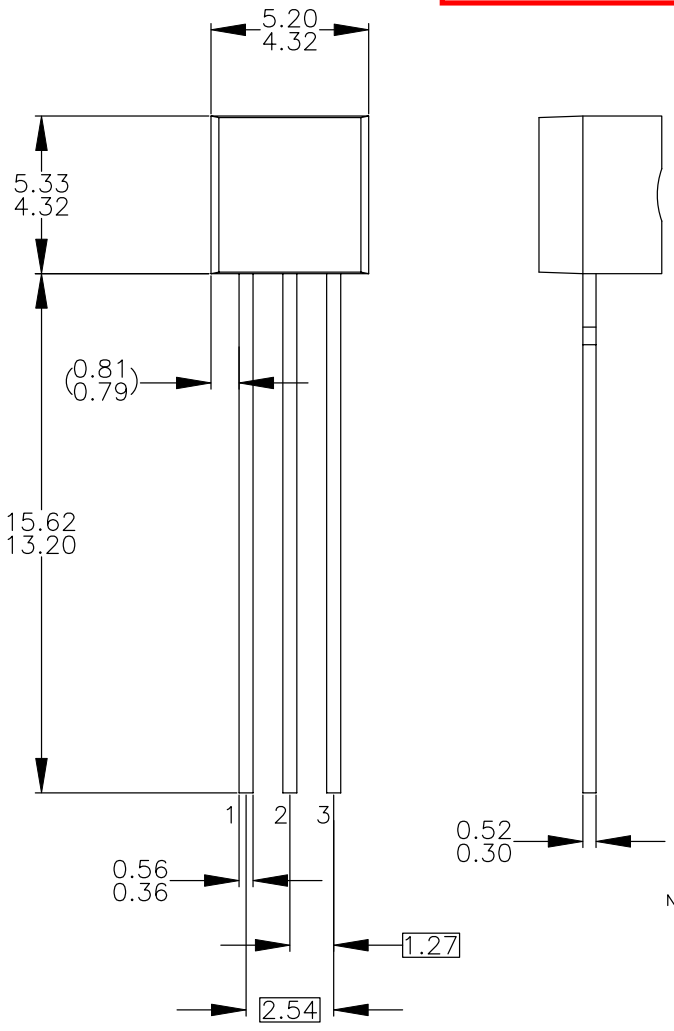
NOTES: UNLESS OTHERWISE SPECIFIED

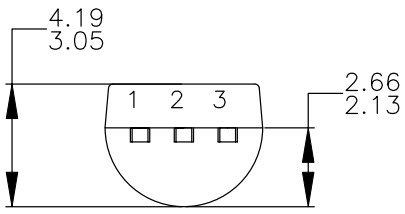
A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5M-2009.
D. DRAWING FILENAME: MKT-ZA03FREV3.
E. FAIRCHILD SEMICONDUCTOR.

REVISIONS

NO.	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	MAR.4'96	RP
B	RDRW AS PER STD DWG TEMPLATE. CHG DIM REF FR DUAL DIM INCH[MM] TO SINGLE DIM MM. CHG LD PITCH DIM FR 1.14–1.40 TO 1.27 BSC. ADD DIM 2.54 BSC. CHG PKG WIDTH DIM FR 4.32– 4.70 TO 4.32–4.83; CHG PKG HEIGHT DIM FR 4.32–4.70 TO 4.32–4.78; CHG LD THICK DIM FR 0.30– 0.48 TO 0.30–0.52; DAMBAR–PKG DIM FR 1.27–1.65 TO 0.90–1.65; LD LGH DIM FR 14.47–15.64 TO 14.47–15.62; PKG DIM: 1.02–1.52 TO 0.92–1.52, 3.81–4.45 TO 3.40–4.80; NOTE 2: ADD DMOS "M" OPT'N AND LEGEND; NOTE B PKG 94 JFET OPT'N: CHG D TO S, CHG S TO D. ADD NOTE C; MOVE NOTE B INFO FR PKG 97&98 TO NEW NOTE D.	40CT1999	RCM/MRG
3	CHG LD LEN FR $^{15.61}_{14.07}$ TO $^{15.62}_{13.20}$; CHG MOLD BODY HT FR $^{4.78}_{4.32}$ TO $^{5.33}_{4.32}$; CHG PKG EDGE TO LD EDGE DIST FR (0.81) TO $^{(0.81)}_{(0.79)}$; CHG MOLD BODY WIDTH FR $^{4.83}_{4.32}$ TO $^{5.20}_{4.32}$; ADD PKG THICKNESS DIM 'E'; CHG 's' DIM FR $^{2.41}_{2.15}$ TO $^{2.66}_{2.13}$; REMOVE DAMBAR & EJECTOR PIN LOCATOR FEATURES & DIMENSIONS; REMOVE MOLDED SURFACE & DRAFT ANGLE DIMS; ADD NOTE ON JEDEC REFERENCE; ADD NOTE ON ASME Y14.5M–1994; REMOVE NOTE ON L34Z OPTION; ADD NOTE ON DWG FILENAME.	12FEB08	BMR/FSCP

APPROVED
July-14-2008





NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO–92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M–1994.
D) TO–92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT–ZA03DREV3.

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	03APR2008
CHECKED: L. GALERA	
APPROVED: M.R. GESTOLE	
G.S. BAJE	

PROJECTION INCH [MM]

FAIRCHILD SEMICONDUCTOR™

3LD,TO–92,MOLDED
STD STRAIGHT LD
(NO EOL CODE)

SCALE	SIZE	DRAWING NUMBER	REV
1:1	N/A	MKT–ZA03D	3

FORMERLY: N/A
SHEET : 1 OF 1

TRADEMARKS

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CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
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