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Lab 4 Report

Exercise 2

Using the code from experiment 4 we use it to write a burst of reads and a burst of writes first session is gone in even increasing order second session is done in odd decreasing order

NOTE: in the first session for the even location is done in increasing order
S_WRITE_CYCLE: we write the 16 least significant bits of the address for the first 256 (from location 0 up to location 256k - 2) even locations, and then when the address is equal to 18'h3FFFF, we disable the write and reset the address to 0, and go to the DELAY_1 state:
S_DELAY_1: read_data needs a delay, and update address by 18'd2, go to DELAY_2
S_DELAY_2: read_data needs a delay, and update address by +18'd2
S_READ_CYCLE: we compare the read data against the expected data making sure they match up, for the first 256k locations, then go to the DELAY_3
S_DELAY_3: read_data needs a delay, checks to see if read data match up with expected data if true we set BIST_mismatch to 1'b1, go to DELAY_4
S_DELAY_4: read_data needs a delay, checks to see if read data match up with expected data if true we set BIST_mismatch to 1'b1, set the address to go to 18'h3FFFF enable the write and go to S_WRITE_CYCLE_2

NOTE: in the second session for the odd location is done in decreasing order
S_WRITE_CYCLE_2: we write the 16 least significant bits of the address for the first 256k odd locations (going in decreasing order from 256k – 1 down to location 1), and then when the address is equal to 18'd1, we disable the write and reset the address to 18'h3FFFF, and go to the DELAY_5 state
S_DELAY_5:read_data needs a delay, and update address by -18'd2
S_DELAY_6: :read_data needs a delay, and update address by -18'd2
S_READ_CYCLE_2: we compare the read data against the expected data making sure they match up, for the first 256k locations, then go to the DELAY_7
S_DELAY_7: read_data needs a delay, checks to see if read data match up with expected data if true we set BIST_mismatch to 1'b1, go to DELAY_8
S_DELAY_8: read_data needs a delay, checks to see if read data match up with expected data if true we set BIST_mismatch to 1'b1, go to S_IDLE;