VLSI Design

32-Bit Brent-Kung Adder EE 671 : Assignment #3

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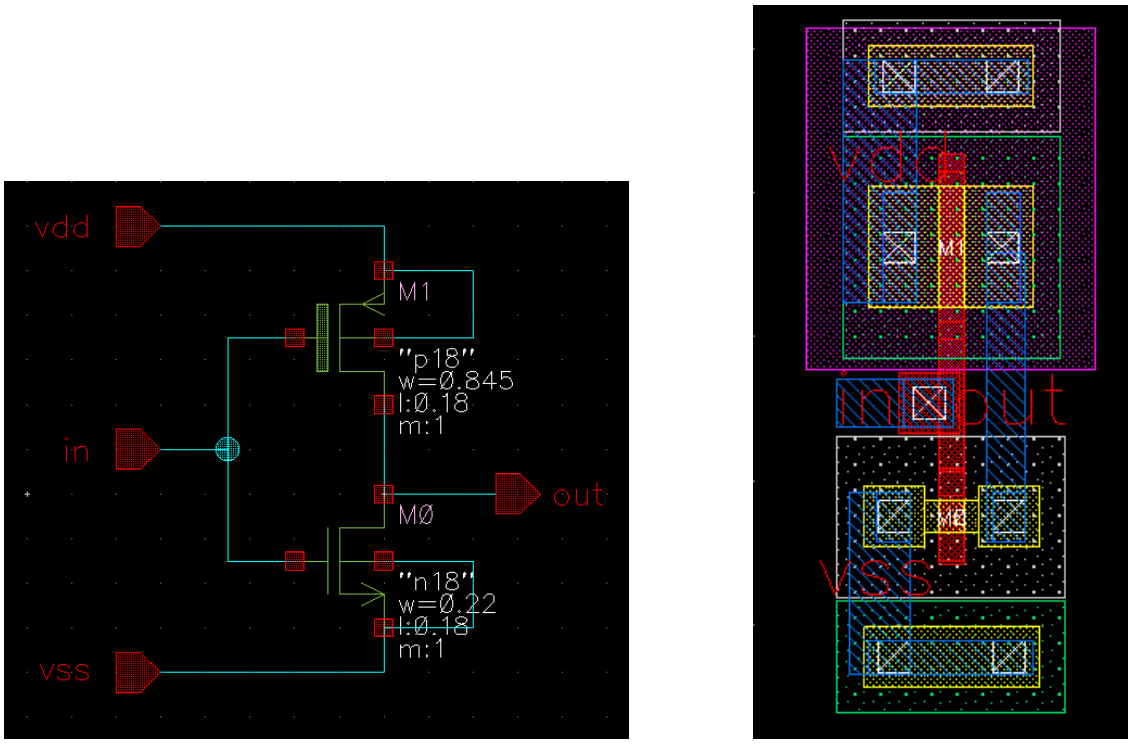
Basic Components

This section includes all the basic components required for 32-bit Brent-Kung adder. All the components are designed and simulated for SCL's 180 nm process.

Minimum Sized Inverter

Design and Layout



(a) Schematic (b) Layout

Figure 1: Minimum Sized Inverter

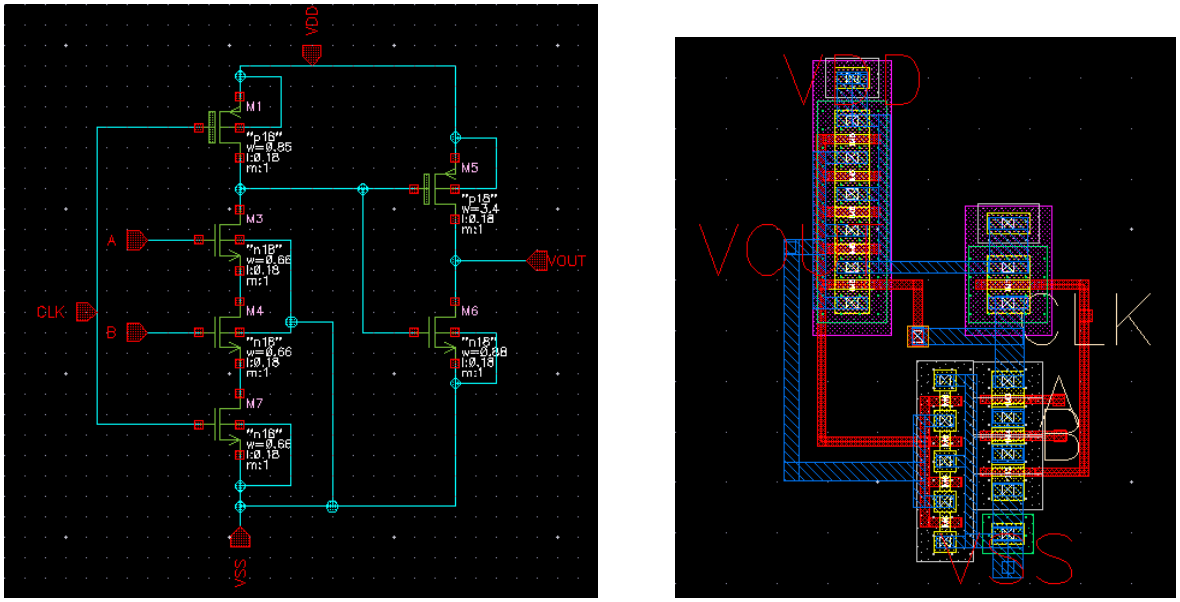
Inverter Parameter γ $\left(\frac{W_p}{W_n}\right)$ is chosen to get nearly equal rise time and fall time under Typical-Typical process corner (SCL).

Table 1: Design

Parameter	Value
P-MOS Gate Width W_p	0.85 μm
P-MOS Gate Length L_p	0.18 μm
N-MOS Gate Width W_n	0.22 μm
N-MOS Gate Length L_n	0.81 μm

Generate using Domino logic

Design and Layout

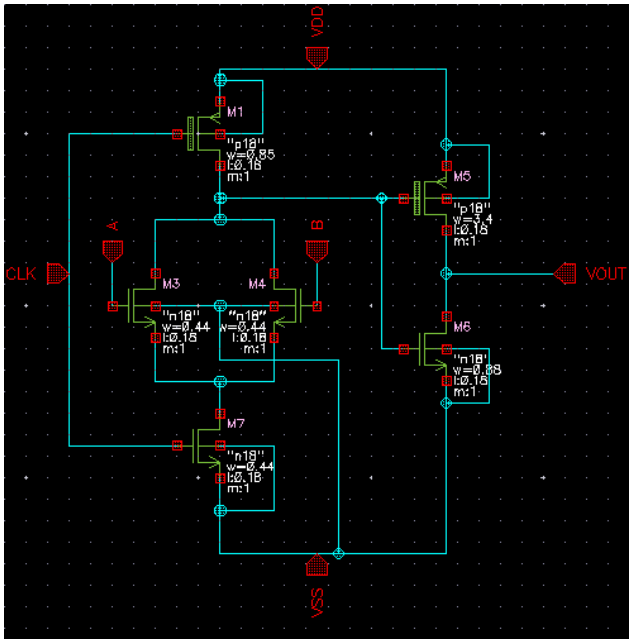


(a) Schematic (b) Layout

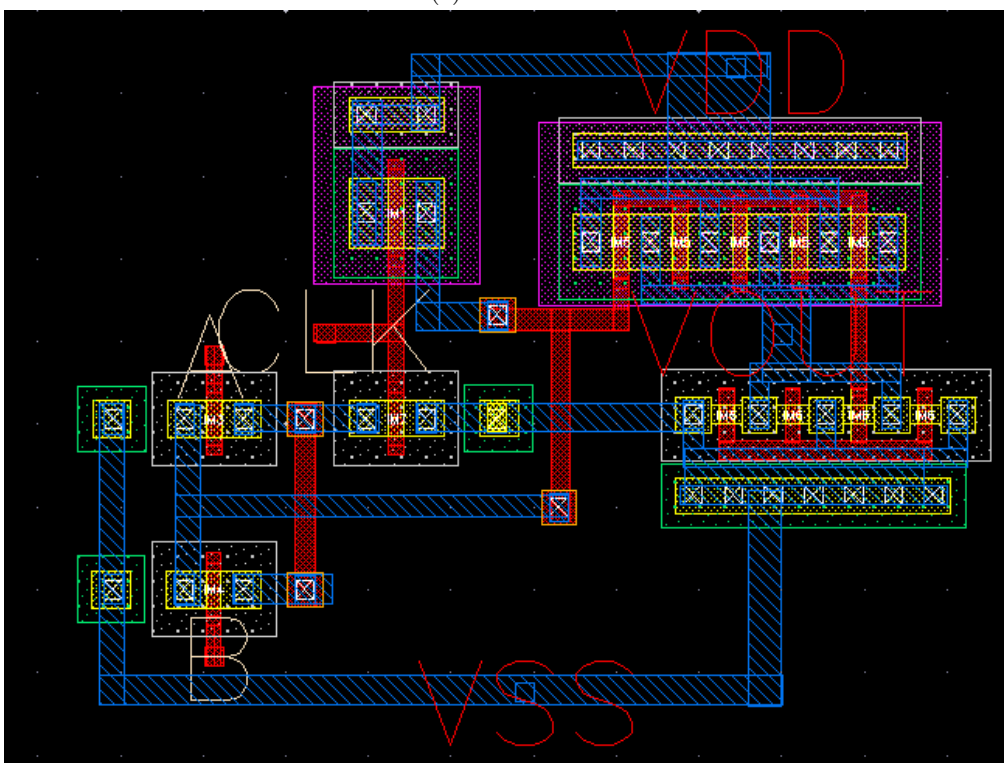
Figure 2: Generate using domino logic

Propagate using Domino logic

Design and Layout



(a) Schematic

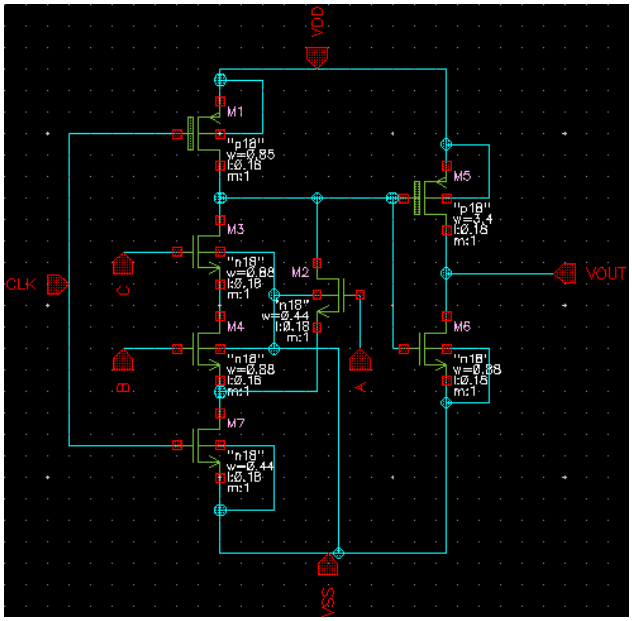


(b) Layout

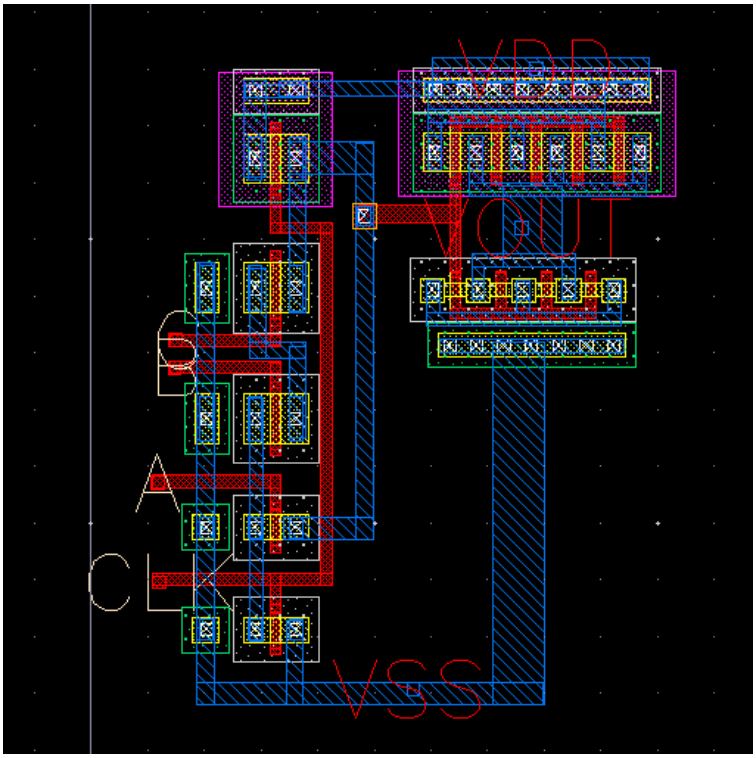
Figure 3: Propagate using domino logic

Carry Generator

Design and Layout



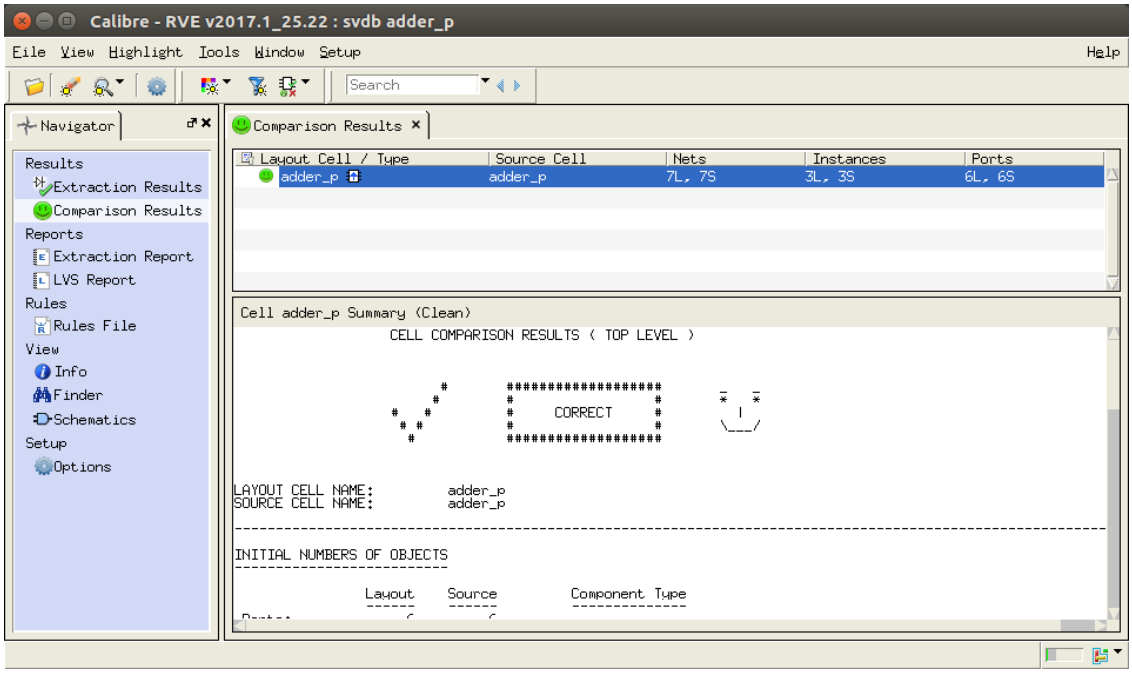
(a) Schematic



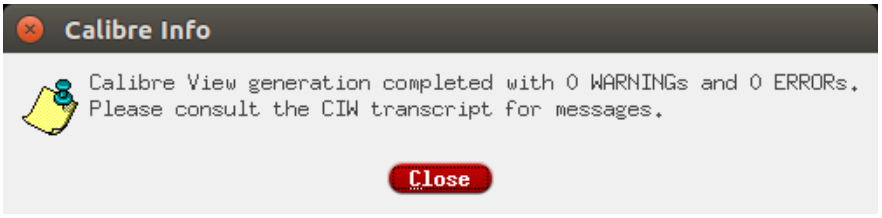
(b) Layout

Figure 4: Carry Generator

LVS and PEX generation



(a) LVS report



(b) PEX generation

Figure 5: Carry Generator

Test Bench Simulation

For the following simulation, time period of clock and input signal is 1 ns.

Generate

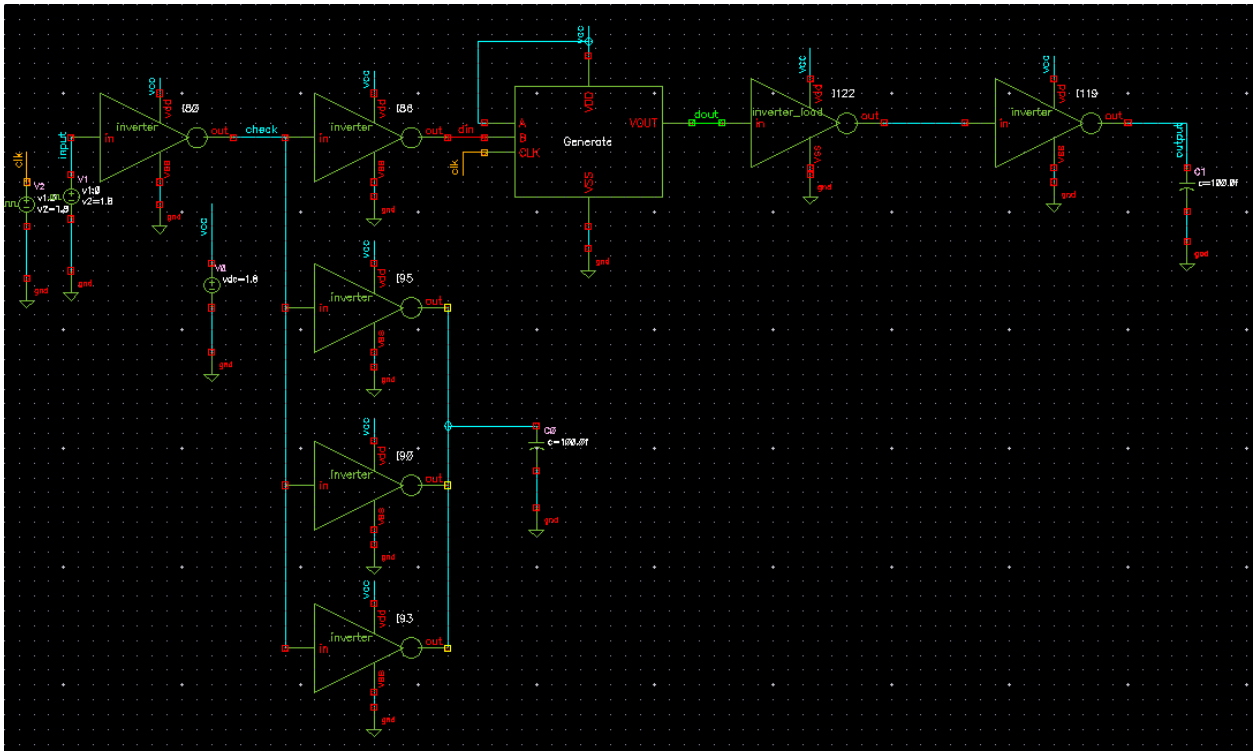


Figure 6: Generate

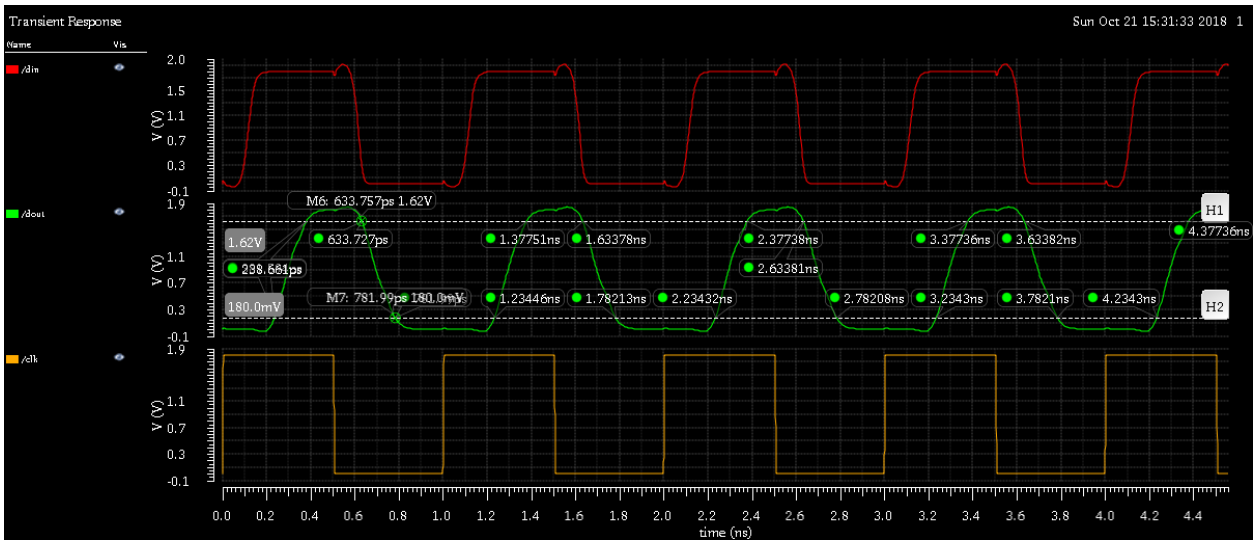


Figure 7: Generate

Table 2: Calculation of generate delay

Parameter	Value
Rise Time	141.339 *ps*
Fall Time	148.223 *ps*

Propagate

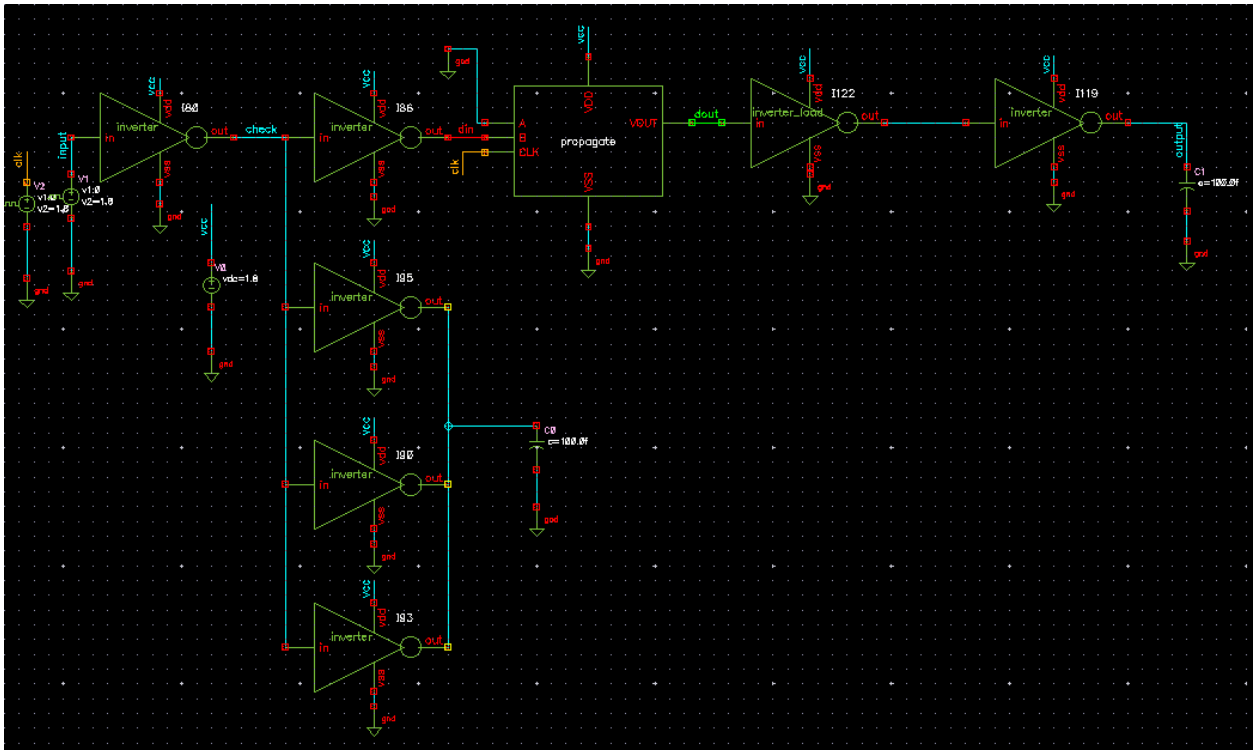


Figure 8: Test Bench

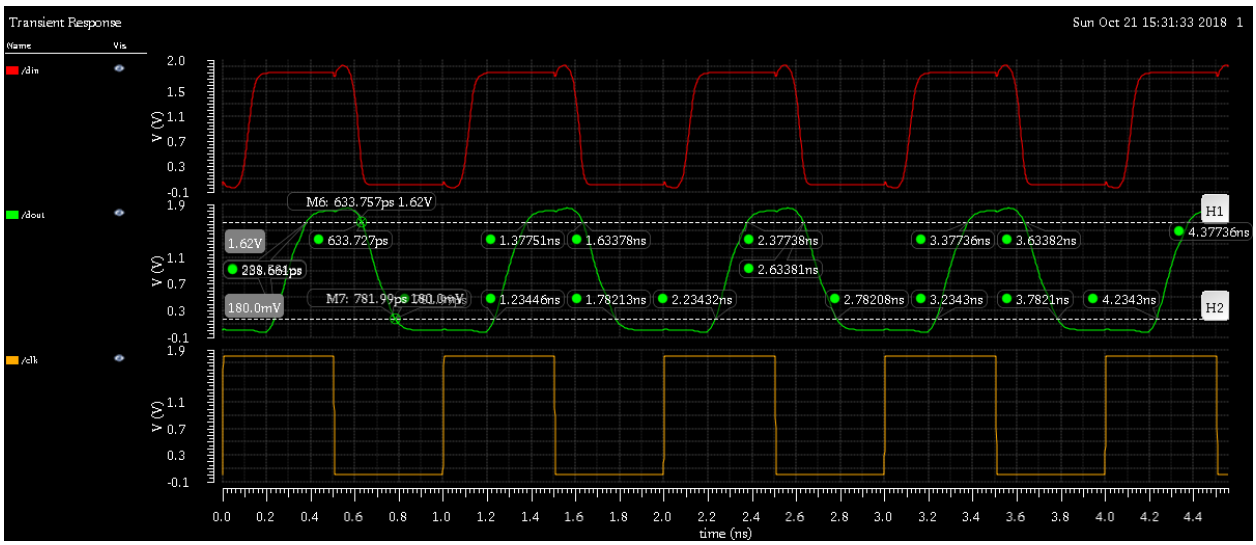


Figure 9: Delay

Table 3: Calculation of propagate delay

Parameter	Value
Rise Time	141.651 *ps*
Fall Time	145.575 *ps*

Carry Out

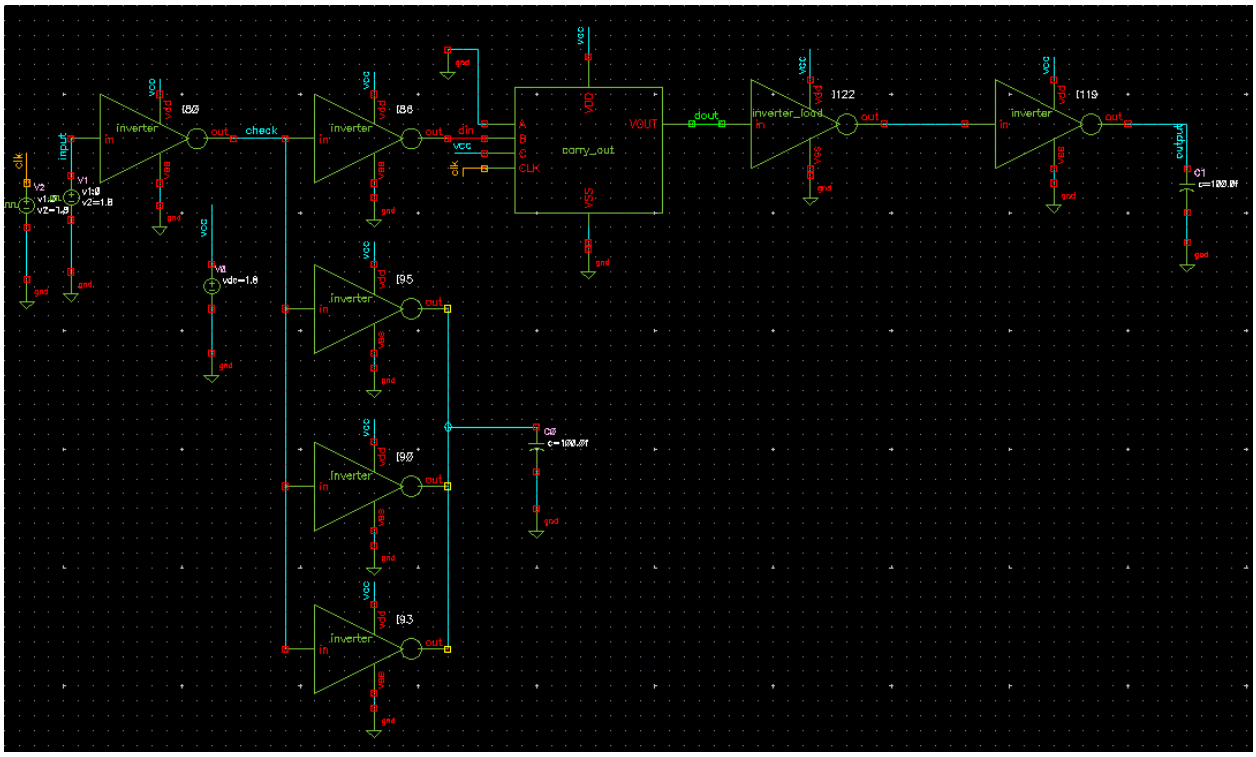


Figure 10: Test Bench

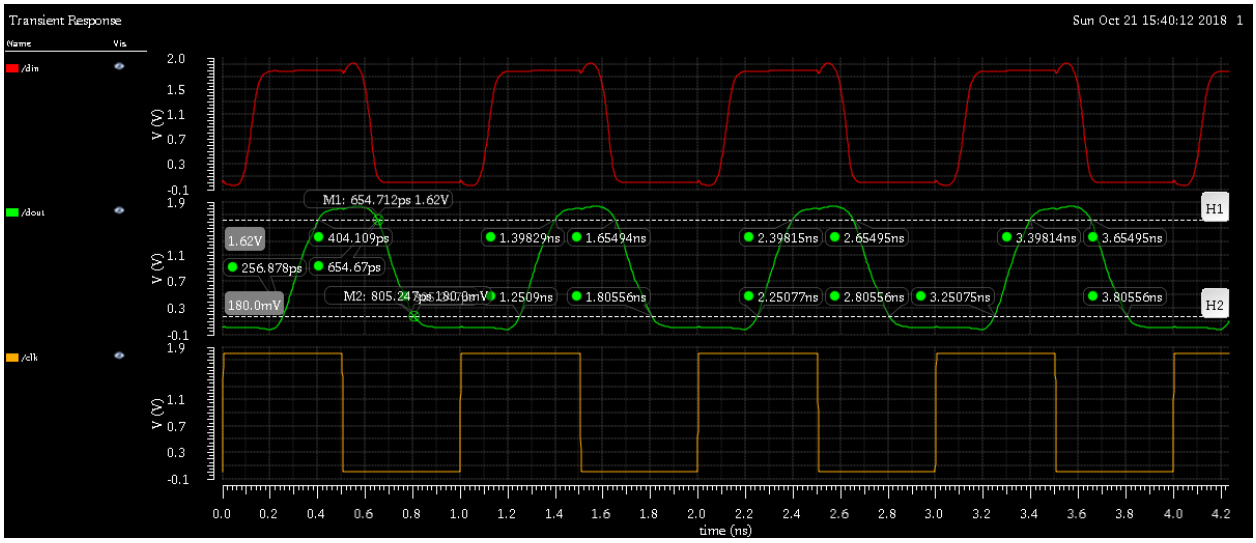


Figure 11: Delay

Table 4: Calculation of carry delay

Parameter	Value
Rise Time	144.231 *ps*
Fall Time	150.529 *ps*

VHDL Simulation

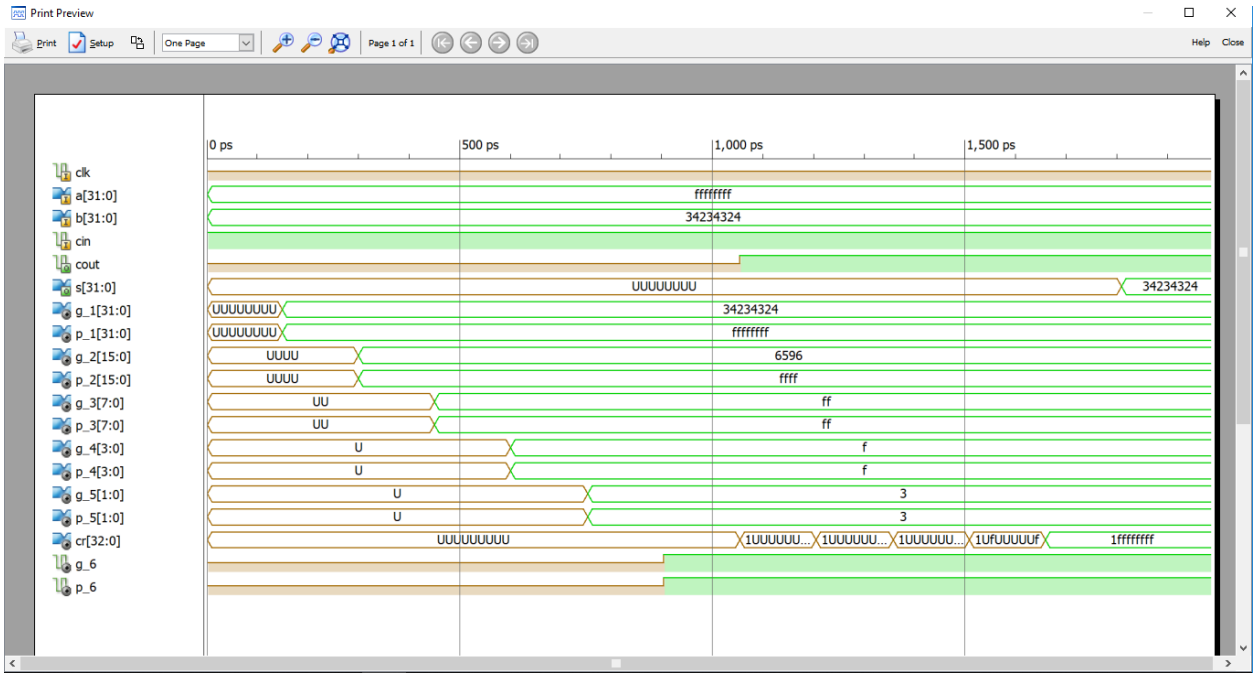


Figure 12: simulation Result

The clock frequency calculated is:301.38 Mhz The maximum delay to generate the sum is 1659 ps.