VLSI Design

Dadda Multiplier 8 × 8
EE 671 : Assignment #4

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November 12, 2018

Dadda Reduction

Dadda Multiplier 8 × 8 reduction is shown in the following Figure 1. Table represent the number of half adder and full adder required to implement this multiplier.

Table 1: Number of adder

Adder	Number
Full Adder	48
Half Adder	8

Given delay

As per the given in the Assignment problem statement.

Table 2: Delay parameter

Adder	Sum Delay	Carry Delay
Full Adder	120 ps	80 ps
Half Adder	70 ps	40 ps
MUX	—	50 ps

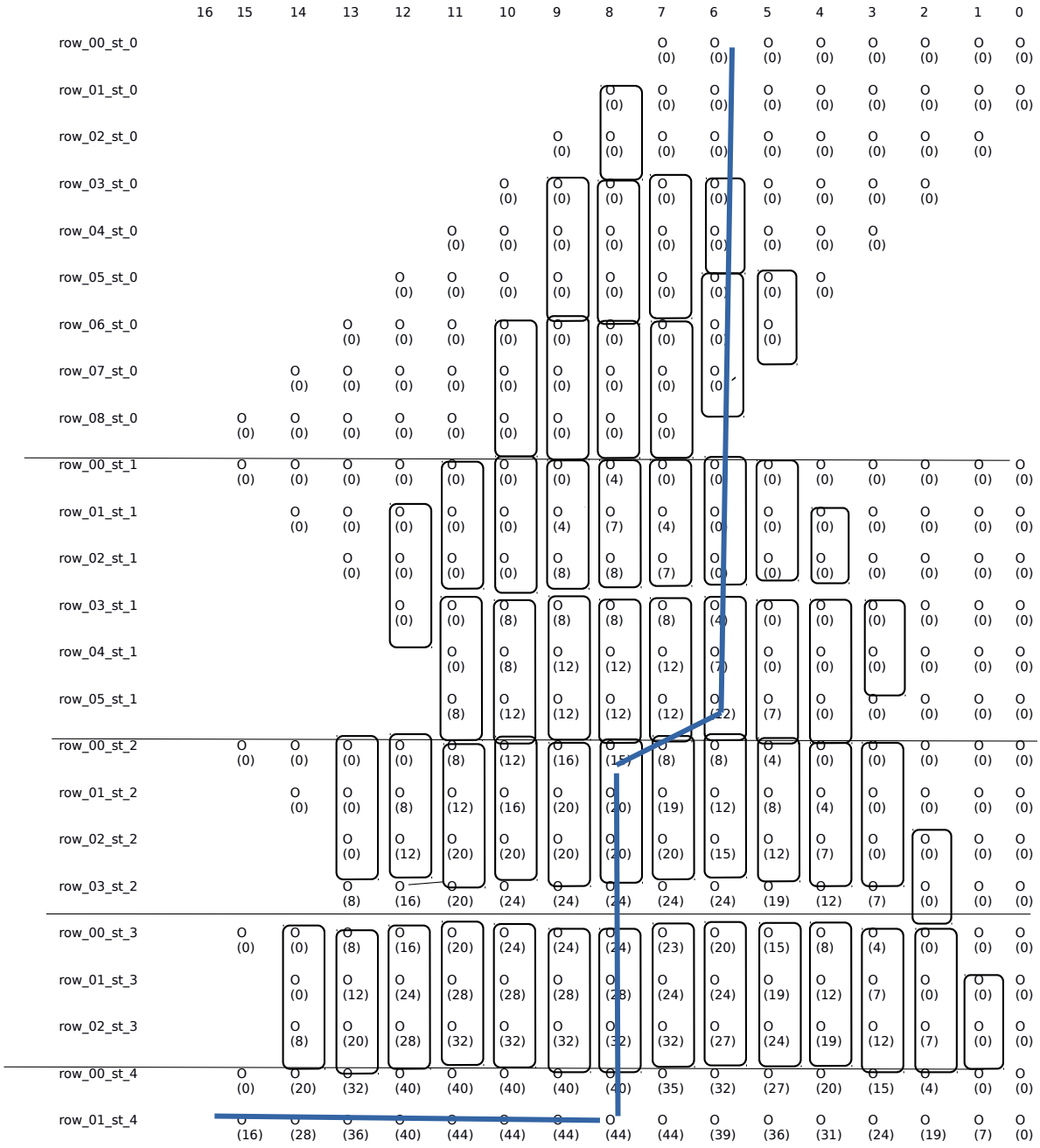

Figure 1: Dadda multiplier

Simulation Result

Result Shown in the below figure is tested by applying the input (FF $\times FF$) + 0F0F = 10D10. The complete result is available at 810 ps

Observation

I have tested the code on different test vector to check the delay model. The worst delay i was finding on the following case:
(FF $\times 0F$) + 00FF = 000F0 - 910 ps

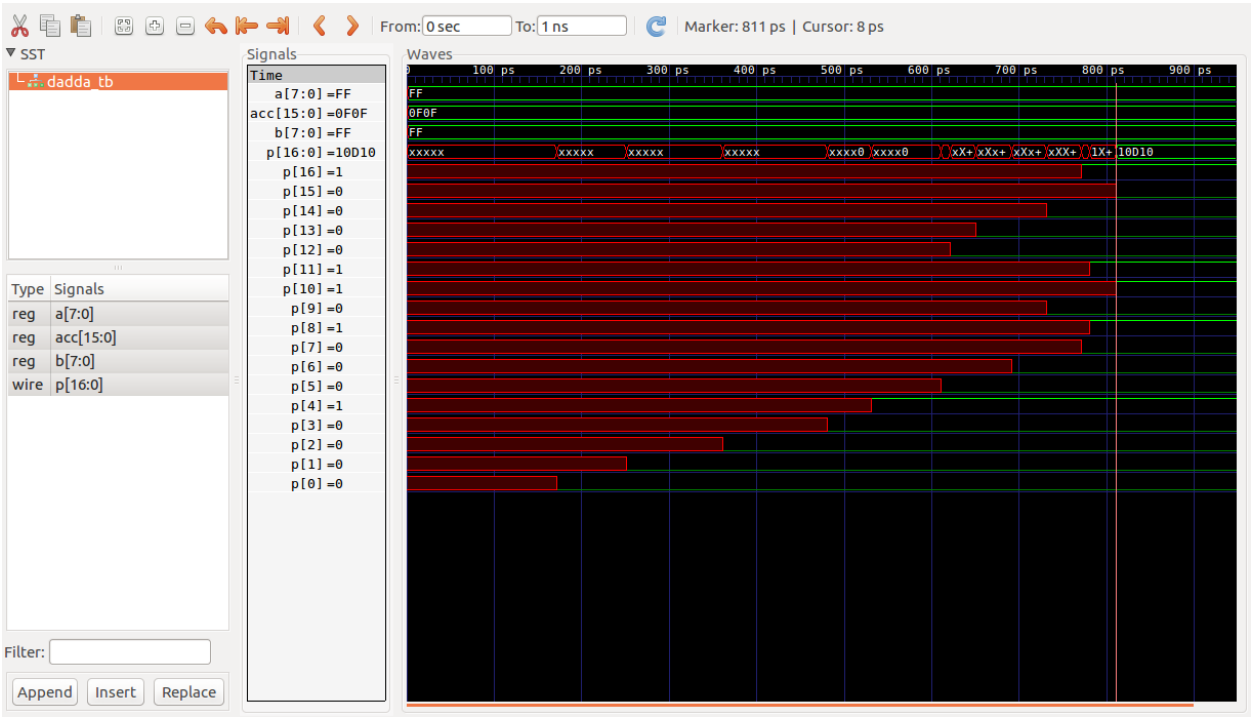

Figure 2: Dadda Multiplier Simulation