PMAP Comparison Model

Data and Results

April 2022

Politecnico di Torino

Contents

Chapter 1

Introduction

This is an accompanying document of the following manuscript

title *Architectural Comparison Model for Area-Efficient PMAP Turbo-Decoders*
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submitted to IEEE Transactions on Circuits and Systems II: Express Briefs.

The document reports data extracted from the area efficiency model available in the following repository:
https://github.com/simomaiden/turbo_dec_aeff.

Chapter 1 presents results obtained by exploring a given architectural space, considering different Frame Sizes, Sub Frame Sizes and Window Sizes. The focus is to analyze the consequences on the selection of radix-orders capable of maximizing the area efficiency of the decoder. The analysis is repeated, considering both Ripple-Carry and Carry-Look-Ahead logic for the adders implementation. Chapter 2 includes various interesting results, extracted from several model's analysis, as well. All the presented estimations are based on estimations derived for the 65 nm technology, which have been used to tune the model.

Chapter 2

Efficient Radix-Orders

A total of 48 architectures are explored, by combining different Frame Sizes (K), Sub Frame Sizes (Kp) and Windows Sizes (WS), included in the following ranges:

- K = [2048, 4096, 6144]
- Kp = [128, 256, 384, 512]
- WS = [32, 64, 96, 128]

The first section refers to results achieved by assuming the usage of Ripple-Carry based logic. The second section considers of Carry-Look-Ahead logic instead. The mentioned sections are similarly structured: first, the selection of the most efficient radix-orders is remarked. Then, consequences on various parameters are analyzed, including throughput, latency, area, area efficiency and power.

2.1 Ripple-Carry Logic

The following 3D graphical representation shows the radix-orders selected by the model, in order to maximize the area efficiency. Each marker represents an architecture, given the values of K, Kp and WS. The color of the marker reflects the choice on the radix-order. In order to simplify the visualization, the 3D-plot has been sliced in 3 2D-plots on the right, considering planes with constant Frame Sizes (K). As visible, just radix-2 and radix-4 architectures have been selected.

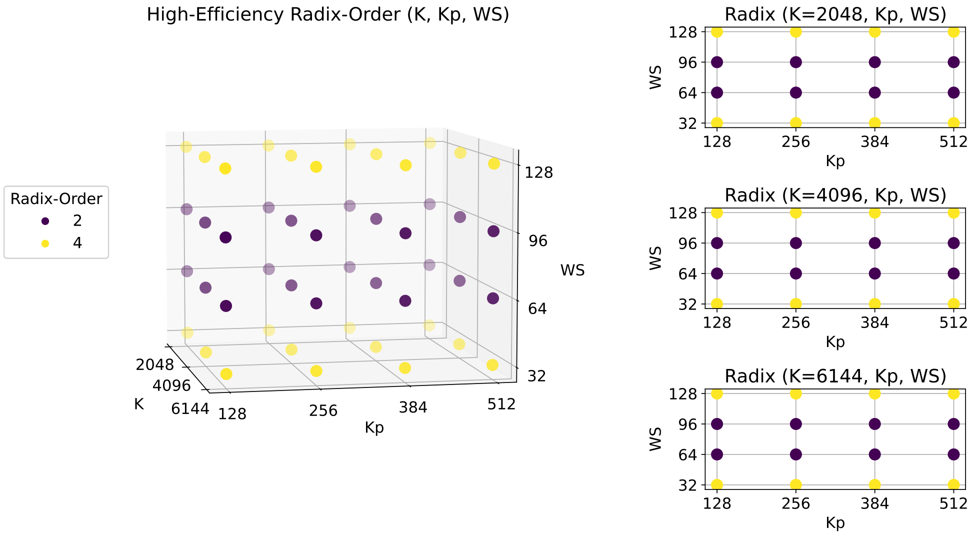

Figure 2.1: Most efficient radix-order selection.

2.1.1 Throughput

The following parametric plots depict the throughput results obtained following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. Throughput is defined as the amount of decoded bits per unit time, and it is measured in [Gb/s].

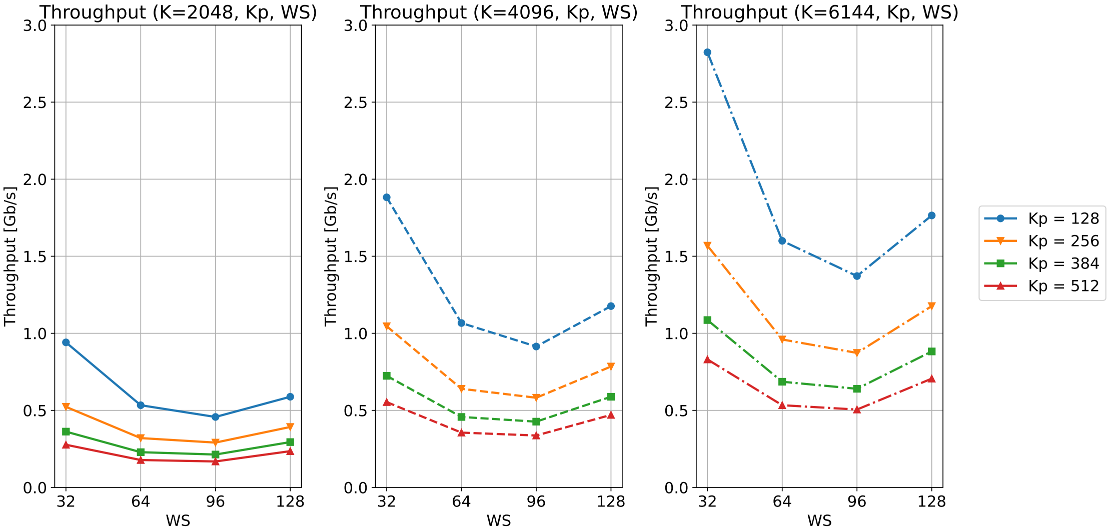

Figure 2.2: Throughput distribution after selecting the most efficient radix-orders.

2.1.2 Latency

The following parametric plots depict the latency results obtained following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. Latency is defined as the amount of time required to decode a single information frame. It is measured in [us].

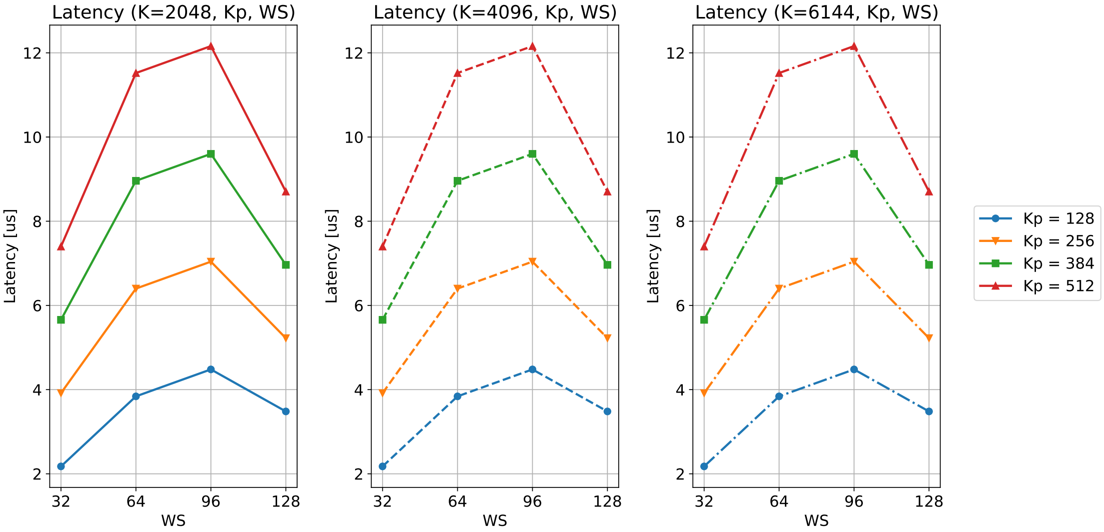

Figure 2.3: Latency distribution after selecting the most efficient radix-orders.

2.1.3 Area

The following parametric plots depict the area results obtained following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. The total decoder area, measured in [mm^2], includes the contribution of both logic and memory.

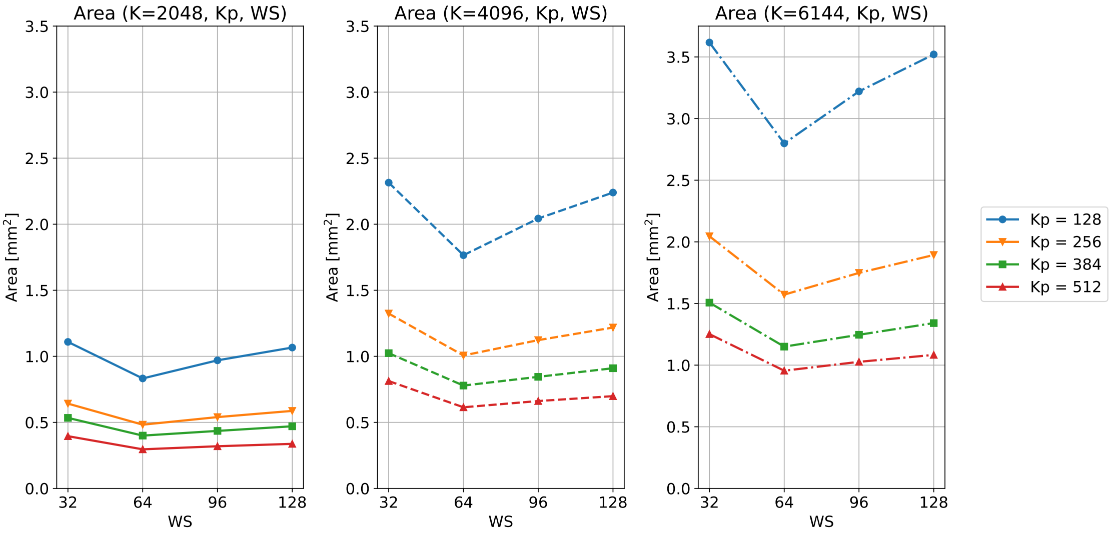

Figure 2.4: Area distribution after selecting the most efficient radix-orders.

2.1.4 Area Efficiency

The following parametric plots depict the area efficiency results obtained following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. Area efficiency is defined as the ratio between the achieved throughput and the total area, and it is measured in [Gb/s/mm^2]. It is the quantity maximized during the radix-order selection.

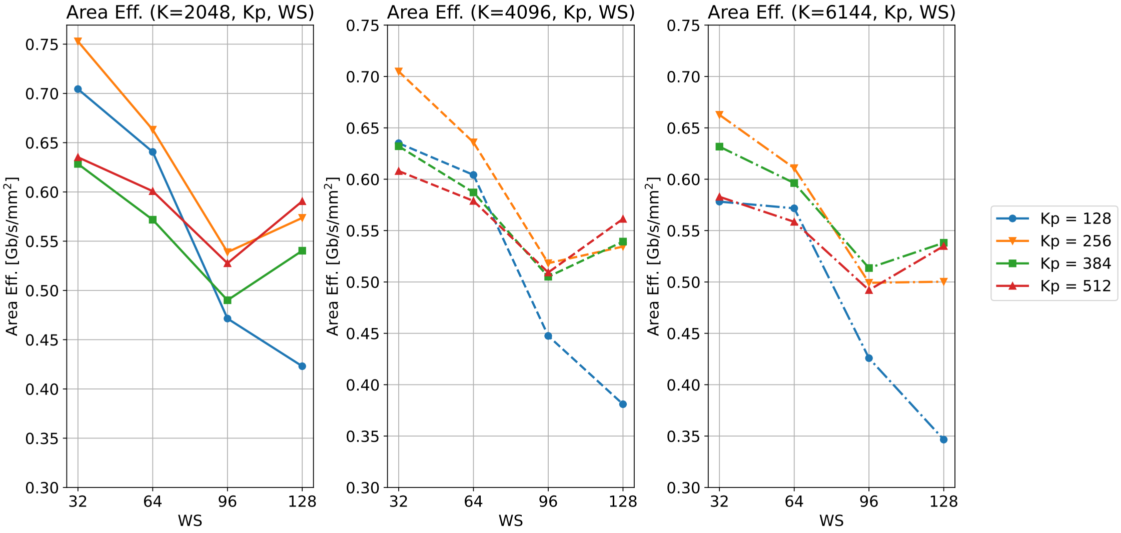

Figure 2.5: Area efficiency distribution after selecting the most efficient radix-orders.

2.1.5 PMAP Number on 10mm^2

The following parametric plots depict the number of available PMAP-Decoders in a 10mm^2 area, following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. This result comes from the need to parallelize the architecture, relying on its area efficiency, to look for high-throughput solution. The larger the available area, the larger the throughput benefits from increasing the area efficiency of a single PMAP-Decoder.

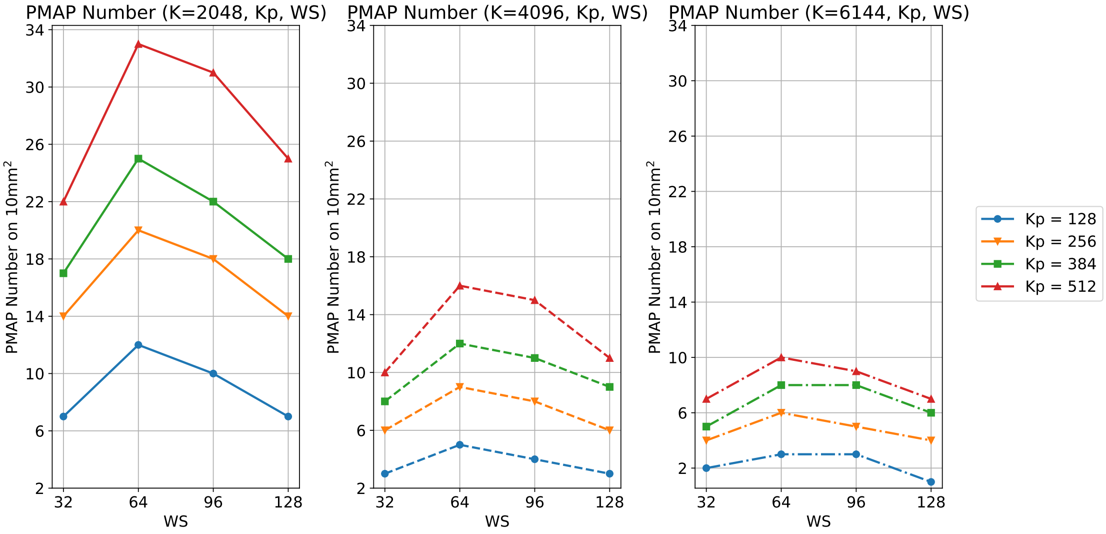

Figure 2.6: Number of PMAP processors after selecting the most efficient radix-orders.

2.1.6 Available Throughput on 10mm^2

The following parametric plots depict the available throughput on parallel PMAP-Decoders on a 10mm^2 area, following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. Also in this case, the throughput is measured in [Gb/s]. These results are a direct consequence of the computation presented in Figure 2.6.

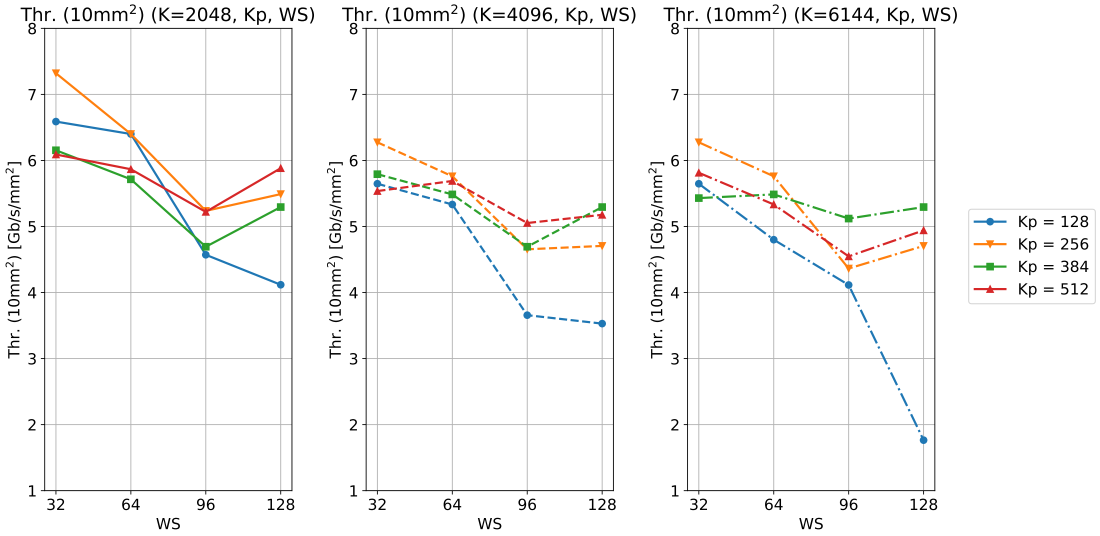

Figure 2.7: Throughput on 10mm^2 after selecting the most efficient radix-orders.

2.1.7 Power

The following parametric plots depict the power results, following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. Power, measured in [W], is estimated using a high-level model, which considers variations in working clock frequency and total area.

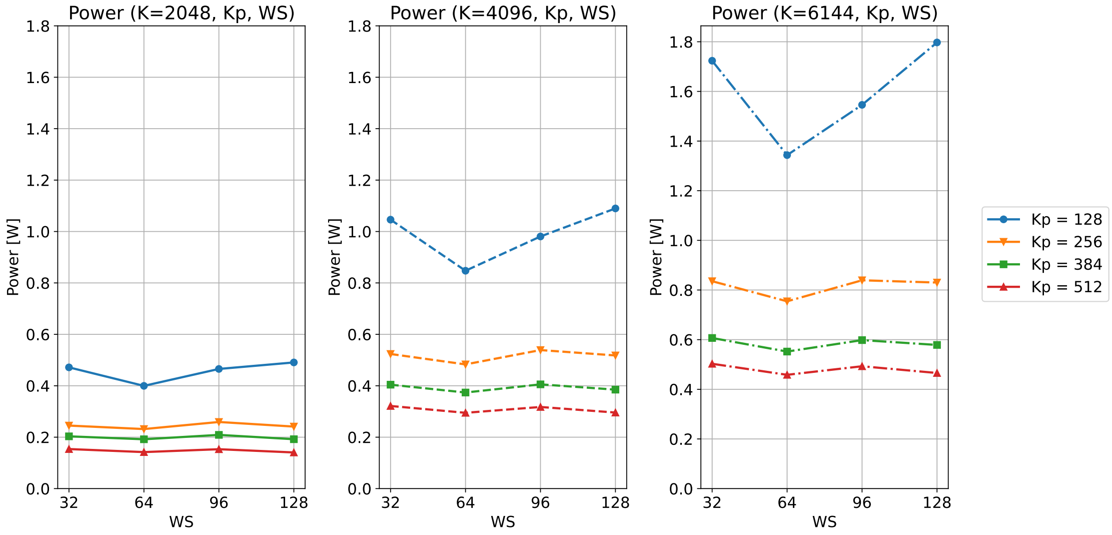

Figure 2.8: Power distribution after selecting the most efficient radix-orders.

2.2 Carry-Look-Ahead Logic

The following 3D graphical representation shows the radix-orders selected by the model, in order to maximize the area efficiency. Each marker represents an architecture, given the values of K, Kp and WS. The color of the marker reflects the choice on the radix-order. In order to simplify the visualization, the 3D-plot has been sliced in 3 2D-plots on the right, considering planes with constant Frame Sizes (K). As visible, just radix-2 and radix-4 architectures have been selected.

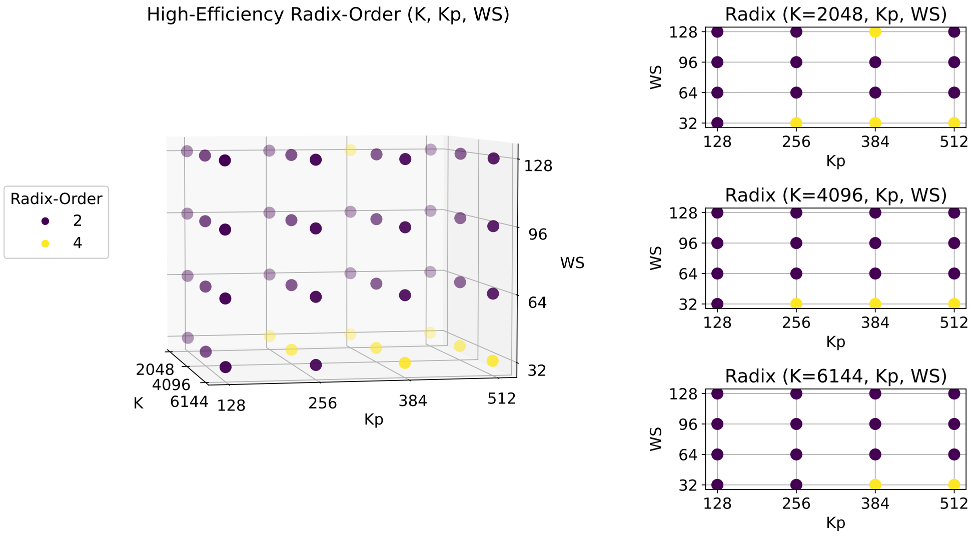

Figure 2.9: Most efficient radix-order selection.

2.2.1 Throughput

The following parametric plots depict the throughput results obtained following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. Throughput is defined as the amount of decoded bits per unit time, and it is measured in [Gb/s].

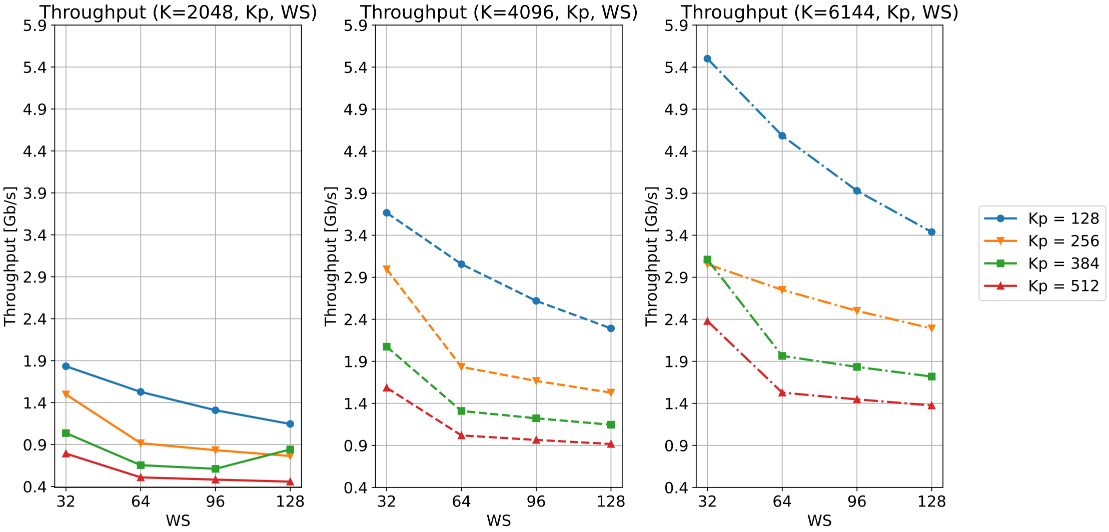

Figure 2.10: Throughput distribution after selecting the most efficient radix-orders.

2.2.2 Latency

The following parametric plots depict the latency results obtained following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. Latency is defined as the amount of time required to decode a single information frame. It is measured in [us].

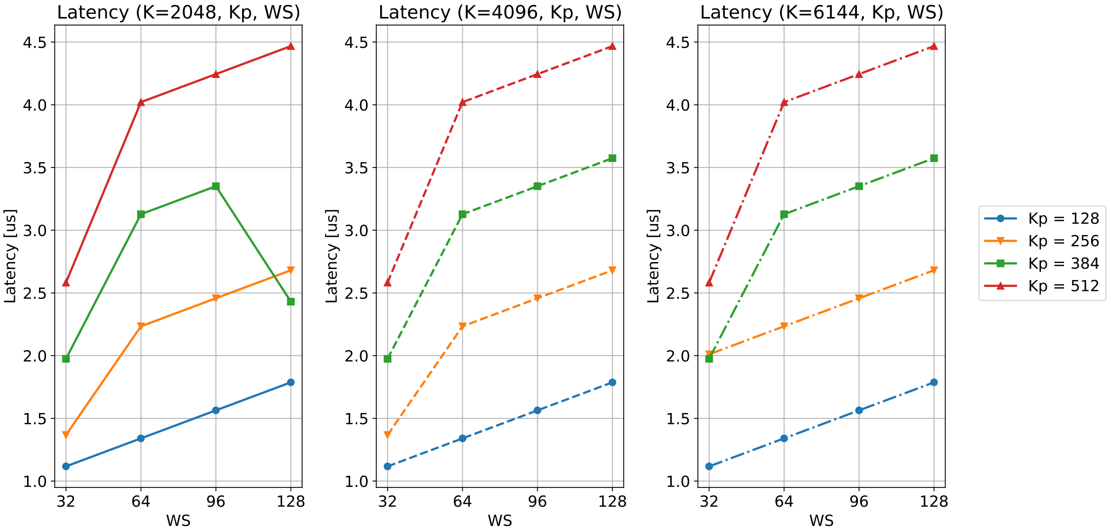

Figure 2.11: Latency distribution after selecting the most efficient radix-orders.

2.2.3 Area

The following parametric plots depict the area results obtained following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. The total decoder area, measured in [mm^2], includes the contribution of both logic and memory.

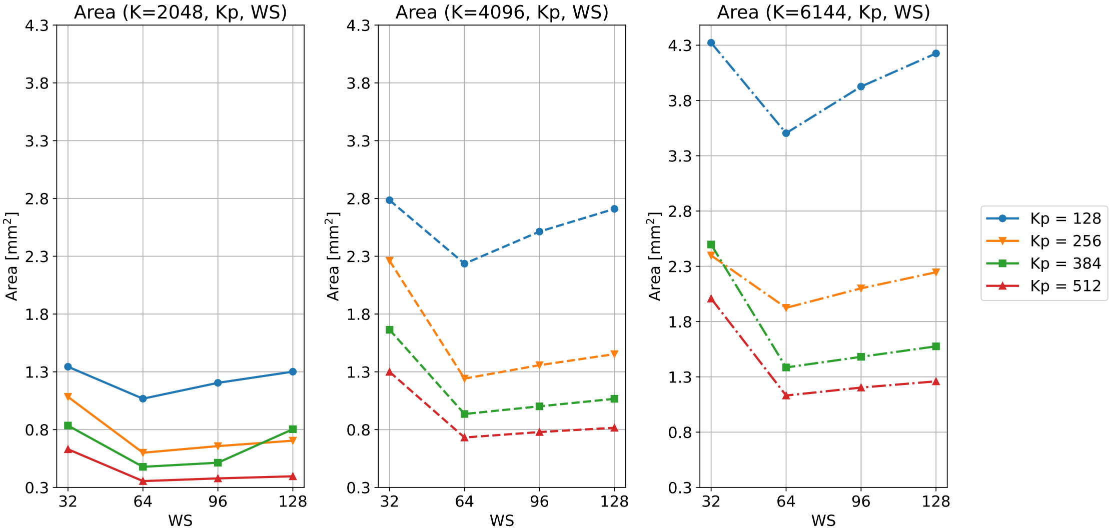

Figure 2.12: Area distribution after selecting the most efficient radix-orders.

2.2.4 Area Efficiency

The following parametric plots depict the area efficiency results obtained following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. Area efficiency is defined as the ratio between the achieved throughput and the total area, and it is measured in [Gb/s/mm^2]. It is the quantity maximized during the radix-order selection.

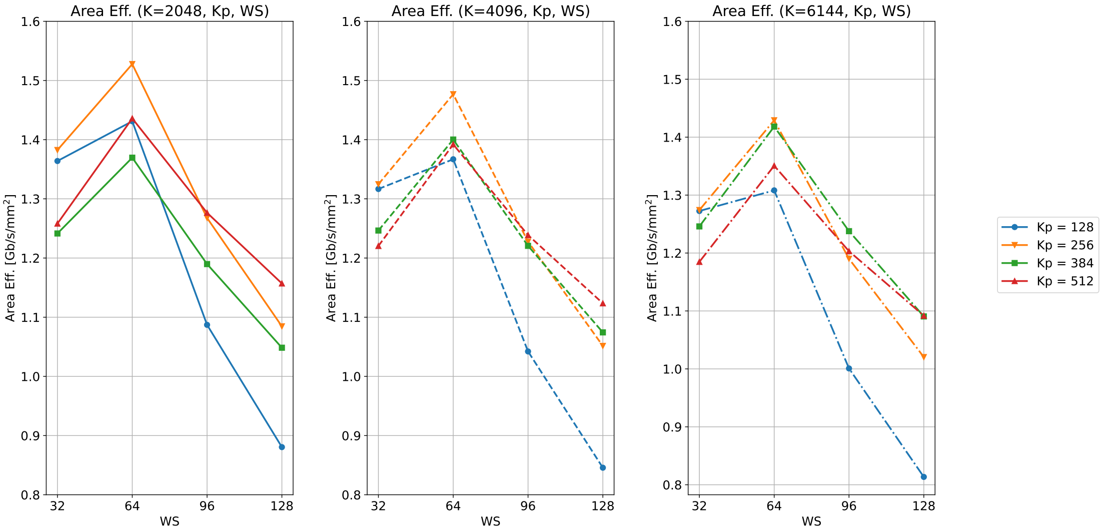

Figure 2.13: Area efficiency distribution after selecting the most efficient radix-orders.

2.2.5 PMAP Number on 10mm^2

The following parametric plots depict the number of available PMAP-Decoders in a 10mm^2 area, following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. This result comes from the need to parallelize the architecture, relying on its area efficiency, to look for high-throughput solution. The larger the available area, the larger the throughput benefits from increasing the area efficiency of a single PMAP-Decoder.

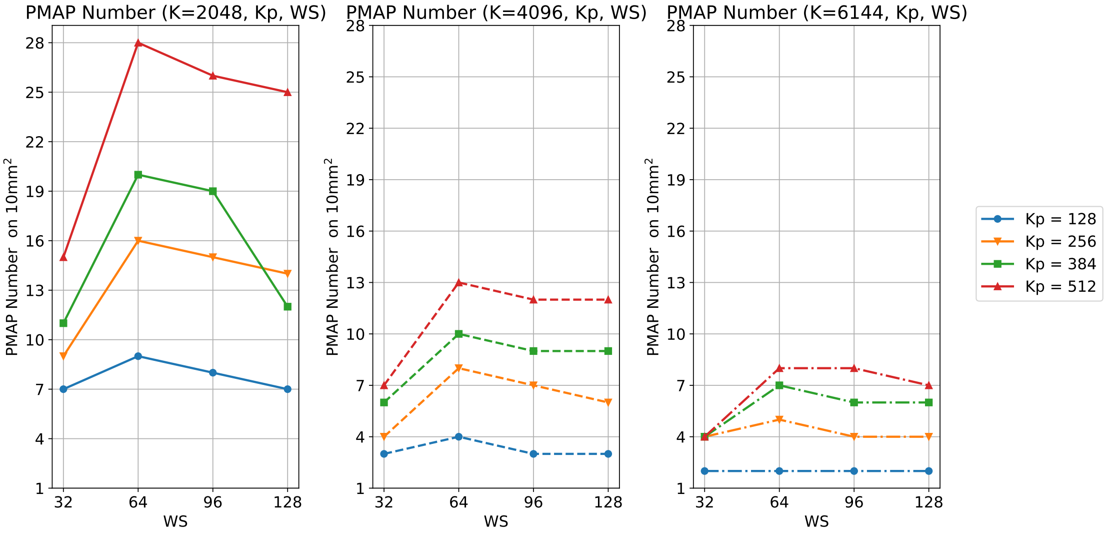

Figure 2.14: Number of PMAP processors after selecting the most efficient radix-orders.

2.2.6 Available Throughput on $10mm^2$

The following parametric plots depict the available throughput on parallel PMAP-Decoders on a $10mm^2$ area, following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. Also in this case, the throughput is measured in [Gb/s]. These results are a direct consequence of the computation presented in Figure 2.6.

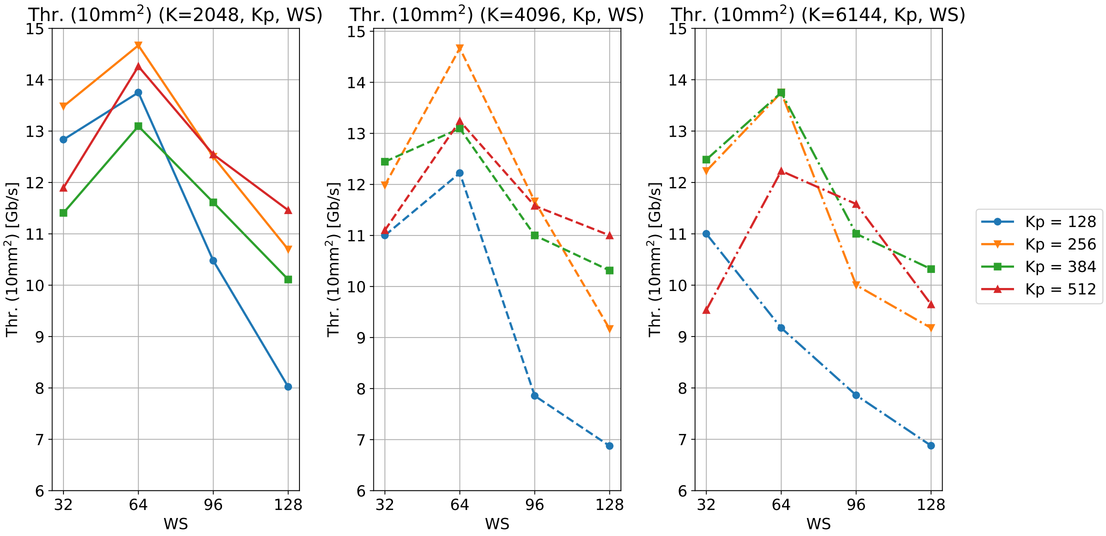

Figure 2.15: Throughput on $10mm^2$ after selecting the most efficient radix-orders.

2.2.7 Power

The following parametric plots depict the power results, following the radix-order selection presented in Figure 2.1. Each plot is related to a specific Frame Size (K). The Sub Frame Size (Kp) variation is parametric, using different colors. Different Window Sizes (WS) can be found on the horizontal axis. Power, measured in [W], is estimated using a high-level model, which considers variations in working clock frequency and total area.

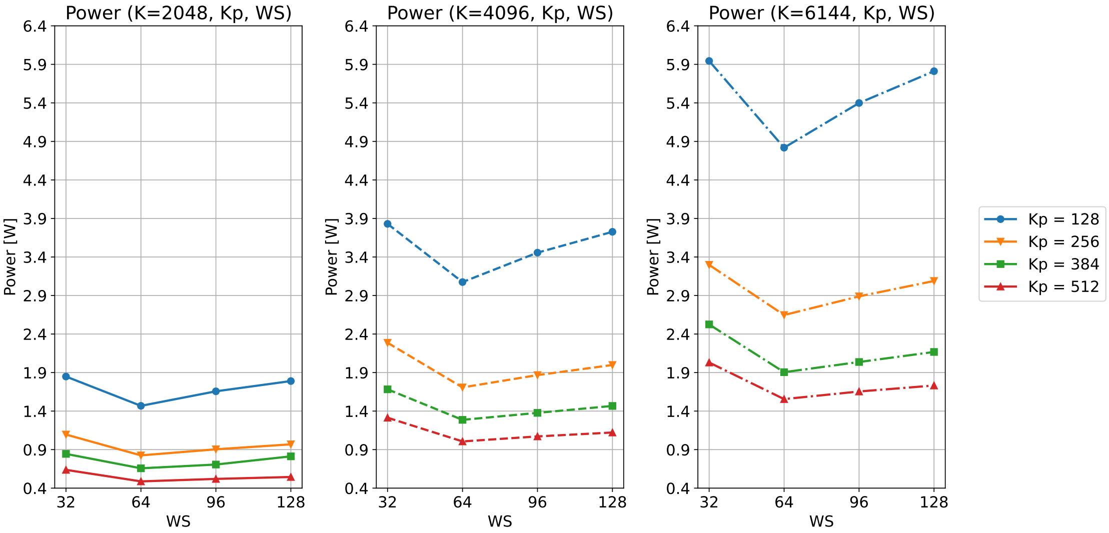

Figure 2.16: Power distribution after selecting the most efficient radix-orders.

Chapter 3

Additional Data

3.1 Latency on different radix-orders

The following parametric plots include latency estimations on different radix-orders and Window Sizes (WS), while fixing the Frame Size (K) to 6144 and the Sub Frame Size (Kp) to 384. Furthermore, results are generated on both Ripple-Carry logic and Carry-Look-Ahead logic, with the purpose of comparing the effects of the two implementations.

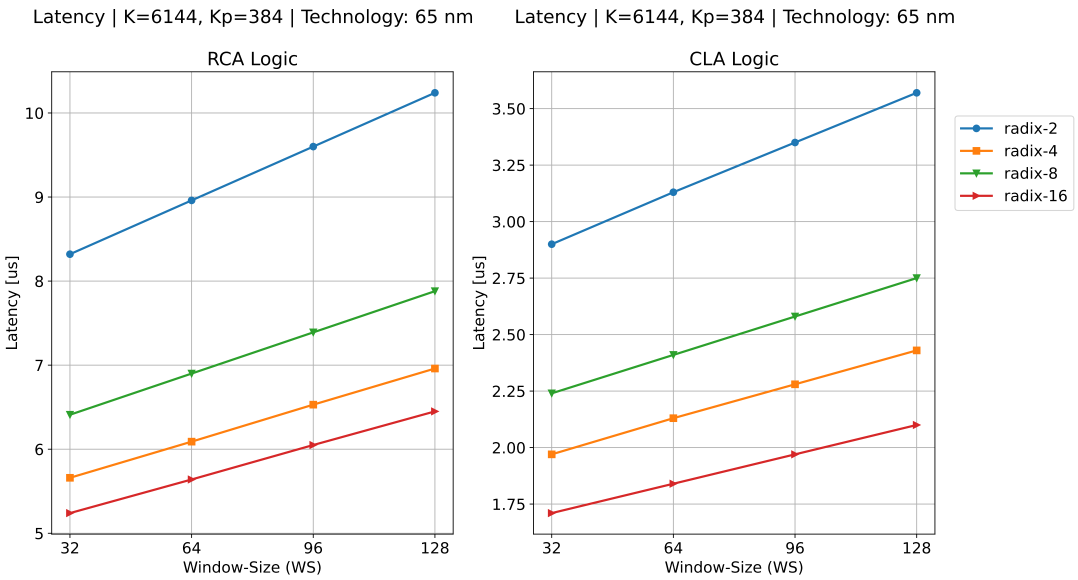

Figure 3.1: Latency distribution across different radix-orders and window-sizes.

3.2 Typical Logic and Memory Area Distributions

The following tables include statistics about the logic and memory area distributions in a typical PMAP-Decoder implementation, with Frame Size equal to 6144, Sub Frame Size equal to 256 and Window Size equal to 32. Moreover, a radix-4 implementation has been selected. A bried explanation of the reported labels is provided:

- BMU: Branch Metric Unit.
- PMU: Path Metric Unit.
- SOU: Soft Output Unit.
- Input Frame: Memory to store the Input Frame LLRs.
- Extr. Inf.: Memory to store the computed extrinsic information.
- Permutation: Memory to store the permutation law addresses.
- Alpha: Memory to store the computed Alpha Metrics, during the forward propagation.
- NII: Memory to store Beta Metrics in order to apply the Next Iteration Initialization technique.

Library memory models (*Library*) and synthesis mappings (*Synthesis*) have been considered for memory implementations.

Log. Unit	**% $\mathbf{A_L}$**
BMU	9%
PMU	61%
SOU	30%

Memory	**Model**	**% $\mathbf{A_M}$**
Input Frame	*Library*	23%
Extr. Inf.	*Library*	10%
Permutation	*Library*	25%
Alpha	*Synthesis*	28%
NII	*Synthesis*	14%

Table 3.1: Logic and Memory area distributions in a typical architecture.