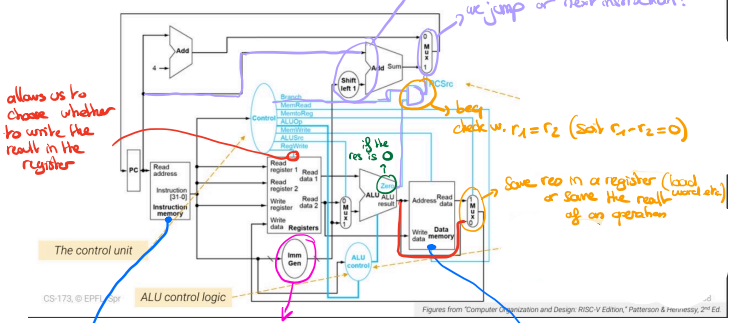
Adding the Control Unit



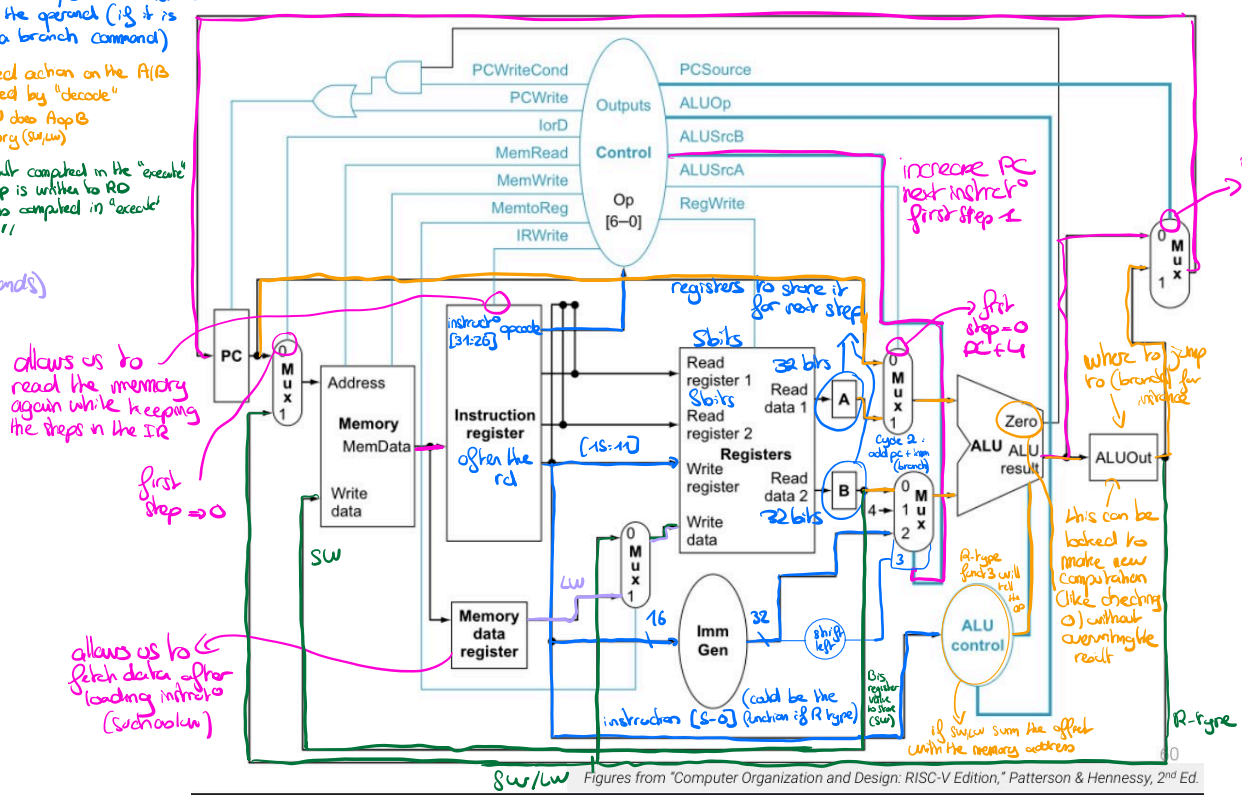
does the sign extension when needed (rs1 ∧ sext(imm))

Harvard architecture instruct° ≠ data

MULTI CYCLE

5 instruct°

- fetch: get the steps for the current instruction and put them into the instruction register (IR)
- decode: retrieve registers values / decode instruction + sign-extend the operand (if it is a branch command)
- execute: do the required action on the A/B values retrieved by "decode"
  - R-type: ALU does A op B
  - Accessing memory (sw, lw)
- memory: R-type: result computed in the "execute" step is written to RD
  sw: address computed in "execute"
  lw: //
- write back (only for load commands) write to the registers



allows us to fetch data after loading instruct° (sw/load w)