(a)

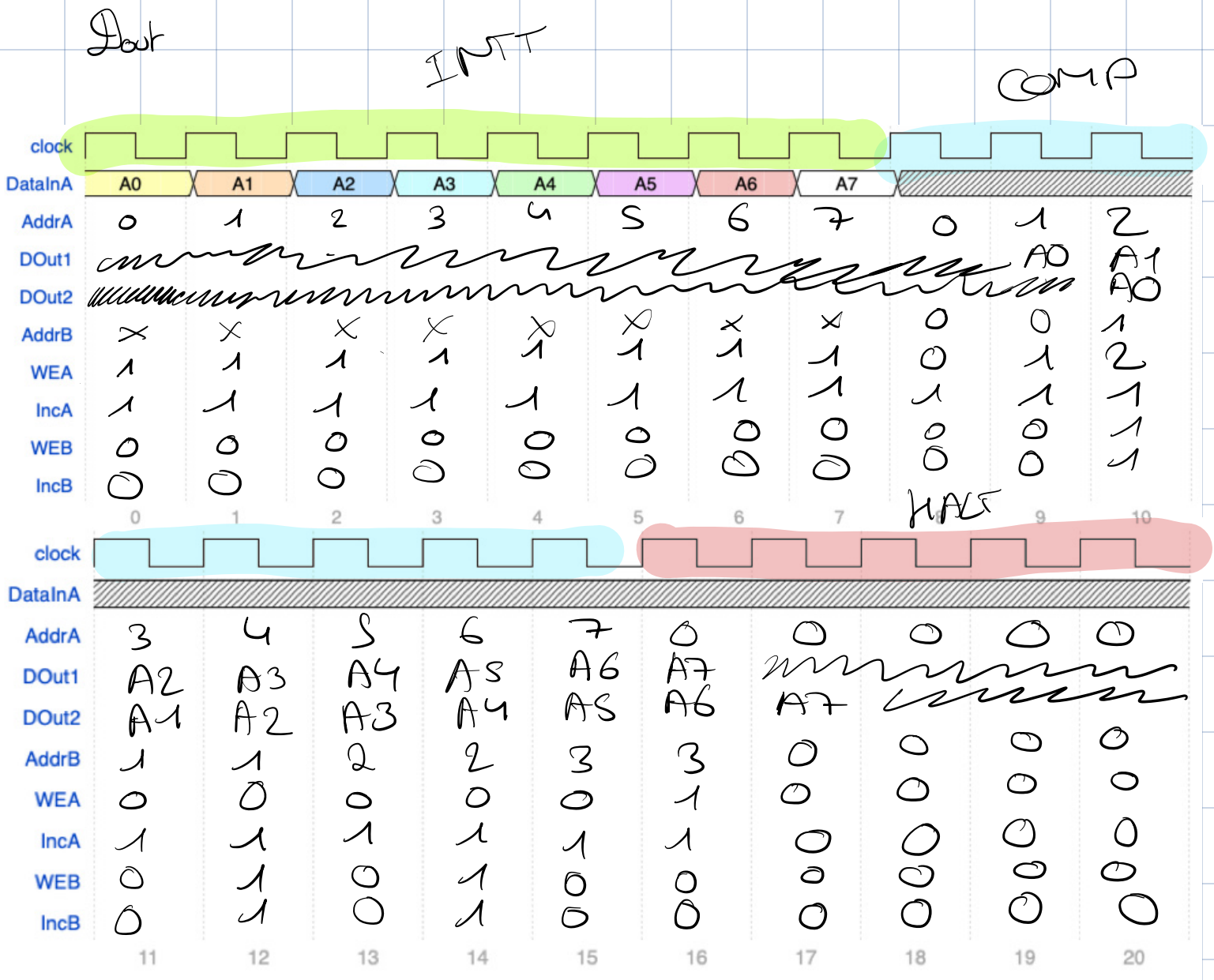
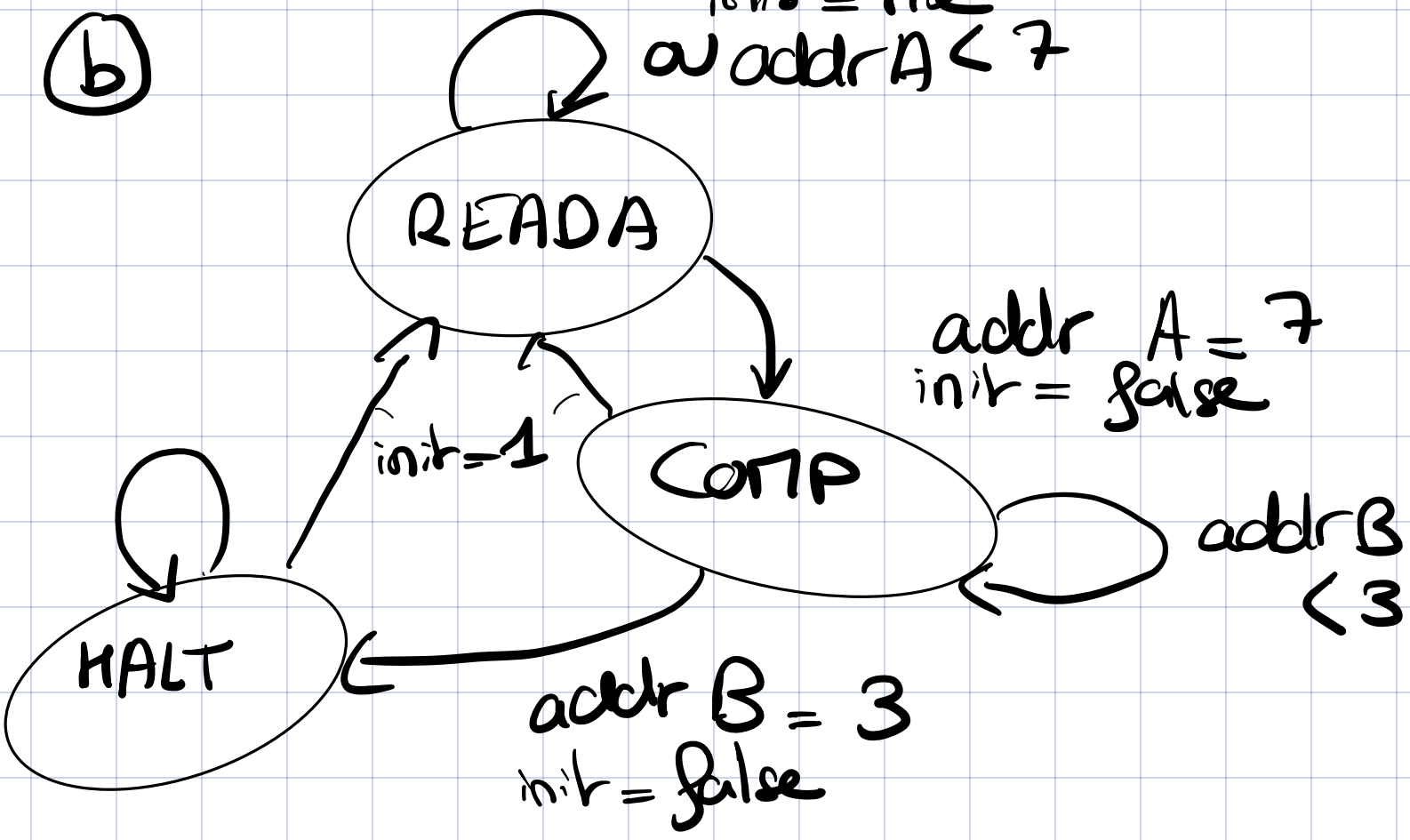


Figure 2: Timing diagram for the memory processing design.

(b)



(c)

		init = 1		init = 0
		A0		A7
		B3	$\overline{B3}$	B0
READA	READA	R	R	C
COMP		H	C	C
HALT		H	H	H