CSE460L: Assignment 0 (Fall 2021)

Sections: 1, 2, 3, 4, 5, 6, 7, 8 & 9

Assignment 0 submission link:
https://docs.google.com/forms/d/e/1FAIpQLSdilpaOmAXFpEiisj0L-s2mPHnIt9VacSoZxNan3E-pMDKMew/viewform?usp=sf_link

Assignment 0 deadline: **21 Oct, 2021, 4.59 PM (BDT)**

General guidelines

- Assignments are individual

- Each assignment will contain 3 to 4 problems

- **For each problem you will need to prepare 3 parts:**
  1. **Code:** attach a screenshot of your code from Quartus.
  2. **Output: attach *FULL SCREEN* screenshots** of
     - Compilation Report - Flow Summary (Compilation report of the .v file)
     - Simulation Report - Simulation Waveforms (Simulation report of the .vwf file)

  [**Tampered/edited/cropped screenshots will be considered as a violation of general guidelines and therefore will not be accepted**]

  3. **Discussion/Explanation:** explain the output waveforms of your simulation report as described in the **Expected Output** section within each problem statement.

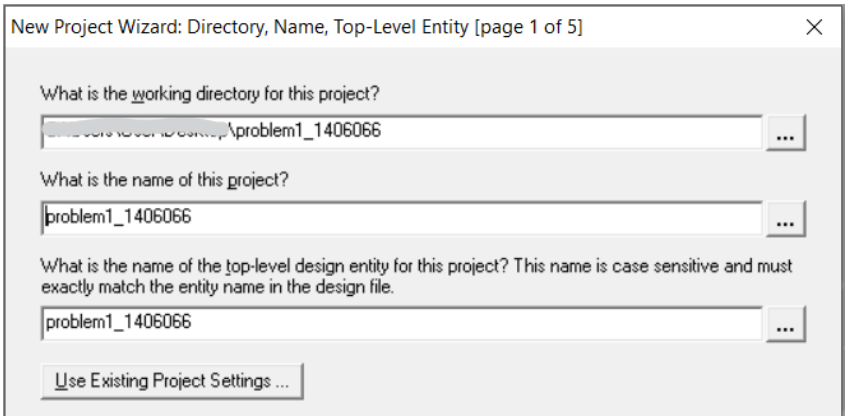
- Each problem will be of equal points. You will not be graded on the length/number of code/explanation/outputs; rather on the clarity, readability and precise explanations of your code/logic/outputs

- Points distribution for each problem is

  Code: **40%**
  Output: **20%**
  Discussion/Explanation of output: **40%**

- **You will need to create separate directories/project for each problem**

- **The name of your working directory for each problem of the assignment should be …\problem#_StudentID [# = 1/2/3/4..]**
  For example, for problem 1 the name of the directory should be problem1_1406066



- Consequently, the name of your main module in the Verilog file should be problem#_StudentID [# = 1/2/3/4..]
  Continuing from the previous example, the name of the module should be problem1_1406066

- Finally, **compile all the problems for a given assignment into a single pdf file**

- The **name of the pdf should be Section_StudentID_assignment0.pdf** (Example: 1_1406066_assignment0.pdf)

Problem for Assignment 0

1. Design the digital logic circuit in Verilog from the following logic expression:

$$Y = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$$

Submit the answers to the following questions (provide necessary simulation outputs where applicable):

(a) Draw the truth table for the logic circuit expressed by the equation above and explain the logic operation performed by the circuit. **[5]**

(b) Assign suitable clocks to the input pins in Verilog to generate all possible input combinations as in the truth table in Q.1(a), perform simulation for 50 ns and show the timing diagram. From the timing diagram, pick the outputs from two randomly selected time instances and crosscheck the input/output values with the truth table in Q.1(a). **[5]**

(c) Assign random values to the input pins in Verilog **at half grid intervals**, perform simulation for 50 ns and show the timing diagram. From the timing diagram, pick the outputs from two randomly selected time instances and crosscheck with the truth table in Q.1(a). **[5]**

(d) Modify the equation so that the logic circuit is composed of only **NAND** gates. Simulate the logic circuit in Verilog for 50 ns and show the timing diagram by assigning suitable clocks to the input pins to generate all possible input combinations. Provide the circuit diagram synthesized by the Verilog compiler. **[5]**