CSE460L: Assignment 04

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Section: 02

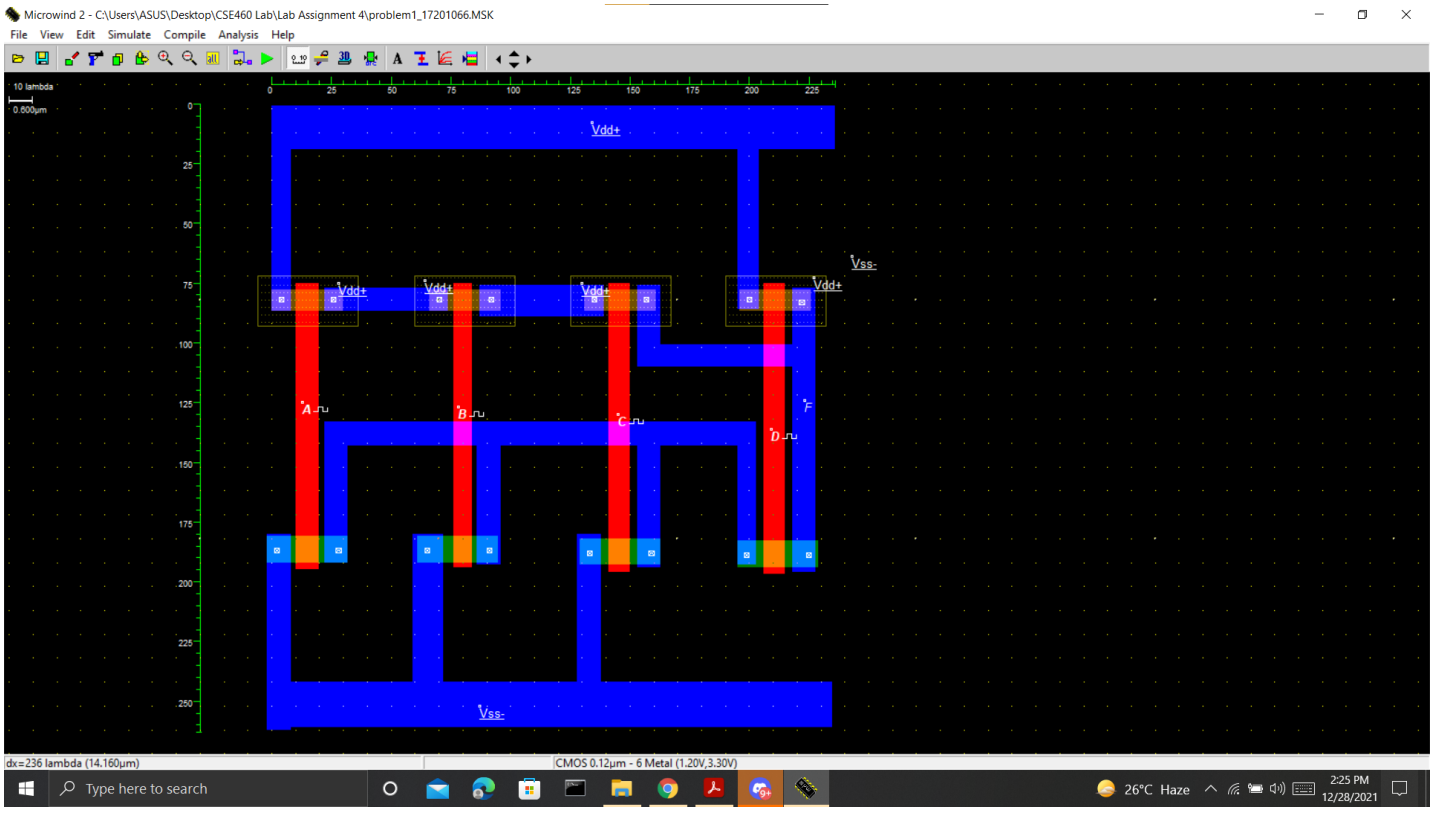
Couse: CSE460

Problem 1:

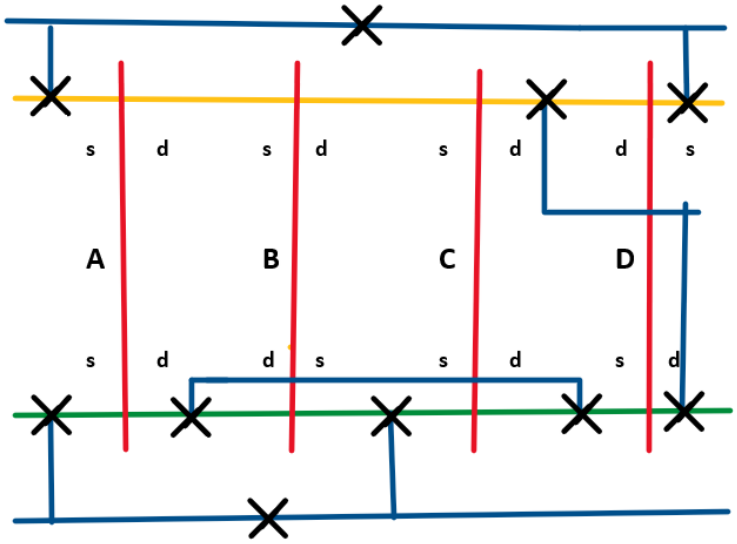
The logical expression:

$$Y = \overline{(A+B+C)D}$$

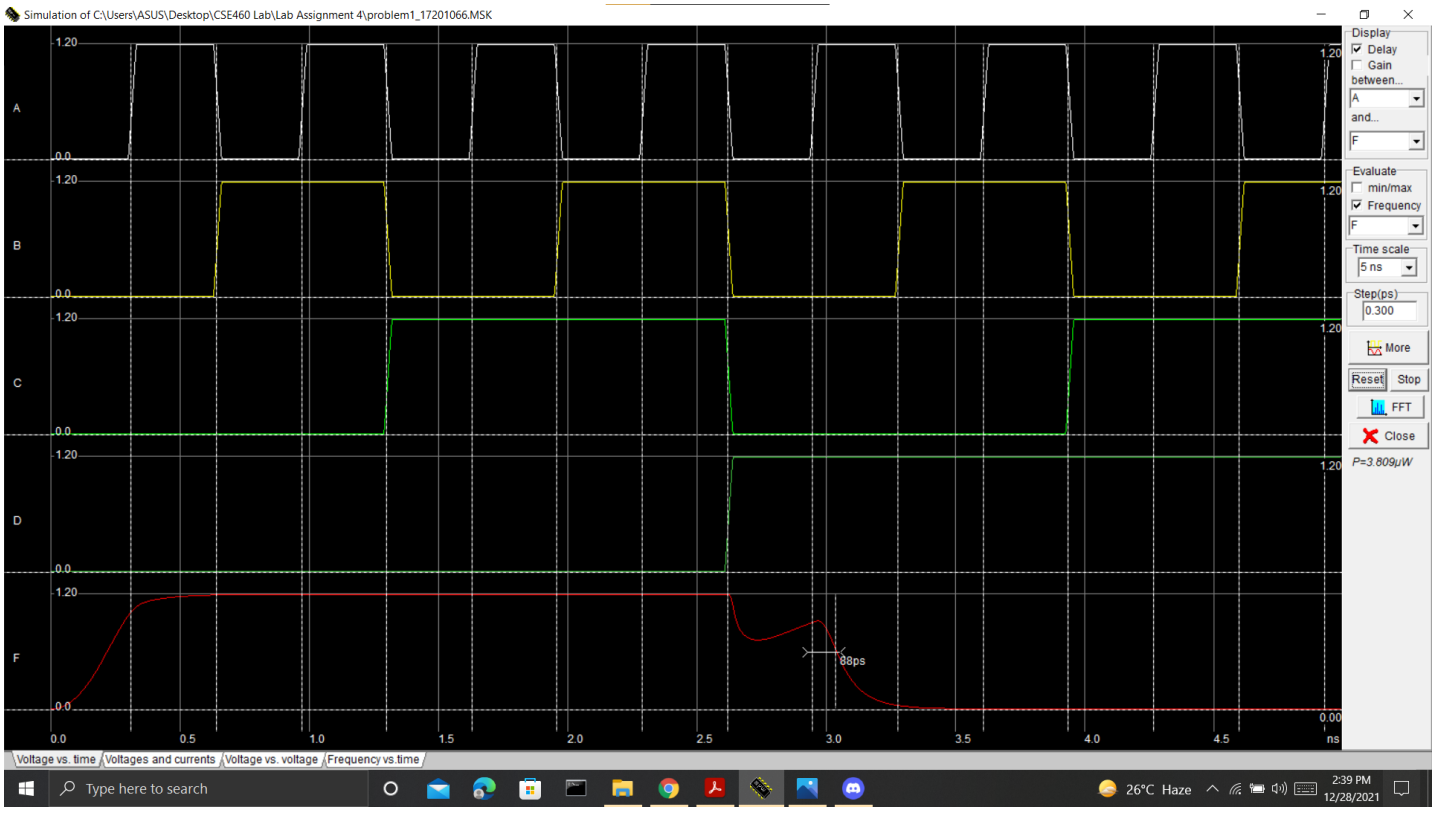
The layout (without using the MOS generator from the design palette) of the Logic Circuit in Microwind2:



Stick Diagram of the given Logical Circuit:



Time Diagram Generated From Microwind2:



Discussion:

Here in the Microwind2 the dimensions of the circuit are,
Width (Vertical) = 263
Height/Length (Horizontal) = 237

For scale 10 lamda and 0.600 micrometer,
Width = 15.78 micrometer
Height/Length = 14.22 micrometer

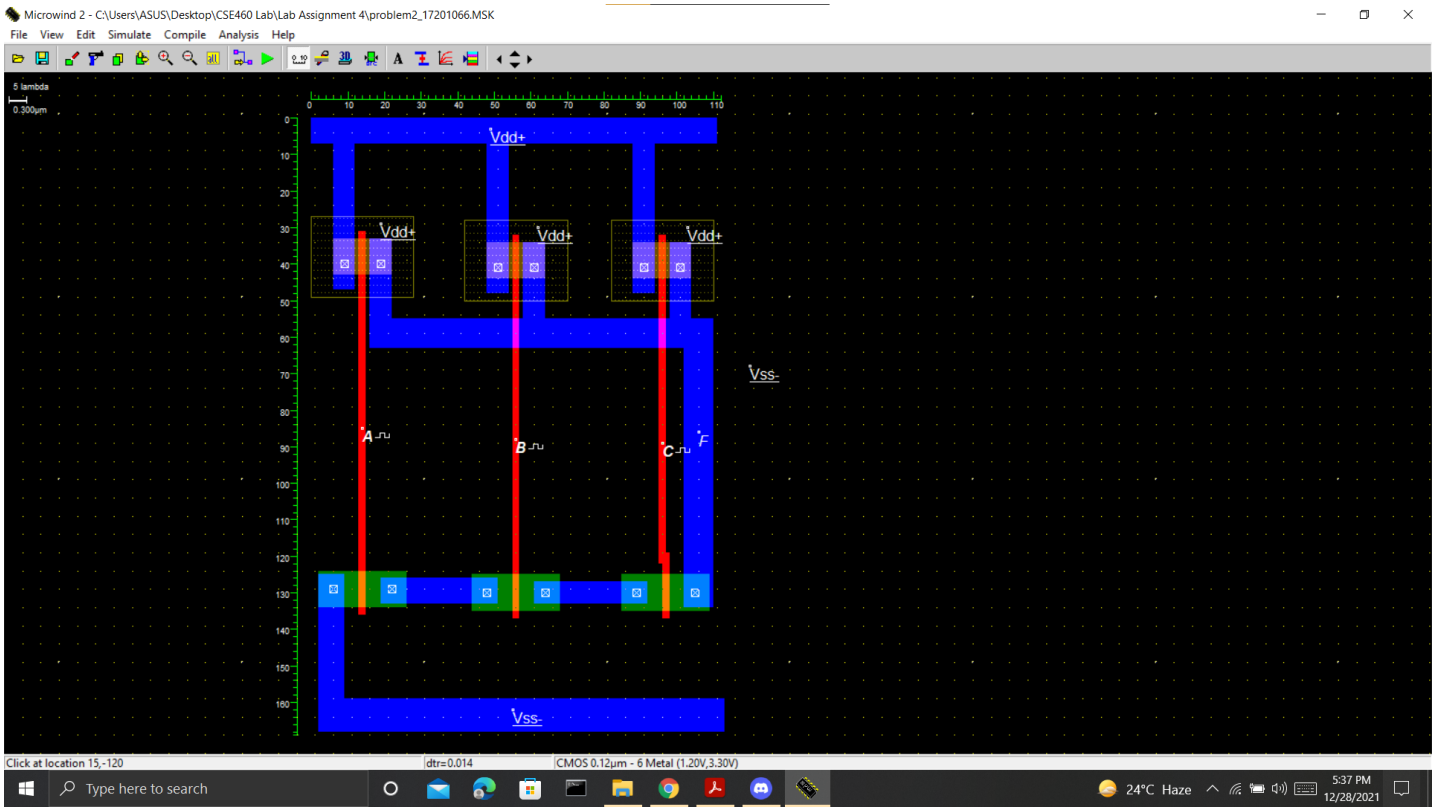
So, in microwind2 the area of the circuit will be 15.78 x 14.22 = 224.3916 micrometer^2

For the stick diagram, the theoretical,
Width = 5 x 10 lambda
Height/Length = 6 x 10 lambda
10 Lambda = 0.600 micrometer
Area = 5 x 6 x 0.600 x 0.600 = 10.8 micrometer^2

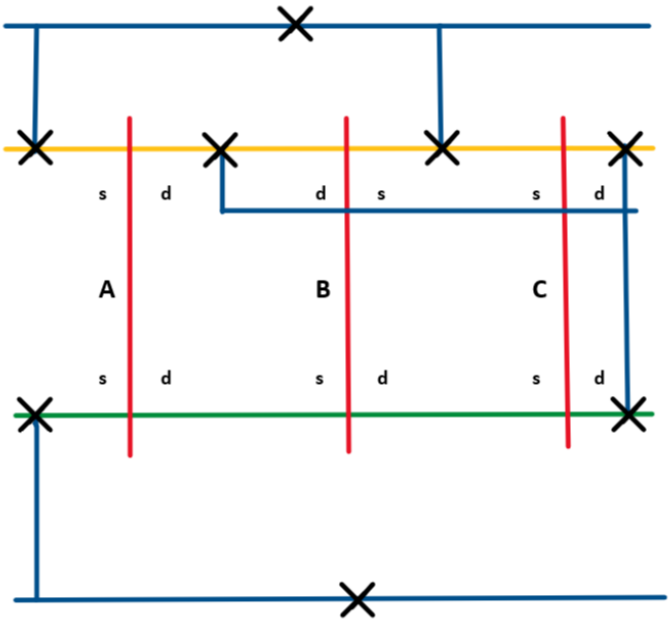
So here we can see that, the area we computed from Microwind2, is 20.77 times bigger than the Theoretical stick diagram best case result.

Problem 2:

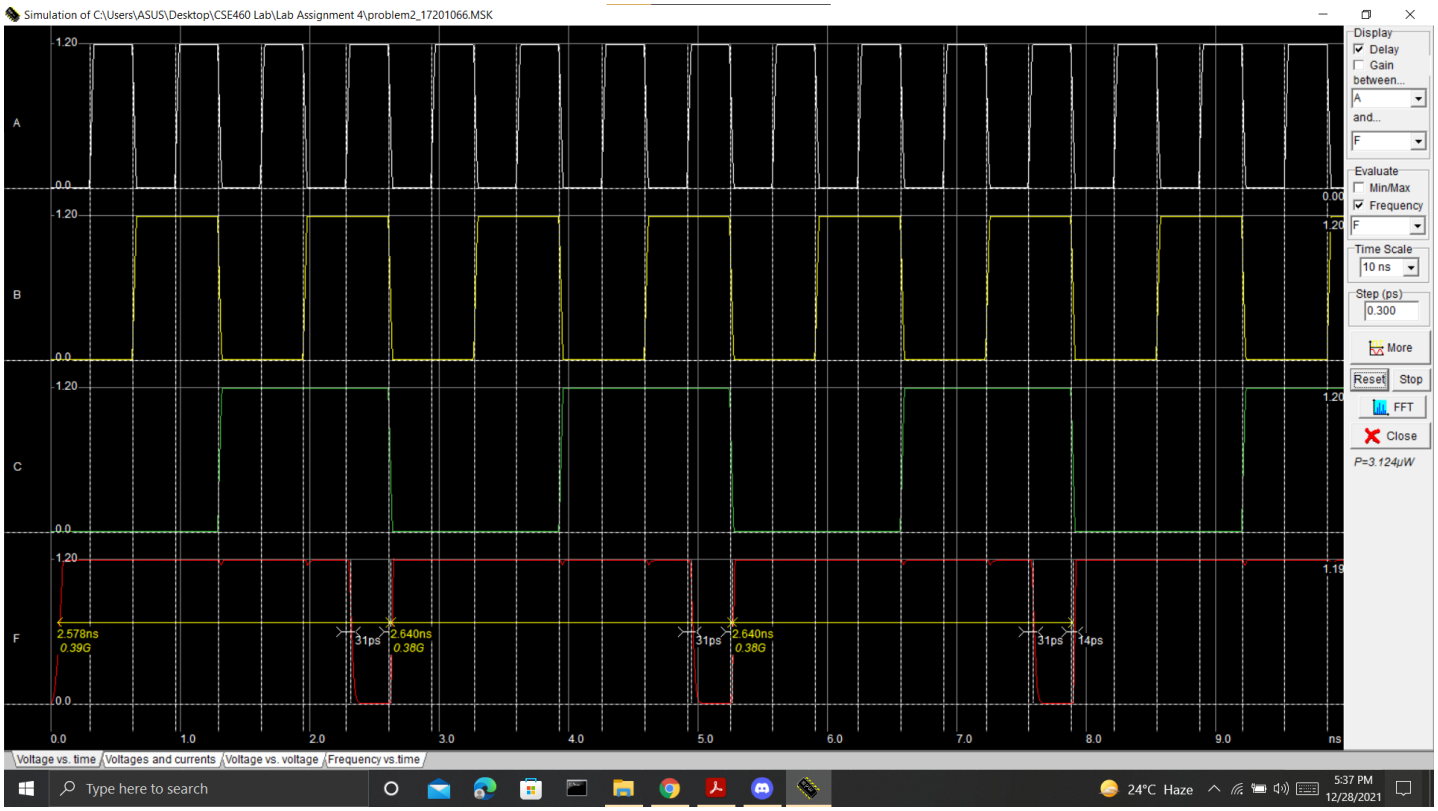
The layout of a 3-input NAND gate using the MOS generator from the design palette in Microwind:



Stick Diagram of the given Logical Circuit:



Time Diagram Generated From Microwind2:



Discussion:

Here in the Microwind2 the dimensions of the circuit are,
Width (Vertical) = 169
Height/Length (Horizontal) = 112

For scale 5 lamda and 0.300 micrometer,

Width (Vertical) = 10.14 micrometer
Height/Length (Horizontal) = 6.72 micrometer

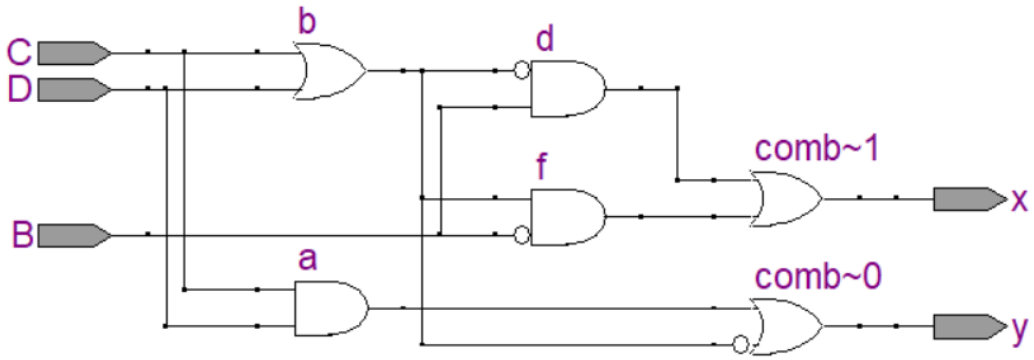
So, in microwind2 the area of the circuit will be 10.14 x 6.72 = 68.141 micrometer^2.

For the stick diagram, the theoretical,
Width = 4 x 5 lambda
Height/Length = 5 x 5 lambda
5 Lambda = 0.300 micrometer
Area = 4 x 5 x 0.300 x 0.300 = 1.8 micrometer^2

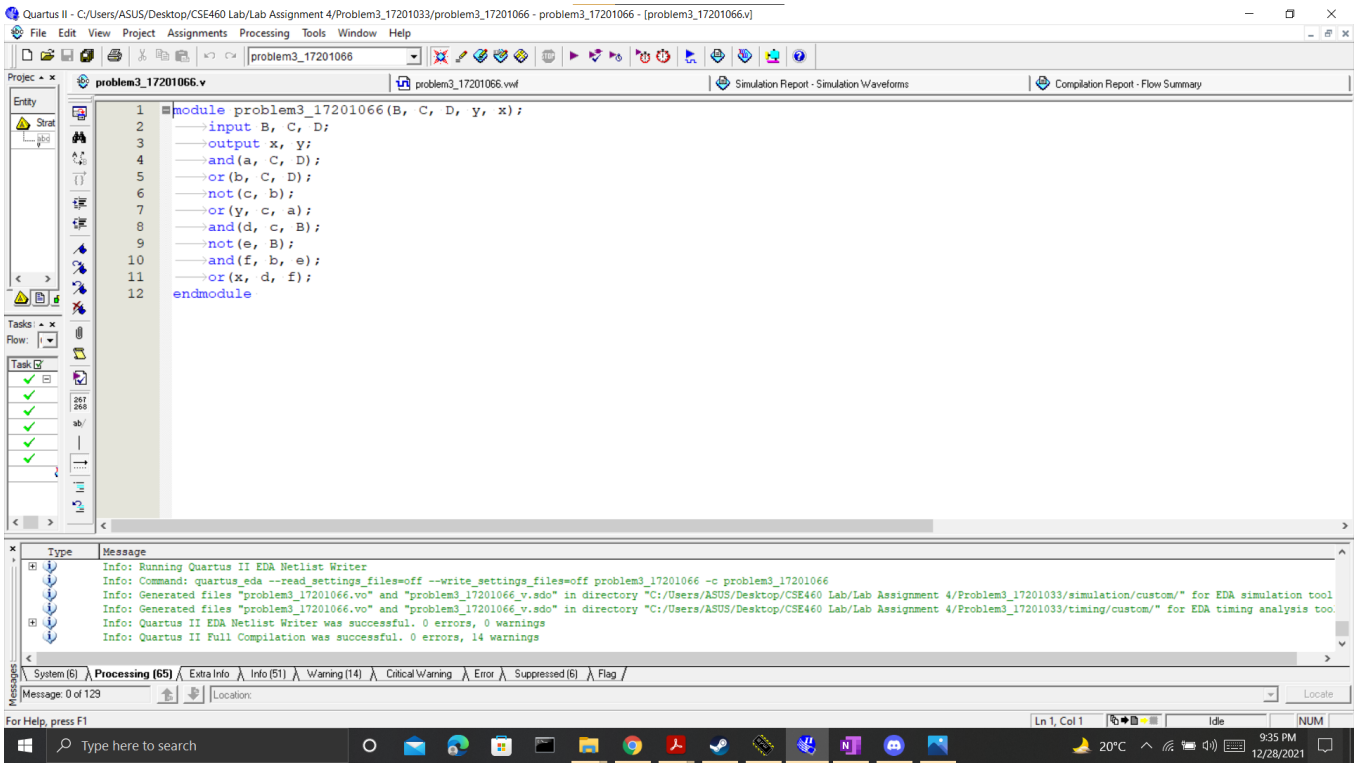
So here we can see that, the area we computed from Microwind2, is 37.85 times bigger than the Theoretical stick diagram best case result.

Problem 3:

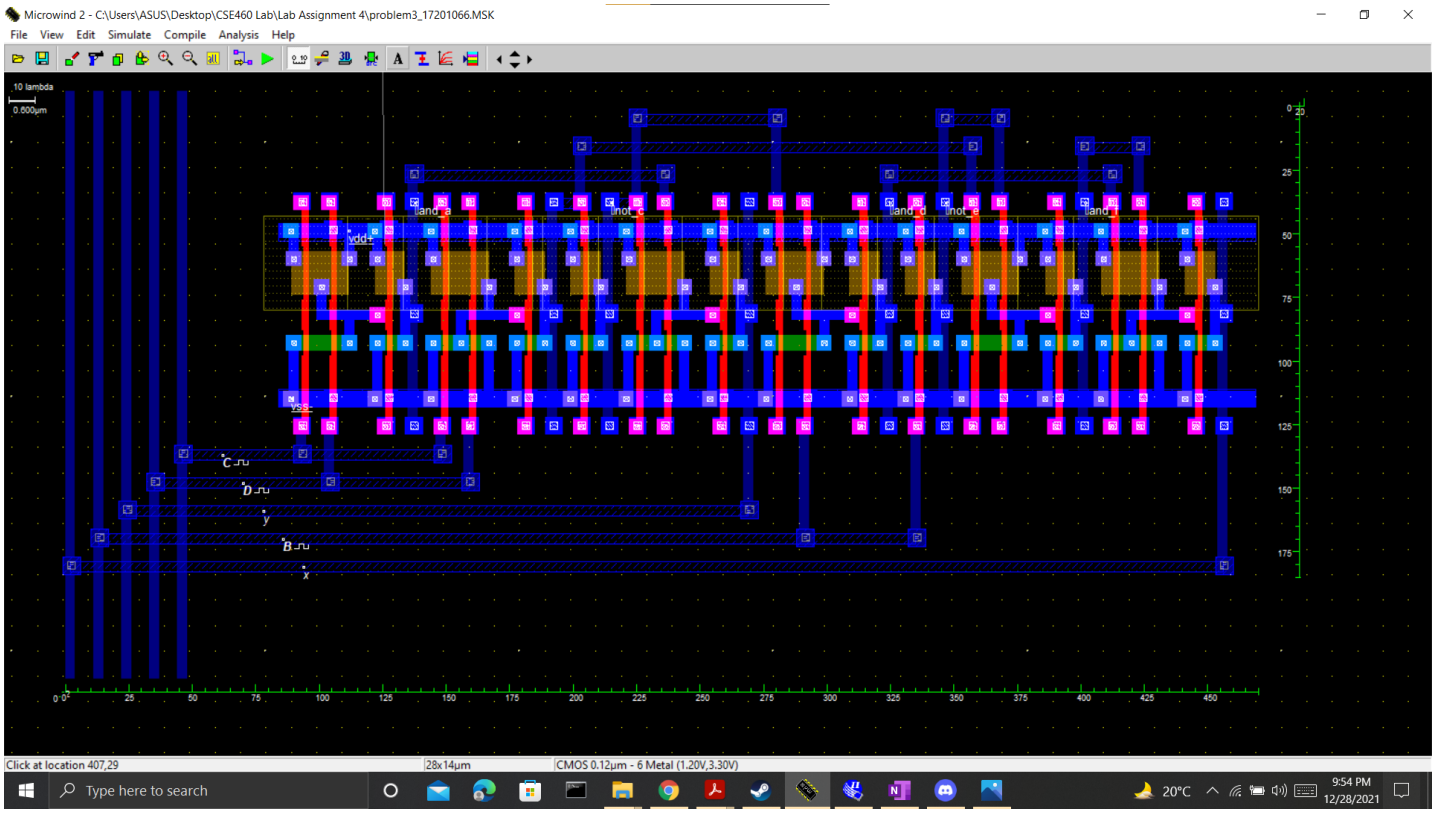
The logical Circuit:



Verilog Code:



The layout generated form the verilog code:



Discussion:

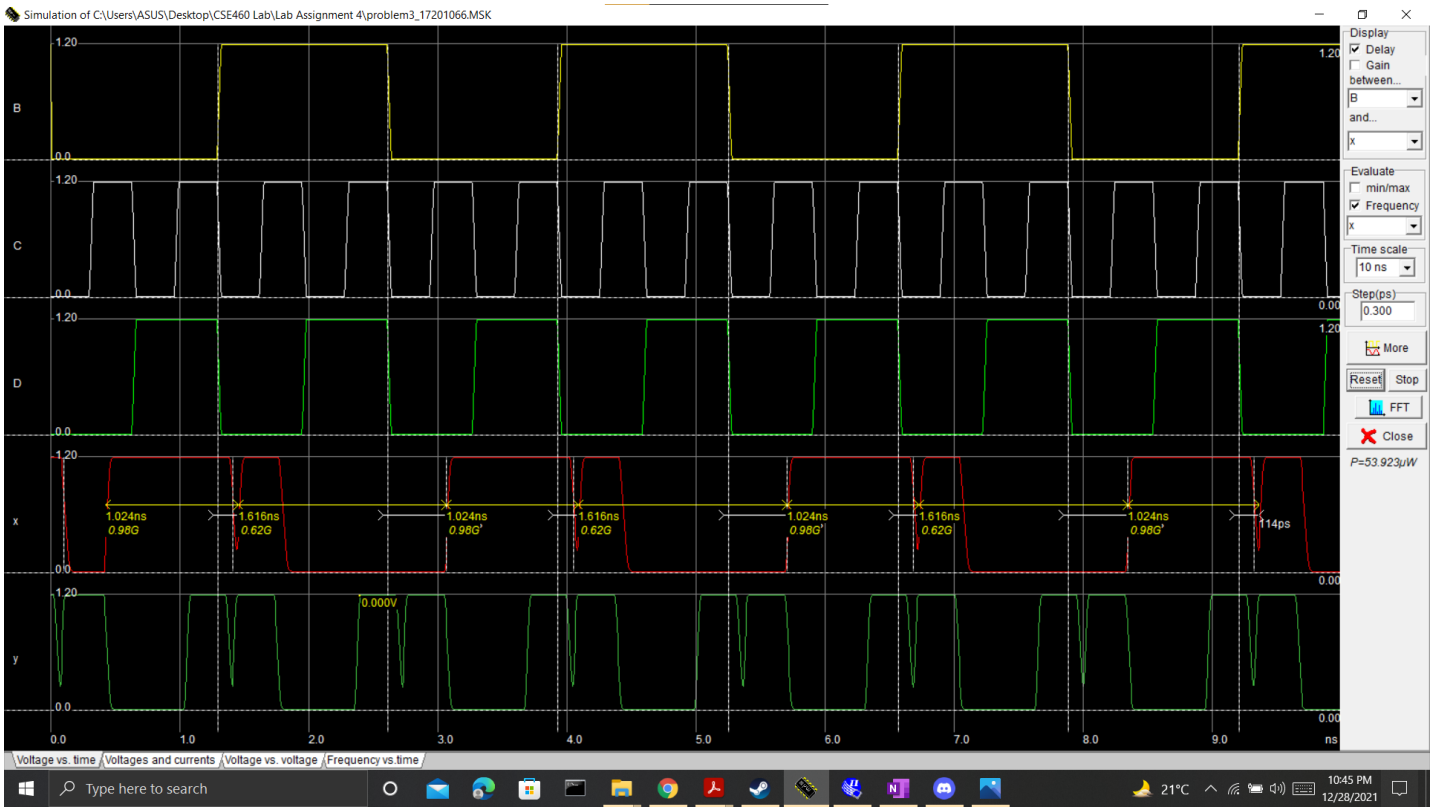
Here in the Microwind2 the dimensions of the circuit are,
Width (Vertical) = 185
Height/Length (Horizontal) = 470

For scale 10 lamda and 0.600 micrometer,

Width (Vertical) = 11.1 micrometer
Length (Horizontal) = 28.2 micrometer

So, in microwind2 the area of the circuit will be 11.1 x 28.2 = 313.02 micrometer^2.

Time Diagram Generated From Microwind2:



The logical expression of the above logical circuit,

$$y = ((C + D)' + CD)$$
$$x = B'(C + D) + B(C + D)'$$

Truth Table of the above logical expression:

B	C	D	y	x
0	0	0	1	0
1	0	0	1	1
0	1	0	0	1
1	1	0	0	0
0	0	1	0	1
1	0	1	0	0

0	1	1	1	1
1	1	1	1	0

Discussion:

Verifying the value of x:
In the microwind2 time diagram, between (4.0 - 5.0)ns time interval when,
B = 1, C = 0 and D = 1
The value of x = 0.
In the truth table, we can see the value of x is 0 when B = 1, C = 0 and D =1.

Again, at (6.0 - 6.5)ns the value of x is 1 while B = 0, C = 1 and D = 1
The truth table above gives the similar result for B = 0, C = 1 and D = 1.

Verifying the value of y:
In the microwind2 generated time diagram, between (0.0 - 1.0)ns time interval for
B = 0, C = 0 and D = 1, the value of y is 0.
In the truth table, we can see the value of y is 0 when B = 0, C = 0 and D =1.

Similarly, between (2.0 - 3.0)ns when B = 1, C = 1, D = 1, the output y = 1. Again, the above truth table shows us the similar result y = 1 for B = 1, C = 1, D = 1.

Clearly, the theoretically calculated result from the logical expression and the result we received from microwind2 is almost the same in spite of having some delay issue in Microwind2.