CSE460L: Assignment 3 (Fall 2021)

Sections: 1, 2, 3, 4, 5, 6, 7, 8 & 9

Assignment 3 submission link:
https://docs.google.com/forms/d/e/1FAIpQLScHIfgIGUnDiCHMvJc7ZbwRMyVj0-PHccatEslv9k8bSEvmrg/viewform?usp=sf_link
Assignment 3 deadline: **Nov 9, 2021 (5 PM)**

General guidelines

- Assignments are individual
- Each assignment will contain 3 to 4 problems
- **For each problem you will need to prepare 3 parts:**

  1. **Code / Schematic Diagram / Layout:** attach a screenshot of your code from *Quartus* or the circuit schematic diagram from *dsch2* or layout from *microwind2* as applicable.

  2. **Output: attach *FULL SCREEN* screenshots** of
  For *Quartus*:
    - Compilation Report - Flow Summary (Compilation report of the .v file)
    - Simulation Report - Simulation Waveforms (Simulation report of the .vwf file)

  For *dsch2* / *microwind2*:
    - Simulation Report - Simulation Waveforms (Timing diagrams of inputs & outputs)

  [**Tampered/edited/cropped screenshots will be considered as a violation of general guidelines and therefore will not be accepted**]

  3. **Discussion/Explanation:** Explain the output waveforms of your simulation report as described in the **Expected Output** section within each problem statement.

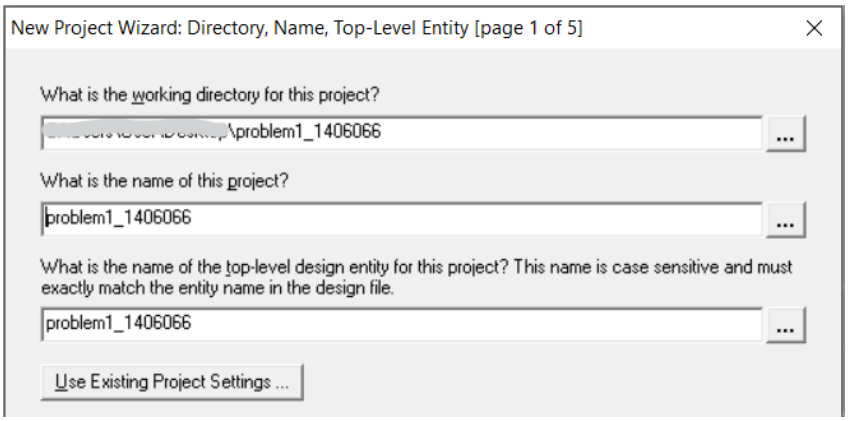
- Each problem will be of equal points. You will not be graded on the length/number of code/diagrams/explanation/outputs; rather on the clarity, readability and precise explanations of your code/diagrams/logic/outputs.

- Points distribution for each problem is

  Code / Schematic Diagram / Layout: **40%**
  Output: **20%**
  Discussion/Explanation of output: **40%**

- **You will need to create separate directories/project for each problem**

- **The name of your working directory for each problem of the assignment should be …\problem#_StudentID [# = 1/2/3/4/5/6/7/8/9]**
  For example, for problem 1 the name of the directory should be problem1_1406066



- Consequently, the name of your main module in the Verilog file should be problem#_StudentID [# = 1/2/3/4/5/6/7]
  Continuing from the previous example, the name of the module should be problem1_1406066

- Finally, **compile all the problems for a given assignment into a single pdf file**

- The **name of the pdf should be Section_StudentID_assignment3.pdf** (Example: 1_1406066_assignment3.pdf)

Problems for Assignment 3

(All problems must be done in dsch2 and you can't use a pre designed gate. You need to build the gate from scratch)

1. Derive the Boolean logic expression from the following K-Map and implement the logic function using CMOS technology. You may use blocks/sub-circuits made using CMOS technology but cannot use readily available logic gates.

CD \ AB	00	01	11	10
00	1	0	1	1
01	1	d	d	0
11	d	d	1	0
10	1	1	0	1

Expected Output:

Show the necessary steps to derive the logic expression from the K-Map and draw the CMOS circuit in *dsch2.* Assign clocks of suitable frequencies to each of the inputs so that all possible input combinations are generated in the timing diagram. From your timing diagram explain one case where *Output = 1* and another case where *Output = 0*. Verify the values with your theoretical values calculated from the logic expressions.

2. Implement the following logic expression using an ***16 to 1*** multiplexer.

$$f(A,B,C,D,E) = \sum(0,4,5,8,9,12,15,21,22,29,30); \text{ don't care } 7$$

The ***16 to 1*** multiplexer is to be designed using sub-circuit blocks of ***4 to 1*** multiplexers only.

Expected Output:

Show the necessary steps to derive the desired circuit and draw the circuit in *dsch2.* Assign clock signals of suitable frequencies to the pins and clearly show when each input is passed to the output in a table using the timestamps from the timing diagram.

3. Design a 4 bit down-counter with *Reset* functionality using D flip-flops and show the count value at any instant using a seven segment display (the seven segment display is available at the symbol library). You may use blocks/sub-circuits made using CMOS technology but cannot use readily available logic gates.

   Expected Output:

   The counting value decrement should take place at the positive edge of the *Clock.* Choose a suitable clock frequency so that the simulation takes place for a minimum of two counting cycles. Clearly show the circuit in dsch2 and briefly explain the timing diagram.