CSE460L: Assignment 02

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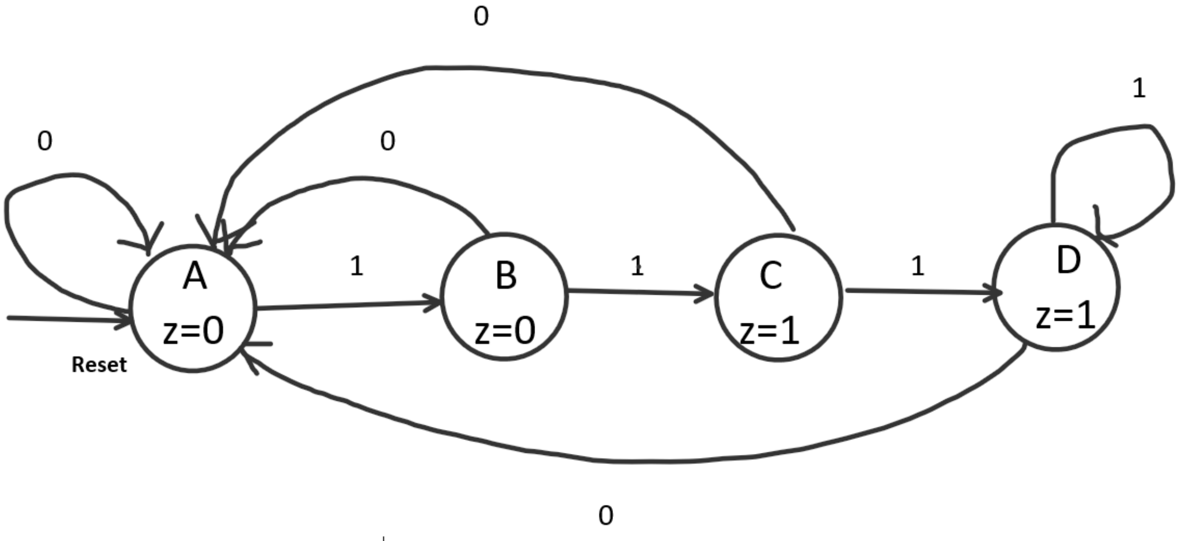
Section: 02

Couse: CSE460

Problem 1

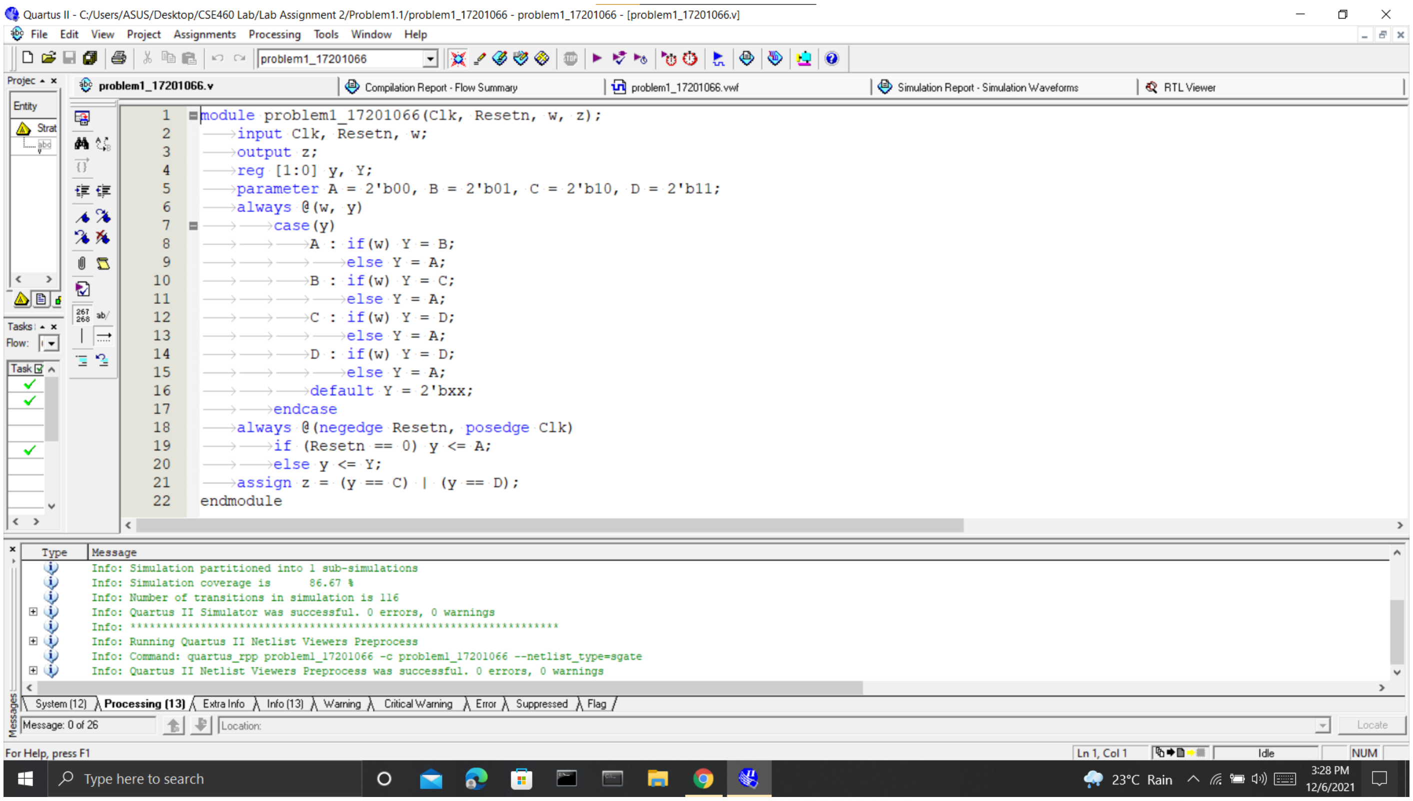
The State Diagram:



The State-assigned Table:

Current State (y2y1)	Next State w = 0 Y2Y1	Next State w = 1 Y2Y1	Output z
00 (A)	00	01	0
01 (B)	00	10	0
10 (C)	00	11	1
11 (D)	00	11	1

Verilog code:

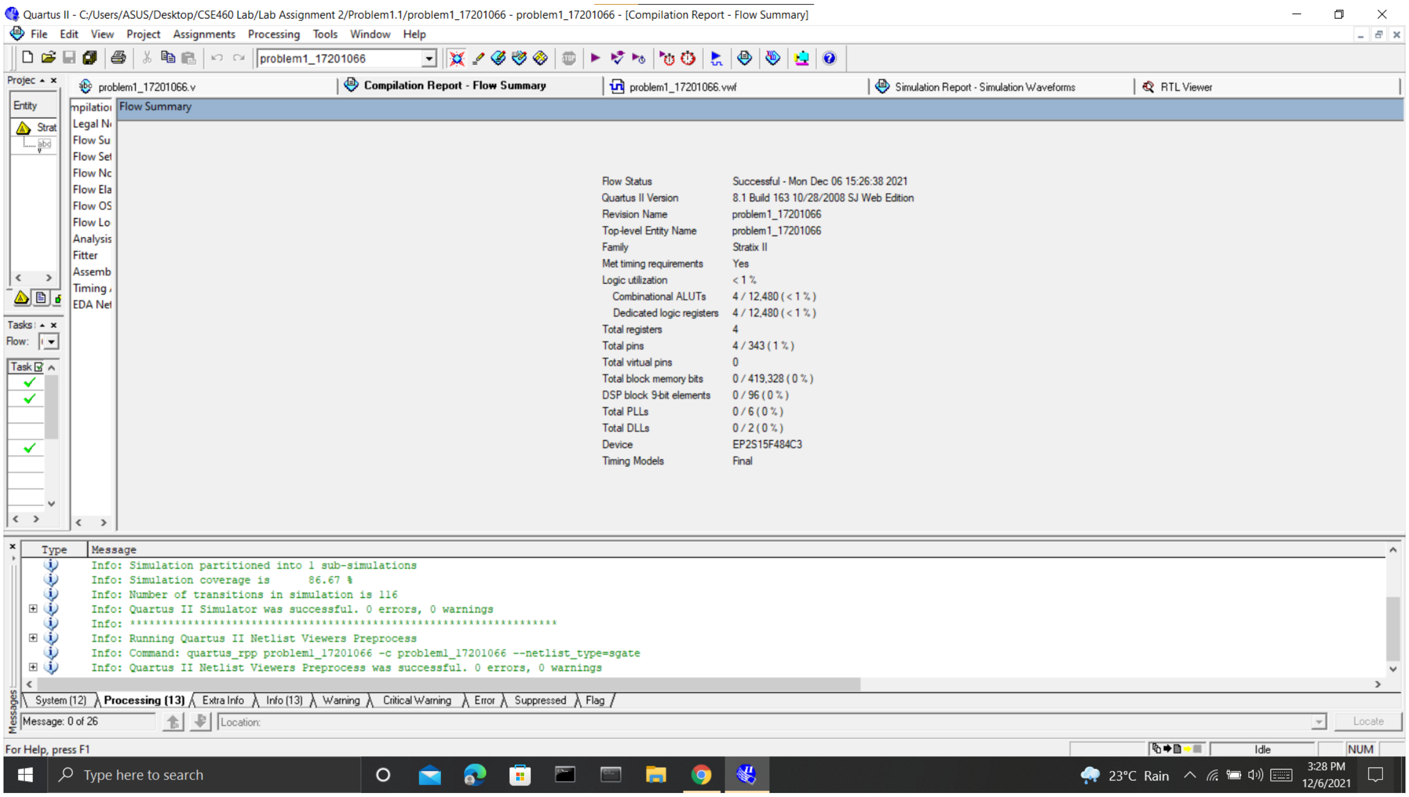


Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem1.1/problem1_17201066 - problem1_17201066 - [problem1_17201066.v]

```verilog
module problem1_17201066(Clk, Resetn, w, z);
    input Clk, Resetn, w;
    output z;
    reg [1:0] y, Y;
    parameter A = 2'b00, B = 2'b01, C = 2'b10, D = 2'b11;
    always @(w, y)
        case(y)
            A : if(w) Y = B;
                else Y = A;
            B : if(w) Y = C;
                else Y = A;
            C : if(w) Y = D;
                else Y = A;
            D : if(w) Y = D;
                else Y = A;
            default Y = 2'bxx;
        endcase
    always @(negedge Resetn, posedge Clk)
        if (Resetn == 0) y <= A;
        else y <= Y;
    assign z = (y == C) | (y == D);
endmodule
```

```
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is      86.67 %
Info: Number of transitions in simulation is 116
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
Info: *******************************************************************
Info: Running Quartus II Netlist Viewers Preprocess
Info: Command: quartus_rpp problem1_17201066 -c problem1_17201066 --netlist_type=sgate
Info: Quartus II Netlist Viewers Preprocess was successful. 0 errors, 0 warnings
```

Message: 0 of 26



Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem1.1/problem1_17201066 - problem1_17201066 - [Compilation Report - Flow Summary]

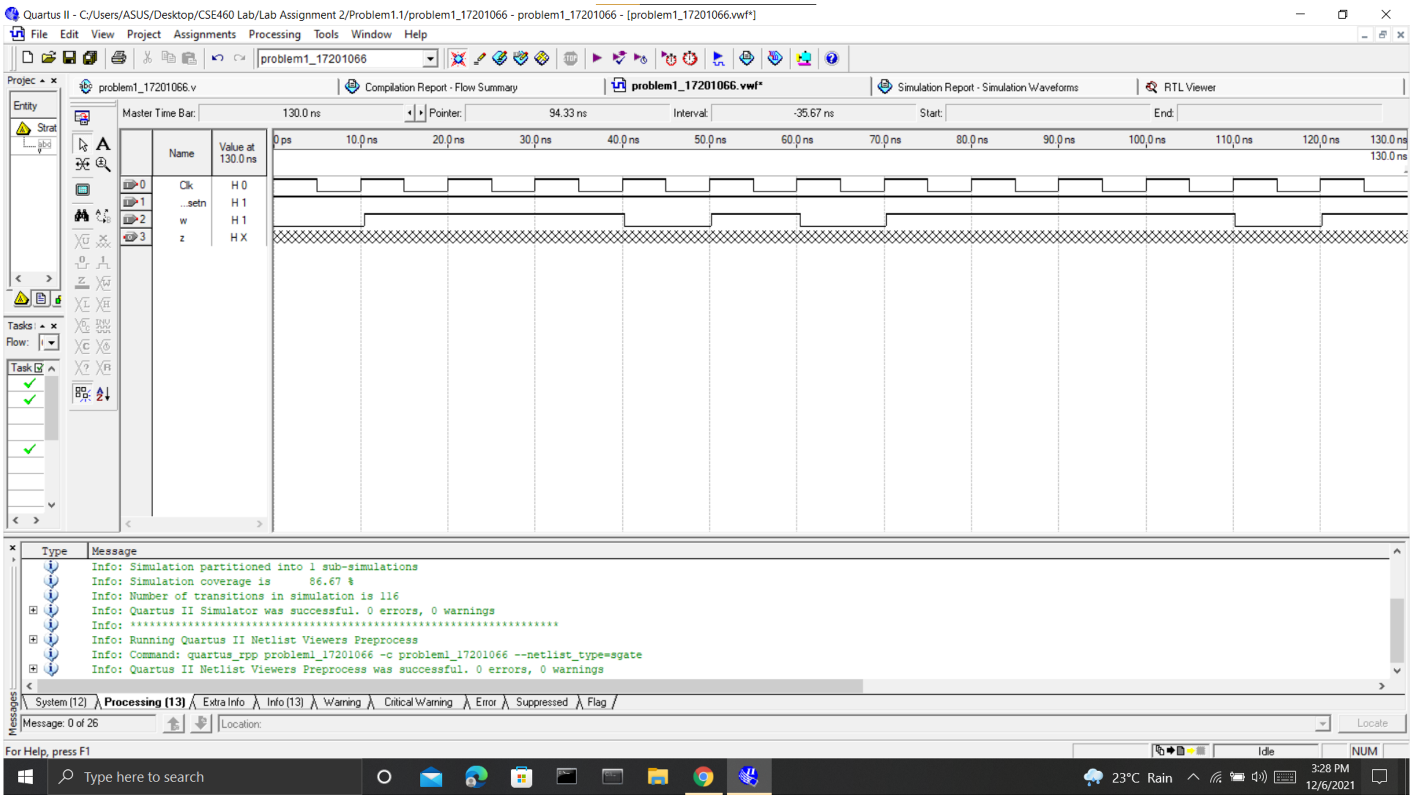
Flow Summary

Flow Status	Successful - Mon Dec 06 15:26:38 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem1_17201066
Top-level Entity Name	problem1_17201066
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	4 / 12,480 (< 1 %)
Dedicated logic registers	4 / 12,480 (< 1 %)
Total registers	4
Total pins	4 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

```
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is      86.67 %
Info: Number of transitions in simulation is 116
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
Info: *******************************************************************
Info: Running Quartus II Netlist Viewers Preprocess
Info: Command: quartus_rpp problem1_17201066 -c problem1_17201066 --netlist_type=sgate
Info: Quartus II Netlist Viewers Preprocess was successful. 0 errors, 0 warnings
```

Message: 0 of 26

Simulation:



Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem1.1/problem1_17201066 - problem1_17201066 - [problem1_17201066.vwf*]

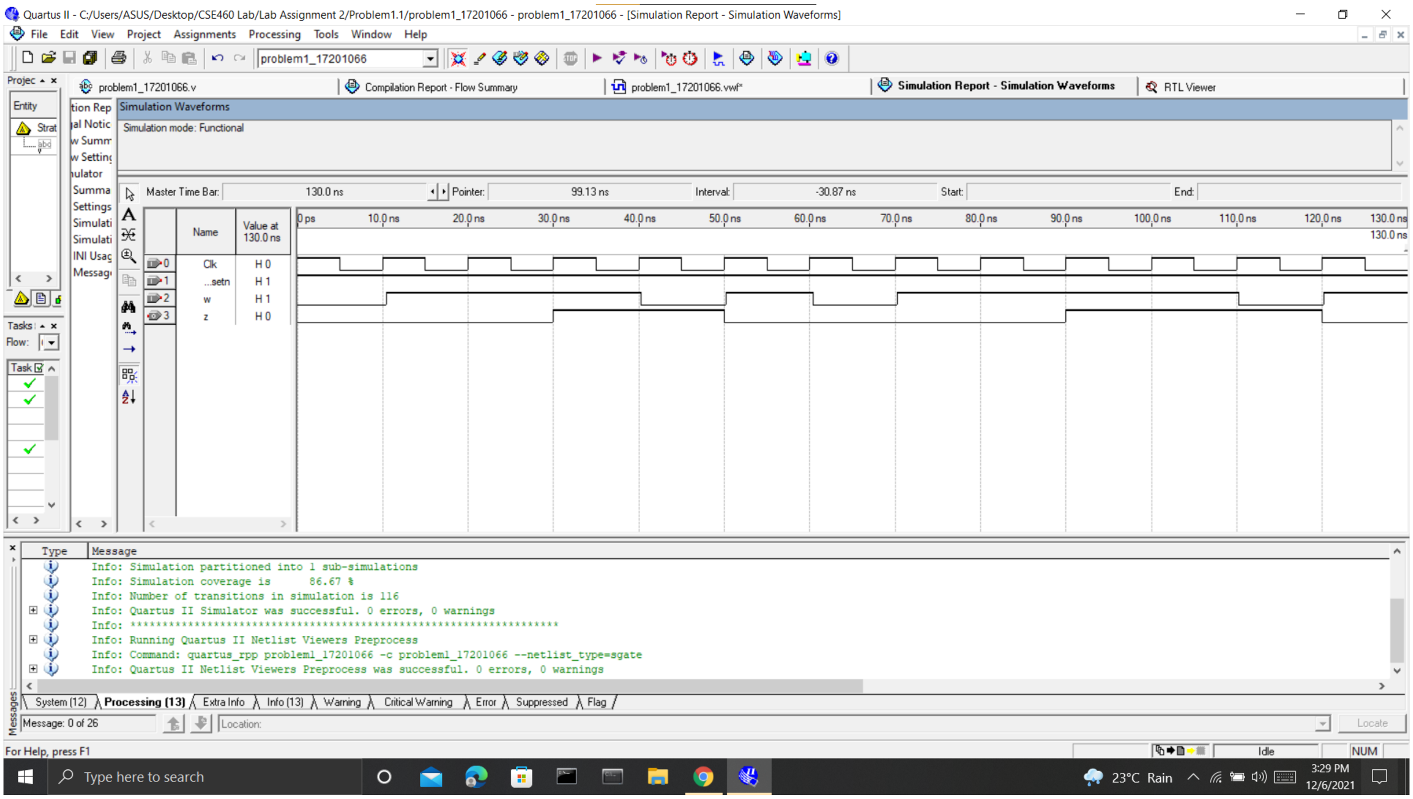
File Edit View Project Assignments Processing Tools Window Help
problem1_17201066
problem1_17201066.v
Compilation Report - Flow Summary
problem1_17201066.vwf*
Simulation Report - Simulation Waveforms
RTL Viewer
0 ps 10.0 ns 20.0 ns 30.0 ns 40.0 ns 50.0 ns 60.0 ns 70.0 ns 80.0 ns 90.0 ns 100.0 ns 110.0 ns 120.0 ns 130.0 ns

Master Time Bar: 130.0 ns Pointer: 94.33 ns Interval: -35.67 ns Start: End:

	Name	Value at 130.0 ns
0	Clk	H 0
1	...setn	H 1
2	w	H 1
3	z	H X

```
Type  Message
      Info: Simulation partitioned into 1 sub-simulations
      Info: Simulation coverage is      86.67 %
      Info: Number of transitions in simulation is 116
      Info: Quartus II Simulator was successful. 0 errors, 0 warnings
      Info: *******************************************************************
      Info: Running Quartus II Netlist Viewers Preprocess
      Info: Command: quartus_rpp problem1_17201066 -c problem1_17201066 --netlist_type=sgate
      Info: Quartus II Netlist Viewers Preprocess was successful. 0 errors, 0 warnings
```

System (12) Processing (13) Extra Info Info (13) Warning Critical Warning Error Suppressed Flag
Message: 0 of 26
Location:
Locate
For Help, press F1
Idle
NUM
Type here to search
23°C Rain
3:28 PM
12/6/2021



Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem1.1/problem1_17201066 - problem1_17201066 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help
problem1_17201066
problem1_17201066.v
Compilation Report - Flow Summary
problem1_17201066.vwf*
Simulation Report - Simulation Waveforms
RTL Viewer
Simulation Waveforms
0 ps 10.0 ns 20.0 ns 30.0 ns 40.0 ns 50.0 ns 60.0 ns 70.0 ns 80.0 ns 90.0 ns 100.0 ns 110.0 ns 120.0 ns 130.0 ns

Simulation mode: Functional

Master Time Bar: 130.0 ns Pointer: 99.13 ns Interval: -30.87 ns Start: End:

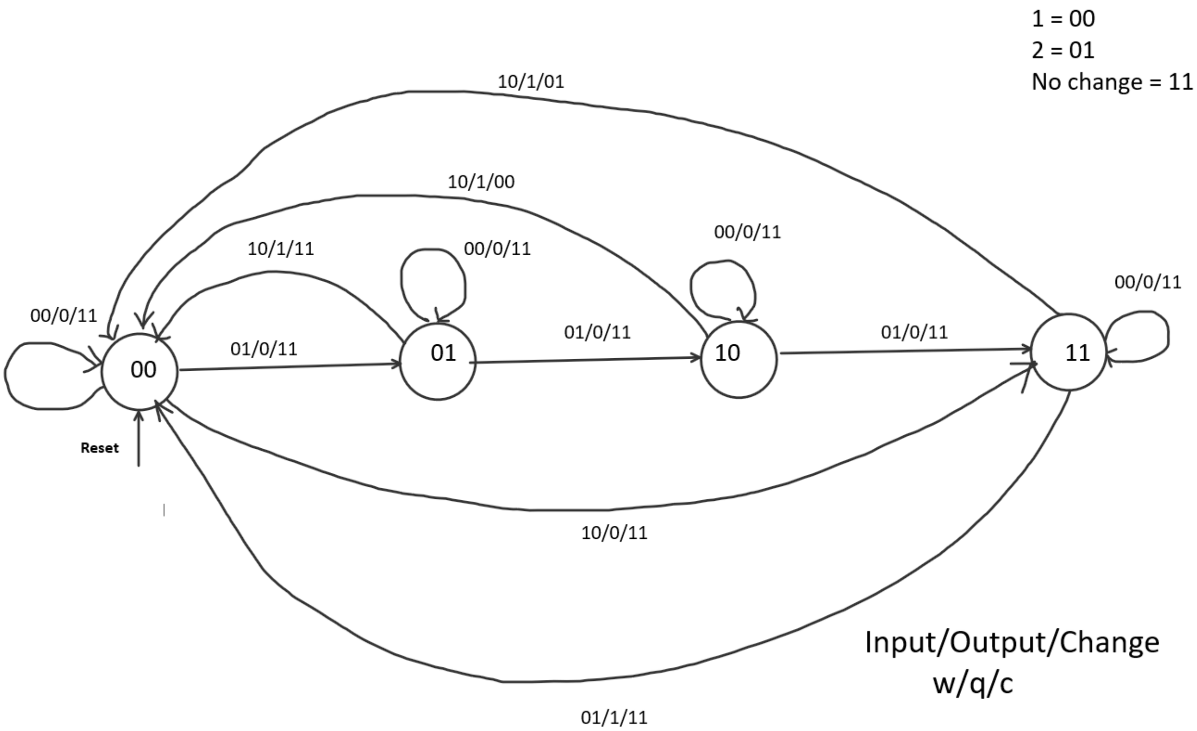
	Name	Value at 130.0 ns
0	Clk	H 0
1	...setn	H 1
2	w	H 1
3	z	H 0

```
Type  Message
      Info: Simulation partitioned into 1 sub-simulations
      Info: Simulation coverage is      86.67 %
      Info: Number of transitions in simulation is 116
      Info: Quartus II Simulator was successful. 0 errors, 0 warnings
      Info: *******************************************************************
      Info: Running Quartus II Netlist Viewers Preprocess
      Info: Command: quartus_rpp problem1_17201066 -c problem1_17201066 --netlist_type=sgate
      Info: Quartus II Netlist Viewers Preprocess was successful. 0 errors, 0 warnings
```

From the table it is clear that it follows a moore state machine. Here we get high output z at 30 - 40ns because between 10 - 20 ns input value w is in high mode. In FSM between 10 to 30 ns it receives 011 input when input in 0 it stays in A state. When it gets 1 it moves to A to B. Now B is not the accepted state so for getting 0 it will again move to state A. However in our example it received 1 so it moved to state C. C is an accepting state. Since the FSM is a moore machine, in the next clock cycle between 30 - 40ns the FSM gives output z = 1. After 011 the machine receives another 1. As a result state C changed to D which is also an accepting state. So, we get again 1 in output at 40 - 50ns. Between 70 - 100 ns we receive 1 continuously. Like before for 11 input the FSM reaches to C. C is an accepting state. So output becomes 1 in 90 - 100 ns. After 11 when the input is again 1, C moves to D and D is accepting state. As a result we receive 1 between 100 to 110 ns. D state stays in D when FSM gets 1 again. So output is again 1 between 110 - 120 ns. After that, in the example input is 0. So, D state moves to state A.

Problem 2

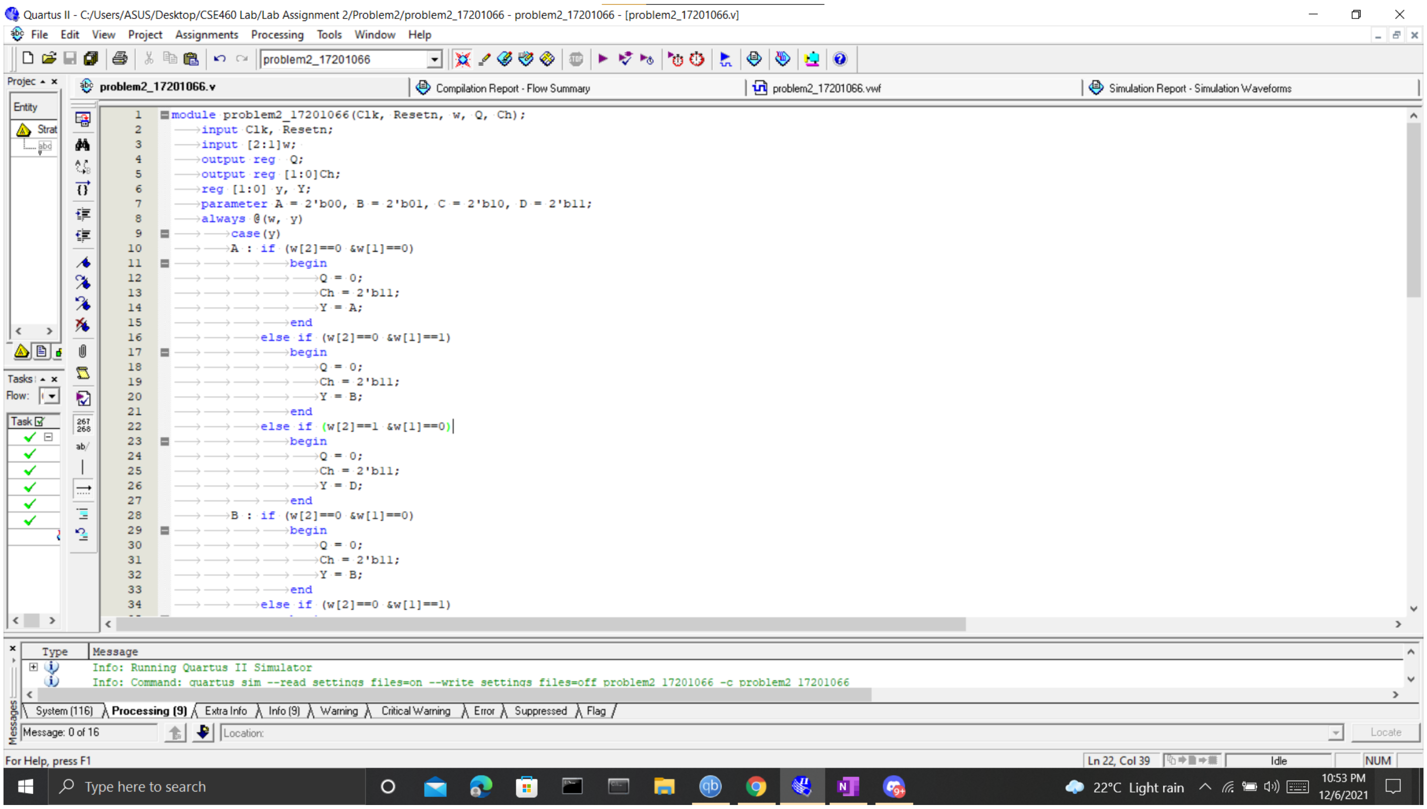
The State Diagram:



The State-assigned Table:

Current State y2y1	Next state w=00 Y2Y1	Next state w=01 Y2Y1	Next state w=10 Y2Y1	Output Q w=00	Output Q w=01	Output Q w=10	Change C w=00	Change C w=01	Change C w=10
00	00	01	11	0	0	1	11	11	11
01	01	10	00	0	0	1	11	11	11
10	10	11	00	0	0	1	11	11	00
11	11	00	00	0	1	1	11	11	01

Verilog code:

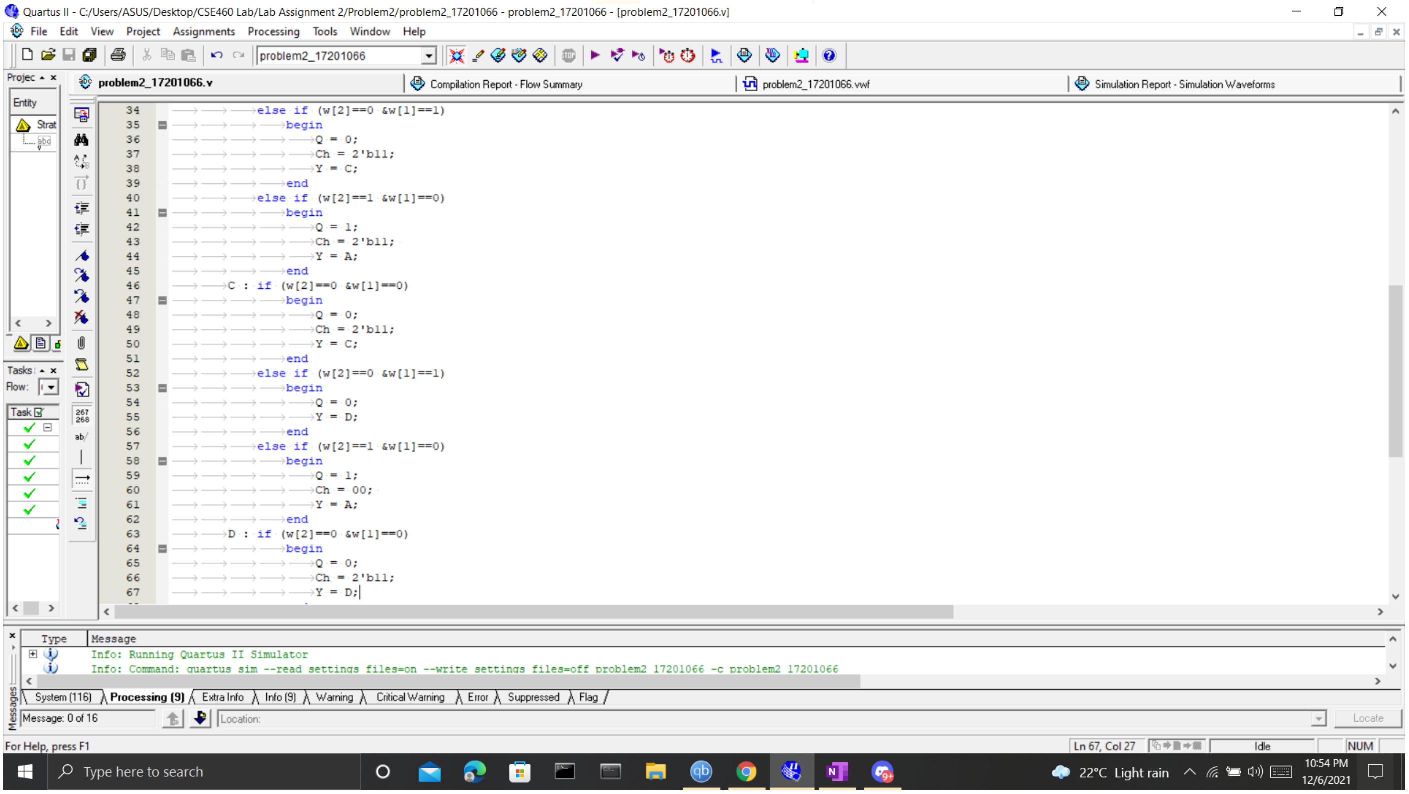


Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem2/problem2_17201066 - problem2_17201066 - [problem2_17201066.v]

File Edit View Project Assignments Processing Tools Window Help
problem2_17201066
problem2_17201066.v
Compilation Report - Flow Summary
problem2_17201066.vwf
Simulation Report - Simulation Waveforms
Entity
Tasks
Flow:
Task

```
module problem2_17201066(Clk, Resetn, w, Q, Ch);
    input Clk, Resetn;
    input [2:1]w;
    output reg  Q;
    output reg [1:0]Ch;
    reg [1:0] y, Y;
    parameter A = 2'b00, B = 2'b01, C = 2'b10, D = 2'b11;
    always @(w, y)
        case(y)
        A : if (w[2]==0 &w[1]==0)
                begin
                    Q = 0;
                    Ch = 2'b11;
                    Y = A;
                end
            else if (w[2]==0 &w[1]==1)
                begin
                    Q = 0;
                    Ch = 2'b11;
                    Y = B;
                end
            else if (w[2]==1 &w[1]==0)
                begin
                    Q = 0;
                    Ch = 2'b11;
                    Y = D;
                end
        B : if (w[2]==0 &w[1]==0)
                begin
                    Q = 0;
                    Ch = 2'b11;
                    Y = B;
                end
            else if (w[2]==0 &w[1]==1)
```

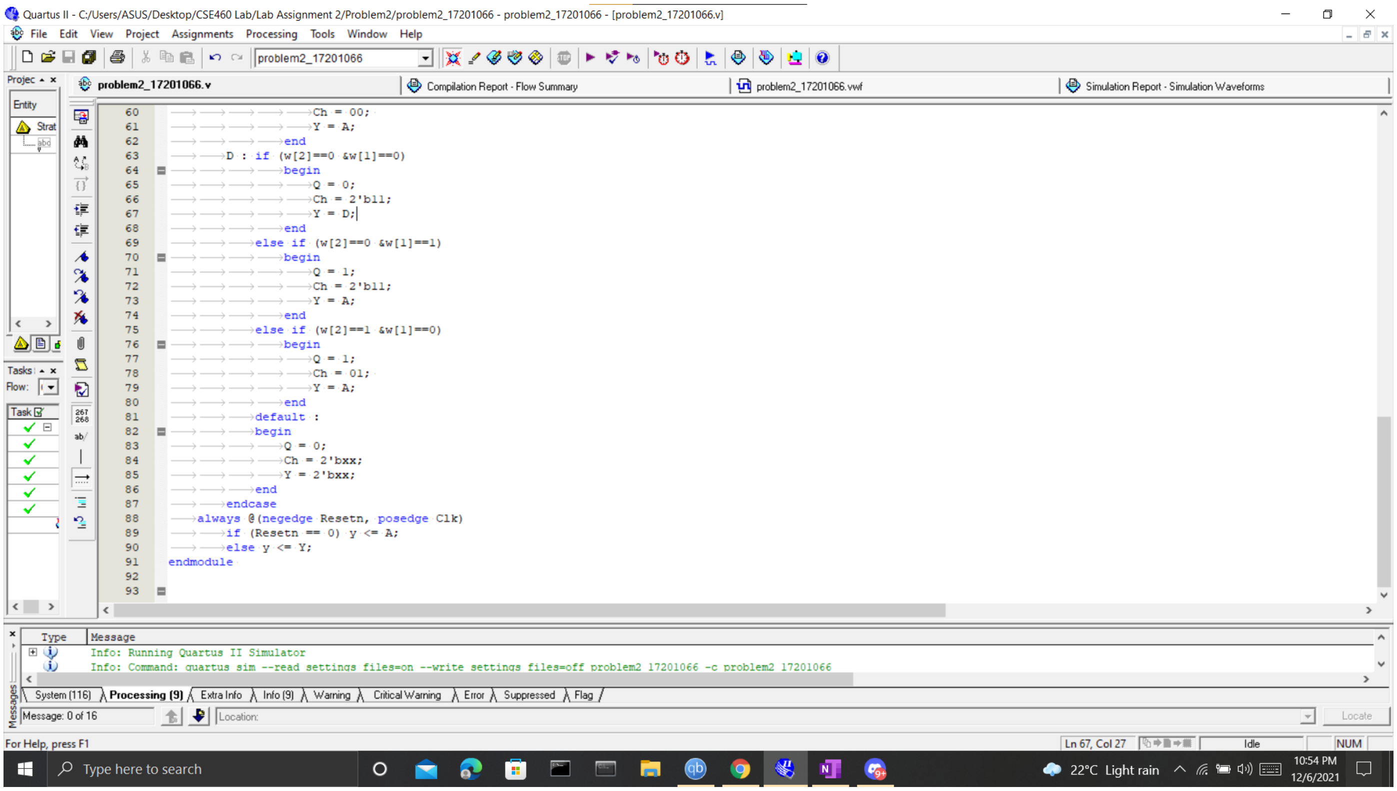
```
Type    Message
        Info: Running Quartus II Simulator
        Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off problem2_17201066 -c problem2_17201066
```



Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem2/problem2_17201066 - problem2_17201066 - [problem2_17201066.v]

```
            else if (w[2]==0 &w[1]==1)
                begin
                    Q = 0;
                    Ch = 2'b11;
                    Y = C;
                end
            else if (w[2]==1 &w[1]==0)
                begin
                    Q = 1;
                    Ch = 2'b11;
                    Y = A;
                end
        C : if (w[2]==0 &w[1]==0)
                begin
                    Q = 0;
                    Ch = 2'b11;
                    Y = C;
                end
            else if (w[2]==0 &w[1]==1)
                begin
                    Q = 0;
                    Y = D;
                end
            else if (w[2]==1 &w[1]==0)
                begin
                    Q = 1;
                    Ch = 00;
                    Y = A;
                end
        D : if (w[2]==0 &w[1]==0)
                begin
                    Q = 0;
                    Ch = 2'b11;
                    Y = D;
```

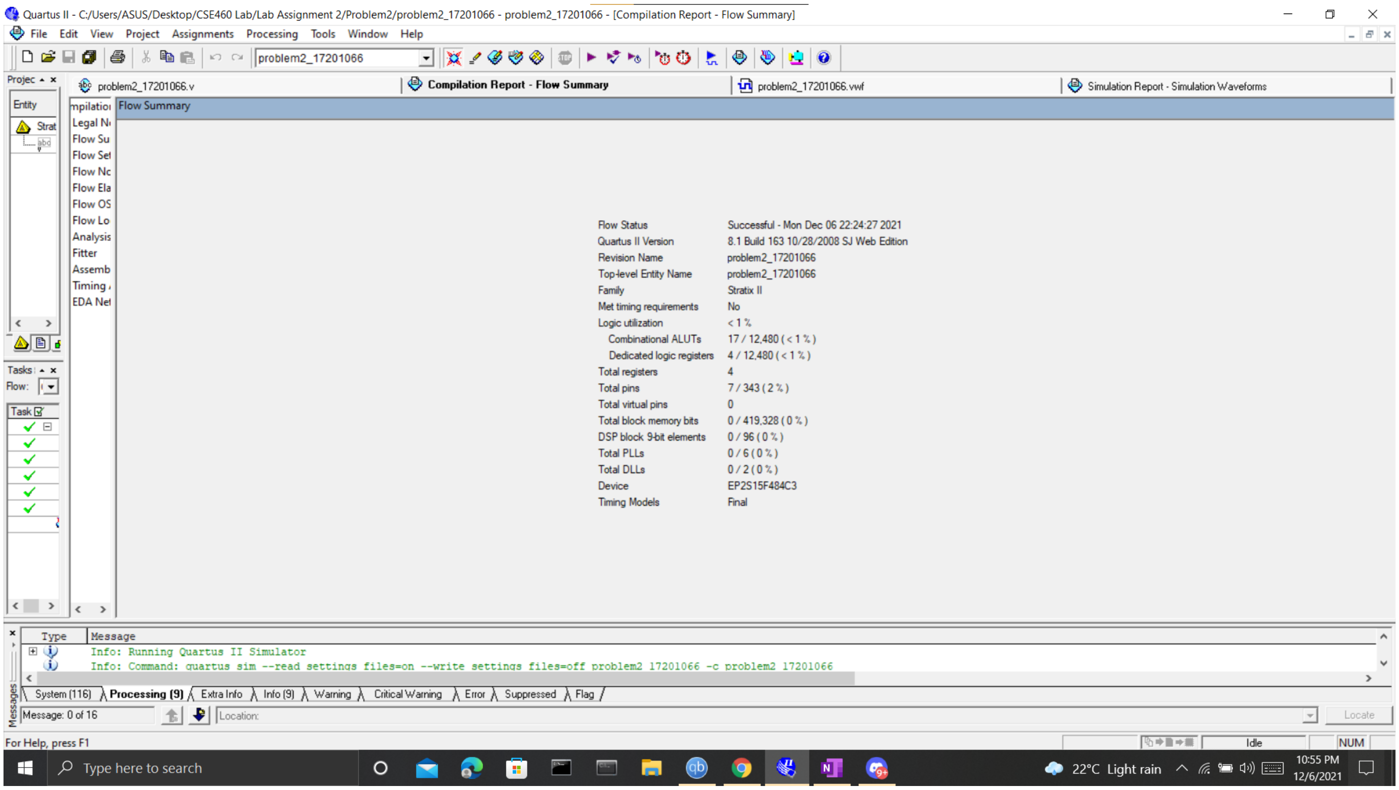
```
Info: Running Quartus II Simulator
Info: Command: quartus sim --read settings files=on --write settings files=off problem2 17201066 -c problem2 17201066
```



Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem2/problem2_17201066 - problem2_17201066 - [problem2_17201066.v]

```
                    Ch = 00;
                    Y = A;
                end
        D : if (w[2]==0 &w[1]==0)
                begin
                    Q = 0;
                    Ch = 2'b11;
                    Y = D;
                end
            else if (w[2]==0 &w[1]==1)
                begin
                    Q = 1;
                    Ch = 2'b11;
                    Y = A;
                end
            else if (w[2]==1 &w[1]==0)
                begin
                    Q = 1;
                    Ch = 01;
                    Y = A;
                end
            default :
            begin
                Q = 0;
                Ch = 2'bxx;
                Y = 2'bxx;
            end
        endcase
    always @(negedge Resetn, posedge Clk)
        if (Resetn == 0) y <= A;
        else y <= Y;
endmodule
```

```
Info: Running Quartus II Simulator
Info: Command: quartus sim --read settings files=on --write settings files=off problem2 17201066 -c problem2 17201066
```



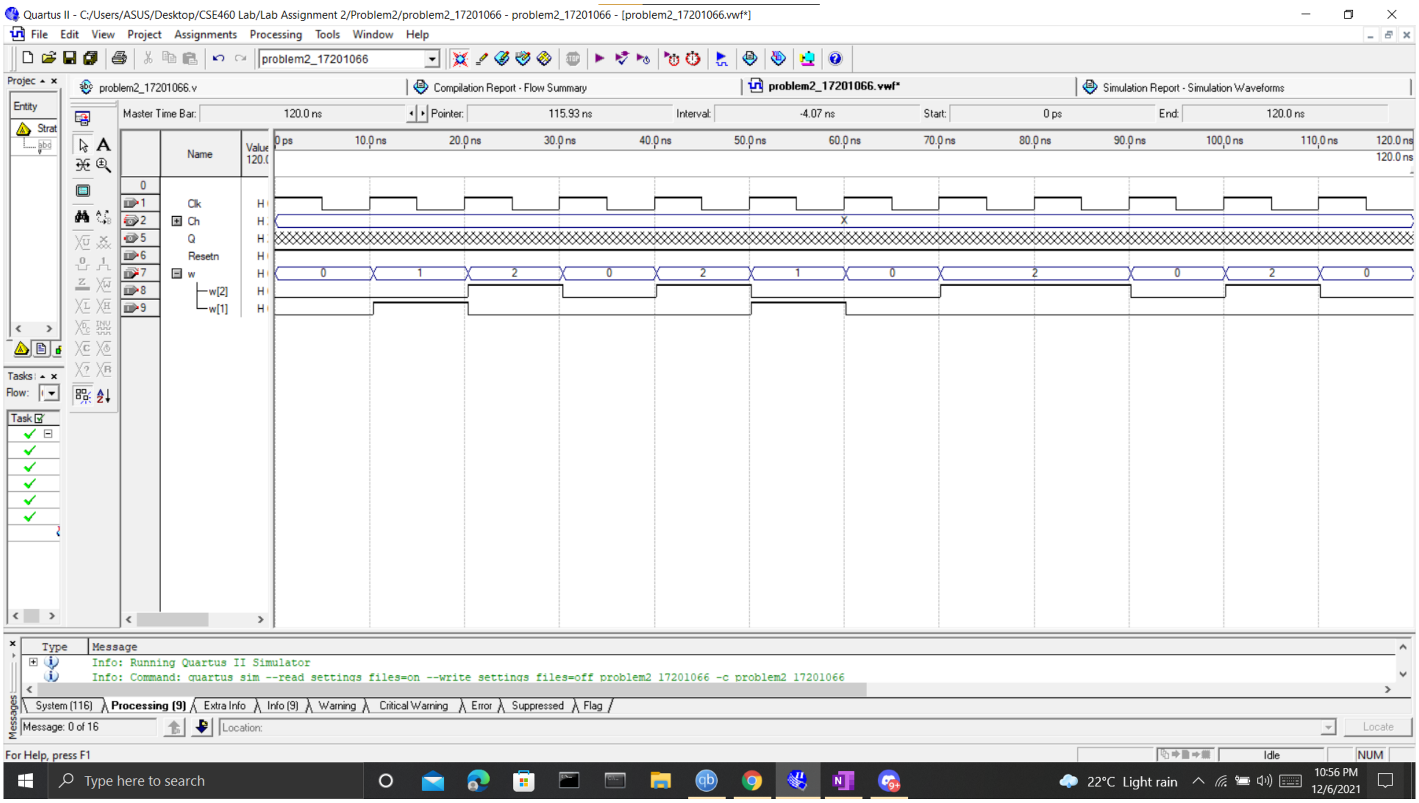
Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem2/problem2_17201066 - problem2_17201066 - [Compilation Report - Flow Summary]

File Edit View Project Assignments Processing Tools Window Help
problem2_17201066
problem2_17201066.v
Compilation Report - Flow Summary
problem2_17201066.vwf
Simulation Report - Simulation Waveforms
Flow Summary

Flow Status	Successful - Mon Dec 06 22:24:27 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem2_17201066
Top-level Entity Name	problem2_17201066
Family	Stratix II
Met timing requirements	No
Logic utilization	< 1 %
Combinational ALUTs	17 / 12,480 (< 1 %)
Dedicated logic registers	4 / 12,480 (< 1 %)
Total registers	4
Total pins	7 / 343 (2 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

```
Type  Message
      Info: Running Quartus II Simulator
      Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off problem2_17201066 -c problem2_17201066
```

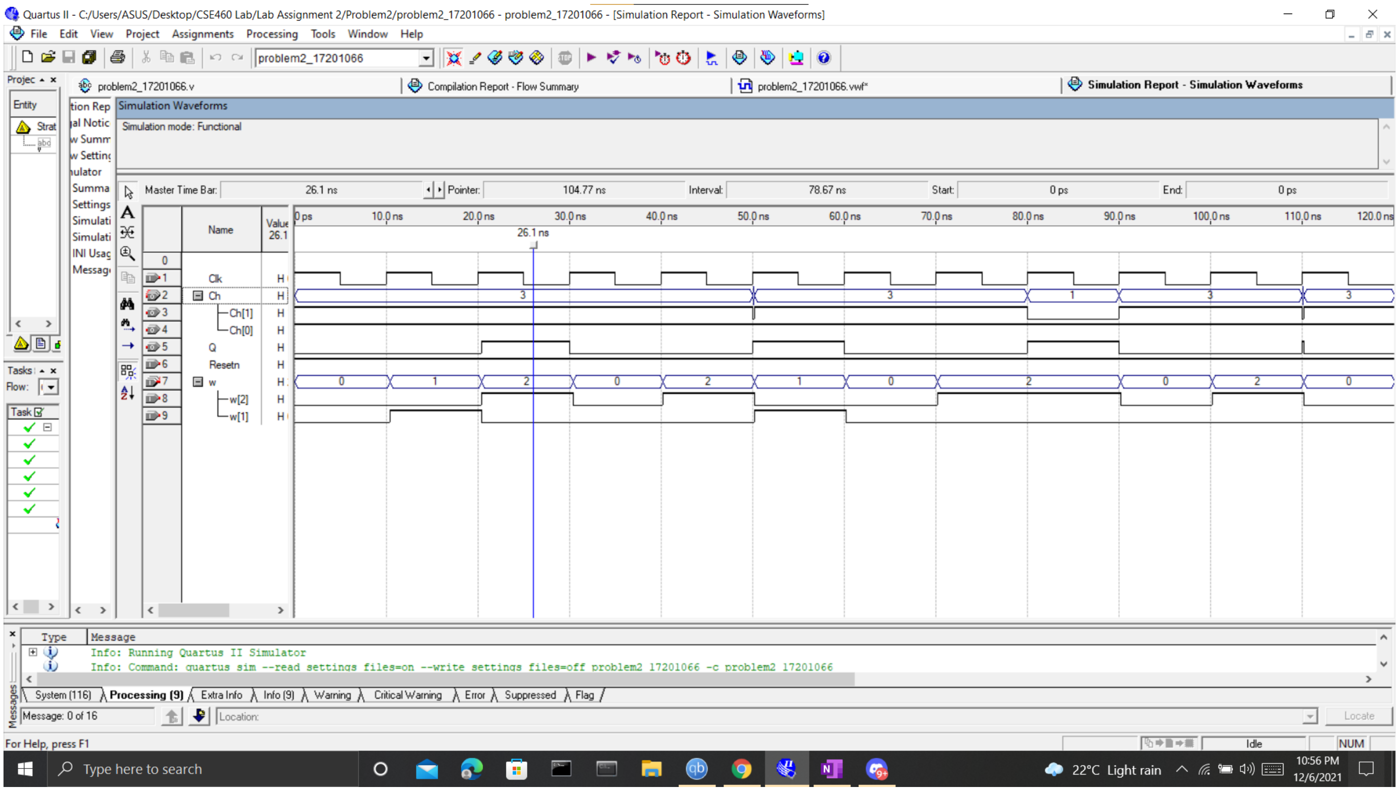
Simulation:



Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem2/problem2_17201066 - problem2_17201066 - [problem2_17201066.vwf*]

Master Time Bar: 120.0 ns Pointer: 115.93 ns Interval: -4.07 ns Start: 0 ps End: 120.0 ns

```
Type  Message
      Info: Running Quartus II Simulator
      Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off problem2_17201066 -c problem2_17201066
```



Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem2/problem2_17201066 - problem2_17201066 - [Simulation Report - Simulation Waveforms]
File Edit View Project Assignments Processing Tools Window Help
problem2_17201066
problem2_17201066.v
Compilation Report - Flow Summary
problem2_17201066.vwf*
Simulation Report - Simulation Waveforms
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 26.1 ns
Pointer: 104.77 ns
Interval: 78.67 ns
Start: 0 ps
End: 0 ps
Name
Value 26.1
Clk
Ch
Ch[1]
Ch[0]
Q
Resetn
w
w[2]
w[1]
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
100.0 ns
110.0 ns
120.0 ns
26.1 ns
3
3
1
3
3
0
1
2
0
2
1
0
2
0
2
0

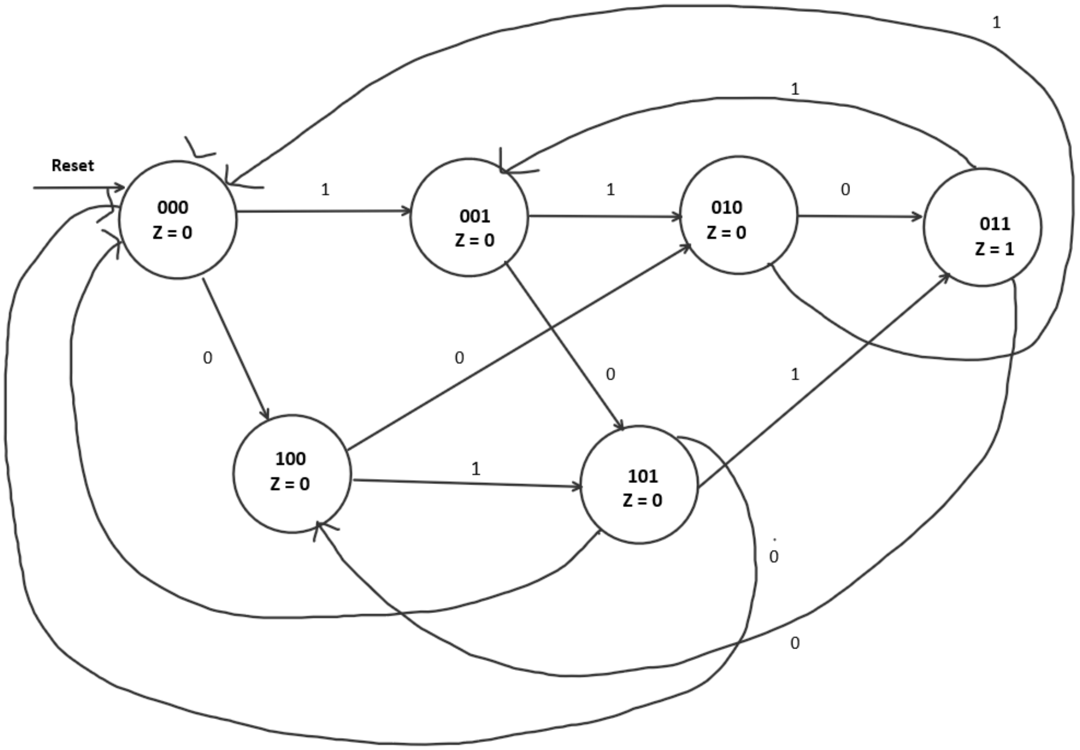
Type | Message

```
Info: Running Quartus II Simulator
Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off problem2_17201066 -c problem2_17201066
```

From the table it is clear that the FSM is a mealy machine. Here W is a 2bit input variable that takes a random value. Ch variable defines the amount of change. Finally the Q variable describes the acceptance. The input 00 means no money, 01 means 1 taka and 10 is 3 taka. In the timing diagram, between 0 to 30ns the values of w are 00, 01 and 10. After receiving this input in the state diagram 01 state moves to 00 state. Since it is a mealy machine. The transition from 01 state to 10 state gives the output Q = 1 but since 00, 01 and 10 means 4taka, the change will be 11 which also means no change. Because of this operation the output between 20 to 30 ns is high. At 50 to 60 ns the output at the timing diagram is also high because before achieving the accepted transition the inputs are 00, 10, 01. So the machine receives 4tk and gives high output without any change. From t7 to t9 (60 - 90ns) the machine receives input 00, 10, 10. When 00 state gets 10 input it moves to state 11 and when state 11 receives 10 input it moves back to state 00 with accepted transition. So when the timing diagram gives high output at t9 (80 - 90ns). The machine accepts 4tk but in this case the machine received 10 and 10 which means 6tk. So there will be value in change. So at 80 to 90ns the Value of Ch is 01. So the change is 2tk.

Problem 3

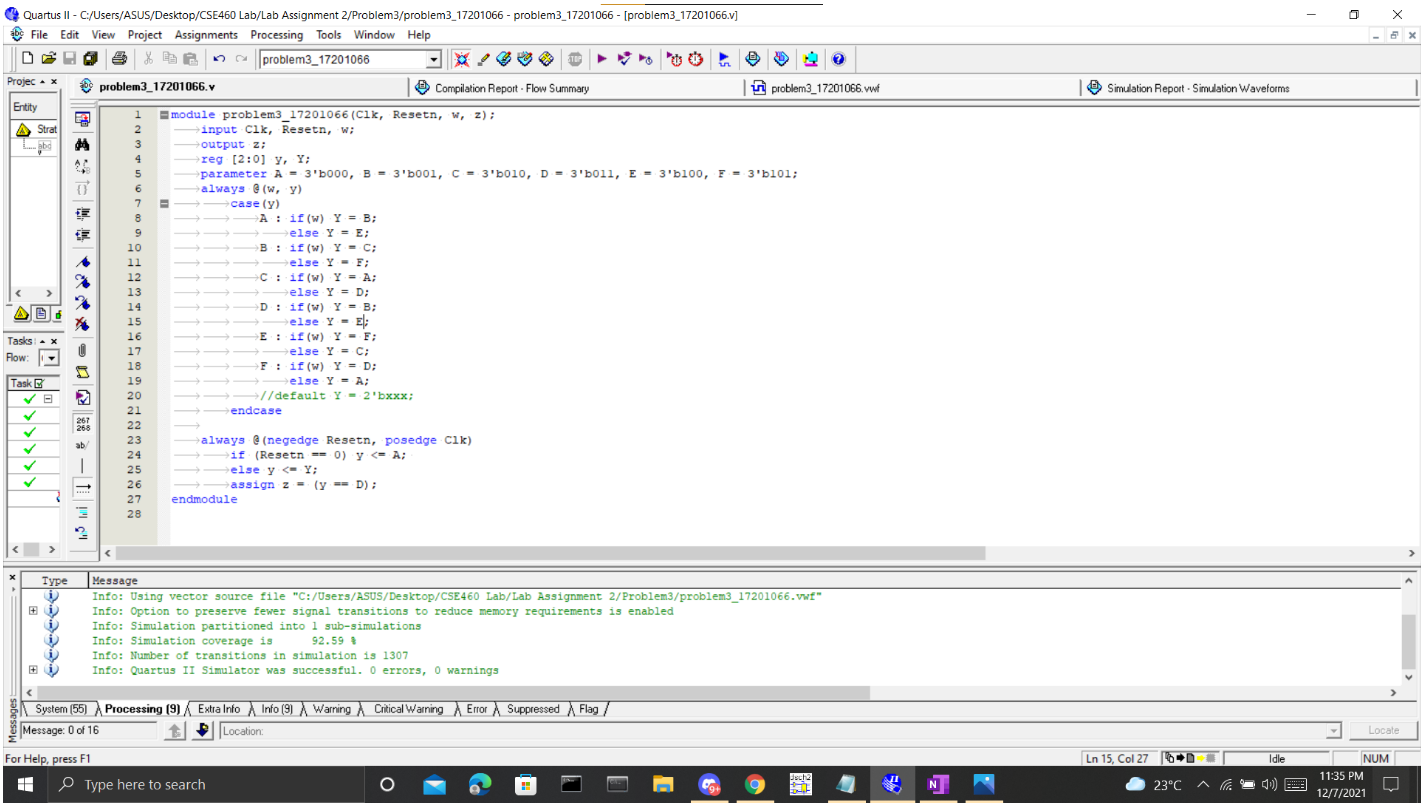
The State Diagram:



the state-assigned table:

Current State y3y2y1	Next state w=0 Y3Y2Y1	Next state w=1 Y3Y2Y1	Output z
000	100	001	0
001	101	010	0
010	011	000	0
011	100	001	1
100	010	101	0
101	000	011	0

Verilog code:

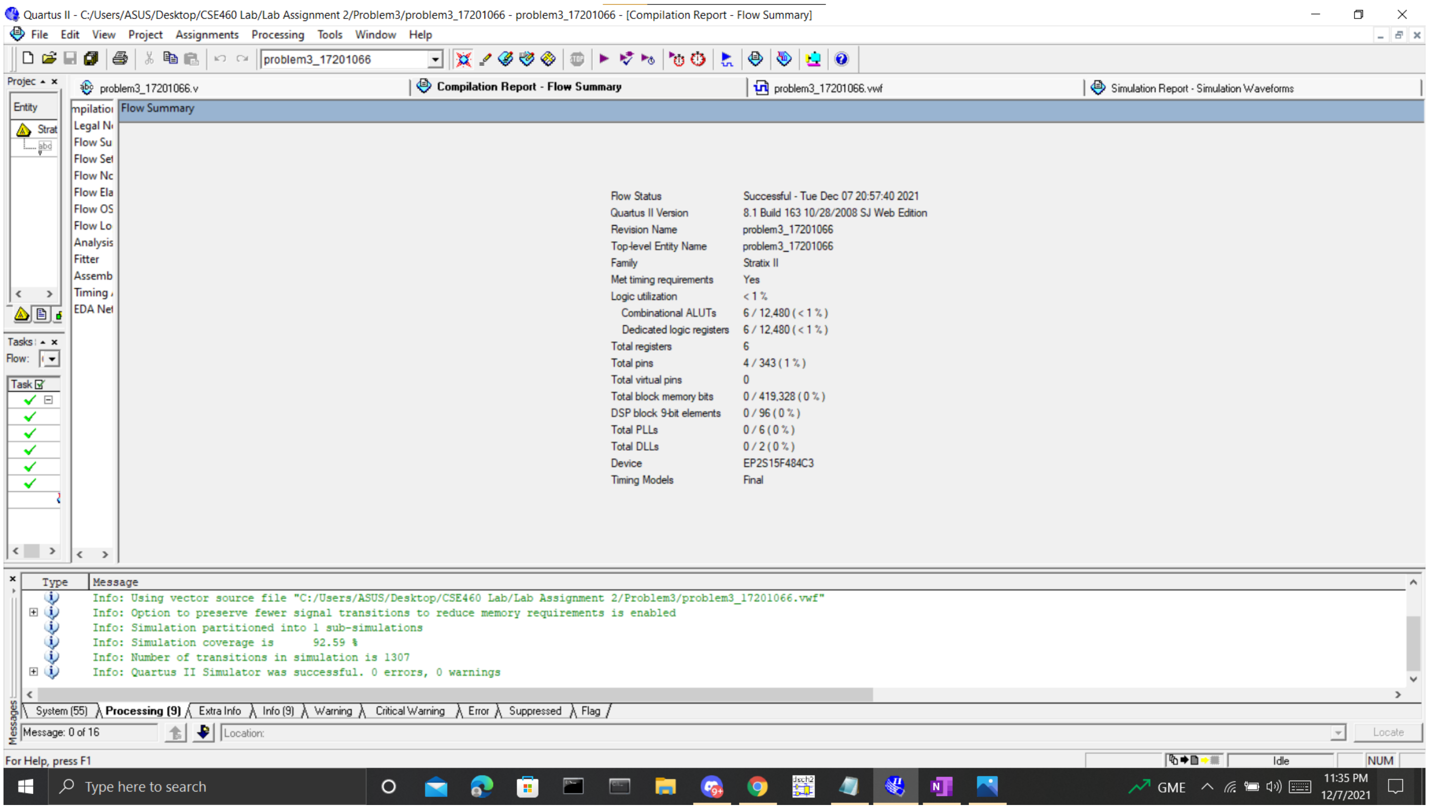


Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem3/problem3_17201066 - problem3_17201066 - [problem3_17201066.v]

```verilog
module problem3_17201066(Clk, Resetn, w, z);
	input Clk, Resetn, w;
	output z;
	reg [2:0] y, Y;
	parameter A = 3'b000, B = 3'b001, C = 3'b010, D = 3'b011, E = 3'b100, F = 3'b101;
	always @(w, y)
		case(y)
			A : if(w) Y = B;
				else Y = E;
			B : if(w) Y = C;
				else Y = F;
			C : if(w) Y = A;
				else Y = D;
			D : if(w) Y = B;
				else Y = E;
			E : if(w) Y = F;
				else Y = C;
			F : if(w) Y = D;
				else Y = A;
			//default Y = 2'bxxx;
		endcase
	
	always @(negedge Resetn, posedge Clk)
		if (Resetn == 0) y <= A;
		else y <= Y;
		assign z = (y == D);
endmodule
```

```
Info: Using vector source file "C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem3/problem3_17201066.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is      92.59 %
Info: Number of transitions in simulation is 1307
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

File Edit View Project Assignments Processing Tools Window Help
problem3_17201066
problem3_17201066.v
Compilation Report - Flow Summary
problem3_17201066.vwf
Simulation Report - Simulation Waveforms
System (55) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
Locate
For Help, press F1
Ln 15, Col 27
Idle
NUM
Type here to search
23°C
11:35 PM
12/7/2021



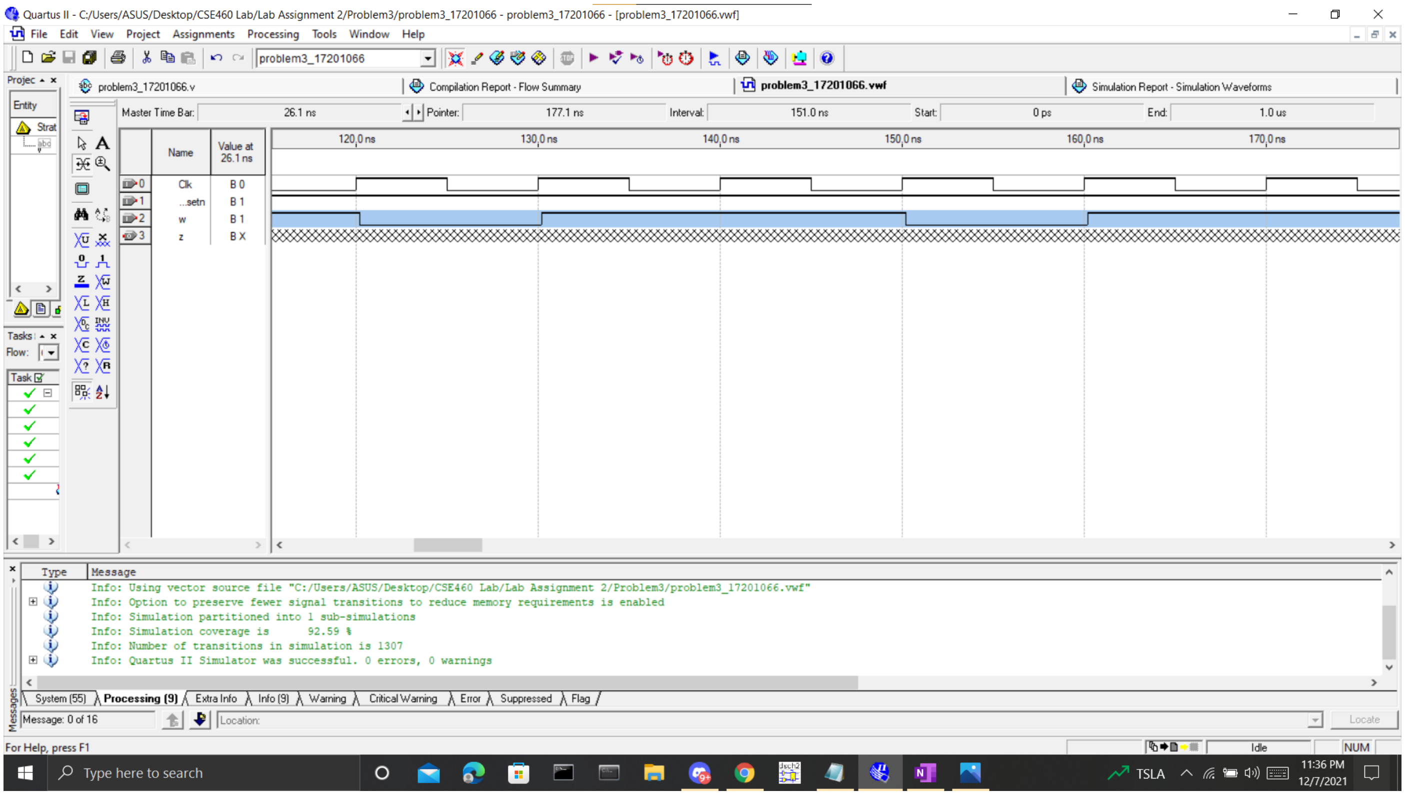
Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem3/problem3_17201066 - problem3_17201066 - [Compilation Report - Flow Summary]

Flow Summary

Flow Status	Successful - Tue Dec 07 20:57:40 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem3_17201066
Top-level Entity Name	problem3_17201066
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	6 / 12,480 (< 1 %)
Dedicated logic registers	6 / 12,480 (< 1 %)
Total registers	6
Total pins	4 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

```
Info: Using vector source file "C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem3/problem3_17201066.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is      92.59 %
Info: Number of transitions in simulation is 1307
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

Simulation:



Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem3/problem3_17201066 - problem3_17201066 - [problem3_17201066.vwf]

File Edit View Project Assignments Processing Tools Window Help
problem3_17201066
problem3_17201066.v
Compilation Report - Flow Summary
problem3_17201066.vwf
Simulation Report - Simulation Waveforms

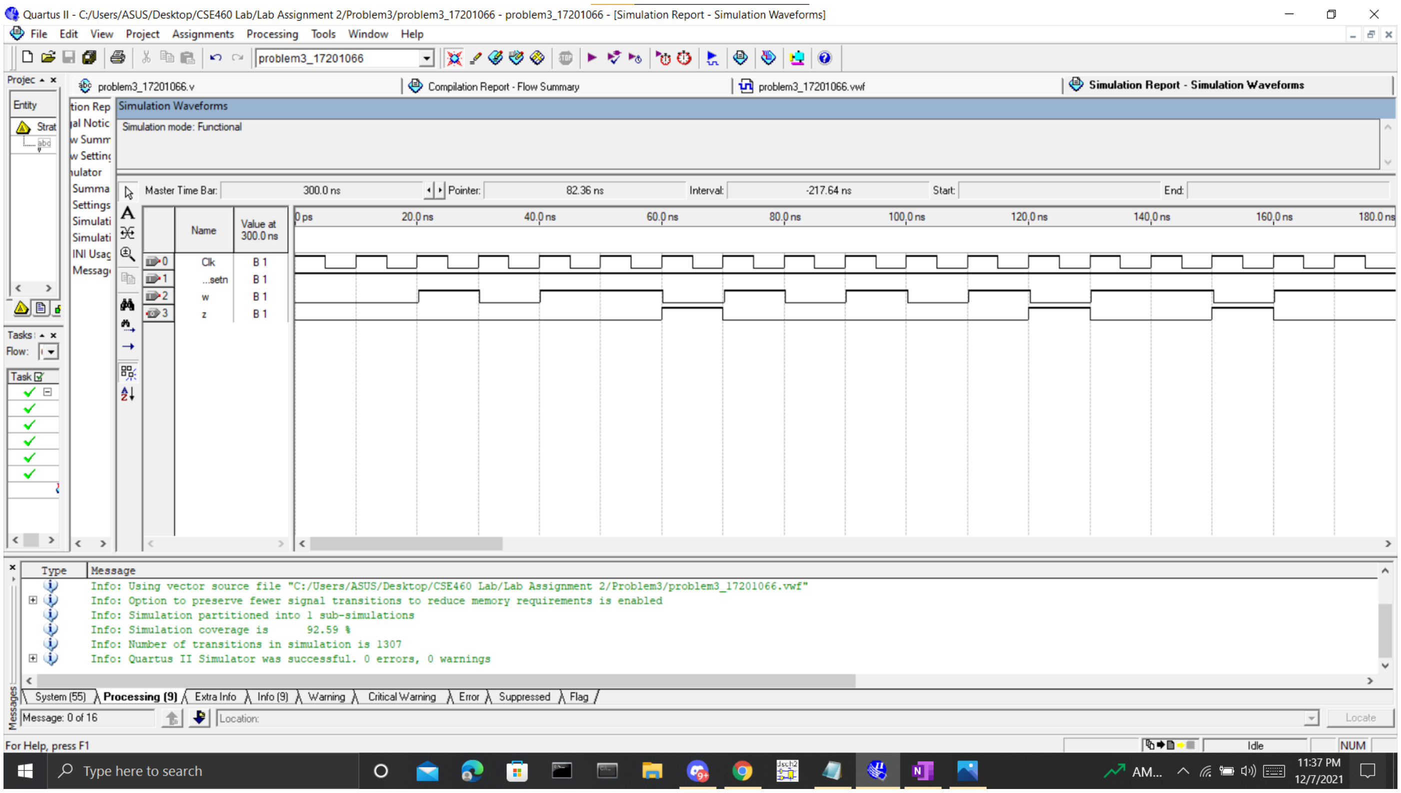
Master Time Bar:	Pointer:	Interval:	Start:	End:
26.1 ns	177.1 ns	151.0 ns	0 ps	1.0 us

	Name	Value at 26.1 ns
0	Clk	B 0
1	...setn	B 1
2	w	B 1
3	z	B X

120.0 ns
130.0 ns
140.0 ns
150.0 ns
160.0 ns
170.0 ns

```
Type  Message
      Info: Using vector source file "C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem3/problem3_17201066.vwf"
      Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
      Info: Simulation partitioned into 1 sub-simulations
      Info: Simulation coverage is      92.59 %
      Info: Number of transitions in simulation is 1307
      Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

System (55) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
For Help, press F1
Idle
NUM
Type here to search
TSLA
11:36 PM
12/7/2021



Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem3/problem3_17201066 - problem3_17201066 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help
problem3_17201066
problem3_17201066.v
Compilation Report - Flow Summary
problem3_17201066.vwf
Simulation Report - Simulation Waveforms
Simulation Waveforms

Simulation mode: Functional

Master Time Bar:	Pointer:	Interval:	Start:	End:
300.0 ns	82.36 ns	-217.64 ns		

	Name	Value at 300.0 ns
0	Clk	B 1
1	...setn	B 1
2	w	B 1
3	z	B 1

```
Type  Message
      Info: Using vector source file "C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 2/Problem3/problem3_17201066.vwf"
      Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
      Info: Simulation partitioned into 1 sub-simulations
      Info: Simulation coverage is      92.59 %
      Info: Number of transitions in simulation is 1307
      Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

System (55) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
For Help, press F1
Idle
NUM
Type here to search
AM...
11:37 PM
12/7/2021

The FSM is a moore machine. In this case overlapping is not allowed so after finishing a three-bit sequence there will be a reset. In the timing diagram, at first in a 3 bit sequence the machine receives 001 input. For 0 state 000 moves to state 100. Then after receiving 0, 100 moves to state 010. FInally when it gets 1 it is clear that the number of 1s can not be even so it moves to reset state 000. Since it is more machine and input 001 the machine does not reach to state 011, the output signal at t4 (30 - 40ns) is low. Another 3 bit sequence starts from that same time interval at 000 state. For input of 011, 000 reach 100 then 101 to 011. 011 is the state where z = 1. So, the timing shows high output at the t7 (60 - 70ns) interval. After that the machine receives 010 input. As the number 1s is odd it does not reach to the 011 state so the output becomes z = 0 at (90 - 100ns) intervals. Then for 101 input for 0, 000 moves to 001. Sequentially for 001 moves to 101 state and for 1 input 101 moves to 011. Like before 011 state gives output z = 1. So the output value is high at (120 - 130ns). Similarly, between (150 - 160ns) output is high due to 011 input sequence.