

CSE460L: Assignment 04

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Section: 02

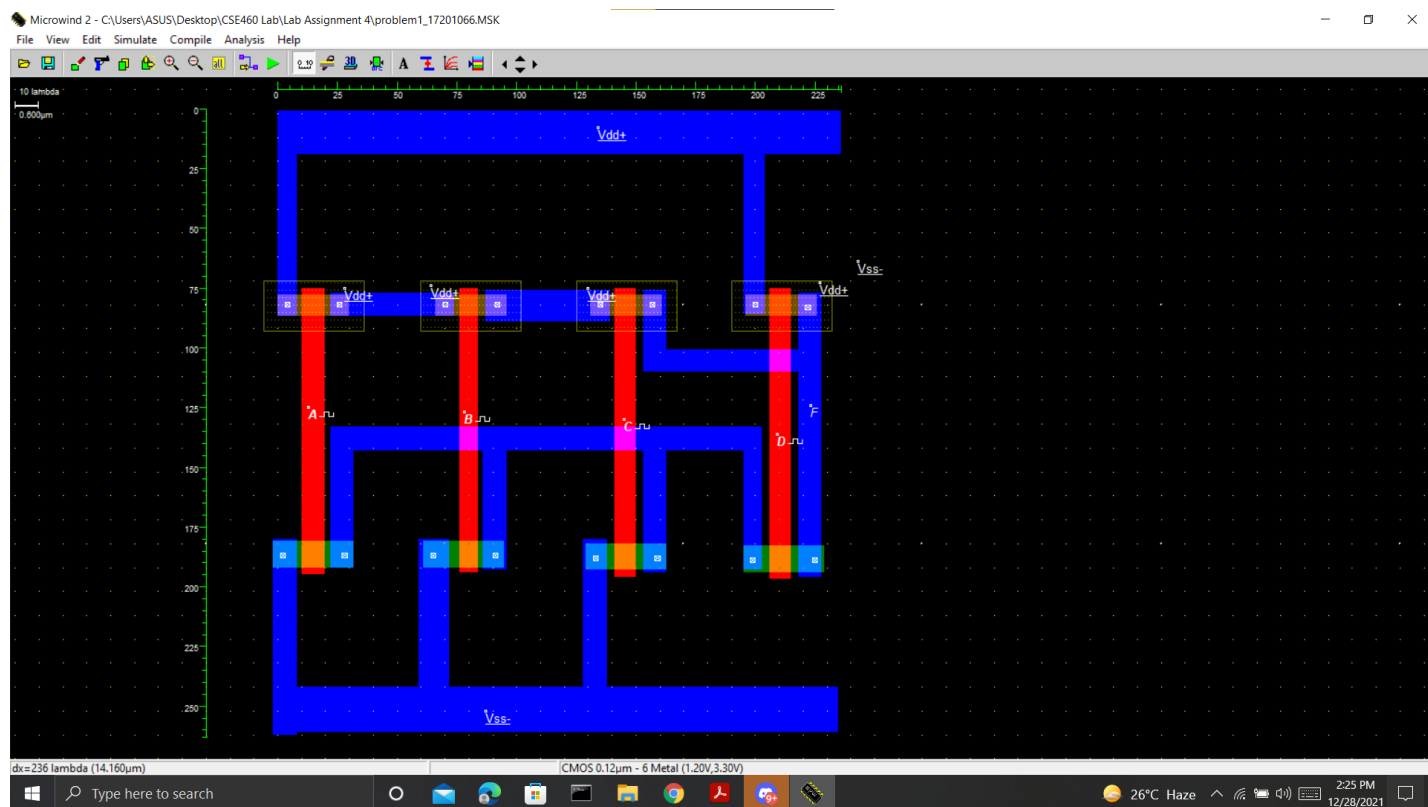
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Problem 1:

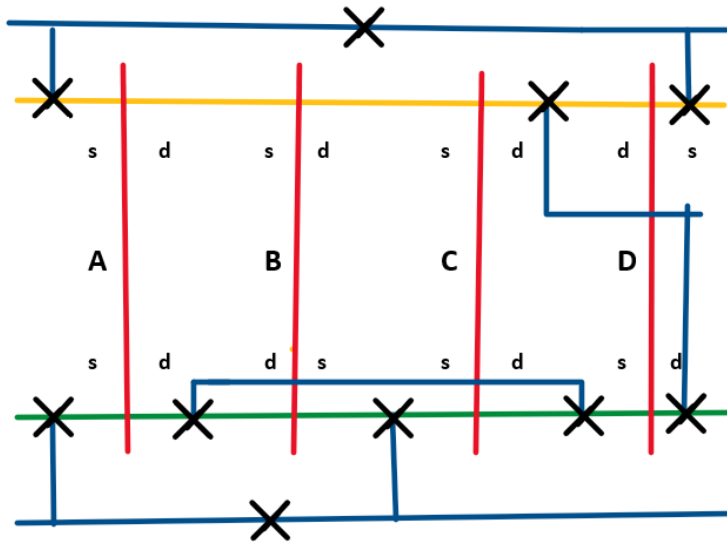
The logical expression:

$$Y = \overline{(A+B+C)D}$$

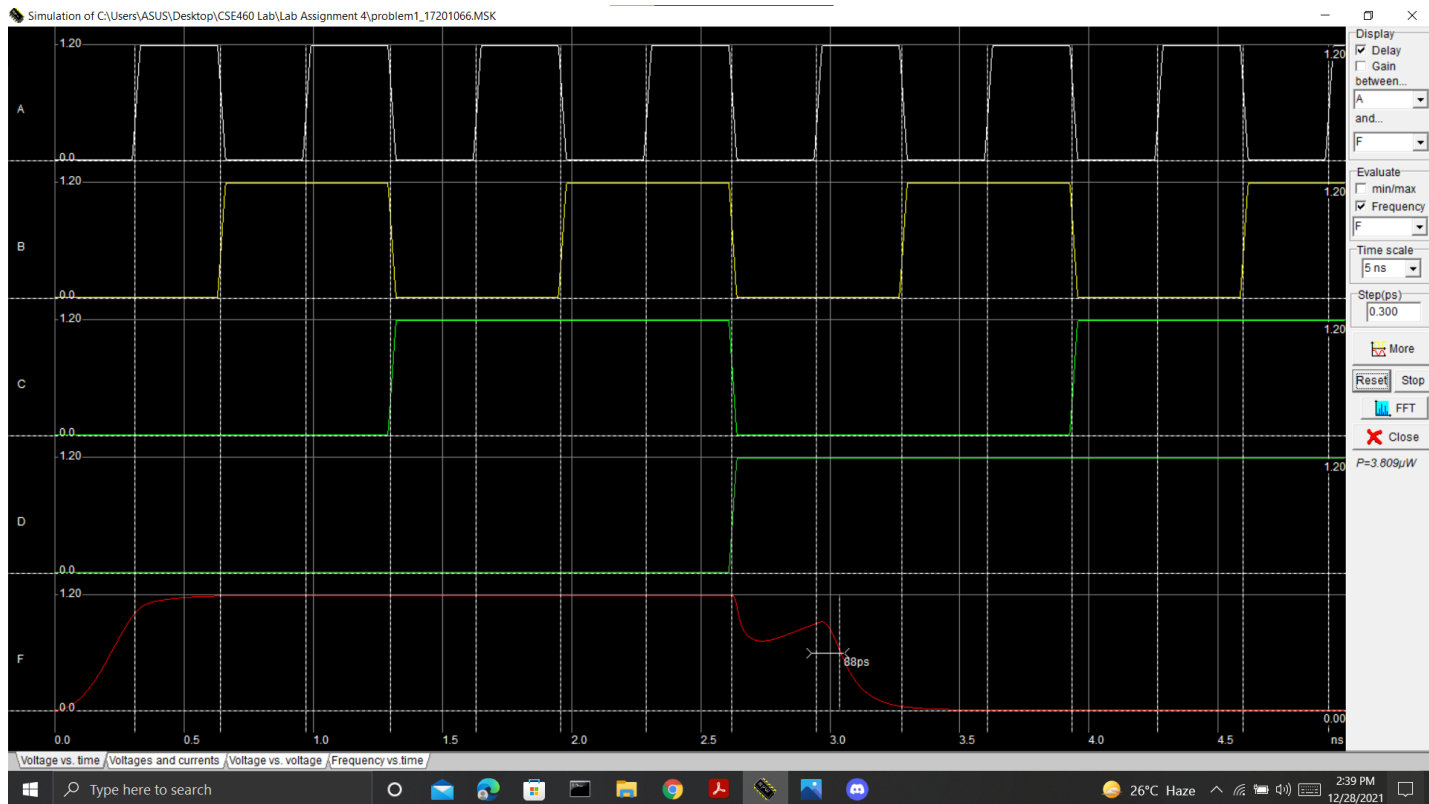
The layout (without using the MOS generator from the design palette) of the Logic Circuit in Microwind2:



Stick Diagram of the given Logical Circuit:



Time Diagram Generated From Microwind2:



Discussion:

Here in the Microwind2 the dimensions of the circuit are,

Width (Vertical) = 263

Height/Length (Horizontal) = 237

For scale 10 lambda and 0.600 micrometer,

Width = 15.78 micrometer

Height/Length = 14.22 micrometer

So, in microwind2 the area of the circuit will be $15.78 \times 14.22 = 224.3916 \text{ micrometer}^2$

For the stick diagram, the theoretical,

Width = $5 \times 10 \text{ lambda}$

Height/Length = $6 \times 10 \text{ lambda}$

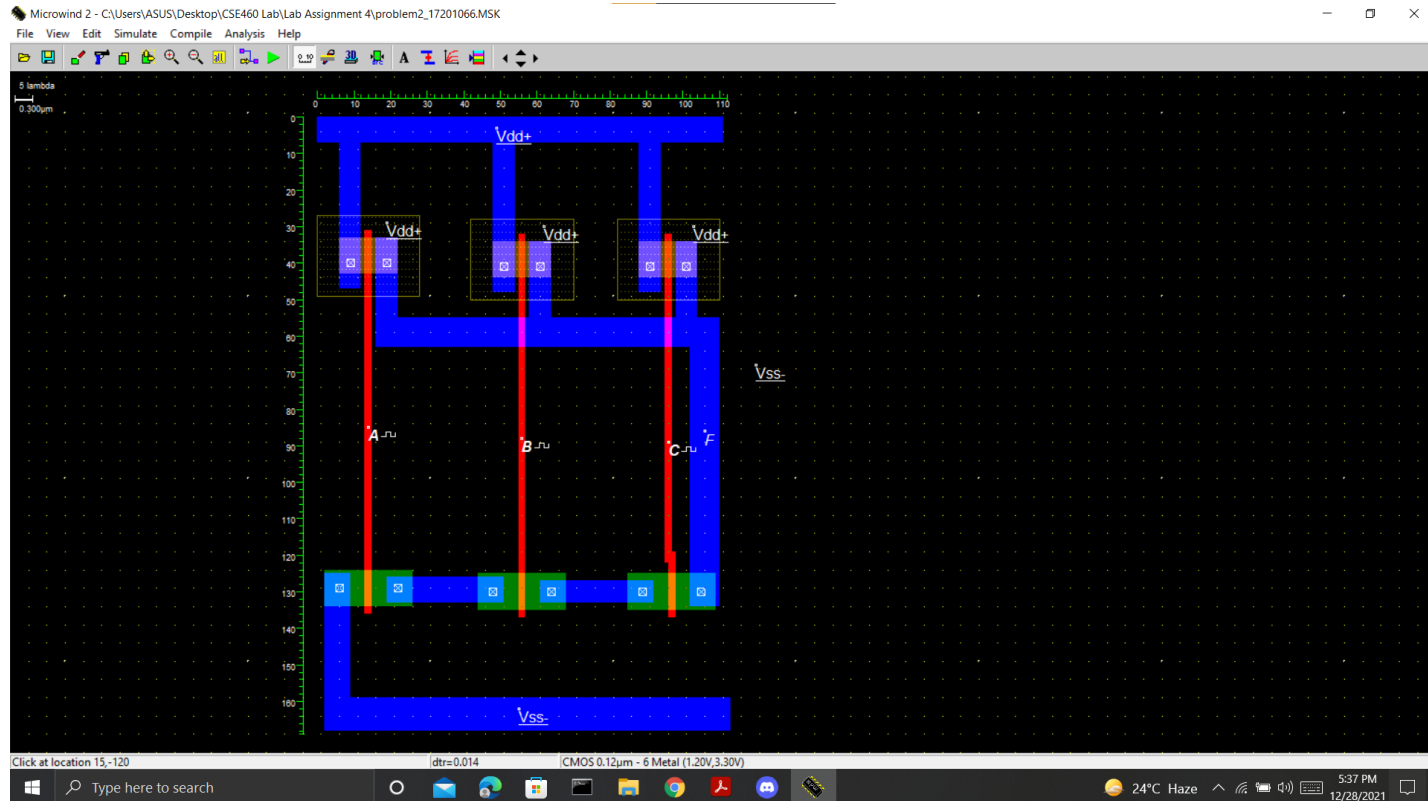
10 Lambda = 0.600 micrometer

Area = $5 \times 6 \times 0.600 \times 0.600 = 10.8 \text{ micrometer}^2$

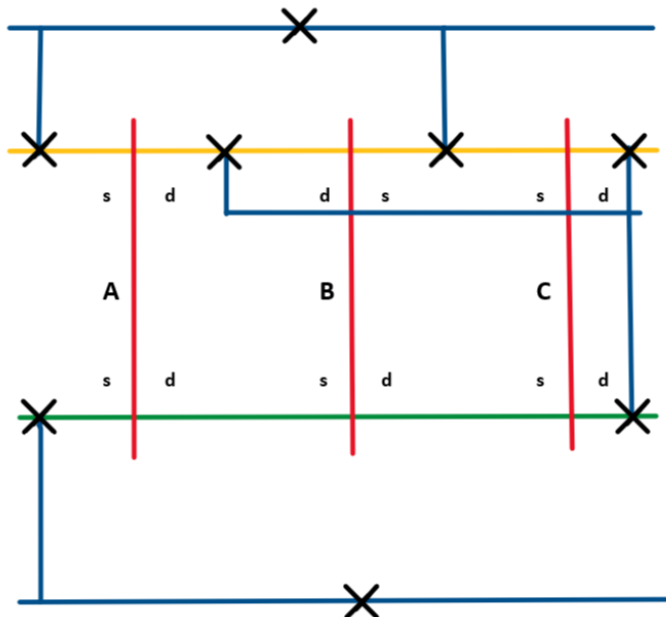
So here we can see that, the area we computed from Microwind2, is 20.77 times bigger than the Theoretical stick diagram best case result.

Problem 2:

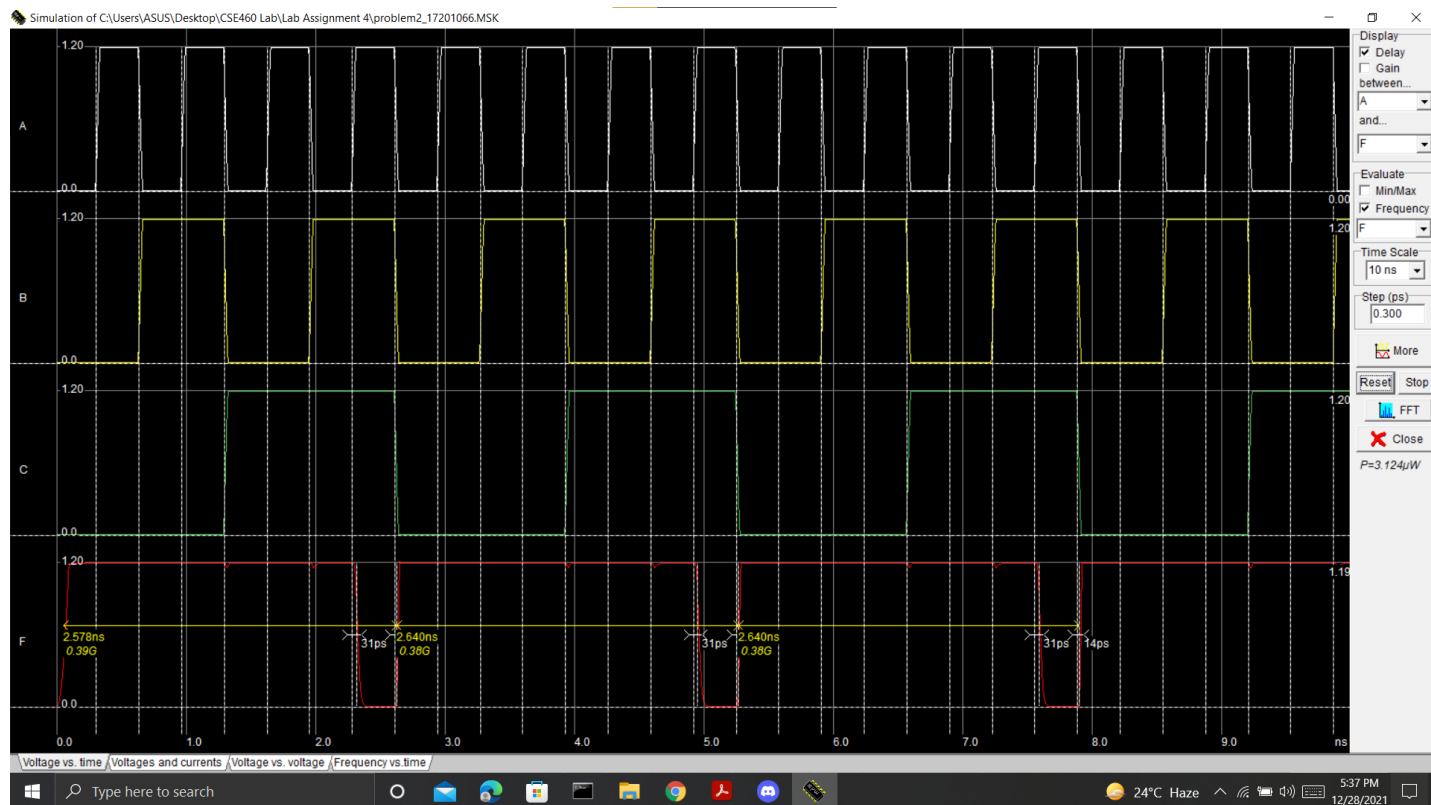
The layout of a 3-input NAND gate using the MOS generator from the design palette in Microwind:



Stick Diagram of the given Logical Circuit:



Time Diagram Generated From Microwind2:



Discussion:

Here in the Microwind2 the dimensions of the circuit are,

Width (Vertical) = 169

Height/Length (Horizontal) = 112

For scale 5 lambda and 0.300 micrometer,

Width (Vertical) = 10.14 micrometer

Height/Length (Horizontal) = 6.72 micrometer

So, in microwind2 the area of the circuit will be $10.14 \times 6.72 = 68.141$ micrometer².

For the stick diagram, the theoretical,

Width = $4 \times 5 \lambda$

Height/Length = $5 \times 5 \lambda$

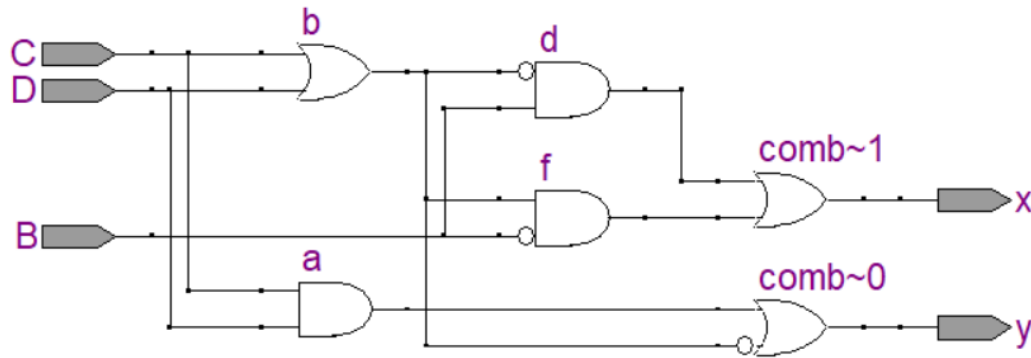
$5 \lambda = 0.300$ micrometer

Area = $4 \times 5 \times 0.300 \times 0.300 = 1.8$ micrometer²

So here we can see that, the area we computed from Microwind2, is 37.85 times bigger than the Theoretical stick diagram best case result.

Problem 3:

The logical Circuit:



Verilog Code:

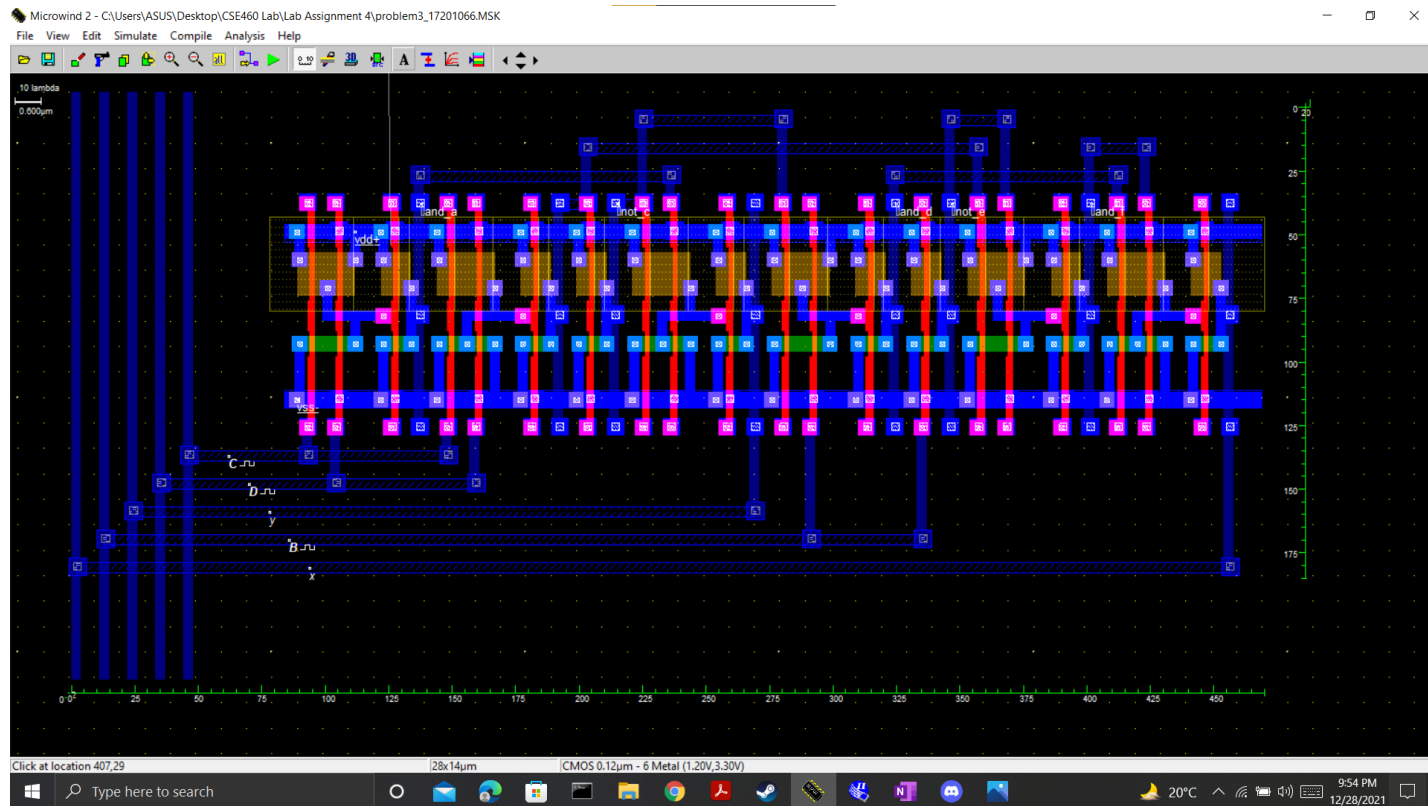
```
Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 4/Problem3_17201033/problem3_17201066 - problem3_17201066.v [problem3_17201066.v]
File Edit View Project Assignments Processing Tools Window Help
problem3_17201066.v problem3_17201066.vwf Simulation Report - Simulation Waveforms Compilation Report - Flow Summary

1 module problem3_17201066(B, C, D, y, x);
2     input B, C, D;
3     output x, y;
4     and(a, C, D);
5     or(b, C, D);
6     not(c, b);
7     or(y, c, a);
8     and(d, c, B);
9     not(e, B);
10    and(f, b, e);
11    or(x, d, f);
12 endmodule

Type Message
Info: Running Quartus II EDA Netlist Writer
Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off problem3_17201066 -c problem3_17201066
Info: Generated files "problem3_17201066.vo" and "problem3_17201066_v.sdo" in directory "C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 4/Problem3_17201033/simulation/custom/" for EDA simulation tool
Info: Generated files "problem3_17201066.vo" and "problem3_17201066_v.sdo" in directory "C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assignment 4/Problem3_17201033/timing/custom/" for EDA timing analysis tool
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 14 warnings

System (6) Processing (65) Extra Info (51) Warning (14) Critical Warning Error Suppressed (6) Flag /
Message: 0 of 129 Location:
For Help, press F1
Ln 1, Col 1 Idle NUM
Type here to search 20°C 9:35 PM 12/28/2021
```

The layout generated from the verilog code:



Discussion:

Here in the Microwind2 the dimensions of the circuit are,

Width (Vertical) = 185

Height/Length (Horizontal) = 470

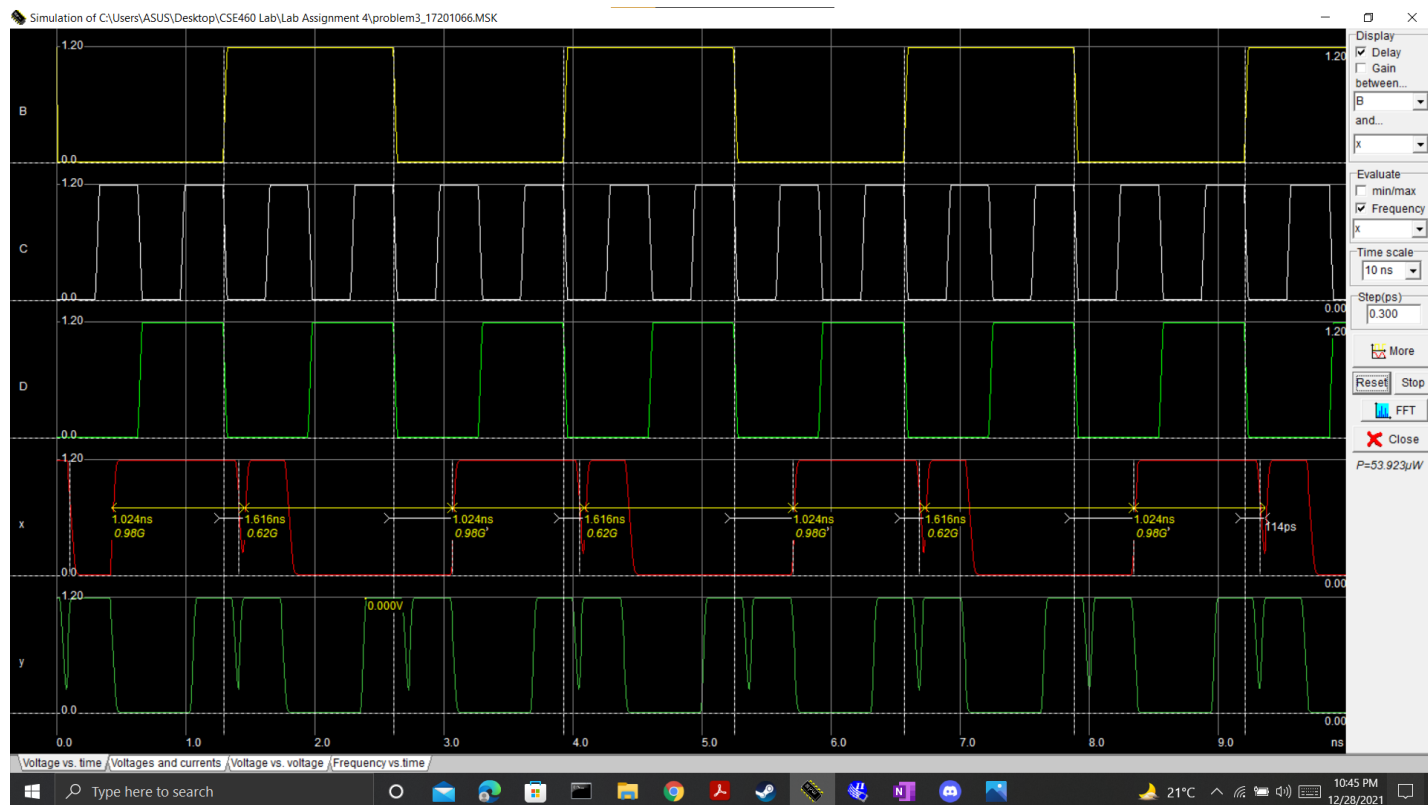
For scale 10 lamda and 0.600 micrometer,

Width (Vertical) = 11.1 micrometer

Length (Horizontal) = 28.2 micrometer

So, in microwind2 the area of the circuit will be $11.1 \times 28.2 = 313.02 \text{ micrometer}^2$.

Time Diagram Generated From Microwind2:



The logical expression of the above logical circuit,

$$y = ((C + D)' + CD)$$

$$x = B'(C + D) + B(C + D)'$$

Truth Table of the above logical expression:

B	C	D	y	x
0	0	0	1	0
1	0	0	1	1
0	1	0	0	1
1	1	0	0	0
0	0	1	0	1
1	0	1	0	0

0	1	1	1	1
1	1	1	1	0

Discussion:

Verifying the value of x:

In the microwind2 time diagram, between (4.0 - 5.0)ns time interval when,

B = 1, C = 0 and D = 1

The value of x = 0.

In the truth table, we can see the value of x is 0 when B = 1, C = 0 and D = 1.

Again, at (6.0 - 6.5)ns the value of x is 1 while B = 0, C = 1 and D = 1

The truth table above gives the similar result for B = 0, C = 1 and D = 1.

Verifying the value of y:

In the microwind2 generated time diagram, between (0.0 - 1.0)ns time interval for

B = 0, C = 0 and D = 1, the value of y is 0.

In the truth table, we can see the value of y is 0 when B = 0, C = 0 and D = 1.

Similarly, between (2.0 - 3.0)ns when B = 1, C = 1, D = 1, the output y = 1. Again, the above truth table shows us the similar result y = 1 for B = 1, C = 1, D = 1.

Clearly, the theoretically calculated result from the logical expression and the result we received from microwind2 is almost the same in spite of having some delay issue in Microwind2.