CSE460L: Assignment 4 (Fall 2021)

Sections: 1, 2, 3, 4, 5, 6, 7, 8 & 9

Assignment 4 submission link:
https://docs.google.com/forms/d/1PBZBxcTm3m2HV_AAXGHGiFaJUojDjfI5ssngcsJBRFM/edit?usp=sharing

Assignment 4 deadline: **Dec 29, 2021**

General guidelines

- Assignments are individual

- Each assignment will contain 3 to 4 problems

- **For each problem you will need to prepare 3 parts:**

  1. **Code / Schematic Diagram / Layout:** attach a screenshot of your code from *Quartus* or the circuit schematic diagram from *dsch2* or layout from *microwind2* as applicable.

  2. **Output: <u>attach *FULL SCREEN* screenshots</u>** of
  For *Quartus*:
     - Compilation Report - Flow Summary (Compilation report of the .v file)
     - Simulation Report - Simulation Waveforms (Simulation report of the .vwf file)

  For *dsch2 / microwind2*:
     - Simulation Report - Simulation Waveforms (Timing diagrams of inputs & outputs)

  [**Tampered/edited/cropped screenshots will be considered as a violation of general guidelines and therefore will not be accepted**]

  3. **Discussion/Explanation:** Explain the output waveforms of your simulation report as described in the **Expected Output** section within each problem statement.

- Each problem will be of equal points. You will not be graded on the length/number of code/diagrams/explanation/outputs; rather on the clarity, readability and precise explanations of your code/diagrams/logic/outputs.

- Points distribution for each problem is

Code / Schematic Diagram / Layout: **40%**
Output: **20%**
Discussion/Explanation of output: **40%**

- **You will need to create separate directories/project for each problem**

- **The name of your working directory for each problem of the assignment should be …\problem#_StudentID [# = 1/2/3/4/5/6/7]**
  For example, for problem 1 the name of the directory should be problem1_1406066
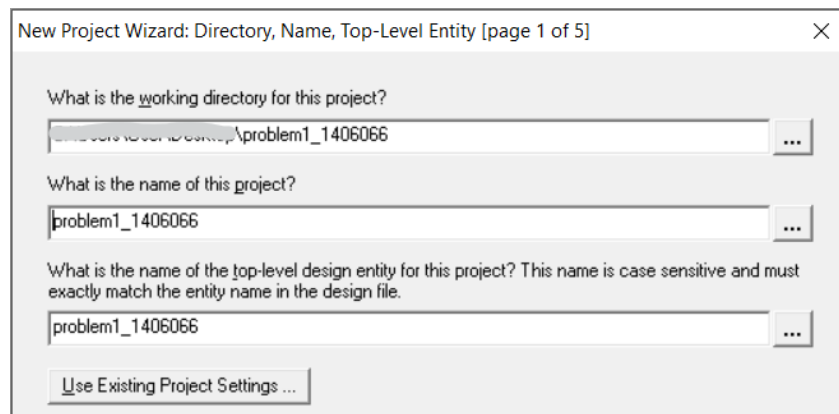
- Consequently, the name of your main module in the Verilog file should be problem#_StudentID [# = 1/2/3/4/5/6/7]
  Continuing from the previous example, the name of the module should be problem1_1406066

- Finally, **compile all the problems for a given assignment into a single pdf file**

- The **name of the pdf should be Section_StudentID_assignment4.pdf** (Example: 1_1406066_assignment4.pdf)

Problems for Assignment 4

1. Draw the layout (without using the MOS generator from the design palette) of the logic circuit in correspondence with it's stick diagram defined by the following expression:

$$Y = \overline{(A+B+C)D}$$

Clear all the design errors (DRC) and determine the area of your designed layout.
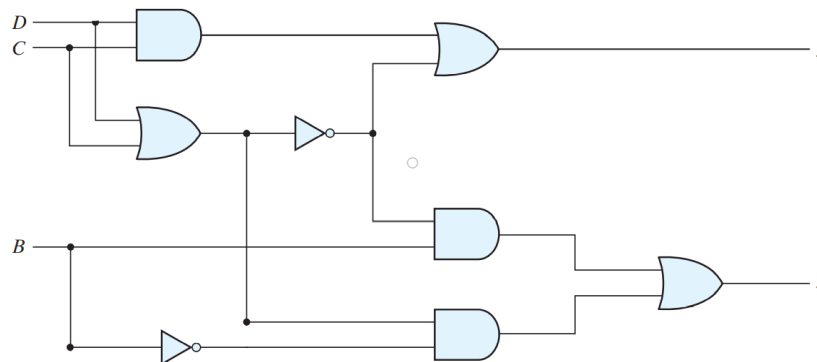
Expected Output:

Draw the stick diagram of the circuit. Determine the height, width and area of the stick diagram and compare them with the corresponding parameters derived from your design in Microwind. Attach the timing diagram with the time scale set to 5 ns.

2. Draw the layout of a 3-input NAND gate using the MOS generator from the design palette in Microwind. Clear all the design errors (DRC) and determine the area of your designed layout.

Expected Output:

Draw the stick diagram of the circuit. Determine the height, width and area of the stick diagram and compare them with the corresponding parameters derived from your design in Microwind. Attach the timing diagram with the time scale set to 10 ns.

3. Compile the layout using Microwind from the Verilog code of the following schematic diagram:

Expected Output:

Determine the height, width and area of the layout from your design. From your timing diagram, randomly choose two timestamps and verify the values of X and Y from both timestamps with your theoretical values calculated from the logic expressions.