CSE460L: Assignment 0

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Section: 02

Couse: CSE460

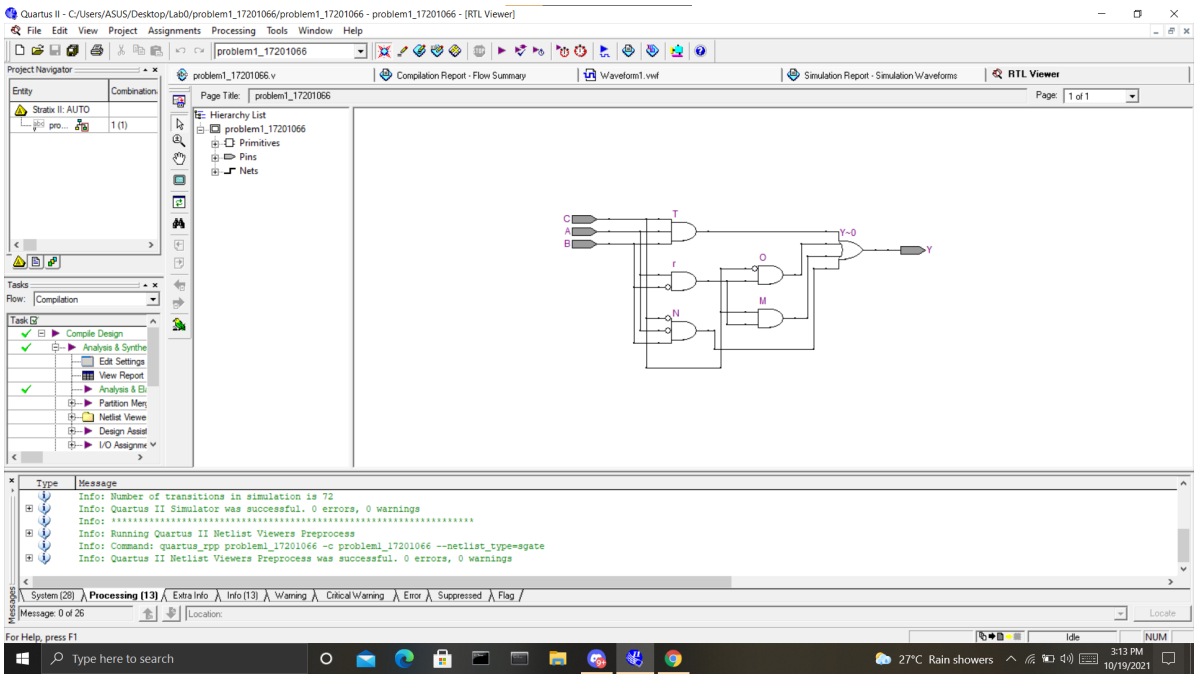
Problem 1: (a)

$$Y = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$$

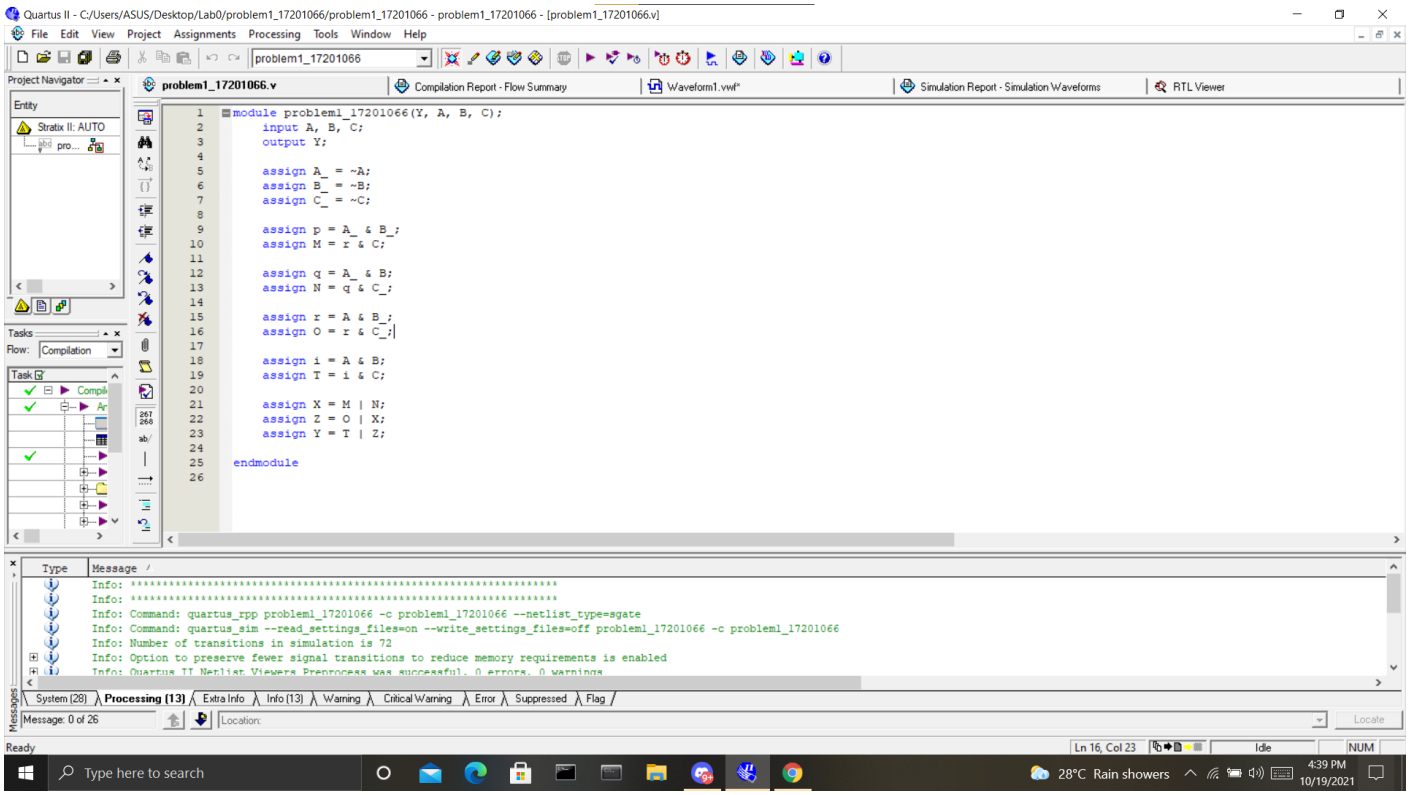
The truth table for the logic circuit expressed by the equation above:

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

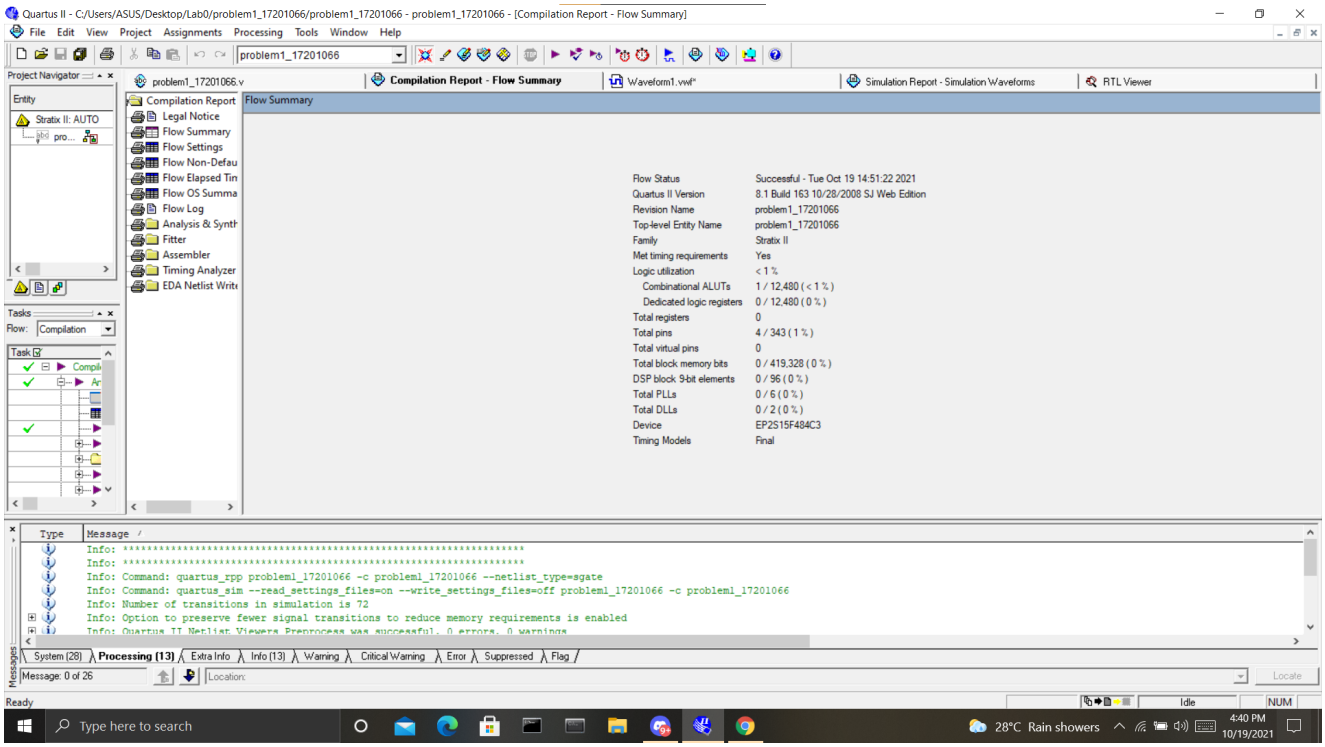
The output Y is the combination of four NOT Gates, five AND Gates and one OR Gate logic operations.



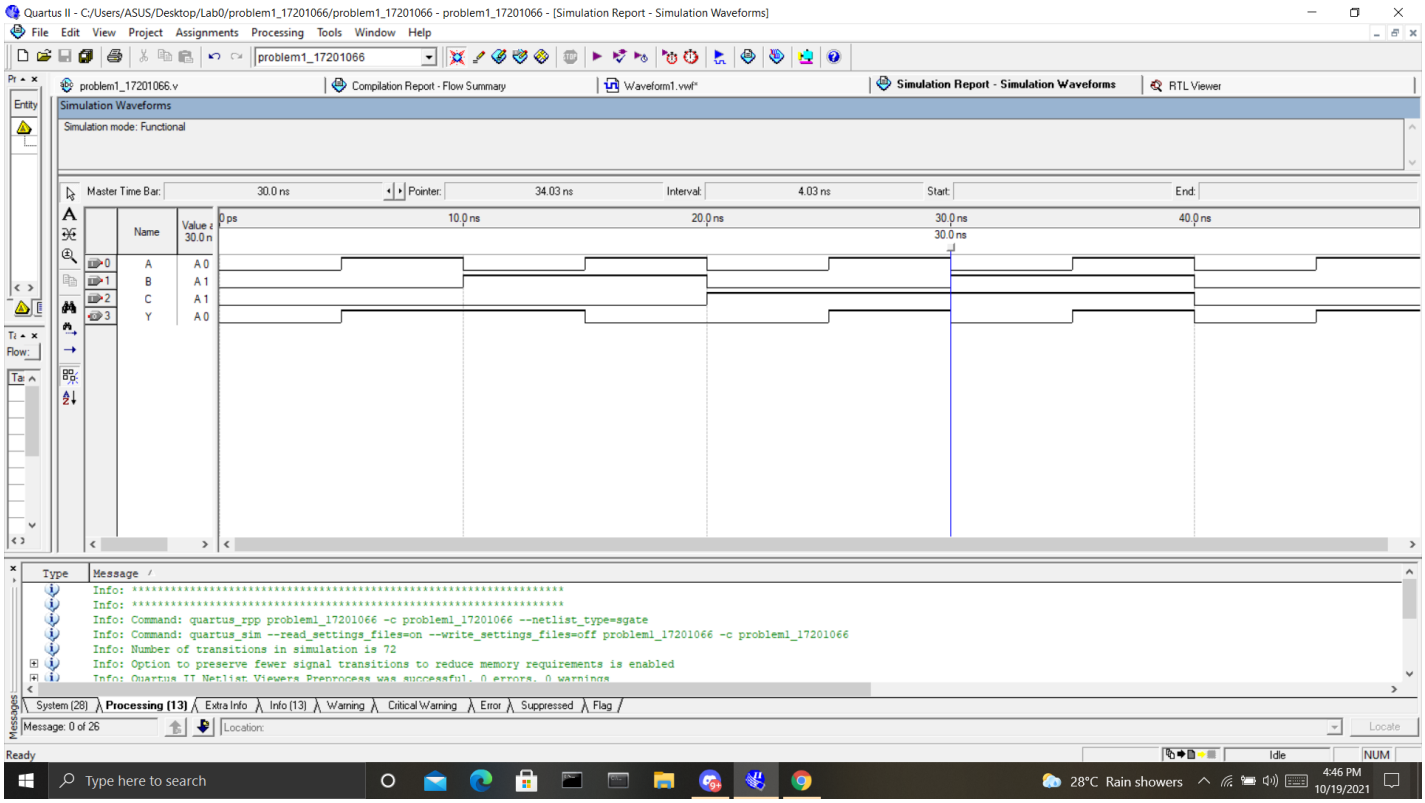
(b) Code for above logic circuit:



Summary:



Simulated Waveform for 50ns:



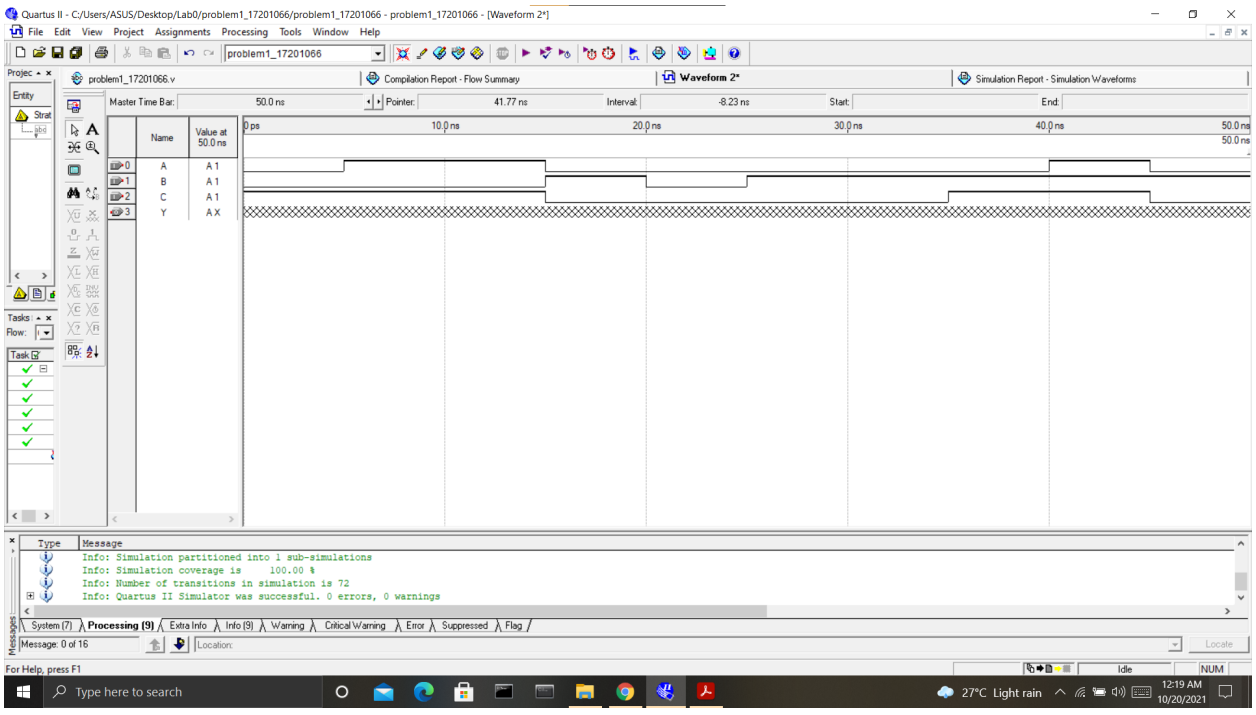
Truth table of the simulated result in Quartus II:

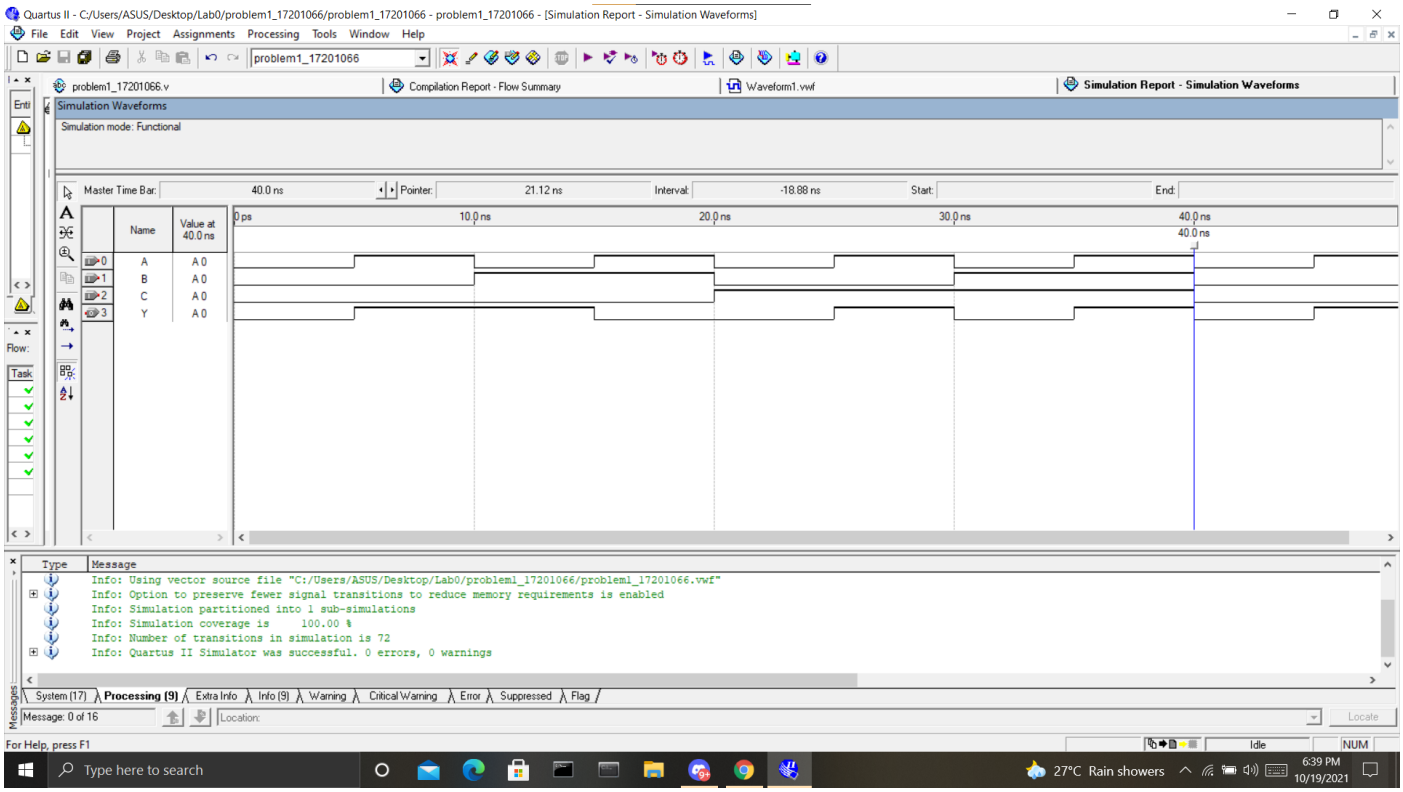
A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	0
1	1	1	1

In Quartus II, from the 5 to 10ns interval, the values of A, B, & C are 1, 0, 0 and for this the output of the logical expression Y is 1. Similarly, the output value, Y is 1 at the truth table for A, B and C are 1, 0, 0 respectively that have been computed in problem-1 (a) truth table.

From the 20 to 25ns interval, the Output value Y is 0 for A, B and C are 0, 0, and 1. However, from the truth table of problem 1(a), we can see. The output Y is 1 for A, B, and C are 0, 0, 1.

(c) Random value has been assigned to the input pins in Verilog at half grid intervals and performed the operation for 50 ns.





The truth table of the Quartus II simulation:

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	0
1	1	1	1

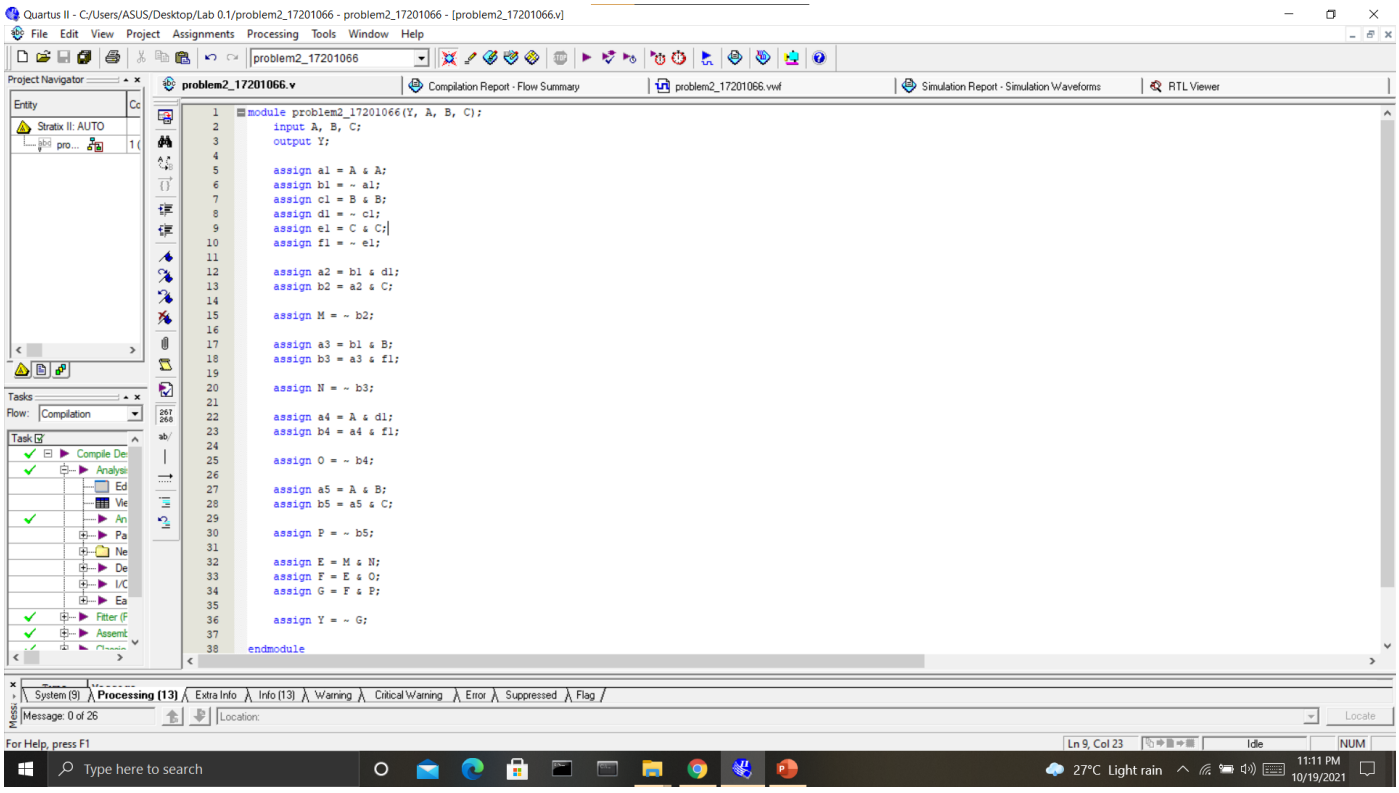
Applying random variables to each, we can see, between 5 to 10 ns, the values of A, B and C are 1, 0, 0. The output we got after putting A, B and C values on logical expression is 1. Similar result we achieved the truth table of problem-1(a).

But between 25 to 30 ns interval, we get output y is 1 for A, B and C are 1, 0 and 1 respectively. However, we achieved output Y is 0 for the same values in problem-1(a) truth table.

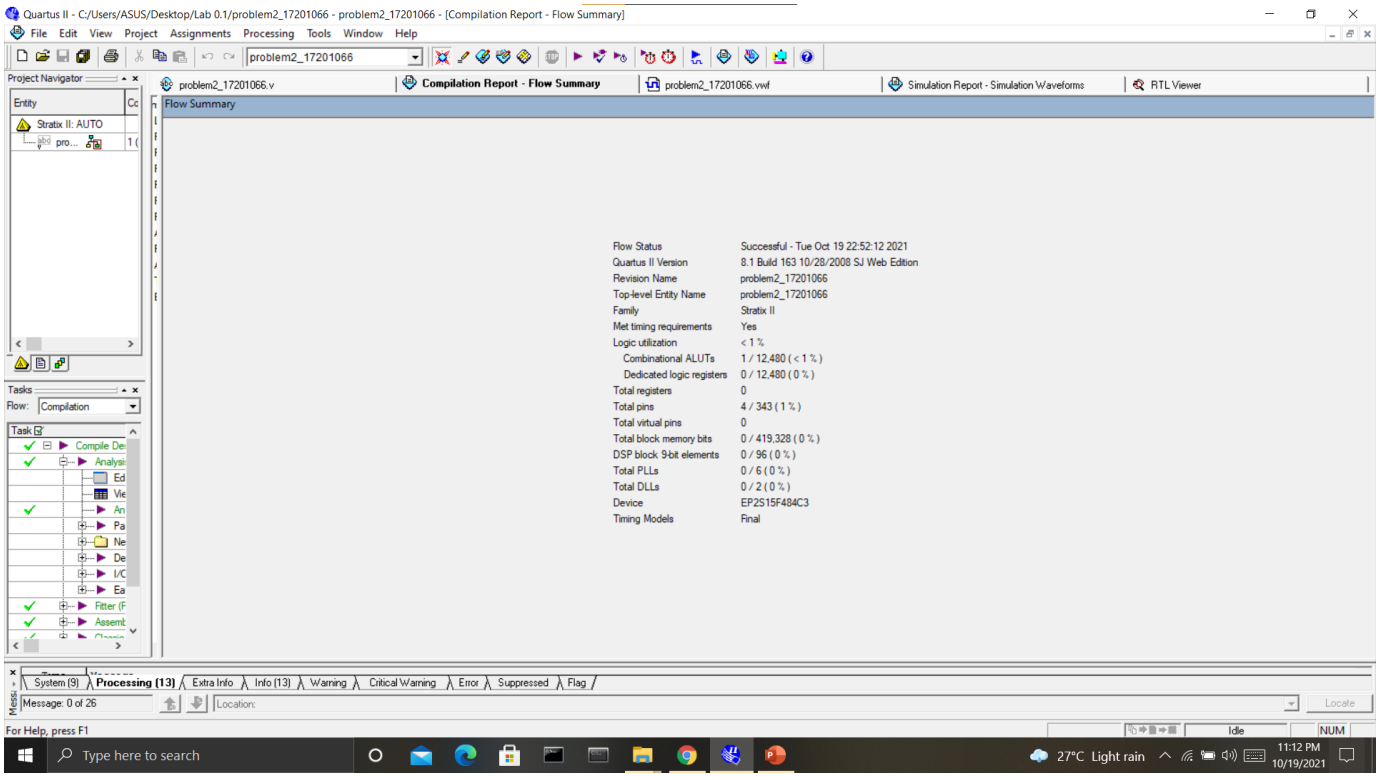
(d) NAND is a universal gate. Any logical gate can be replaced by NAND. If the given equation is modified so that the logic circuit is composed of only NAND gates, the new logic expression will be,

Y = (((A.A)' . (B.B)' . C)' . ((A.A)' . B . (C.C)')' . (A . (B.B)' . (C.C)')' . (A . B. C)')'
  = (A' . B' . C + A' . B . C' + A . B' . C' + A . B . C)
New equation has been applied to Quartus II.

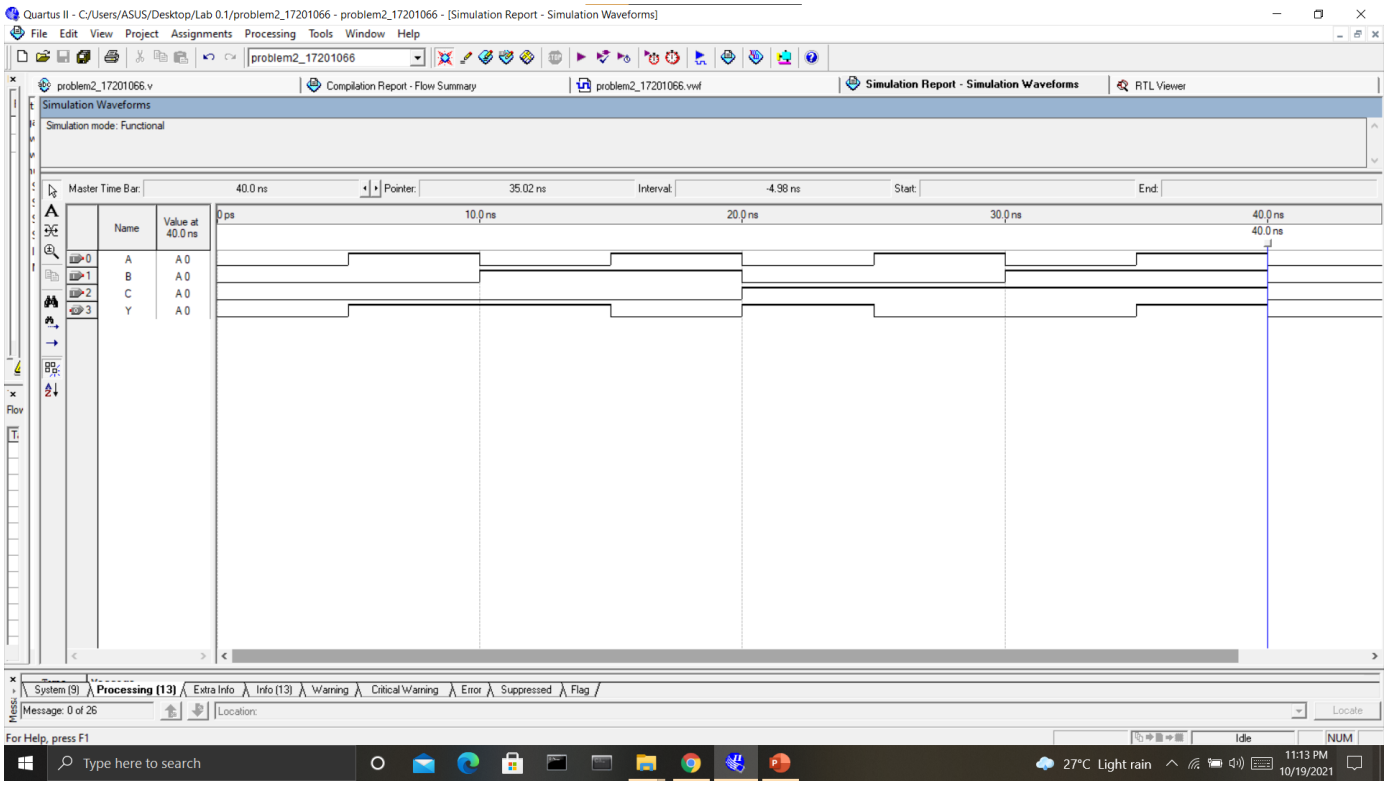
Code:



Summary:



Simulation Waveform:



Truth Table:

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

This truth table is equivalent to the truth table that has been computed at Problem-1 (a)

Circuit Diagram: