CSE460L: Assignment 01

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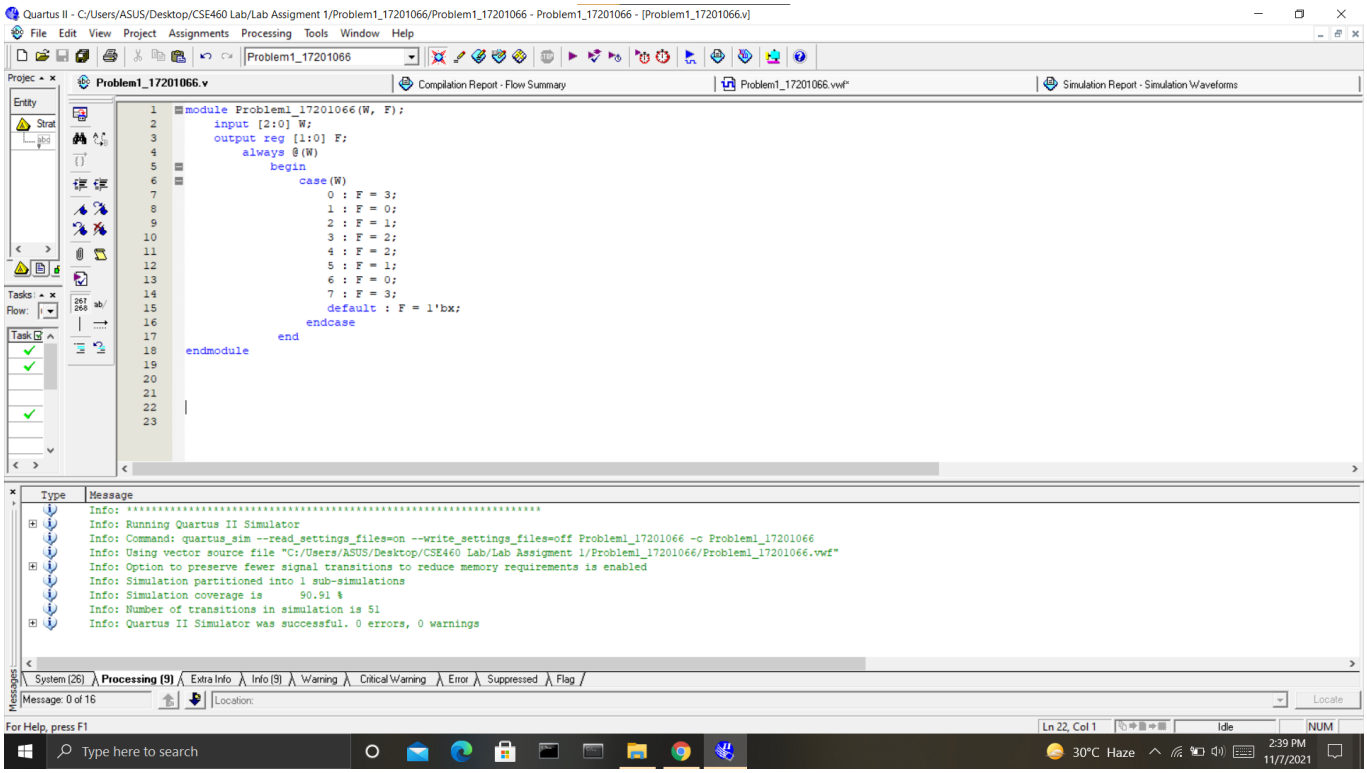
ID: 17201066

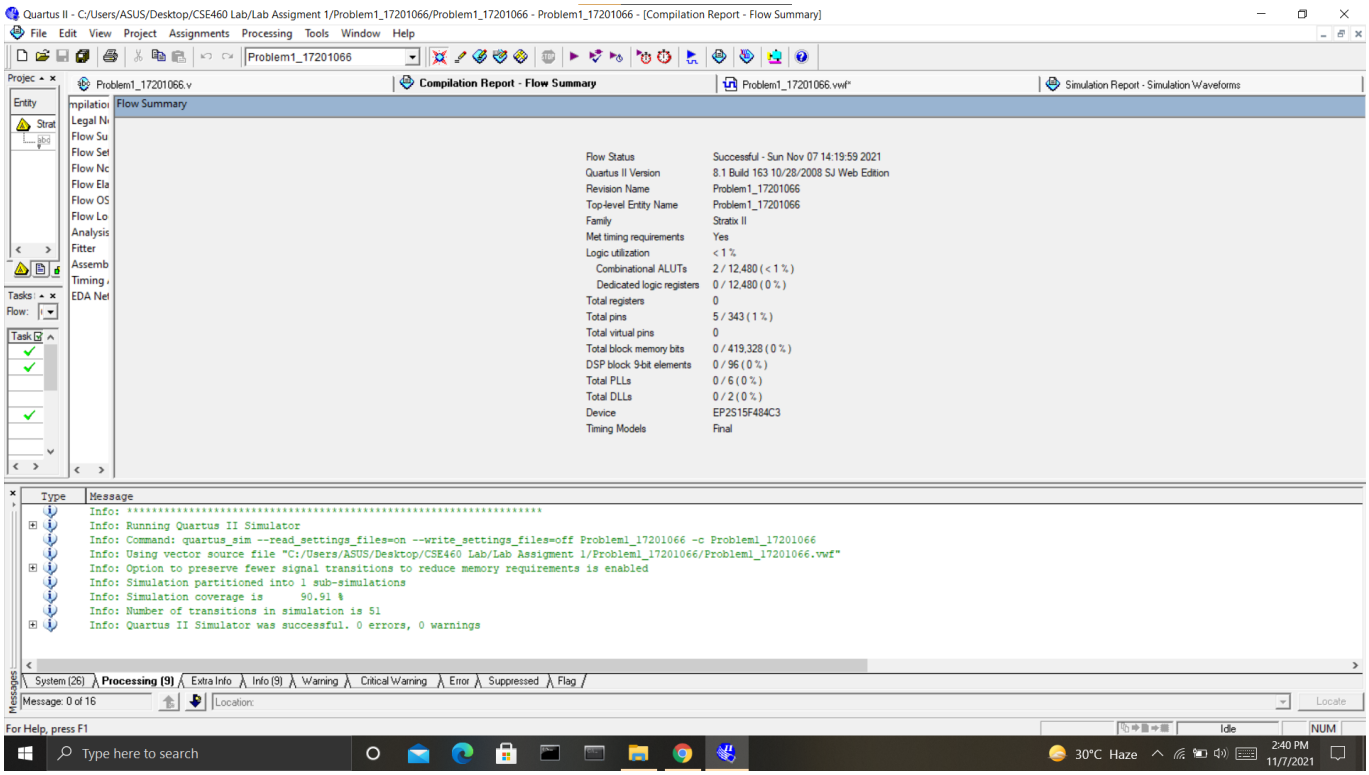
Section: 02

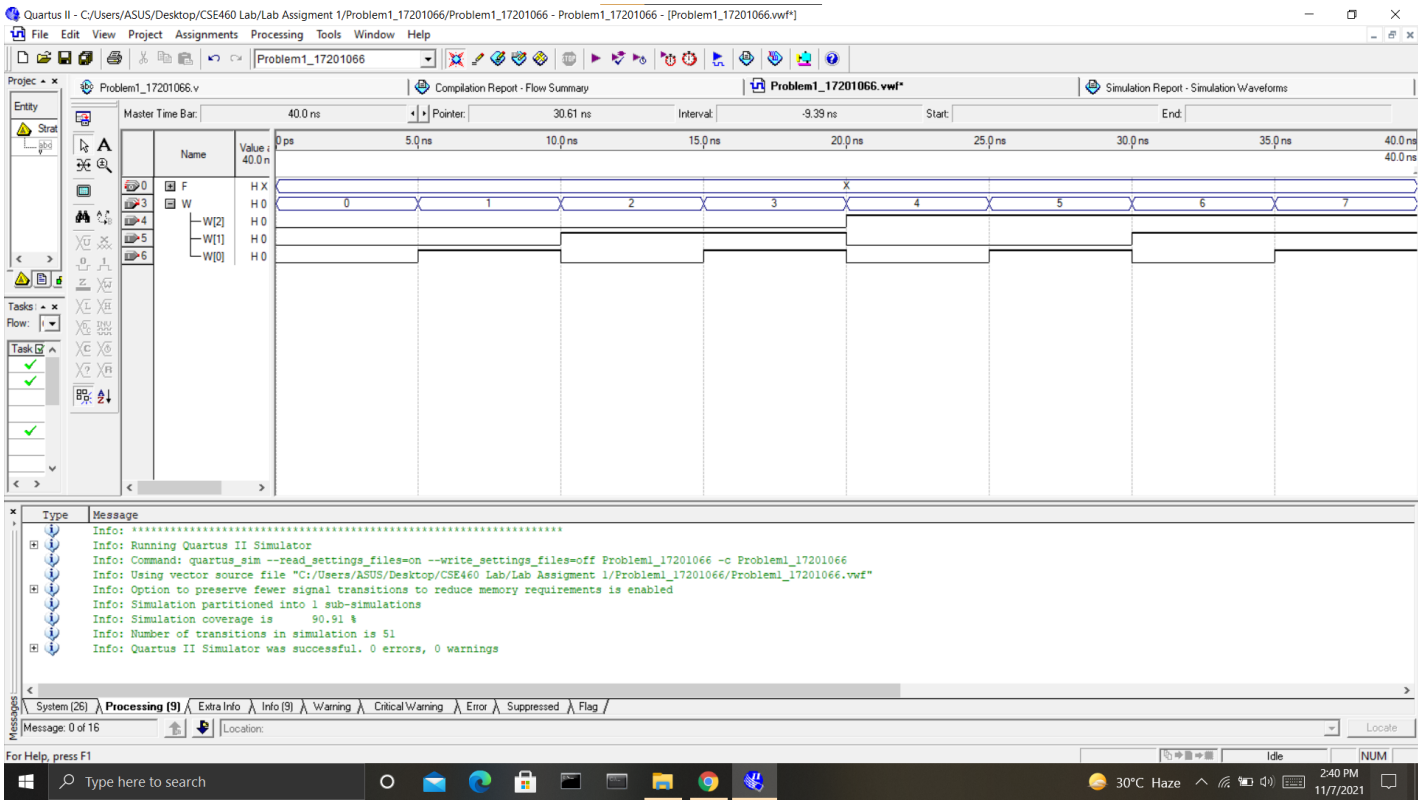
Couse: CSE460

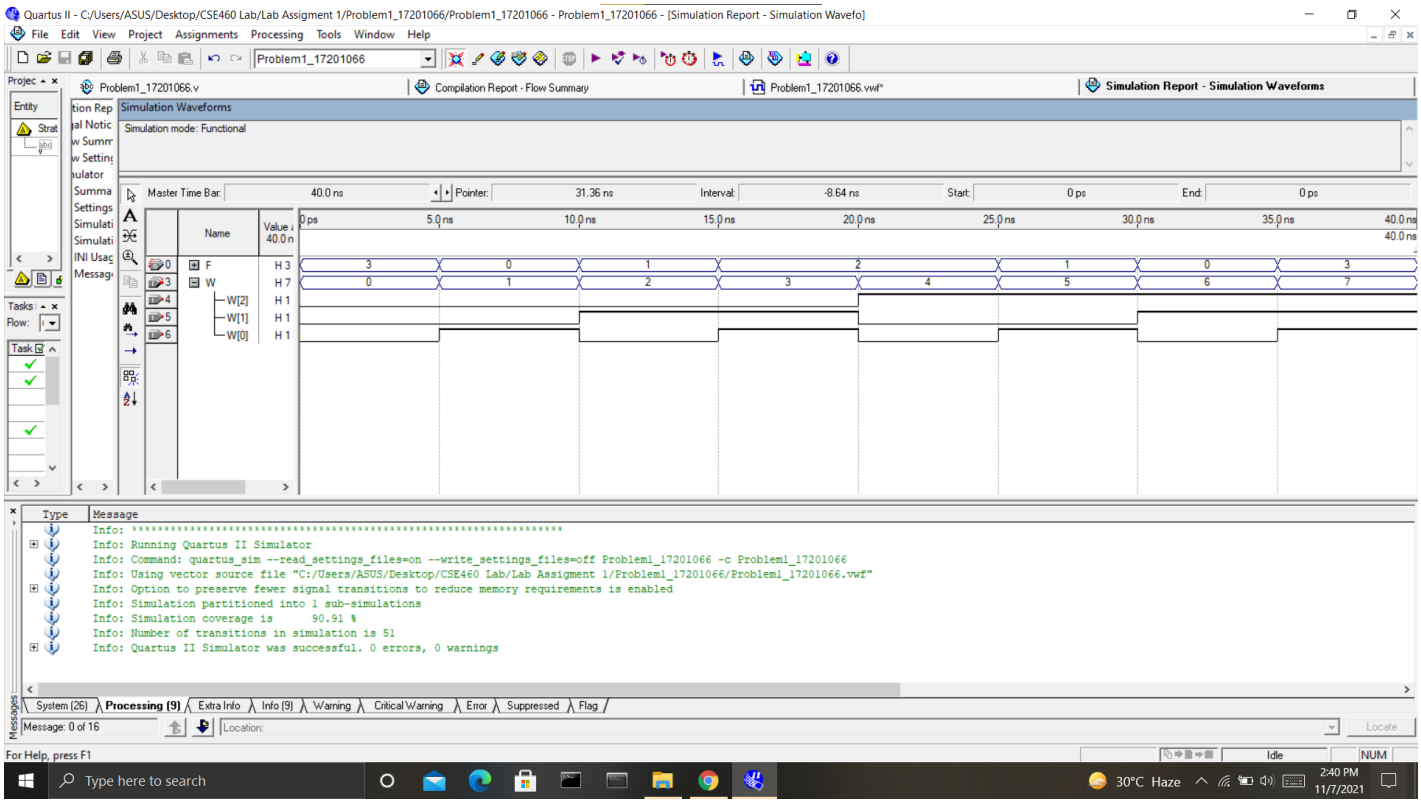
Problem 1:

In this problem, we have to find the position of the unique bit from 3 bits input strings.






Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assigment 1/Problem1_17201066/Problem1_17201066 - Problem1_17201066 - [Problem1_17201066.vwf*]
File Edit View Project Assignments Processing Tools Window Help
Problem1_17201066
Problem1_17201066.v
Compilation Report - Flow Summary
Problem1_17201066.vwf*
Simulation Report - Simulation Waveforms
Master Time Bar: 40.0 ns
Pointer: 30.61 ns
Interval: -9.39 ns
Start:
End:
Name
F
W
W[2]
W[1]
W[0]
0ps 5.0 ns 10.0 ns 15.0 ns 20.0 ns 25.0 ns 30.0 ns 35.0 ns 40.0 ns
Type Message
Info: Running Quartus II Simulator
Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off Problem1_17201066 -c Problem1_17201066
Info: Using vector source file "C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assigment 1/Problem1_17201066/Problem1_17201066.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 90.91 %
Info: Number of transitions in simulation is 51
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
System (26) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
For Help, press F1
Idle
NUM
Type here to search
30°C Haze
2:40 PM
11/7/2021


Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assigment 1/Problem1_17201066/Problem1_17201066 - Problem1_17201066 - [Simulation Report - Simulation Wavefo]
File Edit View Project Assignments Processing Tools Window Help
Problem1_17201066
Problem1_17201066.v
Compilation Report - Flow Summary
Problem1_17201066.vwf*
Simulation Report - Simulation Waveforms
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 40.0 ns
Pointer: 31.36 ns
Interval: -8.64 ns
Start: 0 ps
End: 0 ps
Name
F
W
W[2]
W[1]
W[0]
0ps 5.0 ns 10.0 ns 15.0 ns 20.0 ns 25.0 ns 30.0 ns 35.0 ns 40.0 ns
Type Message
Info: Running Quartus II Simulator
Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off Problem1_17201066 -c Problem1_17201066
Info: Using vector source file "C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assigment 1/Problem1_17201066/Problem1_17201066.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
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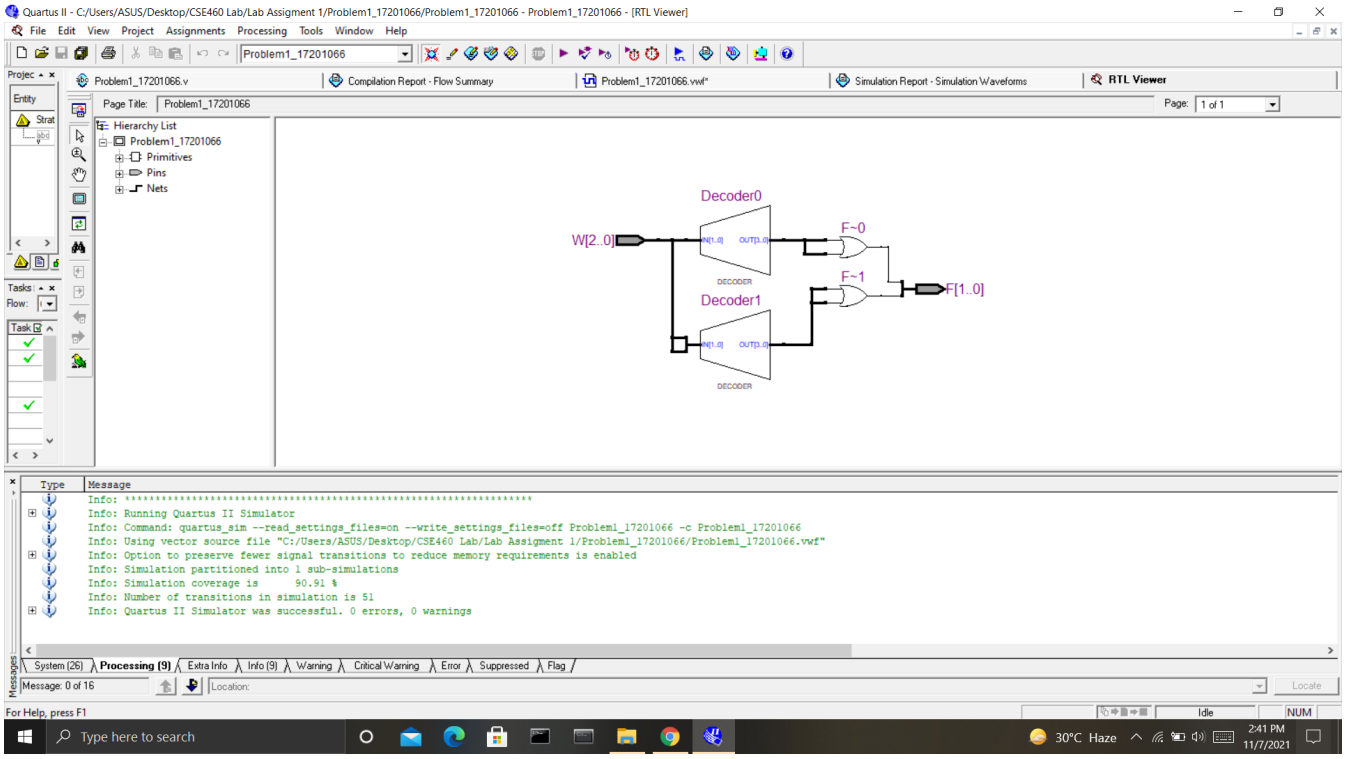
System (26) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
For Help, press F1
Idle
NUM
Type here to search
30°C Haze
2:40 PM
11/7/2021

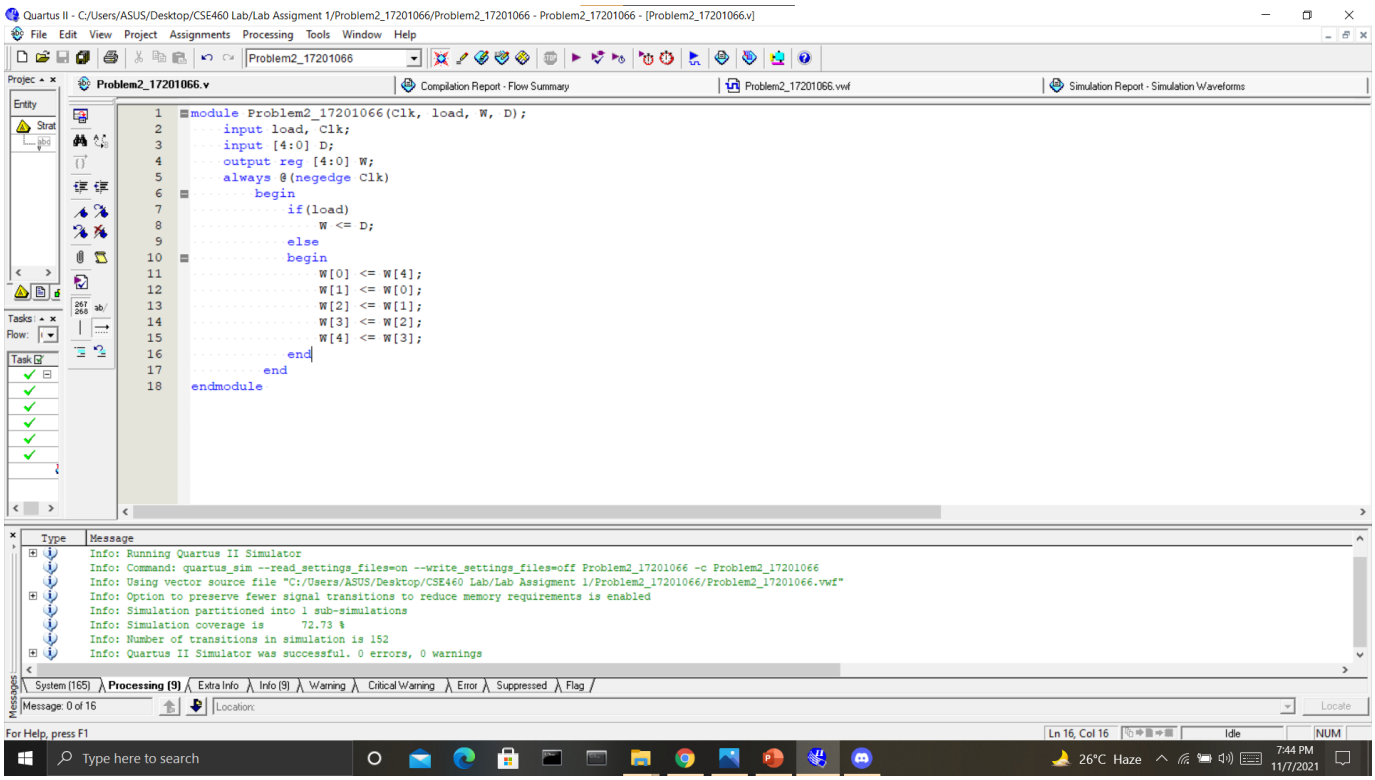


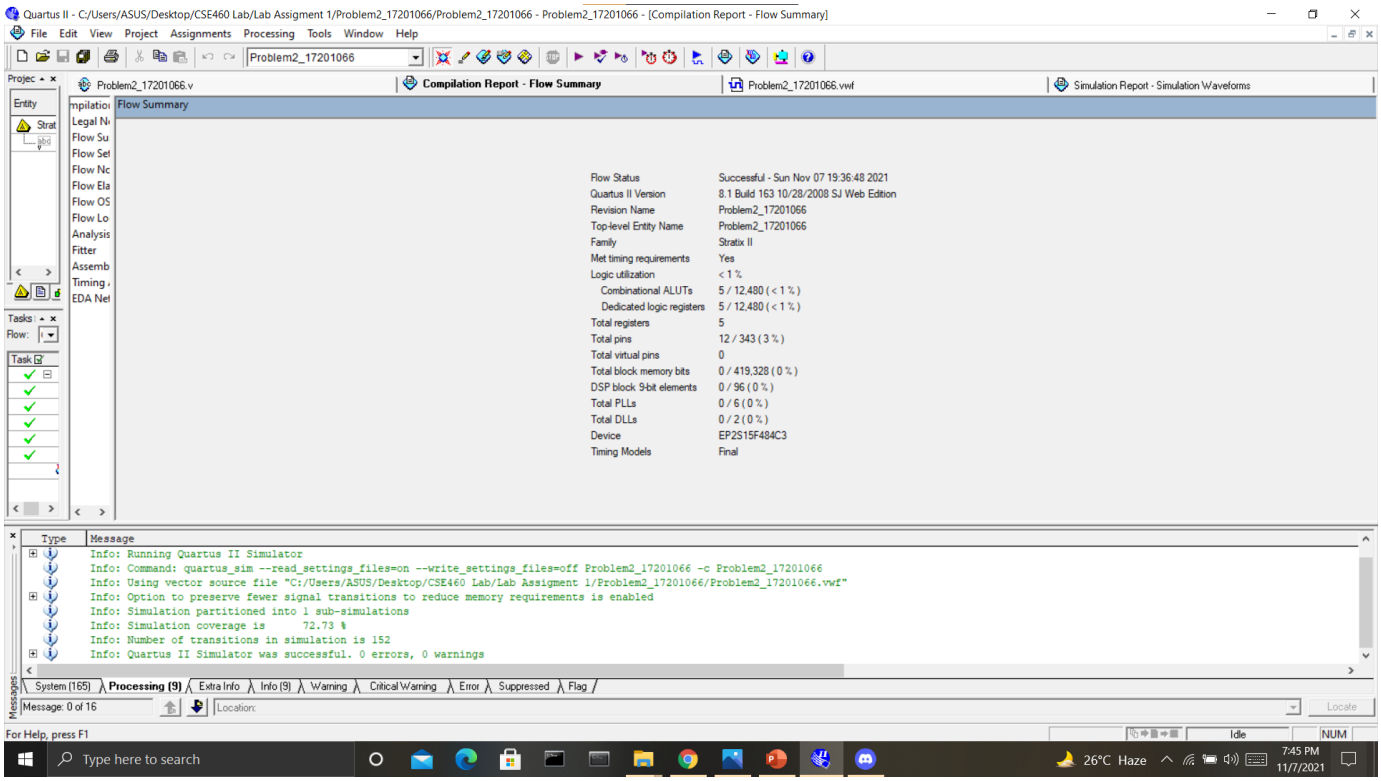
In Quartus II we initialized variable W first. W is a 3 bits variable that takes clock value as input. In the programming section, the program finds the unique bits position for different cases. Register F, store the value of position for different cases. For example, If 011 is the input of W. Here, the unique bit is 0 at position 2 and other two bits contain two 1's. So, the value of F will be 2. The program will also assign the value of F as 3 if all the values in the bits are the same. The table contains the result from the waveform which is generated from our program.

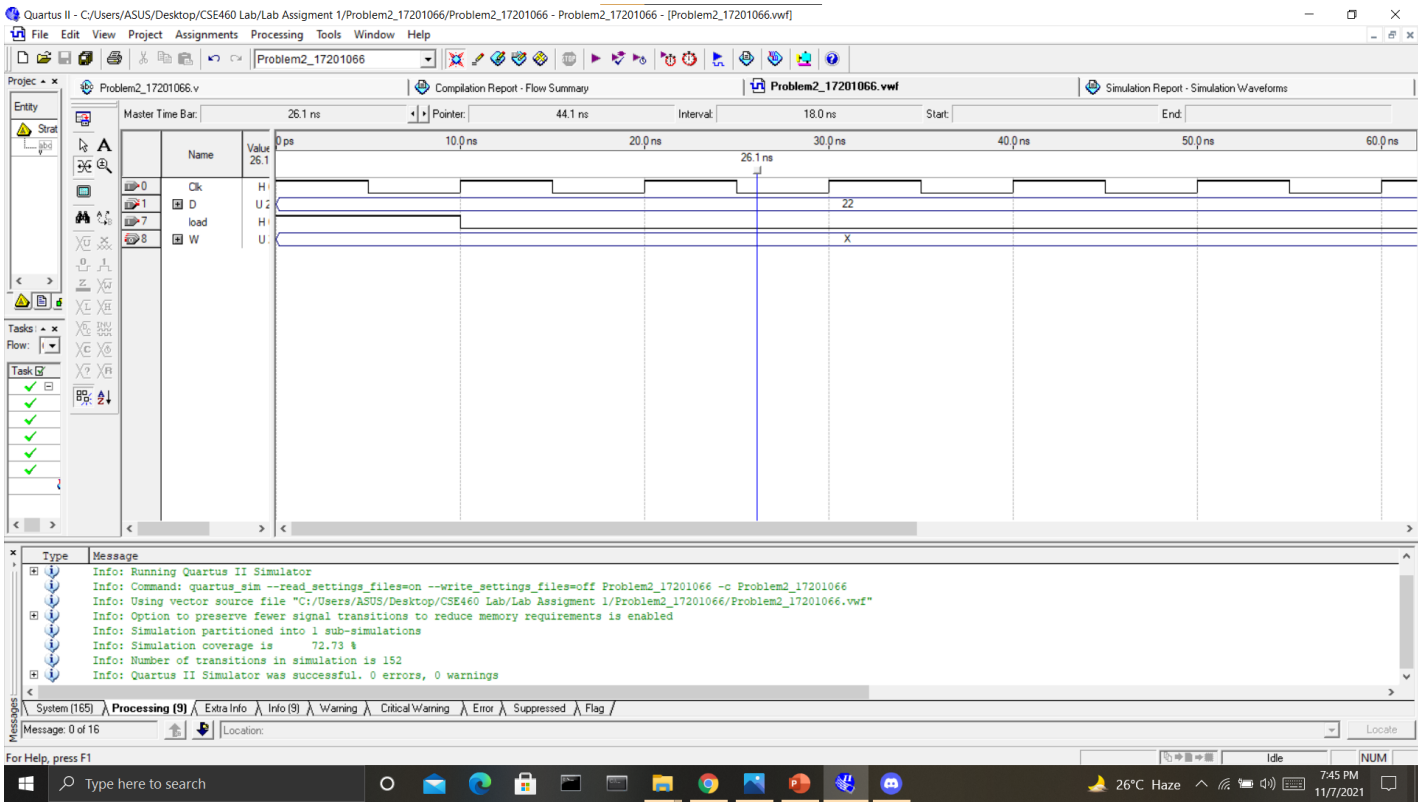
W[2]	W[1]	W[0]	Position of the unique bit
0	0	0	3
0	0	1	0
0	1	0	1
0	1	1	2
1	0	0	2
1	0	1	1
1	1	0	0
1	1	1	3

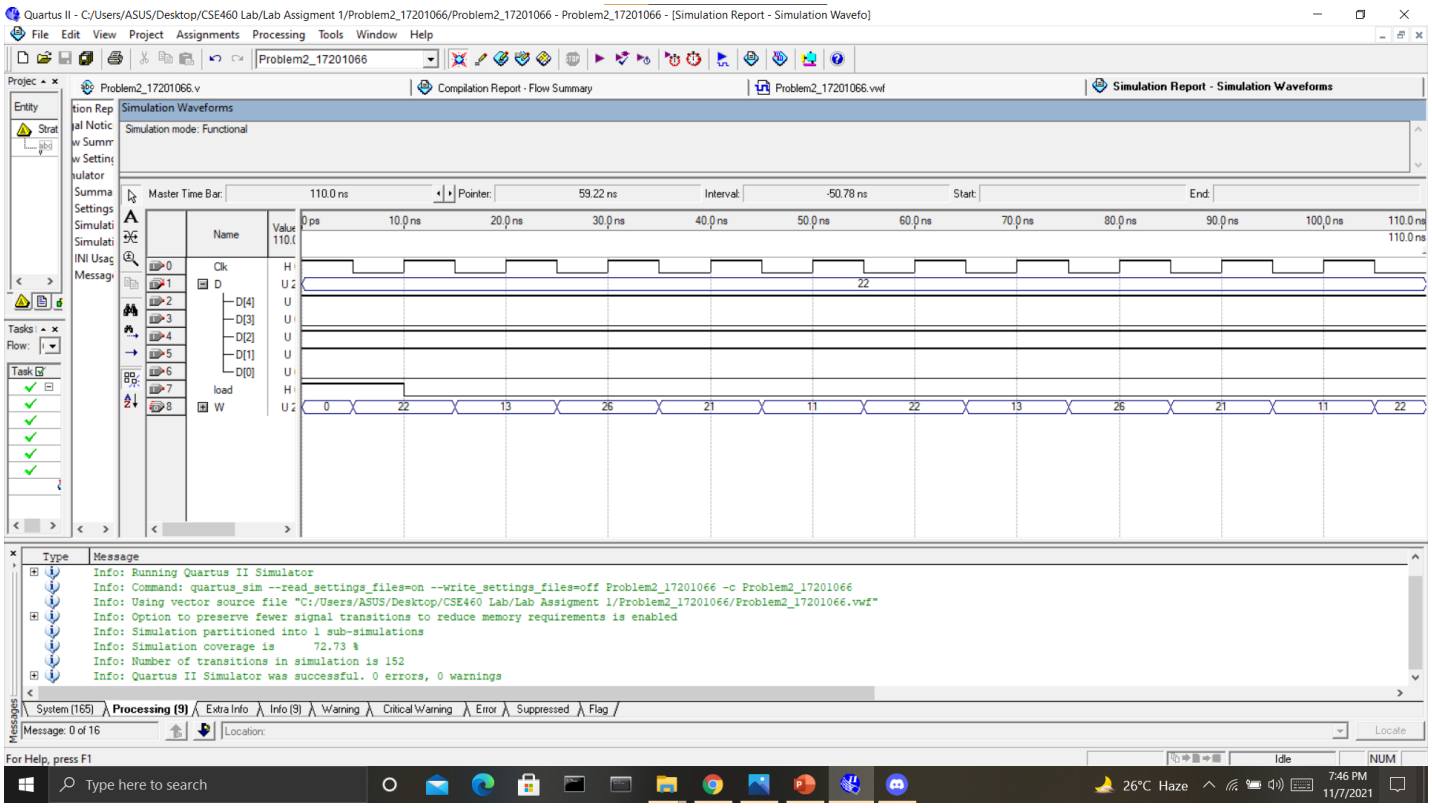
Problem 2:

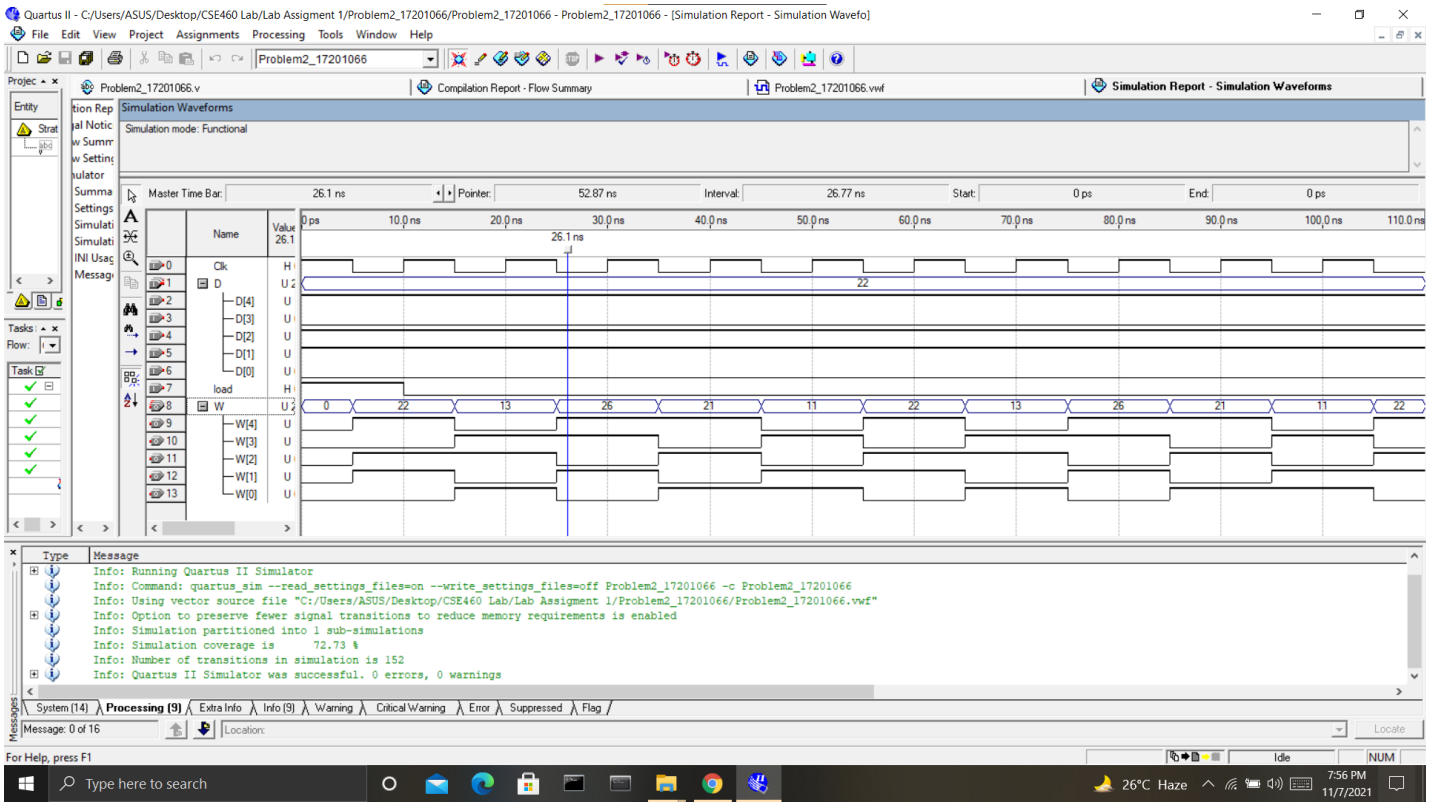
In this problem we have to design a 5-bit end around the left shift register that operates at the negative edge of a clock in Verilog with external load functionality.






Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assigment 1/Problem2_17201066/Problem2_17201066 - Problem2_17201066 - [Problem2_17201066.vwf]
File Edit View Project Assignments Processing Tools Window Help
Problem2_17201066
Problem2_17201066.v
Compilation Report - Flow Summary
Problem2_17201066.vwf
Simulation Report - Simulation Waveforms
Master Time Bar: 26.1 ns
Pointer: 44.1 ns
Interval: 18.0 ns
Start:
End:
Name
Value 26.1
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
26.1 ns
Clk
D
load
W
22
X
Type
Message
Info: Running Quartus II Simulator
Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off Problem2_17201066 -c Problem2_17201066
Info: Using vector source file "C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assigment 1/Problem2_17201066/Problem2_17201066.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 72.73 %
Info: Number of transitions in simulation is 152
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
System (165) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
For Help, press F1
Idle
NUM
Type here to search
26°C Haze
7:45 PM
11/7/2021


Quartus II - C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assigment 1/Problem2_17201066/Problem2_17201066 - Problem2_17201066 - [Simulation Report - Simulation Wavefo]
File Edit View Project Assignments Processing Tools Window Help
Problem2_17201066
Problem2_17201066.v
Compilation Report - Flow Summary
Problem2_17201066.vwf
Simulation Report - Simulation Waveforms
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 110.0 ns
Pointer: 59.22 ns
Interval: -50.78 ns
Start:
End:
Name
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
100.0 ns
110.0 ns
Clk
D
D[4]
D[3]
D[2]
D[1]
D[0]
load
W
22
0 22 13 26 21 11 22 13 26 21 11 22
Type
Message
Info: Running Quartus II Simulator
Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off Problem2_17201066 -c Problem2_17201066
Info: Using vector source file "C:/Users/ASUS/Desktop/CSE460 Lab/Lab Assigment 1/Problem2_17201066/Problem2_17201066.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 72.73 %
Info: Number of transitions in simulation is 152
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
System (165) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
For Help, press F1
Idle
NUM
Type here to search
26°C Haze
7:46 PM
11/7/2021



Since it has a load function, the left shifting will start occurring only when the load value has been set to logical High. It operates on a negative edge. So, the left shifting will occur when the clock value is 0 and the output value will remain the same when clock value is 1. The left function runs by some non-blocking assignments.

Our program takes clk, load and D as inputs. We assign a clock value in the CLK variable. Clock wave starts from a logical high to avoid garbage values. Between 0 - 10ns we set the load value to 1. At 5 - 10ns the clock value is 0 and load value is 1. This instance meets the requirement of the procedural statement and its first condition. So, the value of D at 5 - 10ns, 22 (10110) gets copied to 5 bits W. Between 10 to 15 ns the value of W does not change as the program operates on the negative edge of the signal. At 15 to 20 ns the clock value becomes lower for the second time after insertion of load operation . As a result, a left shift occurs and 10110 (22) turns into 01011 (13). This is a repetitive process so between 55 - 60ns we again received our previously inserted D value, 22.

It takes a total of 10 clock cycles to get one repetition in this program.