CSE460L: Assignment 1 (Fall 2021)

Sections: 1, 2, 3, 4, 5, 6, 7, 8 & 9

Assignment 1 submission link:
https://docs.google.com/forms/d/e/1FAIpQLSdBeAsmOK4FBdDCAn0XgES7KuZ_JaYTqIb2T5JVVVUb7EE9BA/viewform?usp=sf_link

Assignment 1 deadline: **9 Nov, 2021, 4.59 PM (BDT)**

General guidelines

- Assignments are individual

- Each assignment will contain 3 to 4 problems

- **For each problem you will need to prepare 3 parts:**
  1. **Code:** attach a screenshot of your code from Quartus.
  2. **Output: attach *FULL SCREEN* screenshots** of
     - Compilation Report - Flow Summary (Compilation report of the .v file)
     - Simulation Report - Simulation Waveforms (Simulation report of the .vwf file)

  [**Tampered/edited/cropped screenshots will be considered as a violation of general guidelines and therefore will not be accepted**]

  3. **Discussion/Explanation:** explain the output waveforms of your simulation report as described in the **Expected Output** section within each problem statement.

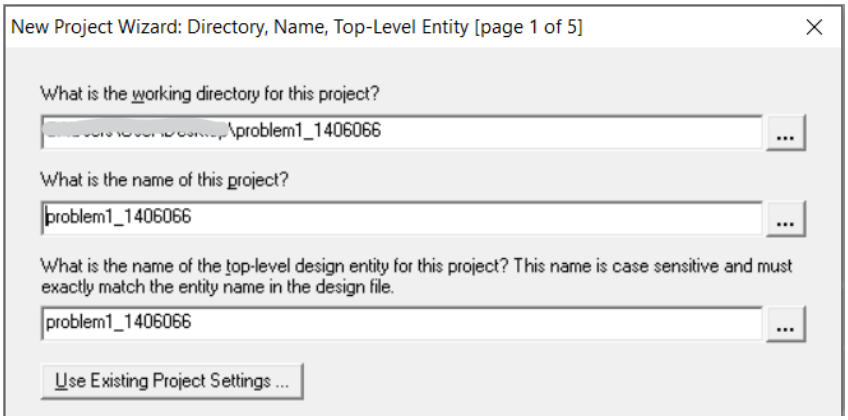
- Each problem will be of equal points. You will not be graded on the length/number of code/explanation/outputs; rather on the clarity, readability and precise explanations of your code/logic/outputs

- Points distribution for each problem is

  Code: **40%**
  Output: **20%**
  Discussion/Explanation of output: **40%**

- **You will need to create separate directories/project for each problem**

- **The name of your working directory for each problem of the assignment should be …\problem#_StudentID [# = 1/2/3/4..]**
  For example, for problem 1 the name of the directory should be problem1_1406066



- Consequently, the name of your main module in the Verilog file should be problem#_StudentID [# = 1/2/3/4..]
  Continuing from the previous example, the name of the module should be problem1_1406066

- Finally, **compile all the problems for a given assignment into a single pdf file**

- The **name of the pdf should be Section_StudentID_assignment1.pdf** (Example: 1_1406066_assignment1.pdf)

Problem for Assignment 1

1. Design a logic circuit in Verilog that will take one **3-bit** input **A**, check whether all of the input bits are **equal or not** and determine the **logic level (0/1)** of the unique bit. Find the possible input conditions and the expected outputs in the following table: **[15]**

Possible input condition	**Output**
All bits are equal	3
Unique bit at position 2	2
Unique bit at position 1	1
Unique bit at position 0	0

Expected Output:
Show all possible outputs in your timing diagram with appropriate inputs and briefly explain your results.

2. Design a **5-bit end around left shift register** that operates at the **negative edge** of a clock in Verilog with external **load** functionality. For example, the output of the shift register would be (for each **negedge** clock time t(i) to t(i+2) and so on): **[15]**

t(i)	t(i+1)	t(i+2)
10110	01101	11010

Expected Output:
Perform the simulation for enough time to get at least **two** repetitions of the initial input after the external **load**. Determine the total number of clock cycles required to get one repetition of the input from the timing diagram and briefly explain your reasoning for that.