CSE460L: Assignment 03

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Section: 02

Couse: CSE460

Problem 1:

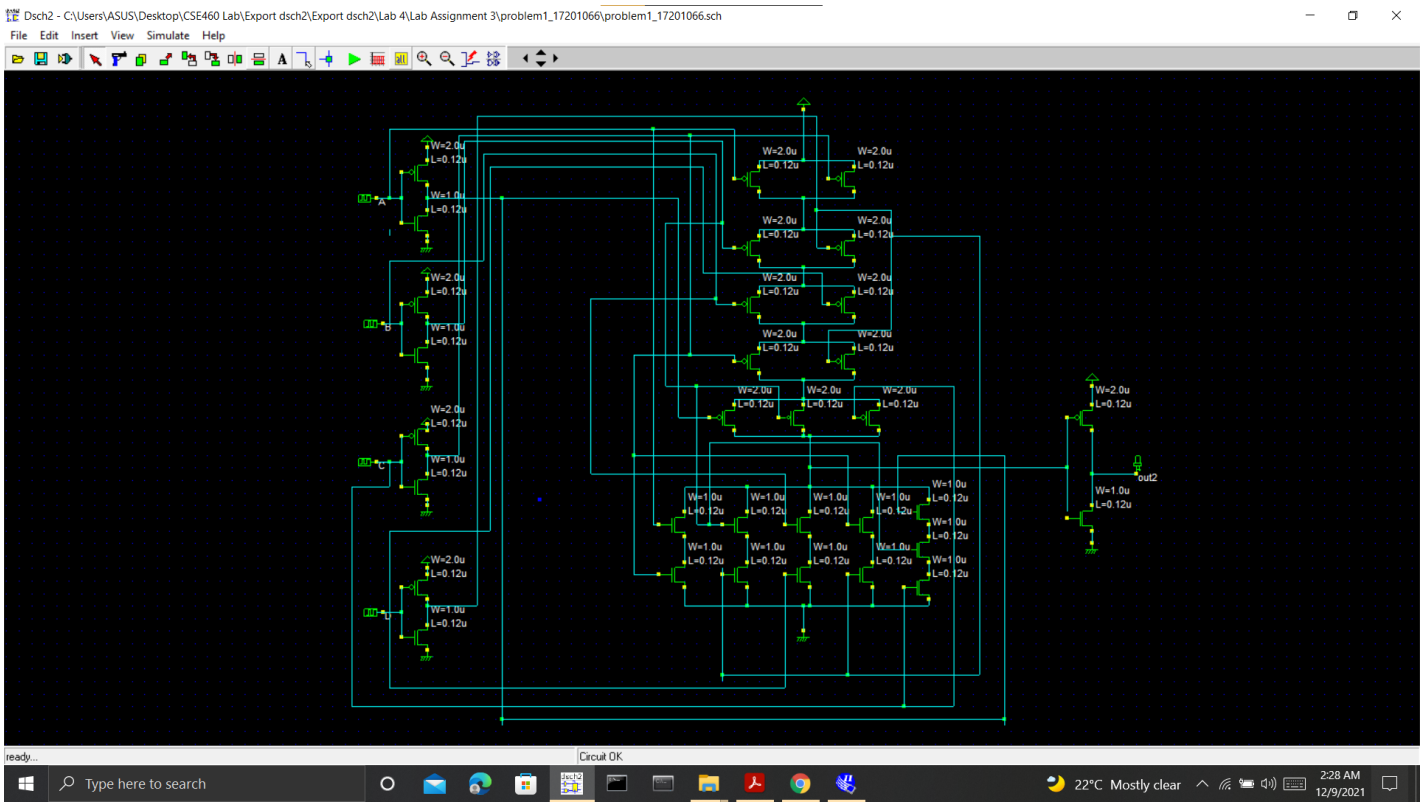
Kmap:

CD \ AB	00	01	11	10
00	1	0	1	1
01	1	d	d	0
11	d	d	1	0
10	1	1	0	1

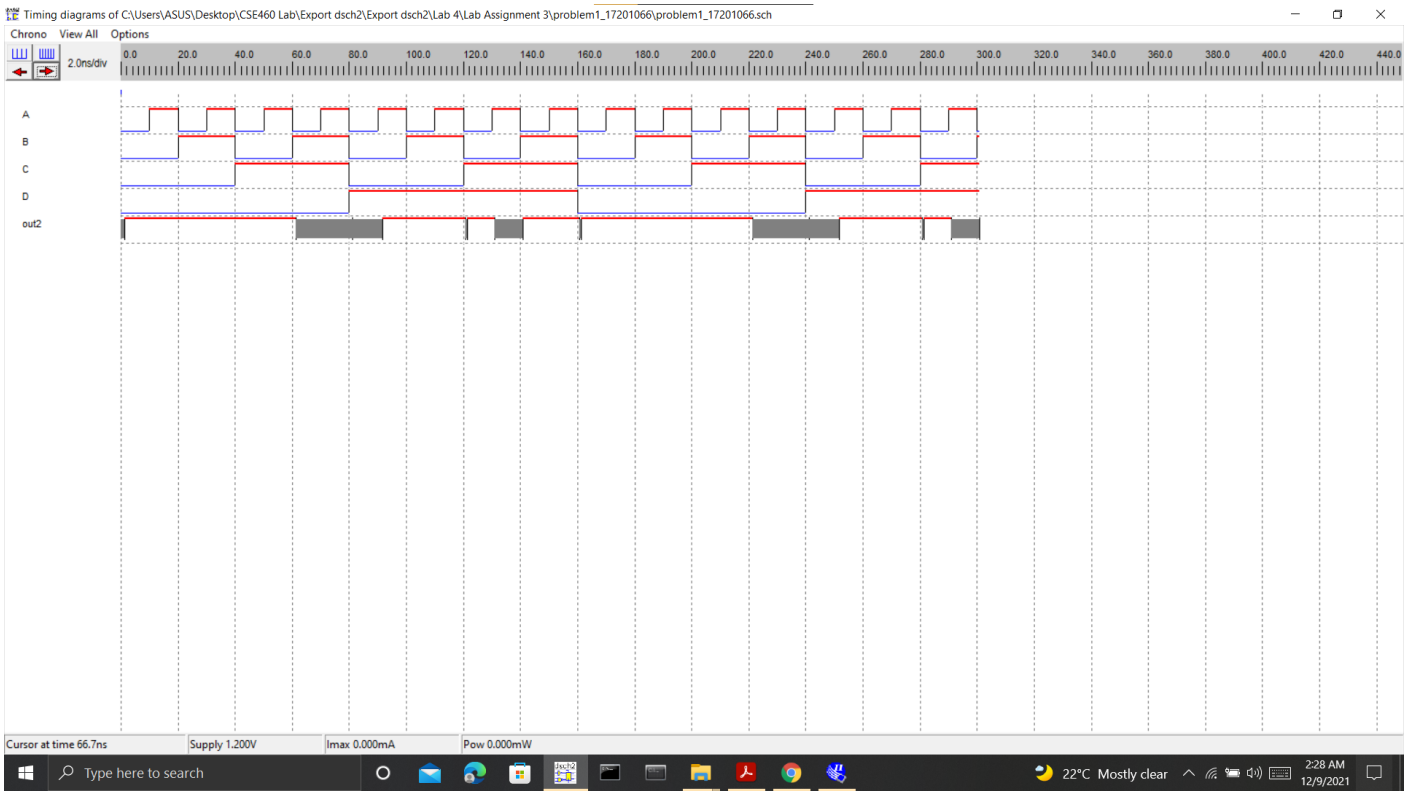
Equation derived from the Kmap is,

F = AC' + B'D' + BD + C'D' + A'B'C

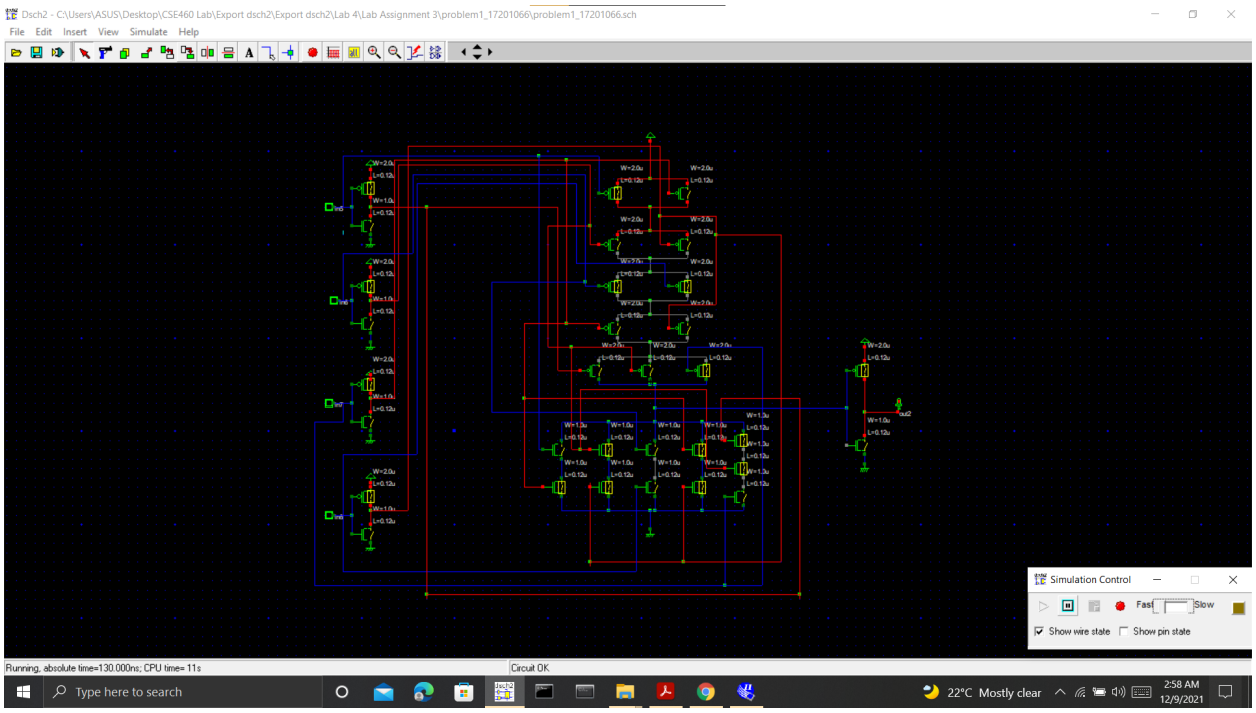
CMOS circuit design in DSCH2:



Time Diagram:



At the beginning from 0 to 10ns the clock values are A = 0, B = 0, C = 0, D = 0. Between this time interval the output value is 1 or High.

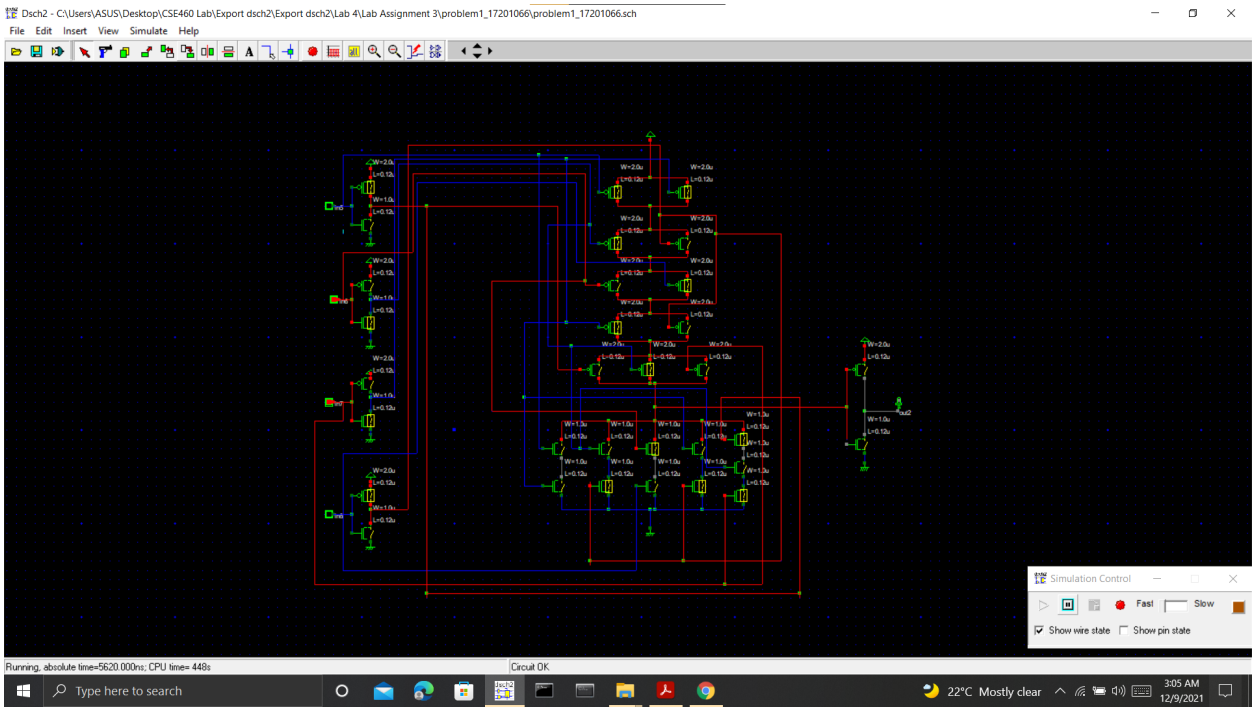


As we know, when the input is low the nmos will be disconnected and pmos will be connected. So, the vdd flows to the output and ground becomes disconnected at cmos. By following these properties of cmos the ground value from the circuit moves to the inverter. When the inverter connected to the output receives lower value, the pmos gets opened and vdd flows to the output. That's how for all lower clock values the output is High.
If we put the clock values on above equation,

F = AC' + B'D' + BD + C'D' + A'B'C
= 0.1 + 1.1 + 0.0 + 1.1 + 1.1.0
= 0 + 1 + 0 + 1 + 0
= 1

Theoretically, it is also High value

Between 60 to 70 ns intervals, the clock values A = 0, B = 1, C = 1, D = 0. At this time the time diagram of the circuit gives Low value.



Here, the circuit from the equation gives a higher value. The inverter, inverts the value and makes it low because of higher input the nmos get connected and it sends ground value to the output.

F = AC' + B'D' + BD + C'D' + A'B'C
= 0.0 + 0.1 + 1.0 + 0.1 + 1.0.1
= 0 + 0 + 0 + 0 + 0
= 0

Here, again the theoretical value for those certain inputs in Low.

Problem 2:

Given logical expression:

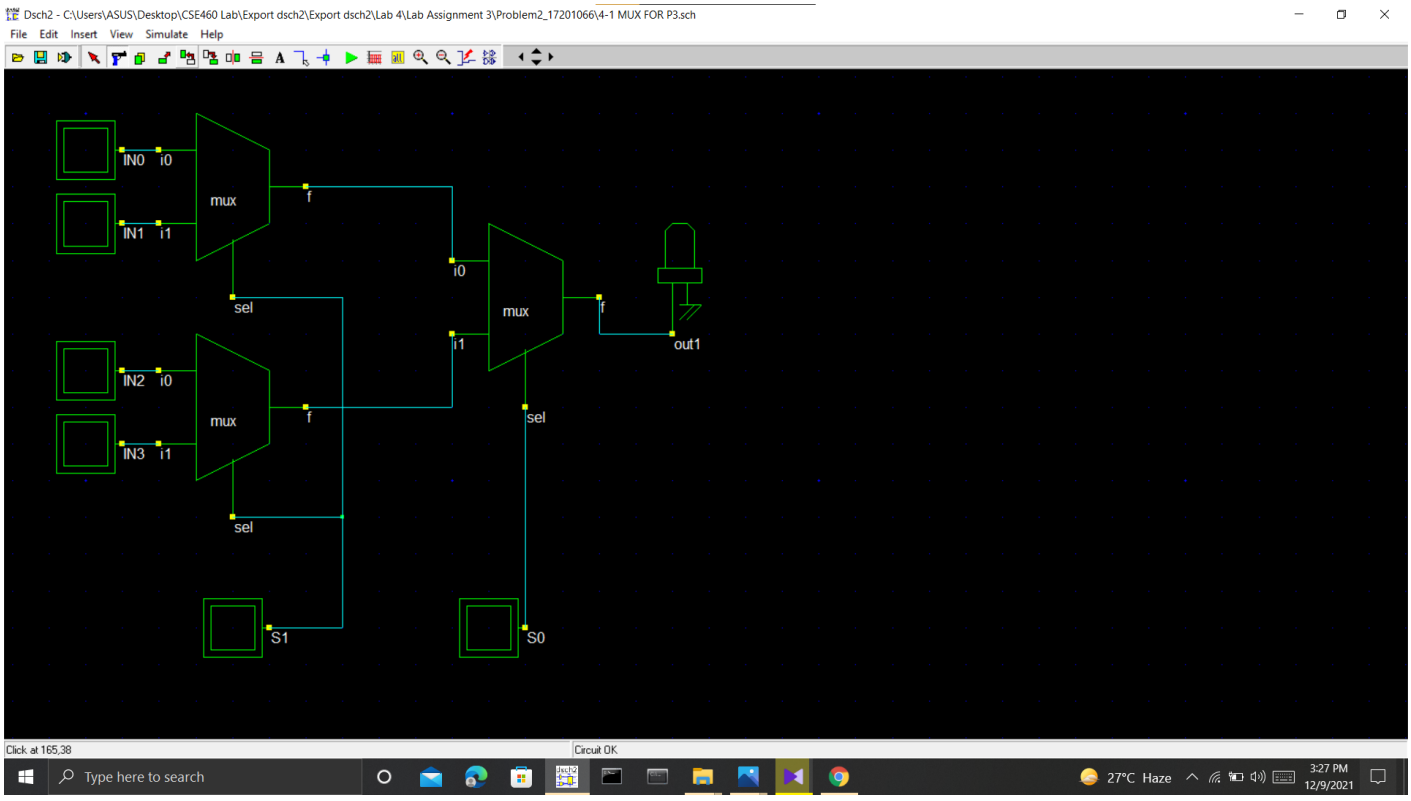
$f(A,B,C,D,E) = \sum(0,4,5,8,9,12,15,21,22,29,30)$; don't care 7

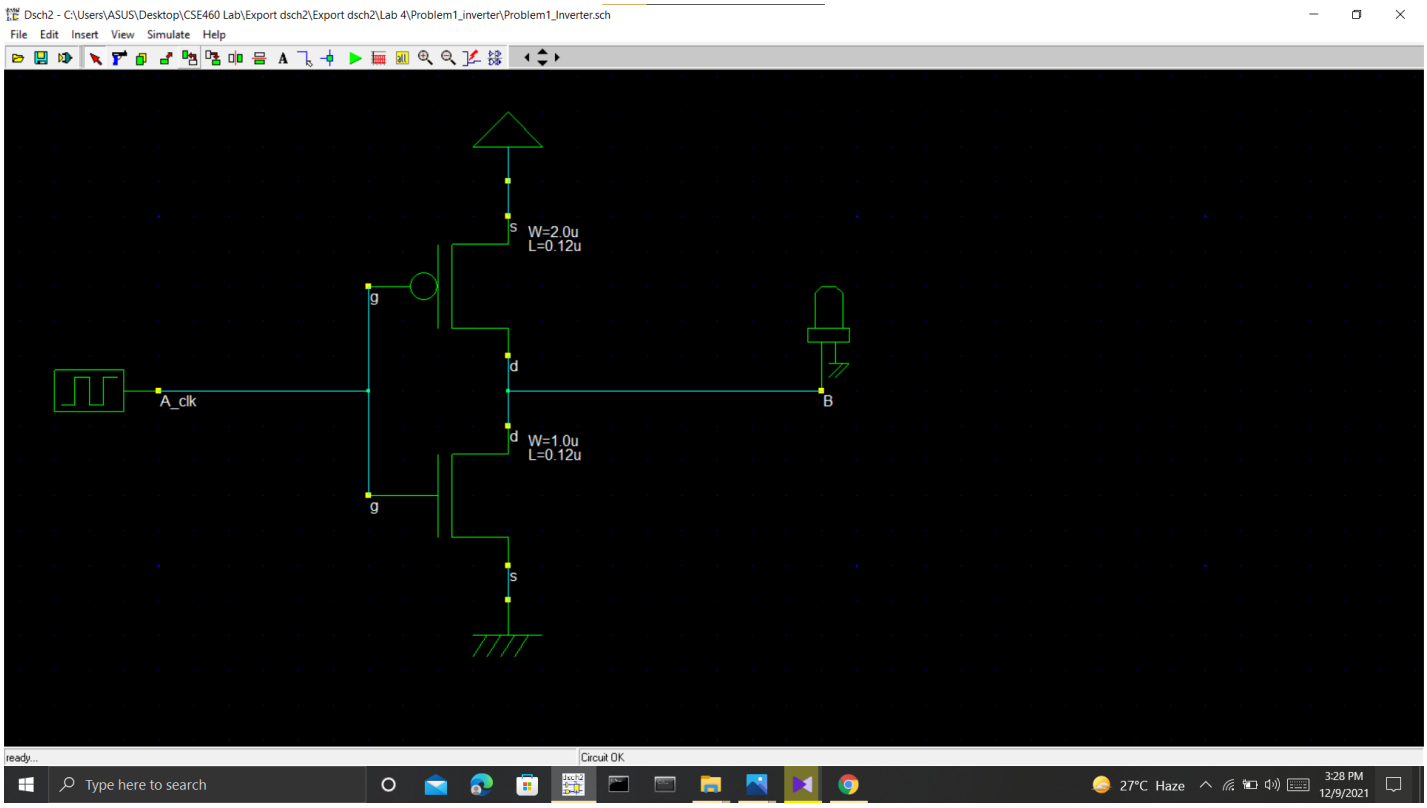
DECIMAL	A	B	C	D	E
0	0	0	0	0	0
4	0	0	1	0	0
5	0	0	1	0	1
8	0	1	0	0	0
9	0	1	0	0	1
12	0	1	1	0	0
15	0	1	1	1	1
21	1	0	1	0	1
22	1	0	1	1	0
29	1	1	1	0	1
1	1	1	1	1	0

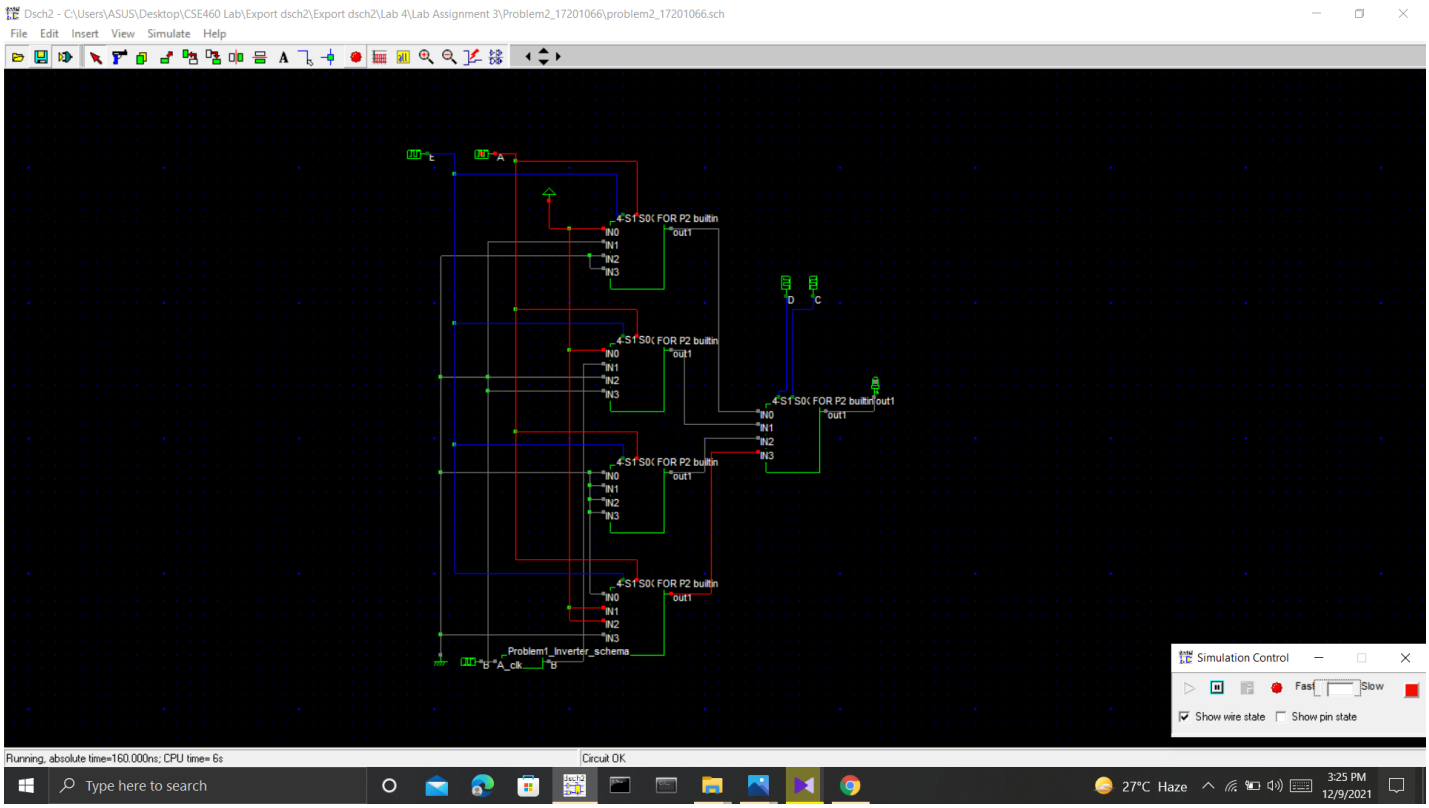
Assumed B as one of the inputs,

Input PIN	A	C	D	E	~B	B	PIN VALUE	Selectors
I0	0	0	0	0	0	8	1	A’C’DE
I1	0	0	0	1	1	9	B	A’BC’DE / A’B’C’DE
I2	0	0	1	0	2	10	0	X
I3	0	0	1	1	3	11	0	X
I4	0	1	0	0	4	12	1	A’BCD’E’
I5	0	1	0	1	5	13	~B	A’B’CD’E
I6	0	1	1	0	6	14	0	X
I7	0	1	1	1	7	15	B / 1	A’BCDE / A’B’CDE
I8	1	0	0	0	16	24	0	X
I9	1	0	0	1	17	25	0	X
I10	1	0	1	0	18	26	0	X
I11	1	0	1	1	19	27	0	X
I12	1	1	0	0	20	28	0	X
I13	1	1	0	1	21	29	1	ABCD’E
I14	1	1	1	0	22	30	1	ABCDE’
I15	1	1	1	1	23	31	0	X

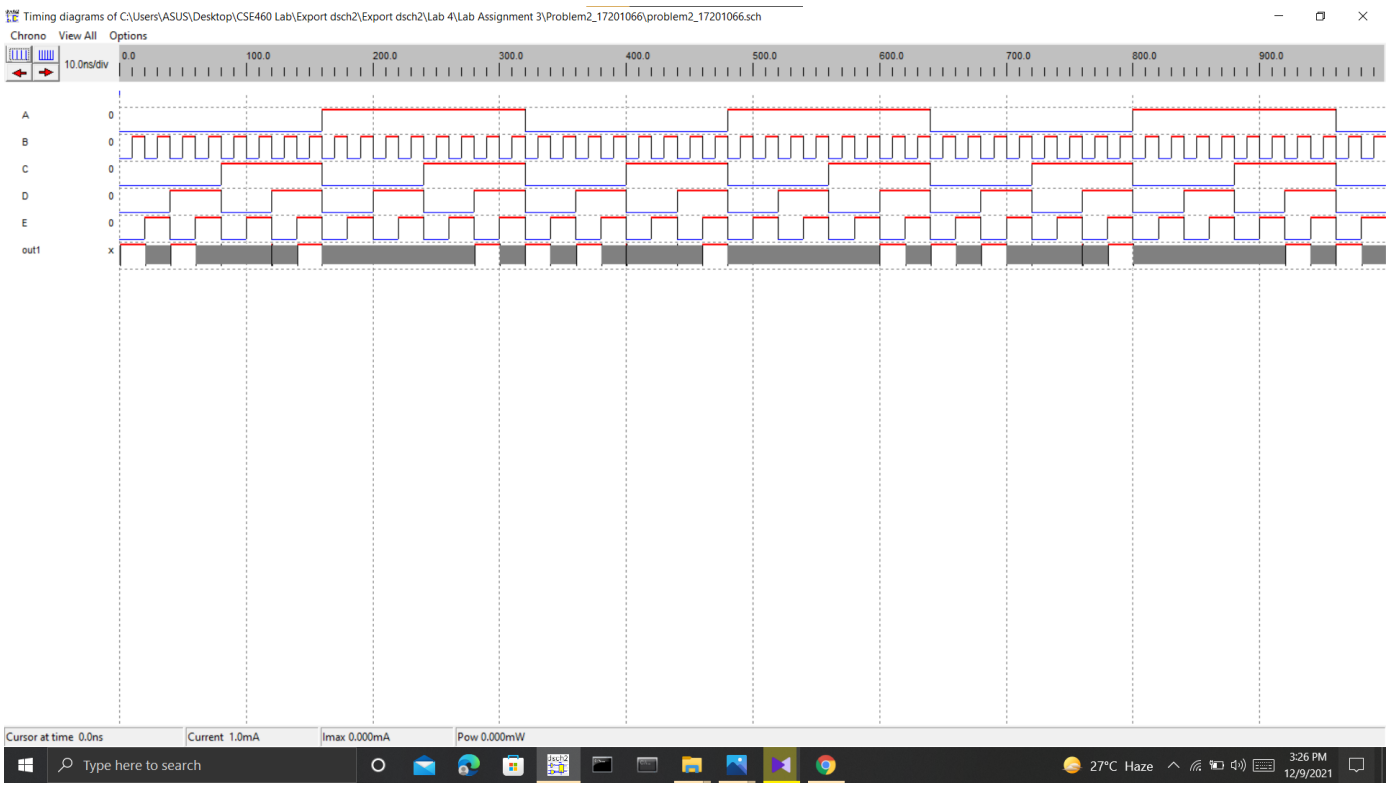
Circuit Design in DSCH2:







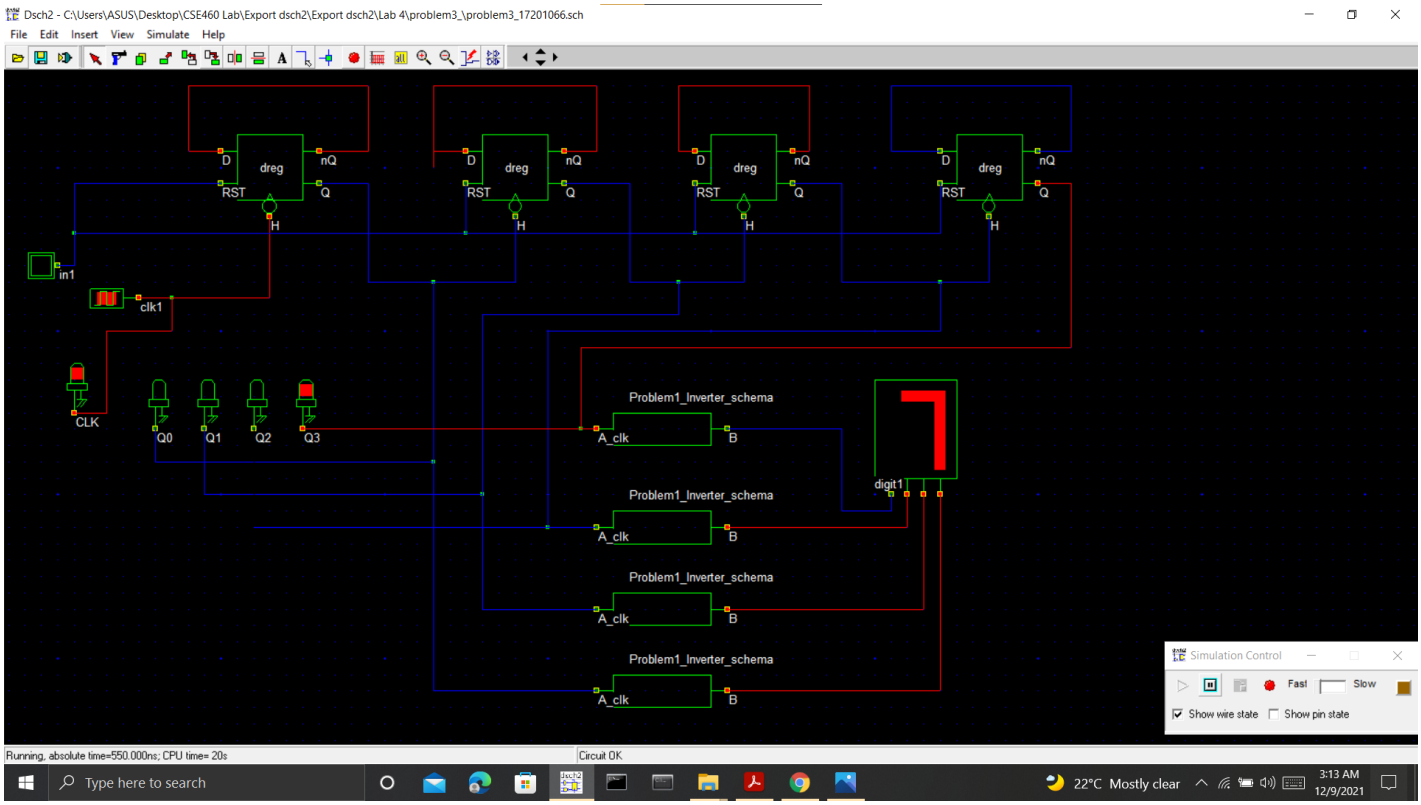
Time Diagram:



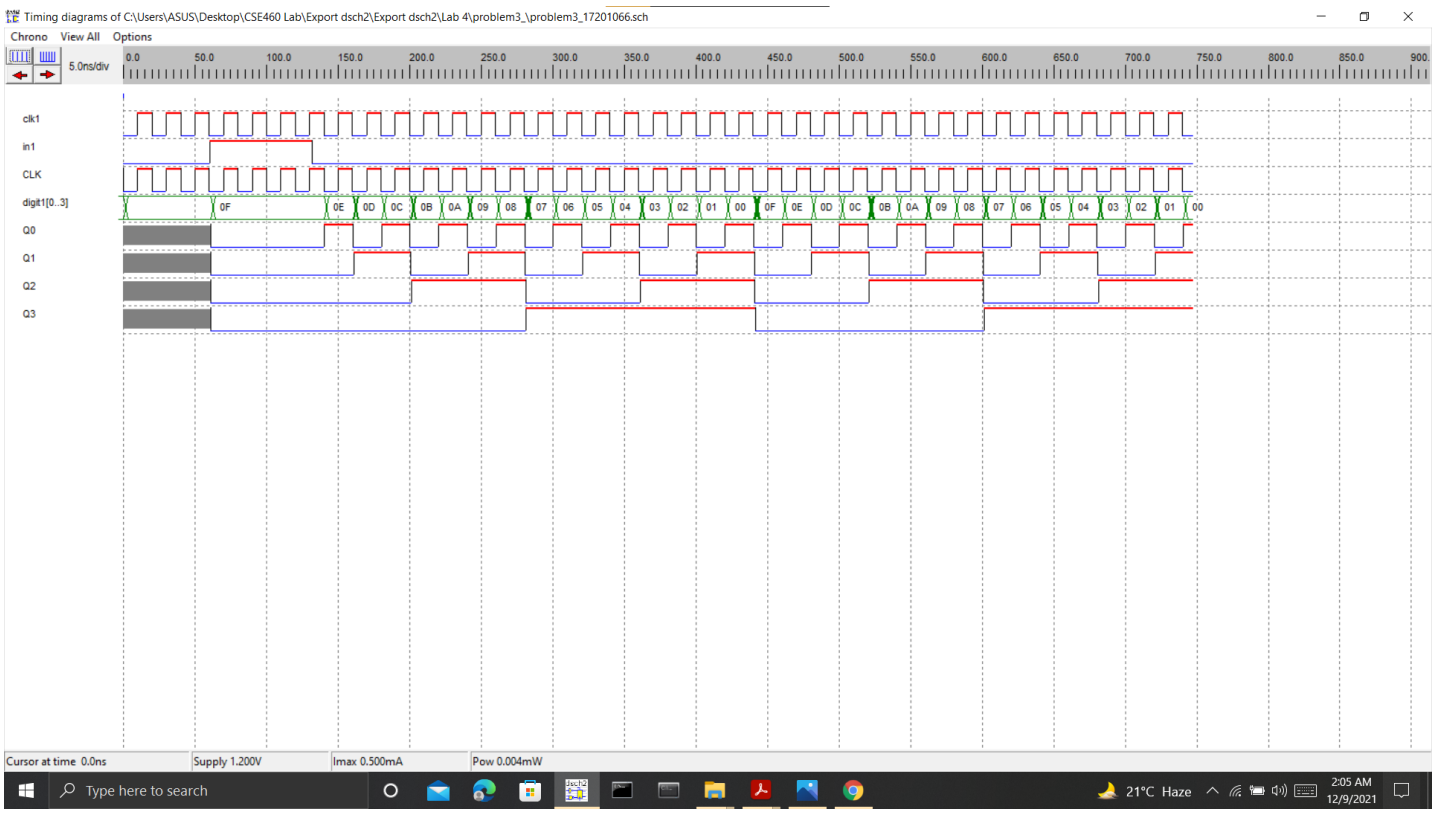
DECIMAL	A	B	C	D	E	Output
0	0	0	0	0	0	1
4	0	0	1	0	0	1
5	0	0	1	0	1	1
8	0	1	0	0	0	1
9	0	1	0	0	1	1
12	0	1	1	0	0	1
15	0	1	1	1	1	1
21	1	0	1	0	1	1
22	1	0	1	1	0	1
29	1	1	1	0	1	1
1	1	1	1	1	0	1

Problem 3:

Circuit design in DSCH2:



Time Diagram:



When the reset button the flip flops receive a default value. Here around 60 to 145ns the flip flop gets a default value of 0000. This value gets inverted and gives an output of hexadecimal value F (1111). After 145ns the reset function stops. In this flip flop when the clock will move from higher to lower the output will flip. At 145ns the clock value gets higher to lower and Q0 flip flop which takes clock value as input, flips lower to higher. At this instance, the value of the flip flops will be 0001. After inverting operation the display gives the hexadecimal value of E (1110). Q0 will remain high until another higher to lower operation occurs in clock. At 165ns the clock will go from higher to lower. As a result, the Q0 will be flipped from higher to lower. Q1 flip flop takes Q0 value as input. Since, Q0 flip higher to lower, Q1 will change from lower to higher. Now the total flip flop value is 0010. So the display shows D (1101). Q1 will stay high until Q0 flips higher to lower. Around 185ns the clock moves higher to lower. So Q0 will also flip lower higher. But Q1 will still remain high as Q0 did not move higher to lower. At 200ns the clock and Q0 both will move from higher to lower. As the input of Q1 moves higher to lower, Q1 will now flip. Now Q2 uses Q1 output as it's input. Since Q2 moves higher to lower, Q2 nower will flip from lower to higher. Now the flip flop values will be 0100. So the display output will be B (1011). Q3 takes Q2 value as input. At 250ns Clock, Q0, Q1, Q2 all flips higher to lower. For this Q3 flips from lower to higher. So at 250 ns the display shows 0111 or in hexadecimal 7 as output, The same process occurs like a loop. Until the reset button is pushed.