

CSE460L: Assignment 0

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Section: 02

Couse: CSE460

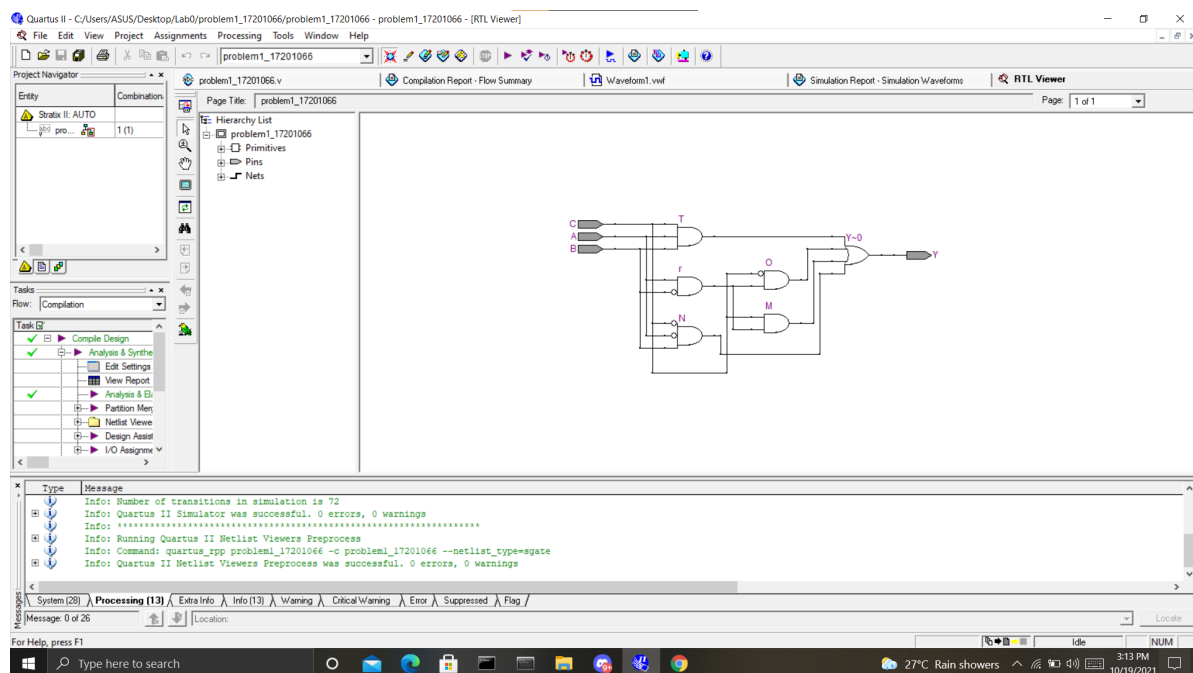
Problem 1: (a)

$$Y = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$$

The truth table for the logic circuit expressed by the equation above:

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

The output Y is the combination of four NOT Gates, five AND Gates and one OR Gate logic operations.



(b) Code for above logic circuit:

```
1 module problem1_17201066(Y, A, B, C);
2   input A, B, C;
3   output Y;
4
5   assign A_ = ~A;
6   assign B_ = ~B;
7   assign C_ = ~C;
8
9   assign p = A_ & B_;
10  assign M = r & C_;
11
12  assign q = A_ & B;
13  assign N = q & C_;
14
15  assign r = A & B;
16  assign O = r & C_;
17
18  assign i = A & B;
19  assign T = i & C;
20
21  assign X = M | N;
22  assign Z = O | X;
23  assign Y = T | Z;
24
25 endmodule
26
```

Messages:

- Info: *****
- Info: *****
- Info: Command: quartus_rpp problem1_17201066 -c problem1_17201066 --netlist_type=sgate
- Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off problem1_17201066 -c problem1_17201066
- Info: Number of transitions in simulation is 72
- Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
- Info: Quartus II Netlist Viewer Preprocess was successful. 0 errors. 0 warnings

Summary:

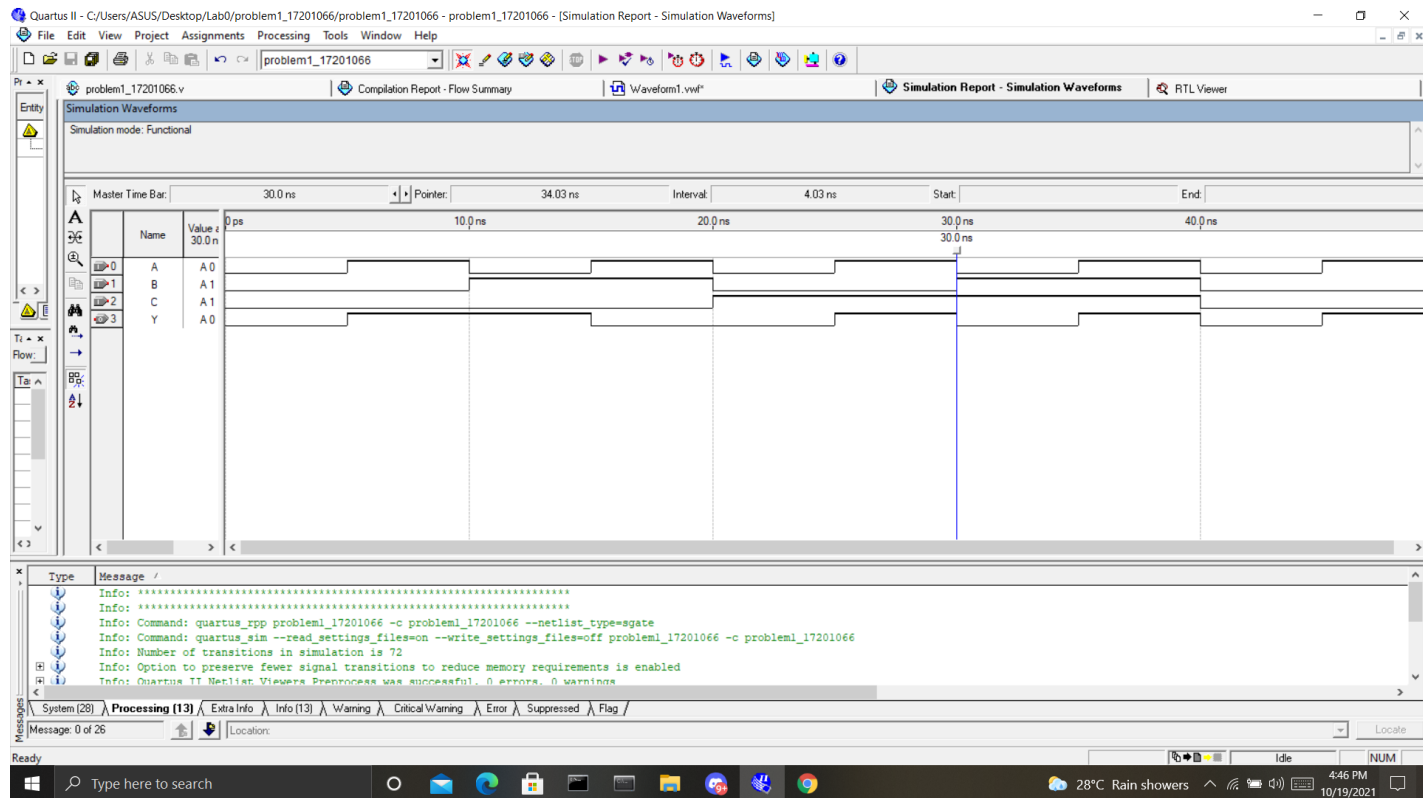
Flow Summary

Flow Status	Successful - Tue Oct 19 14:51:22 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem1_17201066
Top-level Entity Name	problem1_17201066
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total pins	0
Total virtual pins	4 / 343 (1 %)
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

Messages:

- Info: *****
- Info: *****
- Info: Command: quartus_rpp problem1_17201066 -c problem1_17201066 --netlist_type=sgate
- Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off problem1_17201066 -c problem1_17201066
- Info: Number of transitions in simulation is 72
- Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
- Info: Quartus II Netlist Viewer Preprocess was successful. 0 errors. 0 warnings

Simulated Waveform for 50ns:

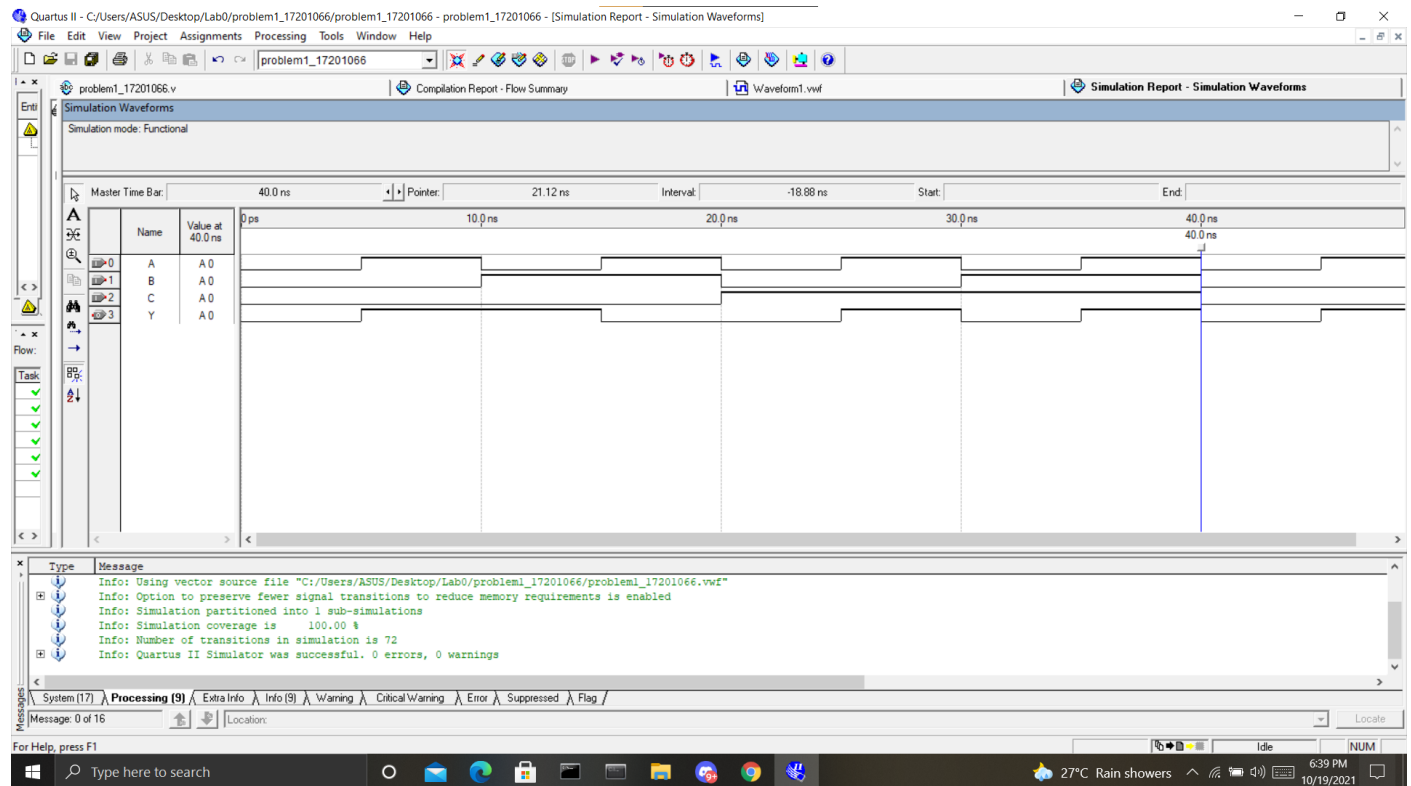


Truth table of the simulated result in Quartus II:

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	0
1	1	1	1

From the 20 to 25ns interval, the Output value Y is 0 for A, B and C are 0, 0, and 1. However, from the truth table of problem 1(a), we can see. The output Y is 1 for A, B, and C are 0, 0, 1.

The screenshot displays the Quartus II software interface during a simulation. The main window shows the 'Simulation Waveforms' for a circuit simulation. The top bar indicates the project name 'problem1_17201066.v' and the waveform name 'Waveform 2*'. The left pane shows the 'Entity' list with signals A, B, C, and Y. The main area shows the waveform for these signals over a 50.0 ns period. The bottom pane shows the 'Task' list with 'Processing' selected. The status bar at the bottom indicates 'Message: 0 of 16'.



The truth table of the Quartus II simulation:

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	0
1	1	1	1

Applying random variables to each, we can see, between 5 to 10 ns, the values of A, B and C are 1, 0, 0. The output we got after putting A, B and C values on logical expression is 1. Similar result we achieved the truth table of problem-1(a).

But between 25 to 30 ns interval, we get output y is 1 for A, B and C are 1, 0 and 1 respectively. However, we achieved output Y is 0 for the same values in problem-1(a) truth table.

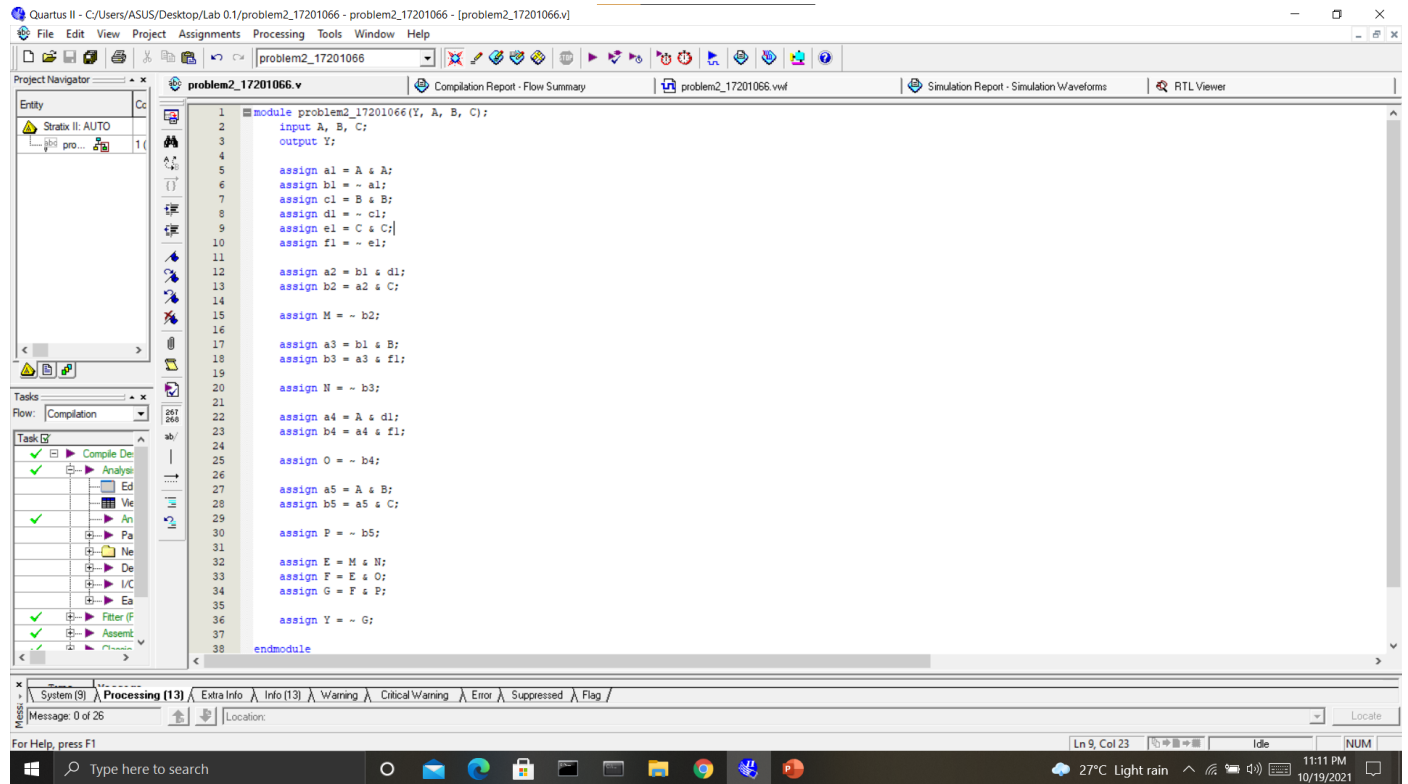
(d) NAND is a universal gate. Any logical gate can be replaced by NAND. If the given equation is modified so that the logic circuit is composed of only NAND gates, the new logic expression will be,

$$Y = (((A.A)' . (B.B)' . C)' . ((A.A)' . B . (C.C)')' . (A . (B.B)' . (C.C)')' . (A . B . C)')'$$

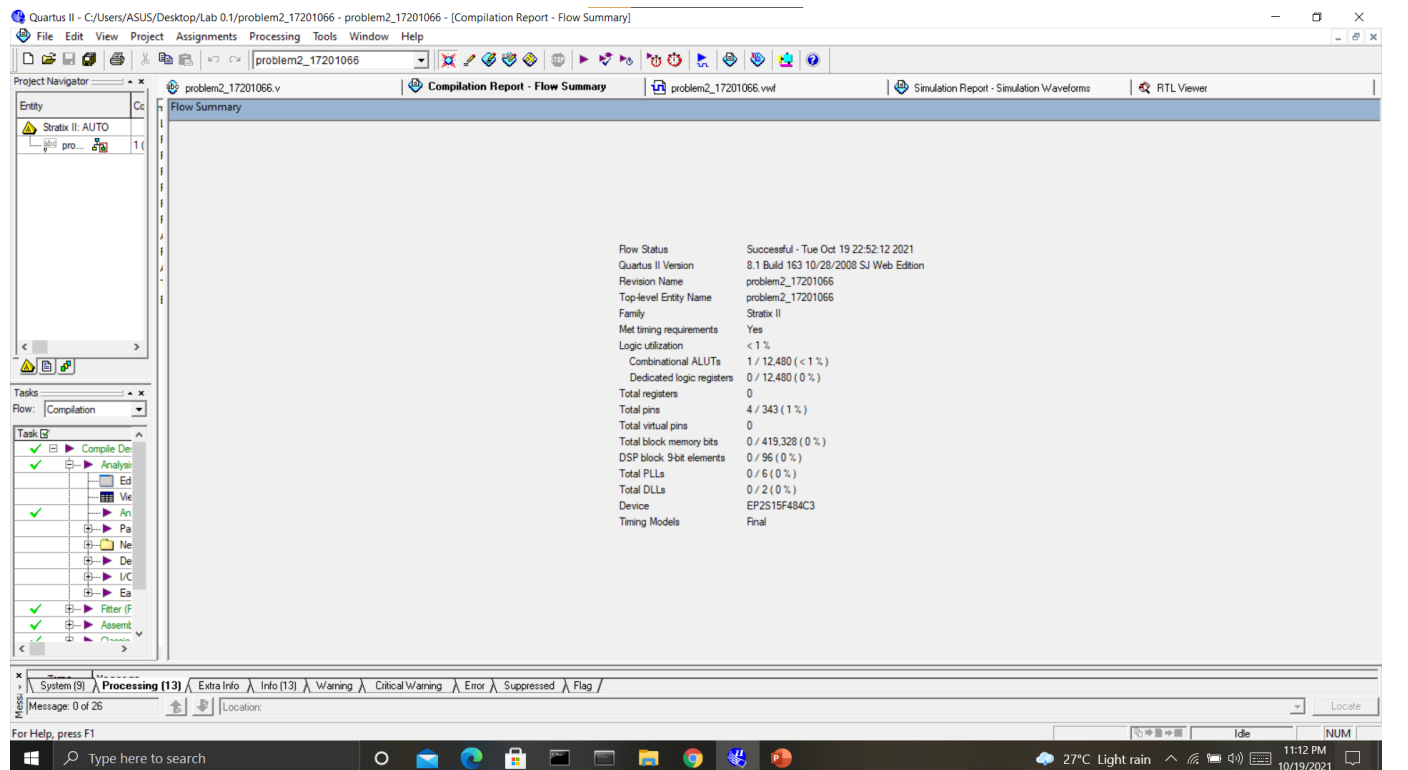
$$= (A' . B' . C + A' . B . C' + A . B' . C' + A . B . C)$$

New equation has been applied to Quartus II.

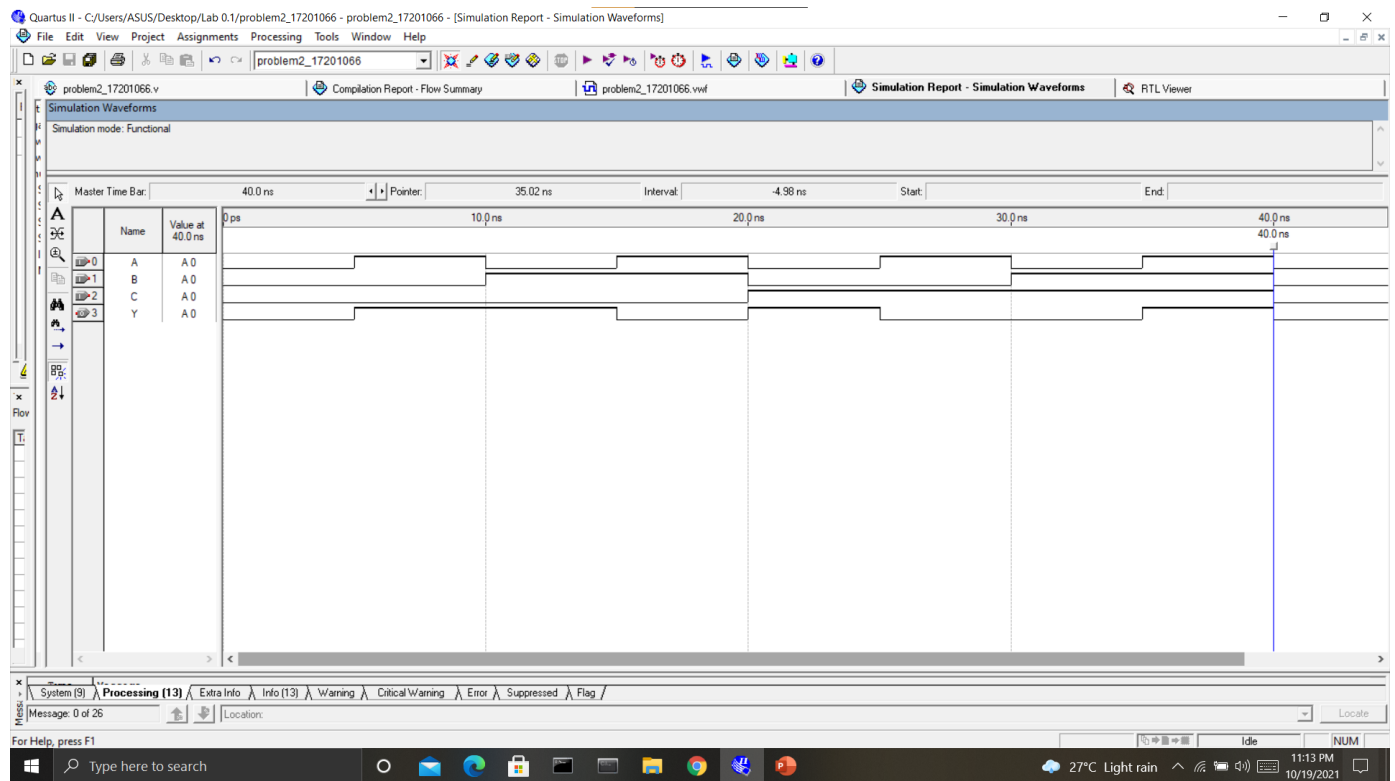
Code:



Summary:



Simulation Waveform:



Truth Table:

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

This truth table is equivalent to the truth table that has been computed at Problem-1 (a)

Circuit Diagram:

