CSE460L: Assignment 2 (Fall 2021)

Sections: 1, 2, 3, 4, 5, 6, 7, 8 & 9

Assignment 2 submission link:
https://docs.google.com/forms/d/e/1FAIpQLSeuUXWMrso25hZcOuOVmBHtUEMrHpzQQMZEOT7QbKpj0JTNMA/viewform?usp=sf_link

Assignment 2 deadline: **29 Nov, 2021, 4.59 PM (BDT)**

General guidelines

- Assignments are individual

- Each assignment will contain 3 to 4 problems

- **For each problem you will need to prepare 3 parts:**
  1. **Code:** attach a screenshot of your code from Quartus.
  2. **Output:** **attach *FULL SCREEN* screenshots** of
     - Compilation Report - Flow Summary (Compilation report of the .v file)
     - Simulation Report - Simulation Waveforms (Simulation report of the .vwf file)

  [**Tampered/edited/cropped screenshots will be considered as a violation of general guidelines and therefore will not be accepted**]

  3. **Discussion/Explanation:** explain the output waveforms of your simulation report as described in the **Expected Output** section within each problem statement.

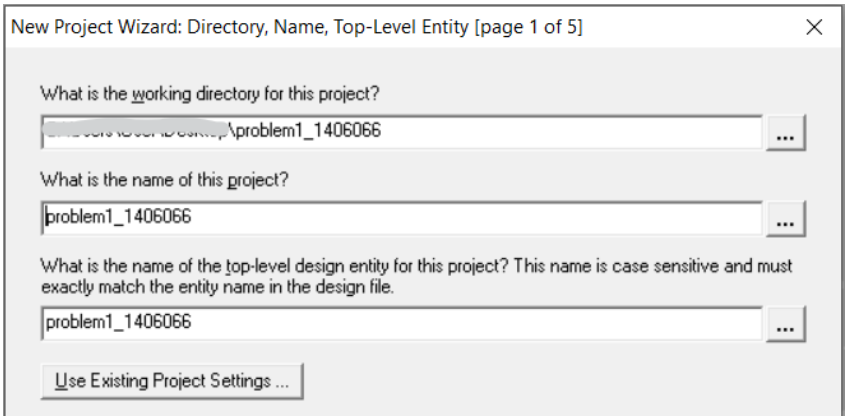
- Each problem will be of equal points. You will not be graded on the length/number of code/explanation/outputs; rather on the clarity, readability and precise explanations of your code/logic/outputs

- Points distribution for each problem is

  Code: **40%**
  Output: **20%**
  Discussion/Explanation of output: **40%**

- **You will need to create separate directories/project for each problem**

- **The name of your working directory for each problem of the assignment should be …\problem#_StudentID [# = 1/2/3/4..]**
  For example, for problem 1 the name of the directory should be problem1_1406066



- Consequently, the name of your main module in the Verilog file should be problem#_StudentID [# = 1/2/3/4..]
  Continuing from the previous example, the name of the module should be problem1_1406066

- Finally, **compile all the problems for a given assignment into a single pdf file**

- The **name of the pdf should be Section_StudentID_assignment2.pdf** (Example: 1_1406066_assignment2.pdf)

Detailed marks distribution for all problems of *Assignment 2*:

Code		6
Output	Compilation report	1
	Simulation report (Timing diagram)	3
Discussion	State diagram	3
	State assigned table	3
	Brief explanations of output	4
Total		**20**

Problem for Assignment 2

1. An FSM has an input w and an output z. The machine has to generate z = 1 when the following patterns in w are detected: 11 or 111; otherwise, z = 0. Reset functionality is not mandatory. **Draw the state diagram, the state-assigned table, write the Verilog code, run simulations and verify your answer.** An example timing diagram can be found here:

clock	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}
w	0	1	1	1	0	1	0	1	1	1	1	0
z	0	0	0	**1**	**1**	0	0	0	0	**1**	**1**	**1**

Expected Output:

The timing diagram should contain waveforms as described in the table. The clock period should be 10 ns. The discussion must contain a state diagram, state assigned table, and brief explanations of all high output situations e.g. z is high during t_5, $t_{11,}$ and t_{12} clock cycles. Briefly explain these situations in light of the problem statement and your derived state diagram/state assigned table.

2. You have to design a vending machine for a 4 Tk product. The vending machine can only accept inputs: no money (can be represented as input w=00), Tk 1 (can be represented as input w=01), and Tk 3 (can be represented as input w=10). Once an acceptable input is more than or equal to 4 Tk, the machine immediately generates an output Q=1, goes back to the initial state, and gives back the change (if required). Change in Tk is represented as 2 digit binary output c={c1c2}. Output c has to be calculated and initialized. Suppose, changes are 1Tk, 2Tk (assumed). Initialize 1Tk as c=00 and 2Tk as c=01. Reset functionality is not mandatory. **Draw the state diagram, the state-assigned table, write the Verilog code, run simulations and verify your answer.**

clock	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}
Tk input	0	1	3	0	3	1	0	3	3	0	3	0
w	00	01	10	00	10	01	00	10	10	00	10	00
Q	0	0	1	0	0	1	0	0	1	0	0	0
c	?	?	?	?	?	?	?	?	?	?	?	?

Expected Output:

The timing diagram should contain waveforms as described in the table. The clock period should be 10 ns. The discussion must contain a state diagram, state assigned table, and brief explanations of all high output situations e.g. Q is high during t_3, t_6, and t_9 clock cycles. Briefly explain these situations in light of the problem statement and your derived state diagram/state assigned table. Also, initialize and complete output c.

3. An FSM has an input w and an output z. For every three bits that are observed on the input w during three consecutive clock cycles, the FSM generates a z = 1 if and only if the number of 1s in the three-bit sequence is even. Overlapping input patterns are not allowed**. Draw the state diagram, the state assigned table, write the verilog code, run simulations and verify your answer.**

Clock	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}	t_{16}
w	0	0	1	0	1	1	0	1	0	1	0	1	0	1	1	0
z	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1

Expected Output:

The timing diagram should contain waveforms as described in the table. The clock period should be 10 ns. The discussion must contain a state diagram, state assigned table and the brief explanations of all high output situations e.g. z is high during t_7, t_{13}, t_{16} clock cycles. Briefly explain these situations in light of the problem statement and your derived state diagram / state assigned table.