A 39% PAE Type-AB Power Amplifier for Car Radar Applications

Jakov Sola, Simon Pedersen

ESAT - KU Leuven

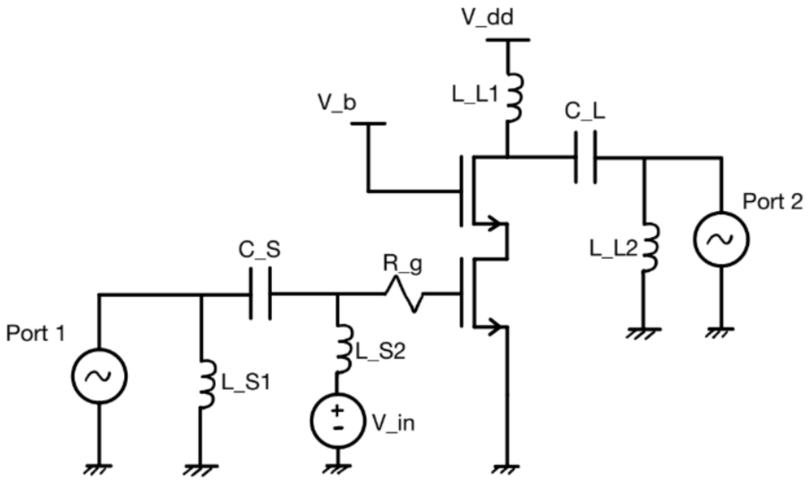
Specifications and Application

This report presents a power amplifier (PA) designed for the specifications listed in table 1 [3]. Where P_{sat} is the saturated output power, f is the operating frequency and V_{dd} is the power supply.

Typology	P_{sat}	f	V_{dd}	Technology	Software
Cascode	23dBm	24GHz	2V	45nm CMOS	Cadence & ADS

Table 1: PA desired specifications

Radar applications usually requires high power outputs and therefore high power added efficiency (PAE), this is because the distance between the radar and the detected object is normally large. However, in a car radar application where the distance between objects is low. The output power can be lowered hence lowering the PAE requirement. A class-AB amplifier offers higher PAE than a class-A, at the cost of slightly more distortion to the signal. Continuous waveforms are good for velocity measurements through the Doppler effect [1], while pulsed signals have better range accuracy [2], both of them are important in a car radar, so a choice of a combination between the two with a class-AB amplifier was made.



Component	Value
C_S	614fF
L_{S1}	328pH
L_{S2}	62pH
C_L	294fF
L_{L1}	62pH
L_{L2}	150pH
W	1mm
L	45nm
V_b	1.46V
Vb_{in}	543mV
R_g	1Ω

Figure 1: Schematic and parameters

Methodology

The design started of with a pragmatic choice of $Vb = 1.6V$, $V_{in} = 600mV$ and $L = L_{min} = 45nm$, intended to design for a class AB-amplifier.

From previous attempts not achieving P_{sat} due to a small transistor width, W was set to 1mm. The stabilizing resistor was chosen as $R_g = 1\Omega$ to enforce stability.

The amplifier was matched to the load and source impedance for maximum voltage gain by inductor-capacitor-inductor matching networks (LCL-matching networks). This was done in a iterative way by monitoring practical inductor values through ADS and adjusting the corresponding Q-factor while matching the network.

After gain matching, the output network was removed and conjugate matched to maximizing power delivered to the load. The source side (impedance matched network) and load side (conjugate matched network) had to be adjusted a few times because they influence each other through parasitic capacitance. This step was also done by adjusting for simulated Q-factors in ADS for corresponding inductors. Further a parametric sweep of V_b, V_{in} and R_g was performed to choose the values giving the highest P_{1dB}. As a consequence, the input network needed to be matched again.

A design choice was made so that the power gain would not have peaking before the P_{1dB} point. This was adjusted through V_b and V_{in}, effectively adjusting the damping factor, resulting in a lower P_{1dB}.

The transient output swing showed distortion in the upper half of the waveform, as expected from a class AB amplifier.

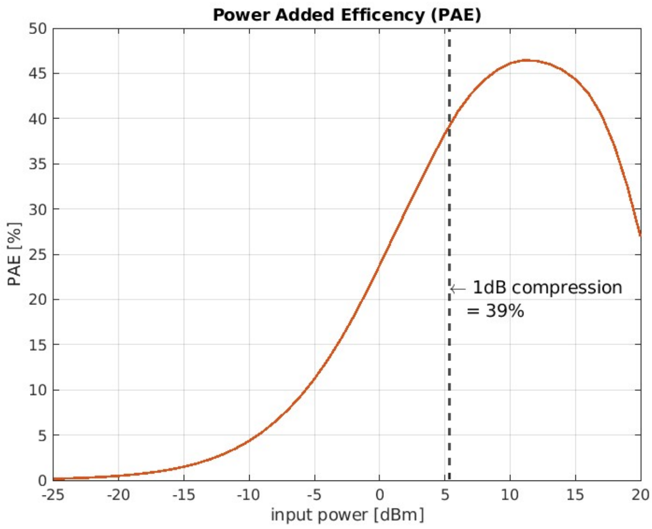


Figure 2: Power added efficency

Results

In table 2 results for the operating frequency is presented. Where P_{1dB} is the one dB compression point (input referred). P_{sat} is the saturated output power, P_{DC} is the DC power consumption, PAE is the power added efficiency at P_{1dB} and PAE_{max} is the maximum power added efficiency. Further the scatter parameters are shown in dB20. The k_f indicates the stability of the amplifier.

P_{1dB}	P_{sat}	PAE	PAE_{max}	S_{11}	S_{22}	S_{12}	S_{21}	K_f	P_{DC}
5.3dBm	23.1dBm	39.1%	46.4%	-24.3dB	-2.1dB	-36.2dB	-36.2dB	2.0	220mW

Table 2: PA results

Figure 2 shows the power added efficiency over input power, achieving 39% PAE at the P_{1dB} point. The PAE at the P_{1dB} is reasonably close to the desired value PAE_{max}. The power gain is shown in the left plot of figure 3. The gain is constant with no peaking, up until a cut-off point where it decreases. Output power as a function of input power is shown in the right part of figure 3. The power output reaches the requirements without over designing $P_{sat} = 23.1dBm > 23dBm$.

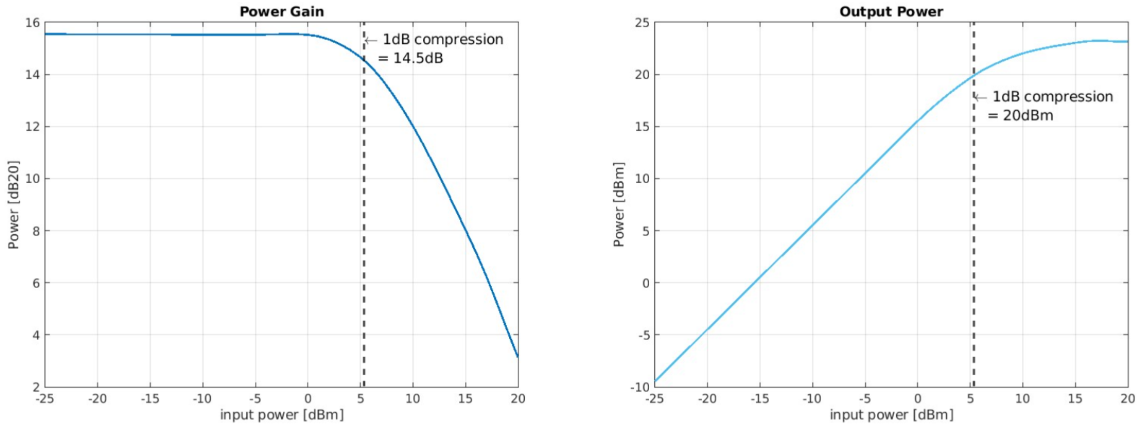


Figure 3: Power gain (left) and Output power (right)

Scatter parameters for the amplifier is shown in figure 4. Subplot b) reveals that the output network is not optimized to absorb signal from the load port. It was challenging to lower S_{22} while simultaneously maintaining high power gain. Ideally in subplot c) $S_{12} = 0$, but $S_{12} = -36.2dB$ is good. A value of $S_{21} = 15.5dB$ from d) is realistic, because the maximum gain during the gain matching of the circuit was 23dBm, optimizing the output network for power gain will lower the voltage gain.

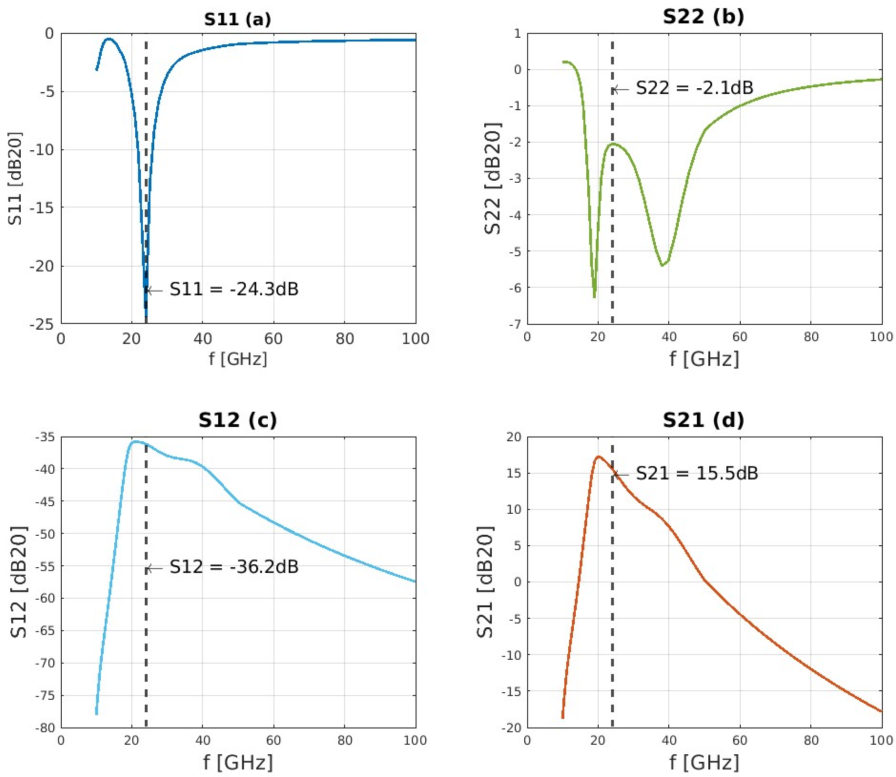


Figure 4: Scatter parameters

The stability factor K_f is plotted over frequency in figure 5. The requirement for the amplifier to be unconditionally stable is $K_f > 1$, a value of 2 at the operating frequency might imply that the stability resistor can be lowered to reduce power loss.

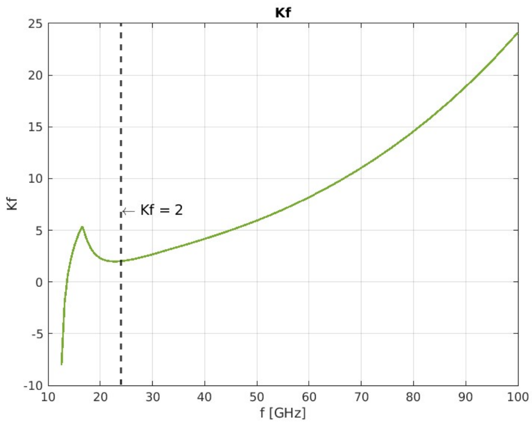


Figure 5: Stability measure K_f

Figure 6, 7, 8 shows the different inductor layouts used and its characteristic over frequency. The metal height is 1um. The matching networks use four inductors in total. Two of which are identical (62pH).

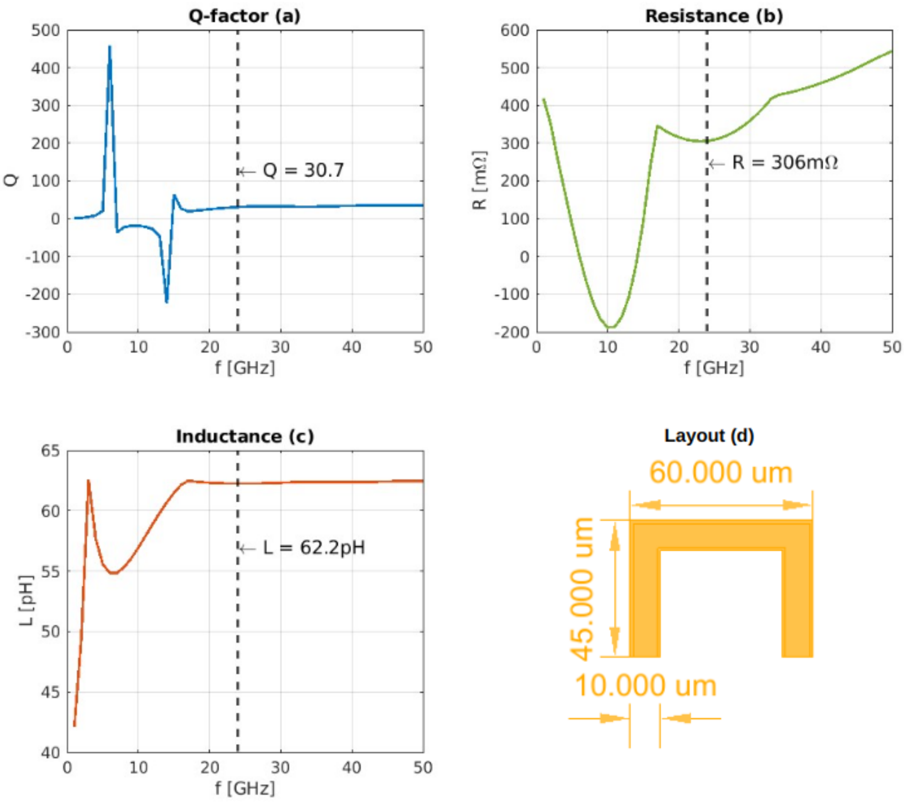


Figure 6: A 62pH inductor

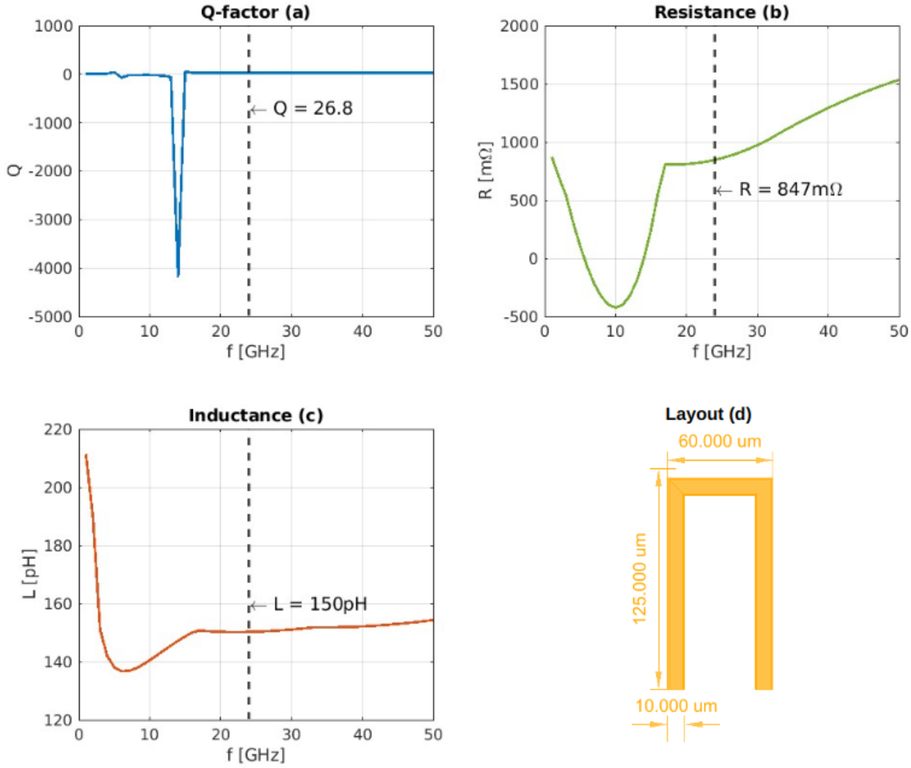


Figure 7: A 150pH inductor

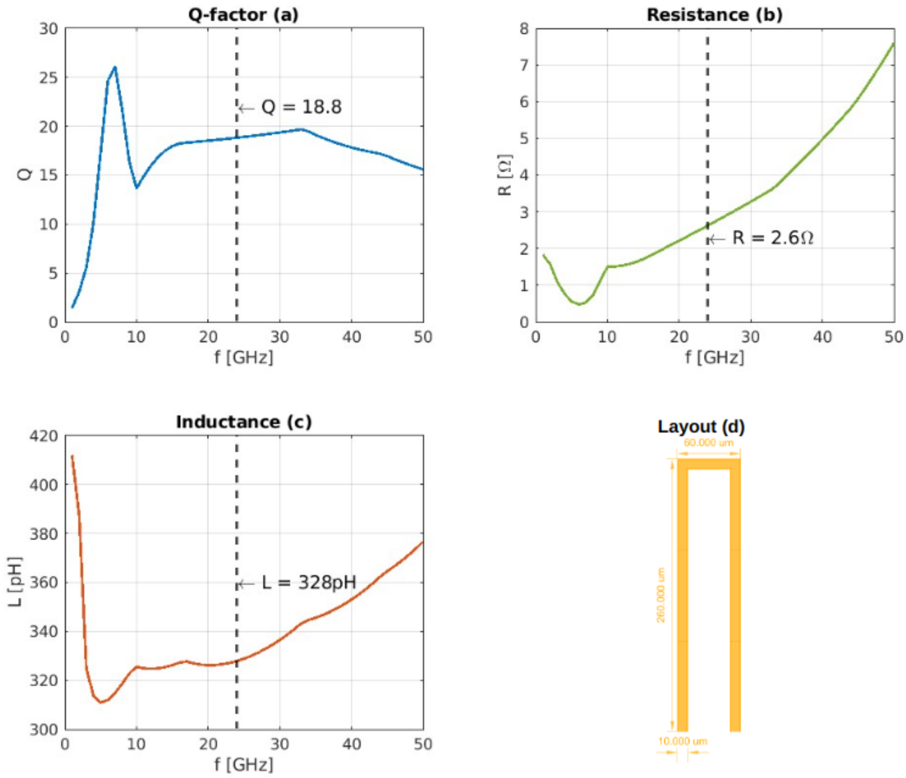


Figure 8: A 328pH inductor

References

[1] Michael Davis. "Radar Frequencies and Waveforms". *Georgia Tech Research Institute*, 2011.

[2] Dr. Robert M. O'Donnell. "Radar Systems Engineering Lecture 11 Waveforms and Pulse Compression". *IEEE New Hampshire Section*, 2010.

[3] Prof. Patrick Reynaert. "Design of High-Frequency Integrated Circuits". *KU Leuven, ESAT-MICAS, Belgium*, 2023.