Design of a Switched-Capacitor Amplifier

H05E4a DAMSIC Project 2023

Parts I, II and III: Parameter derivation, Ideal, Symmetrical, Folded and Gain Boosted OTA

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Group ID: 2

1 General Information and Summary

1.1 Given Target Specifications

Parameter	Unit	Specification
Sampling Frequency	MHz	**50**
SNR	dB	**45**
Static Gain Error	%	**0.05**
Dynamic Settling Error	%	**2.2**
Phase Margin (Min.)	deg	**60**
C_L	pF	**2**
Min. Input Swing	mV_{pp}	**50**
Max. Input Swing	mV_{pp}	**100**
Closed-Loop Gain	V/V	**10**
Input Pair	-	**nmos**

1.2 Derivation of System Design Parameters

$$C_{FB} = \frac{1}{10} C_{in}$$

$$A_{OL} = \frac{A_{idealCL}(\epsilon_{gain} + 1)}{1 - \beta A_{idealCL}(\epsilon_{gain} + 1)} = \frac{10.005}{1 - \frac{1}{10} 10.005} = -20010$$

$$BW = -\frac{2 f_s \ln(\epsilon_{set})}{2\pi} = -2 \times 50 \times 10^6 \times \frac{\ln(0.022)}{2\pi} = 60.7MHz$$

$$GBW = A_{CL} BW = 10.005 \times 60.7 \times 10^6 = 607MHz$$

$$G_m = GBW \times 2\pi \times C_{out} \approx GBW \times 2\pi \times C_l = 7.63mS$$

2 Ideal OTA

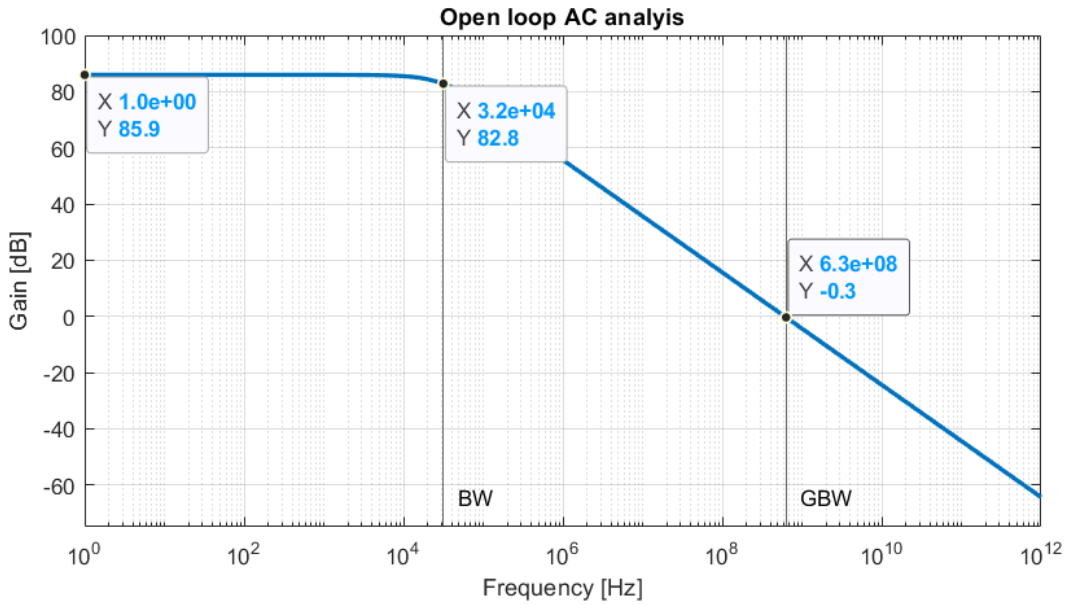


Figure 1 Open loop amplitude response[1]

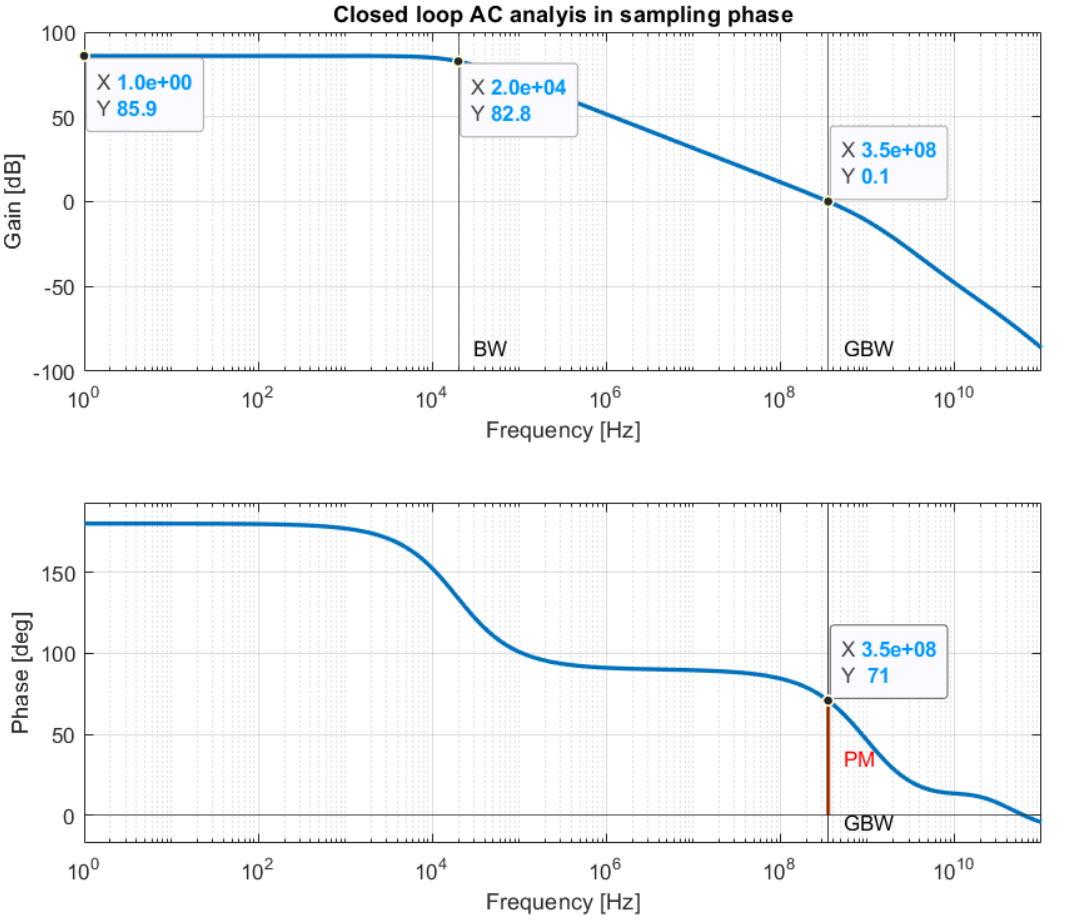


Figure 2 Closed loop amplitude and phase response (sampling phase)

[1] Data tips on all of the plots are dynammically placed to the closest sample point by a Matlab script

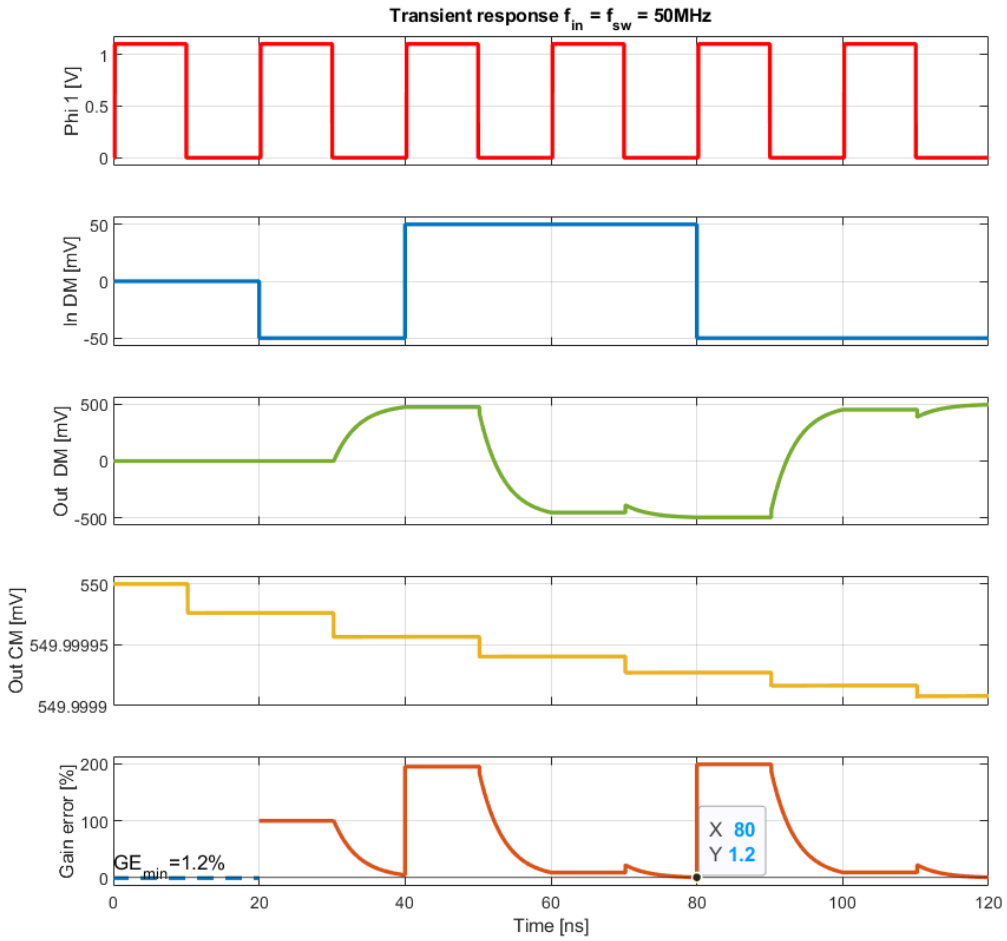


Figure 3 Transient simulation with fsw=fin=50MHz

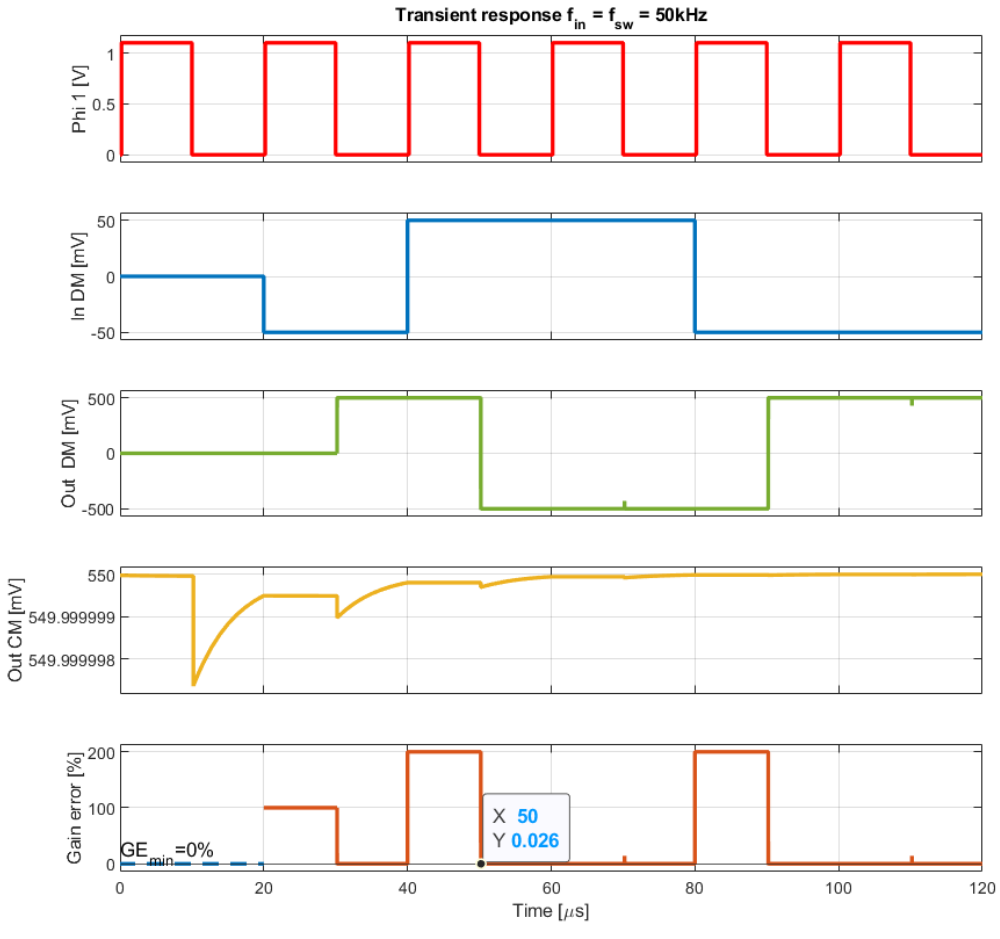


Figure 4 Transient simulation with fsw=fin=50kHz

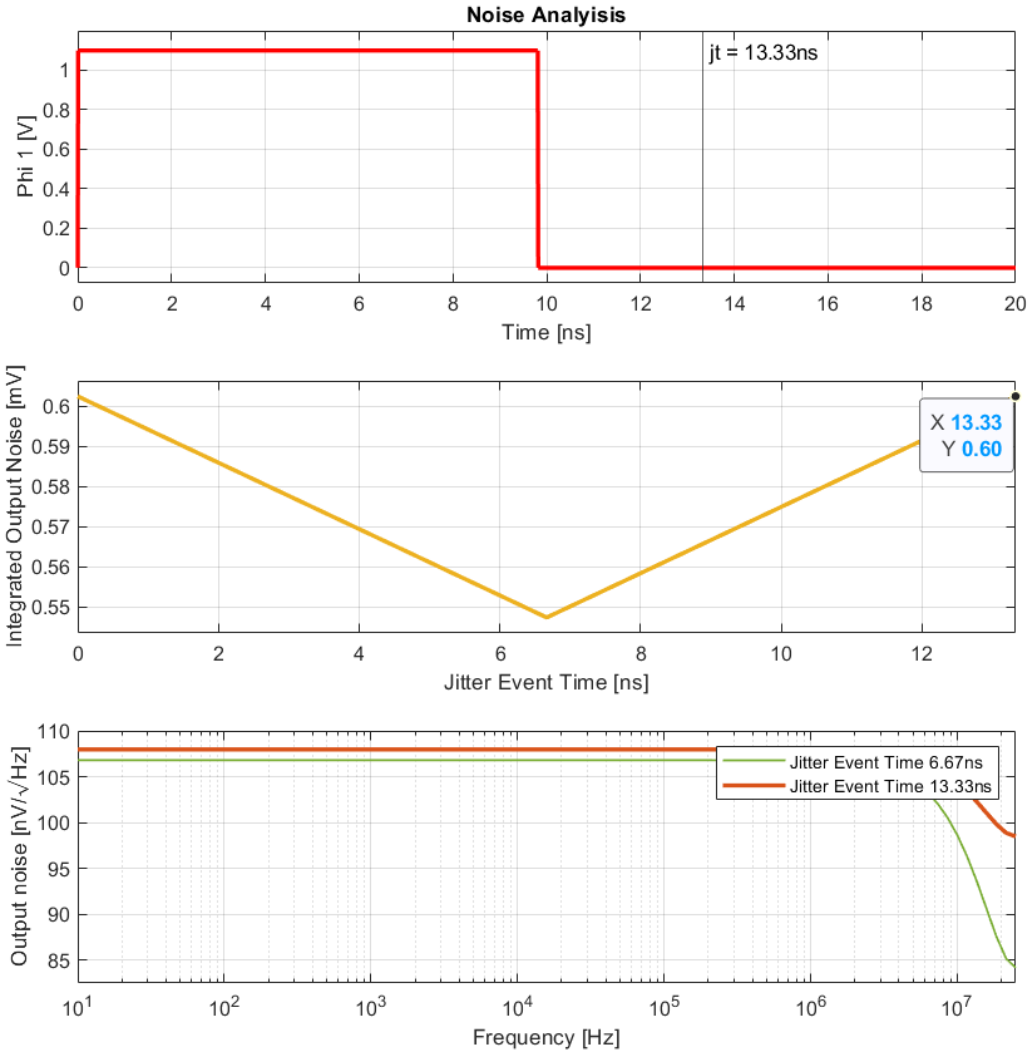


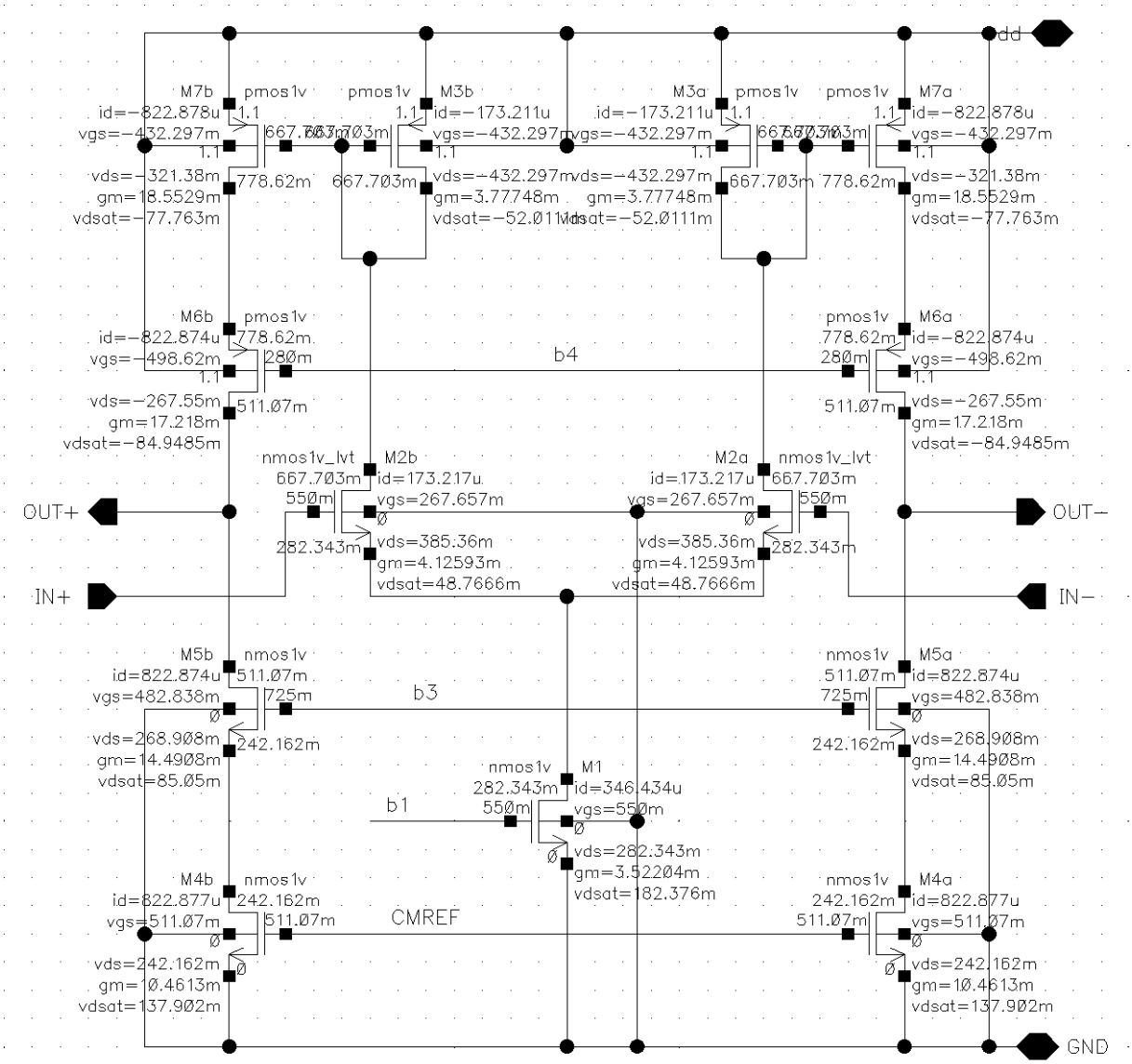
Figure 5 Noise simulation

3 Symmetrical OTA

3.1 Table of Achieved Results

Parameter	Unit	Achieved
Input Swing	mV_{pp}	**100**
Output Swing	mV_{pp}	**964**
Total Integrated Output Noise	mV_{rms}	**3.24**
SNR	dB	**40.8**
C_L	pF	**2**
C_{FB}	pF	**0.23p**
C_{IN}	pF	**2.3p**
Open-Loop Gain	dB	**53.4**
Closed-Loop Gain	V/V	**9.64**
GBW (Sample Phase)	MHz	**630**
Phase Margin (Sample Phase)	deg	**31**
Dynamic Settling Error	%	**3.6**
Static Gain Error	%	**3.3**
Power dissipation	mW	**2.19**

3.2 Schematic Design



Type	Name	Value	Transistor
Supply	vdd	**1.1**	
Bias	b1	**550m**	
	b2	**0m**	
	b3	**725m**	
	b4	**280m**	
	SP	**550m**	
Tail	Wfn_bias	**2u**	M1
	bias_n_L	**1u**	
	bias_n_fn	**30**	
Input (Low Vt)	Wfn_in_n	**2u**	M2
	in_n_fn	**350**	
	in_n_L	**45n**	
Input mirror	Wfn_in_mirror	**2u**	M3
	in_p_fn	**150**	
	in_p_L	**45n**	
Output nMOS	Wfn_n	**2u**	M4/M5
	out_n_L	**300n**	M5
	out_n_fn	**150**	
	out_n_L_2	**600n**	M4
	out_n_fn2	**80**	
Output pMOS	W_fn_p	**2u**	M6/M7
	out_p_fn	**200**	M6
	out_p_L	**300n**	
	out_p_fn2	**330**	M7
	out_p_L2	**200n**	
Load	Cl	**2p**	
CMFB	CMFB_gain	**1**	
	CMFB_r	**10**	
	SP	**550m**	

3.3 Simulation Results

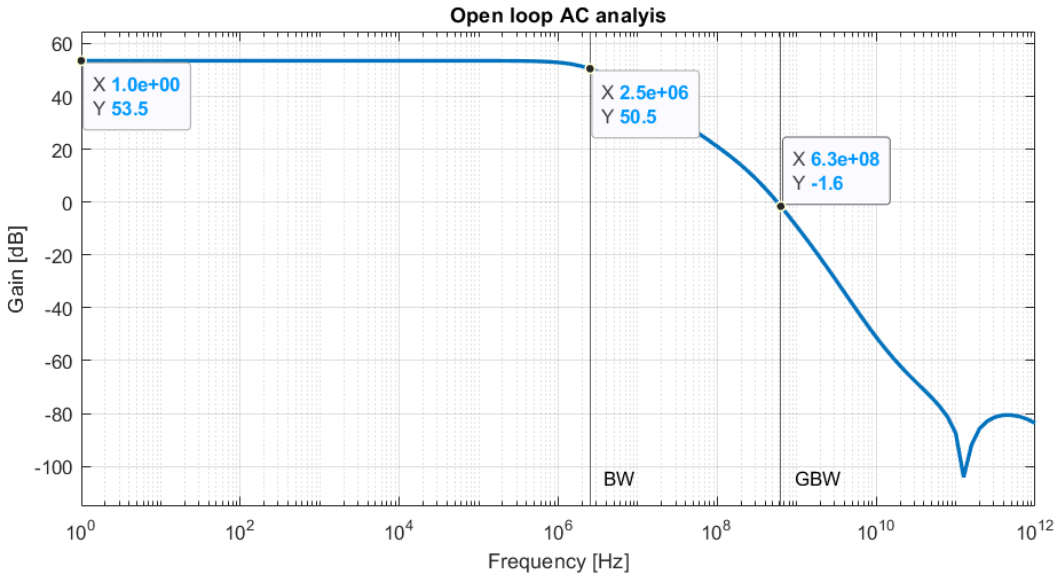


Figure 6 Open loop amplitude response

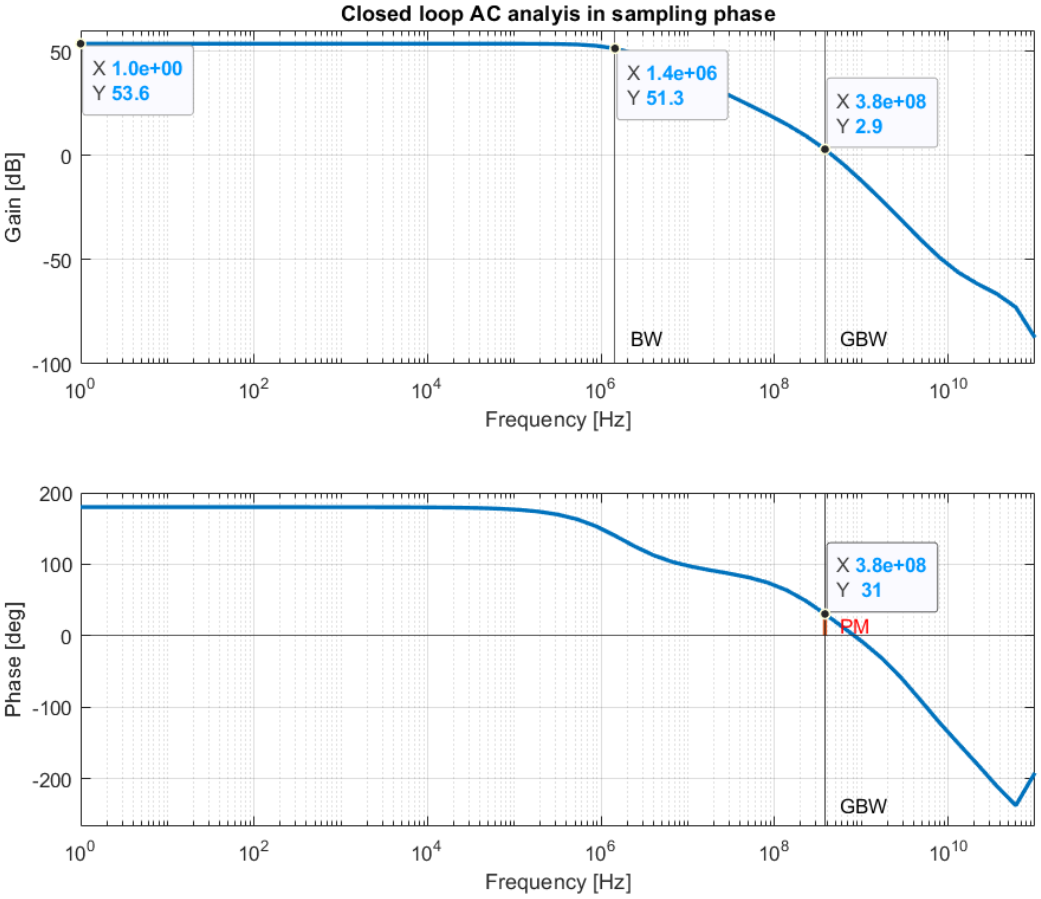


Figure 7 Closed loop amplitude and phase response (sampling phase)

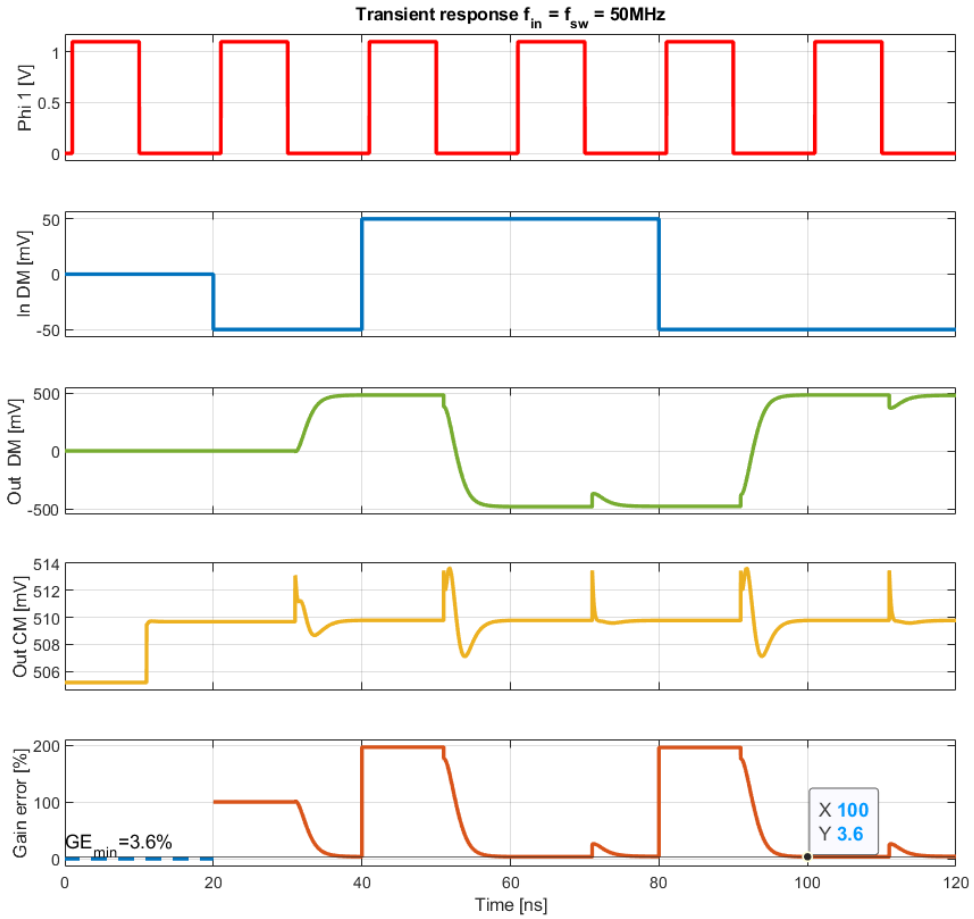


Figure 8 Transient simulation with fsw=fin=50MHz

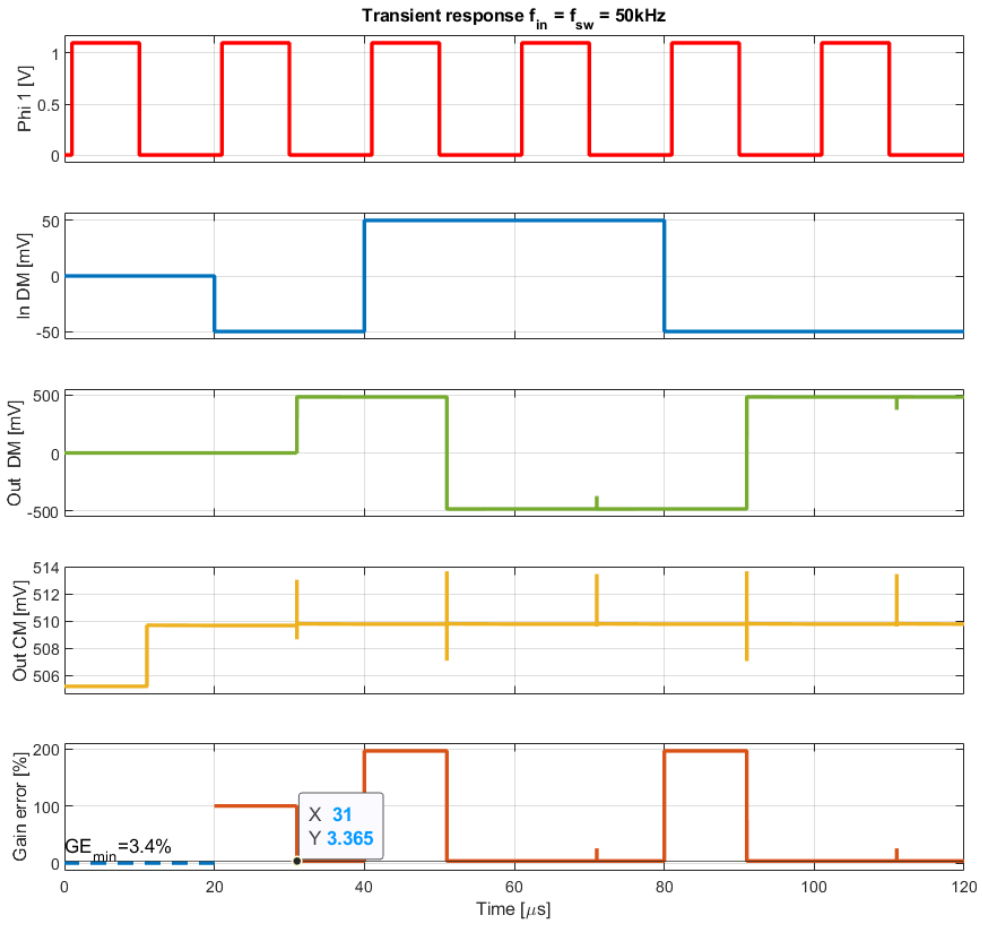


Figure 9 Transient simulation with fsw=fin=50kHz

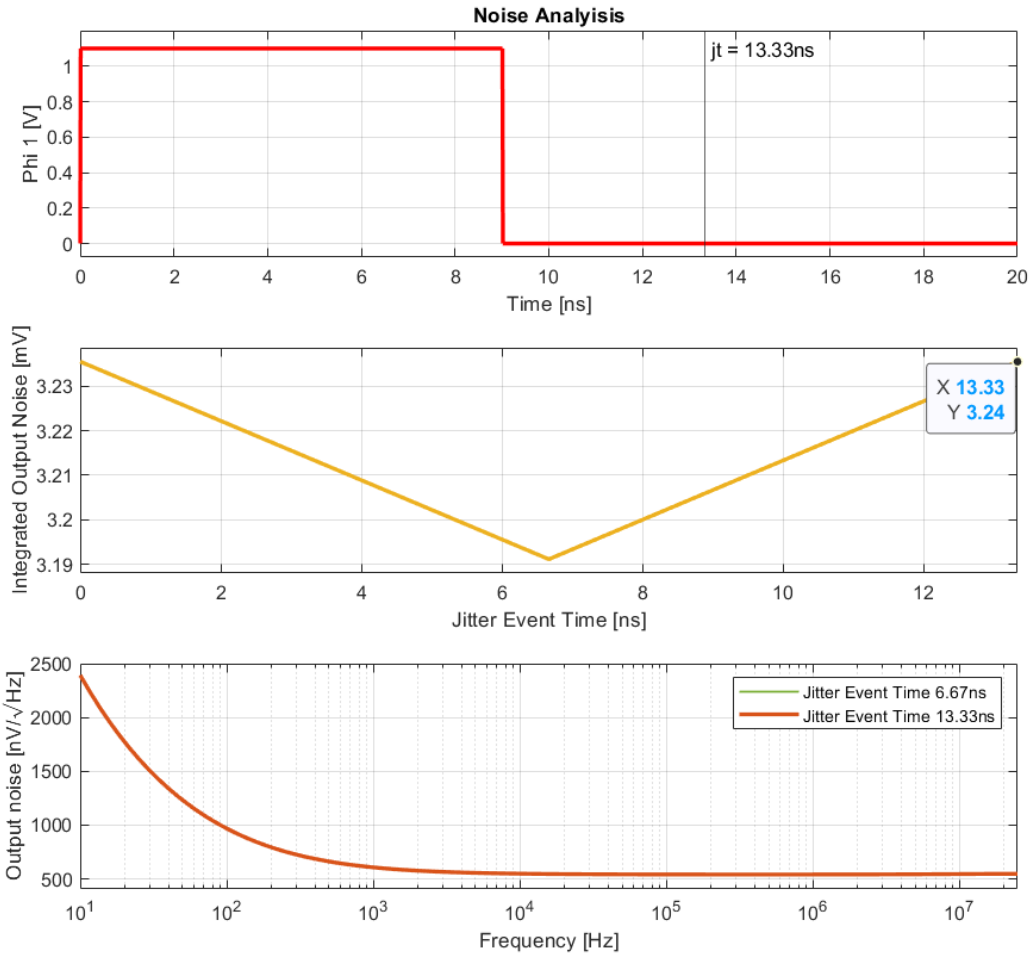


Figure 10 Noise simulation

4 Folded cascode OTA

4.1 Table of Achieved Results

Parameter	Unit	Achieved
Input Swing	mV_{pp}	**100**
Output Swing	mV_{pp}	**932**
Total Integrated Output Noise	mV_{rms}	**1.6**
SNR	dB	**46.9**
C_L	pF	**2p**
C_{FB}	pF	**0.5p**
C_{IN}	pF	**5p**
Open-Loop Gain	dB	**48.3**
Closed-Loop Gain	V/V	**9.34**
GBW (Sample Phase)	MHz	**230**
Phase Margin (Sample Phase)	deg	**82**
Dynamic Settling Error	%	**10.2**
Static Gain Error	%	**6.6**
Power dissipation	mW	**1.98**

4.2 Schematic Design

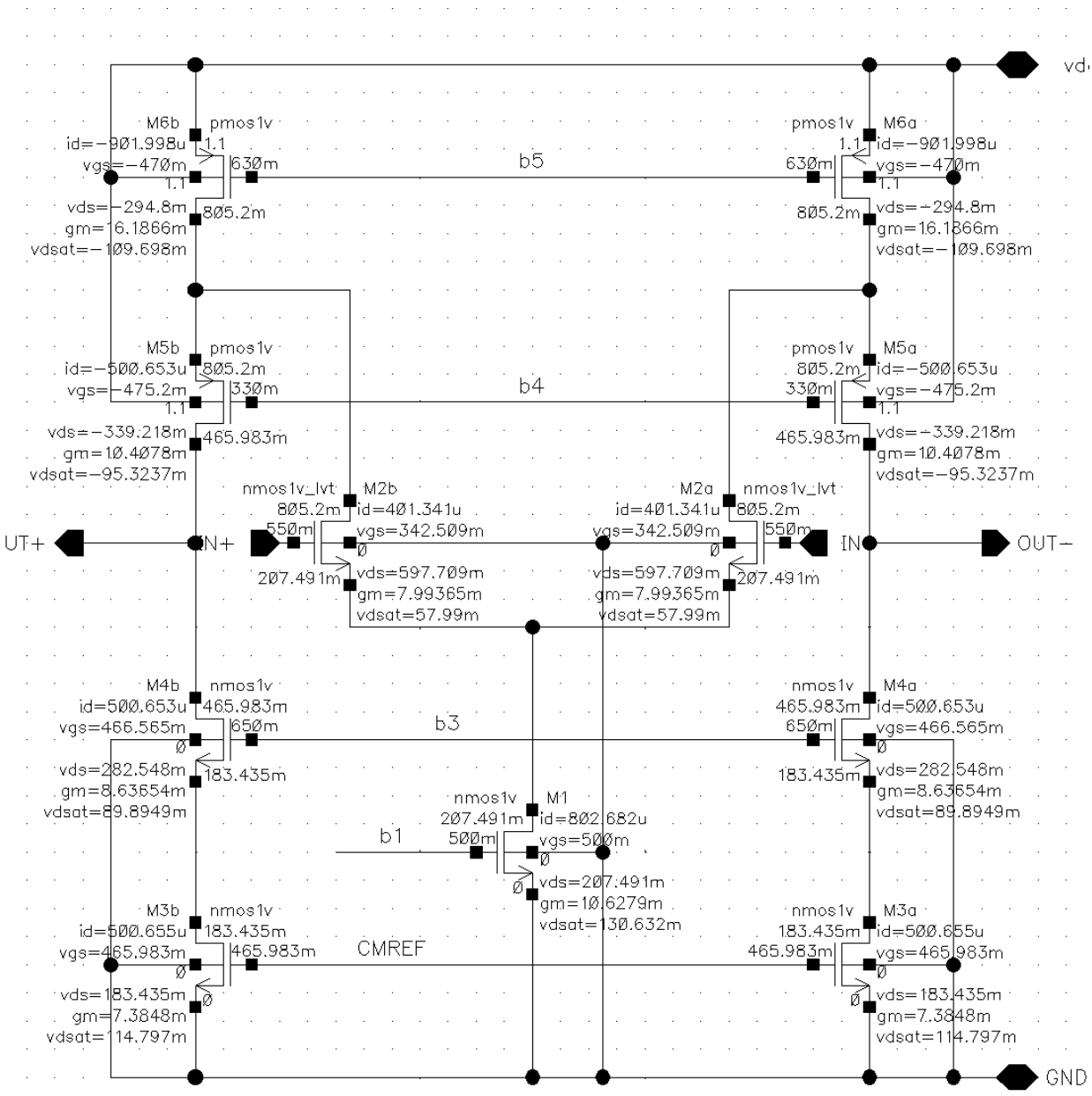


Figure 11 DC Operating point

Type	Name	Value	Transistor
Supply	vdd	**1.1**	
Bias	b1	**500m**	
	b2	**450m**	
	b3	**650m**	
	b4	**330m**	
	b5	**630m**	
	SP	**550m**	
Tail	Wfn_bias	**1.5u**	M1
	bias_n_L	**600n**	
	bias_n_fn	**120**	
Input (Low Vt)	Wfn_in_n	**1.5u**	M2
	in_n_fn	**160**	
	in_n_L	**90n**	
Output nMOS	Wfn_n	**1.5u**	M3/M4
	out_n_L	**450n**	M4
	out_n_fn1	**150**	
	out_n_L_2	**450n**	M3
	out_n_fn2	**150**	
Output pMOS	W_fn_p	**1.5u**	M5/M6
	out_p_fn	**233**	M5
	out_p_L	**390n**	
	out_p_fn2	**233**	M6
	out_p_L2	**450n**	
Load	Cl	**2p**	
CMFB	CMFB_gain	**10**	
	CMFB_r	**1k**	
	SP	**550m**	

4.3 Simulation Results

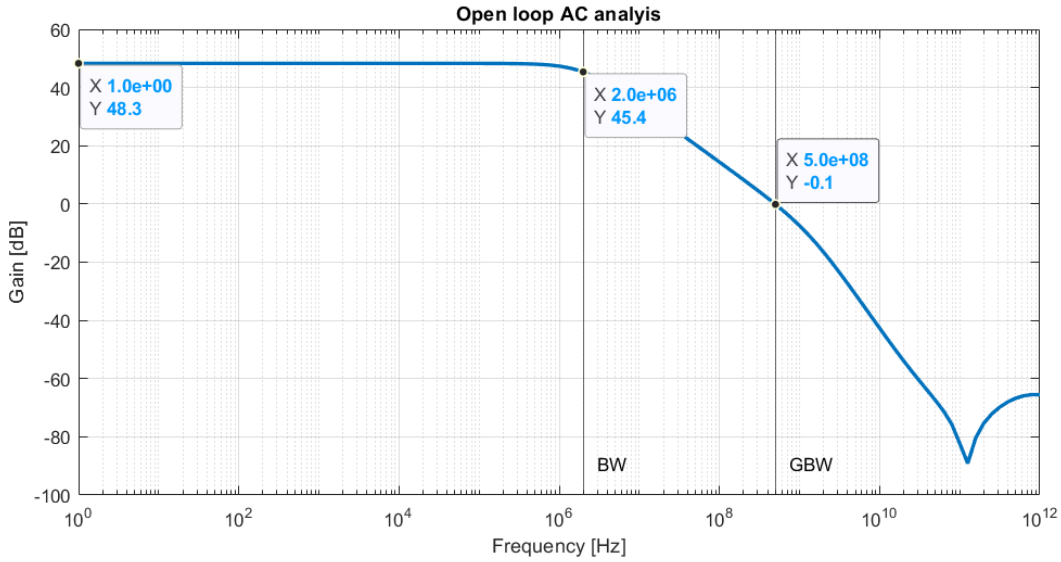


Figure 12 Open loop amplitude response

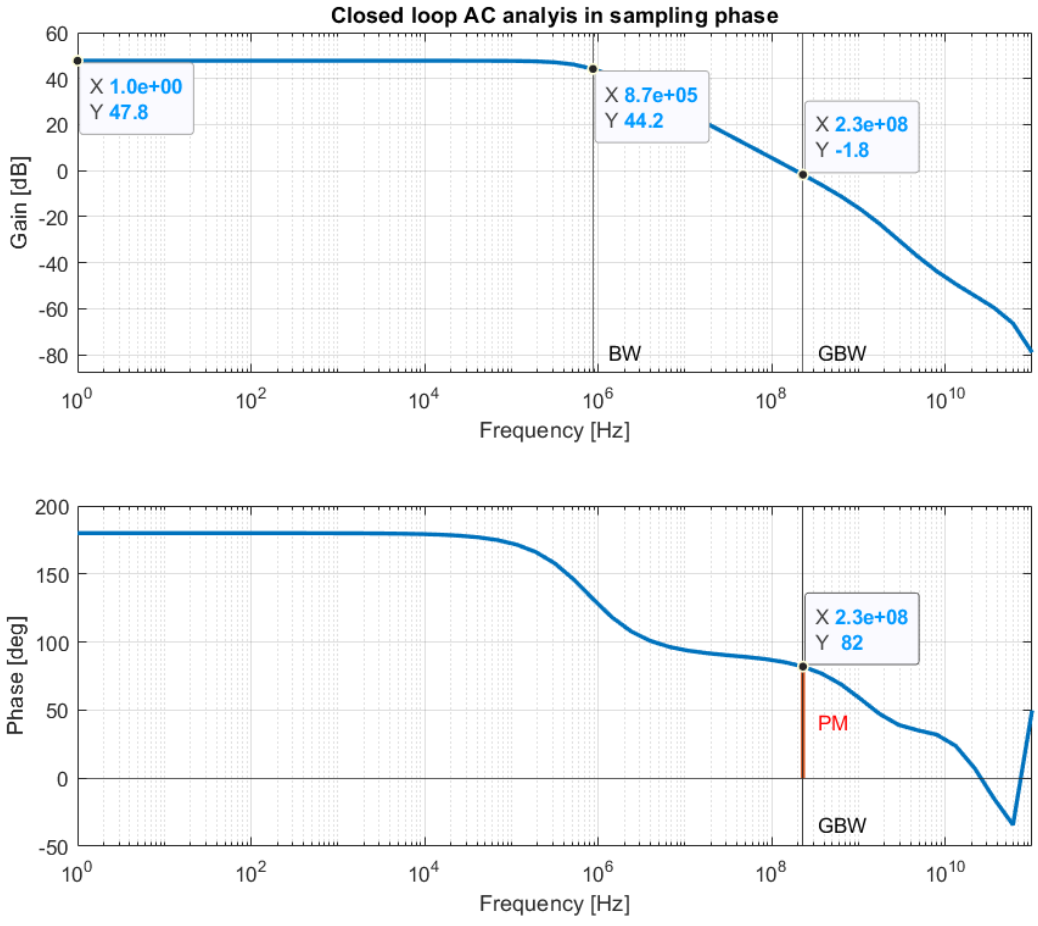


Figure 13 Closed loop amplitude and phase response (sampling phase)

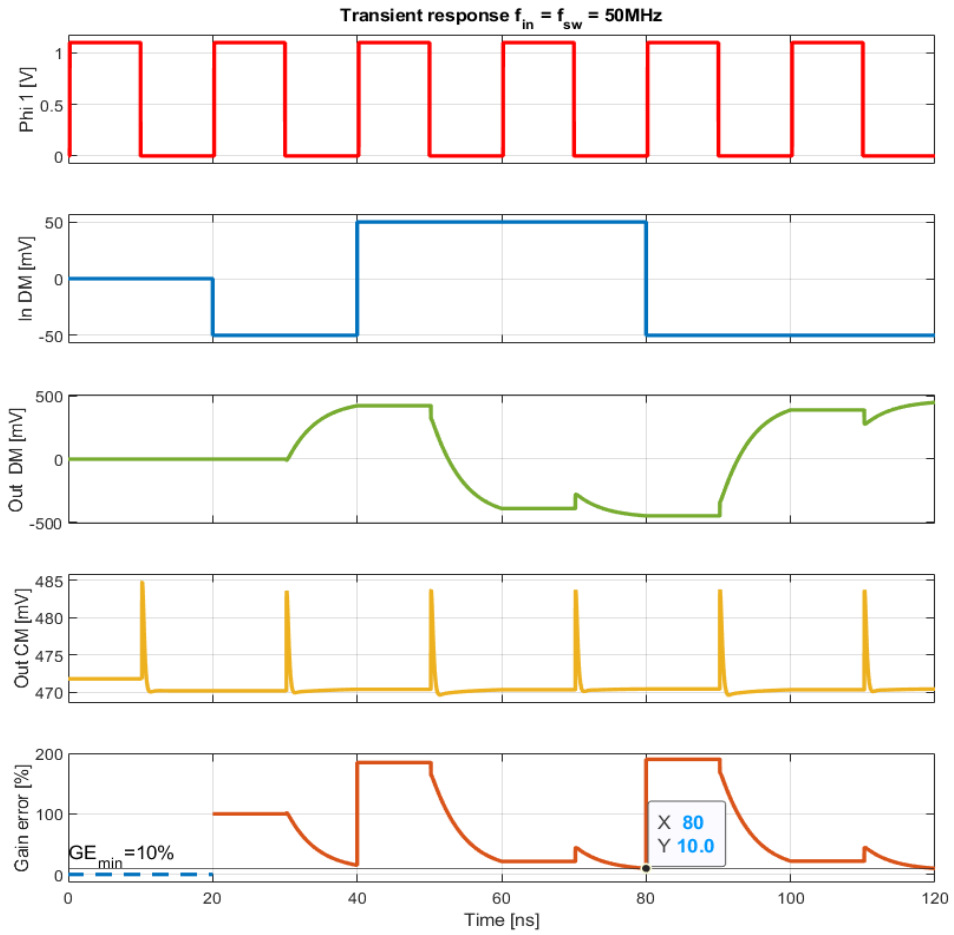


Figure 14 Transient simulation with fsw=fin=50MHz

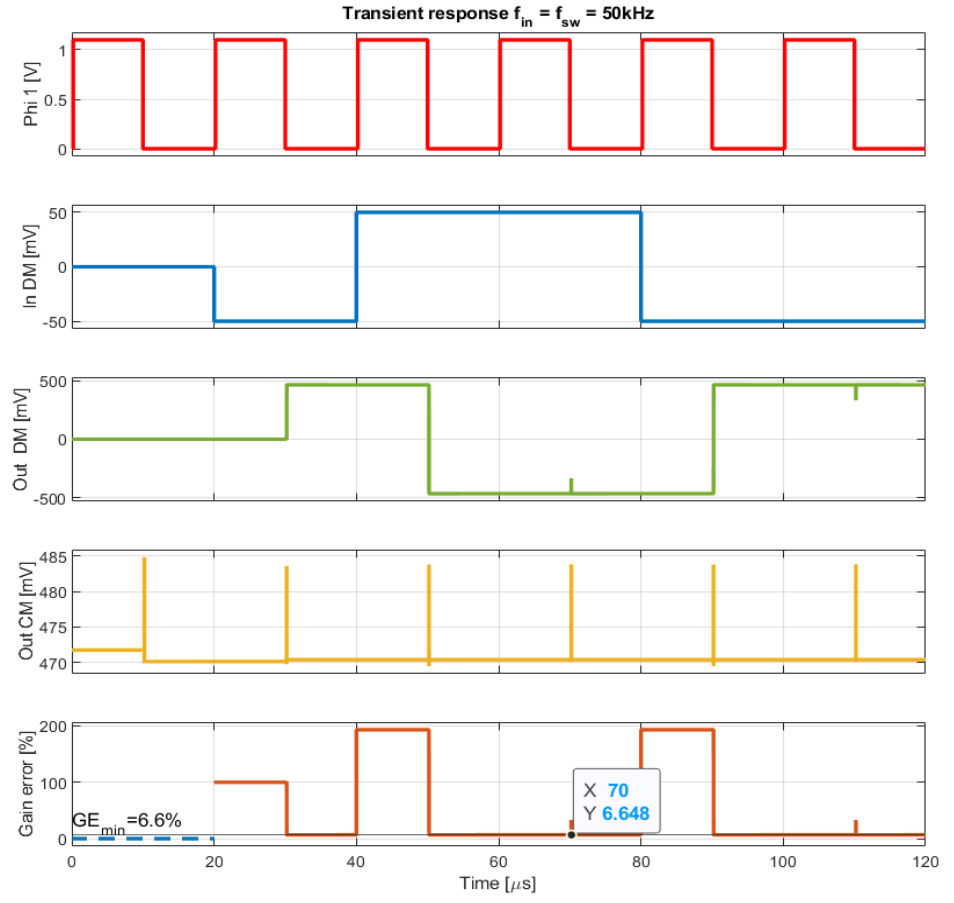


Figure 15 Transient simulation with fsw=fin=50kHz

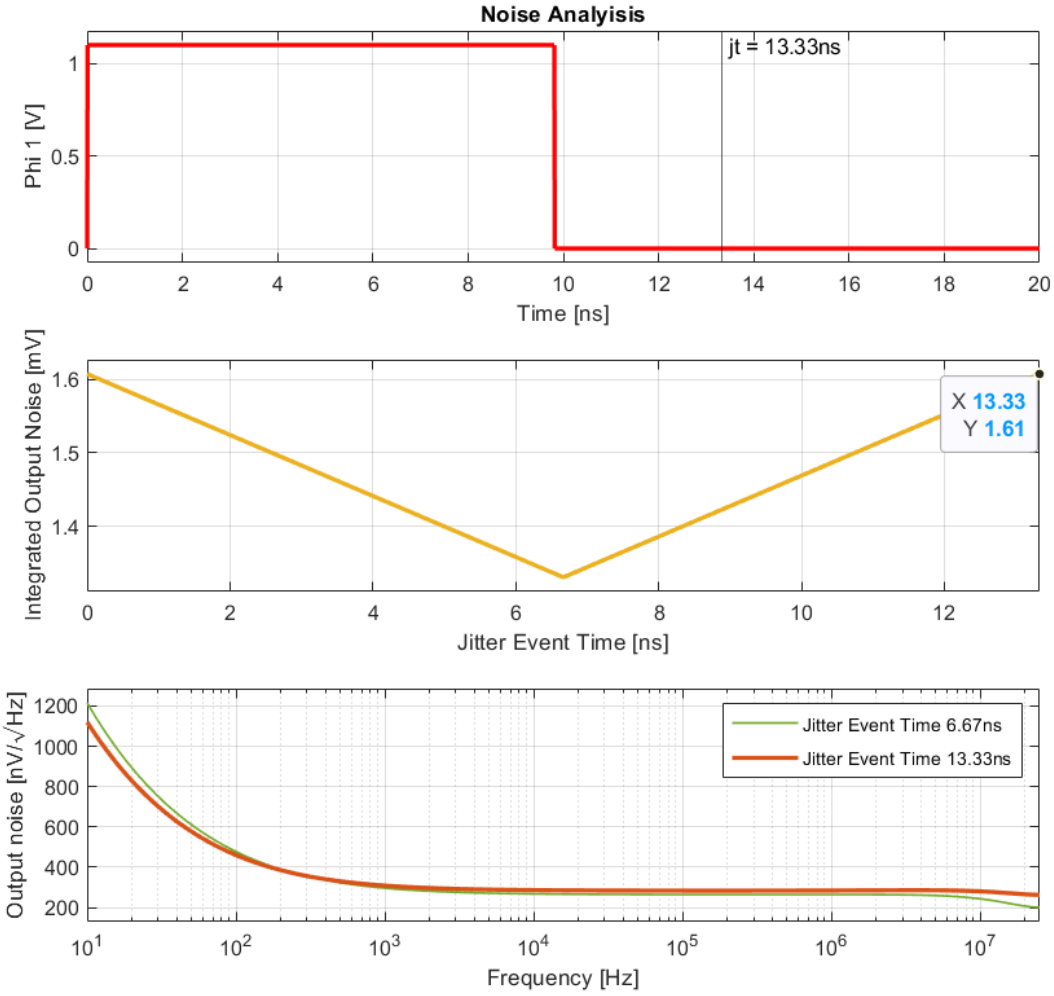


Figure 16 Noise simulation

5 Gain-boosted OTA

5.1 Table of Achieved Results

Parameter	Unit	Achieved
Input Swing	mV_{pp}	**50~100**
Output Swing	mV_{pp}	**499.7~999.2**
Total Integrated Output Noise	mV_{rms}	
SNR	dB	**42.5**
C_L	pF	**2p**
C_{FB}	pF	**0.8**
C_{IN}	pF	**8**
Open-Loop Gain	dB	**91.5**
Closed-Loop Gain	V/V	**9.99**
GBW (Sample Phase)	MHz	**380**
Phase Margin (Sample Phase)	deg	**79**
Dynamic Settling Error	%	**0.7**
Static Gain Error	%	**0.038 (transient sim); 0.84 (PAC sim)**
Power dissipation	mW	**8.31**

5.2 Schematic Design

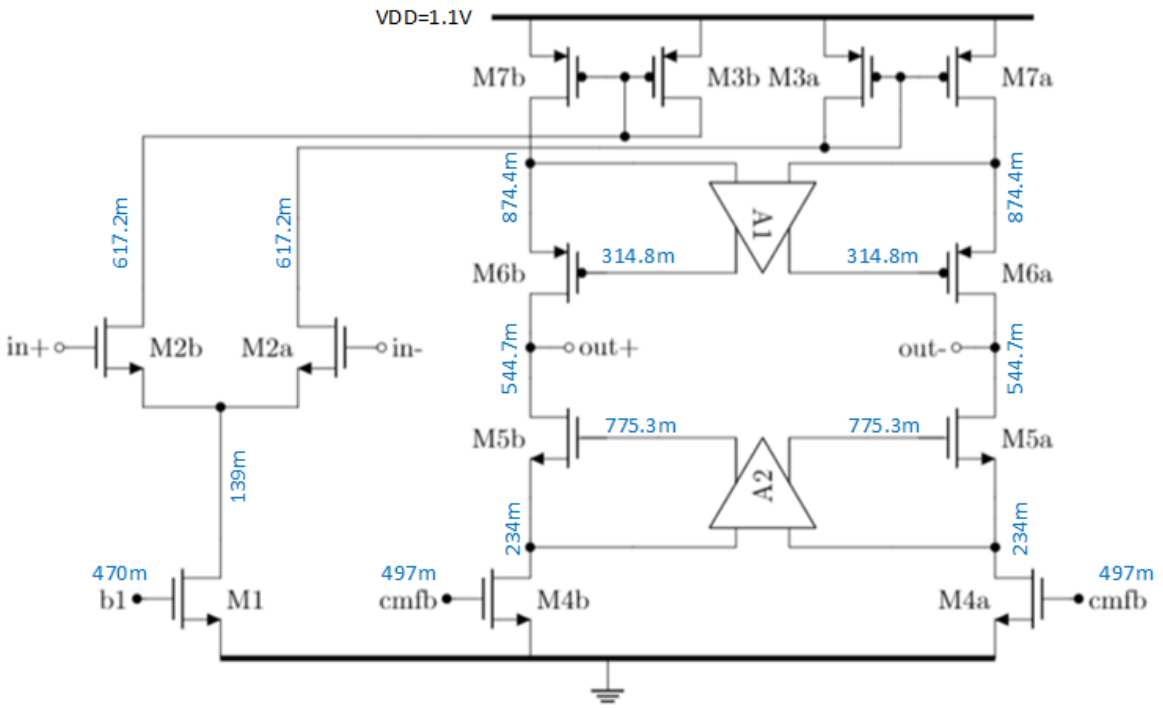


Figure 17 DC Operating point of main OTA

Transistors	Model	Vds[mV]	Vdsat[mV]	gm/Id[S/A]	gm[mS]	Id[mA]
M1	nmos1v	139	116.8	14.3	15.76	1.1
M2	nmos1v_lvt	478.2	61.9	15.1	8.33	0.55
M3	pmos1v_lvt	-452.7	-82.4	13.8	7.59	-0.55
M4	/	235	108	14.8	14.7	11
M5	/	310	102.8	15.17	15	1
M6	pmos1v	-329.7	-98.5	16.3	16.13	-0.99
M7	pmos1v	-225.6	-109.1	17.6	17.4	-0.99

The main OTA is presented with a table due to its size. It is not clearly readable if it is just exported from Cadence.

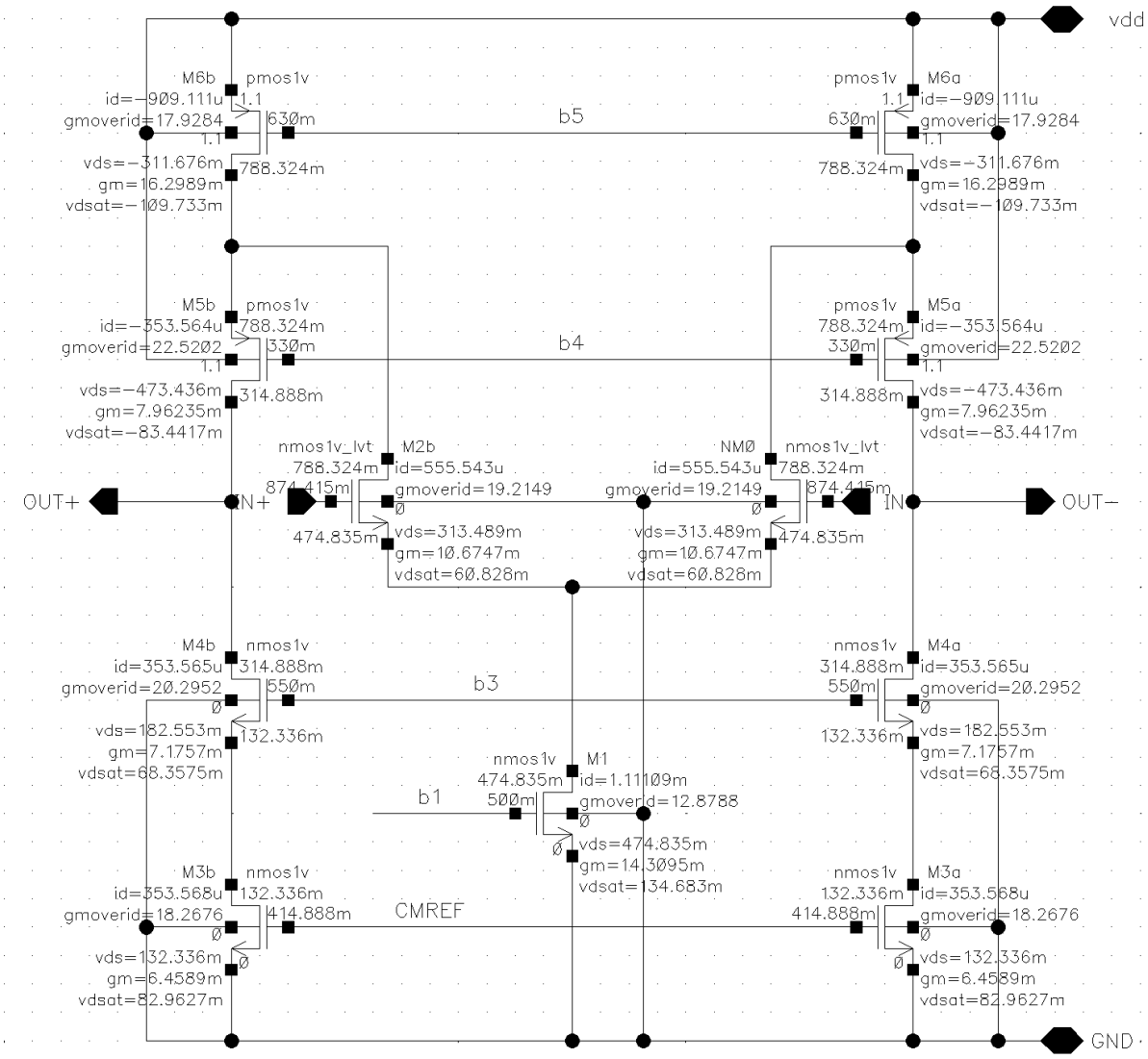


Figure 18 DC Operating point of A1 OTA

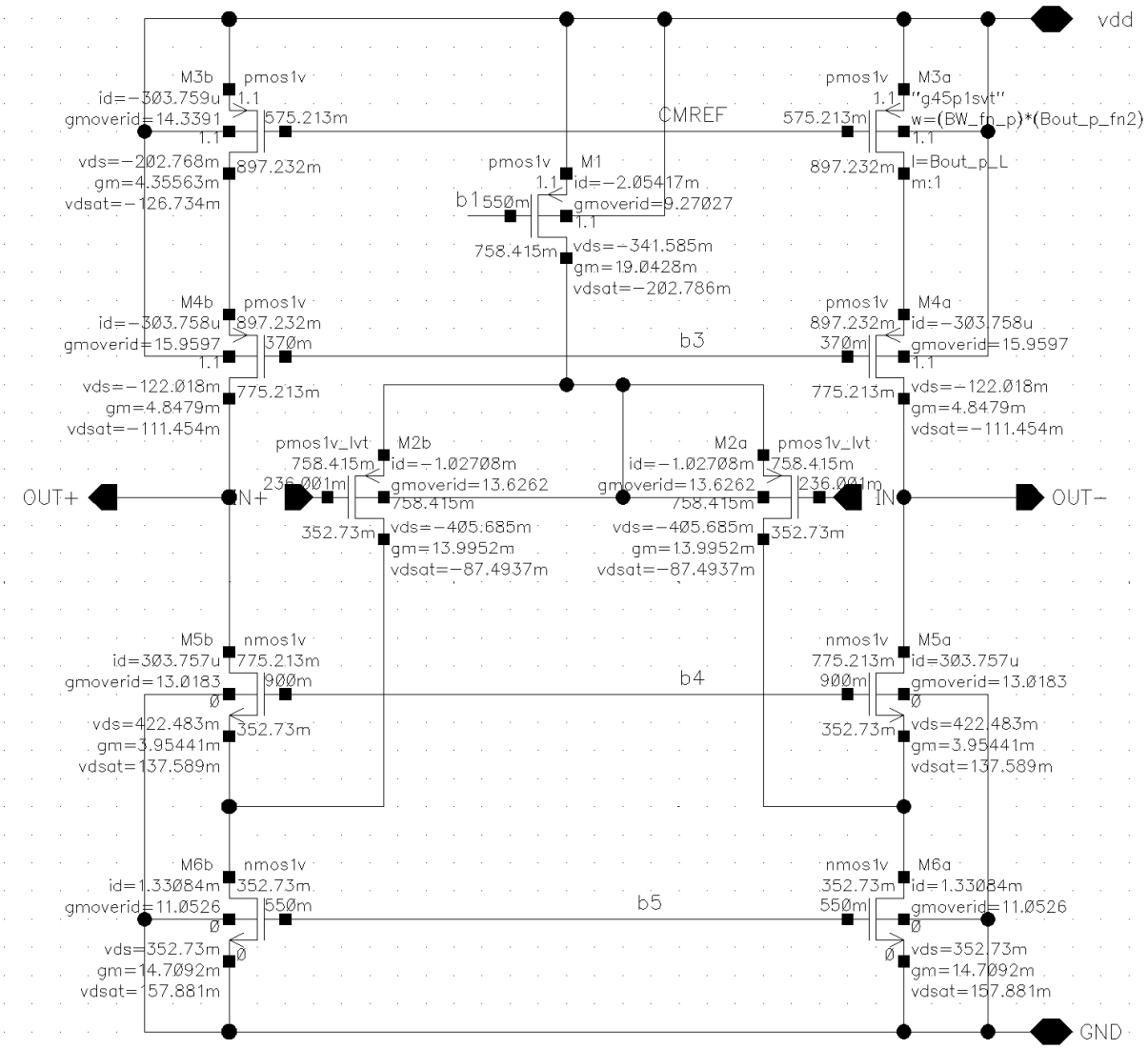


Figure 19 DC Operating point of A2 OTA

Main OTA			
Type	**Name**	**Value**	**Transistor**
Supply	vdd	**1.1**	
Bias	b1	**470m**	
Tail	Finger W	**1.5u**	M1
	Finger #	**420**	
	L	**1.1u**	
Input nMOS (Low Vt)	Finger W	**1.5u**	M2
	Finger #	**53**	
	L	**45n**	
pMOS (Low Vt)	Finger W	**1.5u**	M3
	Finger #	**27**	M3
	L	**45n**	M3
Output nMOS	Finger W	**1.5u**	M4/M5
	Finger #	**100**	M5
	L	**215n**	
	Finger #	**133**	M4
	L	**340n**	
Output pMOS	Finger W	**1.5u**	M5/M6
	Finger #	**100**	M5
	L	**110n**	
	Finger #	**200**	M6
	L	**300n**	
CMFB	Gain	**10**	
	R	**10**	
	CMFB SP	**550m**	

Gain Boosting nMOS input OTA – A1			
Type	**Name**	**Value**	**Transistor**
Supply	vdd	**1.1**	
Bias	b1	**500m**	
	b3	**550m**	
	b4	**330m**	
	b5	**630m**	
Tail	Finger W	**1.5u**	M1
	Finger #	**144**	
	L	**600n**	
Input (Low Vt)	Finger W	**1.5u**	M2
	Finger #	**192**	
	L	**90n**	
Output nMOS	Finger W	**2u**	M3/M4
	Finger #	**200**	M4
	L	**450n**	
	Finger #	**200**	M3
	L	**450n**	
Output pMOS	Finger W	**1.5u**	M5/M6
	Finger #	**233**	M5
	L	**390n**	
	Finger #	**233**	M6
	L	**450n**	
CMFB	Gain	**1**	
	R	**10**	
	CMFB SP	**315m**	

Gain Boosting pMOS input OTA – A2			
Type	**Name**	**Value**	**Transistor**
Supply	vdd	**1.1**	
Bias	b1	**550m**	
	b3	**370m**	
	b4	**900m**	
	b5	**550m**	
Tail	Finger W	**1.5u**	M1
	Finger #	**300**	
	L	**1u**	
Input (Low Vt)	Finger W	**1.5u**	M2
	Finger #	**50**	
	L	**45n**	
Output nMOS	Finger W	**1.5u**	M5/M6
	Finger #	**40**	M5
	L	**600n**	
	Finger #	**60**	M6
	L	**400n**	
Output pMOS	Finger W	**1.5u**	M3/M4
	Finger #	**30**	M4
	L	**200n**	
	Finger #	**50**	M3
	L	**200n**	
CMFB	Gain	**1**	
	R	**10**	
	CMFB SP	**775m**	

Derivation

5.3 Simulation Results

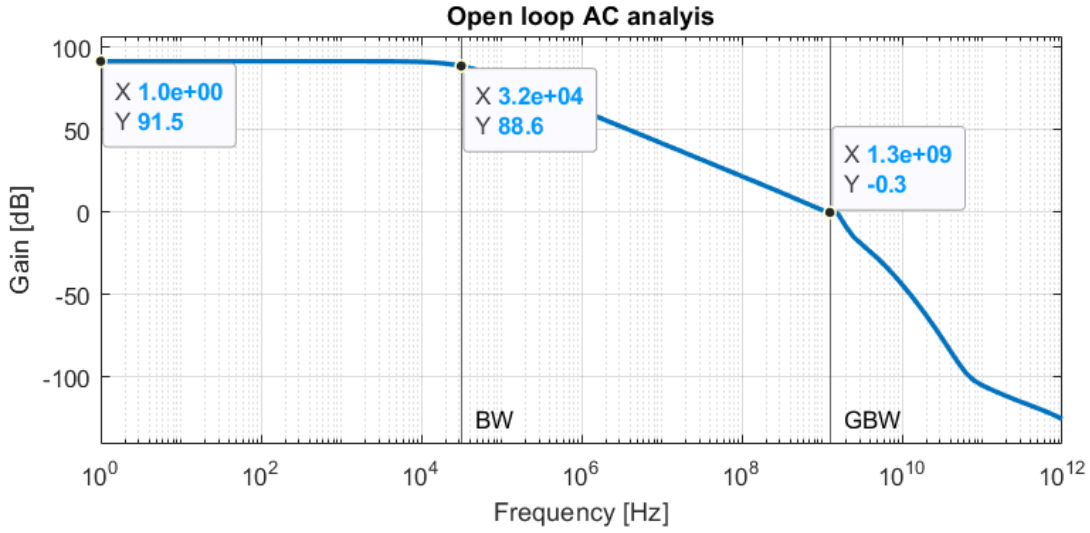


Figure 20 Open loop amplitude response

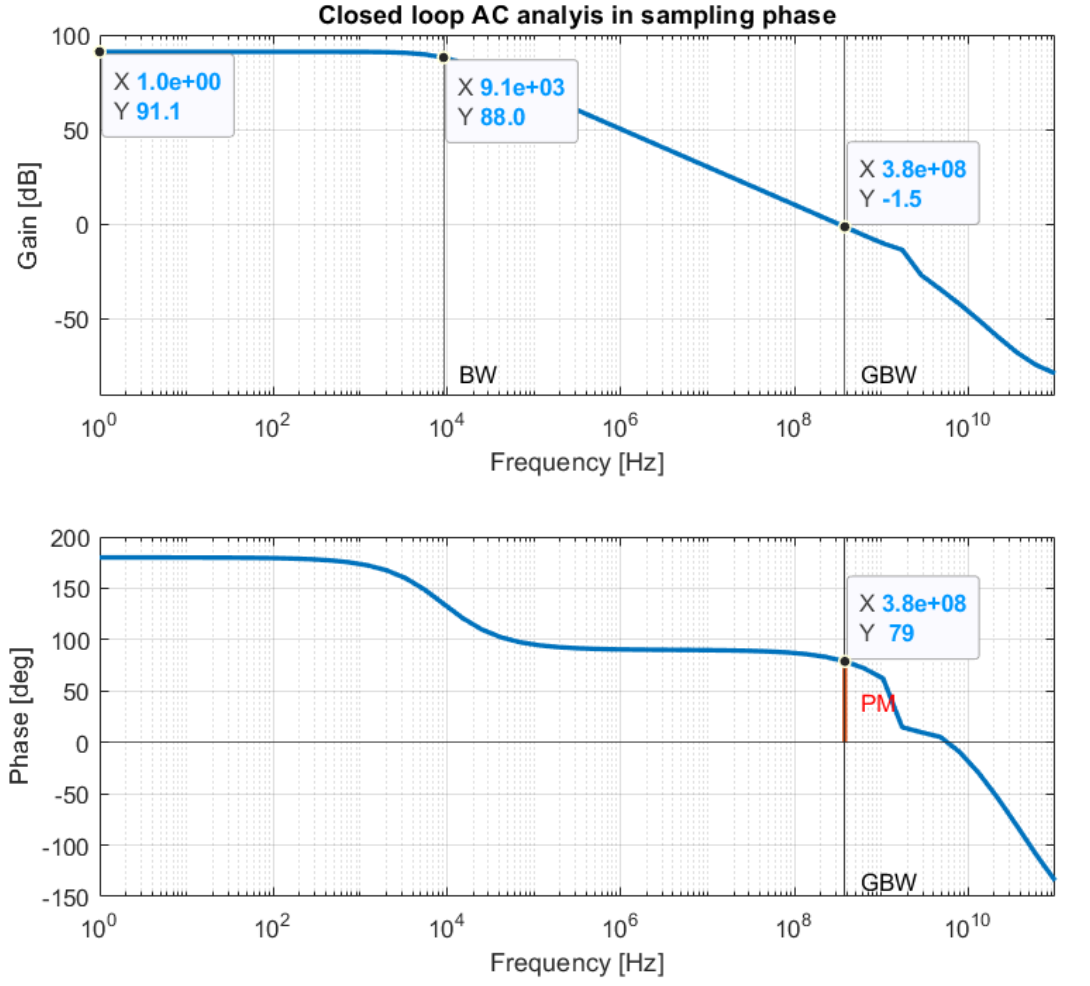


Figure 21 Closed loop amplitude and phase response (sampling phase) - differential loop

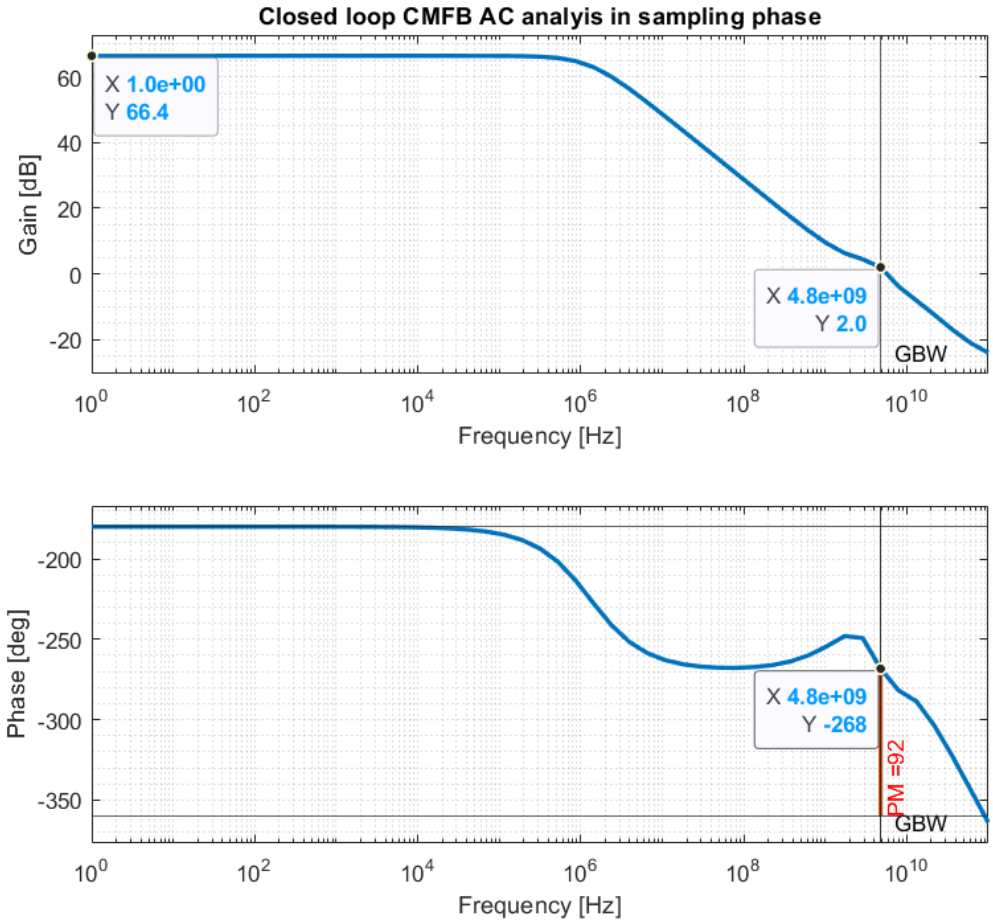


Figure 22 Closed loop amplitude and phase response (sampling phase) – CMFB loop

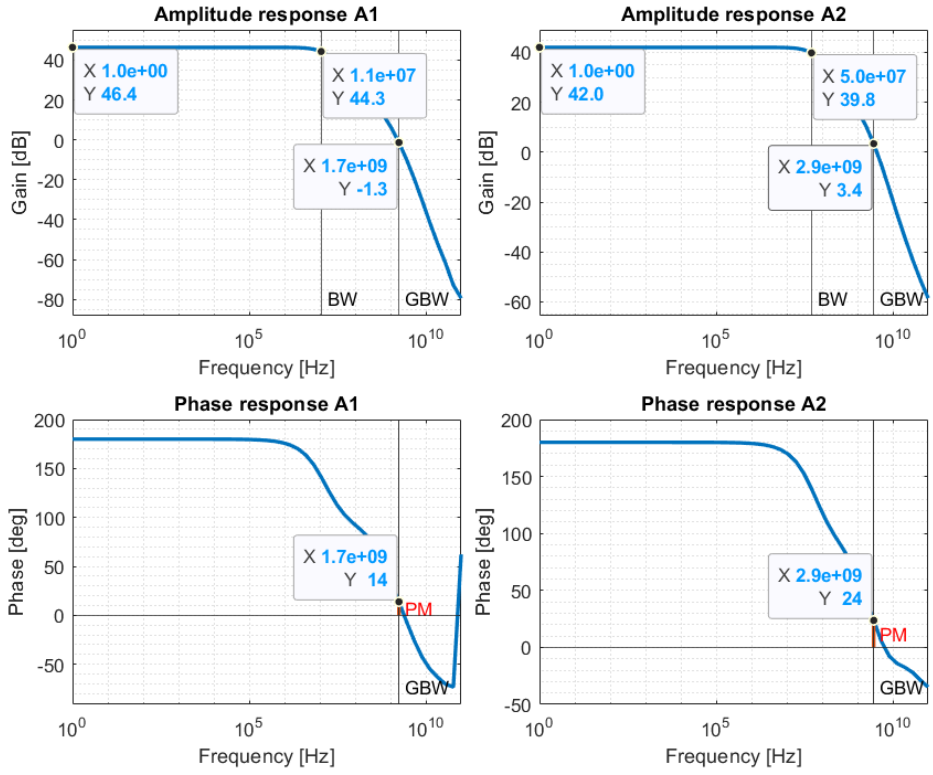


Figure 23 Closed loop amplitude and phase response A1 and A2

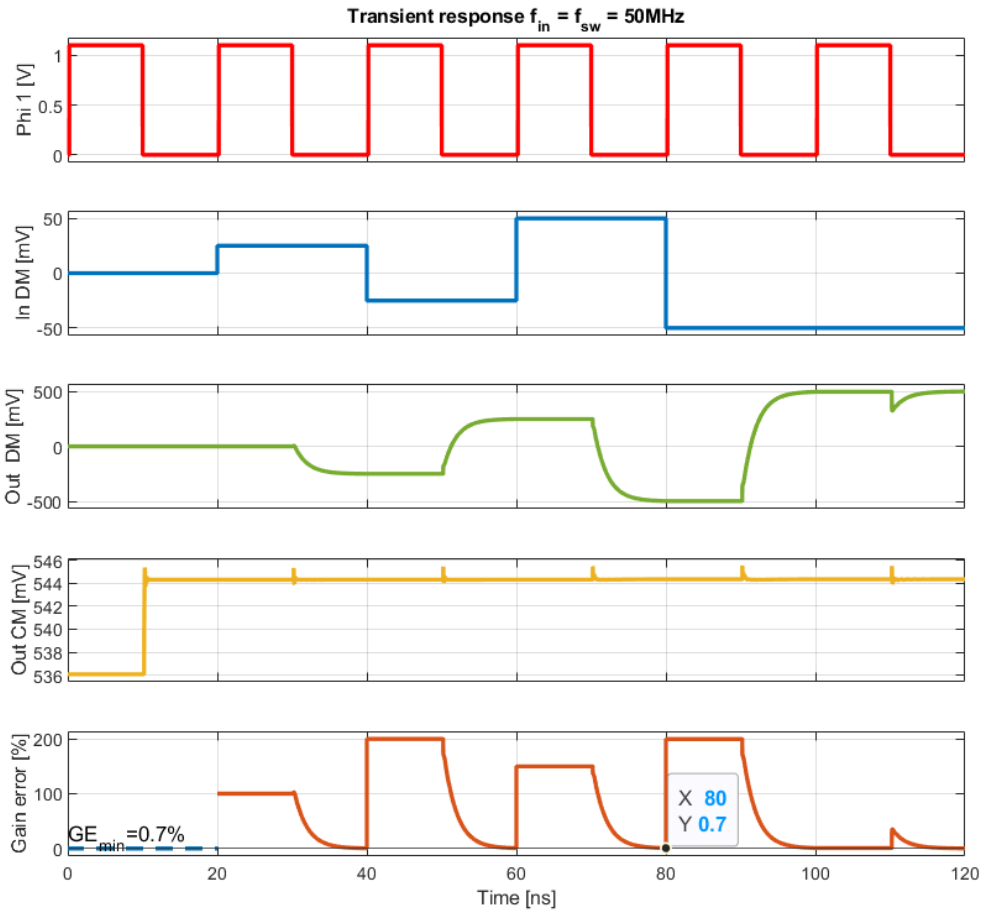


Figure 24 Transient simulation with fsw=fin=50MHz

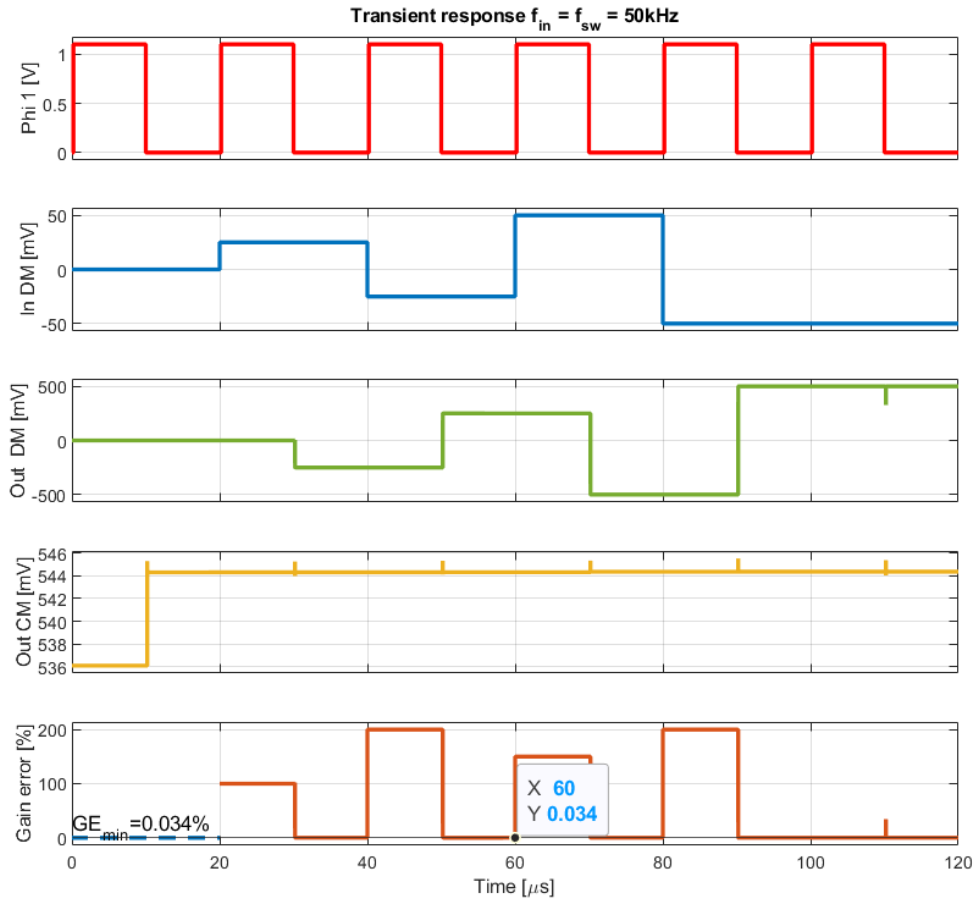


Figure 25 Transient simulation with fsw=fin=50kHz

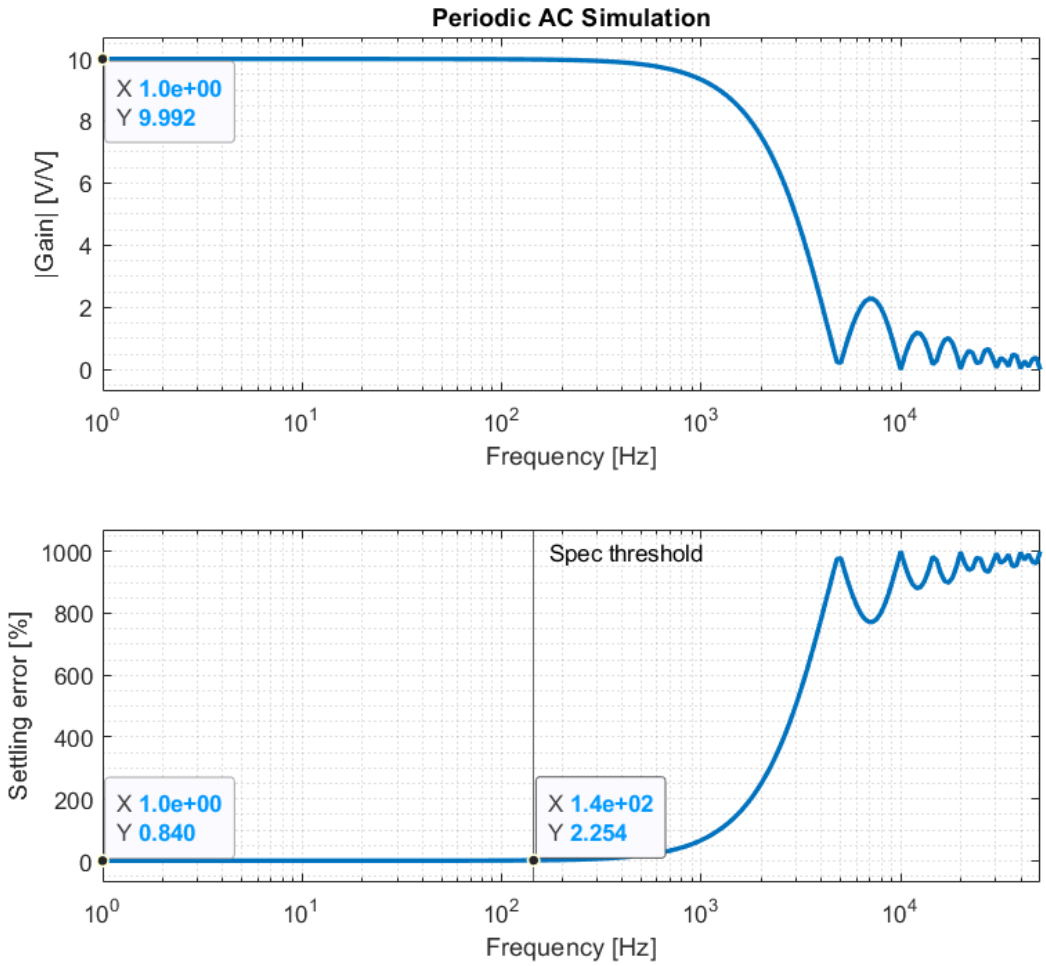


Figure 26 Closed loopo PAC simulation

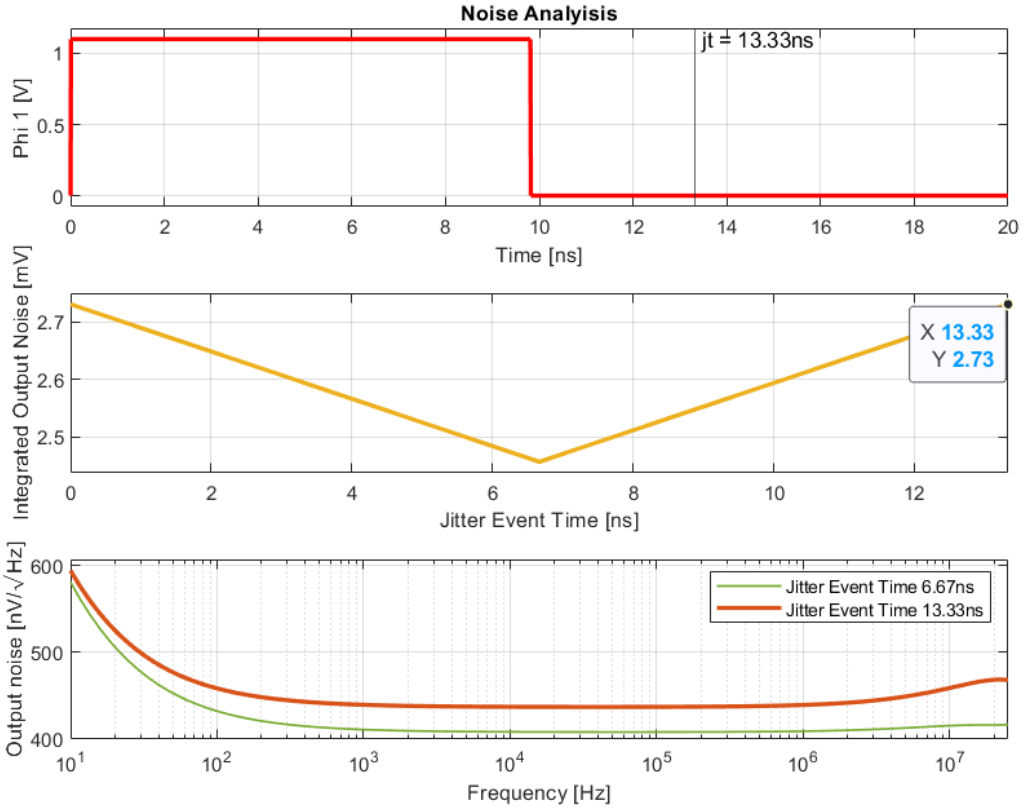


Figure 27 Noise simulation

6 Summary and Additional Remarks

Specifications

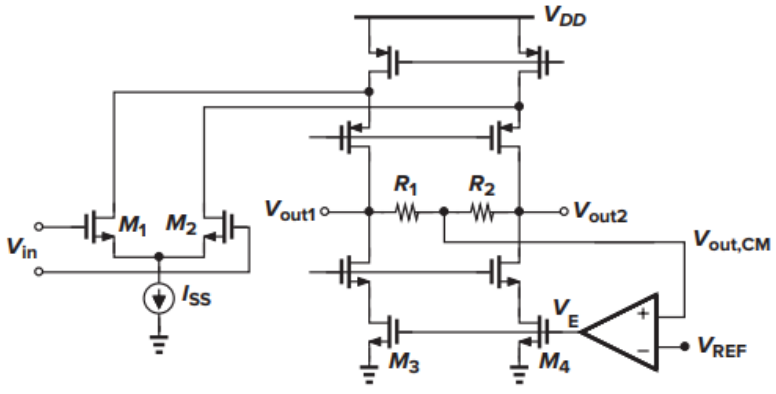
- We managed to reach all of the given specifications except the SNR that is 2.5dB less than required. We were **able to meet all the specifications** when using voltage sources to adjust the CM output of the gain boosting amplifiers. Our dynamic settling error (0.7%) is significantly better than the specification (2.2%). According to the PAC simulation we do not meet the static gain error specification but do in the transient simulation.

Plotting and specification extraction

- We wrote a script in Matlab that takes in CSV data from Cadence, analyses it and plots the results. It automatically adjusts the axis scales, calculates important points such as the BW, GBW, phase margin and dynamically labels them on the plots in a clear and readable way. This eliminates the time-consuming task of the user having to manually place points on the graph and makes the graphs and the important points easier to read.

7 Other Results

- We attempted to make a real CMFB block instead of using the ideal one that was provided to us. We managed to implement the following topology by making a separate simple OTA that would be used as a comparator in the feedback loop. This gave stable and good results when used only on the folded cascode OTA but was very unstable in the gain boosting implementation due to too much gain.



- An obvious downside of this implementation are the two sensing resistors that cause many problems. We had panned to replace them with a better CM sensing circuit later on.