BRAC UNIVERSITY

Department of Electrical and Electronic Engineering

CSE350: Digital Electronics and Pulse Techniques

Experiment No: 2

Implementing a DTL logic gate

Objective

1. Construct a DTL logic gate.
2. Understand the circuit operation.

Equipments:

1. Oscilloscope
2. Digital Trainer Board
3. Digital Multimeter
3. DC power supply

Component:

- NPN Transistor: C828 1pieces
- Diode 1N4003 4+pieces
- Resistors

2K 2 pieces

20K 1 piece

Circuit Diagram

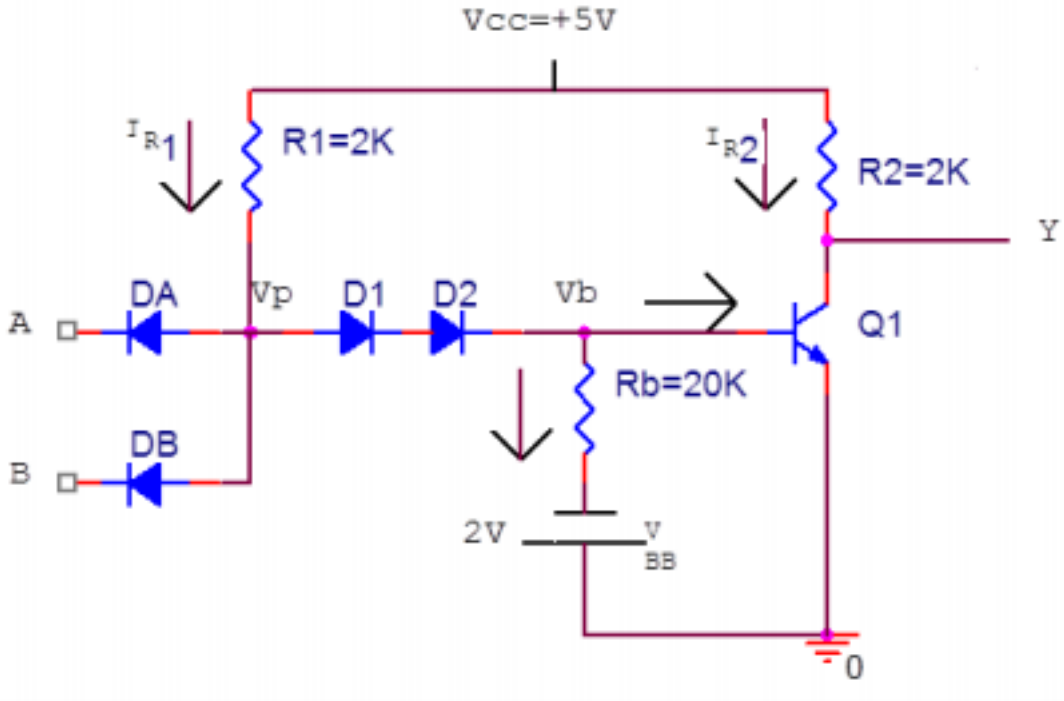
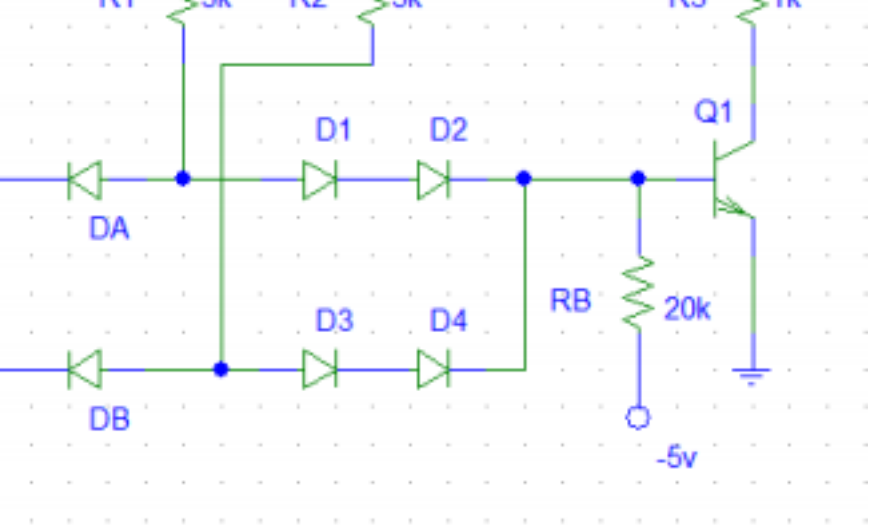


Fig: 1



Vp

Fig : 2

Laboratory tasks

1. Connect the circuit as shown in Fig: 1 and Fig: 2
2. Observe the output for all possible inputs and determine the type of gate.
3. Fill up the following table.

Input A	Input B	V_{DA}	V_{DB}	V_P	I_{R1}	Ir2	Vb	Output Y
0	0							
0	1							
1	0							
1	1							

In both cases compare the values with the theoretical values.

4. Operate the gate in Fig 1 as an inverter by connecting either of the inputs to +5V and using the remaining one as input terminal. Fill up the following table.

Input A	Input B	V_P	Vb	Output Y
1	0			
1	1			

Report

1. Assume that Logic low has been applied to both inputs of the circuit shown in Fig: 1, draw the partial circuit consisting of only those components which remain active.

2. Explain briefly how NAND operation is performed in the circuit. 3. Using proteus data show that Q1 will be in saturation when both inputs are high. 4. What is the maximum value of inputs A,B to keep the output high? (use simulation data)

Reference

Reference: Microelectronics: Digital and Analog Circuits and Systems by Jacob Millman, Page- 140-145