
## CSE350, LAB02

**Submitted by:**
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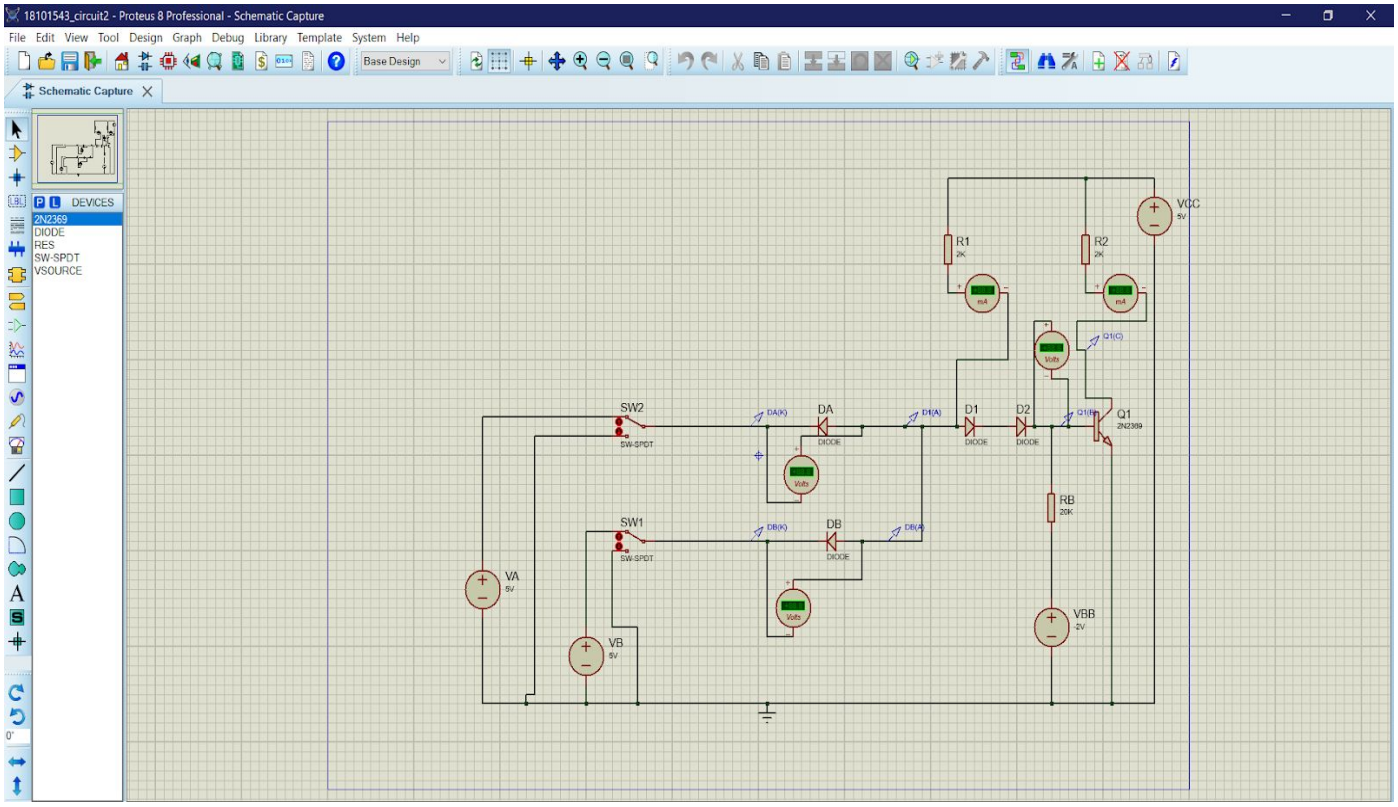
Section: 04.

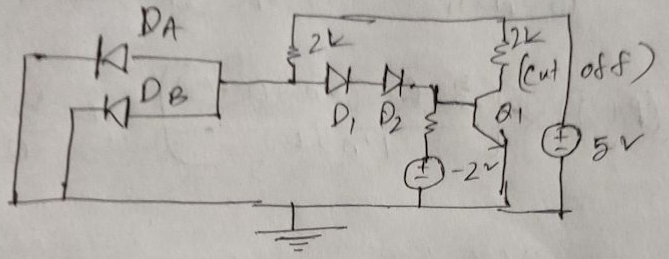
| Input A | Input B | V(DA) | V(DB) | V(P) | I(R1) | I(R2) | V(b) | Output Y |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | +0.66 | 0.66 | 0.65 | 2.17 | 0 | 0.51 | 5 |
| 0 | 1 | +0.67 | -4.33 | 0.67 | 2.16 | 0 | 0.50 | 5 |
| 1 | 0 | -4.33 | 0.67 | 0.67 | 2.16 | 0 | 0.50 | 5 |
| 1 | 1 | -2.86 | -2.86 | 2.13 | 1.43 | 2.45 | 0.811 | 0.09 |

| Input A | Input B | Vp | Vb | Output Y |
|---|---|---|---|---|
| 1 | 0 | 0.67 | 0.50 | 5 |
| 1 | 1 | 2.13 | 0.811 | 0.09 |


18101543_circuit2 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
2N2369
DIODE
RES
SW-SPDT
VSOURCE
VCC
5V
R1
2K
R2
2K
SW2
SW-SPDT
DA
DIODE
D1
DIODE
D2
DIODE
Q1
2N2369
RB
20K
SW1
SW-SPDT
DB
DIODE
VA
6V
VB
6V
VBB
-2V
Volts

CSE 350
LAB 02

## Ans. to the Ques. no.:-01




## Ans. to the ques. no.:-02

NAND is made with AND gate and NOT gate. Here, output are inverse of AND gate. when inputs are logical non the output becomes high or logical "1". that time DA and DB turn on.

When any of the input is logical "0" that time also the circuit will cause the transistor to go in cutoff region as the voltage of vp will be very low. ~~so, no current passed through collector~~

when the both inputs are high or in logical "1" mode that time vp increase and causes the diodes to turn off. for that reason, the voltage is enough to turn on the transistors and Ve becomes almost 0v which can be considered as logical "0"

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## Ans. to the Ques. no. 3-03

From ~~pro~~ proteus data we can see that when both inputs are high $V_b$ is 0.811 V and output voltage is 0.09 V.

So, we can see base voltage is almost 0.8 V and collector voltage is almost 0.1 V which are characteristics of saturation mode.

Hence, $I_{R2} = 2.45 > 0$, $I_{R1} = 1.43 > 0$

## Ans. to the Ques. no. 3-04

By using proteus we can see that maximum voltage 1V as inputs of A, B can keep the output high as it gives 4.99 V $\simeq$ 5 V in output.

# The End