CSE350, LAB04

Submitted by:
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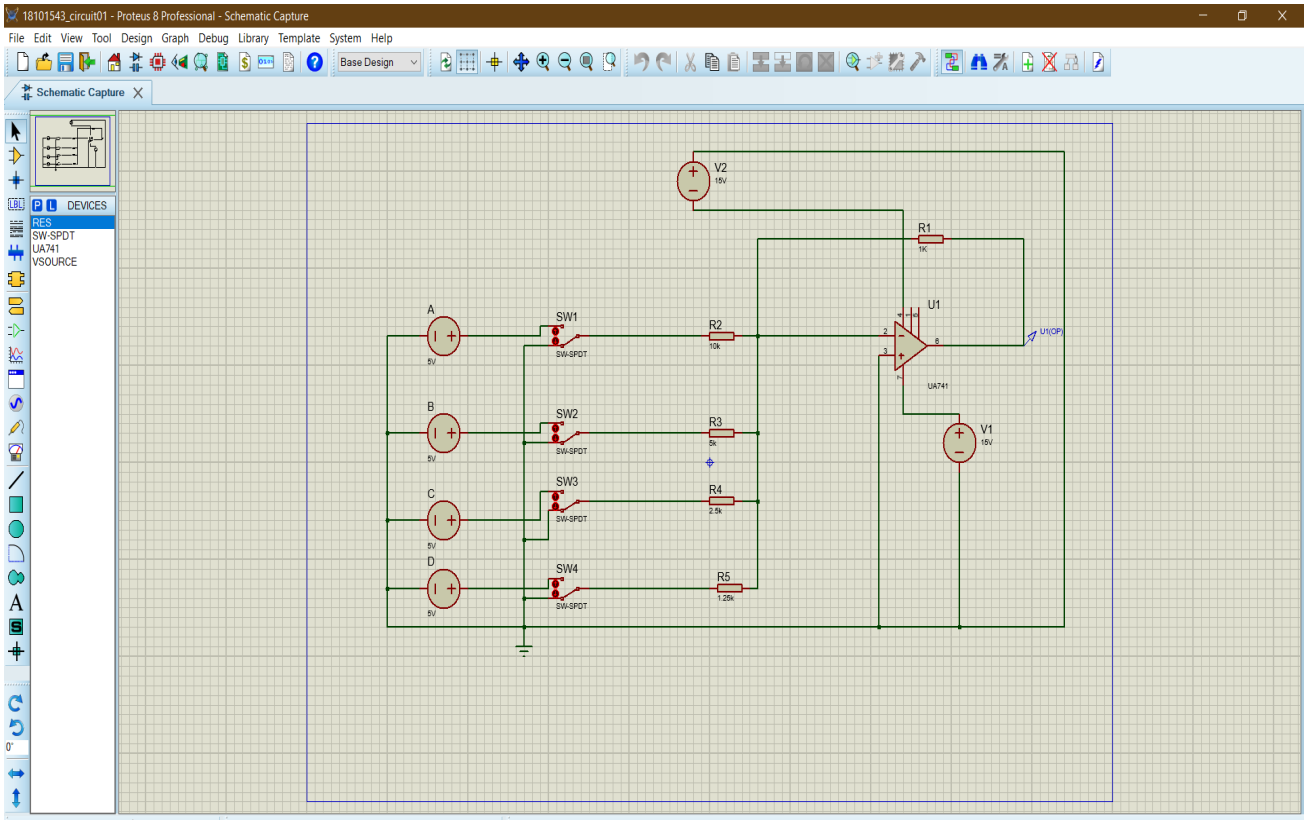
Id:18101543
Section: 04.

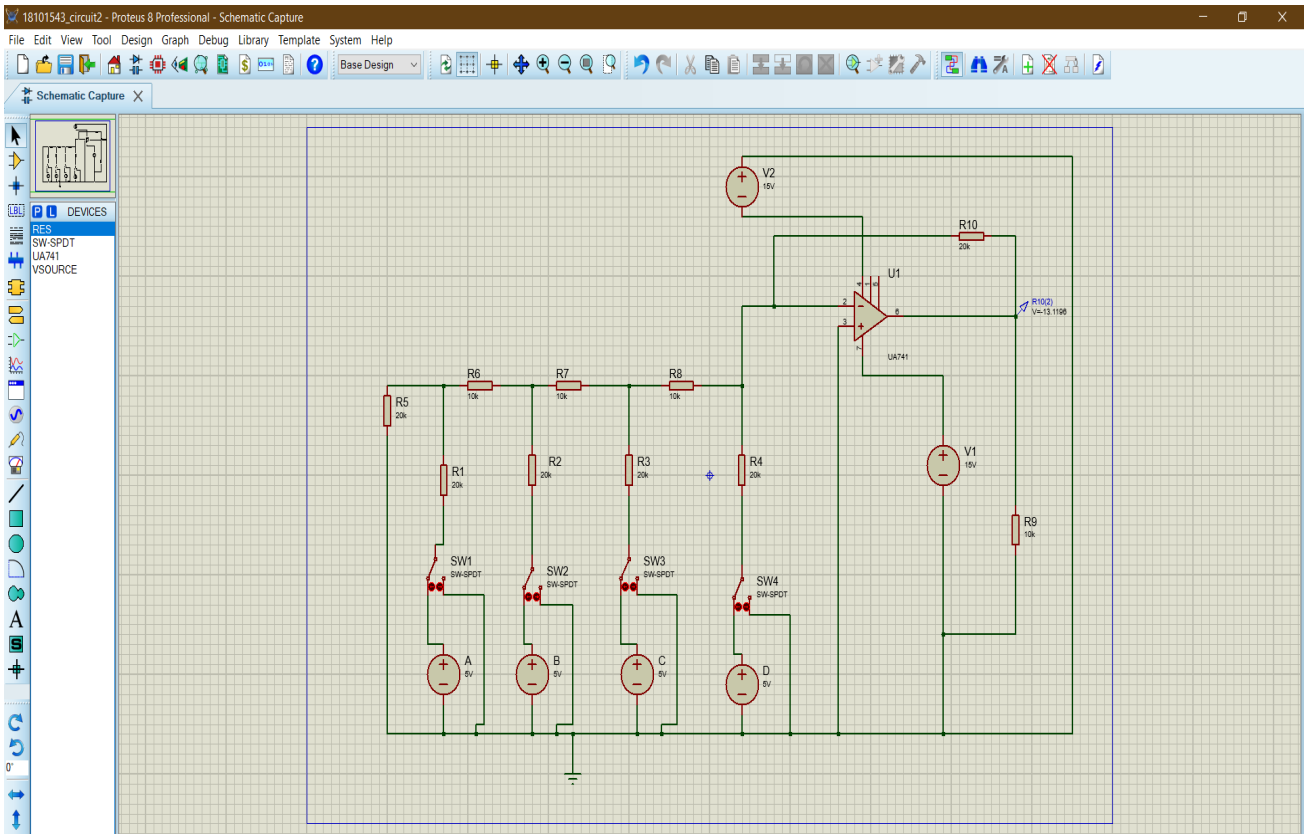
Datasheet for circuit 1:

Configuration	D	C	B	A	Output Voltage, Vo (V)
1	0	0	0	0	-0.0027
2	0	0	0	5	-0.49
3	0	0	5	0	-0.99
4	0	0	5	5	-1.49
5	0	5	0	0	-1.99
6	0	5	0	5	-2.49
7	0	5	5	0	-2.99
8	0	5	5	5	-3.49
9	5	0	0	0	-3.99
10	5	0	0	5	-4.49
11	5	0	5	0	-4.99
12	5	0	5	5	-5.49
13	5	5	0	0	-5.99
14	5	5	0	5	-6.49
15	5	5	5	0	-3.49
16	5	5	5	5	-7.49


18101543_circuit01 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
V2
15V
R1
1K
U1
UA741
U1(OP)
A
5V
SW1
SW-SPDT
R2
10k
B
5V
SW2
SW-SPDT
R3
5k
C
5V
SW3
SW-SPDT
R4
2.5k
D
5V
SW4
SW-SPDT
R5
1.25k
V1
15V

Datasheet for circuit 2:

Configuration	D	C	B	A	Output Voltage, Vo (V)
1	0	0	0	0	0.0049
2	0	0	0	5	-0.62
3	0	0	5	0	-1.245
4	0	0	5	5	-1.869
5	0	5	0	0	-2.49
6	0	5	0	5	-3.11
7	0	5	5	0	-3.74
8	0	5	5	5	-4.36
9	5	0	0	0	-4.99
10	5	0	0	5	-5.81
11	5	0	5	0	-6.24
12	5	0	5	5	-6.86
13	5	5	0	0	-7.49
14	5	5	0	5	-8.11
15	5	5	5	0	-8.74
16	5	5	5	5	-9.36


18101543_circuit2 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
V2
15V
R10
20k
U1
UA741
R102)
V=-13.1196
R6
10k
R7
10k
R8
10k
R5
20k
R1
20k
R2
20k
R3
20k
R4
20k
V1
15V
R9
10k
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT
SW4
SW-SPDT
A
5V
B
5V
C
5V
D
5V

Ans. to the Ques. no. :-02

Here full step size of the circuit is 1v. We get this by plotting the values in a graph by plotting the values in a graph for both the circuits.

Ans. to the Ques. no. :-03

Resolution is 1V for the LSB of the 4 bit option.

Ans. to the ques. no. :- 04

Here, my id is = 18101543. So, sum of last 2 digits is (4+3) = 7. So, high input is 7. So, from circuit 2 by using 7v as high input we get these outputs:-

Input configuration	D	C	B	A	output voltage, V_0(V)
1	0	0	0	0	0.0049
2	0	0	0	7	-0.87
3	0	0	7	0	-1.74
4	0	0	7	7	-2.61
5	0	7	0	0	-3.49
6	0	7	0	7	-4.36
7	0	7	7	0	-5.24
8	0	7	7	7	-6.11
9	7	0	0	0	-6.99
10	7	0	0	7	-7.86
11	7	0	7	0	-8.74
12	7	0	7	7	-9.61
13	7	7	0	0	-10.49
14	7	7	0	7	-11.36
15	7	7	7	0	-12.24
16	7	7	7	7	-13.11

Ans. to the Ques. no. 8- (b)

For the 1st circuit the output is a staircase waveform and each step being roughly -0.5 V each. The output current is $a V_{BF}$. So, when the V_{BF} is increased or decreased ~~V_{BF} dies~~ the step size and full size output will change proportionally.

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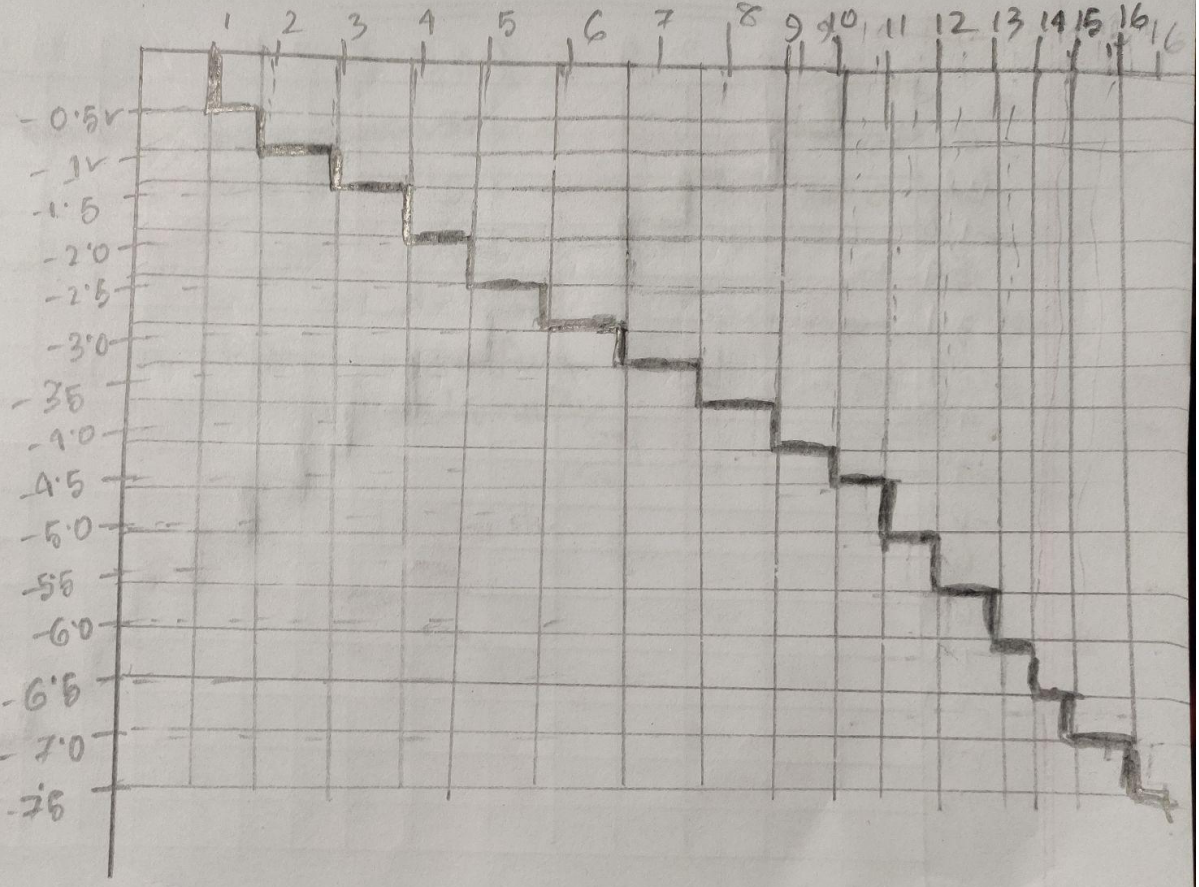
firaph for circuit 1



Graph for circuit 2: