CSE350, LAB01

Submitted by:
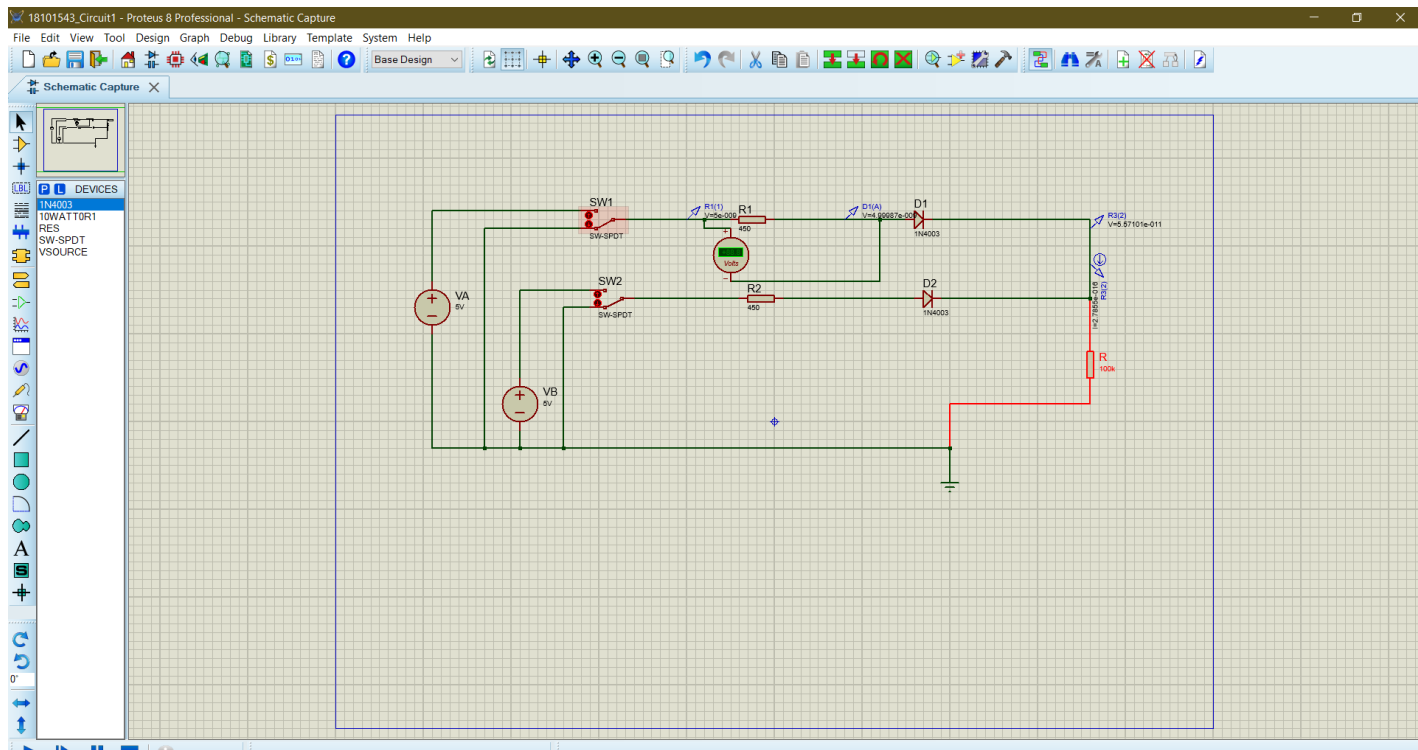Simon Biswas,
Id:18101543
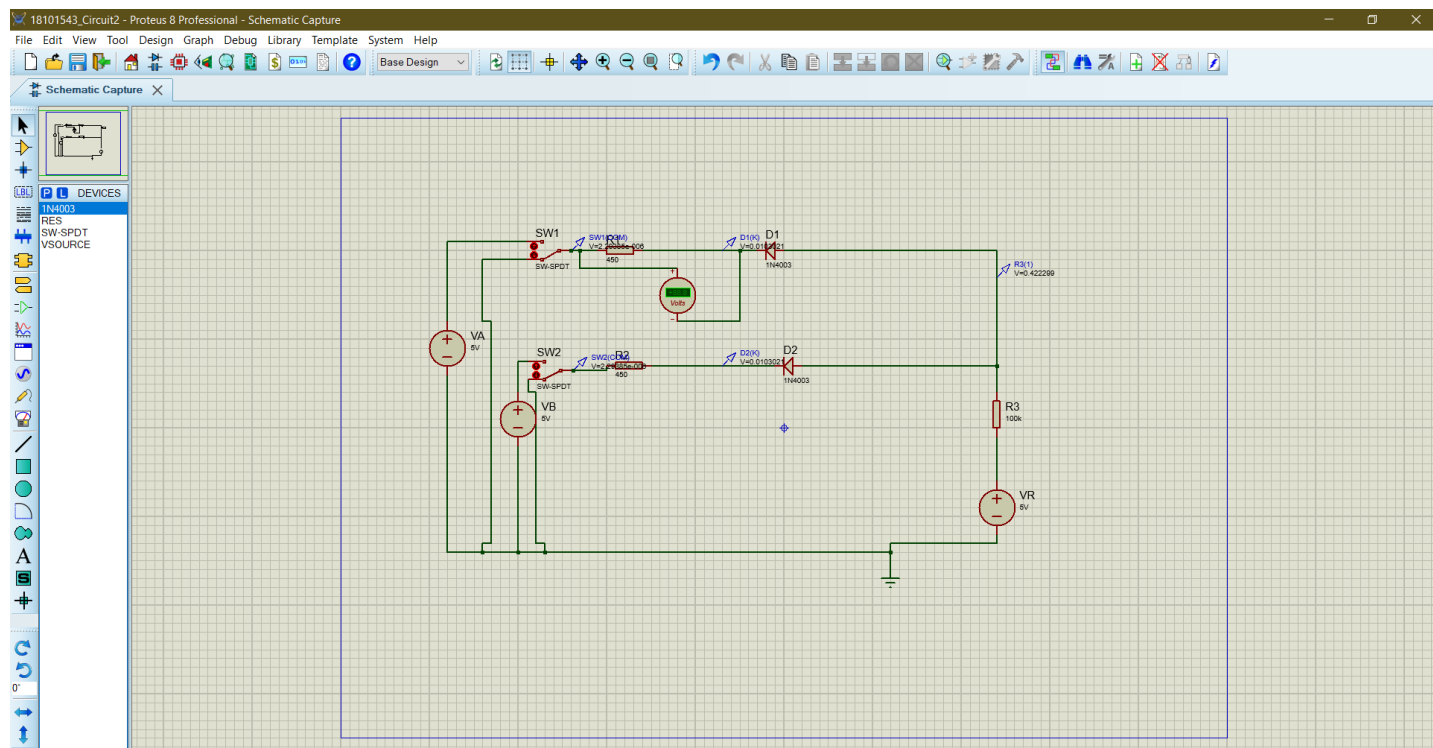Section: 04.

OR Gate(Figure 01) :

VA	VB	VR1	VR2	IR1	IR2	VR=Y
5	5	0.01	0.01	0.000022	0.000022	4.57
0	5	0.00	0.02	0	0.000044	4.536
5	0	0.02	0.00	0.000044	0	4.536
0	0	0.00	0.00	0	0	5.57101e-011/0.00

AND Gate(Figure 02):

VA	VB	VR1	VR2	IR1	IR2	VR=Y
5	5	0.00	0.00	0.00	0.00	5
0	5	0.02	0.00	0.000044	0.00	0.463
5	0	0.00	0.02	0.00	0.000044	0.463
0	0	0.01	0.01	0.000022	0.000022	0.42229

Inverter(Figure 03):

Vi	VR1	VR2	VRC	I1	I2	IB	IC	Y
5	4.30	5.70	4.89	0.28	0.05	0.23	2.22	0.108118
0	0.65	4.35	0	0.04	0.04	0.0	0	5
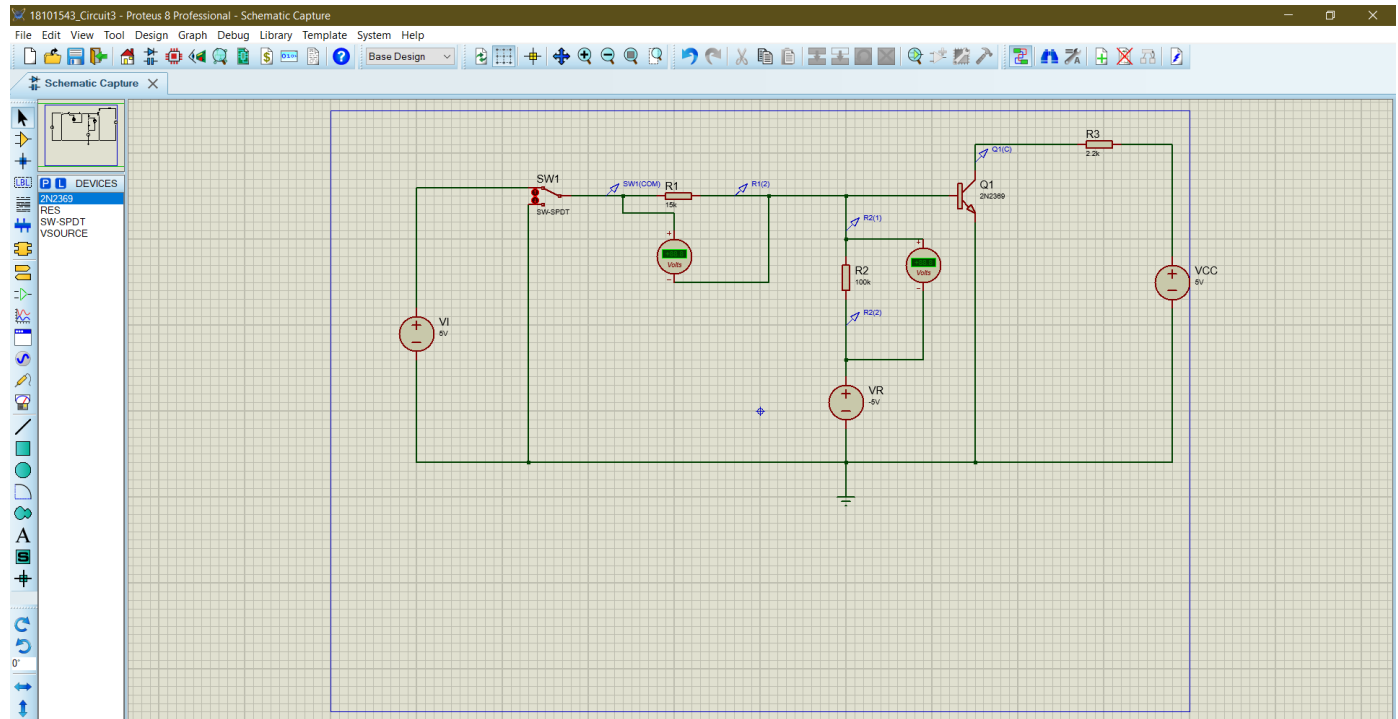
① What happens if not all inputs have the same uppor levels?

⇒ fore OR gate: when all the inputs are in lower level the ouput becomes 0. If one or more inputs are in high level then output becomes 1.

fore AND gate: If all the inputs are in lower level output becomes 0. If any of the input is in lower level, output will be 0. But if all the inputs have are in high level then output will be 1.

② Will the diode D_1 and D_2 will work, if $V_A = V_B = 6V$ and $V_R = 5 V_0$

⇒ By using proteus we can see if we use $V_A = V_B = 6V$ and $V_R = 5 V$ the diode will be in reverse bias mode.

③ What is the function of $R2 = 10\Omega$ at the base
of an invertor in figure 39
flow
⇒ It helps to ~~reed~~ ~~produce~~ less amount of
current in the ease of I_1 and I_2 so that
more current can pass through I_B.

ID-18101543

9) Verify that the transistore will be operating in the saturation and cutoff region in two cases for the invertere circuit.

⇒ From data I got from proteus,

when $V_i = 5v$ (on),

$I_B = 0.23A > 0$

$I_e = 2.22 A > 0$

output voltage $= 0.108 \approx 0v$

$V_{EF} = 0$

we know, $I_E = I_B + I_e = 0.23 + 2.22$

$= 2.45 A > 0$

So, the invertere is in saturation mode

when $V_i = 0v$ (off)

$I_B = 0 A$

$I_e = 0 A$

so, $I_E = I_B + I_e = 0 A$

so, $I_E = I_B = I_e = 0 A$

$V_B < 0$

so, it is in cutoff mode.

⑤ What is the function of $-5v$ voltage source in the inverter circuit?

⇒ When $v_i = 0v$ that time $-5v$ helps to the inverter not to go in reverse bias mode, No current pass through the base, we only get I_1 and I_2. As no current flow through base, the inverter remains in cutoff mode.