1. Description

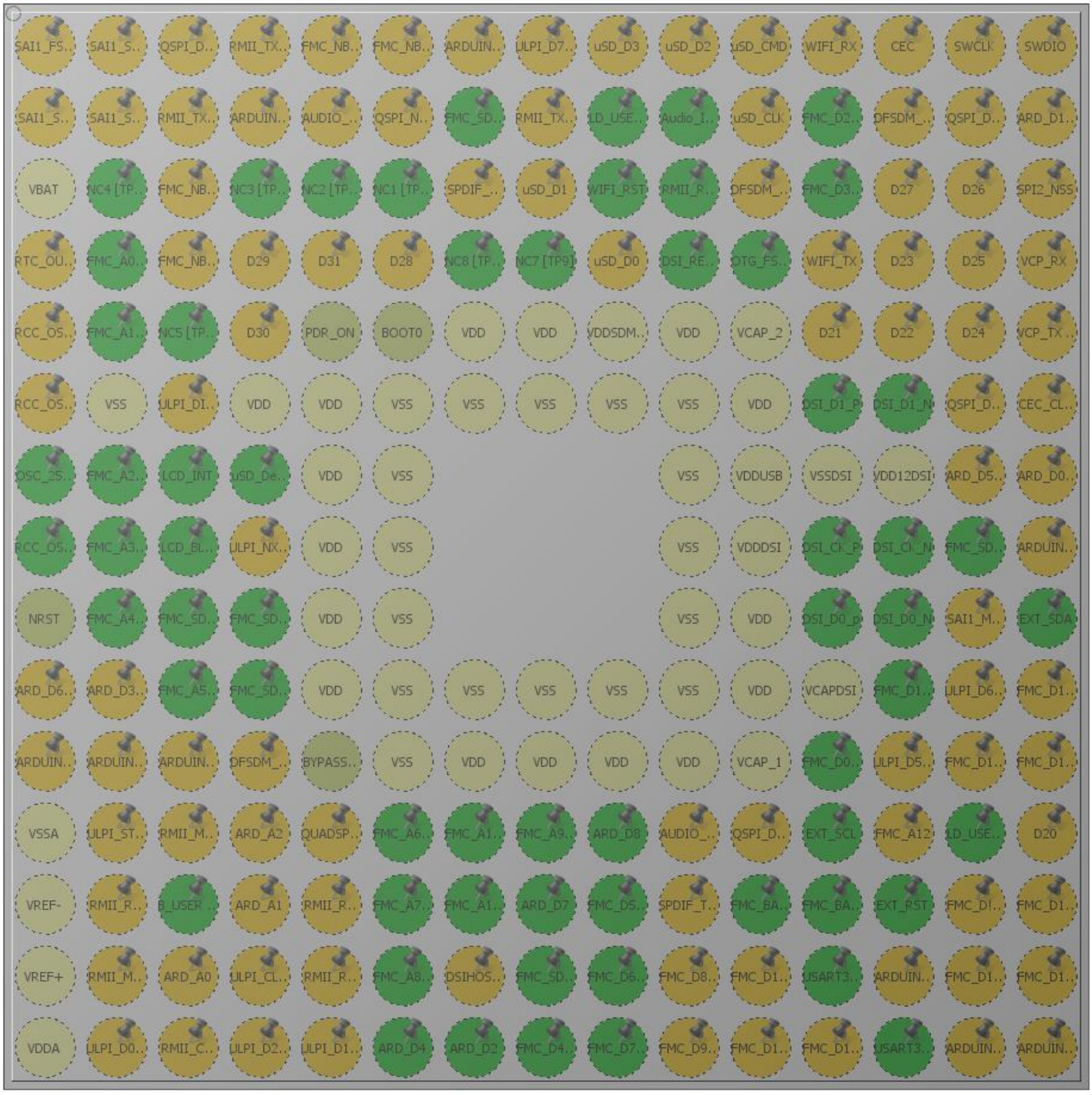
1.1. Project

Project Name	Projet
Board Name	STM32F769I-DISCO
Generated with:	STM32CubeMX 4.22.1
Date	03/19/2018

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x9
MCU name	STM32F769NIHx
MCU Package	TFBGA216
MCU Pin number	216

2. Pinout Configuration



STM32F769NIHx
TFBGA216 (Top view)

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PE4 *	I/O	SAI1_FS_A	SAI1_FSA [WM8994ECS/R_LRCLK1]
A2	PE3 *	I/O	SAI1_SD_B	SAI1_SDB [WM8994ECS/R_ADCDAT1]
A3	PE2 *	I/O	QUADSPI_BK1_IO2	QSPI_D2 [N25Q128A13EF840E_DQ2]
A4	PG14 *	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
A5	PE1 *	I/O	FMC_NBL1	FMC_NBL1 [MT48LC4M32B2B5-6A_DQM1]
A6	PE0 *	I/O	FMC_NBL0	FMC_NBL0 [MT48LC4M32B2B5-6A_DQM0]
A7	PB8 *	I/O	I2C1_SCL	ARDUINO SCL/D15
A8	PB5 *	I/O	USB_OTG_HS_ULPI_D7	ULPI_D7 [USB3320C-EZK_D7]
A9	PB4 *	I/O	SDMMC2_D3	uSD_D3
A10	PB3 *	I/O	SDMMC2_D2	uSD_D2
A11	PD7 *	I/O	SDMMC2_CMD	uSD_CMD
A12	PC12 *	I/O	UART5_TX	WIFI_RX
A13	PA15 *	I/O	CEC	CEC
A14	PA14 *	I/O	SYS_JTCK-SWCLK	SWCLK
A15	PA13 *	I/O	SYS_JTMS-SWDIO	SWDIO
B1	PE5 *	I/O	SAI1_SCK_A	SAI1_SCKA [WM8994ECS/R_BCLK1]
B2	PE6 *	I/O	SAI1_SD_A	SAI1_SDA [WM8994ECS/R_DACDAT1]
B3	PG13 *	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
B4	PB9 *	I/O	I2C1_SDA	ARDUINO SDA/D14
B5	PB7 *	I/O	I2C4_SDA	AUDIO_SDA [WM8994ECS/R_SDA]
B6	PB6 *	I/O	QUADSPI_BK1_NCS	QSPI_NCS [N25Q128A13EF840E_S]

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
B7	PG15	I/O	FMC_SDNCAS	FMC_SDNCAS [MT48LC4M32B2B5-6A_CAS]
B8	PG11 *	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
B9	PJ13 **	I/O	GPIO_Input	LD_USER1 [Led_RED]
B10	PJ12 **	I/O	GPIO_Input	Audio_INT [WM8994ECS/R_GPIO1]
B11	PD6 *	I/O	SDMMC2_CK	uSD_CLK
B12	PD0	I/O	FMC_D2	FMC_D2 [MT48LC4M32B2B5-6A_DQ2]
B13	PC11 *	I/O	DFSDM1_DATIN5	DFSDM_DATIN5 [TP100]
B14	PC10 *	I/O	QUADSPI_BK1_IO1	QSPI_D1 [MT25QL512ABB1EW9_DQ1]
B15	PA12 *	I/O	SPI2_SCK	ARD_D13/SCK
C1	VBAT	Power		
C2	PI8 **	I/O	GPIO_Input	NC4 [TP12]
C3	PI4 *	I/O	FMC_NBL2	FMC_NBL2 [MT48LC4M32B2B5-6A_DQM2]
C4	PK7 **	I/O	GPIO_Input	NC3 [TP15]
C5	PK6 **	I/O	GPIO_Input	NC2 [TP16]
C6	PK5 **	I/O	GPIO_Input	NC1 [TP17]
C7	PG12 *	I/O	SPDIFRX_IN1	SPDIF_RX [74LVC1G04SE_4]
C8	PG10 *	I/O	SDMMC2_D1	uSD_D1
C9	PJ14 **	I/O	GPIO_Input	WIFI_RST
C10	PD5 **	I/O	GPIO_Input	RMII_RXER[LAN8742A-CZ-TR_RXERR]
C11	PD3 *	I/O	DFSDM1_CKOUT	DFSDM_CKOUT [TP102]
C12	PD1	I/O	FMC_D3	FMC_D3 [MT48LC4M32B2B5-6A_DQ3]
C13	PI3 *	I/O	FMC_D27	D27
C14	PI2 *	I/O	FMC_D26	D26
C15	PA11 *	I/O	SPI2_NSS	SPI2_NSS
D1	PC13 *	I/O	RTC_OUT_ALARM	
D2	PF0	I/O	FMC_A0	FMC_A0 [MT48LC4M32B2B5-6A_A0]

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
D3	PI5 *	I/O	FMC_NBL3	FMC_NBL3 [MT48LC4M32B2B5-6A_DQM3]
D4	PI7 *	I/O	FMC_D29	D29
D5	PI10 *	I/O	FMC_D31	D31
D6	PI6 *	I/O	FMC_D28	D28
D7	PK4 **	I/O	GPIO_Input	NC8 [TP18]
D8	PK3 **	I/O	GPIO_Input	NC7 [TP9]
D9	PG9 *	I/O	SDMMC2_D0	uSD_D0
D10	PJ15 **	I/O	GPIO_Input	DSI_RESET
D11	PD4 **	I/O	GPIO_Input	OTG_FS_OverCurrent [STMPS2141STR_Fault]
D12	PD2 *	I/O	UART5_RX	WIFI_TX
D13	PH15 *	I/O	FMC_D23	D23
D14	PI1 *	I/O	FMC_D25	D25
D15	PA10 *	I/O	USART1_RX	VCP_RX
E1	PC14/OSC32_IN *	I/O	RCC_OSC32_IN	RCC_OSC32_IN
E2	PF1	I/O	FMC_A1	FMC_A1 [MT48LC4M32B2B5-6A_A1]
E3	PI12 **	I/O	GPIO_Input	NC5 [TP13]
E4	PI9 *	I/O	FMC_D30	D30
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDDSDMMC	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
E12	PH13 *	I/O	FMC_D21	D21
E13	PH14 *	I/O	FMC_D22	D22
E14	PI0 *	I/O	FMC_D24	D24
E15	PA9 *	I/O	USART1_TX	VCP_TX [STM32F103CBT6_PA3]
F1	PC15/OSC32_OUT *	I/O	RCC_OSC32_OUT	RCC_OSC32_OUT
F2	VSS	Power		
F3	PI11 *	I/O	USB_OTG_HS_ULPI_DIR	ULPI_DIR [USB3320C-EZK_DIR]
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F12	DSIHOST_D1P	MonoIO	DSIHOST_D1P	DSI_D1_P
F13	DSIHOST_D1N	MonoIO	DSIHOST_D1N	DSI_D1_N
F14	PC9 *	I/O	QUADSPI_BK1_IO0	QSPI_D0 [N25Q128A13EF840E_DQ0]
F15	PA8 *	I/O	RCC_MCO_1	CEC_CLK [TP2]
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	OSC_25M [NZ2520SB-25.00M_OUT]
G2	PF2	I/O	FMC_A2	FMC_A2 [MT48LC4M32B2B5-6A_A2]
G3	PI13	I/O	GPIO_EXTI13	LCD_INT
G4	PI15 **	I/O	GPIO_Input	uSD_Detect
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
G12	VSSDSI	Power		
G13	VDD12DSI	Power		
G14	PC8 *	I/O	TIM3_CH3	ARD_D5/PWM
G15	PC7 *	I/O	USART6_RX	ARD_D0/RX
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF3	I/O	FMC_A3	FMC_A3 [MT48LC4M32B2B5-6A_A3]
H3	PI14 **	I/O	GPIO_Input	LCD_BL_CTRL
H4	PH4 *	I/O	USB_OTG_HS_ULPI_NXT	ULPI_NXT [USB3320C-EZK_NXT]
H5	VDD	Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDDDSI	Power		
H12	DSIHOST_CKP	MonoIO	DSIHOST_CKP	DSI_CK_P
H13	DSIHOST_CKN	MonoIO	DSIHOST_CKN	DSI_CK_N
H14	PG8	I/O	FMC_SDCLK	FMC_SDCLK [MT48LC4M32B2B5-6A_CLK]
H15	PC6 *	I/O	USART6_TX	ARDUINO TX/D1

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J1	NRST	Reset		
J2	PF4	I/O	FMC_A4	FMC_A4 [MT48LC4M32B2B5-6A_A4]
J3	PH5	I/O	FMC_SDNWE	FMC_SDNME [MT48LC4M32B2B5-6A_WE]
J4	PH3	I/O	FMC_SDNE0	FMC_SDNE0 [MT48LC4M32B2B5-6A_CS]
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		
J12	DSIHOST_D0P	MonoIO	DSIHOST_D0P	DSI_D0_p
J13	DSIHOST_D0N	MonoIO	DSIHOST_D0N	DSI_D0_N
J14	PG7 *	I/O	SAI1_MCLK_A	SAI1_MCLKA [WM8994ECS/R_MCLK1]
J15	PG6 **	I/O	GPIO_Input	EXT_SDA
K1	PF7 *	I/O	TIM11_CH1	ARD_D6/PWM
K2	PF6 *	I/O	TIM10_CH1	ARD_D3/PWM
K3	PF5	I/O	FMC_A5	FMC_A5 [MT48LC4M32B2B5-6A_A5]
K4	PH2	I/O	FMC_SDCKE0	FMC_SDCKE0 [MT48LC4M32B2B5-6A_CKE]
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
K12	VCAPDSI	Power		
K13	PD15	I/O	FMC_D1	FMC_D1 [MT48LC4M32B2B5-6A_DQ1]
K14	PB13 *	I/O	USB_OTG_HS_ULPI_D6	ULPI_D6 [USB3320C-EZK_D6]
K15	PD10 *	I/O	FMC_D15	FMC_D15 [MT48LC4M32B2B5-6A_DQ15]
L1	PF10 *	I/O	ADC3_IN8	ARDUINO A1

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
L2	PF9 *	I/O	ADC3_IN7	ARDUINO A2
L3	PF8 *	I/O	ADC3_IN6	ARDUINO A3
L4	PC3 *	I/O	DFSDM1_DATIN1	DFSDM_DATIN1 [TP101]
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
L12	PD14	I/O	FMC_D0	FMC_D0 [MT48LC4M32B2B5-6A_DQ0]
L13	PB12 *	I/O	USB_OTG_HS_ULPI_D5	ULPI_D5 [USB3320C-EZK_D5]
L14	PD9 *	I/O	FMC_D14	FMC_D14 [MT48LC4M32B2B5-6A_DQ14]
L15	PD8 *	I/O	FMC_D13	FMC_D13 [MT48LC4M32B2B5-6A_DQ13]
M1	VSSA	Power		
M2	PC0 *	I/O	USB_OTG_HS_ULPI_STP	ULPI_STP [USB3320C-EZK_STP]
M3	PC1 *	I/O	ETH_MDC	RMII_MDC [LAN8742A-CZ-TR_MDC]
M4	PC2 *	I/O	ADC1_IN12	ARD_A2
M5	PB2 *	I/O	QUADSPI_CLK	
M6	PF12	I/O	FMC_A6	FMC_A6 [MT48LC4M32B2B5-6A_A6]
M7	PG1	I/O	FMC_A11	FMC_A11 [MT48LC4M32B2B5-6A_A11]
M8	PF15	I/O	FMC_A9	FMC_A9 [MT48LC4M32B2B5-6A_A9]
M9	PJ4 **	I/O	GPIO_Input	ARD_D8
M10	PD12 *	I/O	I2C4_SCL	AUDIO_SCL [WM8994ECS/R_SCLK]
M11	PD13 *	I/O	QUADSPI_BK1_IO3	QSPI_D3 [N25Q128A13EF840E_DQ3]
M12	PG3 **	I/O	GPIO_Input	EXT_SCL

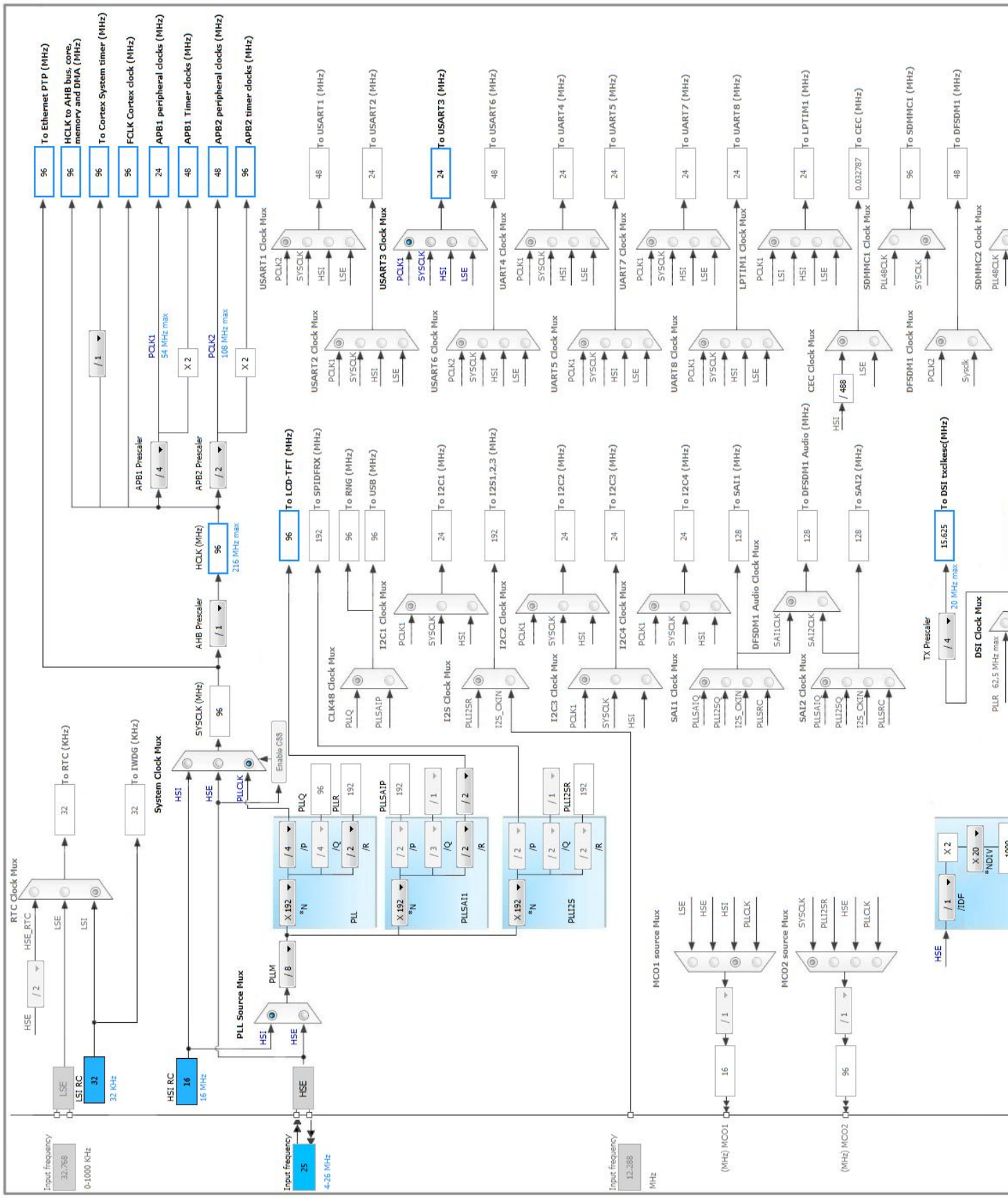
Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
M13	PG2 *	I/O	FMC_A12	FMC_A12
M14	PJ5 **	I/O	GPIO_Input	LD_USER2 [LED_Green]
M15	PH12 *	I/O	FMC_D20	D20
N1	VREF-	Power		
N2	PA1 *	I/O	ETH_REF_CLK	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
N3	PA0/WKUP	I/O	GPIO_EXTI0	B_USER [B1]
N4	PA4 *	I/O	ADC1_IN4	ARD_A1
N5	PC4 *	I/O	ETH_RXD0	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
N6	PF13	I/O	FMC_A7	FMC_A7 [MT48LC4M32B2B5-6A_A7]
N7	PG0	I/O	FMC_A10	FMC_A10 [MT48LC4M32B2B5-6A_A10]
N8	PJ3 **	I/O	GPIO_Input	ARD_D7
N9	PE8	I/O	FMC_D5	FMC_D5 [MT48LC4M32B2B5-6A_DQ5]
N10	PD11 *	I/O	SAI2_SD_A	SPDIF_TX [TP20]
N11	PG5	I/O	FMC_BA1	FMC_BA1 [MT48LC4M32B2B5-6A_BA1]
N12	PG4	I/O	FMC_BA0	FMC_BA0 [MT48LC4M32B2B5-6A_BA0]
N13	PH7 **	I/O	GPIO_Input	EXT_RST
N14	PH9 *	I/O	FMC_D17	FMC_D!7 [MT48LC4M32B2B5-6A_DQ17]
N15	PH11 *	I/O	FMC_D19	FMC_D19 [MT48LC4M32B2B5-6A_DQ19]
P1	VREF+	Power		
P2	PA2 *	I/O	ETH_MDIO	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
P3	PA6 *	I/O	ADC1_IN6	ARD_A0
P4	PA5 *	I/O	USB_OTG_HS_ULPI_CK	ULPI_CLK [USB3320C-EZK_CLKOUT]
P5	PC5 *	I/O	ETH_RXD1	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
P6	PF14	I/O	FMC_A8	FMC_A8 [MT48LC4M32B2B5-6A_A8]
P7	PJ2 *	I/O	DSIHOST_TE	DSIHOST_TE
P8	PF11	I/O	FMC_SDNRAS	FMC_SDNRAS [MT48LC4M32B2B5-6A_RAS]
P9	PE9	I/O	FMC_D6	FMC_D6 [MT48LC4M32B2B5-6A_DQ6]
P10	PE11 *	I/O	FMC_D8	FMC_D8 [MT48LC4M32B2B5-6A_DQ8]
P11	PE14 *	I/O	FMC_D11	FMC_D11 [MT48LC4M32B2B5-6A_DQ11]
P12	PB10	I/O	USART3_TX	
P13	PH6 *	I/O	TIM12_CH1	ARDUINO PWM/D6
P14	PH8 *	I/O	FMC_D16	FMC_D16 [MT48LC4M32B2B5-6A_DQ16]
P15	PH10 *	I/O	FMC_D18	FMC_D18 [MT48LC4M32B2B5-6A_DQ18]
R1	VDDA	Power		
R2	PA3 *	I/O	USB_OTG_HS_ULPI_D0	ULPI_D0 [USB3320C-EZK_D0]
R3	PA7 *	I/O	ETH_CRS_DV	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
R4	PB1 *	I/O	USB_OTG_HS_ULPI_D2	ULPI_D2 [USB3320C-EZK_D2]
R5	PB0 *	I/O	USB_OTG_HS_ULPI_D1	ULPI_D1 [USB3320C-EZK_D1]
R6	PJ0 **	I/O	GPIO_Input	ARD_D4
R7	PJ1 **	I/O	GPIO_Input	ARD_D2
R8	PE7	I/O	FMC_D4	FMC_D4 [MT48LC4M32B2B5-6A_DQ4]
R9	PE10	I/O	FMC_D7	FMC_D7 [MT48LC4M32B2B5-6A_DQ7]
R10	PE12 *	I/O	FMC_D9	FMC_D9 [MT48LC4M32B2B5-6A_DQ9]

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R11	PE15 *	I/O	FMC_D12	FMC_D12 [MT48LC4M32B2B5-6A_DQ12]
R12	PE13 *	I/O	FMC_D10	FMC_D10 [MT48LC4M32B2B5-6A_DQ10]
R13	PB11	I/O	USART3_RX	
R14	PB14 *	I/O	SPI2_MISO	ARDUINO MISO/D12
R15	PB15 *	I/O	SPI2_MOSI	ARDUINO MOSI/PWM/D11

** The pin is affected with an I/O function
* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. DMA2D

mode: Activated

5.1.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0
DMA2D ALPHA Inversion	Regular Alpha
DMA2D Red and Blue swap	Regular mode (RGB or ARGB)

5.2. DSIHOST

DSIHost: Video Mode

5.2.1. DSI Clocks:

from PLLDSI:

Pllndiv	20
Pllodf	DSI_PLL_OUT_DIV1
Pllidf	DSI_PLL_IN_DIV1
High Speed Clock - PLLDSI Output	500000
Lane Byte Clock	62500
Tx Escape Ckdiv	4
Transmission Escape Clock	15625
Time Out Clock	62500

from PLLR:

Lane Byte Clock	192000
Transmission Escape Clock	48000
Time Out Clock	192000

5.2.2. Timeout Counters:

Time Out Clock Setting:

Time Out Clock Divider	1
Time Out Clock - from PLLDSI	62500

Contention Error Detection:

High-speed transmission time-out	0
No High-speed transmission time-out	
Low-power reception time-out	0
No Low-power reception time-out	

5.2.3. Data and Clock Lanes:

Basic Settings:

Number of Lanes	One Data Lane
Automatic Clock Lane Control	Clock Data lane is always provided
Bus Turn Around Request is	Enabled

Flow Control - Configuration:

CRC Reception	Disabled
ECC Reception	Disabled
EoTP Reception is	Disabled
EoTP Transmission is	Disabled

Flow Control - Packet Analyzer Configuration:

CRC Error Interrupt	Disable
ECC Errors Interrupt	Disable
EoTP Error Interrupt	Disable
Packet Size Error Interrupt	Disable
Acknowledge Errors Interrupt	Disable
PHY related Errors Interrupt	Disable

5.2.4. PHY Timings:

LP to HS and HS to LP Transitions Timings:

Maximum time taken by the D-PHY clock lane to go from HS to LP transmission	28
Resulting Maximum time taken by the D-PHY clock lane to go from HS to LP transmission	448
Maximum time taken by the D-PHY clock lane to go from LP to HS transmission	33
Resulting Maximum time taken by the D-PHY clock	528

lane to go from LP to HS transmission	
Maximum time taken by the D-PHY data lane to go from HS to LP transmission	15
Resulting Maximum time taken by the D-PHY data lane to go from HS to LP transmission	240
Maximum time taken by the D-PHY data lane to go from LP to HS transmission	25
Resulting Maximum time taken by the D-PHY data lane to go from LP to HS transmission	400
Minimum wait period to request a HS transmission after the Stop state (min est 1 cycle de esccape clock)	0
Resulting Minimum wait period to request a HS transmission after the Stop state (min est 1 cycle de esccape clock)	0

5.2.5. Commands:

APB Interface Error Configuration:

Generic Command Error Interrupt	Disable

Transmission of Commands during HS Video Transmission Mode:

During HS Video Mode, Commands are Transmited in	High Speed

Read Command Timing:

Maximum time taken to perform a read command	0

5.2.6. Display Interface:

Basic Settings:

Display ID	0
Color Coding	RGB888 (24 bits) - DSI mode

Video Mode Configuration:

Video Mode	Non Burst Mode with Sync
Video Packet Size	1
Number of Chuncks	640
Null Packet Size	0
Frame BTA Acknowledge Enable	Disable

Frame Vertical Timings:

VSA: Vertical Synchronism Active duration (Default value is retrieved from LTDC)	4
VBP: Vertical Back-Porch duration (Default value is retrieved from LTDC)	2
VFP: Vertical Front-Porch duration (Default value is retrieved from LTDC)	2
VACT: Vertical Active duration (Default value is	480

retrieved from LTDC)

Frame Horizontal Timings:

HSA: Horizontal Synchronism Active duration (Default value is retrieved from LTDC)	5
HBP: Horizontal Back-Porch duration (Default value is retrieved from LTDC)	5
HLINE: Horizontal Line duration (Default value is retrieved from LTDC)	430

Enabling Low-Power Transitions during: :

Horizontal Front-Porch (HFP) Period	Disable
Horizontal Back-Porch (HBP) Period	Disable
Vertical Active (VACT) Period	Disable
Vertical Front Porch (VFP) Period	Disable
Vertical Back Porch (VBP) Period	Disable
Vertical Sync time (VSA) Period	Disable

5.2.7. LTDC Interface:

Frame Vertical Timings:

VSA: Vertical Synchronism Active duration (set in LTDC)	4
VBP: Vertical Back-Porch duration (set in LTDC)	2
VFP: Vertical Front-Porch duration (set in LTDC)	2
VACT: Vertical Active duration (set in LTDC)	480

Frame Horizontal Timings:

HSA: Horizontal Synchronism Active duration (set in LTDC)	8
HBP: Horizontal Back-Porch duration (set in LTDC)	7
HACT: Horizontal Active duration (set in LTDC)	640
HLINE: Horizontal Line duration (set in LTDC)	661

Clocking:

LTDC Pixel Clock (from Clock tree)	96

Polarity of the Control Signals:

VSYNC Polarity (set in LTDC)	DSI_VSYNC_ACTIVE_LOW
HSYNC Polarity (set in LTDC)	DSI_HSYNC_ACTIVE_LOW
Data Enable Polarity (set in LTDC)	DSI_DATA_ENABLE_ACTIVE_LOW

Interface Error Configuration:

LTDC FIFO Overflow Error Interrupt is	Disabled

5.3. FMC

SDRAM 2

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 12 bits

Data: 8 bits

5.3.1. SDRAM 2:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	1 memory clock cycle
Write protection	Disabled
SDRAM common clock	Disabled
SDRAM common burst read	Disabled
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	16
Exit self-refresh delay	16
Self-refresh time	16
SDRAM common row cycle delay	16
Write recovery time	16
SDRAM common row precharge delay	16
Row to column delay	16

5.4. LTDC

Display Type: RGB888 (24 bits) - DSI mode

5.4.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	640
Horizontal Front Porch	6
HSync Width	7

Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	654
Total Width	660

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	480
Vertical Front Porch	2
VSync Height	3
Accumulated Vertical Back Porch Height	5
Accumulated Active Height	485
Total Height	487

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

5.4.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Number of Layers:

Number of Layers	2 layers

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	0
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	0
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	0
Layer 1 - Window Vertical Start	0

Layer 1 - Window Vertical Stop	0

Pixel Parameters:

Layer 0 - Pixel Format	ARGB8888
Layer 1 - Pixel Format	ARGB8888

Blending:

Layer 0 - Alpha constant for blending	0
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant
Layer 1 - Alpha constant for blending	0
Layer 1 - Default Alpha value	0
Layer 1 - Blending Factor1	Alpha constant
Layer 1 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	0
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	0

5.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Disabled

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 3

5.6. SYS

Timebase Source: SysTick

5.7. USART3

Mode: Asynchronous

5.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DSIHOST	DSIHOST_D1P	DSIHOST_D1P	n/a	n/a	n/a	DSI_D1_P
	DSIHOST_D1N	DSIHOST_D1N	n/a	n/a	n/a	DSI_D1_N
	DSIHOST_CKP	DSIHOST_CKP	n/a	n/a	n/a	DSI_CK_P
	DSIHOST_CKN	DSIHOST_CKN	n/a	n/a	n/a	DSI_CK_N
	DSIHOST_D0P	DSIHOST_D0P	n/a	n/a	n/a	DSI_D0_p
	DSIHOST_D0N	DSIHOST_D0N	n/a	n/a	n/a	DSI_D0_N
FMC	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNCAS [MT48LC4M32B2B5-6A_CAS]
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D2 [MT48LC4M32B2B5-6A_DQ2]
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D3 [MT48LC4M32B2B5-6A_DQ3]
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A0 [MT48LC4M32B2B5-6A_A0]
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A1 [MT48LC4M32B2B5-6A_A1]
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A2 [MT48LC4M32B2B5-6A_A2]
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A3 [MT48LC4M32B2B5-6A_A3]
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDCLK [MT48LC4M32B2B5-6A_CLK]
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A4 [MT48LC4M32B2B5-6A_A4]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNME [MT48LC4M32B2B5-6A_WE]
	PH3	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNE0 [MT48LC4M32B2B5-6A_CS]
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A5 [MT48LC4M32B2B5-6A_A5]
	PH2	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDCKE0 [MT48LC4M32B2B5-6A_CKE]
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D1 [MT48LC4M32B2B5-6A_DQ1]
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D0 [MT48LC4M32B2B5-6A_DQ0]
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A6 [MT48LC4M32B2B5-6A_A6]
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A11 [MT48LC4M32B2B5-6A_A11]
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A9 [MT48LC4M32B2B5-6A_A9]
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A7 [MT48LC4M32B2B5-6A_A7]
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A10 [MT48LC4M32B2B5-6A_A10]
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D5 [MT48LC4M32B2B5-6A_DQ5]
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_BA1 [MT48LC4M32B2B5-6A_BA1]
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_BA0 [MT48LC4M32B2B5-6A_BA0]
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A8 [MT48LC4M32B2B5-6A_A8]
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNRAS [MT48LC4M32B2B5-

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
						6A_RAS]
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D6 [MT48LC4M32B2B5-6A_DQ6]
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D4 [MT48LC4M32B2B5-6A_DQ4]
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D7 [MT48LC4M32B2B5-6A_DQ7]
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	OSC_25M [NZ2520SB-25.00M_OUT]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
USART3	PB10	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PB11	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
Single Mapped Signals	PE4	SAI1_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI1_FSA [WM8994ECS/R_LRCLK1]
	PE3	SAI1_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI1_SDB [WM8994ECS/R_ADCDAT1]
	PE2	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D2 [N25Q128A13EF840E_DQ2]
	PG14	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_NBL1 [MT48LC4M32B2B5-6A_DQM1]
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_NBL0 [MT48LC4M32B2B5-6A_DQM0]
	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	Low	ARDUINO SCL/D15
	PB5	USB_OTG_HS_ULPI_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ULPI_D7 [USB3320C-EZK_D7]
	PB4	SDMMC2_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	uSD_D3
	PB3	SDMMC2_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	uSD_D2
	PD7	SDMMC2_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	uSD_CMD
	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	WIFI_RX

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA15	CEC	Alternate Function Open Drain	No pull-up and no pull-down	Low	CEC
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PE5	SAI1_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI1_SCKA [WM8994ECS/R_BCLK1]
	PE6	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI1_SDA [WM8994ECS/R_DACDAT1]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	Low	ARDUINO SDA/D14
	PB7	I2C4_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	AUDIO_SDA [WM8994ECS/R_SDA]
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_NCS [N25Q128A13EF840E_S]
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
	PD6	SDMMC2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	uSD_CLK
	PC11	DFSDM1_DATIN5	Alternate Function Push Pull	No pull-up and no pull-down	Low	DFSDM_DATIN5 [TP100]
	PC10	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D1 [MT25QL512ABB1EW9_DQ1]
	PA12	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARD_D13/SCK
	PI4	FMC_NBL2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_NBL2 [MT48LC4M32B2B5-6A_DQM2]
	PG12	SPDIFRX_IN1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPDIF_RX [74LVC1G04SE_4]
	PG10	SDMMC2_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	uSD_D1
	PD3	DFSDM1_CKOUT	Alternate Function Push Pull	No pull-up and no pull-down	Low	DFSDM_CKOUT [TP102]
	PI3	FMC_D27	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D27
	PI2	FMC_D26	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D26
	PA11	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI2_NSS
	PC13	RTC_OUT_ALARM	n/a	n/a	**n/a**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PI5	FMC_NBL3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_NBL3 [MT48LC4M32B2B5-6A_DQM3]
	PI7	FMC_D29	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D29
	PI10	FMC_D31	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D31
	PI6	FMC_D28	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D28
	PG9	SDMMC2_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	uSD_D0
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	WIFI_TX
	PH15	FMC_D23	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D23
	PI1	FMC_D25	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D25
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	VCP_RX
	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	**n/a**	RCC_OSC32_IN
	PI9	FMC_D30	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D30
	PH13	FMC_D21	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D21
	PH14	FMC_D22	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D22
	PI0	FMC_D24	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D24
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	VCP_TX [STM32F103CBT6_PA3]
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	RCC_OSC32_OUT
	PI11	USB_OTG_HS_ULPI_DIR	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ULPI_DIR [USB3320C-EZK_DIR]
	PC9	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D0 [N25Q128A13EF840E_DQ0]
	PA8	RCC_MCO_1	Alternate Function Push Pull	No pull-up and no pull-down	Low	CEC_CLK [TP2]
	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARD_D5/PWM
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARD_D0/RX
	PH4	USB_OTG_HS_ULPI_NXT	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ULPI_NXT [USB3320C-EZK_NXT]
	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARDUINO TX/D1
	PG7	SAI1_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI1_MCLKA [WM8994ECS/R_MCLK1]
	PF7	TIM11_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARD_D6/PWM
	PF6	TIM10_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARD_D3/PWM
	PB13	USB_OTG_HS_ULPI_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ULPI_D6 [USB3320C-EZK_D6]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D15 [MT48LC4M32B2B5-6A_DQ15]
	PF10	ADC3_IN8	Analog mode	No pull-up and no pull-down	n/a	ARDUINO A1
	PF9	ADC3_IN7	Analog mode	No pull-up and no pull-down	n/a	ARDUINO A2
	PF8	ADC3_IN6	Analog mode	No pull-up and no pull-down	n/a	ARDUINO A3
	PC3	DFSDM1_DATIN1	Alternate Function Push Pull	No pull-up and no pull-down	Low	DFSDM_DATIN1 [TP101]
	PB12	USB_OTG_HS_ULPI_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ULPI_D5 [USB3320C-EZK_D5]
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D14 [MT48LC4M32B2B5-6A_DQ14]
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D13 [MT48LC4M32B2B5-6A_DQ13]
	PC0	USB_OTG_HS_ULPI_STP	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ULPI_STP [USB3320C-EZK_STP]
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_MDC [LAN8742A-CZ-TR_MDC]
	PC2	ADC1_IN12	Analog mode	No pull-up and no pull-down	**n/a**	ARD_A2
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD12	I2C4_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	AUDIO_SCL [WM8994ECS/R_SCLK]
	PD13	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D3 [N25Q128A13EF840E_DQ3]
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A12
	PH12	FMC_D20	Alternate Function Push Pull	No pull-up and no pull-down	Very High	D20
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	**n/a**	ARD_A1
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
	PD11	SAI2_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPDIF_TX [TP20]
	PH9	FMC_D17	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D!7 [MT48LC4M32B2B5-6A_DQ17]
	PH11	FMC_D19	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D19 [MT48LC4M32B2B5-6A_DQ19]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	**n/a**	ARD_A0
	PA5	USB_OTG_HS_ULPI_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ULPI_CLK [USB3320C-EZK_CLKOUT]
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
	PJ2	DSIHOST_TE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	DSIHOST_TE
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D8 [MT48LC4M32B2B5-6A_DQ8]
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D11 [MT48LC4M32B2B5-6A_DQ11]
	PH6	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARDUINO PWM/D6
	PH8	FMC_D16	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D16 [MT48LC4M32B2B5-6A_DQ16]
	PH10	FMC_D18	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D18 [MT48LC4M32B2B5-6A_DQ18]
	PA3	USB_OTG_HS_ULPI_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ULPI_D0 [USB3320C-EZK_D0]
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
	PB1	USB_OTG_HS_ULPI_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ULPI_D2 [USB3320C-EZK_D2]
	PB0	USB_OTG_HS_ULPI_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ULPI_D1 [USB3320C-EZK_D1]
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D9 [MT48LC4M32B2B5-6A_DQ9]
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D12 [MT48LC4M32B2B5-6A_DQ12]
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D10 [MT48LC4M32B2B5-6A_DQ10]
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARDUINO MISO/D12
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARDUINO MOSI/PWM/D11
GPIO	PJ13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LD_USER1 [Led_RED]
	PJ12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Audio_INT

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
						[WM8994ECS/R_GPIO1]
	PI8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NC4 [TP12]
	PK7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NC3 [TP15]
	PK6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NC2 [TP16]
	PK5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NC1 [TP17]
	PJ14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	WIFI_RST
	PD5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	RMII_RXER[LAN8742A-CZ-TR_RXERR]
	PK4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NC8 [TP18]
	PK3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NC7 [TP9]
	PJ15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DSI_RESET
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	OTG_FS_OverCurrent [STMPS2141STR_Fault]
	PI12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NC5 [TP13]
	PI13	GPIO_EXTI13	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	LCD_INT
	PI15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	uSD_Detect
	PI14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LCD_BL_CTRL
	PG6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	EXT_SDA
	PJ4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ARD_D8
	PG3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	EXT_SCL
	PJ5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LD_USER2 [LED_Green]
	PA0/WKUP	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	B_USER [B1]
	PJ3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ARD_D7
	PH7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	EXT_RST
	PJ0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ARD_D4
	PJ1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ARD_D2

6.2. DMA configuration

DMA request	Stream	Direction	Priority
MEMTOMEM	DMA2_Stream0	Memory To Memory	**High ***

MEMTOMEM: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Src Memory Increment:	**Enable ***
Dst Memormy Increment:	**Enable ***
Src Memory Data Width:	Byte
Dst Memormy Data Width:	Byte
Src Memory Burst Size:	Single
Dst Memormy Burst Size:	Single

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line0 interrupt	unused		
USART3 global interrupt	unused		
FMC global interrupt	unused		
FPU global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		
DMA2D global interrupt	unused		
DSI global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x9
MCU	STM32F769NIHx
Datasheet	029041_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	Projet
Project Folder	C:\Users\TophersAlien\workspace\Projet
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.8.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No