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Computer Engine USA

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VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

OCTOBER 1992

Currie, Peak & Frazier, Inc.



Electronic Marketing Specialist
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MICROVAD

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TABLE OF CONTENTS

1.0 SYSTEM OVERVIEW	1
1.1 Product Objectives	4
2.0 HARDWARE DESCRIPTION	
2.1 Vadem's Single Bus Architecture	4
2.1.1 Configuration Registers	4
2.1.2 Bus Cycle Generator (BCG)	4
2.2 Memory Subsystem	9
2.2.1 ROM	13
2.2.2 BIOS ROM Addressing	15
2.2.3 Static RAM (SRAM)	15
2.2.4 Psuedo Static RAM (PSRAM)	17
2.2.5 Dynamic RAM (DRAM)	19
2.2.6 Implementing the VG-230 Memory Subsystem	21
2.2.7 Memory Controller and Memory Manager	24
2.2.8 Memory Mapping Examples	28
2.2.9 Flash ROM Support	28
2.3 PCMCIA PC Card Support	31
2.3.1 Hardware	33
2.3.2 Hot Insertion	34
2.3.3 PCMCIA Register Description	35
2.4 Firmware	46
2.5 Display Subsystem	49
2.5.1 VG-230 CGA LCD Controller	49
2.5.2 CGA Compatible Registers	51
2.5.3 VG-230 Specific CGA LCD Controller Registers	54
2.5.4 CGA and AT&T Compatibility Registers	58
2.5.5 Interfacing to LCD Panels	60
2.5.6 Support of Small LCD Panels	62
2.5.7 Ink Plane Feature	64
2.6 Power Management	65
2.6.1 Vadem PMU Modes	65
2.6.1.1 The ON State	67
2.6.1.2 The DOZE State	67
2.6.1.3 The SLEEP State	68
2.6.1.4 The SUSPEND State	70
2.6.1.5 The OFF State	72
2.6.1.6 State Status	72

2.6.2	Activity Monitor	74
2.6.3	Power Control Registers	77
2.6.4	Power Sequencing	78
2.6.5	Power Down Considerations	82
2.6.6	Low Battery Input (LB)	83
2.6.7	Modem Ring-In Input (RI)	84
2.6.8	Real Time Clock Alarm Wake-Up Feature	84
2.6.9	Suspend Mode Support of DRAM Refresh	84
2.7	Power Supply Interfacing	86
2.7.1	External Input (EXT)	87
2.7.2	System Power Control - VPSYS	88
2.7.3	LCD Power Control - VPLCD and VPBIAS	88
2.7.4	PC Card Power Control - VPCRD, VPPENA and VPPENB	88
2.7.5	SNEPWRGD and SYSPWRGD	89
2.7.6	Power Switching	90
2.8	Keyboard	91
2.8.1	Scanned Keyboard Interface	91
2.8.2	Serial PC/XT Keyboard Interface	97
2.8.3	Disabling Internal Keyboard Controller	99
2.9	UART	100
2.10	Parallel Printer Interface	103
2.10.1	Implementing a Bi-directional Port	107
2.11	Real Time clock	108
2.11.1	RTC Timer Registers	108
2.11.2	RTC Alarm	110
2.11.3	Periodic Interrupt Feature	112
2.11.4	Setting The RTC and Power Up Considerations	112
2.11.5	RTC CMOS RAM	113
2.12	Expansion	114
2.12.1	Interrupts	114
2.12.2	DMA	117
2.12.3	Command Delay and DMA Clock Control	118
2.12.4	The ISA Bus and Buffering	118

2.13	Other Peripherals	120
2.13.1	Speaker	120
2.13.2	Revision Register	121
2.13.3	Floppy Expansion	121
2.14	General Purpose I/O Pins (GPIO)	122
3.0	IMPLEMENTATION NOTES	126
3.1	Crystal/Oscillator Selection	126
3.1.1	Selection of 32.215905/28.63636 Crystal Oscillators	126
3.1.2	Selection of 3.6864MHz Crystal	130
3.2	Bus Loading Specifications	131
3.3	Layout Considerations	131
3.4	Battery Life Calculation	131
4.0	NON MASKABLE INTERRUPTS AND SYSTEM MANAGEMENT MODE (SMM)	135
4.1	Power Management NMIs	137
4.2	Keyboard NMIs	139
4.3	System Management Mode NMIs	140
5.0	ICE / TESTSUPPORT	142

LIST OF FIGURES

Figure 1.0-1	VG-230 Block Diagram	1
Figure 1.0-2	Configuration 1—2 PC Card Slots, Printer Port, Serial Keyboard	2
Figure 1.0-3	Configuration 2—1 PC Card Slot, Scanned Keyboard I/F	3
Figure 2.1-1	Clock Distribution	5
Figure 2.2-1	Memory Map	9
Figure 2.2-2	8 bit ROM Interface	14
Figure 2.2-2a	16 bit ROM Interface	14
Figure 2.2-3	8 Bit SRAM Interface	16
Figure 2.2-3a	6 Bit SRAM Interface	16
Figure 2.2-4	8 Bit PSRAM Interface	18
Figure 2.2-4a	16 Bit PSRAM Interface	18
Figure 2.2-5	8 Bit DRAM Interface	20
Figure 2.2-5a	16 Bit DRAM Interface	20
Figure 2.2-6	Large Array Interface	23
Figure 2.2-7	Memory Mapping Example	29
Figure 2.2-8	128 x 8 Flash ROM Interface	30
Figure 2.2-8A	128 x 16 Flash ROM Interface	30
Figure 2.3-1	PCMCIA SLOT A Interface	33
Figure 2.3-2	PCMCIA SLOT B Interface	33
Figure 2.3-3	Hot Insertion Buffering	34
Figure 2.4-1	Interface Between Hardware, Drivers and DOS	46
Figure 2.4-2	PCMCIA Support Layers	47
Figure 2.5-1	LCD Signal Interface	61
Figure 2.5-2	400 Line LCD Panel Interface	63
Figure 2.5-3	240 x 128 LCD Panel Interface	63
Figure 2.5-4	Ink Plane	64
Figure 2.6-1	VG-230 PMU State Diagram	66
Figure 2.6-2	Entering / Exiting SUSPEND—DRAM PSRAM System	79
Figure 2.6-3	Entering / Exiting SUSPEND—SRAM System	81
Figure 2.7-1	Power Supply Interface	87
Figure 2.7-3	VG-230 Power On Sequence	89
Figure 2.7-4	Load Switch Example	90
Figure 2.8-1	Keyboard Matrix Connection	97
Figure 2.8-2	XT Keyboard Interface	99
Figure 2.9-1	SIO Block Diagram	100
Figure 2.10-1	Parallel Printer Interface	106
Figure 2.10-2	VG-230 Parallel Port Implementation	107
Figure 2.12-1	Internal Interrupt Configuration	115
Figure 2.12-2	Expansion Buffer Configuration	119

Figure 2.13-1	Speaker Circuit	120
Figure 2.13-2	Floppy Expansion	121
Figure 3.1-1	High Frequency Xtal Oscillator Configuration	126
Figure 3.1-2	3.6864 MHz Crystal Selection	129
Figure 3.1-3	32 KHz Crystal Selection	130
Figure 4.0-1	NMI Distribution	135

LIST OF TABLES

Table 2.2-1	VG-230 Memory Areas	24
Table 2.2-2	Memory Mapping Register Description	26
Table 2.2-3	PSRAM/SRAM and ROM/FLASH ROM Selects	28
Table 2.5-1	ATT Mode Selection	60
Table 2.5-2	LCD Data Bit Interface	61
Table 2.5-3	LCD Resolutions	62
Table 2.6-1	VG-230 Power Management Modes	65
Table 2.6-2	Activity Monitor Address	74
Table 2.8-1	Scanned Keyboard Alternate Pin Functions	98
Table 2.12-1	Internal Interrupts of Control / Status Registers	114
Table 3.4-1	Capacity Coefficient (K)	132
Table 3.4-2	VG-230 Power Consumption	134

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

0CS-OV MEGAV
BUNDLES NO OBTAIN-BUS
DISKGRAPHIC JACKHORN

1.0 SYSTEM OVERVIEW

The Vadem VG-230 Sub-notebook Engine (SNE) is a single chip implementation of a PC/XT class portable computer. The VG-230 contains the following subsystems:

- 16MHz NEC V-30HL CPU core
- PC/XT compatible core logic
- LCD controller capable of up to 640 x 400 resolution
- PCMCIA version 2.0 PC card support
- 8250 compatible UART
- XT keyboard interface
- EMS 4.0 compatible memory subsystem, supports up to 64Mbytes
- Real Time clock with CMOS RAM
- Vadem Power Management Unit (PMU)

See Figure 1.0-1 for an internal block diagram of the VG-230 SNE.

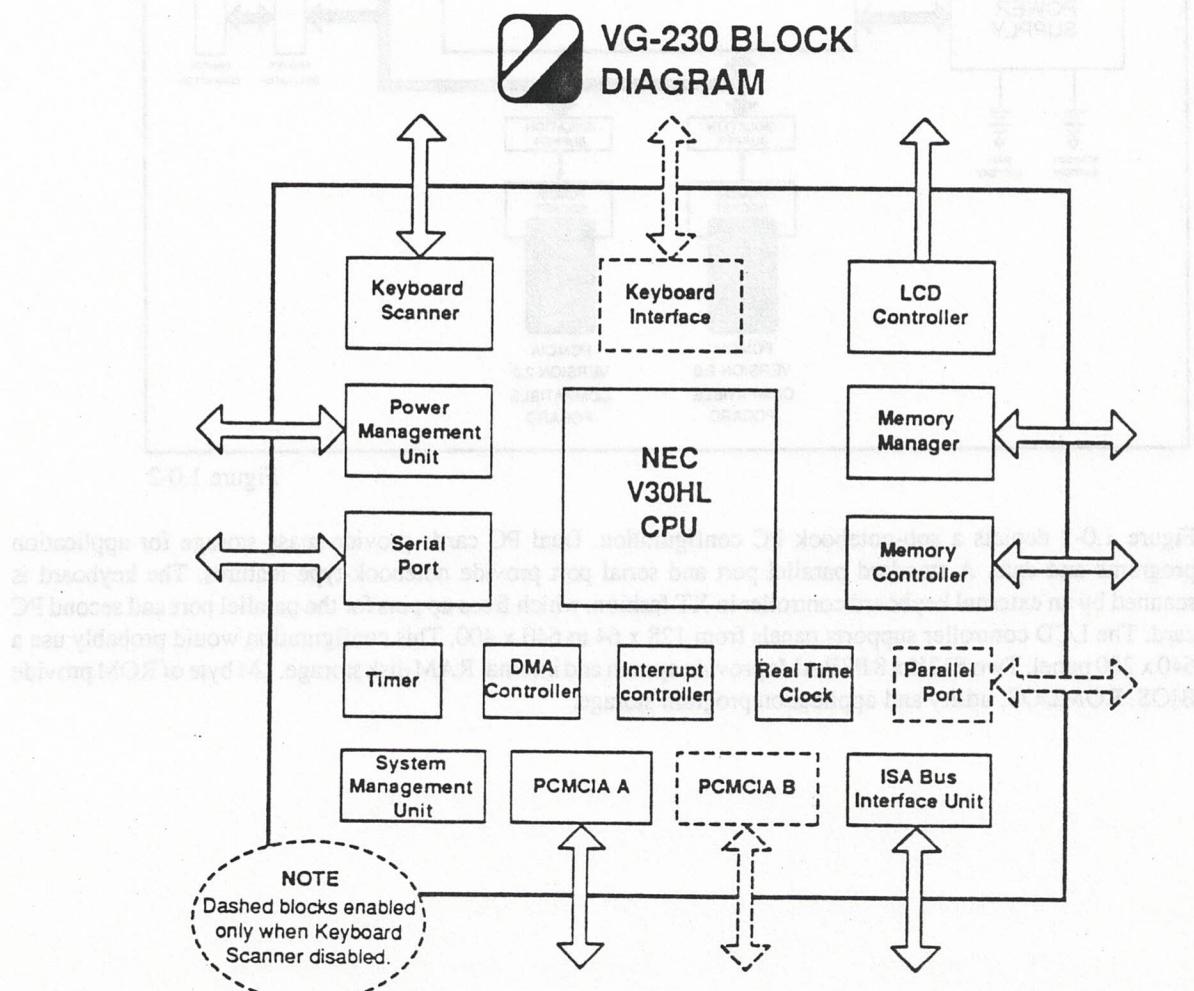


Figure 1.0-1

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CONFIGURATION 1 - 2 PC Card Slots, Printer Port, Serial Keyboard

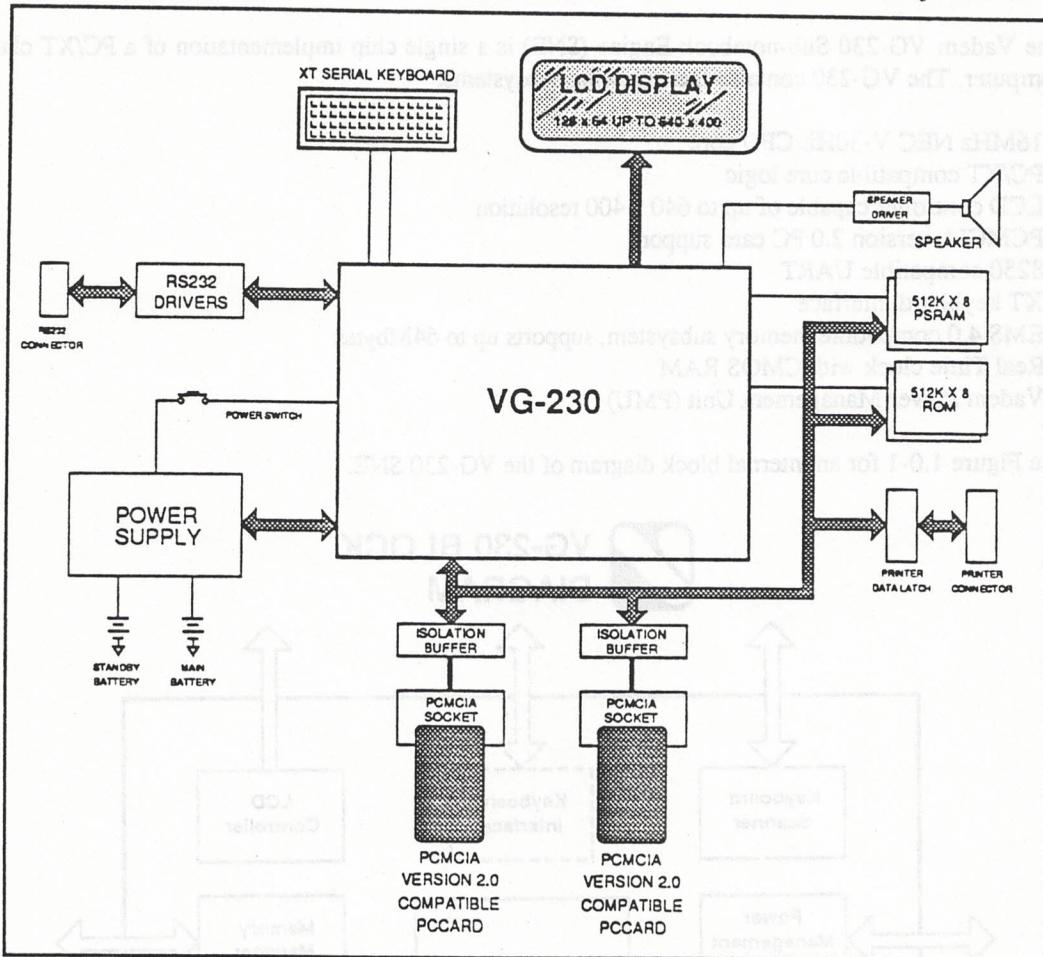
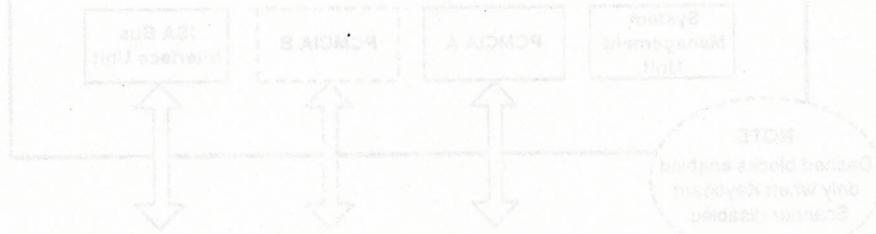


Figure 1.0-2

Figure 1.0-2 depicts a sub-notebook PC configuration. Dual PC cards provide mass storage for application programs and data. A standard parallel port and serial port provide notebook-type features. The keyboard is scanned by an external keyboard controller in XT fashion, which frees up pins for the parallel port and second PC card. The LCD controller supports panels from 128 x 64 to 640 x 400. This configuration would probably use a 640 x 200 panel. Two 512K x 8 PSRAMs provide system and internal RAM disk storage. 1M byte of ROM provide BIOS, ROMDOS, utility and application program storage.



VADEM VG-230

SUB-NOTEBOOK ENGINE

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CONFIGURATION 2 - 1 PC Card Slot, Scanned Keyboard I/F

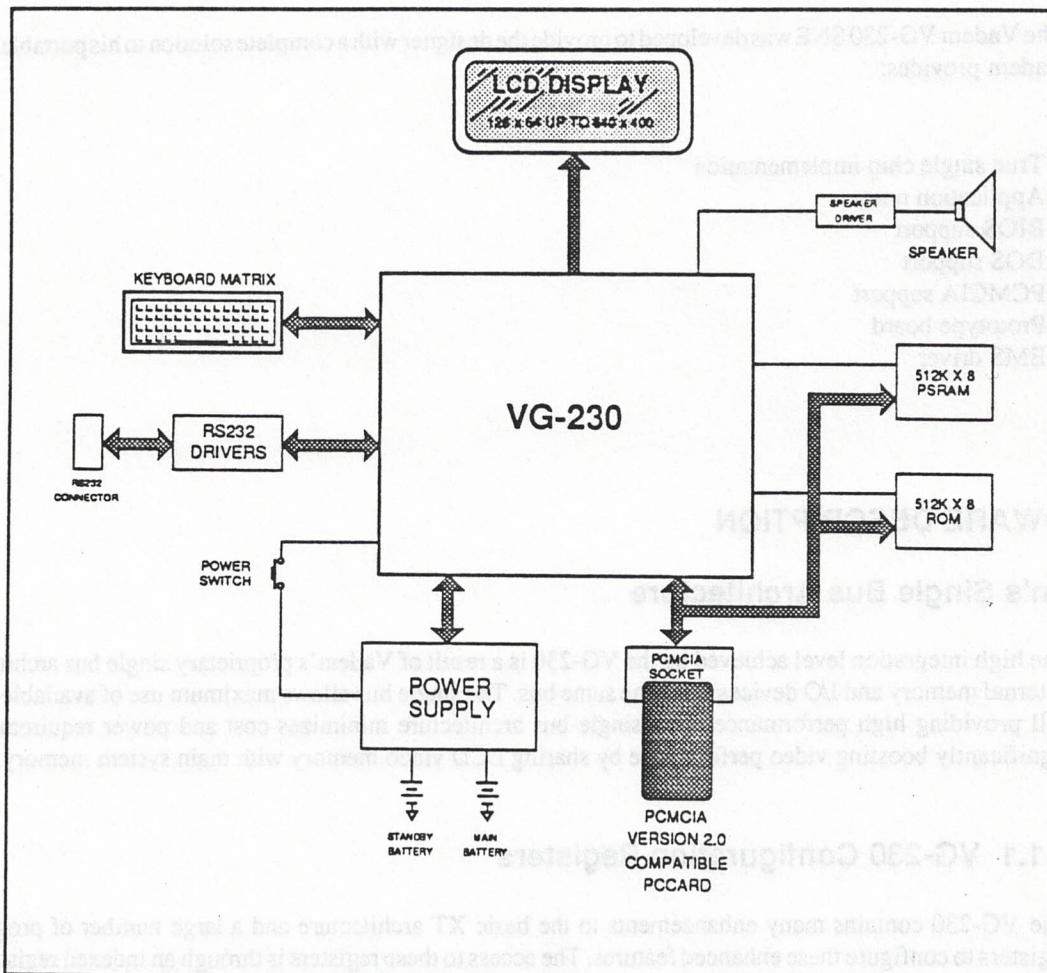


Figure 1.0-3

Figure 1.0-3 depicts a minimal system configuration for a DOS-compatible pocket organizer-type product. A single PC card provides mass storage for applications and data. The internally scanned keyboard reduces parts count and power consumption. The full range of LCD displays are supported, however for this type of product a smaller display may be desirable. A single package provides 512K of PSRAM for system RAM, video RAM and an internal RAM disk. A single 4M ROM provides 512K of BIOS, DOS and application storage.

This diagram shows the VG-230 with 12 bits of memory resulting in a total of 320KB of memory. The memory is divided between 512KB of RAM and 512KB of ROM. The ROM is used for booting and contains 512KB of BIOS, DOS, and application code. The RAM is used for system operations and contains 512KB of PSRAM for video and system memory. The VG-230 also includes a PCMCIA socket for a 4MB PC card, which provides additional storage and functionality. The VG-230 is powered by a 3.6V battery, which is rechargeable and can be charged via a power adapter or a USB port. The VG-230 also features a speaker and a speaker driver, as well as a keyboard matrix and RS232 drivers for communication with external devices. The VG-230 is designed to be a compact and portable device, making it ideal for use as a sub-notebook engine or a pocket organizer.

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1.1 Product Objectives

The Vadem VG-230 SNE was developed to provide the designer with a complete solution to his portable PC design. Vadem provides:

- True single chip implementation
- Application notes
- BIOS support
- DOS support
- PCMCIA support
- Prototype board
- EMS driver

2.0 HARDWARE DESCRIPTION

2.1 Vadem's Single Bus Architecture

The high integration level achieved by the VG-230 is a result of Vadem's proprietary single bus architecture. All external memory and I/O devices share the same bus. The single bus allows maximum use of available pins while still providing high performance. This single bus architecture minimizes cost and power requirements while significantly boosting video performance by sharing LCD video memory with main system memory.

2.1.1 VG-230 Configuration Registers

The VG-230 contains many enhancements to the basic XT architecture and a large number of programmable registers to configure these enhanced features. The access to these registers is through an indexed register scheme. The address of the desired register is first written to the index register located at I/O address 26H. The contents of the desired register may be read from or written to the data register at I/O address 27H.

2.1.2 Bus Cycle Generator (BCG)

The Bus Cycle Generator (BCG) controls the system timing for all I/O and memory accesses. The BCG can be configured for various memory and I/O wait states through registers located in the VG-230's configuration space.

CPUOSC is the frequency of the crystal oscillator connected to the X1 and X2 pins. There are two possible frequencies at which the VG-230 can run, 32.215905 MHz and 28.63636 MHz. CPUOSC is routed through the PMU to the CPUCLK divider. The PMU will divide the clock from 1 to 8 times depending on its state and the CLKSPD bit. PMUOSC is divided from 2 to 8 times to create CPUCLK. CPUCLK is used as the timebase for all VG-230 controlled RAM and ROM accesses. SYSLCK is generated from CPUCLK and can equal CPUCLK or be divided 2, 3 or 4 times. SYSLCK is used for all I/O cycles and expansion memory cycles. Figure 2.1-1 illustrates the clock divider circuitry in the VG-230.

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SEC-01 M3 CAV
SOKOMS HOGESTON-SUB
COMBUSTER JACKMINT

CLOCK DISTRIBUTION

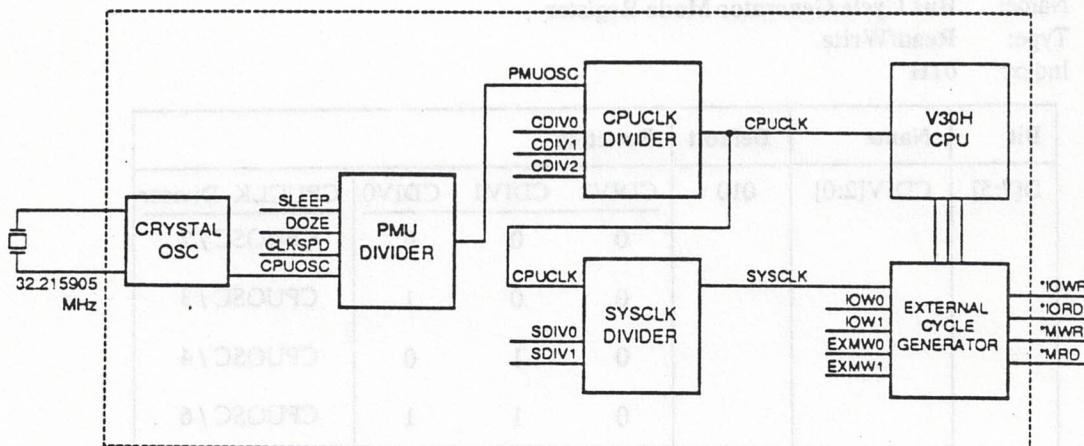


Figure 2.1-1

CPUCLK is derived from CPUOSC, and is configured through the BCG mode register at offset 01H. CDIV[2:0] select the divisor for CPUCLK. The default is CPUOSC/4.

CLK14/*16 selects the CPUOSC frequency of 32.21 MHz or 28.63 MHz. This option configures the internal divider chain to provide a PC-compatible 1.19MHz timer clock.

The LTCHADDR bit enables address latching for certain cycles. Latching of the address reduces switching on the external address bus. Reduced switching reduces the power consumption.

The BINH bit disables bus cycles for internal I/O accesses. This reduces activity on the external bus, thereby reducing power consumption.

SYSCLK is generated from CPUCLK and can equal CPUCLK or be divided 2, 3 or 4 times. SYSCLK is used for all I/O cycles and expansion memory cycles. The SDIV[1:0] bits control the generation of SYSCLK. Divisors of 1, 2, 3 and 4 are selectable. The default is CPUCLK/2.

The BCG Wait State Control 1 Register selects the number of wait states for the various I/O and memory subsystems. ROMW[1:0] control the number of wait states for ROMs connected to *ROMCE0 and *ROMCE1. RAMW[1:0] control the number of wait states for all RAM. IOW[1:0] control the number of SYSCLK wait states for all I/O cycles. EXMW[1:0] control the number of SYSCLK wait states for all expansion memory cycles.

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The BCG Mode register at offset 01H controls the frequency of the system clocks.

Name: Bus Cycle Generator Mode Register

Type: Read/Write

Index: 01H

Bit	Name	Default	Function			CPUCLK Divisor
D[7:5]	CDIV[2:0]	010	CDIV2	CDIV1	CDIV0	
			0	0	0	CPUOSC /2
			0	0	1	CPUOSC /3
			0	1	0	CPUOSC /4
			0	1	1	CPUOSC /6
			1	0	0	CPUOSC /8
			1	0	1	Reserved
			1	1	0	Reserved
			1	1	1	Reserved
D4	CLK14/*16	0	0 - Max. CPUCLK frequency = 16 Mhz (32Mhz input clock) 1 - Max. CPUCLK frequency = 14.3 Mhz (28.6 Mhz input clock)			
D3	LTCHADR	0	0 - Disable A[25:0] latches A[25:0] valid for all CPU cycles 1 - Enable A[25:0] latches A[25:11] invalid for DRAM cycles and A[25:20] only valid for PC Card or ROM1 cycles.			
D2	BINH	0	0 - Enable external bus for all bus cycles 1 - Disable external bus during accesses to internal devices			
D[1:0]	SDIV[1:0]	10	SDIV1	SDIV0	SYSCLK Divisor	
			0	0	CPUCLK /4	
			0	1	CPUCLK /3	
			1	0	CPUCLK /2	
			1	1	CPUCLK	

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Name: Bus Cycle Generator Wait State Control Register
 Type: Read/Write
 Index: 02H

Bit	Name	Default	Function		
D[7:6]	ROMW[1:0]	11	<u>ROMW1 ROMW0</u>		ROM Wait States
			0 0	0	0 CPUCLK Wait States
			0 1	1	1 CPUCLK Wait States
			1 0	2	2 CPUCLK Wait States
			1 1	3	3 CPUCLK Wait States
D[5:4]	RAMW[1:0]	01	<u>RAMW1 RAMW1</u>		RAM Wait States
			0 0	0	0 CPUCLK Wait States
			0 1	1	1 CPUCLK Wait States
			1 0	2	2 CPUCLK Wait States
			1 1	3	3 CPUCLK Wait States
D[3:2]	IOW[1:0]	01	IOW1 IOW0	I/O Wait States	
			0 0	0	0 SYSCLK Wait States
			0 1	1	1 SYSCLK Wait States
			1 0	2	2 SYSCLK Wait States
			1 1	3	3 SYSCLK Wait States
D[1:0]	EXMW[1:0]	00	<u>EXMW1 EXMW0</u>		Expansion Memory Wait States
			0 0	0	0 SYSCLK Wait States
			0 1	1	1 SYSCLK Wait States
			1 0	2	2 SYSCLK Wait States
			1 1	3	3 SYSCLK Wait States

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Name: Bus Cycle Generator Wait State Control 2 Register
 Type: Read/Write
 Index: 03H

Bit	Name	Default	Function	Decoding	Description
D[7:5]	PCAW[2:0]	111	PCW2	PC Card 'A' Wait States	
			0 0 0	0 CPUCLK Wait States	
			0 0 1	1 CPUCLK Wait States	
			0 1 0	2 CPUCLK Wait States	
			0 1 1	3 CPUCLK Wait States	
			1 0 0	4 CPUCLK Wait States	
			1 0 1	5 CPUCLK Wait States	
			1 1 0	6 CPUCLK Wait States	
			1 1 1	7 CPUCLK Wait States	
D4	Reserved	0	Reserved for future use		
D[3:1]	PCBW[2:0]	111	PC Card 'B' Wait States. Decoding is same as for PC Card 'A'.		
D0	PCIODLY	0	0 - No I/O command delay. 1 - PC Card I/O Command Delay one Bus Clock (SYSCLK) cycle		

BCG Wait State Control 2 register selects the number of wait states for PCMCIA access. Up to 7 CPUCLK wait states are selectable through the PCAW[2:0] bits. Each PC card may have a different wait state value, depending on the card information structure provided in every card.

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2.2 Memory Subsystem

The VG-230 is based on the NEC V30HL 8086 compatible core. Up to 1Mbyte of directly addressable memory space is supported by the V30HL. Through mapping registers the VG-230's memory manager provides access to over 256 Mbytes of address space. The 26 mapping registers allow mapping of various memory areas into the upper 512K of directly addressable 1M space. Each memory mapping register controls a 16K block of memory. Figure 2.2-1 illustrates the directly addressable 1M of memory and the mapping registers assigned to each 16K block when EMS is enabled.

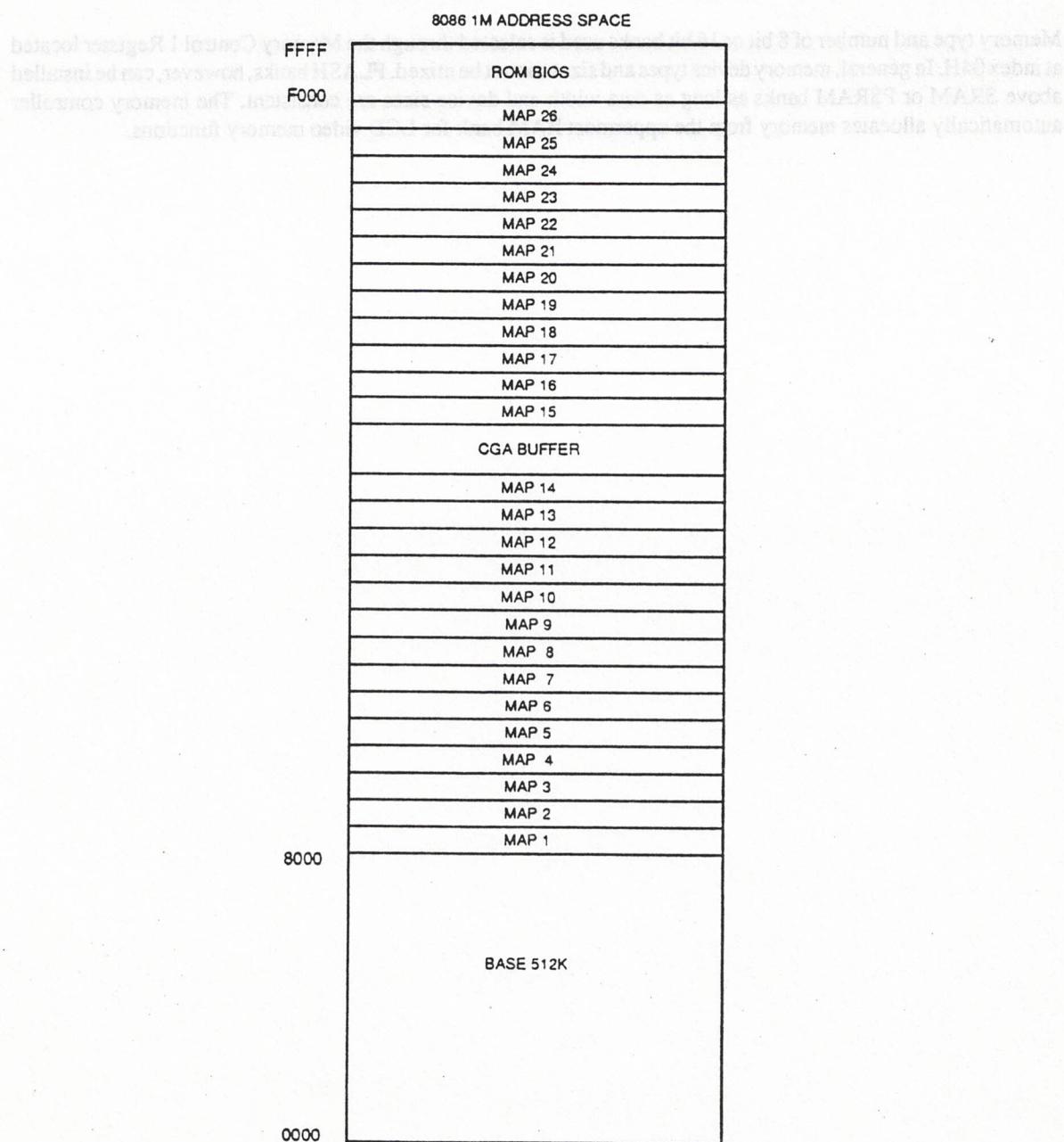


Figure 2.2-1

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The VG-230 bus architecture supports several classes of devices, using only one data bus D[15:0] and one address bus A[25:0]. Control signals such as *SIORD, *SIOWR, *ROMCE_x, *RAS_x, *CAS_x, and so forth, are generated as needed to enable the type of device being accessed in each cycle.

Each device type will be discussed in the next section. However, the following general rules apply. For an 8 bit memory bus, $D[7:0]$ is used. Address bits $A[N:0]$ are connected to the address inputs $A[N:0]$ of the memory devices. For a 16 bit memory bus, the even byte resides on $D[7:0]$ and the odd byte resides on $D[15:8]$. With the exception of DRAM, address bits $A[N+1:1]$ are connected to address inputs $A[N:0]$ of the memory devices. The DRAM address lines for a 16 bit memory bus are connected in the same way as for an 8 bit bus.

Memory type and number of 8 bit or 16 bit banks used is selected through the Memory Control 1 Register located at index 04H. In general, memory device types and sizes cannot be mixed. FLASH banks, however, can be installed above SRAM or PSRAM banks as long as data width and device sizes are consistent. The memory controller automatically allocates memory from the uppermost RAM bank for LCD video memory functions.

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DES-DV MEQAV
BNUICB NOGERTOM-SUS
SOMEREFBR JACMHOST

Name: **Memory Control Register**
 Type: **Read/Write**
 Index: **04H**

Bit	Name	Default	Function			
D7	MAPEN	0	0 - Disable Memory Mapping 1 - Enable Memory			
D[6:4]	BANK[2:0]	111	BANK2 BANK1 BANK0			No. of RAM Banks Installed
			0	0	0	1 Note: FLASH banks can be installed above SRAM or PSRAM banks as long as data widths and device sizes are consistent.
			0	0	1	2
			0	1	0	3
			0	1	1	4
			1	0	0	5
			1	0	1	6
			1	1	0	7
			1	1	1	8
D[3:0]	MTYP[3:0]	0H	MTYP3 MTYP2 MTYP1 MTYP0			
			0	0	0	0 32K x 8 SRAM
			0	0	0	1 128K x 8 SRAM
			0	0	1	0 512K x 8 SRAM
			0	0	1	1 32K x 8 PSRAM
			0	1	0	0 128K x 8 PSRAM
			0	1	0	1 512K x 8 PSRAM
			0	1	1	0 256K x 1/4 DRAM
			0	1	1	1 512K x 8 DRAM
			1	0	0	0 1M x 1/4 DRAM
			1	0	0	1 4M x 1/4 DRAM
			1	0	1	0 256K x 16 DRAM
			1	0	1	1 Reserved for future use

Other memory options are controlled through the Memory Control 2 register located at index 05H.

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Name: Memory Control 2 Register
Type: Read/Write
Index: 05H

Bit	Name	Default	Function
D7	RAMSIZ	0	0 - RAM is 16 bits wide 1 - RAM is 8 bits wide
D6	ROM0SIZ	X	Read Only bit reflecting state of ROM8/*16 pin 0 - BIOS ROM is 16 bits wide 1 - BIOS ROM is 8 bits wide
D5	ROM1SIZ	1	0 - Option ROM is 16 bits wide 1 - Option ROM is 8 bits wide
D4	SLWREF	0	0 - Normal Refresh Rate DRAM 1 - Slow Refresh Rate DRAM
D3	SRFDRAM	0	1 - Self Refresh DRAM. During Suspend, CAS before RAS cycles are not generated. Refresh is performed by DRAM
D[2:1]	Reserved	0	Reserved for future use
D0	*MRASDLY	0	0 - Delay mapper memory cycles until CPU T3 state 1 - Begin mapper memory cycles at CPU T2 state

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des-ov MEIGAV
EMIGAV NOGSTOM-SUB
BOMERBEE JACUHOT

2.2.1 ROM

The chip selects *ROMCE0 and *ROMCE1 can each control one ROM on an 8 bit bus or an even/odd address pair of 8 bit wide ROMs on a 16 bit bus, without glue logic.

MC8 is used as the *OE for 8 bit ROM arrays. For 16 bit arrays MC8 is used as *OEL for the lower 8 bits, and MC9 as *OEH for the upper 8 bits.

For the ROM space selected by *ROMCE0, chip selects for additional ROMs can be controlled by decoding the address lines A[19:0] which do not connect to the ROMs themselves, and enabling the decoder with *ROMCE0. Only 1 Mbyte of ROM is accessible in this space.

For the ROM space selected by *ROMCE1, chip selects for additional ROMs can be controlled by decoding the address lines A[25:0] which do not connect to the ROMs themselves, and enabling the decoder with *ROMCE1. Up to 64 Mbytes of ROM are accessible in this space.

The VG-230 imposes two timing requirements for a ROM read cycle: t121, which represents the time from valid *ROMCE_x output to valid data, and t119+t121, which represents the time from valid address output to valid data. The delay through three timing paths must satisfy these requirements, as shown in the following equations:

$$tB1 + tACC + tB2 < t119 + t121$$

$$tABY + tCE + tB2 < t119 + t121$$

$$tGY + tCE + tB2 < t121$$

tB1 and tB2 are the slowest edge propagation delay of buffers[†] B1 and B2, tABY is the select-to-low propagation delay of the decoder, and tGY is the enable-to-low propagation delay of the decoder. tACC and tCE are the address access and chip enable times of the ROM.

Note: $t121 = 0\text{ws}$ 16 MHz
If wait states are added
 $t121 = (t121 + (n * \text{CPUTCYC}))$

[†]Buffers are illustrated in Figure 2.2-6.

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TECHNICAL REFERENCE

VADEM VG-230
 SUB-NOTEBOOK ENGINE
 TECHNICAL REFERENCE

8 BIT ROM INTERFACE

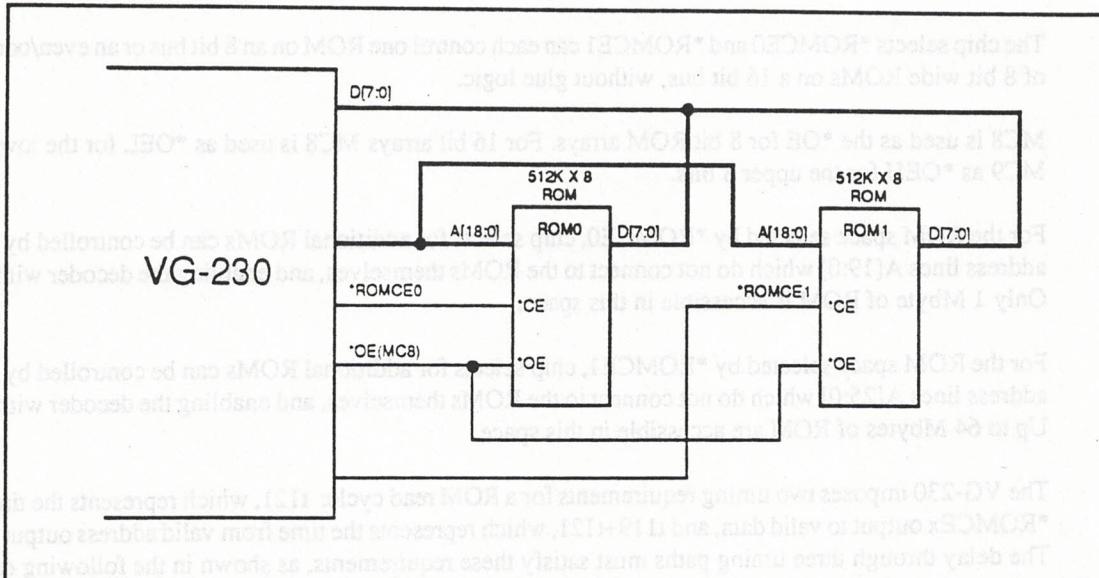


Figure 2.2-2

16 BIT ROM INTERFACE

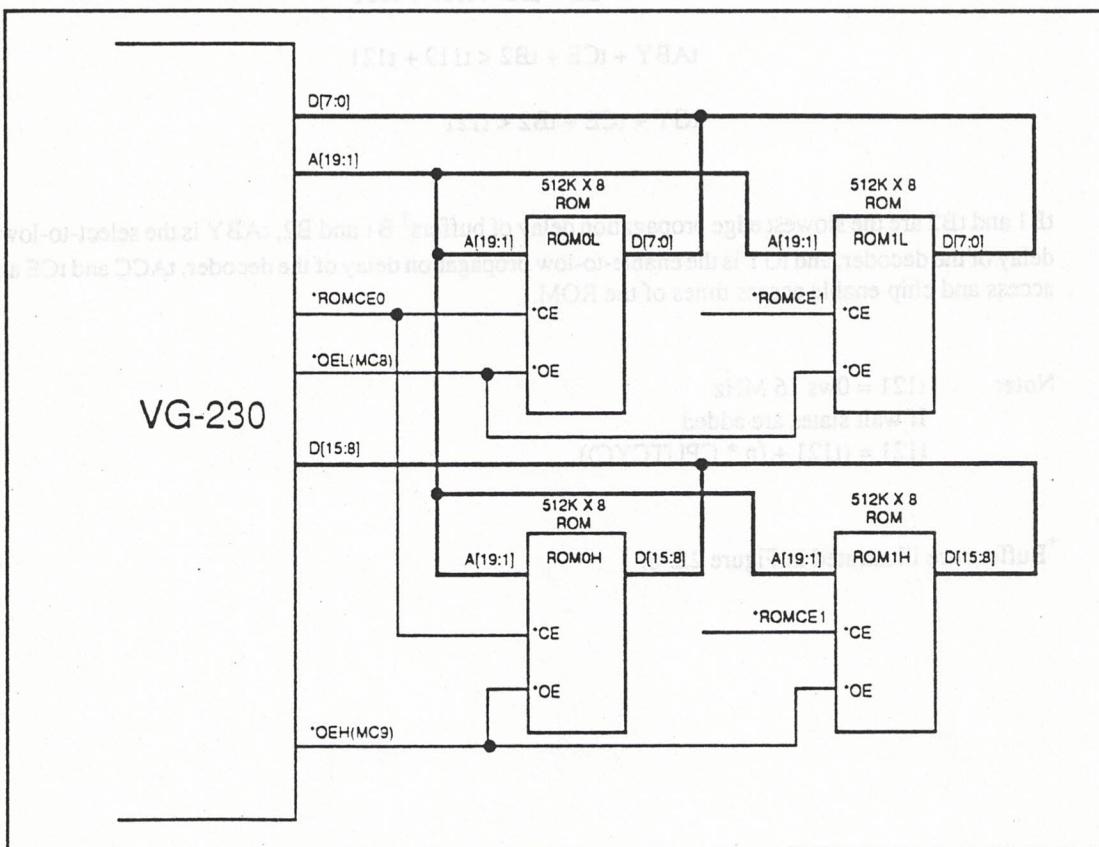


Figure 2.2-2A

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

2.2.2 ROM #0 (BIOS ROM)

ROM #0 can hold up to 1 Mbyte of BIOS and other code. *ROMCE0, the ROM #0 chip enable, is always asserted during CPU accesses to the BIOS area (F0000..FFFFH). Separately, ROM #0 can also be accessed via the VG-230 EMS mapping hardware.

The VG-230 saves power by limiting the activity of address lines during accesses to ROM #0. During direct access to the BIOS area, A[25:16] are held low. Therefore, BIOS code must be located in the bottom 64K of ROM #0. For EMS mapping, specifying PEN=1 and DTYP[2:0]=010 in any EMS Map High Byte Data Register will cause A[25:14] to come from that register and *ROMCE0 to be asserted. In this case, A[25:20] are held low. This is the source of the 1Mbyte ROM size limitation.

2.2.3 Static RAM (SRAM)

For an 8 bit bus, MC[7:0] drives the *CE pins on up to 8 RAMs. MC8 drives *OE and MC9 drives *WE on all RAMs. For a 16 bit bus, up to 12 bytewide RAMs are organized in even/odd address pairs. MC[5:0] each drive the *CE pins on one even/odd address pair. MC6 drives *OE and MC8 drives *WE on all even RAMs, while MC7 drives *OE and MC9 drives *WE on all odd RAMs.

The VG-230 imposes two timing requirements for an SRAM read cycle: t104, which represents the time from valid *CSx output to valid data, and t100+t104, which represents the time from valid address output to valid data. The delay through two timing paths must satisfy these requirements, as shown in the following equations:

$$tB3 + tACC + tB5 < t100 + t104$$

$$tB4 + tCE + tB5 < t104$$

tB3 and tB5 are the slowest propagation delay of buffers[†] B3 and B5, and tB4 is the high to low propagation delay of buffer[†] B4. tACC and tCE are the address access and chip enable access times of the RAM.

SRAM write cycles are CE controlled. Most systems that satisfy read timing will also satisfy write timing, but where buffers[†] are used, the following equation should be verified:

$$t125 + tB4(cs) - tB4(we) > tWP$$

tB4(cs) is the low to high propagation delay of B4, and tB4(we) is the high to low propagation delay of B4.

[†]Buffers are illustrated in Figure 2.2-6.

VADEM VG-230
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TECHNICAL REFERENCE

VADEM AG-530
 SUB-NOTEBOOK ENGINE
 TECHNICAL REFERENCE

8 BIT SRAM INTERFACE

(MOS 2016) & MOS 5.5

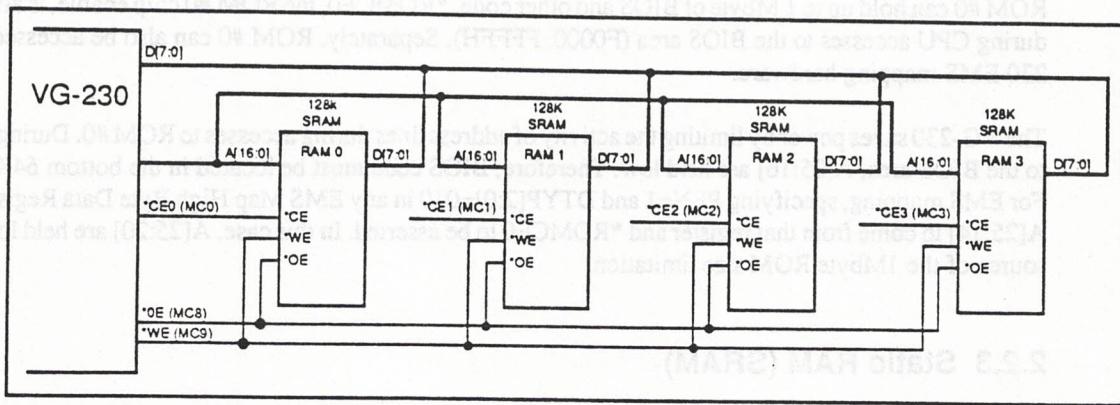


Figure 2.2-3

16 BIT SRAM INTERFACE

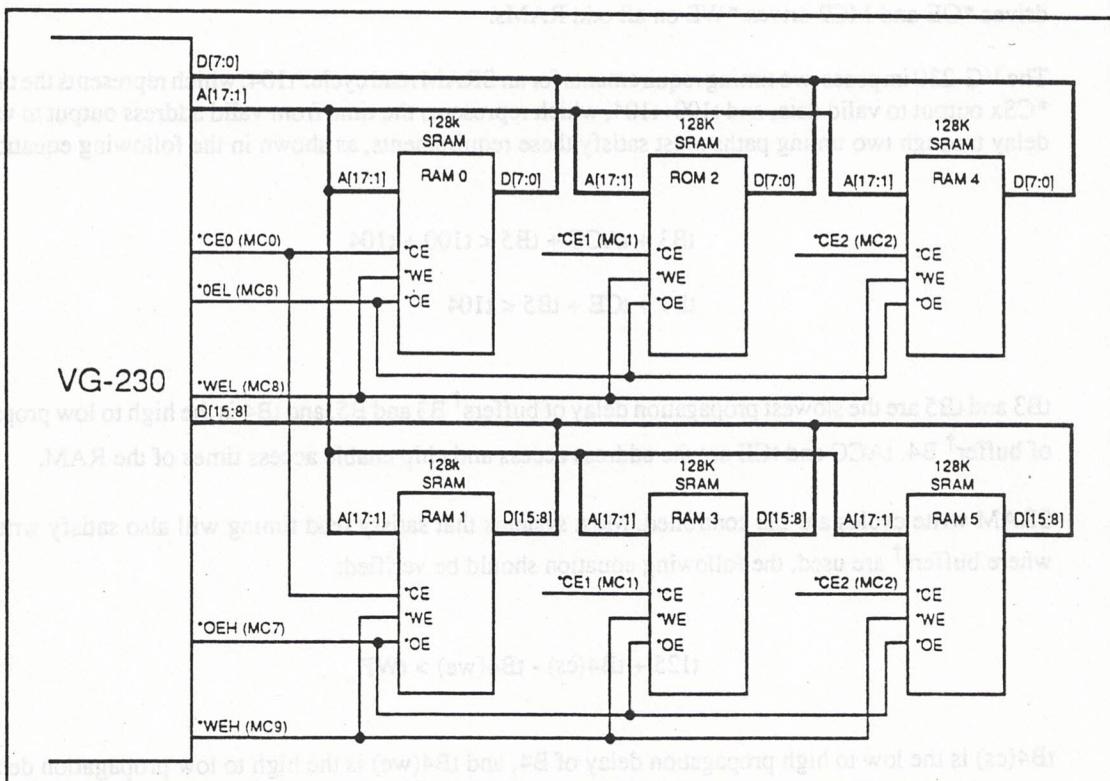


Figure 2.2-3A

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

2.2.4 Pseudo Static RAM (PSRAM)

For an 8 bit bus, MC9 drives *WE on all RAMs. MC[6:0] drive *CE on up to 7 RAMs. For RAMs with a combined *RFSH/OE pin, MC6 is available to drive *CE on a sixth RAM, MC7 drives *RFSH/OE on even numbered RAMs 0, 2, 4, and 6, while MC8 drives *RFSH/OE on odd numbered RAMs 1, 3, and 5. For RAMs with separate *RFSH and *OE pins, MC6 drives *RFSH on even numbered RAMS 0, 2, and 4, while MC7 drives *RFSH on odd numbered RAMS 1, 3, and 5. MC8 drives *OE on all RAMs.

For a 16 bit bus, MC6 drives *OE and MC8 drives *WE on even addressed RAMs, while MC7 drives *OE and MC9 drives *WE on odd addressed RAMs. MC[3:0] drive *CE on up to 4 odd/even addressed RAM pairs. For RAMs with a combined *RFSH/OE pin, MC[5:4] are available to drive *CE on a fifth and sixth RAM pair. For RAMs with separate *RFSH and OE pins, MC4 drives *RFSH on the odd addressed RAMs and MC5 drives *RFSH on the even addressed RAMs.

The VG-230 imposes three timing requirements for a PSRAM read cycle: t100, which represents the address to *CS setup time; t104, which represents the time from valid *CSx output to valid data; and t103, which represents the time from valid *OEx output to valid data.

The delay through three timing paths must satisfy these requirements, as shown in the following equations:

$$t100 + tB4(cs) - tB3 > tAS$$

$$tB4(cs) + tCEA + tB5 < t104$$

$$tB4(oe) + tOEA + tB5 < t104$$

tB3 and tB5 are the slowest propagation delay of buffers[†] B3 and B5, and tB4 is the high to low propagation delay of buffer[†] B4. The (cs) and (oe) notation refers to which signal is being buffered[†]. tAS, tCEA and tOEA are the address setup, address access and output enable access times of the RAM.

The first equation is exceptional in that t100 and tAS are specified as minimum values, while all of the other specifications are maximum values. Representative minimum values for t100 and tAS are 5ns and 0ns respectively. This implies that tB4(cs) - tB3 cannot be more negative than -5ns, or the equation will not be satisfied. In practice, this means that buffer[†] differential delay is critical, and if buffer[†] 4(cs) cannot be guaranteed to be significantly slower than buffer[†] 3, then buffer[†] 3, or buffers[†] 3 and 4(cs), must not be used.

Most systems that satisfy read timing will also satisfy write timing, but where buffers[†] are used, the following equation should be verified:

$$t125 + tB4(cs) - tB4(we) > tCWL$$

tB4(cs) is the low to high propagation delay of B4, and tB4(we) is the high to low propagation delay of B4.

[†]Buffers are illustrated in Figure 2.2-6.

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

8 BIT PSRAM INTERFACE

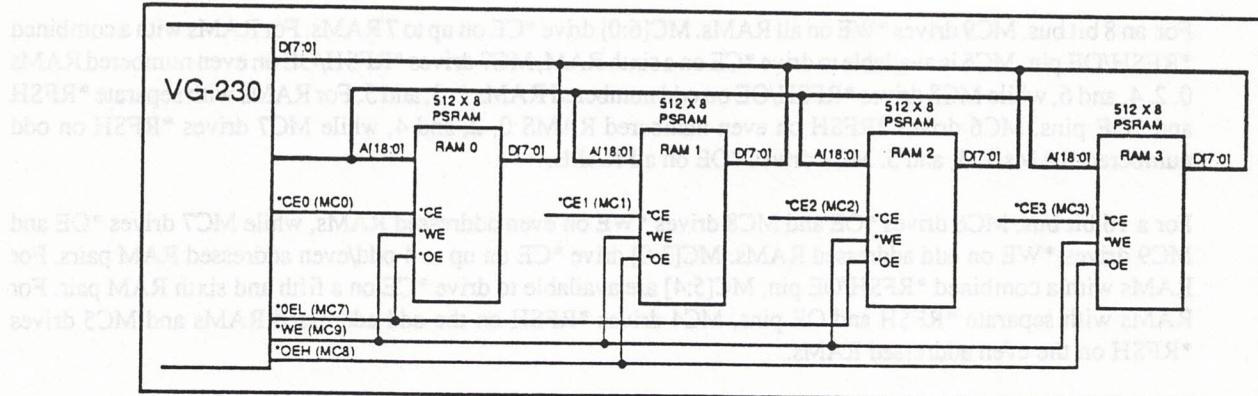


Figure 2.2-4

16 BIT PSRAM INTERFACE

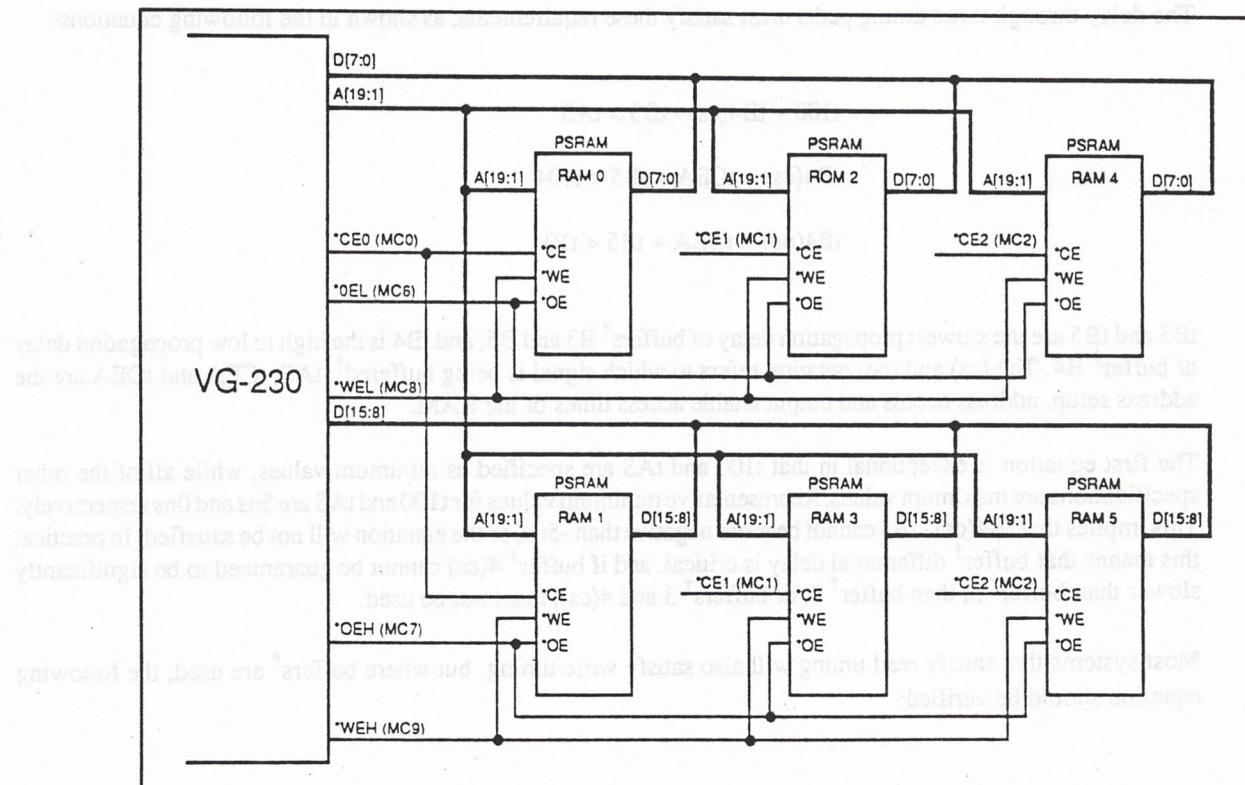


Figure 2.2-4A

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

2.2.5 Dynamic RAM (DRAM)

For an 8 bit bus, MC0:5 each drive *CAS on one bank. MC6 and MC7 drive *RAS on even and odd numbered banks respectively. MC8 drives *OE (if needed) and MC9 drives *WE.

For a 16 bit bus, MC0:4 each drive *CAS on one even/odd addressed bank pair. MC5 drives *RAS and MC8 drives *WE to the even addressed banks, while MC6 drives *RAS and MC9 drives *WE to the odd addressed banks. MC7 drives *OE (if needed) to all RAMs.

For by-16 DRAMs, MC[5:0] each drive *RAS on one even/odd addressed bank pair. MC6 drives *CAS to the even addressed banks, while MC7 drives *CAS to the odd addressed banks. MC8 drives *OE (if needed) and *MC9 drives *WE to all RAMs.

The most critical requirements of the VG-230 for a DRAM read cycle are: t100, which represents the address to *RASx setup time; t114, which represents the time from valid *RASx output to valid data; and t114-t112, which represents the time from valid *CASx output to valid data.

The delay through three timing paths must satisfy these requirements, as shown in the following equations:

$$t100 + tB4(ras) - tB3 > tASR$$

$$tB4(ras) + tRAC + tB5 < t114$$

$$tB4(cas) + tCAC + tB5 < t114 - t112$$

tB3 and tB5 are the slowest propagation delay of buffers B3 and B5, and tB4 is the high to low propagation delay of buffer B4. The (ras) and (cas) notation refers to which signal is being buffered. tASR, tRAC and tCAC are the row address setup, RAS access and CAS access times of the RAM.

The first equation is exceptional in that t100 and tASR are specified as minimum values, while all of the other specifications are maximum values. Representative minimum values for t100 and tASR are 5 ns and 0 ns respectively. This implies that tB4(ras) - tB3 cannot be more negative than -5 ns, or the equation will not be satisfied. In practice, this means that buffer differential delay is critical, and if buffer 4(ras) cannot be GUARANTEED to be significantly slower than buffer 3, then buffer 3, or buffers 3 and 4(ras), must not be used. A similar situation exists for tASC, the column address setup time. The relevant equation for this parameter is:

$$t111 + tB4(cas) - tB3 > tASC$$

The margins are not nearly so tight here since representative minimum values for t111 and tASC are 20 ns and 0 ns respectively. tASC should be easy to satisfy if 74ACT buffers, or no buffers, are used.

The timing for the DRAM tRAH spec should also be checked where buffering is used. The equation is:

$$t110 + tB3 - tB4(ras) > tRAH$$

Representative minimum values for t110 and tRAH are 30 ns and 15 ns respectively. Unless tB4(ras) is excessively enlarged in order to satisfy other specifications, tRAH should be easy to satisfy if 74ACT buffers, or no buffers, are used.

DRAM write cycles are early write cycles. Most systems that satisfy read cycle timing will also satisfy write timing, but where buffering is used the following equations should be verified:

$$t118 + tB4(cas) - tB4(we) > tWCS$$

$$t116 + tB4(cas) - tB5 > tDS$$

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

VADEM VG-230
 SUB-NOTEBOOK ENGINE
 TECHNICAL REFERENCE

8 BIT DRAM INTERFACE

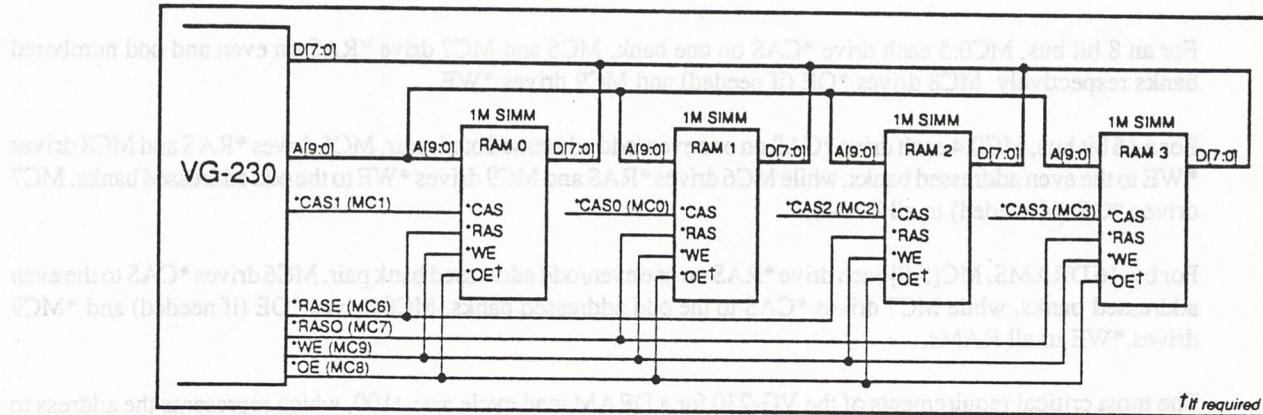


Figure 2.2-5

16 BIT DRAM INTERFACE

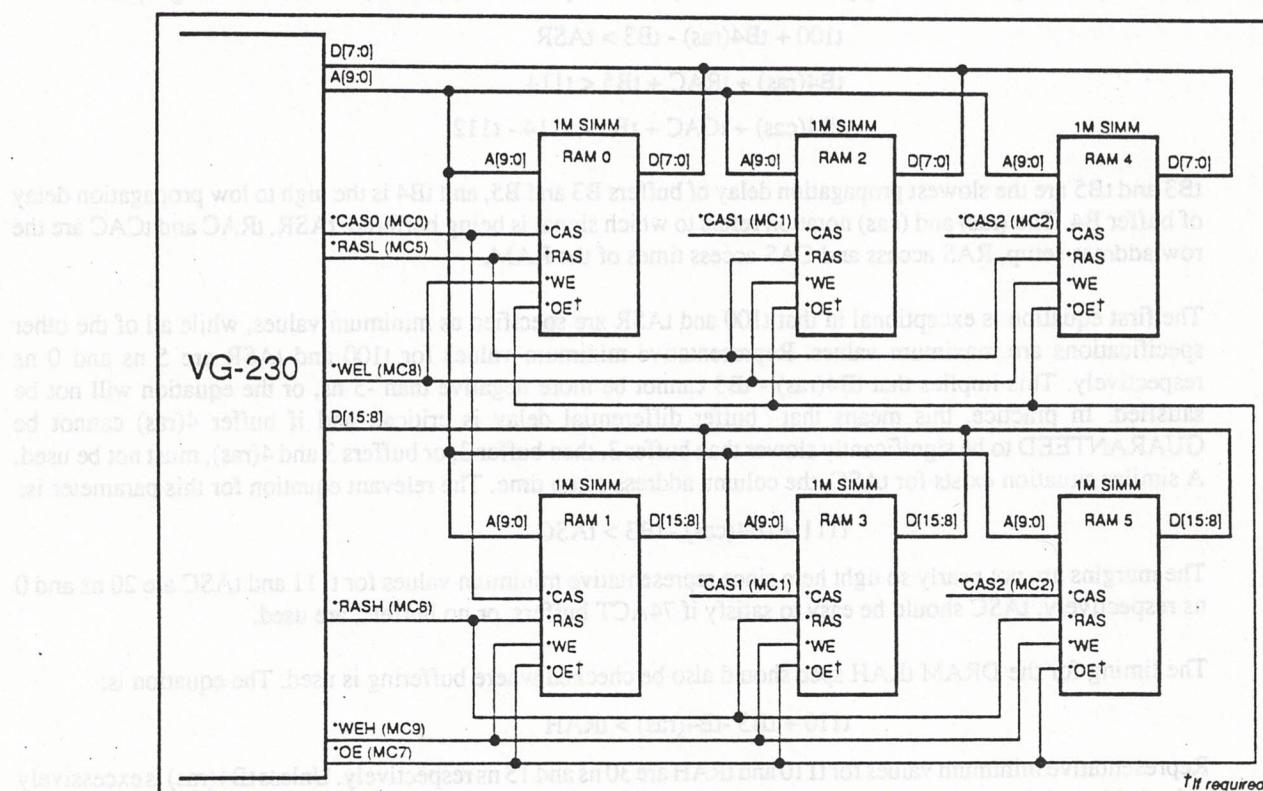


Figure 2.2-5A

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

OS-3V MCGAV
EINOMS NOGERTOM-SRIS
SOMERFUR JACINTH

2.2.6 Implementing the VG-230 Memory Subsystem

After completing a rough initial design of a VG-230 system, calculations must be performed to determine the memory speed requirements and whether buffering is required. This may be an iterative process, depending on the constraints of the design. Buffering may be necessary if the capacitive loading becomes large, but this will affect cost and/or performance.

There is also the possibility that a memory device (typically ROM) could be so slow to tristate its output when deselected that contention occurs at the beginning of a write cycle which follows a read cycle. This is not a problem with 5 volt operation using commonly available ROMs, however although buffering should alleviate this problem, a better alternative would be to select a different memory.

Capacitive Loading

The first task is to calculate the total capacitance on each signal in the A[25:0], D[15:0], and MC[9:0] bus by summing the I/O capacitance of all devices connected to that line, including those that may be plugged into XT bus or PCMCIA card connectors, plus the parasitic capacitance of the PC board traces, IC sockets, and connectors.

Notice that the loading on different signals within a bus will vary, and for this reason the VG-230 is specified with higher capacitive loads on the most heavily loaded lines. Capacitive loading may become a problem if the total capacitance exceeds a certain limit. To determine this limit, check the data sheets for every device which drives that bus line for the capacitive load at which the device's maximum delay is guaranteed. The device with the smallest capacitive load specification is the weak link, and its rated capacitive load is the limiting value for that bus line.

If the capacitive load limit is exceeded, the first step is to try to reduce the total capacitance. Consider using fewer memory chips by selecting denser parts. A 16 bit organization can also help by spreading the data bus loading over twice as many signals.

If this fails, try to determine the effect of the excessive loading. Most manufacturers do not publish information regarding speed as a function of capacitive load, but they may be able to provide some guidelines. For example, if the capacitive load in your design is 150 pF, which is within the specs for all parts you have used except for a RAM rated for a 100 pF load, you may find that the access time of the RAM is reduced by 10 ns due to the additional 50 pF. It may turn out that the additional 10 ns does not cause a problem, or if it does, you may be able to spec a faster part. Or consider adding a wait state for that portion of memory if its performance is not critical; this could result in a cost savings if the wait state allows use of a slower part. Note, however, that the memory bank which contains video memory must be accessed without wait states.

As a last resort, buffers may be required. In this situation, the objective is to minimize the number of buffers and to place them such that their presence does not degrade the memory timing. It is difficult to provide specific recommendations because the memory mix and performance constraints of VG-230 systems are very diverse, however it is possible to make general suggestions. If a lower parts count is more important than performance, consider an 8 bit data bus: in some cases, this may require fewer components. If performance is of more importance, connect critical bus paths directly from the VG-230 to the memory devices without interposing buffers, and use the buffers to isolate slower memory sections from the critical portions of the bus.

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Timing Calculations

The next step is the timing calculations. Sections 2.2.1 through 2.2.5 discuss timing calculations for different types of memory. Notice that a great number of specifications that appear in the memory data sheets are not mentioned here. This is because the VG-230 has been designed to provide such generous timing margins for specifications that are not mentioned that only a quick check should be needed to verify compatibility. This is true even for slow devices (100 ns SRAM and DRAM, 120 ns PSRAM). The sections should be checked carefully. The discussion assumes that all external logic has propagation delays comparable to 74ACT series. 5 volt operation is also assumed, and all external specifications such as loading are satisfied.

The calculations shown are for a worst-case very large system with decoders and buffers in many places, as shown in figure 2.2-6. Delete all delays from the formulas that correspond to decoders or buffers that are not present in your system.

The formulas shown are inequalities that specify a system delay on the left which must be less than a maximum VG-230 requirement on the right, or greater than a minimum memory requirement on the right. Satisfying the inequality with a margin of 1 nanosecond, for example, represents good mathematics, but poor design practice. Within reason, build in as much design margin as can be justified by business considerations.

There are other factors that affect the timing calculations which may be significant if the timing margins are tight. These include delays introduced by series termination resistors and by the length of traces on the PC board. Termination resistor delay will be less than the RC time constant of the termination resistance times the load capacitance. The delay introduced by a trace over a ground plane can be approximated by transmission line methods, and will be equal to the square root of LC, where L is the inductance of the trace (a suitable approximation is 1 nanohenry per millimeter) and C is its capacitance as calculated in section 2.1, assuming that the capacitive loads are evenly distributed along its length.

Figure 2.2-6 shows a simplified schematic of a VG-230 with very large memory arrays and buffering.

Figure 2.2-6 shows a simplified schematic of a VG-230 with very large memory arrays and buffering. The schematic illustrates a complex memory system architecture. It features two main memory blocks, each consisting of a RAM array and a ROM array. These are interconnected via bidirectional buses. The RAM arrays are connected to a central bus, while the ROM arrays are connected to another. Address and control signals are distributed across the system, with various buffers and decoders managing signal flow between the different components. Power and ground connections are also clearly marked throughout the diagram.

The schematic is a simplified representation of the VG-230's internal structure, focusing on the memory subsystem. It highlights the use of large memory arrays and sophisticated buffering and decoding logic to manage data flow between the different memory types. The diagram serves as a key reference for understanding the system's memory architecture and timing requirements.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

CGS-3V MEDAV
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

LARGE ARRAY INTERFACE

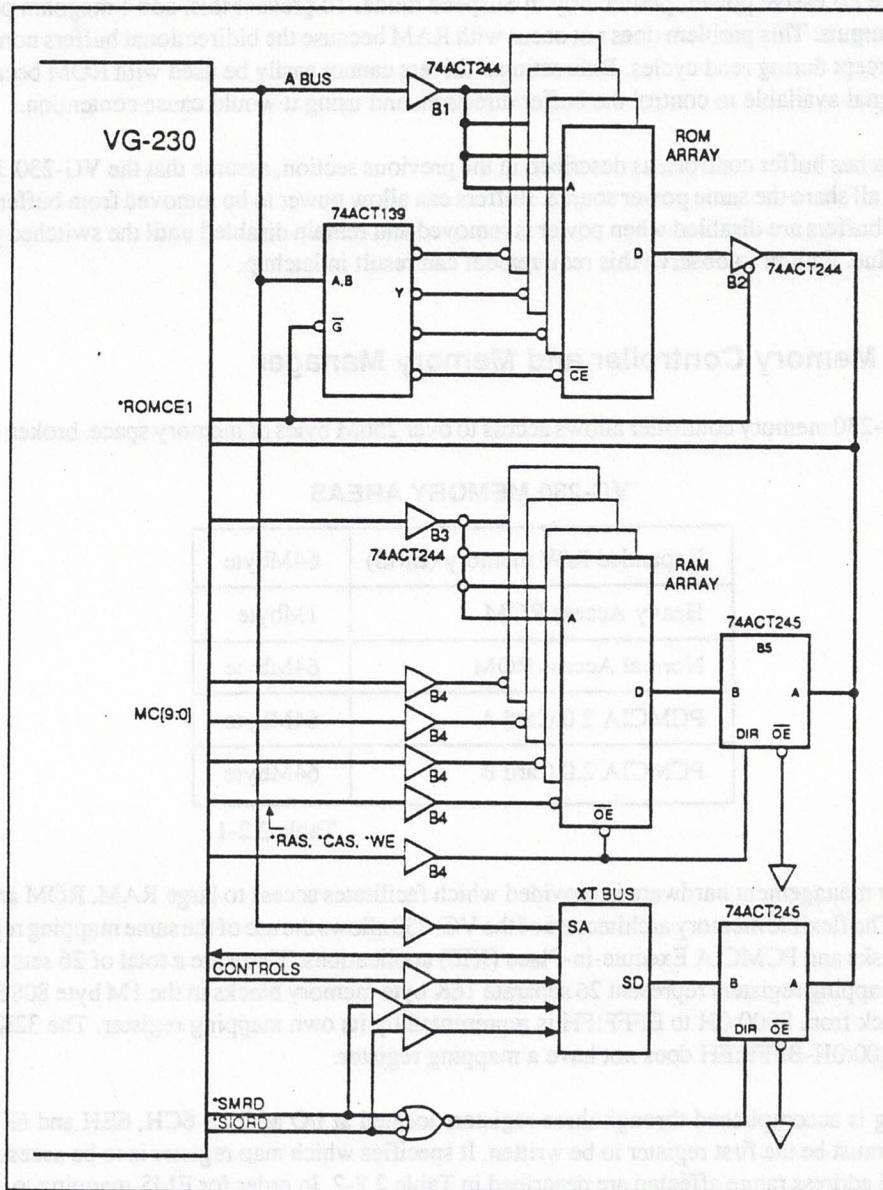


Figure 2.2-6

In many cases, data bus buffers can be controlled by VG-230 outputs without additional glue logic.

ROM data outputs to the D bus can be buffered by a 74ACT244. The ROMs controlled by *ROMCE0 should be connected to one buffer, and those controlled by *ROMCE1 should be connected to another buffer. The buffer *OE inputs are then directly connected to *ROMCE0 or *ROMCE1 as appropriate.

SRAM, PSRAM and DRAM D bus buffering is done with a 74ACT245. Connect the A side of the buffer to the VG-230 and the B side to the memory array. Ground the *OE pin of the buffer, and connect the DIR pin to the MC[9:0] output of the VG-230 which is acting as the *OE for the memory array.

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The data bus between the ROM and its buffer will float between ROM accesses. This could cause the buffer to consume excessive power, particularly in Suspend mode. To prevent this, add 1 megohm pullup resistors on the ROM outputs. This problem does not occur with RAM because the bidirectional buffers normally drive the RAM array except during read cycles. Bidirectional drivers cannot easily be used with ROM because *ROMCE is the only signal available to control the buffer direction, and using it would cause contention.

The data bus buffer controls, as described in the previous section, assume that the VG-230, buffers, and buffered devices all share the same power source. Buffers can allow power to be removed from buffered devices, provided that the buffers are disabled when power is removed and remain disabled until the switched power has risen to its final value. Failure to observe this requirement can result in latchup.

2.2.7 Memory Controller and Memory Manager

The VG-230 memory controller allows access to over 256M bytes of memory space, broken down into five areas:

VG-230 MEMORY AREAS

Expanded R/W memory (EMS)	64Mbyte
Heavy Access ROM	1Mbyte
Normal Access ROM	64Mbyte
PCMCIA 2.0 Card A	64Mbyte
PCMCIA 2.0 Card B	64Mbyte

Table 2.2-1

Memory management hardware is provided which facilitates access to large RAM, ROM and PCMCIA PC card arrays. The flexible memory architecture of the VG-230 allows the use of the same mapping registers for both EMS, ROM disks and PCMCIA Execute-in-Place (XIP) applications. There are a total of 26 sets of mapping registers. These mapping registers represent 26 separate 16K byte memory blocks in the 1M byte 8086 address range. Each 16K block from 8000:0H to EFFF:FH is represented by its own mapping register. The 32K video memory area from B800:0H-BFFF:FH does not have a mapping register.

Mapping is accomplished through three registers located at I/O address 6CH, 6EH and 6FH. The Map address register must be the first register to be written. It specifies which map register is to be accessed. Valid values and the 8086 address range affected are described in Table 2.2-2. In order for EMS mapping to occur, mapping must be globally enabled via the MAPEN bit of Memory Control 1 Register at index 04H.

... angel ring laptop with the model number DCS-DV and features a CD-ROM and a 1.44MB floppy disk drive. The system includes a 13.3" active matrix LCD screen with a resolution of 1024x768 pixels. The keyboard is a full-size 101-key layout with integrated numeric keypad. The mouse is a standard 3D scrollball mouse. The system also includes a built-in speaker and a microphone. The power supply is a 19V 4.7A AC adapter. The system is designed for portability and is suitable for use as a mobile computing platform.

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DCS-DV MEGAV
 DIVISIONS ROGERSVILLE-SUG
 SOUTHERN HIGHWAY MACHINERY

Name: Map Address Register

Type: Read/Write

I/O Address: 6CH

Bit	Name	Default	Function
D[7:2]	PA[7:2]	00H	Page address of the Mapping register to access through the Map Data registers. Valid entries are: 80, 84, 88, & 8C 90, 94, 98, & 9C A0, A4, A8, & AC B0 & B4 C0, C4, C8, & CC D0, D4, D8, & DC E0, E4, E8, & EC
D[1:0]	N/U	0	Not used. Ignored when written and zero when read.

H8C - 15 memory qM	H08 - 8 memory qM
87780 - 0.0000	77770 - 0.0000
H0C - 15 memory qM	H0A - 8 memory qM
87780 - 0.0000	7776A - 0.0000
H0F - 15 memory qM	HAA - 16 memory qM
87783 - 0.0000	777FA - 0.000A
H48 - 15 memory qM	H8A - 11 memory qM
87783 - 0.0000	777FA - 0.000A
H89 - 25 memory qM	H0A - 15 memory qM
87783 - 0.0000	777FA - 0.000A
H0F - 15 memory qM	H08 - 15 memory qM
87782 - 0.0000	777F8 - 0.0000

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

Memory Mapping Register Description

Map register 1 - 80H 8000:0 - 83FF:F	Map register 14 - B4H B400:0 - B7FF:F
Map register 2 - 84H 8400:0 - 87FF:F	Map register 15 - C0H C000:0 - C3FF:F
Map register 3 - 88H 8800:0 - 8BFF:F	Map register 16 - C4H C400:0 - C7FF:F
Map register 4 - 8CH 8C00:0 - 8FFF:F	Map register 17 - C8H C800:0 - CBFF:F
Map register 5 - 90H 9000:0 - 93FF:F	Map register 18 - CCH CC00:0 - CFFF:F
Map register 6 - 94H 9400:0 - 97FF:F	Map register 19 - D0H D000:0 - D3FF:F
Map register 7 - 98H 9800:0 - 9BFF:F	Map register 20 - D4H D400:0 - D7FF:F
Map register 8 - 9CH 9C00:0 - 9FFF:F	Map register 21 - D8H D800:0 - DBFF:F
Map register 9 - A0H A000:0 - A3FF:F	Map register 22 - DCH DC00:0 - DFFF:F
Map register 10 - A4H A400:0 - A7FF:F	Map register 23 - E0H E000:0 - E3FF:F
Map register 11 - A8H A800:0 - ABFF:F	Map register 24 - E4H E400:0 - E7FF:F
Map register 12 - ACH AC00:0 - AFFF:F	Map register 25 - E8H E800:0 - EBFF:F
Map register 13 - B0H B000:0 - B3FF:F	Map register 26 - ECH EC00:0 - EFFF:F

Table 2.2-2

VADEM VG-230

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TECHNICAL REFERENCE

The second register at I/O address 6EH is the Map Low Byte Data Register. This byte represents bits 14 to 21 of the mapped address.

Name: **Map Low Byte Data Register**

Type: **Read/Write**

I/O Address: **6EH**

Bit	Name	Default	Function
D[7:0]	MAP[21:14]	00H	Least significant byte of the memory map address

The third register at I/O address 6FH is the Map High Byte Data Register. This byte contains bits 22 to 25 of the mapped address.

Name: **Map High Byte Data Register**

Type: **Read/Write**

I/O Address: **6FH**

Bit	Name	Default	Function	Page Memory Device Type		
D7	PEN	0	0 - Disable mapping for this page 1 - Enable mapping for this page			
D[6:4]	DTYP[2:0]	000	DTYP2 DTYP1 DTYP0	None (external bus cycle)	RAM (specified by MTYP[3:0])	ROM #0
			0 0 0			ROM #1
			0 0 1			PC Card A
			0 1 0			PC Card B
			0 1 1			Reserved
			1 0 0			
			1 0 1			
			1 1 0			
			1 1 1			
D[3:0]	MAP[25:22]	0H	Most significant nibble of memory map address			

VADEM VG-230

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The DTYP[2:0] bits specify which type of memory is selected. RAM, ROMCS0, ROMCS1, PCMCIA A, PCMCIA B or external memory are the available selections.

Also included in this register is a mapping enable bit called PEN. When this bit is cleared, mapping for the selected mapping register is disabled.

2.2.8 Memory Mapping Examples

The following example illustrates the flexibility built into the VG-230 memory manager. Figure 2.2-7 represents a memory design based on a medium sized VG-230 system. This system is based on 1M byte of ROM for BIOS and DOS. 1M byte of RAM and a 1Mbyte PCMCIA card for applications code. The block to the left represents the 1Mbyte address space of the 8086.

The three blocks to the right represent the three types of physical memory available. The base 512K of 8086 address space is always mapped to the bottom of the RAM array. The 32K bytes of CGA BUFFER is always mapped to the top 32K bytes of the RAM array. The ROM BIOS (64K bytes) is always mapped to the bottom 64K of the heavy access ROM array (ROMCE0).

2.2.9 Flash ROM Support

The VG-230 can support FLASH EPROM in its ROM, in its main memory or in both. A FLASH programming voltage generator (VPP) and associated control are required. Control of the VPP voltage can be supplied through one of the GPIO pins (see section 2.14). It is up to the BIOS, driver or application software to supply the necessary programming algorithm to program the FLASH devices. When using FLASH EPROM in the ROM array, it must be of the same data width as all other ROMs/EPROMs connected to its chip-enable (*ROMCE0 or *ROMCE1). The FLASH EPROM must also be no wider than the main memory array. Memory writes to any ROM address automatically generate a modified MWR strobe that is compatible with FLASH.

When FLASH ROM is used in the main memory array, it must be of the same size and data width as the RAM devices. DRAM cannot be mixed with FLASH EPROM because its addressing method is fundamentally incompatible with FLASH's row/column addressing. The VG-230 reads the BANK bits of the Memory Control 1 Register (04H) in order to position video memory at the top of the main memory array. Therefore, FLASH, if used, must be placed above the top bank of RAM and the BANK bits set so as not to include the FLASH. For example, if a system has two banks of PSRAM, FLASH can be located in banks 3 and above. The BANK bits must be programmed to the binary value corresponding to one less than the number of PSRAM banks (2-1=1 or 001).

The following table illustrates the definitions of MC[9:6] for the various memory combinations:

Memory Combination	Pin Definitions During ROM Access			
	MC6	MC7	MC8	MC9
Any RAM type and width, 8 bit ROM BY16 DRAM, 16 bit ROM	n/a	n/a	*OE	*WE
Any 8 bit RAM, 16 bit ROM	n/a	n/a	*OEL	*OEH
16 bit SRAM/PSRAM, 16 bit ROM	*OEL	*OEH	*WEL	*WEH
16 bit DRAM, 16 bit ROM	n/a	*OE	*WEL	*WEH

Table 2.2-3

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

020-MEDIAV
SUB-NOTEBOOK-ENGINE
TECHNICAL REFERENCE

MEMORY MAPPING EXAMPLE

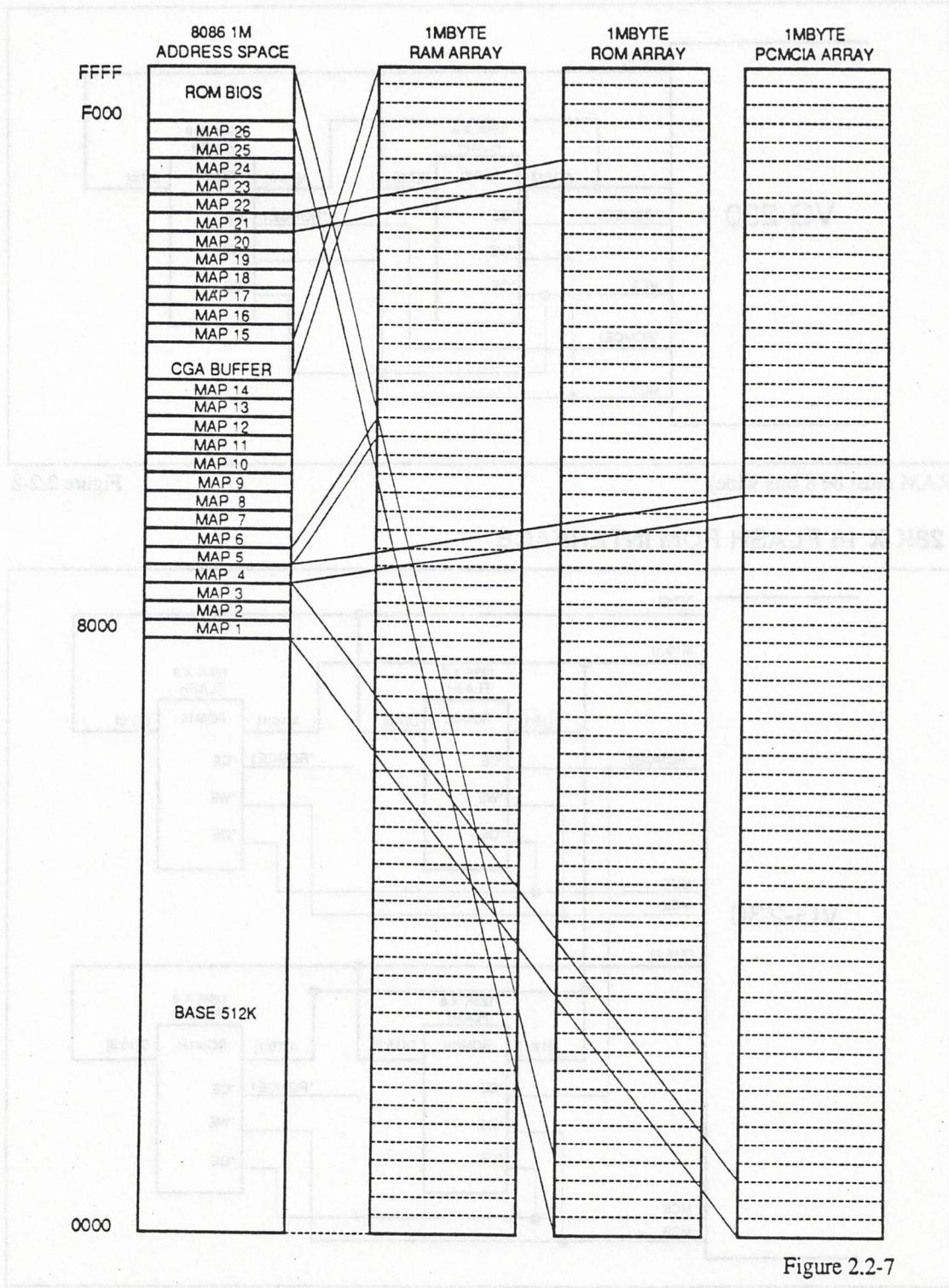
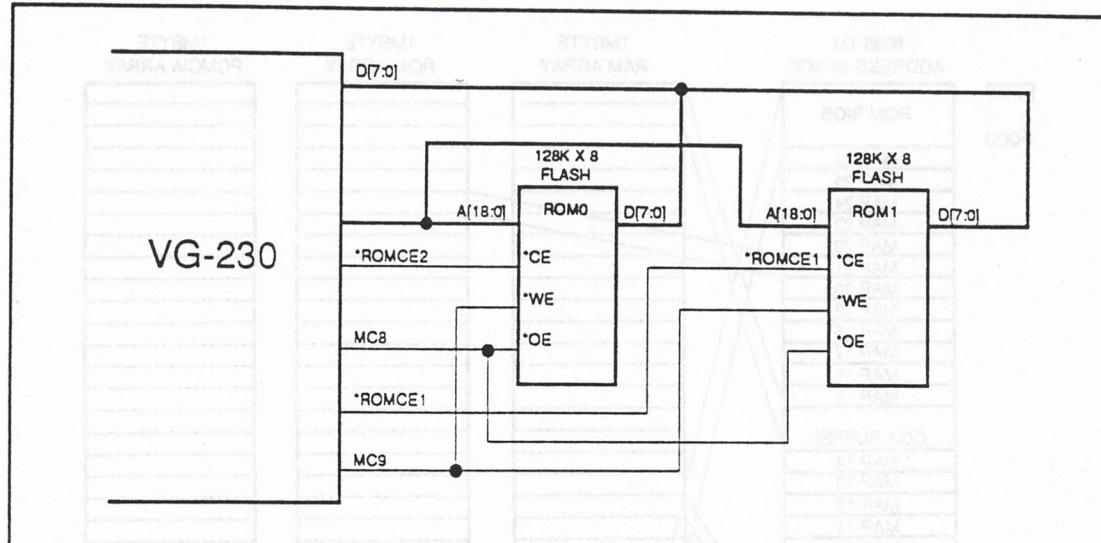


Figure 2.2-7

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

VADEM VG-230
 SUB-NOTEBOOK ENGINE
 TECHNICAL REFERENCE

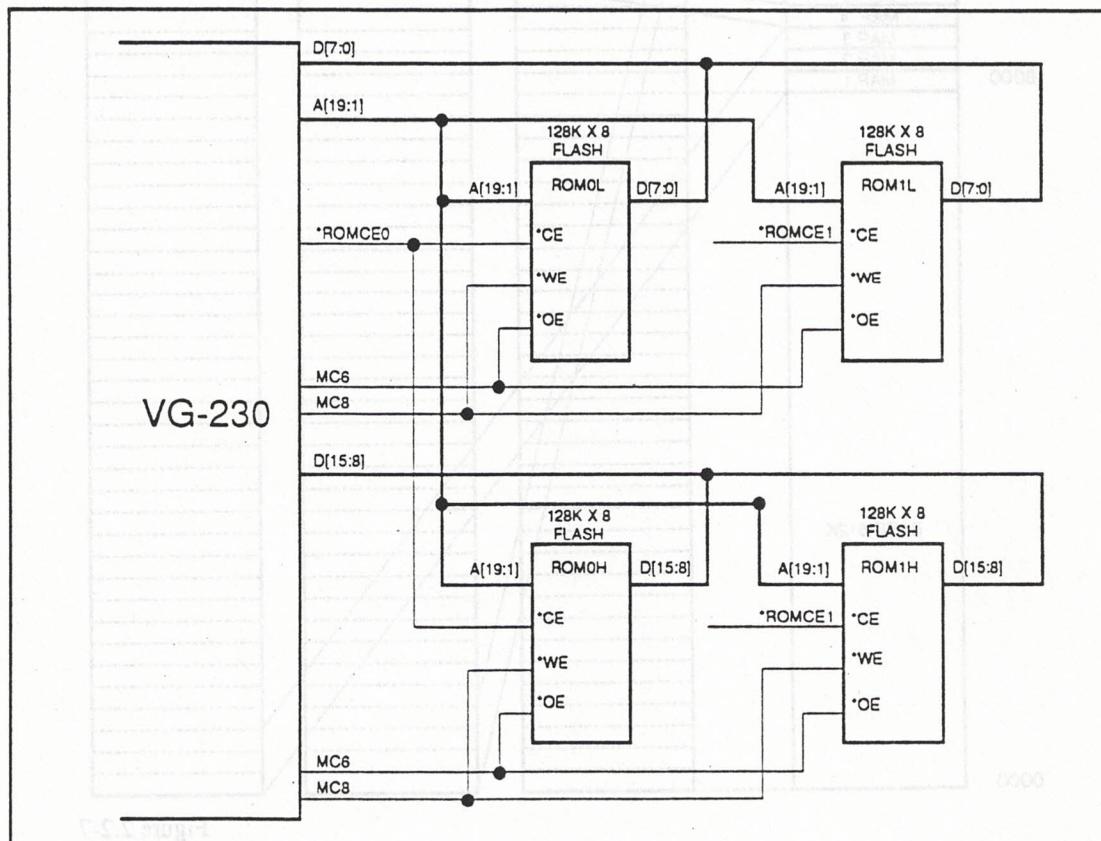
128K X 8 FLASH ROM INTERFACE



(RAM must be 8 bits wide)

Figure 2.2-8

128K X 16 FLASH ROM INTERFACE



(RAM must be 16 bits wide)

Figure 2.2-8A

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

In this example, mapping registers 1, 2 and 3 are mapped to the bottom 3 pages of the PCMCIA card.

Mapping Register 1

Map Address Register	Low Byte	High Byte
80H	0000 0000	1 100 0000

Mapping Register 2

Map Address Register	Low Byte	High Byte
84H	0000 0001	1 100 0000

Mapping Register 3

Map Address Register	Low Byte	High Byte
88H	0000 0010	1 100 0000

Mapping register 4 is mapped to the 40th 16K page in PCMCIA.

Mapping Register 4

Map Address Register	Low Byte	High Byte
8CH	0010 1001	1 100 0000

Mapping register 5 is mapped to the 44th page in the RAM array.

Mapping Register 5

Map Address Register	Low Byte	High Byte
90H	0010 1101	1 001 0000

Mapping register 21 is mapped to 59th page of the ROM array.

Mapping Register 21

Map Address Register	Low Byte	High Byte
D8H	0011 1011	1 010 0000

As you can see from this example, the VG-230's flexible memory architecture allows access to very large memory arrays through the 8086's limited address space. Access can be controlled through several different memory managers including EMS driver, PCMCIA XIP drivers, ROMDOS and ROM Disk drivers.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
Sub-Notebook Engine
Technical Reference

2.3 PCMCIA PC Card Support

PCMCIA version 2.0 is fully supported in the VG-230. If the internally scanned keyboard is enabled, a single PC card slot is supported. If the scanned keyboard is disabled, two PC card slots are supported. Version 2.0 of the PCMCIA standard supports the following:

- I/O cards
- Up to 64 Mbytes of memory
- Flash memory
- Execute in place (XIP)

0000 0011 1000 0000 H88

Access can be limited to ROM or RAM by setting the ROM/RAM bit. ROM access is limited to 64K bytes memory. RAM access is limited to 64M bytes memory. Access can be controlled through several different methods.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

020-0VMEGAV
БИОДА МОДЕЛОН-02
СВЕЧЕНІЯ ЗАКЛЮЧ

2.3.1 Hardware

The PCMCIA card interfaces directly to the VG-230 address and data lines. Several control signals complete the interface to the PC card. Figure 2.3-1 shows the interface to the SLOT A PC card. Figure 2.3-2 shows the interface to the SLOT B PC card.

PCMCIA SLOT "A" INTERFACE

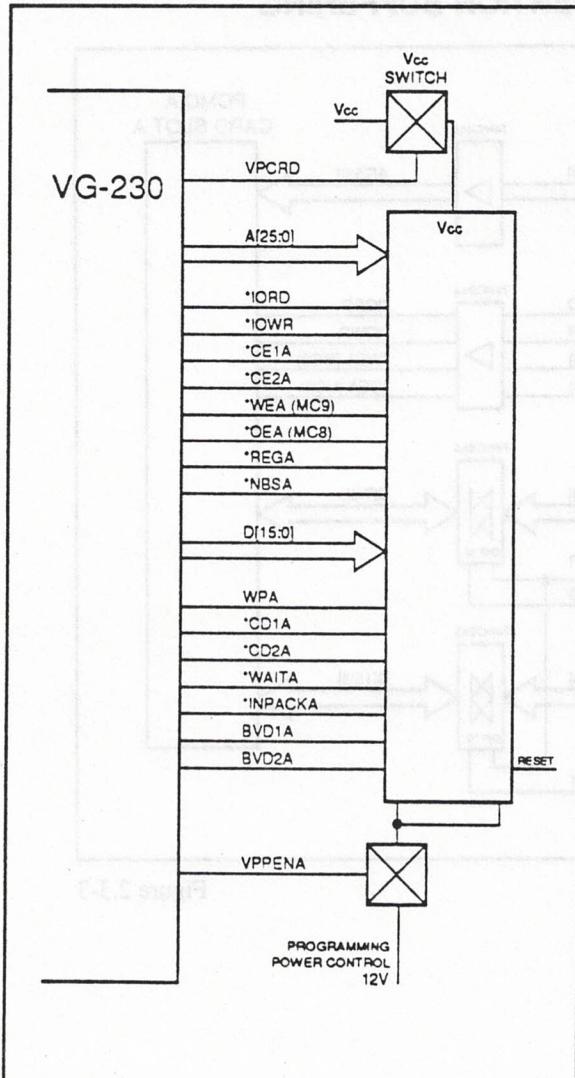


Figure 2.3-1

PCMCIA SLOT "B" INTERFACE

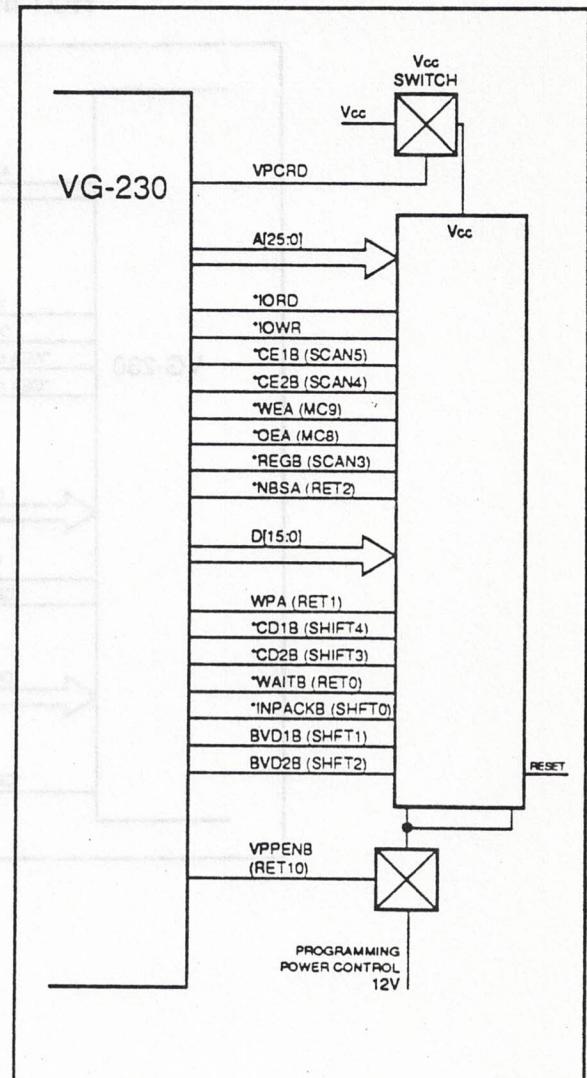


Figure 2.3-2

Reference the PCMCIA version 2.0 specification for detailed information on hardware and software interface requirements. This document can be obtained from the PCMCIA group directly at:

PCMCIA
(408)720-0107

2.3.2 Hot Insertion

The ability of the PC card to be inserted with system power on, without affecting the systems operation is called hot insertion. The VG-230 supports hot insertion with the addition of isolation buffers. These buffers isolate the PC card's I/O lines from the active data and address bus of the VG-230. The data buffer is controlled with the CDIR, *CBEN0 and *CBEN1 signals. Figure 2.3-3 illustrates the additional circuitry required for hot insertion support.

HOT INSERTION BUFFERING

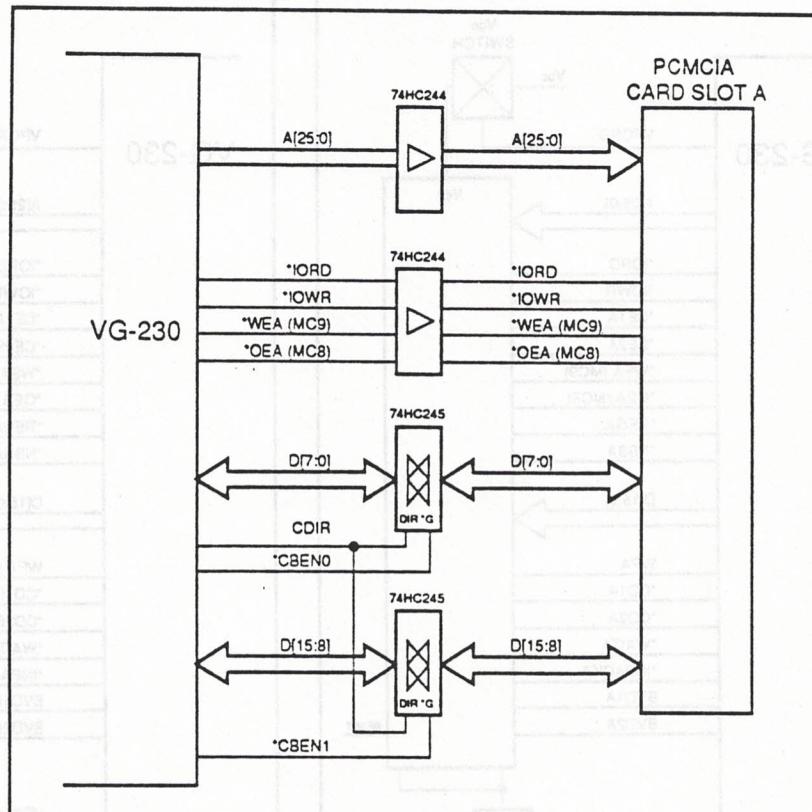


Figure 2.3-3

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

OSR-0V MEGAV
TURBO MODE BUS
SLOT1EN JACMPORT

2.3.3 PCMCIA Register Description

There are a total of 15 registers that control the PC card interface. These registers can be placed into the following 3 groups:

Global PC Card Control

PC Card Controller Mode Register	20H
PC Card Power Control Register	2DH
PC Card Activity Timer Mode Register	2EH

Slot 0 PC Card Control

PC Card Slot 0 Control Register	21H
PC Card Slot 0 Status Register	22H
PC Card Slot 0 Interrupt Mask Register	23H
PC Card Slot 0 I/O High Address Register	24H
PC Card Slot 0 I/O Low Address Register	25H
PC Card Slot 0 I/O Address Range Register	26H

Slot 1 PC Card Control

PC Card Slot 1 Control Register	27H
PC Card Slot 1 Status Register	28H
PC Card Slot 1 Interrupt Mask Register	29H
PC Card Slot 1 I/O High Address Register	2AH
PC Card Slot 1 I/O Low Address Register	2BH
PC Card Slot 1 I/O Address Range Register	2CH

There is also an additional register described in the Bus Cycle Generator section that controls the PC card interface:

Bus Cycle Generator Wait State Control 2 Reg	03H
--	-----

Global PC Card Control

The PC Card Controller Mode Register at offset 20H controls the global enable for each PC card. *SLOTOEN and *SLOT1EN enable the I/O and memory chip select decoding of the selected PC card.

The PC card controller can be configured to interrupt the CPU on status changes that occur on the PC card interface. These changes include:

- Card Change
- Battery Fail
- Low Battery
- Card Timeout

The IRSTS[1:0] bits route the status interrupt to IRQ2, IRQ6, IRQ7 or NMI. Interrupt status is presented in the PC Card Status registers at offset 22H and 28H.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

These bits control the programming enable pin. VPPENA and VPPENB are asserted only under the following conditions:

- S1PGMEN or S0PGMEN are set
- VPCRD is true
- PC card is inserted into the socket

It is the responsibility of the BIOS or software drivers to provide proper programming voltage sequencing and timing for memory programming.

Name: PC Card Controller Mode Register

Type: Read/Write

Index: 20H

Bit	Name	Default	Function	
D7	*SLOT0EN	0	0 - Enable PC Card Slot 0	
D6	*SLOT1EN	1	0 - Enable PC Card Slot 1 Note: In order to enable PC Card Slot 1, the Keyboard Scan function must be disabled.	
D[5:4]	IRSTS[1:0]	11	IRSTS1 IRSTS0	Interrupt Channel Select for Controller Status Interrupts
			0 0	NMI
			0 1	IRQ2
			1 0	IRQ6
			1 1	IRQ7
D3	S0PGMEN	0	1 - Enable Slot 0 Programming Voltage (VPPENA)	
D2	Reserved	0	Reserved bits	
D1	S1PGMEN	0	1 - Enable Slot 1 Programming Voltage (VPPENB)	
D0	Reserved	0	Reserved bits	
Note: Programming controls are automatically disabled when a card is removed from its socket or when Vcc to the cards has been removed.				

The PC card power control register at offset 2DH controls the power management features of the PC card interface. Bit TMOMSK enables a PC card status interrupt for activity timeout. The PC card interface contains its own activity monitor for any I/O or memory access to the card. This timer is reset every time access is made to the PC card. When this timer times out and TMOMSK is set, a status interrupt is generated. This allows the BIOS to decide if the PC card interface should be powered down. If TMOMSK is cleared, the power is automatically removed from the PC card interface.

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

The VPEN bit allows the PMU, in addition to the PC card activity timer, to control power to the PC card interface. When set the VP3 output of the PMU is Or'ed with the PC card activity timer output to control the VPCRD output.

Name: **PC Card Power Control Register**

Type: **Read/Write**

Index: **2DH**

Bit	Name	Default	Function
D7	TMOMSK	1	0 - Enable interrupts for Activity Time-Out 1 - VP output from PMU does not control power to PC Cards
D6	VPEN	0	0 - VPCRD output is defined as Low = ON 1 - VPCRD output is defined as High = ON
D5	POL	1	PC Card On/Off bit This bit is ignored when Time-Out interrupts are disabled or when both PC Card Slots are empty. When Time-Out interrupts are disabled, power to the PC Card is automatically removed when the PC Card Activity timer expires. When Time-Out interrupts are enabled, this bit is used by software to control power to the PC Cards.
D4	VPCRD	0	
D[3:0]	Reserved	0H	Reserved bit

The POL bit controls the polarity of the VPCRD output. The default condition is ON = VPCRD = 1.

The VPCRD bit is used to directly control the VPCRD output. This bit is only enabled when TMOMSK is set to 0 and one or more PC cards are inserted into the slots. VPCRD is used by the BIOS to control power to the PC card interface.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

The PC card activity timer register at offset 2EH enables the PC card activity timer. The TMRES bit sets the timer resolution. When set the resolution is 1 minute and 15 seconds when cleared. Therefore, the minimum timeout is 15 seconds and maximum is 15 minutes. Setting TMO[3:0] to a non zero number enables the activity timer. Any I/O or memory access to an enabled PC card resets the timer.

Name: PC Card Activity Timer Register
Type: Read/Write
Index: 2EH

Bit	Name	Default	Function
D7	TMRES	0	0 - Timer supports from 15 to 225 sec. (15 sec. resolution) 1 - Timer supports from 1 to 15 min. (1 min. resolution)
D[6:4]	Reserved	000	Reserved bits
D[3:0]	TMO[3:0]	0H	TMO[3:0] select the Activity Time-Out value. Setting TMO[3:0] all low will disable the timer.

Note: When Activity Time-Out interrupts are disabled and the Activity Timer expires, power to the PC Cards will automatically be removed. Subsequent activity to the PC Cards WILL NOT restore power to the Slots. In order for power to be restored, software must first write any value to the PC Card Activity Timer Register.

When the timer expires, an interrupt is generated or power is automatically removed from the card. When Activity timeout interrupts are enabled (through the TMOMSK bit in the PC card power control register) an interrupt is generated and it is up to the BIOS to determine if power is to be removed from the PC cards. The BIOS must restore power by writing a non-zero number into the TMO[3:0] register and setting VPCRD in the PC card power control register.

When activity timeout interrupts are disabled, power is automatically removed from the PC card. When power is automatically removed in this method, power must be re-enabled through a software routine.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

Slot 0 PC Card Register Interface

The following descriptions will describe the register interface to the Slot 0 PC Card. The operation of Slot 1 is identical to Slot 0.

Name: **PC Card Slot 0 Control Register**

Type: **Read/Write**

Index: **21H**

Bit	Name	Default	Function																																
D7	IO8BIT	0	1 - PC Card Slot 0 supports 8 bit I/O only. Data is transferred from the PC I/O Card on the low order data bus (D[7:0]).																																
D6	IO/*M	0	0 - PC Card Slot 0 configured for Memory I/F 1 - PC Card Slot 0 configured for I/O I/F While either one of *CD[2:1]A is high indicating a PC Card is not installed, or the PC Card is powered OFF, this bit is automatically reset low and the controller is forced into the Memory I/F Mode.																																
D5	*REG	0	0 - Direct PC Card access to REG (Attribute) memory 1 - Direct PC Card access to Common memory Normally, the *REGA output pin is driven directly from this bit. During DMA Cycles, this bit is ignored and the *REGA output is driven high.																																
D[4:2]	IRCRD[2:0]	111	<table border="1"> <thead> <tr> <th>IRCRD2</th> <th>IRCR0</th> <th>IRCRD0</th> <th>Interrupt Channel Select for PC Card (IREQ)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>X</td> <td>Illegal</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>IRQ2</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>IRQ3</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>IRQ4</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>IRQ5</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>IRQ6</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>IRQ7</td> </tr> </tbody> </table>	IRCRD2	IRCR0	IRCRD0	Interrupt Channel Select for PC Card (IREQ)	0	0	X	Illegal	0	1	0	IRQ2	0	1	1	IRQ3	1	0	0	IRQ4	1	0	1	IRQ5	1	1	0	IRQ6	1	1	1	IRQ7
IRCRD2	IRCR0	IRCRD0	Interrupt Channel Select for PC Card (IREQ)																																
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1	0	1	IRQ5																																
1	1	0	IRQ6																																
1	1	1	IRQ7																																
D[1:0]	CDLY[1:0]	01	<table border="1"> <thead> <tr> <th>CDLY1</th> <th>CDLY0</th> <th>PC Card Memory Command Delay</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0 CPUCLK cycle</td> </tr> <tr> <td>0</td> <td>1</td> <td>1 CPUCLK cycle</td> </tr> <tr> <td>1</td> <td>0</td> <td>2 CPUCLK cycle</td> </tr> <tr> <td>1</td> <td>1</td> <td>3 CPUCLK cycle</td> </tr> </tbody> </table>	CDLY1	CDLY0	PC Card Memory Command Delay	0	0	0 CPUCLK cycle	0	1	1 CPUCLK cycle	1	0	2 CPUCLK cycle	1	1	3 CPUCLK cycle																	
CDLY1	CDLY0	PC Card Memory Command Delay																																	
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0	1	1 CPUCLK cycle																																	
1	0	2 CPUCLK cycle																																	
1	1	3 CPUCLK cycle																																	

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

The PC Card Slot 0 Control Register at index 21H sets various operating modes for the PC card. IO8BIT sets the I/O word length for the PC card in slot 0 when configured in the I/O mode. When cleared, data is transferred on D[7:0] and when set, data is transferred on D[15:0].

IO/*M sets whether the card in slot 0 is configured for I/O or memory interface. This bit is reset (to a memory configuration) when the PC Card is powered off or a card is changed.

The *REG bit controls the *REGA pin on the PC Card interface. When cleared, the *REGA pin is forced low, enabling the PC card's attribute memory. This memory is accessed through the memory space and contains details on the PC card physical and logical configuration.

The IRCRD[2:0] bits select the interrupt level for a PC card configured for I/O. These bits are only valid when the IO/*M bit is set. For example, a modem card will use IRQ4 for COM1 or IRQ3 for COM2.

The CDLY[1:0] bits select the memory read command delay for accesses to the PC Card. Default is 1 CPUCLK cycle.

The PC Card Slot 0 Status Register at index 22H indicates various status items of the card in slot 0.

***BUSY/*CRDINT** - In memory mode this is a read-only bit reflecting the state of the RDY/*BSYA input. When cleared, the card is busy.

In I/O mode, this bit indicates the presence of a pending interrupt. The pending interrupt status is cleared by writing a 1 to this bit.

BVD2/*AUDIO - In memory mode with status interrupts disabled, this bit reflects the state of the BVD2A (Battery Voltage Detect Pin 2). When status interrupts are enabled, this bit indicates a pending status interrupt. The pending interrupt is cleared by writing a 1 to this bit.

In I/O mode, this bit reflects the state of the *SPKR input. This input can be monitored to see if the I/O card is generating any audio.

BVD1/*STSCHG - In the memory mode with status interrupts disabled, this bit reflects the state of the BVD1A (Battery Voltage Detect Pin 1). When status interrupts are enabled, this bit indicates a pending status interrupt. The pending interrupt is cleared by writing a 1 to this bit.

In the I/O mode, this bit reflects the state of the *STSCHG input. When interrupts are enabled, this bit indicates that a *STSCHG interrupt is pending. Writing a 1 to this bit will clear the status change interrupt.

***PRESENT** - This bit indicates that a card is properly inserted into the PC card socket. When low both *CD2A and *CD1A are active indicating that both sides of the card are properly seated in the socket.

***CRDCHG** - This bit is cleared when a card change occurs. It is cleared on the rising edge of either *CD[2:1]A. When status interrupts are enabled, this bit indicates a pending interrupt. Writing a 1 to this bit clears the pending interrupt.

CRDTM0 - This bit indicates that the PC card activity timer has timed out and an interrupt is pending. Writing a 1 to this bit clears the pending interrupt.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

OS-3V N30AV
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

WP/NU - This bit reflects the state of the WPA input pin. This pin is only used in the memory interface and is not used when in I/O mode. When this bit is a 1, the card is write-protected.

CRDOFF - Status bit indicating that the power to both PC cards is off. A 1 in this bit indicates that power to the interface is off.

Pin	Name	Description	Value
82	CRDOFF	CRDOFF is state generator for pins Q1 and Q2. It is also used to hold memory cards when power is off. Q1 is set to 1 when CRDOFF is 1. Q2 is set to 0 when CRDOFF is 0. Both Q1 and Q2 are tied to ground.	1
83	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q3 and Q4. It is also used to hold memory cards when power is off. Q3 is set to 1 when CRDOFF is 1. Q4 is set to 0 when CRDOFF is 0. Both Q3 and Q4 are tied to ground.	1
84	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q5 and Q6. It is also used to hold memory cards when power is off. Q5 is set to 1 when CRDOFF is 1. Q6 is set to 0 when CRDOFF is 0. Both Q5 and Q6 are tied to ground.	1
85	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q7 and Q8. It is also used to hold memory cards when power is off. Q7 is set to 1 when CRDOFF is 1. Q8 is set to 0 when CRDOFF is 0. Both Q7 and Q8 are tied to ground.	1
86	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q9 and Q10. It is also used to hold memory cards when power is off. Q9 is set to 1 when CRDOFF is 1. Q10 is set to 0 when CRDOFF is 0. Both Q9 and Q10 are tied to ground.	1
87	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q11 and Q12. It is also used to hold memory cards when power is off. Q11 is set to 1 when CRDOFF is 1. Q12 is set to 0 when CRDOFF is 0. Both Q11 and Q12 are tied to ground.	1
88	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q13 and Q14. It is also used to hold memory cards when power is off. Q13 is set to 1 when CRDOFF is 1. Q14 is set to 0 when CRDOFF is 0. Both Q13 and Q14 are tied to ground.	1
89	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q15 and Q16. It is also used to hold memory cards when power is off. Q15 is set to 1 when CRDOFF is 1. Q16 is set to 0 when CRDOFF is 0. Both Q15 and Q16 are tied to ground.	1
90	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q17 and Q18. It is also used to hold memory cards when power is off. Q17 is set to 1 when CRDOFF is 1. Q18 is set to 0 when CRDOFF is 0. Both Q17 and Q18 are tied to ground.	1
91	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q19 and Q20. It is also used to hold memory cards when power is off. Q19 is set to 1 when CRDOFF is 1. Q20 is set to 0 when CRDOFF is 0. Both Q19 and Q20 are tied to ground.	1
92	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q21 and Q22. It is also used to hold memory cards when power is off. Q21 is set to 1 when CRDOFF is 1. Q22 is set to 0 when CRDOFF is 0. Both Q21 and Q22 are tied to ground.	1
93	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q23 and Q24. It is also used to hold memory cards when power is off. Q23 is set to 1 when CRDOFF is 1. Q24 is set to 0 when CRDOFF is 0. Both Q23 and Q24 are tied to ground.	1
94	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q25 and Q26. It is also used to hold memory cards when power is off. Q25 is set to 1 when CRDOFF is 1. Q26 is set to 0 when CRDOFF is 0. Both Q25 and Q26 are tied to ground.	1
95	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q27 and Q28. It is also used to hold memory cards when power is off. Q27 is set to 1 when CRDOFF is 1. Q28 is set to 0 when CRDOFF is 0. Both Q27 and Q28 are tied to ground.	1
96	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q29 and Q30. It is also used to hold memory cards when power is off. Q29 is set to 1 when CRDOFF is 1. Q30 is set to 0 when CRDOFF is 0. Both Q29 and Q30 are tied to ground.	1
97	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q31 and Q32. It is also used to hold memory cards when power is off. Q31 is set to 1 when CRDOFF is 1. Q32 is set to 0 when CRDOFF is 0. Both Q31 and Q32 are tied to ground.	1
98	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q33 and Q34. It is also used to hold memory cards when power is off. Q33 is set to 1 when CRDOFF is 1. Q34 is set to 0 when CRDOFF is 0. Both Q33 and Q34 are tied to ground.	1
99	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q35 and Q36. It is also used to hold memory cards when power is off. Q35 is set to 1 when CRDOFF is 1. Q36 is set to 0 when CRDOFF is 0. Both Q35 and Q36 are tied to ground.	1
100	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q37 and Q38. It is also used to hold memory cards when power is off. Q37 is set to 1 when CRDOFF is 1. Q38 is set to 0 when CRDOFF is 0. Both Q37 and Q38 are tied to ground.	1
101	NOVA DIGITAL	NOVA DIGITAL is state generator for pins Q39 and Q40. It is also used to hold memory cards when power is off. Q39 is set to 1 when CRDOFF is 1. Q40 is set to 0 when CRDOFF is 0. Both Q39 and Q40 are tied to ground.	1

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

Name: PC Card Slot 0 Status Register

Type: Read/Write

Index: 22H

Bit	Name	Default	Function
D7	*BUSY/ *CRDINT	1	Read Only bit reflecting state of RDY/*BSYA input during Memory Mode or latched *IREQA for I/O Mode. 0 - Card Busy (Memory) Card Interrupt Pending (I/O) In I/O mode this bit may be set by writing this register with bit D7 set high.
D6	BVD2/ *AUDIO	1	Read Only bit reflecting state of BVD2A input during Memory Mode or *AUDIOA for I/O Mode. 0 - Battery Low (Memory) Card Speaker Active (I/O) In Memory mode, this bit is driven directly from the BVD2 input pin when Low Battery interrupts are masked OFF. Or, it is driven from the latched BVD2 input when Low Battery interrupts are enabled. When interrupts are enabled, writing this register with bit D6 set high clears the Low Battery Interrupt and sets this bit. In I/O mode the state of the I/O card signal may be read here.
D5	BVD1/ *STSCHG	1	Read Only bit reflecting state of BVD1A input during Memory Mode or *STSCHGA for I/O Mode. 0 - Battery Fail (Memory) Status Change (I/O) This bit is driven directly from the BVD1/*STSCHG input when Battery Fail interrupts are masked OFF. Or, it is driven from the latched BVD1/*STSCHG input when Battery Fail interrupts are enabled. When interrupts are enabled, writing this register with bit D5 set high clears the Battery Fail or Status Changed Interrupt and sets this bit.
D4	*PRESENT	X	Read Only bit reflecting state of *CD[2:1]A inputs 0 - Card Present (Low when both *CD[2:1]A are low) While Card A is removed from its socket, PC Card Slot 0 Status bits D[7:5] will be forced high, and D1 will be forced low.
D3	*CRDCHG	1	Card Change status bit. *CRDCHG is reset on the rising edge of either *CD[2:1]A. 0 - Card has been Changed This bit is set and the Card Change Interrupt is cleared by writing this register with bit D3 set high.
D2	*CRDTM0	1	Card Activity Time-Out. 0 - Card Time-Out Writing this register with bit D2 set high sets this bit and clears the Card Time-Out interrupt.
D1	WP/NU	X	Read Only bit reflecting state of WPA input during Memory Mode. This pin reads back low in I/O Mode. 1 - Card Write Protected
D0	CRDOFF	0	1 - Power to PC Card slot 0 and 1 is OFF.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

08-0V MEGAV
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

The PC Card Slot 0 Interrupt Mask register at index 23H controls interrupt generation for slot 0. Both status interrupts and I/O interrupt features are controlled through this register. When IREQMSK = 1, I/O interrupts are disabled from the selected slot. The PULSED bit selects level- or pulsed-mode interrupts from the I/O card. Both of the previously described bits are "don't care" when a memory card is inserted.

When memory mode is enabled, the LBMSK bit enables low battery status interrupts. This interrupt indicates that the battery is low and requires changing. It does not indicate that the PC Card's memory is invalid. When I/O card is enabled, this bit is used to control the PC card audio output. When set, this bit keeps the audio signal from being ORed into the VG-230's speaker circuit. Status for this interrupt can be monitored in the BVD2/*AUDIO bit in the Status register.

When memory card is enabled, the LLBMSK bit controls the Battery fail alarm (BVD1 input) interrupt. This interrupt indicates that the PC card's battery has failed, and data contained in the card is invalid. In I/O mode this bit controls the status change input interrupt. Status for this interrupt can be monitored in the BVD1/*STSCHG bit in the Status register.

When memory card or I/O card is enabled, the CHGMSK bit controls the card removal interrupt. Status for this interrupt can be monitored in the *CRDCHG bit of the Status register.

Name: PC Card Slot 0 Interrupt Mask Register
Type: Read/Write
Index: 23H

Bit	Name	Default	Function
D7	IREQMSK	1	0 - Enable interrupts generated from Slot 0 I/O Cards
D6	LBMSK	0	0 - Enable Slot 0 low battery warning interrupts (Memory Mode) or disable PC Card Audio Output (I/O Mode). When this bit is reset Low in I/O Mode, the PC Card Audio signal is disabled and will read back High in the Status Register.
D5	LLBMSK	0	0 - Enable Slot 0 Battery Fail Alarm Interrupts (Memory Mode) or enable Slot 0 Status Changed Interrupts (I/O Mode)
D4	Reserved	0	Reserved bit
D3	CHGMSK	0	0 - Enable interrupts for Card Removal from Slot 0
D[2:1]	Reserved	00	Reserved bits
D0	PULSED	0	0 - Controller supports Level Mode Interrupts from PC I/O Cards 1 - Controller supports Pulsed Mode Interrupts from PC I/O Cards

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

The next set of PC card registers control the operation of the I/O card. The VG-230's I/O address interface supports a 64Kbyte address space. The PCMCIA standard allows both fixed address cards and variable address cards. The VG-230 supports both. For cards that support their own internal address decoding, the *INPACK pin is driven when the card recognizes its own address range. For I/O cards that require the host to configure the address the VG-230 contains three registers configure the starting address and length of the I/O space occupied by the PC card. The selection of the type of I/O device is controlled by the *INPMISK bit in the I/O address range register at offset 26H. When this bit is set, the I/O decode address is determined by the PC card. When this bit is cleared, the I/O decode address is determined by the I/O high address reg (24H), the I/O low address register (25H) and the I/O address range reg (26H).

Name: PC Card Slot 0 I/O High Address Register

Type: Read/Write

Index: 24H

Bit	Name	Default	Function
D[7:0]	A[15:8]	00H	Upper address bits for slot 0 PC Card base I/O address.

Name: PC Card Slot 0 I/O Low Address Register

Type: Read/Write

Index: 25H

Bit	Name	Default	Function
D[7:3]	A[7:3]	00H	Low address bits for slot 0 PC Card base I/O address.
D[2:0]	Reserved	000	Reserved bits

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

Name: PC Card Slot 0 I/O Address Range Register
 Type: Read/Write
 Index: 26H

Bit	Name	Default	Function																																										
D[7:3]	A[7:3]MSK	00H	<p>Mask bits for lower address bits. Each bit allows its corresponding address bit to be masked from the address comparison as follows:</p> <table> <thead> <tr> <th>A7MSK</th><th>A6MSK</th><th>A5MSK</th><th>A4MSK</th><th>A3MSK</th><th>I/O Range</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>8 Bytes</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>16 Bytes</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>32 Bytes</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>64 Bytes</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>128 Bytes</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>256 Bytes</td></tr> </tbody> </table>	A7MSK	A6MSK	A5MSK	A4MSK	A3MSK	I/O Range	0	0	0	0	0	8 Bytes	0	0	0	0	1	16 Bytes	0	0	0	1	1	32 Bytes	0	0	1	1	1	64 Bytes	0	1	1	1	1	128 Bytes	1	1	1	1	1	256 Bytes
A7MSK	A6MSK	A5MSK	A4MSK	A3MSK	I/O Range																																								
0	0	0	0	0	8 Bytes																																								
0	0	0	0	1	16 Bytes																																								
0	0	0	1	1	32 Bytes																																								
0	0	1	1	1	64 Bytes																																								
0	1	1	1	1	128 Bytes																																								
1	1	1	1	1	256 Bytes																																								
D[2:1]	Reserved	000	Reserved bits																																										
D0	*INPMSK	0	<p>Card A input acknowledge mask bit</p> <p>0 - Ignore PC I/O card *INPACK signal. PC card data buffers enabled whenever chip select is asserted.</p> <p>1 - Enable PC I/O Card *INPACK signal. PC card data buffers enabled only when chip select is asserted and *INPACK is returned from PC I/O card.</p>																																										

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

2.4 Firmware

The VG-230's PC card interface is version 2.0 compatible. This means that the hardware interface is compatible with the hardware standard. This includes the following:

- Hardware interface compatible with PCMCIA
- 64 Mbyte address space
- Support I/O cards
- Support XIP memory mapping

However the hardware interface is only one part to the PCMCIA standard. There are additional firmware and software drivers required to fully utilize all the features of PCMCIA version 2.0. Figure 2.4-1 illustrates the interface between the hardware, drivers and DOS.

INTERFACE BETWEEN HARDWARE, DRIVERS AND DOS

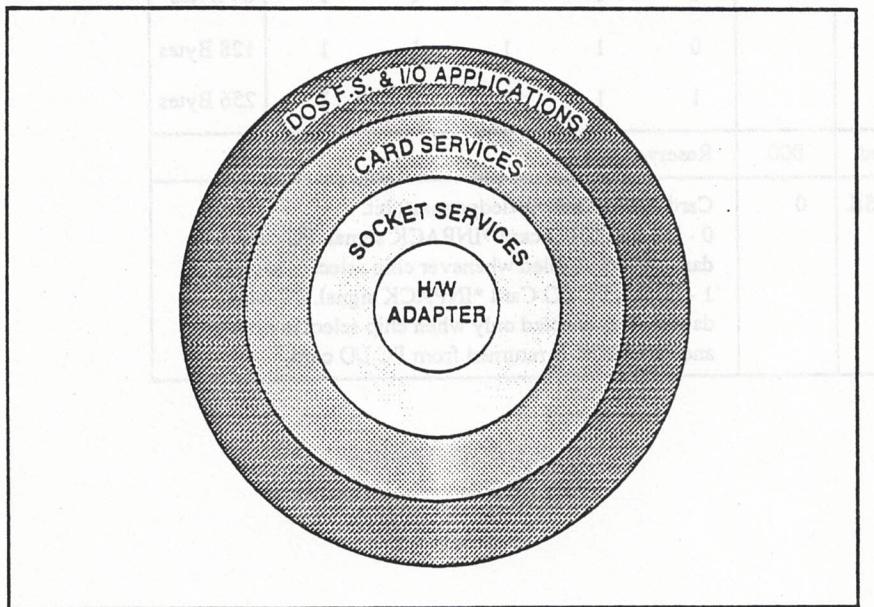


Figure 2.4-1

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

The PCMCIA support designed in the system has several layers starting with the hardware and ending with the DOS file system. The interaction of the various layers is diagrammed in figure 2.4-2

PCMCIA SUPPORT LAYERS

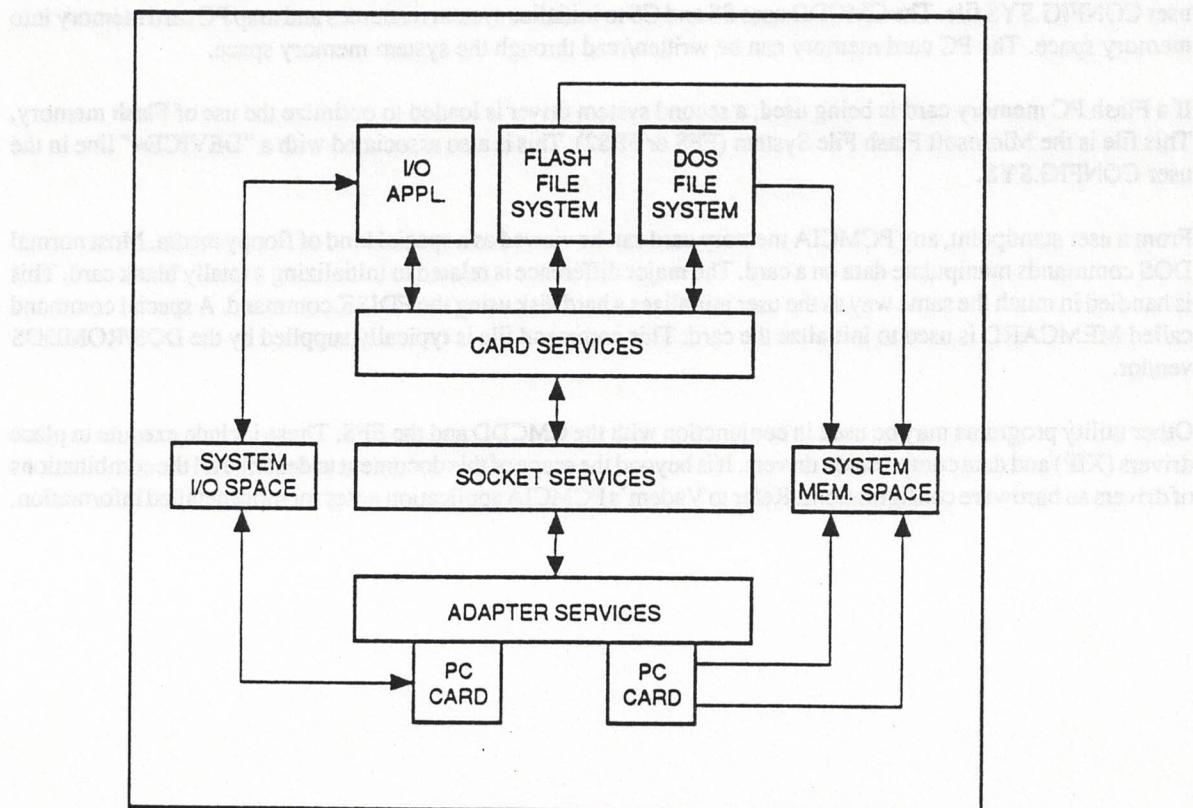


Figure 2.4-2

While the actual hardware interface to the PC card has been defined, the interface to the system has not. Therefore, no standard I/O addresses or hardware configurations have been specified by the standards committee. It is up to the system manufacturer to provide a standard BIOS level interface to the PC card. This BIOS interface is called "Socket Services" (SS) and provides an interface through an extension to interrupt 1AH. Socket services provides a hardware-independent interface to control the following functions:

- Card initialization
- Low battery check, card removal detection and I/O change notification
- I/O and memory card select
- System card memory mapping

This BIOS interface is typically supplied by the BIOS vendor and is contained in the system BIOS. Additional BIOS code to control power management of the PC card is also supplied by the BIOS vendor.

The level above Socket Services (SS) is called Card Services (CS). This level provides system resource allocation and other services directly related to the PC cards.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

DE5-DV MEGAV
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

The level above Card Services is the Compliant Memory Card Device Driver (CMCDD). The CMCDD reads the configuration ROM contained in every PC card and provides information to DOS on the format and configuration of the PC card. The CMCDD is typically provided by the DOS or ROMDOS supplier. During the operating system boot, DOS will install and initialize the CMCDD. The normal method for this is to have a "DEVICE=" line in the user CONFIG.SYS file. The CMCDD uses SS and CS to initialize system resources and map PC card memory into memory space. The PC card memory can be written/read through the system memory space.

If a Flash PC memory card is being used, a second system driver is loaded to optimize the use of Flash memory. This file is the Microsoft Flash File System (FFS or FFS2). This is also associated with a "DEVICE=" line in the user CONFIG.SYS.

From a user standpoint, any PCMCIA memory card can be viewed as a special kind of floppy media. Most normal DOS commands manipulate data on a card. The major difference is related to initializing a totally blank card. This is handled in much the same way as the user initializes a hard disk using the FDISK command. A special command called MEMCARD is used to initialize the card. This command file is typically supplied by the DOS/ROMDOS vendor.

Other utility programs may be used in conjunction with the CMCDD and the FFS. These include execute in place drivers (XIP) and data compression drivers. It is beyond the scope of this document to describe all the combinations of drivers and hardware configurations. Refer to Vadem's PCMCIA application notes for more detailed information.

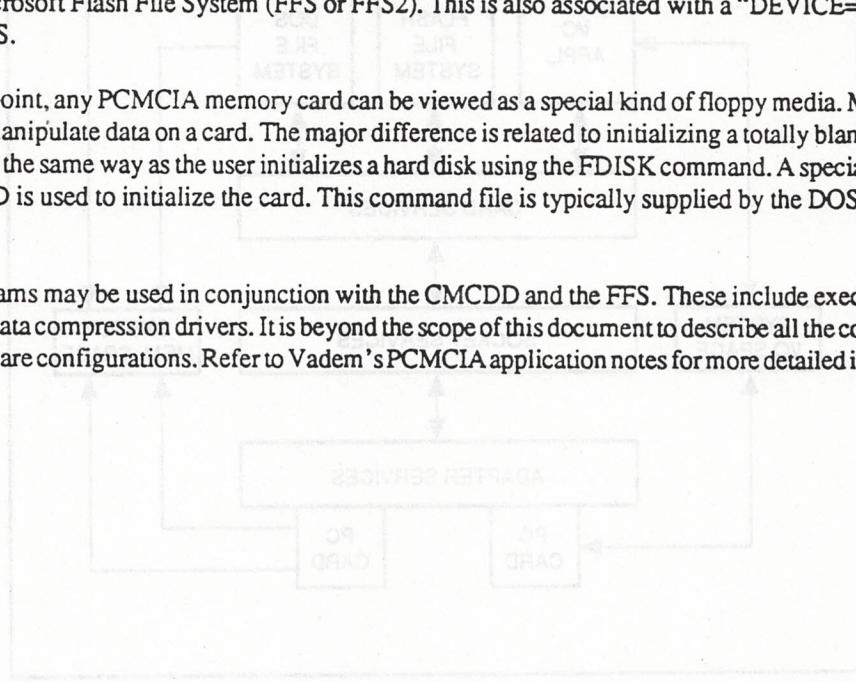


Figure 2-4.5

Another level above the PCMCIA services is the PCMCIA drivers. These drivers are responsible for interfacing between the PCMCIA card and the rest of the system. They handle tasks such as reading/writing data to the card, managing memory, and providing interrupt handling. The PCMCIA drivers are typically supplied by the card manufacturer or the DOS/ROMDOS vendor.

At the lowest level is the PCMCIA card itself. It contains the memory chips and logic required to interface with the host system. The card is connected to the PCMCIA slot via a ribbon cable. The card is controlled by the PCMCIA drivers, which provide the necessary power and control signals to the card.

The PCMCIA card is just one type of PC card. There are others, such as SCSI cards, which provide additional functionality. However, the basic architecture remains the same: a software stack consisting of system services, PCMCIA services, PCMCIA drivers, and the card itself.

In conclusion, the PCMCIA card is a specialized type of memory card that provides additional storage and processing power to the system. It is controlled by the PCMCIA drivers, which are part of the overall system architecture. The card is connected to the host system via a ribbon cable and provides a standard interface for data transfer.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

2.5 Display Subsystem

The VG-230 integrates a CGA/AT&T compatible LCD controller. The controller interfaces directly to a wide variety of panels. Refer to the VG-230 data sheet for some of the compatible panels.

2.5.1 VG-230 CGA LCD Controller

The VG-230 CGA LCD Controller is enabled by clearing the *ENALCD bit of the LCD Configuration Control Register at offset 07H. The LCD Configuration Control Register is a Read/Write register located at Index 07H. The following is the bit assignment and description of the LCD Configuration Control Register.

Name: LCD Configuration Control Register
Type: Read/Write
Index: 07H

Bit	Name	Default	Function
D7	*ENALCD	0	Sub-Notebook Engine LCD Enable/Disable Bit 0 - Enable SNE LCD Controller 1 - Disable SNE LCD Controller
D[6:5]	VIDSPD[1:0]	00	These bits determine the access speed of system RAM during video refresh cycles as follows: VIDSPD1 VIDSPD0 Clocks per video cycle 0 0 4-8 bit RAM / 5-16 bit RAM (normal) 0 1 5-8 bit RAM / 6-16 bit RAM (slow) 1 0 3-8 bit RAM / 4-16 bit RAM (fast) 1 1 Reserved
D[4:0]	Reserved	0H	Reserved for future use.

The VG-230's LCD Controller is programmed using an index and data register scheme. The Index register is at 3D4 and the data register is at 3D5. Both registers are Read/Write and shadowed at 3D0/3D1, 3D2/3D3, and 3D6/3D7 respectively. The address is decoded using A0-A9 and AEN=0 (the PC/XT uses only A0-A9). The 6845 registers R1-R9 are used to program the display characteristics for a CRT. They have no meaning for an LCD and are therefore not implemented here. In addition to CGA registers, three additional registers are implemented for AT&T compatibility. These are Mode Select Register A (3D8H), Mode Select Register B (3DEH), and Status Register (3DAH).

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

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Sub-NOTEBOOK ENGINE
TECHNICAL REFERENCE

The following list summarizes the registers of the VG-230 CGA/AT&T LCD Controller:

Name: CGA Index Register
Type: Read/Write
Address: 3D4H

Note: The Index register is shadowed at 3D0, 3D2, and 3D6

Name: CGA Data Register
Type: Read/Write
Address: 3D5H

Note: The Data register is shadowed at 3D1, 3D3, and 3D7

REGISTER

INDEX

Cursor Start Raster Register 0AH

Cursor End Raster Register 0BH

Display Start Address MSB Register 0CH

Display Start Address LSB Register 0DH

Cursor Location Address MSB Register 0EH

Cursor Location Address LSB Register 0FH

These VG-230-specific registers are used to control the windowing, select the LCD type, set the time-out delays, control the PMU, and control the LCD resolution:

Window Start MSB Register C0H

Window Start LSB Register C1H

LCD Configuration Register C2H

LCD Panel Resolution Register CAH

LCD Mode Register CCH

This section contains a detailed description of the VG-230's CGA/LCD Controller. It includes a description of the architecture, memory map, and various registers. The VG-230 is a high-performance CGA/LCD controller designed for sub-notebook applications. It features a 640x400 pixel resolution and supports up to 16 colors. The controller is based on the AT&T 32032 processor and includes a built-in memory management unit (MMU) and a direct memory access (DMA) controller. The VG-230 also includes a timer, a programmable interrupt controller, and a serial port. The controller is controlled via a 16-bit parallel port and a 16-bit serial port. The parallel port is used for video output and can support up to 16 colors. The serial port is used for communication with other devices and can support up to 16 colors. The controller is controlled via a 16-bit parallel port and a 16-bit serial port. The parallel port is used for video output and can support up to 16 colors. The serial port is used for communication with other devices and can support up to 16 colors.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

2.5.2 CGA Compatible Registers

The following is a brief description of the registers necessary to maintain IBM CGA compatibility:

Name: **Cursor Start Raster Register**
Type: **Read/Write**
Address: **CGA INDEX 0AH**

Bit	Name	Default	Function
D[7:6]	Reserved	00	Not used
D5	*CURON	0	0 = Cursor displayed 1 = Cursor not displayed
D[4:0]	SC[4:0]	00H	Select raster to start cursor 00 = line 0, 01 = line 1, 02 = line 2, etc.

This register is used to determine whether or not the cursor is to be displayed. *CURON (Bit D5) controls the cursor display. When *CURON is reset low, the cursor is displayed, when set high, the cursor is not displayed. SC[4:0] (Bits D[4:0]) are used to determine what line the cursor begins on. The value written to these bits corresponds to the line at which the cursor begins.

Name: **Cursor End Raster Register**
Type: **Read/Write**
Address: **CGA INDEX 0BH**

Bit	Name	Default	Function
D[7:5]	Reserved	000	Not used
D[4:0]	EC[4:0]	0H	Select raster to end cursor 00 = line 0, 01 = line 1, 02 = line 2, etc.

SC[4:0] (Bits D[4:0]) are used to determine what line the cursor ends on. The value written to these bits corresponds to the line at which the cursor ends.

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

The following registers are also CGA compatible registers. They are used by software to locate the start of the display at the upper left corner of the display device.

Name: Display Start Address MSB Register
Type: Read/Write
Address: CGA INDEX 0CH

Name: Display Start Address LSB Register
Type: Read/Write
Address: CGA INDEX 0DH

Bit	Address
D[7:6]	Not used
D5	13
D4	12
D3	11
D2	10
D1	9
D0	8
Note: Holds the upper byte of address for the character at the upper left corner of a normal CGA display. See Window Start MSB Register.	

Bit	Address
D7	7
D6	6
D5	5
D4	4
D3	3
D2	2
D1	1
D0	0
Note: Holds the lower byte of address for the character at the upper left corner of a normal CGA display. See Window Start LSB Register.	

Column 1	Column 2	Column 3	Column 4
Window Start MSB	00H	00H	00H
Window Start LSB	00H	00H	00H

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

020-0V MEGAV
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

The following two registers hold the cursor location address. They are CGA compatible registers. Software writes these registers to provide the address for the cursor location.

Name: Cursor Location Address MSB Register
Type: Read/Write
Address: CGA INDEX 0EH

Bit	Address
D[7:6]	Not used
D5	13
D4	12
D3	11
D2	10
D1	9
D0	8

Note: Holds the upper byte of the cursor location address.

Name: Cursor Location Address LSB Register
Type: Read/Write
Address: CGA INDEX 0FH

Bit	Address
D7	7
D6	6
D5	5
D4	4
D3	3
D2	2
D1	1
D0	0

Note: Holds the lower byte of the cursor location address.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

2.5.3 VG-230-Specific CGA LCD Controller Registers

The following registers are specific to the VG-230 CGA LCD Controller. They are accessed via the same Index and Data addresses as the previously described CGA-compatible registers. These registers are used to configure the VG-230 LCD controller. They control windowing, LCD type and resolution, set time-out delays, and control related PMU functions.

The standard Display Start Address MSB and LSB Registers address a display area of 640 x 200. The VG-230 provides the additional Window Start MSB and LSB Registers to address smaller displays. When the VG-230 LCD Controller is configured for a display that is smaller than 640 x 200, software writes and reads intended for the Display Start Address MSB and LSB registers are redirected by the BIOS to the Window Start MSB and LSB Registers. This redirection is totally transparent to the software and user.

The following is the bit assignment of the Window Start MSB and LSB Registers.

Name: **Window Start MSB Register**
Type: **Read/Write**
Address: **CGA INDEX C0H**

Name: **Window Start LSB Register**
Type: **Read/Write**
Address: **CGA INDEX C1H**

Bit	Address
D[7:5]	Not used
D4	12
D3	11
D2	10
D1	9
D0	8

Note: The Window Start registers contain the memory address for the upper left corner of the LCD panel. Writes to Index 0CH are automatically copied to this register.

Bit	Address
D7	7
D6	6
D5	5
D4	4
D3	3
D2	2
D1	1
D0	0

Note: Writes to index 0DH are automatically copied to this register.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

CGA-DV MEGAV
VIDEOPACIFICUS
SOCIETAS INDUSTRIALIS

The LCD configuration register selects the cursor blink rate and the selection of reverse/normal video.

Name: **LCD Display Control Register**

Type: **Read/Write**

Address: **CGA INDEX C2H**

Bit	Name	Default	Function
D[7:6]	ATTBLK[1:0]	00	Controls blink rate for character blink attribute
			Bit 7 Bit 6
			0 0 Steady
			0 1 1/64 frame
			1 0 1/32 frame
			1 1 1/16 frame
D[5:4]	CURBLK[1:0]	00	Controls blink rate for the cursor in conjunction with bit 5 of the Cursor Start Scan Line Register.
			Bit 5 Bit 4
			0 0 Steady
			0 1 1/64 frame
			1 0 1/32 frame
			1 1 1/16 frame
D[3:1]	Reserved	000	Reserved bits
D0	RVVD	0	Reverse video for entire LCD 0 = normal polarity 1 = LCD in reverse video

ATTBLK[1:0] control the rate at which a character blinks. The value written to these bits determines whether a character remains steady or blinks at various rates.

CURBLK[1:0] along with Bit5 of the Cursor Start Raster Register determine the blink rate of the cursor.

RVVD controls the polarity of the LCD display. The default value is for normal polarity. Setting this bit high reverses the video of the entire display.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

Name: LCD Panel Resolution Register

Type: Read/Write

Address: CGA INDEX CAH

Bit	Name	Default	Function																				
D[7:6]	LCDW[1:0]	00	LCD data bus width 00=4 bit, 01=2 bit, 10=1 bit, 11=not used																				
D[5:0]	LCDR[5:0]	000000	<table> <thead> <tr> <th>LCDR[5:0]</th> <th>Panel Resolution</th> </tr> </thead> <tbody> <tr><td>000000</td><td>640 x 400</td></tr> <tr><td>000000</td><td>640 x 200</td></tr> <tr><td>000010</td><td>640 x 100</td></tr> <tr><td>001001</td><td>480 x 128</td></tr> <tr><td>010001</td><td>240 x 128</td></tr> <tr><td>010011</td><td>240 x 64</td></tr> <tr><td>011001</td><td>128 x 128</td></tr> <tr><td>011011</td><td>128 x 64</td></tr> <tr><td>100000</td><td>320 x 200</td></tr> </tbody> </table>	LCDR[5:0]	Panel Resolution	000000	640 x 400	000000	640 x 200	000010	640 x 100	001001	480 x 128	010001	240 x 128	010011	240 x 64	011001	128 x 128	011011	128 x 64	100000	320 x 200
LCDR[5:0]	Panel Resolution																						
000000	640 x 400																						
000000	640 x 200																						
000010	640 x 100																						
001001	480 x 128																						
010001	240 x 128																						
010011	240 x 64																						
011001	128 x 128																						
011011	128 x 64																						
100000	320 x 200																						

LCDW[1:0] are used to select the proper LCD data bus width required for the LCD panel. Large panels usually require a 4 bit data bus. Smaller panels may require a 2 bit or 1 bit data bus. Table 2.5-2 gives the data pin names for 4 bit, 2 bit, and 1 bit wide LCD data bus requirements.

Pin	Name	000	001	010	011
DATA[3:0]	RVAQD	0			

DATA[3:0] controls the logic level of the four data pins required to interface with a standard 4-bit LCD panel. The logic levels are determined by the value of the RDQS[2:0] pins.

RDQS[2:0] selects which of the four data pins will be active at any one time. RDQS[2:0] = 000 enables DATA[3:0], RDQS[2:0] = 001 enables DATA[2:1], RDQS[2:0] = 010 enables DATA[1:0], and RDQS[2:0] = 011 enables DATA[0]. RDQS[2:0] also controls the logic level of the RDQS[1:0] pins.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

Name: LCD Mode Register
 Type: Read/Write
 Address: CGA INDEX CCH

Bit	Name	Default	Function																																
D7	SEL60HZ	0	Frame Rate for LCD Widths																																
			<table> <thead> <tr> <th>SEL60HZ Value</th><th>Clock MHz</th><th>640;320 Hz</th><th>480;240 Hz</th><th>128 Hz</th></tr> </thead> <tbody> <tr> <td>0</td><td>14.3</td><td>69</td><td>72</td><td>67</td></tr> <tr> <td>0</td><td>16</td><td>72</td><td>75</td><td>70</td></tr> <tr> <td>1</td><td>14.3</td><td>60</td><td>62</td><td>58</td></tr> <tr> <td>1</td><td>16</td><td>59</td><td>62</td><td>57</td></tr> </tbody> </table>	SEL60HZ Value	Clock MHz	640;320 Hz	480;240 Hz	128 Hz	0	14.3	69	72	67	0	16	72	75	70	1	14.3	60	62	58	1	16	59	62	57							
SEL60HZ Value	Clock MHz	640;320 Hz	480;240 Hz	128 Hz																															
0	14.3	69	72	67																															
0	16	72	75	70																															
1	14.3	60	62	58																															
1	16	59	62	57																															
D6	Reserved	0	Reserved bit																																
D[5:3]	DLY[2:0]	000	LCD Sequencing Delay Setting																																
			<table> <thead> <tr> <th>DLY2</th><th>DLY1</th><th>DLY0</th><th>Sequencing Delay</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>7.5 ms</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>15 ms</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>30 ms</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>60 ms</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>120 ms</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>240 ms</td></tr> <tr> <td>1</td><td>1</td><td>X</td><td>Reserved</td></tr> </tbody> </table>	DLY2	DLY1	DLY0	Sequencing Delay	0	0	0	7.5 ms	0	0	1	15 ms	0	1	0	30 ms	0	1	1	60 ms	1	0	0	120 ms	1	0	1	240 ms	1	1	X	Reserved
DLY2	DLY1	DLY0	Sequencing Delay																																
0	0	0	7.5 ms																																
0	0	1	15 ms																																
0	1	0	30 ms																																
0	1	1	60 ms																																
1	0	0	120 ms																																
1	0	1	240 ms																																
1	1	X	Reserved																																
D2	400LINE	0	400 Line select 0 - LCD is 640x200 resolution or lower 1 - LCD is 640x400 lines																																
D1	Toshiba	0	1 - Toshiba LOADCLK Timing																																
D0	Sharp	0	1 - Sharp LOADCLK Timing																																
Note: For physical 400-line panels, the lower 4 data bits to the panel (LCDL[3:0]) must be explicitly enabled using the GPIO Mode Register (index 32H).																																			

SEL60HZ (bit D7) is used to select the frame rate frequency. The FRAME output is measured in Hz and is based on the CPUCLK. The value written to SEL60HZ selects the proper frame rate for the different panel widths supported. The actual frame rate is dependent upon the CPUCLK frequency and the setting of SEL60HZ.

LCD panels have different power sequencing requirements. The DLY[2:0] bits control the delay interposed between power sequencing events to meet the requirements of the specific panel in the system.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

400LINE (bit D2) in conjunction with the LCD Panel Resolution Register are used to configure the VG-230 LCD controller for the various supported panel resolutions. For panels of 64, 100, 128, and 200 lines, the 400LINE bit must be set low. Setting 400LINE high normally is used for 400 line panels.

The Toshiba (bit D1) and Sharp (bit D0) register bits are used to provide the proper LOADCLK timing. Toshiba and Sharp panels require specific LOADCLK timings. When a Toshiba or Sharp LCD panel is used, setting the appropriate bit high enables the correct LOADCLK timing for that panel. When both these bits are low, the generic LOADCLK timing is selected. The generic LOADCLK timing is valid for most LCD panels other than Toshiba or Sharp.

2.5.4 CGA and AT&T Compatibility Registers

The following registers are provided for CGA and AT&T mode compatibility. The Mode Select Registers and Status Register are used by software to control the mode and check the status of the display.

Name: Mode Select Register A

Type: Read/Write

Address: 3D8H

Bit	Name	Default	Function
D[7:6]	Reserved	00	Reserved bits
D5	BLINK	0	0 - MSB of Attribute Byte is intensity 1 - MSB of Attribute Byte is blink
D4	GRES0	0	0 - 320x200 APA 1 - 640x200 or 640x200 APA
D3	VIDE	0	0 = Video disabled 1 = Video enabled <i>Note: Used by power management logic only, does not actually control video.</i>
D2	Reserved	0	Reserved bit
D1	GRAPH	0	0 = Character mode 1 = Graphics mode
D0	CRES	0	0 = 40x25 Alpha 1 = 80x25 Alpha

In text mode, the BLINK bit (D5) is used to identify the function of the most significant bit of the character Attribute Byte. When this bit is reset low, The Attribute Byte MSB controls the intensity of the character. When this bit is set high, the MSB of the character Attribute Byte controls the character blink.

GRES0 (bit D4), GRAPH (bit D1), and CRES (bit D0) are used in conjunction with GRES1 (bit D0) of the Mode Select Register B, to control the AT&T mode of display. VIDE (bit D3) is used by the VG-230 PMU to determine whether the LCD panel should be turned on or off.

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

Name: Status Register
 Type: Read/Write
 Address: 3DAH

Bit	Name	Default	Function
D[7:4]	Reserved	FH	Reserved bits
D3	VSYNC	0	Simulated vertical retrace time
D2	Reserved	1	Reserved bit
D1	Reserved	0	Reserved bit
D0	Hsync	0	Simulated horizontal retrace time

This register provides software with the status of the vertical and horizontal retrace. VSYNC (bit D3) gets set to simulate a vertical retrace. HSYNC (bit D0) gets set to simulate a horizontal retrace.

Name: Mode Select Register B
 Type: Read/Write
 Address: 3DEH

Bit	Name	Default	Function
D7	Reserved	0	Reserved bit
D6	UNDRLN	0	0 = Underline disabled, grayscaling enabled 1 = Underline enabled, grayscaling disabled
D[5:4]	Reserved	00	Reserved bits
D3	PAGSEL	0	0 = Select low page for display 1 = Select high page for display
D[2:1]	Reserved	00	Reserved bits
D0	GRES1	0	0 = 640x200 APA, two 16K alpha pages. 1 = 640x400 APA, one 32K alpha page.

UNDRLN (bit D6) is used to enable and disable underlining and gray scaling. PAGSEL (bit D3) is used in AT&T mode to select which 16K page of video memory is to be used for the display.

GRES1 (bit D0) is used in AT&T mode to select the number and size of the display memory pages available. It is also used in conjunction with the GRES0, GRAPH, and CRES bit of the Mode Select Register A to determine the AT&T display mode. Table 2.5-1 shows the combinations of these signals needed to select the AT&T modes.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

AT&T Mode Selection

GRAPH	CRES	GRES1	GRES0	Mode
0	0	X	X	40X25 Alpha
0	1	X	X	80X25 Alpha
1	X	X	0	320X200 APA
1	X	0	1	640X200 APA
1	X	1	1	640X400 APA

Table 2.5-1

2.5.5 Interfacing to LCD panels

The hardware interface to the LCD involves two parts. The first is the power supply. Most panels require a main VCC power and also a negative bias voltage, which we will call VBIAS. It is important to sequence the power correctly to the panel to avoid damaging latchup conditions. The VG-230 provides this power sequencing with VPLCD and VPBIAS. Figure 2.5-1 illustrates the power supply interface to the LCD panel.

The second part of the interface involves the actual display signals. The VG-230 supplies the following pins:

- | | |
|------------------|--|
| FRAME | - The FRAME clock. Indicates that line of pixels just transferred is the first line of a new frame. |
| LOCLK | - LCD Line load clock. Indicates that one line of pixels has been transferred to LCD |
| M | - AC drive to LCD panel. Square wave required by some LCDs Period equals two Frame times. |
| LCDL[0:3] | - Lower LCD Data bits. Used for 400 line panels only. Used for the lower 4 bits of a 400 line panel. |
| LCDU[0:3] | - Upper LCD Data bits. Used for all single screen panels. |
| SHCLK | - LCD Data shift clock. Clocks LCDL[0:3] and LCDU[0:3] on the falling edge. |

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

LCD SIGNAL INTERFACE

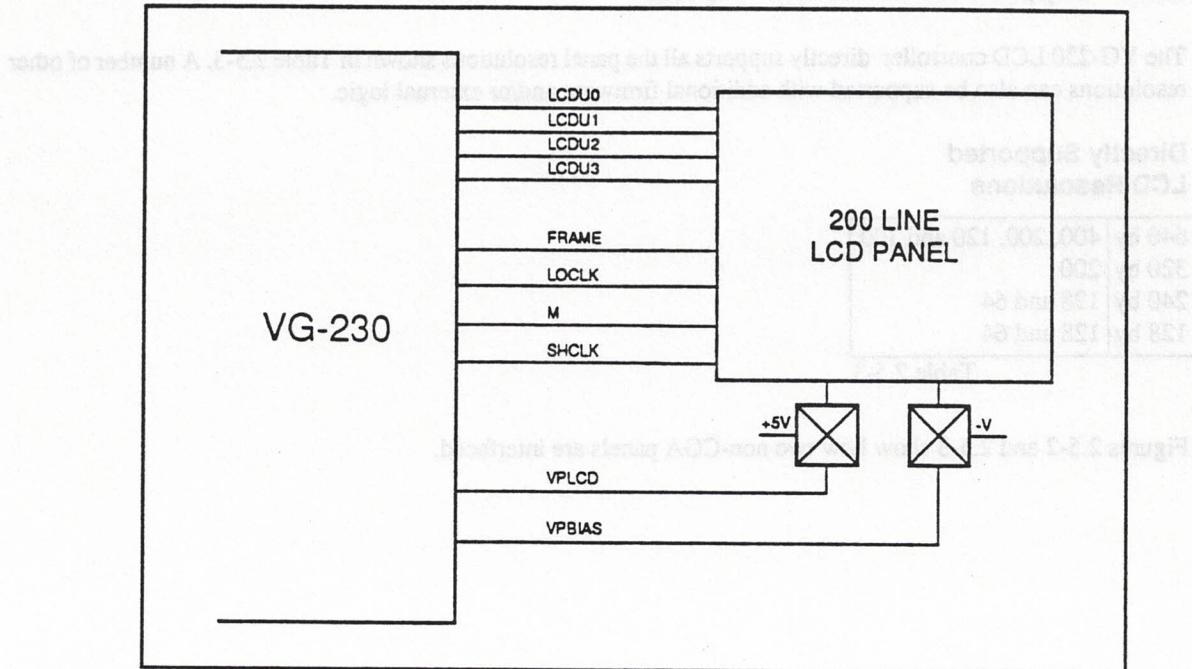


Figure 2.5-1

LCD Data Bit Interface

LCD DATA BUS WIDTH			
Pin Number	4 Bit	2 Bit	1 Bit
95	LCDU0	LCDU0	LCDU0
96	LCDU1	LCDU1	n/c
97	LCDU2	n/c	n/c
98	LCDU3	n/c	n/c

Table 2.5-2

2.5.6 Support for Small LCD Panels

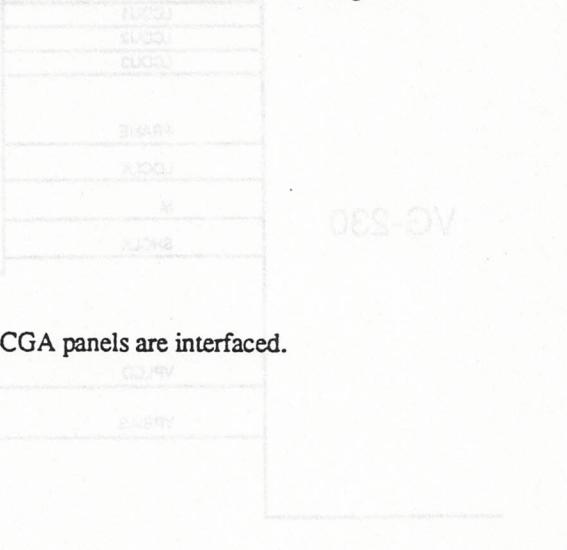
The VG-230 LCD controller directly supports all the panel resolutions shown in Table 2.5-3. A number of other resolutions can also be supported with additional firmware and/or external logic.

Directly Supported LCD Resolutions

640 by 400	400, 200, 120 and 100
320 by 200	
240 by 128	128 and 64
128 by 128	128 and 64

Table 2.5-3

Figures 2.5-2 and 2.5-3 show how two non-CGA panels are interfaced.



LCD DATA BUS WIDTH				
Panel Type	1 bit	2 bits	4 bits	8 bits
PCB10	PCD10	PCD10	PCD10	PCD10
PCB11	PCD11	PCD11	PCD11	PCD11
PCB12	PCD12	PCD12	PCD12	PCD12
PCB13	PCD13	PCD13	PCD13	PCD13
PCB14	PCD14	PCD14	PCD14	PCD14

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

VG-230 SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

400 LINE LCD PANEL INTERFACE

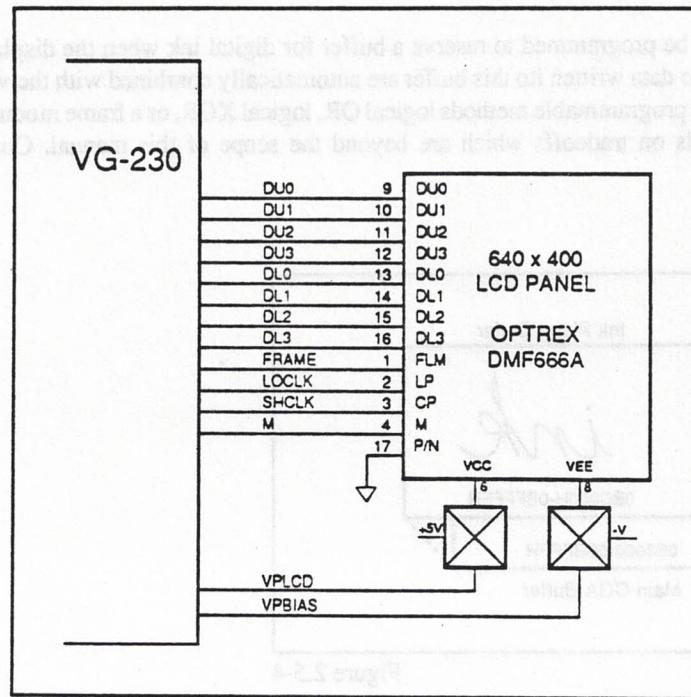


Figure 2.5-2

240 X 128 LCD PANEL INTERFACE

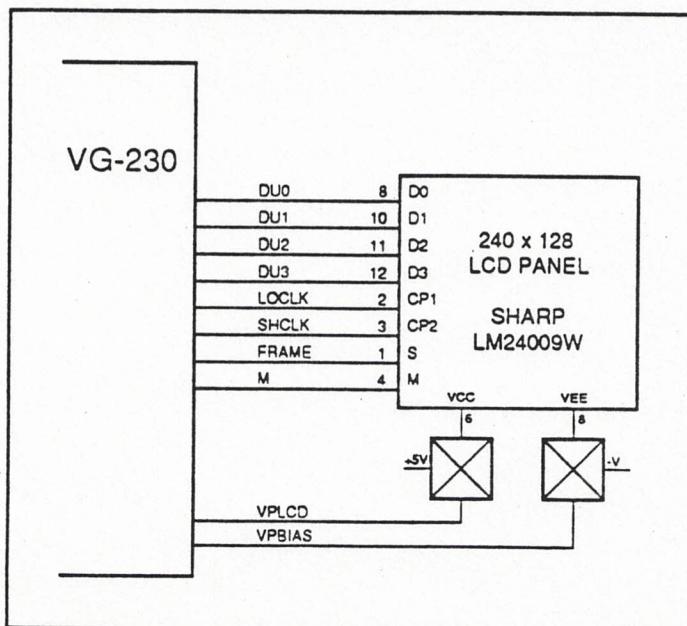


Figure 2.5-3

2.5.7 INK PLANE FEATURE

The VG-230 can be programmed to reserve a buffer for digital ink when the display panel size is 200 lines or smaller. The video data written into this buffer are automatically combined with the video data in the CGA buffer using one of three programmable methods logical OR, logical XOR, or a frame modulation technique. Which one to choose depends on tradeoffs which are beyond the scope of this manual. Contact Vadem for additional information.

INK PLANE

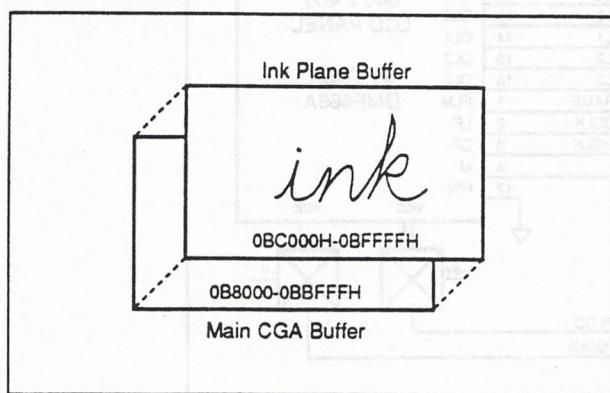


Figure 2.5-4

The Ink Plane Register is found at index CDH.

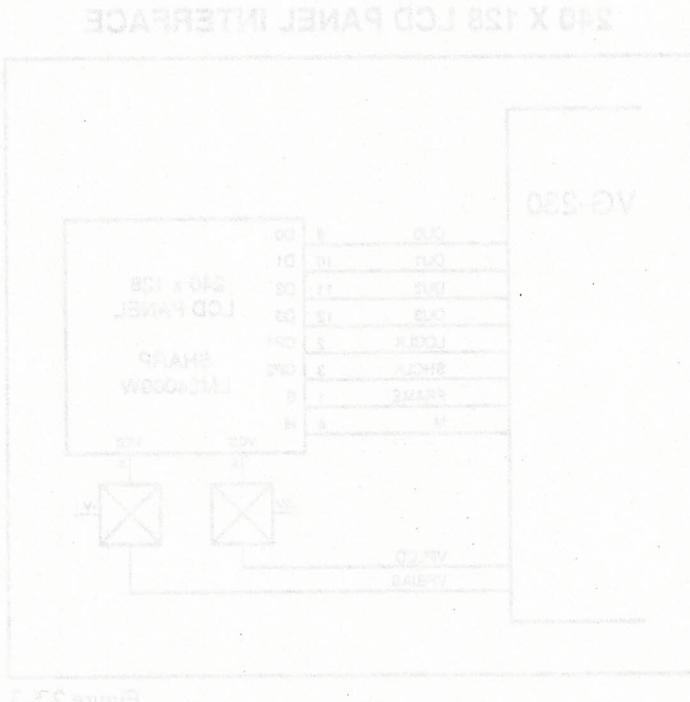


Figure 2.5-5

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TECHNICAL REFERENCE

2.6 Power Management

The VG-230 contains a Power Management Unit (PMU) derived from the field-proven VG-647 PMU. The PMU is responsible for controlling power and clocks to various function blocks of the VG-230 and its external subsystems. Total operation power is reduced automatically during periods of inactivity. Inactivity is determined by hardware in the PMU or through software control.

2.6.1 Vadem PMU modes

The PMU has five states: On, Doze, Sleep, Suspend and Off. Each one of the states controls certain power consuming devices to reduce the overall system power consumption. These states and the controlled devices are shown in Table 2.6-1 below.

VG-230 Power Management Modes

	VG-230	LCD	RAM	ROM	CPU CLOCK	CPU OSC
ON	On	On*	On*	On*	Full	On
DOZE	On	On*	On*	On*	Reduced or Off*	On
SLEEP	On	Off*	On*	On*	Reduced or Off*	On
SUSPEND	On	Off*	On*	Off*	Off	Off
OFF	On	Off	Off	Off	Off	Off

Table 2.6-1

- * These ON, reduced, or OFF states are programmable through PMU Control Register, PMU Power Registers and PMU Resume Register.

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TECHNICAL REFERENCE

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State transitions are initiated from a variety of sources. See Figure 2.6-1 for a state diagram of the VG-230 PMU.

VG-230 PMU STATE DIAGRAM

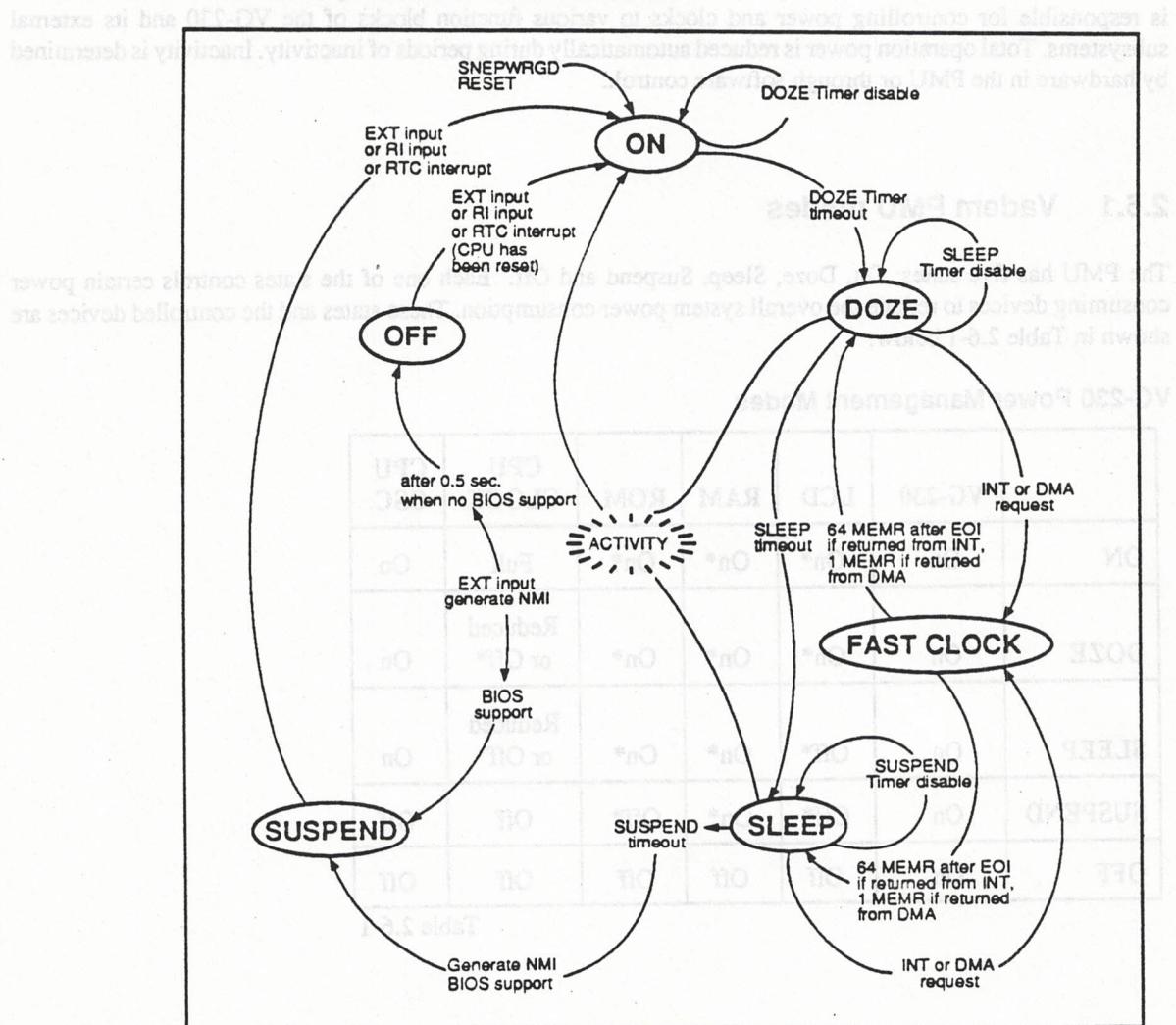


Figure 2.6-1

The present state of the system can be determined by decoding the STATE bits in the PMU status register located at index C0H.

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SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

2.6.1.1 The ON State

The ON state is the full power, full performance state of the VG-230 system. To conserve maximum power it is desirable to remain in the ON state only during computational intensive periods. During the ON state, all I/O peripherals are powered up with clocks supplied.

2.6.1.2 The DOZE State

The DOZE state is the first level of power management. DOZE state is typically entered within a few seconds of inactivity. It is entered when the DOZE timer at index CCH expires. The DOZE state reduces the operating frequency of the internal V30HL CPU. This reduction is controlled by the DOZE divider value specified in the PMU Resume Status Register located at index DAH. Any write to this register also enables the EXT NMI.

Name: PMU Resume Status Register

Type: Read/Write

Address: INDEX DAH

Bit	Name	Default	Function
D[7:2]	Reserved	00H	Reserved bits
D1	PMUREF	0	Read only bit polled by software to determine the end of the Resume Operation. 1 = PMU Refreshing
D0	CLKSPD	0	CPU Clock speed divider during DOZE or SLEEP mode. 0 = divided by 4; 1 = divided by 8.

The DOZE state can be entered through program control by writing the DOZE command to the STATUS register at index C0H. DOZE state exits to the ON state when activity is detected. DOZE state exits to the SLEEP state when the SLEEP timer expires. Activity type is determined from the PMU Activity Status Register (DBH).

Name: PMU Activity Status Register

Type: Read Only

Address: INDEX DBH

Bit	Name	Default	Function
D7	IORNGACT	0	Activity to programmable I/O range
D6	VIDACT	0	Video memory activity
D5	HDACT	0	Hard disk I/O activity
D4	FLPACT	0	Floppy I/O activity
D3	COMACT	0	COM1/COM2 activity
D2	RTCACT	0	I/O Address 70-71H activity
D1	KBDACT	0	Keyboard I/O activity
D0	PIOACT	0	LPT1/LPT2/LPT3 I/O activity

Note: The activity status register is cleared following deassertion of the SNEPWRGD signal, or after being read by the CPU.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

Name: PMU DOZE Timer Register

Type: Read/Write

Index: CCH

Bit	Name	Default	Function			
D[7:4]	Reserved	0000	Reserved bits			
D[3:0]	DOZTM[3:0]	1010	Bit	Time	Bit	Time
			0000	Disabled	1000	1 sec
			0001	1/8 sec	1001	2 sec
			0010	1/4 sec	1010	4 sec
			0011	3/8 sec	1011	6 sec
			0100	1/2 sec	1100	8 sec
			0101	5/8 sec	1101	10 sec
			0110	3/4 sec	1110	12 sec
			0111	7/8 sec	1111	14 sec

2.6.1.3 The SLEEP State

SLEEP state is the lowest power state available without going into the SUSPEND state. Sleep is typically entered within 2 - 5 minutes after the DOZE state. There are three ways to enter the SLEEP state:

- 1) Under program control from the DOZE state when the SLEEP timer times out and generates an NMI as a result of lack of activity. This will be referred to as NMI SLEEP state.
- 2) Under program control from the ON or DOZE state at any time.
- 3) Automatically from the slow clock DOZE state when the SLEEP timer times out as a result of lack of activity.

SLEEP State Via NMI

This mode of SLEEP state is software controlled. This allows power control of I/O devices with register controlled power down modes. To enable NMI SLEEP mode, unmask the SLEEP timeout bit (bit 4) in the NMIMASK register (C4H).

When the SLEEP timer expires, an NMI is generated to inform the BIOS that it's time to power down certain parts of the system. The NMI handler would interrogate the VG-230 STATUS register cause code and determine that the SLEEP state NMI has been generated. The NMI routine will reset the NMI by clearing the NMI cause code in the STATUS register. The NMI is cleared by reading the NMI register at index C4H. At this point the BIOS needs to mask the activity monitor to prevent exiting the DOZE state when powering down devices. The BIOS now puts devices in the low power mode. Now the activity monitor can be re-enabled. The BIOS will then put the VG-230 into SLEEP state by setting SLEEP state in the STATUS register.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

SLEEP State Via Software Command

This method of entering the SLEEP state involves writing the SLEEP command directly to the STATUS register at index C0H. SLEEP can be entered from the ON or DOZE states at any time through this method.

Automatic SLEEP State

Automatic SLEEP state can be entered automatically via the SLEEP timer. When no activity is detected for the time specified in the PMU SLEEP Timer register at index CDH and the NMI SLEEP timeout bit is masked in the NMIMASK register, the PMU will enter the SLEEP mode. In the SLEEP mode, the LCD and the PC card can be powered down. The SLEEP state also maintains the reduced clock to the CPU. The SLEEP state is exited through the detection of activity or through software command.

When the BIOS puts the VG-230 into SLEEP state, power to the LCD can be controlled. Selection of the LCD or Card power off during SLEEP state is controlled through the PWRSLEEP register. SLEEP state will maintain the reduced clock mode of the DOZE state.

Name: PMU SLEEP Timer Register

Type: Read/Write

Index: CDH

Bit	Name	Default	Function			
D[7:4]	Reserved	0000	Reserved bits			
D[3:0]	SLPTM[3:0]	0010	Bit	Time	Bit	Time
			0000	Disabled	1000	8 min
			0001	1 min	1001	9 min
			0010	2 min	1010	10 min
			0011	3 min	1011	11 min
			0100	4 min	1100	12 min
			0101	5 min	1101	13 min
			0110	6 min	1110	14 min
			0111	7 min	1111	15 min

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

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SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

2.6.1.4 The SUSPEND State

The VG-230 supports the saving of all external chip status to memory for resumption at a later time. This is called SUSPEND/RESUME. The SUSPEND state can be user-invoked via a signal on the EXT pin or automatically invoked by via the SUSPEND timer. The BIOS detects a request to enter SUSPEND state through an NMI. The BIOS then interrogates the VG-230 STATUS register to determine if the NMI is the result of a SUSPEND request. After allowing the system to finish any DMA or interrupt activity it then saves the system status. The BIOS is also responsible for saving the states of all external devices to non-volatile memory. The BIOS sets the SUSPEND status field in the STATUS register located at index C0H. At this point the VG-230 enters SUSPEND state. Power control devices activated by VP pins will be turned off according to the PWRSUSPEND register.

The BIOS command to SUSPEND is followed by a loop which polls the PMU Status Register, looking for the WAKEUP state.

Less than 15 microseconds of instructions may be executed between the BIOS command to SUSPEND and the moment the clock is actually stopped.

SUSPEND Via Hardware Timeout

The following procedure describes the entrance into SUSPEND state via an internal hardware timer (SUSPEND timer).

- 1) Enable SUSPEND timer by writing a non-zero value to the SUSPEND register at index CEH.
- 2) Enable SUSPEND NMI by clearing bit 5 of the NMIMASK register at index C4H.

An NMI will be generated after the VG-230 is in the SLEEP state for the time specified in the SUSPEND REGISTER.

- 3) After the NMI is received, the STATUS register should be read to determine the NMI source. The NMI is cleared by reading the NMIMASK register at index C4H.
- 4) Save system status and place VG-230 into SUSPEND state by writing the PMU Status Register.
- 5) The CPU should wait until the WAKEUP CODE is present in the PMU Status Register and PMUREF is low in the PMU Reserve Status Register.
- 6) Restore system and VG-230 status.

SUSPEND Via EXT Input

The following procedure describes the entrance into SUSPEND state via an external switch input (EXT input).

- 1) Enable EXT NMI by clearing bit 1 of the NMIMASK register at index C4H. An NMI will be generated after the VG-230 detects a positive transition on the EXT input.

Follow steps 3 to 6 above.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

SUSPEND Via Software Command

The system may be placed into the SUSPEND mode from the ON, DOZE or SLEEP state by writing a 03H into the STATUS register (index C0H). Software should follow the procedure outlined above.

RESUME

The VG-230 will enter the ON state when one of the following events happens: an EXT input, a Real Time Clock Alarm Input, or a modem Ring Indicate.

The RESUME source identification will be stored in the WU[1:0] status located in the STATUS register. Normally, RESUME does not reset the CPU. The CPU will restart executing the code it was executing when it was suspended.

The BIOS is responsible for reading the RESUME bit in the STATUS register to determine if a cold boot or return from SUSPEND is requested. If return from SUSPEND is indicated, the BIOS should restore any external devices and verify that the main memory and video memory is still valid. If main memory, video memory or I/O is corrupted, then a cold boot should be performed. Otherwise RESUME can be continued. Note that reading the RESUME bit in the STATUS register resets the RESUME bit.

Name: PMU SUSPEND Timer Register

Type: Read/Write

Index: CEH

Bit	Name	Default	Function			
D[7:4]	Reserved	0000	Reserved bits			
D[3:0]	SUSTM[3:0]	0000	Bit	Time	Bit	Time
			0000	Disabled	1000	40 min
			0001	5 min	1001	45 min
			0010	10 min	1010	50 min
			0011	15 min	1011	55 min
			0100	20 min	1100	60 min
			0101	25 min	1101	65 min
			0110	30 min	1110	70 min
			0111	35 min	1111	75 min

VADEM VG-230

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TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

2.6.1.5 The OFF State

The OFF state is similar to the SUSPEND state, except that the DRAM refresh feature is disabled. The OFF state is used when the contents of the system RAM are not required. In the OFF state, the VG-230's RTC and internal CMOS RAM are maintained. Transition from the OFF state to the ON state results only in resetting the CPU. This transition is treated by the BIOS as a cold boot.

2.6.1.6 Power Management Status

The BIOS can interrogate the state of power management by checking the value of the STATE bits located in the PMU Status Register at index C0H. Bits D0 and D1 reflect the current state of the PMU. These bits can also be written to force the PMU into the desired state.

PMU Suspend/Resume Register							
		Function		Default	Value	Index	Bit
		Register		0000	0000	C0H	D(1:0)
func	BS	func	BS	0000	0000		
min 00	0001	func 00	BS	0000			
min 01	1001	func 01	BS	1000			
min 02	0101	func 02	BS	0100			
min 03	1101	func 03	BS	1100			
min 04	0011	func 04	BS	0010			
min 05	1011	func 05	BS	1010			
min 06	0111	func 06	BS	0110			
min 07	1111	func 07	BS	1110			

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

Name: PMU STATUS Register

Type: Read/Write

Index: C0H

Bit	Name	Default	Function
D7	Resume	0	Resuming from SUSPEND (warmstart)
D[6:5]	WU[1:0]	00	Wakeup code bits
D[4:2]	NMI[2:0]	000	NMI cause code bits
D[1:0]	STATE[1:0]	00	State bits

Note: Only D0 and D1 are affected by a write.

State Code									Function
7	6	5	4	3	2	1	0		
X	X	X	X	X	X	0	0	command to ON	
X	X	X	X	X	X	0	1	command to DOZE	
X	X	X	X	X	X	1	0	command to SLEEP	
X	X	X	X	X	X	1	1	command to SUSPEND	
1	1	1	1	1	1	1	1	command to OFF	

Note: The NMI cause, state and wakeup codes are decoded as follows for a read to C0H.

Wakeup	NMI		State		
	Code	Cause	Code	Cause	
00	None	000	None, or INMI	00	ON
01	EXT	001	EXT	01	DOZE
10	RTC	010	LB	10	SLEEP
11	RI	011	Reserved	11	SUSPEND
		100	SLEEP Timeout		
		101	SUSPEND Timeout		
		110	SLEEP to ON (Activity)		
		111	Reserved		

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2.6.2 Activity Monitor

The activity monitor determines when the PMU changes states. The activity monitor can monitor access to the following PC I/O devices:

Activity Monitor Address

Parallel Printer Port		I/O R/W access to LPT1-LPT3	0	0	0	0	0
LPT1		378H - 37FH	X	X	X	X	X
LPT2		278H - 27FH	X	X	X	X	X
LPT3		3BCH - 3BEH	X	X	X	X	X
Keyboard Port		I/O Reads to port 60H					
Real Time Clock		I/O R/W access to port 70H/71H					
Serial I/O		I/O R/W access to COM1 and COM2	X	X	X	X	X
COM1		3F8H - 3FFH	X	X	X	X	X
COM2		2F8H - 2FFH	X	X	X	X	X
Floppy Disk		I/O R/W access to 3F5H	X	X	X	X	X
Hard Disk		I/O R/W access to XT or AT hard disk					
XT Disk		320H - 323H					
AT Disk		1F0H - 1F8H					
Video Memory Access		Access to CGA video memory					
Programmable I/O		See description of PMU I/O Range register IORNG					

Table 2.6-2

Note: The Real Time Clock activity bit does not monitor access to the VG-230's internal real time clock. Access to the standard "PC/AT" RTC at I/O address 70H/71H is monitored. If the designer wishes to trigger the activity monitor for accesses to the VG-230's internal RTC, the RTC's BIOS routine can do a "dummy" read from 70H or 71H.

VADEM VG-230

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TECHNICAL REFERENCE

Name: **PMU ACTIVITY MASK Register**

Type: **Read/Write**

Index: **C3H**

Bit	Name	Default	Function
D7	MSK_IORNG	1	Mask access to I/O ports defined by IORNG[6:0]
D6	MSK_VIDM	0	Mask access to video memory
D5	MSK_HD	0	Mask access to hard disk I/O
D4	MSK_FLP	0	Mask access to port 3F5
D3	MSK_SIO	0	Mask access to COM 1-2
D2	MSK_RTC	1	Mask access to port 70H, 71H
D1	MSK_KBD	0	Mask keyboard port 60H reads
D0	MSK_PIO	0	Mask access to LPT 1, 2, 3

Note: The activity monitor ACTIVITY output is the logical OR of all unmasked activity sources. This register affects only the ACTIVITY output.

Name: **PMU I/O RANGE (IORNG) Register**

Type: **Read/Write**

Index: **C5H**

Bit	Name	Default	Function
D7	RNGSIZE	0	0 = 16 byte range, 1 = 8 byte range
D6	IORNG6	0	Maskable I/O range base
D5	IORNG5	0	Maskable I/O range base
D4	IORNG4	0	Maskable I/O range base
D3	IORNG3	0	Maskable I/O range base
D2	IORNG2	0	Maskable I/O range base
D1	IORNG1	0	Maskable I/O range base
D0	IORNG0	0	Maskable I/O range base

Note: IORNG[6:0] are the base address bits A[9:3] for the maskable I/O port range in the activity monitor. RNGSIZE is the size of the range. IORNG0 is ignored when RNGSIZE is low.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

The status of the activity monitor can be checked via the ACTIVITY bit in the PMU Supply register. If this bit is set, activity has occurred since the last read of this register. If the ACTIVITY bit is set, the source of the activity can be determined by reading the PMU activity register at index DBH. All bits in the PMU activity register are cleared after being read.

Name: **PMU Activity Status Register**
 Type: **Read Only**
 Index: **DBH**

Bit	Name	Default	Function
D7	IORNGACT	0	Activity to programmable I/O range
D6	VIDACT	0	Video memory activity
D5	HDACT	0	Hard disk I/O activity
D4	FLPACT	0	Floppy I/O activity
D3	COMACT	0	COM1/COM2 activity
D2	RTCACT	0	I/O Address 70-71H activity
D1	KBDACT	0	Keyboard I/O activity
D0	PIOACT	0	LPT1/LPT2/LPT3 I/O activity

Note: The activity status register is cleared following deassertion of the SNEPWRGD signal, or after being read by the CPU.

Bit	Name	Default	Function
D7	RNGRS8	0	Activity to programmable I/O range
D6	IORNG9	0	Video memory activity
D5	IORNG10	0	Hard disk I/O activity
D4	IORNG11	0	Floppy I/O activity
D3	IORNG12	0	COM1/COM2 activity
D2	IORNG13	0	Keyboard I/O activity
D1	IORNG14	0	LPT1/LPT2/LPT3 I/O activity
D0	IORNG15	0	Activity to programmable I/O range

Note: IORNG[0-15] are the six available pins A15:0 for the programmable I/O port. IORNG15 is the size of the large IORNG0 through IORNG7.

VADEM VG-230

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TECHNICAL REFERENCE

2.6.3 Power Control Registers

Each power management mode has an associated power control register. These registers determine the state of the power control pins (VP pins) during the various modes. The power control registers are 8 bits in width, however only 4 of these bits are used in the VG-230. See section 2.7 for details.

Bit	Description
0	VPLCD and VPBIAS control
1	Not used
2	VPSYS control
3	VPCARD control
4	Not used
5	Not used
6	Not used
7	VPRAM control

The power registers are as follows:

PWRON	at C5H	with a default of FFH
PWRDOZE	at C6H	with a default of FFH
PWRSLEEP	at C7H	with a default of 8CH
PWRSSUSPEND	at C8H	with a default of 80H

The default polarity of each power control bit is high true except polarity of VP0, but may be changed individually by programming the PMU POLARITY register (index CAH). This is primarily intended to simplify LCD power control logic. After a hard reset, the VG-230 automatically tri-states the VPLCD and VPBIAS outputs so that external pullup or pulldown resistors (depending on polarity) on the VPLCD and VPBIAS controls can force the power control devices to their off state. This allows firmware to set power control bit polarity to low true if appropriate. LCD power-up sequencing after hard reset begins only after both the SEQEN bit of the PMU LCD Sequence Register (D4H) and the VIDE bit of the Mode Select Register A (3D8H) are set high. VPSYS, VPRAM and VPCARD are not tri-stated by the VG-230.

2.6.4 Power Sequencing

In power management modes SLEEP, SUSPEND and OFF the VG-230 itself remains powered at all times. As a result, care must be taken when configuration VG-230 pins during these modes, both to protect the system against possible latch-up and to prevent excessive current consumption.

In general, all output pins are driven Hi-Z while power to devices connected to them is removed. The exceptions are A[25:0] and D[15:0], which will be driven low during SUSPEND to prevent excessive current consumption of the system RAM. An internal signal from the power management unit (PMU) called *CLAMP controls the state of A[25:0] and D[15:0]. During OFF mode, these pins will be driven Hi-Z along with the rest of the VG-230's pins.

Entering SUSPEND Mode (DRAM/PSRAM systems)

For DRAM and PSRAM systems, when software commands the PMU into the SUSPEND mode, the PMU begins its SUSPEND sequence.

- On the rising edge of *DACK0 (Internal refresh signal), the PMU takes control of the memory interface.
 - Internally the refresh clock is switched from the main 32MHz clock to the 32.768KHz clock
 - On the falling edge of PWGOUT, the internal CPUCLK is stopped.
 - The *RESOUT pin is driven low.
 - All VG-230 output pins are driven Hi-Z, including A[25:0] and D[15:0].
 - Following the completion of the Burst refresh cycle, the PMU will drive the VPSYS pin inactive and begin generating refresh cycles timed from the 32KHz clock. The 32MHz oscillator will continue to run until the power sequencing to the LCD is complete.
 - Approximately 1 second after VPSYS is driven inactive, the PMU will assert an internal *CLAMP signal. At this time the A[25:0] and D[15:0] pins will be switched from Hi-Z to low driven outputs and the transition from ON to SUSPEND will complete.

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

ENTERING / EXITING SUSPEND - DRAM SYSTEM

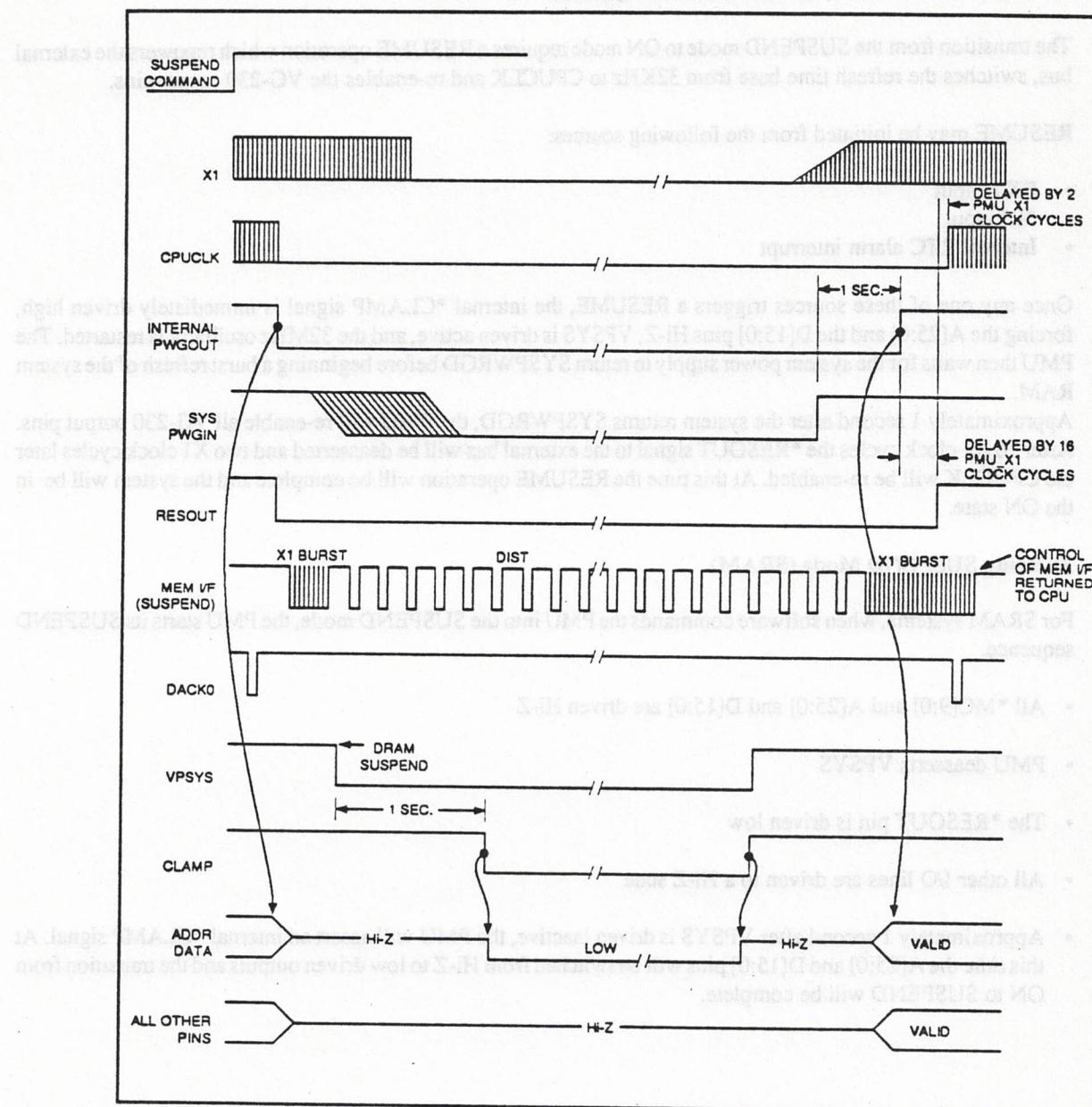


Figure 2.6-2

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

Exiting SUSPEND mode (DRAM/PSRAM systems)

The transition from the SUSPEND mode to ON mode requires a RESUME operation which repowers the external bus, switches the refresh time base from 32KHz to CPUCLK and re-enables the VG-230 output pins.

RESUME may be initiated from the following sources:

- EXT input
- *RI input
- Internal RTC alarm interrupt

Once any one of these sources triggers a RESUME, the internal *CLAMP signal is immediately driven high, forcing the A[25:0] and the D[15:0] pins Hi-Z, VPSYS is driven active, and the 32MHz oscillator is restarted. The PMU then waits for the system power supply to return SYSPWRGD before beginning a burst refresh of the system RAM.

Approximately 1 second after the system returns SYSPWRGD, the PMU will re-enable all VG-230 output pins. After 16 X1 clock cycles the *RESOUT signal to the external bus will be deasserted and two X1 clock cycles later the CPUCLK will be re-enabled. At this time the RESUME operation will be complete and the system will be in the ON state.

Entering SUSPEND Mode (SRAM)

For SRAM systems, when software commands the PMU into the SUSPEND mode, the PMU starts its SUSPEND sequence.

- All *MC[9:0] and A[25:0] and D[15:0] are driven Hi-Z
- PMU deasserts VPSYS
- The *RESOUT pin is driven low
- All other I/O lines are driven to a Hi-Z state
- Approximately 1 second after VPSYS is driven inactive, the PMU will assert an internal *CLAMP signal. At this time the A[25:0] and D[15:0] pins will be switched from Hi-Z to low driven outputs and the transition from ON to SUSPEND will be complete.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

ENTERING / EXITING SUSPEND - SRAM / PSRAM SYSTEM

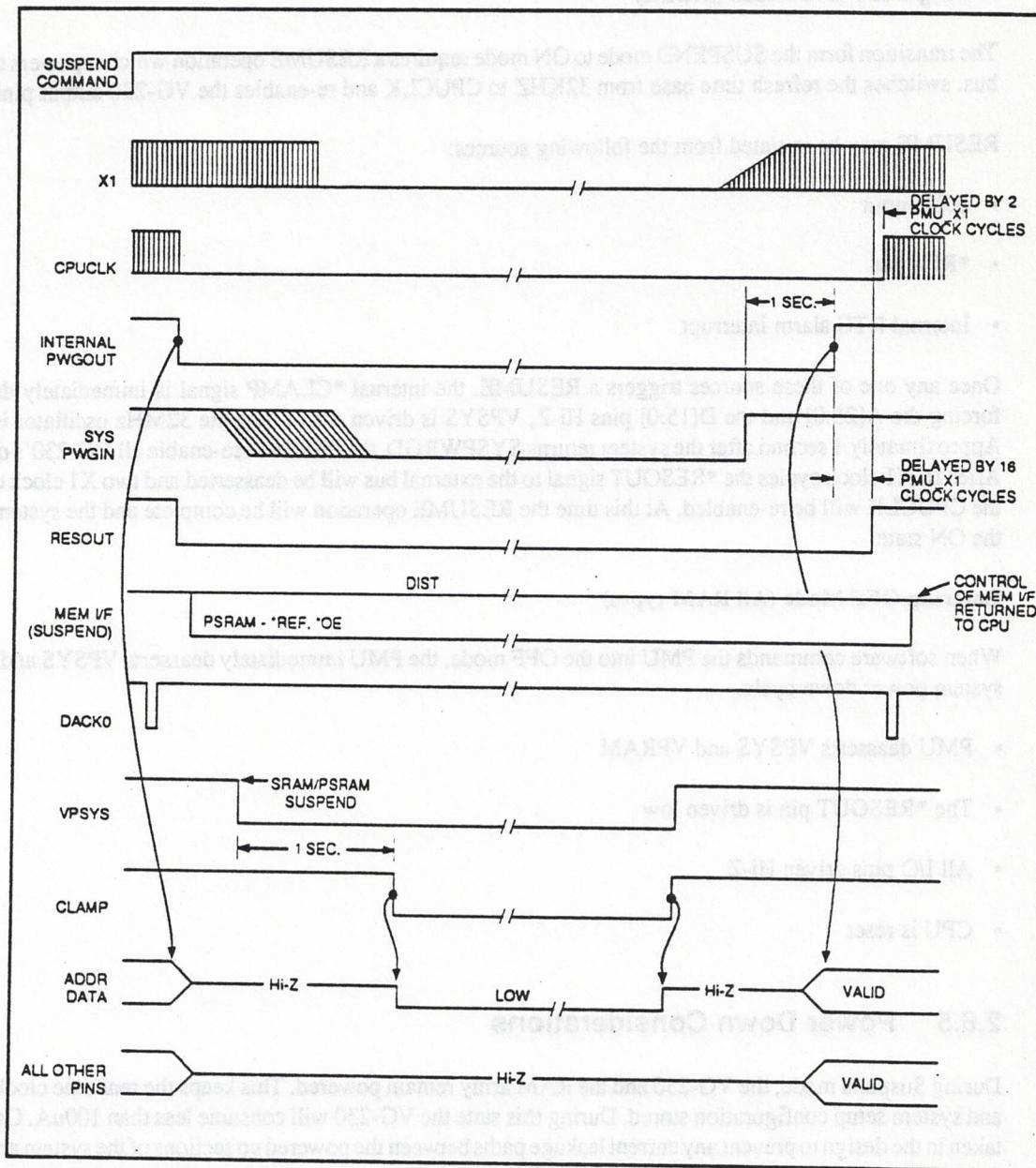


Figure 2.6-3

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

VADEM AG-S80
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

Exiting SUSPEND Mode (SRAM)

The transition from the SUSPEND mode to ON mode requires a RESUME operation which repowers the external bus, switches the refresh time base from 32KHZ to CPUCLK and re-enables the VG-230 output pins.

RESUME may be initiated from the following sources:

- EXT input
- *RI input
- Internal RTC alarm interrupt

Once any one of these sources triggers a RESUME, the internal *CLAMP signal is immediately driven high, forcing the A[25:0] and the D[15:0] pins Hi-Z, VPSYS is driven active, and the 32MHz oscillator is restarted. Approximately 1 second after the system returns SYSPWRGD, the PMU will re-enable all VG-230's output pins. After 16 X1 clock cycles the *RESOUT signal to the external bus will be deasserted and two X1 clock cycles later the CPUCLK will be re-enabled. At this time the RESUME operation will be complete and the system will be in the ON state.

Entering OFF Mode (All RAM types)

When software commands the PMU into the OFF mode, the PMU immediately deasserts VPSYS and begins the system power down cycle.

- PMU deasserts VPSYS and VPRAM
- The *RESOUT pin is driven low
- All I/O pins driven Hi-Z
- CPU is reset

2.6.5 Power Down Considerations

During Suspend mode, the VG-230 and the RAM array remain powered. This keeps the real time clock operating and system setup configuration stored. During this state the VG-230 will consume less than 100uA. Care must be taken in the design to prevent any current leakage paths between the powered up sections of the system and powered down. The VG-230 leakage control circuitry drives certain inputs to prevent excessive current consumption. Also certain outputs are driven low or tri-stated to terminate inputs outside of the VG-230.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

2.6.6 Low Battery Input (LB)

A single Low Battery Input (LB) provides monitoring for the primary battery source. The LB input is a standard TTL level input, to which an external comparator circuit should supply a low level when the battery condition is at a good level. A high on LB input will initiate an NMI within 15 seconds if the LB NMI bit in the NMIMASK register is unmasked. When the LB input stays high and is not masked, the LB interrupts will be generated every 60 seconds. The status of the Low Battery Input can be read in the PMU Supply Register (index C1H).

Name: PMU Supply Register
Type: Read Only
Index: C1H

Bit	Name	Default	Function
D[7:4]	Reserved	0H	Reserved bits
D3	ACTIVITY	0	System activity
D2	Reserved	0	Reserved bit
D1	LB	X	Low battery
D0	LOCKOUT	1	Register write protected

High Time Clock Active Wake-Up Features

The Vadem VG-230 has two high time clock active wake-up features. The first is a high time clock active wake-up feature that is triggered by a logic high on the HSWC pin. This feature is controlled by the HSWC bit in the HSWC register. The second is a high time clock active wake-up feature that is triggered by a logic high on the HSWC2 pin. This feature is controlled by the HSWC2 bit in the HSWC2 register. Both features are controlled by the HSWC bit in the HSWC register.

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

2.6.7 Modem Ring Indicator Input (RI)

The VG-230 can be placed into the ON state from the OFF or SUSPEND state through the modem ring-in signal. The signal must be supplied as a TTL level signal and be a filtered square wave. The RI input is a positive edge triggered input. The VG-230 will go into the ON state after the number of positive transitions on the RI line specified in the PMU CONTROL register (index C2H). If not used, the RI input should be tied low.

Name: PMU Control Register
Type: Read/Write
Index: C2H

Bit	Name	Default	Function	
D7	FSTCLK0	0	1 = Disable clock slow down in DOZE and SLEEP modes	
D[6:4]	RING[2:0]	001	Bits	RI pulses required for turn-on
			000	Disable RI
			001	1
			010	2
			011	3
			100	4
			101	5
			110	6
			111	7
D3	STATIC	0	Static CPU and RAM, clock stops in DOZE and SLEEP	
D2	SLWREF	0	1 = slow refresh	
D[1:0]	Reserved	00	Reserved bit	

2.6.8 Real Time Clock Alarm Wake-Up Feature

The VG-230 can be placed into the ON state from the OFF or SUSPEND state through the internal RTC alarm. The alarm is enabled through the Real Time Clock configuration registers. See section 2.11.2 for more information on the RTC alarm feature.

2.6.9 Suspend Mode Support of DRAM Refresh

Refresh pulses are generated automatically in the SUSPEND state when the DRAM memory type is selected. When the BIOS places the VG-230 into the SUSPEND mode, a power down sequence is initiated. All *CAS lines are driven low and the VG-230 begins generating CAS before RAS refresh cycles. *RAS cycles are generated every 15µS. If the SLWREF bit in PMU control register at index C2H is set, the VG-230 supplies refresh pulses every 120µS. During the SUSPEND state all Address lines during these DRAM cycles are clamped low. Data lines are forced to tri-stated.

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VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

When the VG-230 exits the SUSPEND mode into the ON mode, the VG-230 will issue a burst refresh to insure that all rows are properly refreshed. The BIOS must wait for this burst refresh to complete before accessing the RAMs or initializing the DRAM refresh generator. The status of this burst refresh can be determined by reading the PMUREF bit in the PMU resume status register at index DAH.

Name: **PMU Resume Status Register**

Type: **Read/Write**

Index: **DAH**

Bit	Name	Default	Function
D[7:2]	Reserved	00H	Reserved bits
D1	PMUREF	0	Read only bit polled by software to determine the end of the Resume Operation. 1 = PMU Refreshing
D0	CLKSPD	0	CPU Clock speed divider during DOZE or SLEEP mode. 0 = divided by 4; 1 = divided by 8.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

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SUB-NOTEBOOK ENGINE
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2.7 Power Supply Interfacing

A typical VG-230 implementation contains several switched power supplies. Typical power supplies required are as follows:

+5 Volt main

Supplies ROM, and I/O devices. Powered off during Suspend mode.

+5 Volt RAM

Supplies RAM.

+5 Volt VG-230

Supplies VG-230. Always powered to keep RTC running.

+5 Volt LCD

Provides power for LCD panel

-18-22 volt LCD bias

Provides negative bias power for LCD panel

+5 Volt PC card

Provides main operating power for PC card

+5/+12 Volt PC card

Provides programming voltage for PC cards

The VG-230 provides eight power control outputs:

VPSYS	- Main VCC control
VPRAM	- Controls VCC to RAMs
VPLCD	- Controls VCC to LCD
VPBIAS	- Controls Bias voltage to LCDs
VPCRD	- VCC control for PC card slots A and B
VPPENA	- VPP control - Slot A
VPPENB	- VPP control - Slot B

In a typical system, the VG-230 is constantly powered. This provides constant power for the internal real time clock (RTC) and the internal configuration RAM. Figure 2.7-1 shows a power distribution for a typical pocket computer. Note that when the battery is connected, the VG-230 is always powered. VPRAM controls power to the RAM array and is enabled in all modes, except the OFF mode. VPSYS controls the power to ROM array, and other peripherals. VPLCD and VPBIAS switch the power to the LCD and VPCRD controls power to the PCMCIA PC cards.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

DES-0V MEDIAN
ENGINE PRODUCTIVE SUB
POWERFUL JACKET

POWER SUPPLY INTERFACE

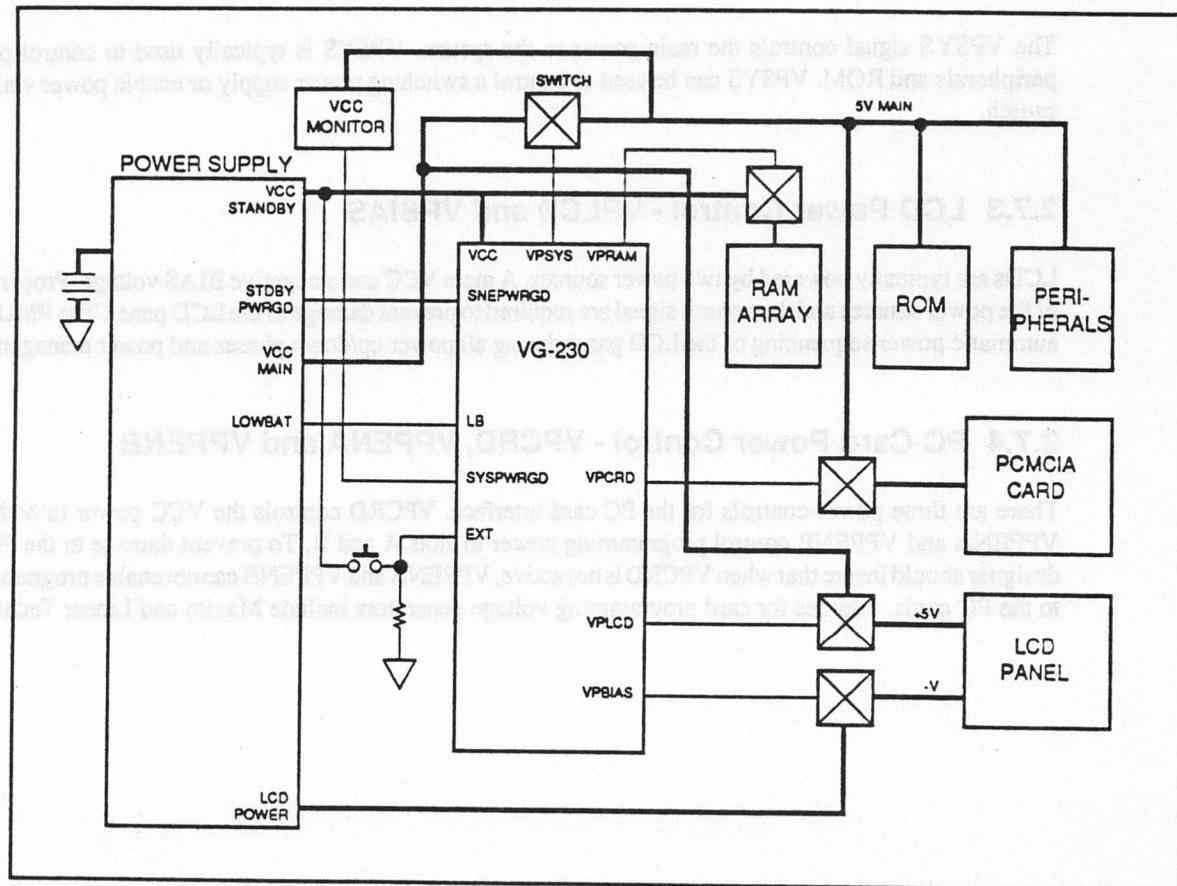


Figure 2.7-1

2.7.1 External Input (EXT)

The EXT input is used to turn on/off the system power. This signal is typically connected to a momentary contact switch. The EXT input is internally debounced and can be directly connected to a mechanical switch. When the system is in the SUSPEND state and the EXT switch is low for more than 60ms, and then becomes high, the VG-230 will be placed into the ON state.

When the VG-230 is in the ON, DOZE or SLEEP state, a positive transition on the EXT input, after it has been low for 60ms, will cause an NMI to be generated to inform the system that a request to power down has been received. The BIOS can place the system into the SUSPEND or OFF state. If the NMI is not serviced within 1/2 second, the system will enter the OFF state automatically.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

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2.7.2 System Power Control - VPSYS

The VPSYS signal controls the main power to the system. VPSYS is typically used to control power to the peripherals and ROM. VPSYS can be used to control a switching power supply or enable power via a MOSFET switch.

2.7.3 LCD Power Control - VPLCD and VPBIAS

LCDs are typically powered by two power sources. A main VCC and a negative BIAS voltage. Proper sequencing of the power sources and the control signal are required to prevent damage to the LCD panel. The PMU in provides automatic power sequencing of the LCD panel during all power up/down phases and power management modes.

2.7.4 PC Card Power Control - VPCRD, VPPENA and VPPENB

There are three power controls for the PC card interface. VPCRD controls the VCC power to both card slots. VPPENA and VPPENB control programming power to slots A and B. To prevent damage to the PC cards, the designer should insure that when VPCRD is not active, VPPENA and VPPENB cannot enable programming power to the PC cards. Sources for card programming voltage generators include Maxim and Linear Technology.



VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

docs.ovAGOAV

SHMKE XOGGTON-SUG
SOMERETTE JAOHHOST

2.7.5 SNEPWRGD and SYSPWRGD

The VG-230 provides two power-good inputs. These inputs inform the VG-230 when the operating power is stabilized. The SNEPWRGD input is a high true input that is driven when the power to the VG-230 has stabilized. This input is used as the initial power-good signal and is used to reset all internal registers, the Real Time Clock, CPU and all peripherals. SNEPWRGD is usually only at a low state when the batteries are being changed or have been depleted.

The second power good input, SYSPWRGD, is used to inform the VG-230 that the system power is good and that the system is ready for operation. SYSPWRGD is used to initialize the external system peripherals, via the *RESOUT signal, and re-start the VG-230 clocks. See Figure 2.7-3 for power up sequence of the VG-230.

POWER ON SEQUENCE

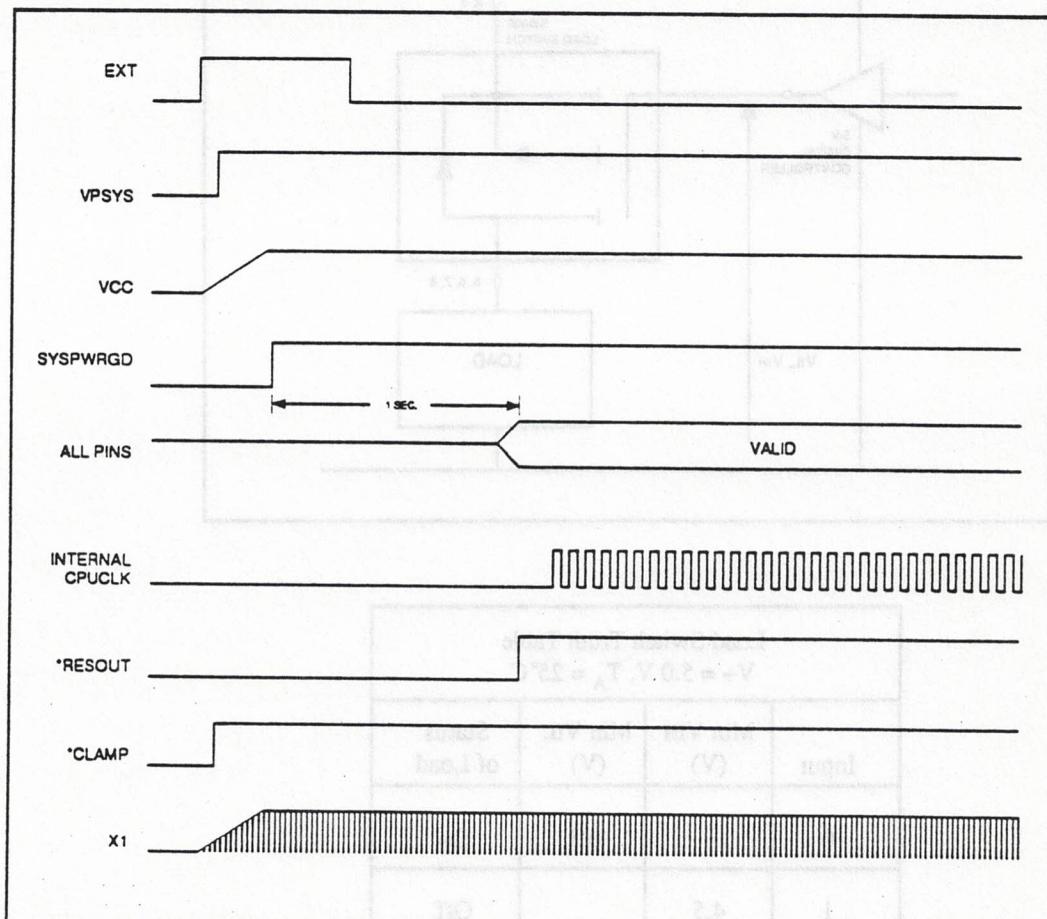
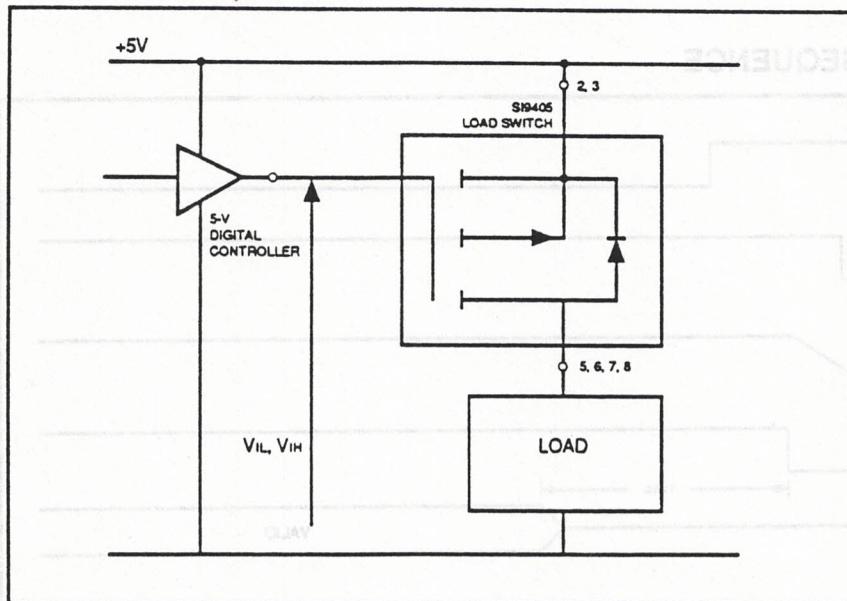


Figure 2.7-3

2.7.6 Power Switching

There are several off-the-shelf solutions for switching power to peripheral devices ranging from relays to MOSFETs. For portable system design, one solution is the Littlefoot family of MOSFET switches from Siliconix. These are high side switches in 8 pin SO packages which can be directly controlled by the VG-230's power control pins. Note that the processor must be running code to change the polarity of the VPSYS and VPRAM power control pins. Therefore if a Littlefoot device is being used to control the system or RAM power, the solution requires default polarity and an external hardware inverter on the control signal.

LOAD SWITCH EXAMPLE



Load Switch Truth Table			
Input	Min V _{IH} (V)	Min V _{IL} (V)	Status of Load
0		0.5	On
1	4.5		Off

Figure 2.7-4

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

DATA AV MEDEV
PARALLEL PORT TO SUB
POWER SUPPLY ADAPTER

2.8 Keyboard

The VG-230 supports two types of keyboard interfaces. The first is an internal matrix keyboard interface. The second is a PC/XT compatible serial keyboard interface. Applications programs address both interface options through PC/XT compatible keyboard registers. These registers are the PC/XT Compatible PPIA Keyboard Data Register, located at I/O address 060H, and the PC/XT Compatible PPIB Keyboard Control Register, located at I/O address 061H.

When the VG-230 is configured for the internal keyboard scanner, it supports an external key matrix of up to 101 keys. 96 of these keys are organized in an 8 x 12 matrix and 5 are dedicated shift keys. When the keyboard scanner is disabled, some of the pins it controls are assigned to other internal devices. These devices are the Parallel Port, the PC/XT serial keyboard interface, and control for a second PCMCIA card slot.

The VG-230 keyboard option is controlled by Bit 3 (KBDMODE) of the Keyboard Mode Register (Index 08H). The Default value of KBDMODE is LOW which selects the internal scanned keyboard interface. When KBDMODE is HIGH, the PC/XT serial keyboard interface is selected.

2.8.1 Scanned Keyboard Interface

The VG-230 contains five indexed registers that are used to control the internal keyboard scanner. These registers are the following:

Keyboard Mode Register	(Index 08H)
Scan Control Register	(Index 09H)
Return Status Low Register	(Index 0AH)
Return Status High Register	(Index 0BH)
Shift and NMI Status Register	(Index 0CH)

These registers allow the BIOS to read the key matrix, determine which key, if any, has been depressed, and then write the proper scan code to the PC/XT compatible PPIA Keyboard Data Register located at I/O address 060H. The Keyboard Mode Register at index 08H contains programmable bits for selecting the setting of system switches SW[8:5], the keyboard mode, NMI scan rate for the internal keyboard scanner.

These registers allow the BIOS to read the key matrix, determine which key, if any, has been depressed, and then write the proper scan code to the PC/XT compatible PPIA Keyboard Data Register located at I/O address 060H. The Keyboard Mode Register at index 08H contains programmable bits for selecting the setting of system switches SW[8:5], the keyboard mode, NMI scan rate for the internal keyboard scanner.

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VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
Sub-Notebook Engine
Technical Reference

Name: Sub-Notebook Engine Keyboard Mode Register

Type: Read/Write

Address: INDEX 08H

2.8 Keyboard

Bit	Name	Default	Function		
D[7:4]	SW[8:5]	0H	Software programmable bits used to select the setting of system switches SW[8:5] (display type and floppy drive count).		
D3	KBDMODE	0	0 - Select Keyboard Scanner pin configuration 1 - Redefine Keyboard Scanner pins		
D2	*KBDENA	0	0 - Enable PC/XT serial keyboard I/F 1 - Disable PC/XT serial keyboard I/F Only meaningful when Keyboard Scanner pins are redefined (KBDMODE=1). Setting this bit high directs port 60H accesses to the external data bus D[15:0] and further redefines KBDAT pin as IRQ1.		
D[1:0]	SCLK[1:0]	00	SCLK1	SCLK0	NMI Scan Rate
			0	0	51.2 Hz
			0	1	64 Hz
			1	0	85.3 Hz
			1	1	128 Hz

The function of SW[8:5] is the same as in a PC/XT system. These are the system switches that select the type of display installed and the number of floppy drives installed. These bits are software programmable.

KBDMODE is used to configure the VG-230 keyboard interface. When this bit is low, the VG-230 is configured to use the internal keyboard scanner. SCAN[7:0], RET[11:0], and SHFT[4:0] are connected to the key matrix and the BIOS uses the Scan Control, Return Status, Shift and NMI Status registers to decode the key matrix. The translated scan code is then written to the Keyboard Data Register at 060H.

Setting KBDMODE high redefines the scanner pins (SCAN[7:0], RET[11:0], and SHFT[4:0]), reassigning them to other internal devices. These devices are the PC/XT serial keyboard interface, Parallel port, and the second PCMCIA Card slot. When the VG-230 is configured for the PC/XT serial keyboard interface, the internal keyboard scan logic is disabled and the Return Status registers are ignored. The serial Keyboard Interface may also be disabled to implement an AT-style bi-directional keyboard.

The keyboard scan logic contains a rate generator that is used to determine how often the keyboard should be scanned. SCLK[1:0] set the frequency at which the scan logic generates a keyboard NMI to request a keyboard scan.

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

The Scan Control register is used when the VG-230 is configured to use the internal keyboard scanner.

Name: Sub-Notebook Engine Scan Control Register
Type: Read/Write
Address: INDEX 09H

Bit	Name	Default	Function
D[7:0]	S[7:0]	00H	SCAN[7:0] output enabled. 0 - Associated SCAN[7:0] pin is driven Hi-Z. 1 - Associated SCAN[7:0] pin driven low.

Note: In PC/XT serial I/F mode the Keyboard Scan logic is disabled (S[7:0] forced low) allowing the SCAN[7:0] output buffers to be controlled by other logic.

S[7:0] are sequentially set high during an active keyboard scan. The Return Status registers are checked to determine if a key has been pressed. The rate at which the keyboard is scanned is determined by the setting of SCLK[1:0] in the Keyboard Mode register.

When the keyboard scan completes without finding that a key has been pressed, S[7:0] are all set high. Thereafter, if a key is pressed, an NMI is generated and the keyboard scan routine begins again.

The Return Status Low Register is used to read the status of the RET[7:0] inputs.

Name: Sub-Notebook Engine Return Status Low Register
Type: Read Only
Address: INDEX 0AH

Bit	Name	Default	Function
D[7:0]	R[7:0]	FFH	RET[7:0] input status. 0 - Associated RET[7:0] switch position is closed. 1 - Associated RET[7:0] switch position is open.

Note: In PC/XT serial I/F mode this register is ignored.

The bits in this register reflect the state of the RET[7:0] inputs. A low indicates the corresponding RET[7:0] switch position is closed. A high indicates the corresponding RET[7:0] switch position is open. This register should be ignored when the VG-230 is configured for the PC/XT serial keyboard interface.

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

The Return Status High Register is used to read the status of four of the five Shift key inputs, SHFT[3:0] and the status of RET[11:8].

Name: Sub-Notebook Engine Return Status High Register

Type: Read Only

Address: INDEX 0BH

Bit	Name	Default	Function	Register	Offset	Name	Bit
D[7:4]	SH[3:0]	FH	SHFT[3:0] input status. 0 - Associated SHFT[3:0] switch position is closed. 1 - Associated SHFT[3:0] switch position is open.	SCALED-0	00H	INDEX 0BH	D[7:4]
D[3:0]	R[11:8]	FH	RET[11:8] input status. 0 - Associated RET[11:8] switch position is closed. 1 - Associated RET[11:8] switch position is open.	SCALED-1	01H	INDEX 0BH	D[3:0]
Note: In PC/XT serial I/F mode, this register is ignored.							

The bits in this register reflect the state of the SHFT[3:0] and RET[11:8] input pins. A low on SH[3:0] indicates the corresponding SHFT[3:0] switch position is closed. A high indicates the SHFT[3:0] switch position is open. A low on R[11:8] indicates the corresponding RET[11:8] switch position is closed. A high indicates the switch position is open. This register should be ignored when the VG-230 is configured for the PC/XT serial keyboard interface mode.

Function	Register	Offset	Name	Bit
SHFT[3:0] input status 0 - Associated RET[11:8] switch position is closed. 1 - Associated RET[11:8] switch position is open.	SCALED-0	00H	INDEX 0BH	D[7:4]

Note: In PC/XT serial I/F mode, this register is ignored.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

The Shift and NMI Status Register is used for both the internal keyboard scanner and PC/XT serial keyboard modes. It contains bits that enable keyboard related NMIs as well as bits that show the cause of the NMI.

Name: Sub-Notebook Engine Shift and NMI Status Register
Type: Read/Write
Address: INDEX 0CH

Bit	Name	Default	Function
D7	KEYNMI	0	1 - NMI caused by Keyboard Input. Writing this register with bit D7 set high will clear both the NMI signal and the KEYNMI bit.
D6	STMONMI	0	1 - NMI caused by Keyboard Scan Time Out. Writing this register with bit D6 set high will clear both the NMI signal and the STMONMI bit.
D5	PPIBNMI	0	1 - NMI caused by write to PPIB port requesting Keyboard Diagnostics. Writing this register with bit D5 set high will clear both the NMI signal and the PPIBNMI bit.
D4	KNMIEN	0	1 - Enable Keyboard Input NMIs.
D3	SNMIEN	0	1 - Enable Periodic NMIs generated by the Scan Timer.
D2	PNMIEN	0	1 - Enable NMIs caused by writes to PPIB port requesting Keyboard Diagnostics.
D1	Reserved	0	Reserved for future use.
D0	SH4	0	SHFT4 input status. 0 - SHFT4 switch position is closed. 1 - SHFT4 switch position is open. Note: In PC/XT serial I/F mode, this register bit is ignored.

Bits D[7:5] are used to determine the cause of the keyboard NMI. A high on KEYNMI (D7) indicates a keyboard NMI was caused when a key was pressed when the keyboard was not being actively scanned. A high on STMONMI (D6) indicates the keyboard NMI was caused by the keyboard scan rate logic. A high on PPIBNMI (D5) indicates a keyboard NMI was caused by a software write to the PPIB Keyboard Control Register (061H) requesting keyboard diagnostics. Writing this register with the appropriate bit set high will clear both the NMI signal and the NMI cause bit.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

Bits D[4:2] are used to enable the keyboard NMIs. A high written to KNMIEN (D4) allows a NMI, generated by a key being pressed, to be passed on to the CPU. When this bit is low, no NMI will be generated. When set high, SNMIEN (D3) enables keyboard scan time-out NMIs to be passed on to the CPU. And when set high, PNMREN (D2), allows NMIs caused by keyboard diagnostic requests to be passed on to the CPU.

SH4 (D0) reflects the state of the SHFT4 input pin. A low indicates the corresponding SHFT4 switch position is closed. A high indicates the switch is open. This bit is ignored when the VG-230 is configured for the PC/XT serial keyboard interface.

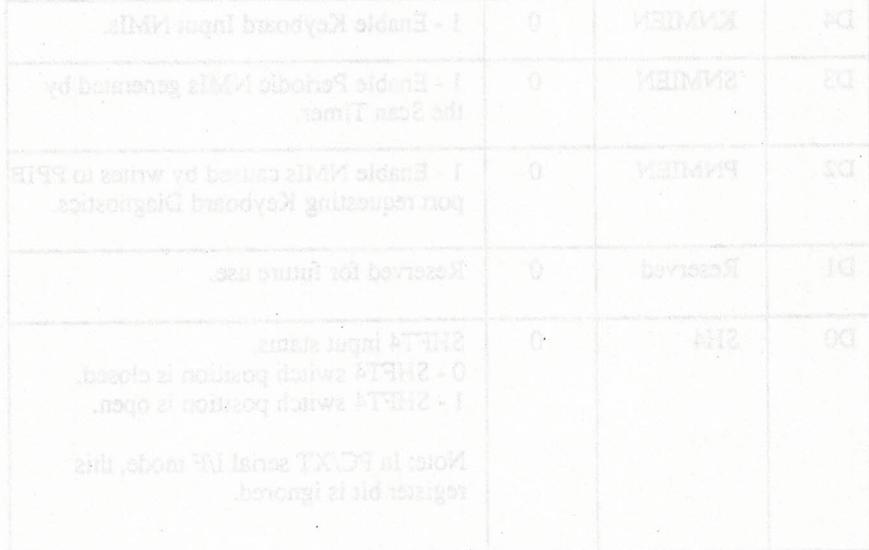
See the Vadem VG-230 BIOS Application Note for more information on the Internal Keyboard Scanner.

Design Notes

The VG-230 internal keyboard scanner supports an external key matrix of up to 101 keys. As mentioned previously, 96 of the keys are organized in an 8 x 12 matrix with 5 dedicated shift keys. There are 8 scan lines (SCAN[7:0]), 12 return lines (RET[11:0]), and 5 shift key lines (SHFT[4:0]). RET[11:0] and SHFT[4:0] are input pins and need pull up resistors. The scan lines SCAN[7:0] are outputs and do not require pull up resistors.

If desired or required by system design constraints, the shift lines can be combined with the return lines to provide support for an 8 x 17 key matrix. A smaller matrix can be used also. When a smaller matrix is desired, the unused scan lines should be left open. The unused return and shift lines still need to have pull up resistors.

The Block Diagram in Figure 2.8-1 shows a typical keyboard matrix connection.



Bit D[4:2] sets the level of the scan lines that causes to the keyboard NMI. A high on KE_NMIEN (D4) enables a keyboard NMI when a key was pressed when the keyboard was not performing a self-test. A high on SNMIEN (D3) generates a keyboard scan time-out NMI when a key was scanned by the keyboard scan line for too long. A high on PNMREN (D2) generates a keyboard diagnostic request NMI when the keyboard diagnostic request line for too long. When this happens with the keyboard diagnostic request line for too long, the NMI is generated.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

DE-3V MECHANICAL
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

KEYBOARD MATRIX CONNECTION

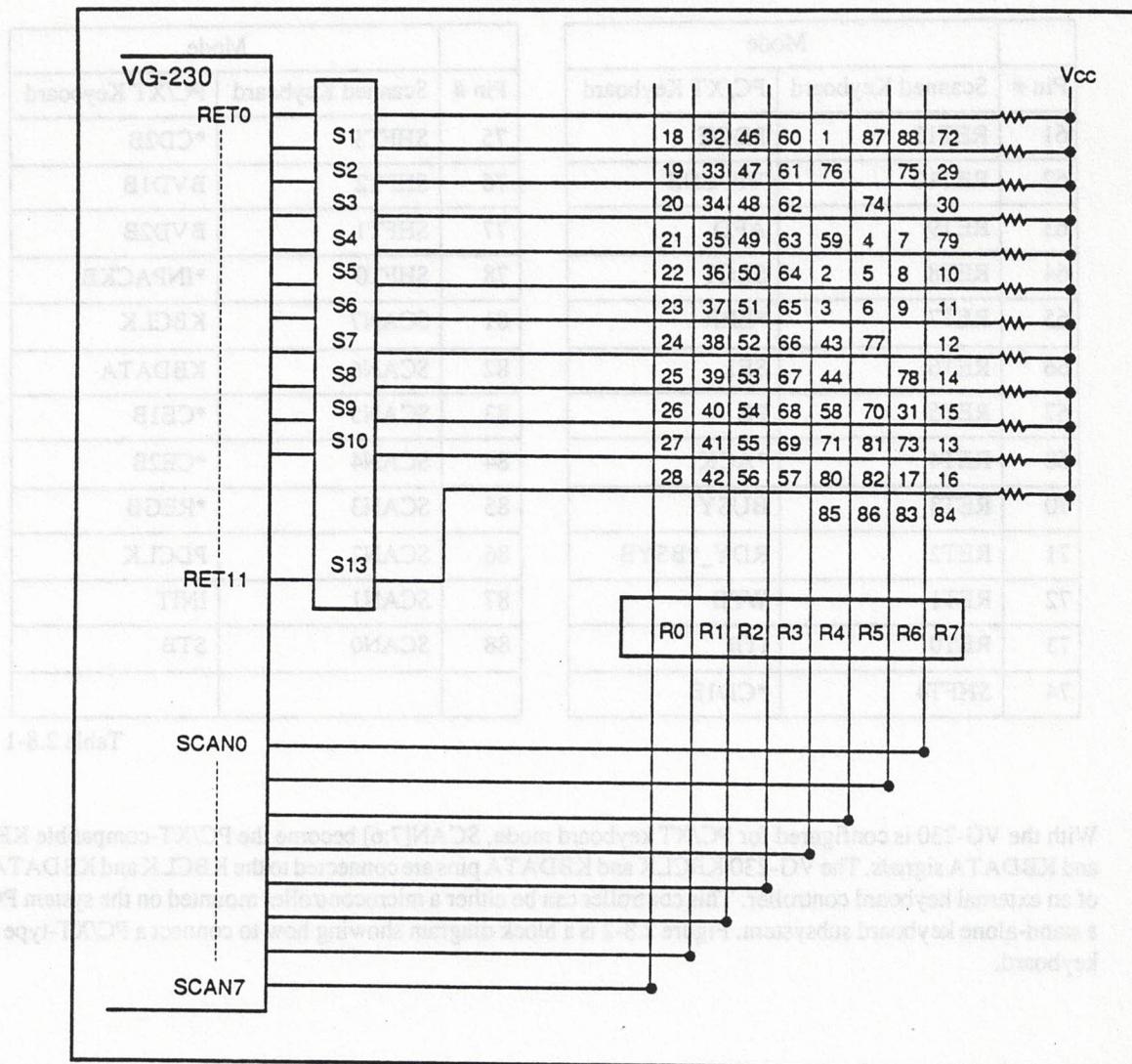


Figure 2.8-1

2.8.2 Serial PC/XT Keyboard Interface

The VG-230 is configured to use the PC/XT keyboard interface by writing KBDMODE (Bit D3) of the Keyboard Mode Register (Index 08H) and setting it high. This disables the internal keyboard scan logic and enables the PC/XT interface, parallel port, and second PCMCIA card slot. It reassigns the functions of the scan, return, and shift pins to support these devices. Table 2.8-1 details the pin number and function of the pins associated with both VG-230 keyboard interface modes.

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

VADEM VG-230
 SUB-NOTEBOOK ENGINE
 TECHNICAL REFERENCE

Scanned Keyboard Alternative Pin Functions

Mode		
Pin #	Scanned Keyboard	PC/XT Keyboard
61	RET11	PDOE
62	RET10	VPPENB
63	RET9	AFD
64	RET8	SLCT
65	RET7	*ERR
66	RET6	SEL
67	RET5	PE
68	RET4	*ACK
70	RET3	BUSY
71	RET2	RDY_*BSYB
72	RET1	WPB
73	RET0	ITB
74	SHFT4	*CD1B

Mode		
Pin #	Scanned Keyboard	PC/XT Keyboard
75	SHFT3	*CD2B
76	SHFT2	BVD1B
77	SHFT1	BVD2B
78	SHFT0	*INPACKB
81	SCAN7	KBCLK
82	SCAN6	KBDATA
83	SCAN5	*CE1B
84	SCAN4	*CE2B
85	SCAN3	*REGB
86	SCAN2	PDCLK
87	SCAN1	INIT
88	SCAN0	STB

Table 2.8-1

With the VG-230 is configured for PC/XT keyboard mode, SCAN[7:6] become the PC/XT-compatible KBCLK and KBDATA signals. The VG-230 KBCLK and KBDATA pins are connected to the KBCLK and KBDATA pins of an external keyboard controller. This controller can be either a microcontroller mounted on the system PCB or a stand-alone keyboard subsystem. Figure 2.8-2 is a block diagram showing how to connect a PC/XT-type serial keyboard.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

XT KEYBOARD INTERFACE

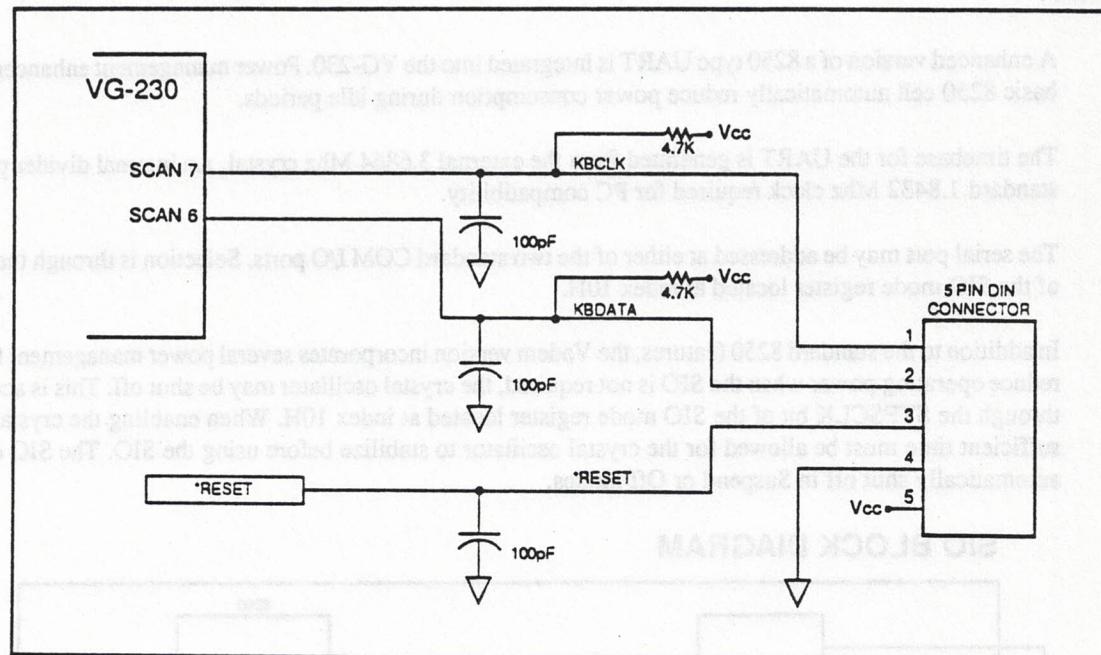


Figure 2.8-2

2.8.3 Disabling the Internal Keyboard Controller

It may be desirable to disable both the internal serial keyboard controller and the scanned keyboard controller in order to use an external microprocessor-type controller. This can be accomplished through the *KBDENA bit in the Keyboard Mode Register at index 08H.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

2.9 UART

An enhanced version of a 8250 type UART is integrated into the VG-230. Power management enhancements to the basic 8250 cell automatically reduce power consumption during idle periods.

The timebase for the UART is generated from the external 3.6864 Mhz crystal. An internal divider provides the standard 1.8432 Mhz clock required for PC compatibility.

The serial port may be addressed at either of the two standard COM I/O ports. Selection is through the SPSEL bit of the SIO mode register located at index 10H.

In addition to the standard 8250 features, the Vadem version incorporates several power management features. To reduce operating power when the SIO is not required, the crystal oscillator may be shut off. This is accomplished through the STPSCLK bit of the SIO mode register located at index 10H. When enabling the crystal oscillator, sufficient time must be allowed for the crystal oscillator to stabilize before using the SIO. The SIO oscillator is automatically shut off in Suspend or Off modes.

SIO BLOCK DIAGRAM

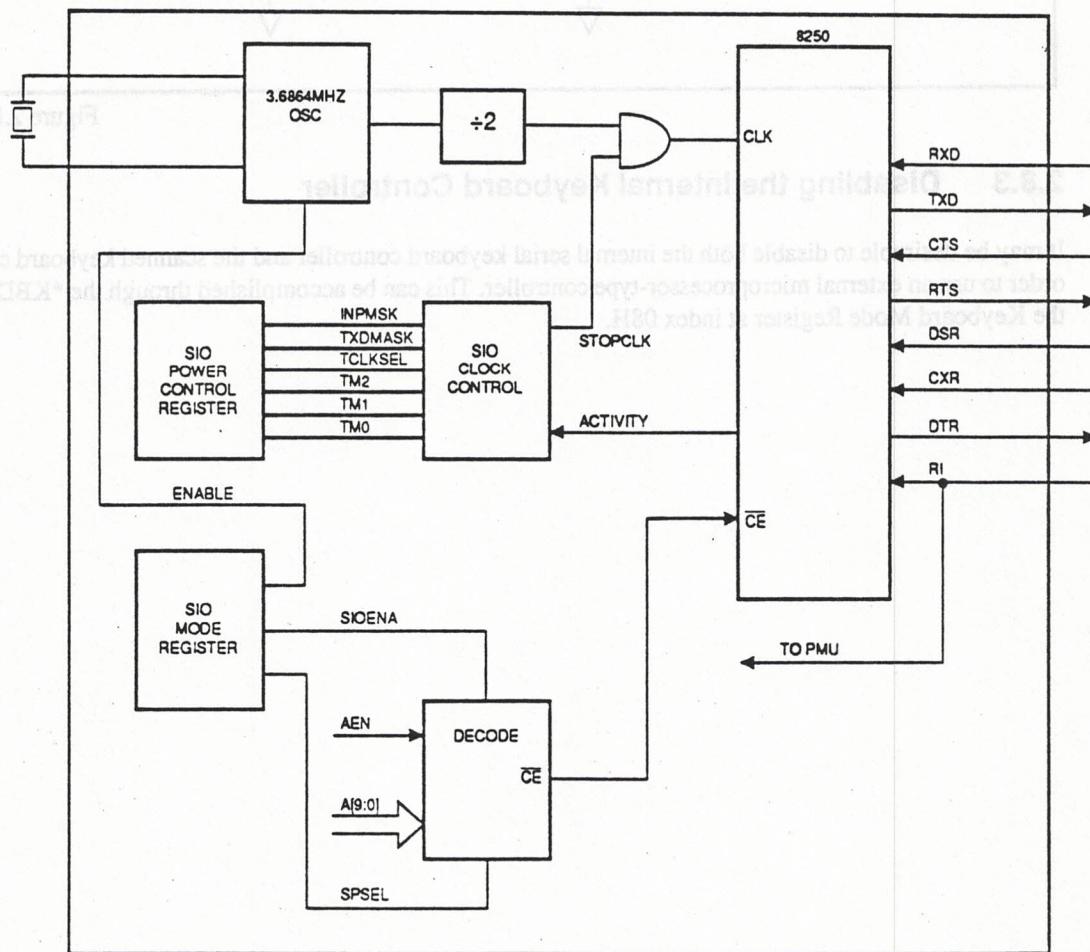


Figure 2.9-1

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

Name: Sub-Notebook Engine SIO Mode Register

Type: Read/Write

Address: INDEX 10H

Bit	Name	Default	Function
D7	SIOENA	1	0 - Disable internal Serial Port 1 - Enable internal Serial Port
D6	STPSCLK	0	0 - Enable SIO crystal oscillator 1 - Disable SIO crystal oscillator
D5	SPSEL	0	0 - SIO Port appears at I/O 3F8H - 3FFH and uses IRQ4 1 - SIO Port appears at I/O 2F8H - 2FFH and uses IRQ3
D[4:0]	Reserved	00H	Reserved for future use.

During normal SIO operation, there may be long periods of time where no characters are being transmitted or received. The VG-230 allows the designer to automatically stop the internal 8250 clocks after a programmable inactive time (from 1 to 120 seconds). These power management controls are located in the SIO Power control register located at index 11H.

Power management is enabled by setting TMO[3:0] to a non-zero number. If TCLKSEL is set to zero TMO[3:0] selects the clock timeout value in 1 second intervals. If TCLKSEL is set to one TMO[3:0] selects the clock timeout value in 8 second intervals. The SIO activity is defined by either writes to the SIO transmit buffer, or transitions on any of the SIO's input lines (RXD, DCD, RI, DSR, or CTS). Either of these events will retrigger the activity timer and place the SIO into the full power mode. Selection of which events will retrigger the activity monitor is accomplished through the INPMSK and the TXDMSK bits in the SIO power control register.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

Name: Sub-Notebook Engine SIO Power Control Register
 Type: Read/Write
 Address: INDEX 11H

Bit	Name	Default	Function
D7	INPMSK	0	0 - Retrigger Serial Port clock timer on high to low transition of RXD, *DCD, *RI, *DSR, or *CTS inputs. 1 - Mask above inputs from retriggering Serial Port clock
D6	TXDMSK	0	0 - Retrigger Serial Port clock timer on writes to transmit buffer 1 - Mask above writes from retriggering Serial Port clock
D5	Reserved	0	Reserved for future use
D4	TCLKSEL	0	0 - Timer range is from 1 to 15 seconds (1 sec. resolution) 1 - Timer range is from 8 sec. to 2 min. (8 sec. resolution)
D[3:0]	TMO[3:0]	0H	SIO Clock time-out value. Setting this register to 0 disables the timer.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

2.10 PARALLEL PRINTER INTERFACE

When the internal keyboard scanner is disabled, the free pins may be used as a standard parallel printer I/O port. The VG-230 supports all three of the standard PC compatible LPT ports. Selection of port address is accomplished through the PIO Mode register located at index 18H.

The implementation of a standard PC compatible printer port requires the addition of an external data latch and a control signal buffer. Figure 2.10-1 shows the configuration required. In addition the status inputs require external pull-up resistors.

Name: Sub-Notebook Engine PIO Mode Register
Type: Read/Write
Address: INDEX 18H

Bit	Name	Default	Function	
D7	PIOENA	0	0 - Disable internal Parallel Port 1 - Enable internal Parallel Port (This bit is valid only if Keyboard Scan function is disabled. Otherwise, Parallel Port is forced to be disabled.)	
D6	Reserved	0	Reserved for future use	
D[5:4]	PPSEL[1:0]	00	PPSEL1	Parallel Port I/O Address
			0	278H-27AH
			0	378H-37AH
			1	3BCH-3BEH
			1	170H-172H
D3	BIDIR	0H	0 - Parallel Port is uni-directional (output only) 1 - Parallel Port is bi-directional. Setting the PPDIR bit of the Parallel Port Control register forces reads from the Parallel port data registers to be sourced from the external data bus.	
D[2:0]	Reserved	0H	Reserved for future use	

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

Data Register

Name: PC/XT Compatible Parallel Port Data Register
 Type: Read/Write
 Address: 170H, 278H, 378H, or 3BCH

Bit	Name	Default	Function
D[7:0]	PD[7:0]	00H	<p>Parallel Data. In uni-directional mode, during reads from the Parallel Port Data Register, data is sourced from the PD[7:0] bits. During writes, data is captured in both this register and an external octal "D" type F/F controlled by the PDCLK pin.</p> <p>In bi-directional mode, the BIDIR bit of the PIO mode register is set high. The PPDIR bit of the Parallel Port Control Register determines the source of the data read from this port. When the PPDIR bit is low, data is read from the internal source. When PPDIR is high, the external parallel port data is read.</p>

Status Register

Name: PC/XT Compatible Parallel Port Status Register
 Type: Read Only
 Address: 171H, 279H, 379H, or 3BDH

Bit	Name	Default	Function
D7	*BUSY	X	Inverted state of the BUSY input pin.
D6	*ACK	X	Driven directly from the *ACK input pin
D5	PE	X	Driven directly from the PE input pin.
D4	SEL	X	Driven directly from the SEL input pin.
D3	*ERROR	X	Driven directly from the *ERR input pin.
D2	IRQSTA	0	Interrupt Status. 1 - PIO Interrupt Pending
D[1:0]	N/U	00	Not Used. Always read back Low.

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

Control Register

Name: PC/XT Compatible Parallel Port Control Register

Type: Read/Write

Address: 172H, 27AH, 37AH, or 3BEH

Bit	Name	Default	Function
D[7:6]	N/U	000	Not Used. Ignored when written and Zero when read.
D5	PPDIR	0	Parallel Port direction control. When the BIDIR bit of the PIO Mode register is set high, the parallel port is configured for bi-directional operation and this bit is used to externally control the OE of the printer data latch and read-back path as follows: 0 - Write data to external parallel I/O device. (PDOE output driven low) 1 - Read data from external parallel I/O device. (PDOE output driven high) This bit is a don't care when the BIDIR bit is reset low.
D4	IRQENA	0	PIO Interrupt Enable. 1 - Enabled 0 - Disabled
D3	SELECT	0	Inverted and drives *SLCT output pin.
D2	*INIT	0	Directly drives *INIT output pin.
D1	AUTOFD	0	Inverted and drives *AFD output pin.
D0	STROBE	0	Inverted and drives *STB output pin.

Care must be taken to prevent the printer device from sourcing current into the VG-230-based system. When selecting parallel data and control drivers, the designer must insure that a high level on any I/O lines will not be gated onto the system power bus. The designer must insure that the logic family used to interface to the external parallel printer device be latchup proof. The VG-230 parallel printer inputs are designed to avoid such a problem.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

UNIDIRECTIONAL PARALLEL PRINTER INTERFACE

Mode		
Pin #	Scanned Keyboard	PC/XT Keyboard
61	RET11	VPPEN1B
62	RET10	VPPEN2B
63	RET9	AFD
64	RET8	SLCT
65	RET7	*ERR
66	RET6	SEL
67	RET5	PE
68	RET4	*ACK
70	RET3	BUSY
71	RET2	RDY_*BSYB
72	RET1	WPB
73	RET0	ITB
74	SHFT4	*CD1B

Mode		
Pin #	Scanned Keyboard	PC/XT Keyboard
75	SHFT3	*CD2B
76	SHFT2	BVD1B
77	SHFT1	BVD2B
78	SHFT0	*INPACKB
81	SCAN7	KBCLK
82	SCAN6	KBDATA
83	SCAN5	*CE1B
84	SCAN4	*CE2B
85	SCAN3	*REGB
86	SCAN2	PDCLK
87	SCAN1	INIT
88	SCAN0	STB

Figure 2.10-1

Note: To enable the parallel printer interface, the internal keyboard scanner must be disabled. This is accomplished through the KBDMODE bit of the Keyboard Mode Register located at index 08H.

2.10.1 Implementing a Bi-Directional Parallel Port

The VG-230 also supports a bi-directional parallel printer port. The addition of an external buffer and some glue logic is required. The BIDIR bit in the VG-230's PIO mode register determines if the bi-directional port is enabled. When enabled, the PPDIR bit in the parallel port control register (172H, 27AH or 37AH) forces reads from the parallel port data registers to be sourced from the external bus.

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

BI-DIRECTIONAL PARALLEL PORT INTERFACE

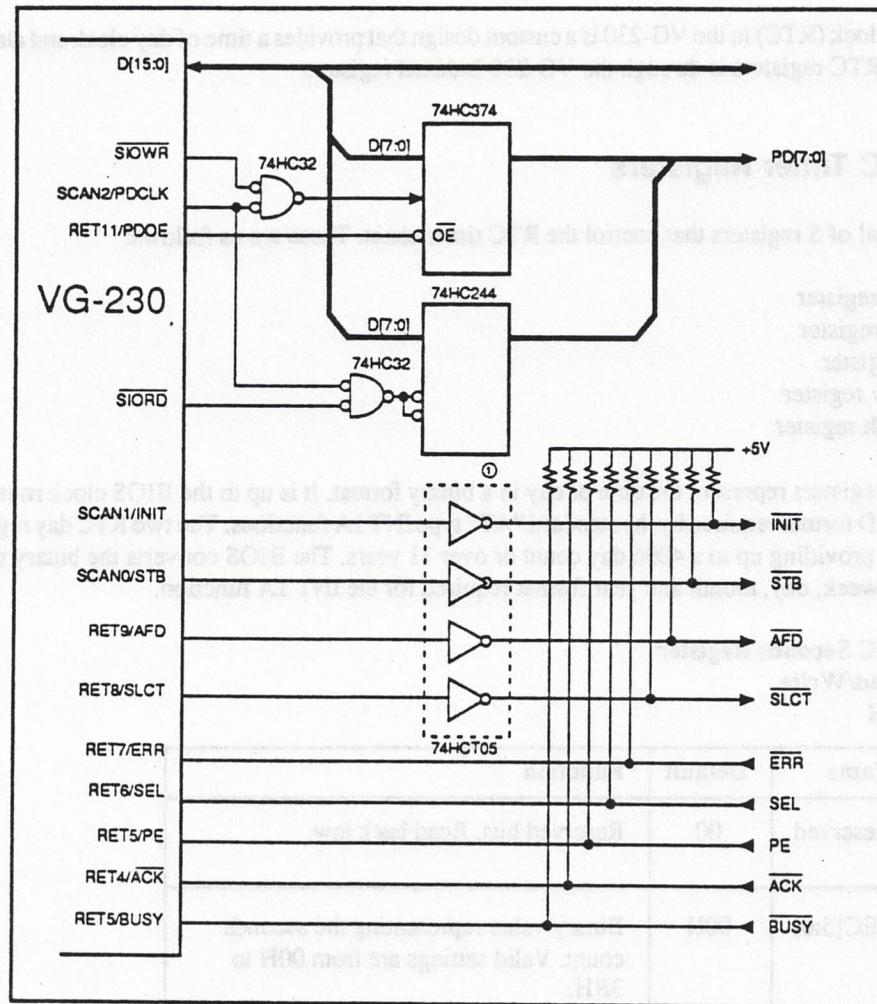


Figure 2.10-2

Address	Function	Value	Notes
0000H	Initial Address	00	Set by ROM BIOS
0001H	Initial Address	00	Set by ROM BIOS

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

2.11 REAL TIME CLOCK (RTC)

The real time clock (RTC) in the VG-230 is a custom design that provides a time of day clock and alarm functions. Access to the RTC registers is through the VG-230 Indexed registers.

2.11.1 RTC Timer Registers

There are a total of 5 registers that control the RTC timer chain. These are as follows:

- RTC Seconds register
- RTC Minutes register
- RTC Hours register
- RTC Days-low register
- RTC Days-high register

Each of these registers represent the time of day in a binary format. It is up to the BIOS clock routine to convert these into a BCD format required by the standard "AT" type INT 1A functions. The two RTC day registers provide a 12 bit count, providing up to a 4096 day count or over 11 years. The BIOS converts the binary day count into a BCD day of week, day, month and year format required for the INT 1A function.

Name: **RTC Seconds Register**
Type: **Read/Write**
Index: **70H**

Bit	Name	Default	Function
D[7:6]	Reserved	00	Reserved bits. Read back low.
D[5:0]	SEC[5:0]	00H	Binary value representing the seconds count. Valid settings are from 00H to 3BH.

Name: **RTC Minutes Register**
Type: **Read/Write**
Index: **71H**

Bit	Name	Default	Function
D[7:6]	Reserved	00	Reserved bits. Read back low.
D[5:0]	MIN[5:0]	00H	Binary value representing the minutes count. Valid settings are from 00H to 3BH.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

Name: **RTC Hours Register**
Type: **Read/Write**
Index: **72H**

Bit	Name	Default	Function
D[7:5]	Reserved	000	Reserved bits. Read back low.
D[4:0]	HR[4:0]	00H	Binary value representing the hours count in 24 hour mode. Valid settings are from 00H to 17H.

Name: **RTC Day Low Register**
Type: **Read/Write**
Index: **73H**

Bit	Name	Default	Function
D[7:0]	DAY[7:0]	00H	Binary value representing the low day count. Valid settings are from 00H to FFH.

Name: **RTC Day High Register**
Type: **Read/Write**
Index: **74H**

Bit	Name	Default	Function
D[7:4]	Reserved	0H	Reserved bits. Read back low.
D[3:0]	DAY[11:8]	0H	Binary value representing the high day count. Valid settings are from 00H to 0FH.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM AG-230
Sub-Notebook Engine
Technical Reference

2.11.2 RTC Alarm

The RTC provides an alarm function. The alarm can be used to generate an interrupt, and when the VG-230 is in the OFF or SUSPEND state, place the system into the ON state. The RTC alarm function is implemented with four registers.

Name: RTC Alarm Seconds Register

Type: Read/Write

Index: 75H

Bit	Name	Default	Function
D[7:6]	Reserved	00	Reserved bits. Read back low.
D[5:0]	ALRS[5:0]	00H	Binary value representing the Alarm seconds count. Valid settings are from 00H to 3BH.

Name: RTC Alarm Minutes Register

Type: Read/Write

Index: 76H

Bit	Name	Default	Function
D[7:6]	Reserved	00	Reserved bits. Read back low.
D[5:0]	ALRM[5:0]	00H	Binary value representing the Alarm minutes count. Valid settings are from 00H to 3BH.

Name: RTC Alarm Hours Register

Type: Read/Write

Index: 77H

Bit	Name	Default	Function
D[7:5]	Reserved	00	Reserved bits. Read back low.
D[4:0]	ALRH[5:0]	00H	Binary value representing the Alarm hours count. Valid settings are from 00H to 17H.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

Name: **RTC Alarm Day Register**
 Type: **Read/Write**
 Index: **78H**

Bit	Name	Default	Function
D[7:5]	Reserved	000	Reserved bits. Read back low.
D[4:0]	ALRD[4:0]	00H	Binary value representing the Alarm day count. Valid settings are from 00H to 1FH. This value is compared with the least significant 5 bits of the RTC Low Day counter.

The alarm is enabled through the RTC MODE register at index 79H. Bit 1 the ALRMINT bit when set enables RTC interrupts. The alarm interrupt RTCINT is asserted on IRQ2. The interrupt is cleared by writing a "1" to the ALARM bit in the RTC status register.

Name: **RTC Mode Register**
 Type: **Read/Write**
 Index: **79H**

Bit	Name	Default	Function
D7	*RTCEN	0	0 - Enable RTC Clock Index Registers 70-78H access 1 - Disable RTC Clock Index Registers 70-78H access
D6	*RAMEN	0	0 - Enable RTC CMOS RAM access 1 - Disable RTC CMOS RAM access
D5	UPDATE	0	0 - RTC Clock Running 1 - Pause RTC Clock for setting of Time and/or Alarm values.
D[4:2]	Reserved	0H	Reserved bits. Read back low.
D1	ALRMINT	0	0 - Disable RTC Alarm interrupts 1 - Enable RTC Alarm interrupts
D0	PERINT	0	0 - Disable 1Hz periodic interrupts 1 - Enable 1Hz periodic interrupts

When the contents of the alarm registers equal the values in the four corresponding clock registers and the RTC alarm interrupt bit (ALRMINT) bit is set, an alarm interrupt is generated. The BIOS can verify that the alarm interrupt was triggered, by reading the ALARM bit in the RTC status register at index 7AH. The interrupt is cleared by writing a "1" to the ALARM bit in the RTC status register.

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

DE5-VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

Name: RTC Status Register
Type: Read/Write
Index: 7AH

Bit	Name	Default	Function
D7	VALID	0	0 - Power to RTC and CMOS RAM has been lost. Contents are not valid. 1 - RTC Clock and CMOS RAM contents valid. System software sets the VALID bit following initialization of the RTC. VALID is cleared when power to VG-230 has been removed.
D[6:2]	Reserved	0	Reserved bit. Read back low.
D1	ALARM	0	0 - No RTC Clock Alarm Pending. 1 - RTC Clock Alarm Pending. Writing this register with bit D1 set high will clear both the RTCINT signal and the ALARM status bit.
D0	Periodic	0	0 - No Periodic Interrupt Pending. 1 - Periodic Interrupt Pending. Writing this register with bit D0 set high will clear both the RTCINT signal and the Periodic Status Bit.

2.11.3 Periodic Interrupt Feature

The RTC is also capable of generating a 1Hz periodic interrupt. This feature is enabled by setting the PERINT bit in the RTC mode register at index 79H. When the PERINT bit is set, an RTCINT will be generated every second. The BIOS can verify that the Periodic interrupt was triggered, by reading the PERIODIC bit in the RTC status register at index 7AH. The interrupt is cleared by writing a "1" to the PERIODIC bit in the RTC status register.

2.11.4 Setting the RTC and Power Up Considerations

The internal RTC contains a VALID bit that is reset when SNEPWRGD goes low. This bit is set via program control, and indicates that the RTC time and RAM is valid. When the BIOS or system software initializes the RTC and CMOS RAM, the VALID bit should be set. The VALID bit is contained in the RTC Status register at index 7AH. The BIOS power up routines should read the status of the VALID bit to check the validity of the RTC and the CMOS RAM.

The RTC should be initialized using the following procedure:

1. Enable RTC by clearing *RTCEN bit in RTC mode register
2. Pause RTC by setting UPDATE bit in RTC mode register
3. Initialize RTC Seconds, Minutes, Hours and Day register to proper time.
4. Clear UPDATE bit in RTC mode register.

Note: When setting the RTC the designer must insure that the PMU does not enter a static DOZE state. If this happens when the RTC is stopped, the RTC will lose time. This can be prevented by using slow-clock DOZE or by having the RTC set routine disable the DOZE timer or trigger activity by a dummy read of an activity monitor address.

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

OSR-DV MSGAV
SHONIE WOODSON-HUB
SOMMERER JACOB

2.11.5 RTC CMOS RAM

The RTC contains CMOS static RAM from index 80H to BFH. This RAM is accessed through the VG-230's Indexed registers. The RAM is valid as long as the VALID bit is set. The RTC RAM contains a write protect feature that is enable via the *RAMEN bit located in the RTC Mode register. When the *RAMEN bit is cleared, RAM reads and writes are enabled. When *RAMEN is set, all read and write accesses are disabled. This feature prevents inadvertent writes to the CMOS RAM.

I-CPLD output 2 outputs current to hardware over a period of time to ensure system and OSC-DV soft

Table 2-11.5: RTC CMOS RAM Address and Data Register Map

Address	Register	Value	Source
AFC	OSC	4	IMC3 Internal
AFC	VIC	5	SMO3 Internal
RTC	RTC	7	RTC Internal
H02	HIC AC	0	INPUT AD200
H02	HIC DS	1	INPUT AD200
H02	HIC ref1	1-1	AD1
H02	HIC ref2	1-2	AD2
H02, H03 ref1	HIC ref1	1-3, 2	AD2, GND
H02	HIC ref2	1-4	AD1 GND
H02	HIC ref3	1-5	AD1 GND
H02	HIC ref4	2	AD2 GND

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

2.12 EXPANSION

The VG-230 implements a standard 8 bit ISA expansion bus. Standard MRD, MWR, IORD, and IOWR signals provide strobes for memory and I/O devices. Data is gated onto the D[7:0] lines and address lines A[9:0] provide address information.

The ISA bus is provided as a means for adding a small amount of custom I/O in a closed system. The VG-230 was not designed to directly drive the heavy loads typically associated with a backplane; therefore address and data bus buffering is required in applications where the end user can install commercially available XT bus cards.

2.12.1 Interrupts

The VG-230 has many sources of internal interrupts in addition to two external interrupt sources. Figure 2.12-1 illustrates the sources of the internal and external sources. The following table lists the internal interrupts and the control/status register associated with each.

Internal Interrupts and Their Control/Status Registers

Source	Levels	Control	Status
Internal COM1	4	3F9	3FA
Internal COM2	3	2F9	2FA
Parallel Port	7	37A	379
82C54 Timer	0	20, 21H	20H
Keyboard	1	20, 21H	20H
IRQA	2-7	Index 0DH	20H
IRQB	2-7	Index 0DH	20H
PCCARD Status	2, 6, 7	Index 20H	Index 22H, 28H
PCCARD A I/O	2-7	Index 21H	20H
PCCARD B I/O	2-7	Index 27H	20H
Real Time Clock	2	Index 79H	Index 7AH

Table 2.12-1

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

DE5-DV-MDAV
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

INTERNAL INTERRUPT CONFIGURATION

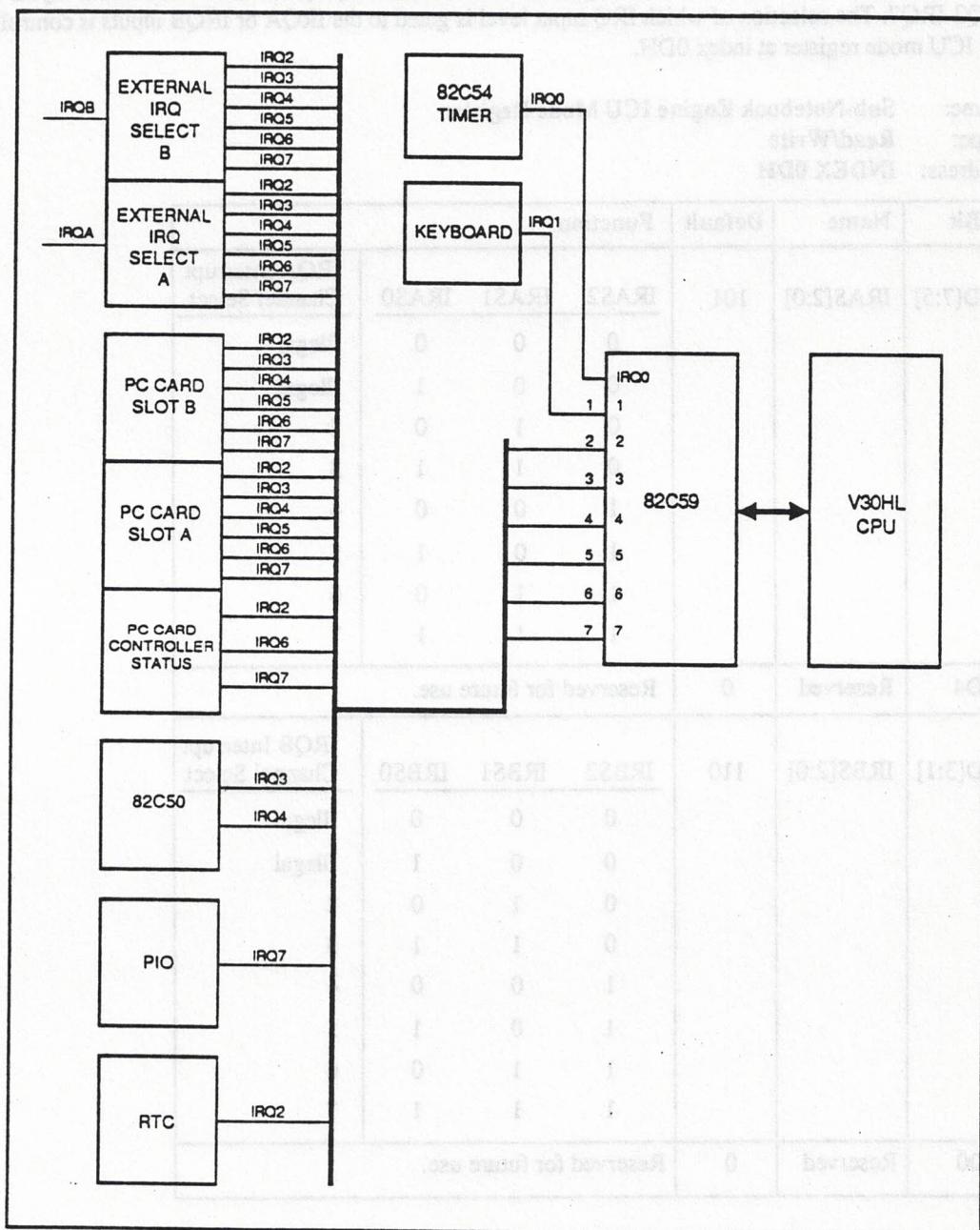


Figure 2.12-1

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

Two pins, IRQA and IRQB, provide support for the standard IRQ inputs. Each one of these inputs can support IRQ2-IRQ7. The selection of which IRQ input level is gated to the IRQA or IRQB inputs is controlled through the ICU mode register at index 0DH.

Name: Sub-Notebook Engine ICU Mode Register

Type: Read/Write

Address: INDEX 0DH

Bit	Name	Default	Function			
D[7:5]	IRAS[2:0]	101	IRAS2	IRAS1	IRAS0	IRQA Interrupt Channel Select
			0	0	0	Illegal
			0	0	1	Illegal
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	7
D4	Reserved	0	Reserved for future use.			
D[3:1]	IRBS[2:0]	110	IRBS2	IRBS1	IRBS0	IRQB Interrupt Channel Select
			0	0	0	Illegal
			0	0	1	Illegal
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
D0	Reserved	0	Reserved for future use.			

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

2.12.2 DMA

The VG-230 provides two pins for DMA support. Because of pin limitations, only a single DMA channel is supported. The DMA pins, DRQ and *DACK are configurable for DRQ/*DACK[1:3]. Selection of the desired DMA channel is made through bits DRQS[1:0] in the DMA mode register located at index 0EH.

Name: Sub-Notebook Engine DMA Mode Register

Type: Read/Write

Address: INDEX 0EH

Bit	Name	Default	Function		
D[7:5]	REFW[2:0]	111	REFW2	REFW1	REFW0
			0	0	0
			0	0	1
			0	1	0
			0	1	1
			1	0	0
			1	0	1
			1	1	0
			1	1	1
D4	STPDCLK	0	0 - DMA clock runs always 1 - DMA clock runs only during DMA cycles		
			WDLY1	WDLY0	IOWR/MWR Command Delay
D[3:2]	WDLY[1:0]	01	0	0	0 SYSCLK cycles
			0	1	1 SYSCLK cycles
			1	0	2 SYSCLK cycles
			1	1	3 SYSCLK cycles
			Note: For each SYSCLK cycle command delay specified by WDLY[1:0] one bus wait state will be added to the DMA cycle.		
D[1:0]	DRQS[1:0]	10	DRQS1	DRQS0	DMA Channel Select
			0	0	Illegal
			0	1	DRQ1/*DACK1
			1	0	DRQ2/*DACK2
			1	1	DRQ3/*DACK3

2.12.3 Command Delay and DMA Clock Control

In some applications it may be desirable to delay the *IOWR and *MWR strobes during DMA. These strobes may be delayed from 0 to 3 SYSCLK cycles. Command delay is programmed through WDLY[1:0] in the DMA mode register.

To reduce current consumption, the VG-230 has a provision to disable the internal 8237's clock during idle times. When the STPDCLK bit in the DMA mode register is cleared (0), the internal DMA clock always runs. When set, the clock is enabled only during DMA cycles.

2.12.4 The ISA Bus and Buffering

The VG-230 was designed to be the core for a small system. Because of the single bus architecture, it may be necessary to buffer the Address and/or Data bus to its external peripherals. (See section 3.2 for information regarding drive calculations). If it is necessary to buffer, an external data and/or address buffer can be used. See Figure 2.12-2 for a typical buffer configuration.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

EXPANSION BUFFER CONFIGURATION

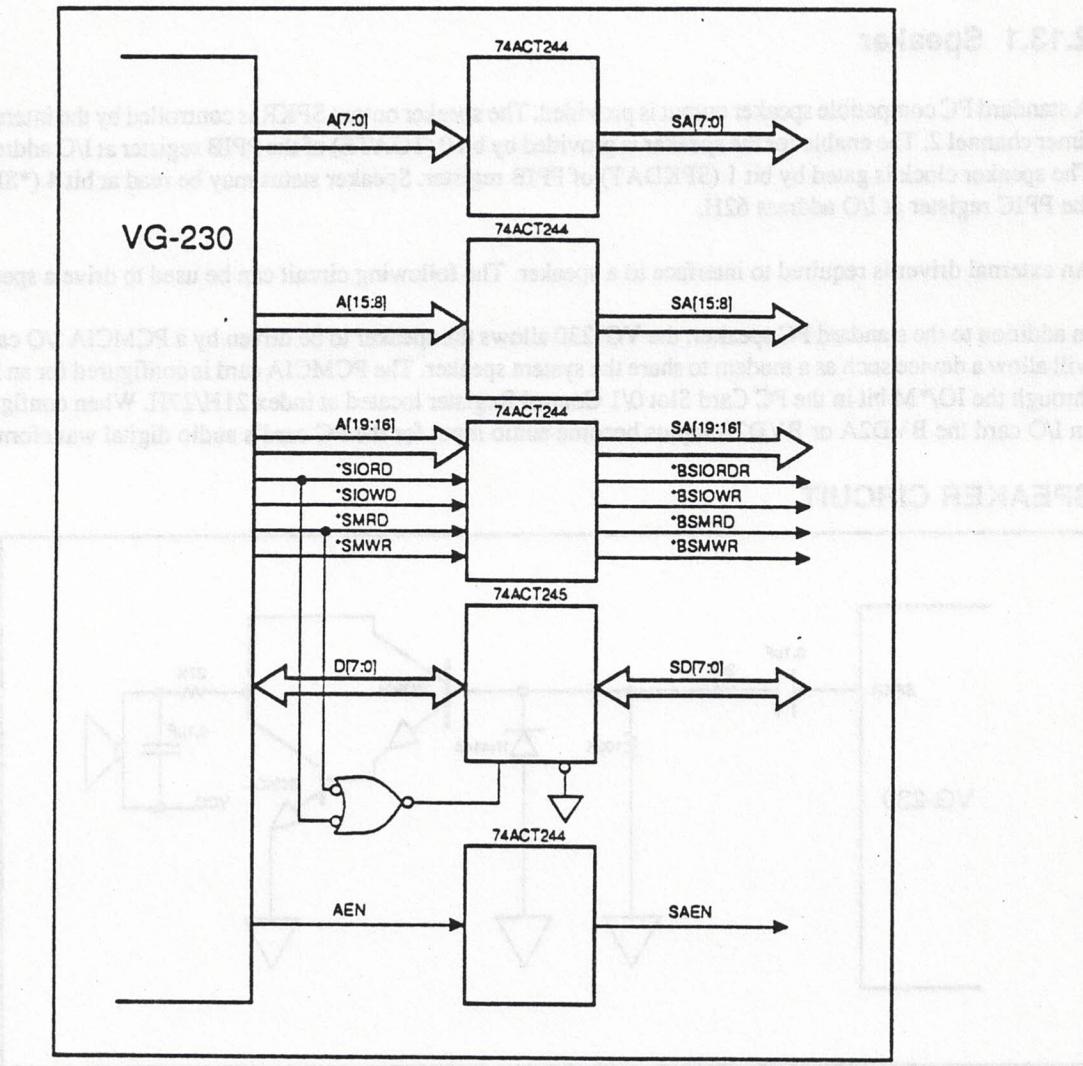


Figure 2.12-2

Data bus buffering for the XT bus requires an AND gate in addition to the 74ACT245. Connect the A side of the buffer to the VG-230 and the B side to the XT bus. Ground the *OE pin of the buffer, and connect the DIR pin to the output of the AND gate. The AND gate inputs are *SIORD and *SMRD. There is a possibility of brief contention at the beginning and end of a read cycle. If this causes problems, delay the falling edge of *SIORD and *SMRD to the XT bus, and delay the rising edge of the AND gate output.

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

2.13 Other Peripherals

2.13.1 Speaker

A standard PC compatible speaker output is provided. The speaker output SPKR is controlled by the internal 8254 timer channel 2. The enable for the speaker is provided by bit 0 (TGATE) of the PPIB register at I/O address 61H. The speaker clock is gated by bit 1 (SPKDAT) of PPIB register. Speaker status may be read at bit 4 (*SPKR) of the PPIC register at I/O address 62H.

An external driver is required to interface to a speaker. The following circuit can be used to drive a speaker.

In addition to the standard PC speaker, the VG-230 allows the speaker to be driven by a PCMCIA I/O card. This will allow a device such as a modem to share the system speaker. The PCMCIA card is configured for an I/O card through the IO/*M bit in the PC Card Slot 0/1 Control Register located at index 21H/27H. When configured for an I/O card the BVD2A or BVD2B inputs become audio input for the PC card's audio digital waveform.

SPEAKER CIRCUIT

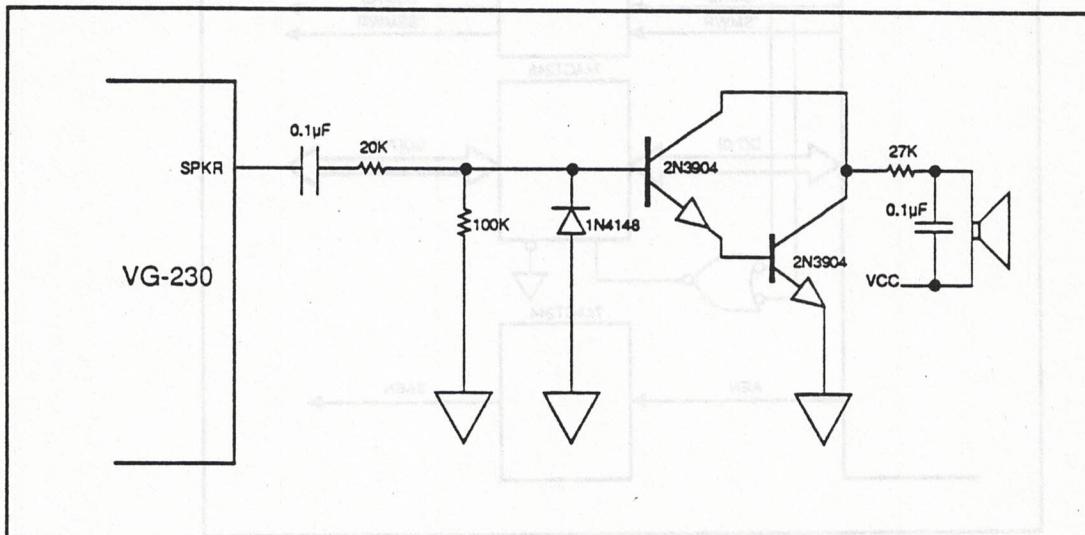


Figure 2.13-1

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

023-0V MEDEV
B10003 PROTOTYPING BOARD
B10003A JACOB

2.13.2 Revision Register

The VG-230 contains a revision register to identify versions of the silicon. This register is accessed through the index register at index 00H. Contact Vadem for information regarding version identification.

Name: **Revision Register**

Type: **Read Only**

Index: **00H**

Bit	Name	Default	Function
D[7:0]	REVD[7:0]		VG-230 Sub-Notebook Engine Silicon Revision Number

2.13.3 Floppy Expansion

The VG-230 PROTO board includes a floppy disk controller. The following block diagram illustrates the additional circuitry required to support a floppy disk interface.

FLOPPY EXPANSION

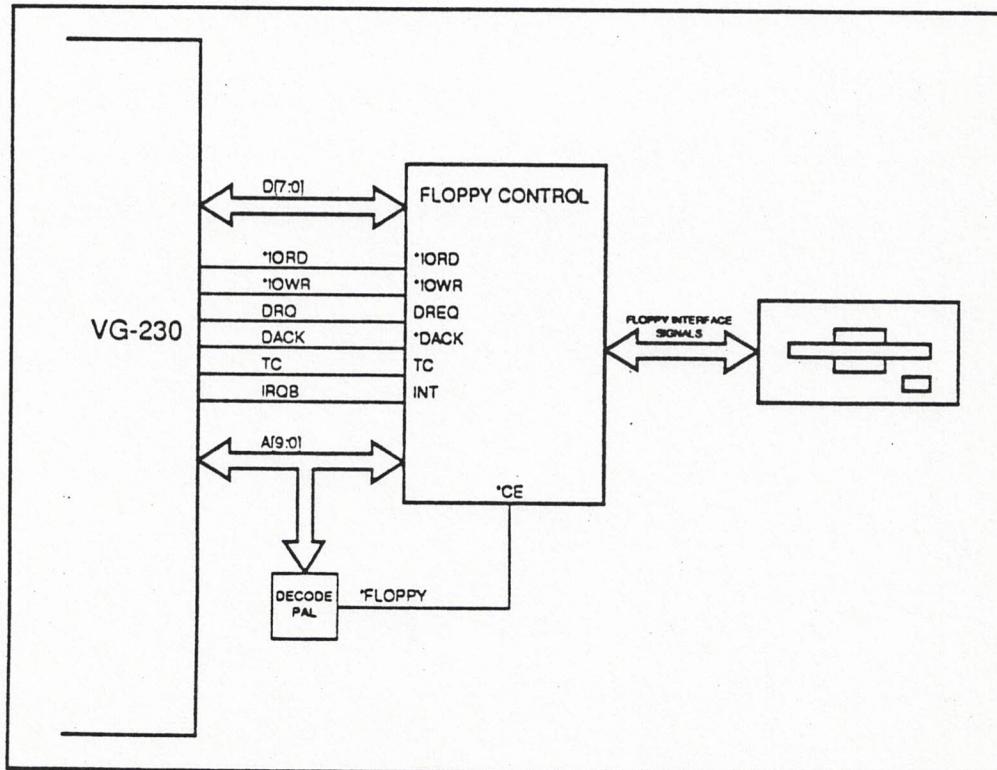


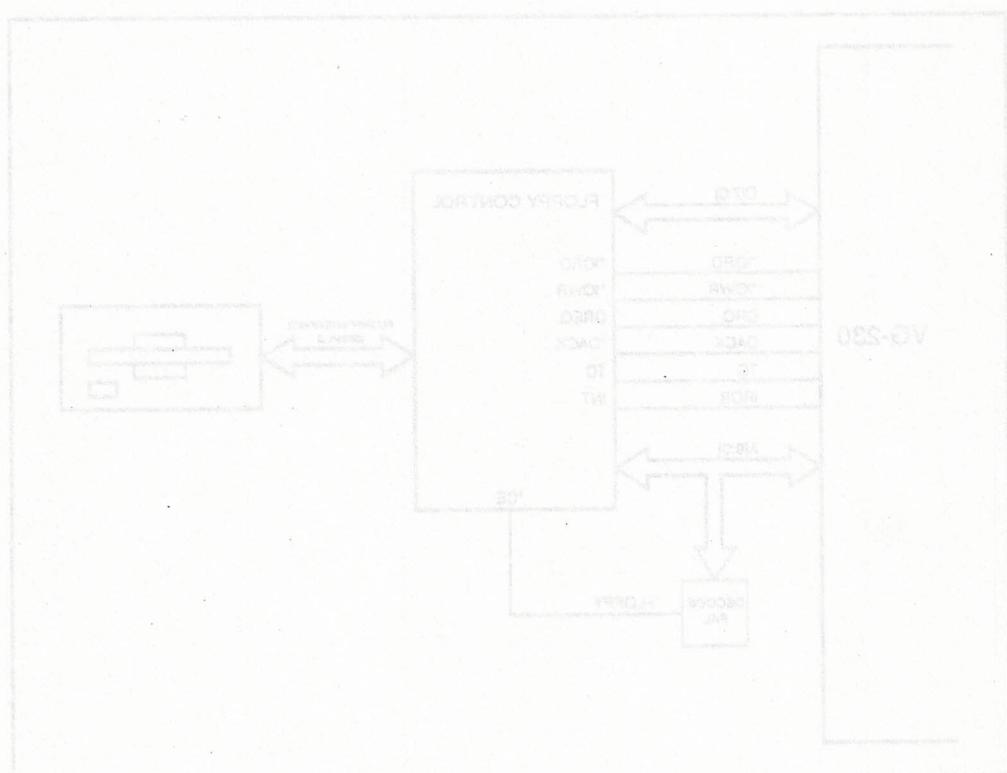
Figure 2.13-2

2.14 General Purpose I/O Pins (GPIO)

The VG-230 provides up to 4 GPIO pins when 200 line or smaller LCD panels are used. The LCDL[3:0] pins are only used when 400 line panels are used. When configured for GPIO these pins can provide general purpose input or output bits which can be used to control peripherals or monitor status. Some examples of possible uses include:

- LCD backlight control
- Additional low battery monitoring
- LED indicator control
- Serial EEPROM interface
- FLASH EPROM programming voltage control

The GPIO is enabled through the GPIO mode register at index 32H. Each of the LCDL[3:0] pins can be individually programmed as LCDL bits, GPIO bits or one of the listed internal signals. The default configuration is GPIO configured as input.. Each pin must first be configured for GPIO through the GPIO mode register. Control of the state of the pins is through the GPIO control register at index 33H.



VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

OSB-DV MEGAV
SUB-NOTEBOOK ENGINE
JANUARY 1993

Name: **GPIO Mode Register**
 Type: **Read/Write**
 Index: **32H**

Bit	Name	Default	Function
D[7:6]	GP3M[1:0]	00	GP3M1 GP3M0 LCDL3 Function 0 0 General Purpose Input-GPI3 0 1 LCDL3 1 0 General Purpose Output-GPO3 1 1 Reserved
D[5:4]	GP2M[1:0]	00	GP2M1 GP2M0 LCDL2 Function 0 0 General Purpose Input-GPI2 0 1 LCDL2 1 0 General Purpose Output-GPO2 1 1 SYSCLK-XT Bus Clock
D[3:2]	GP1M[1:0]	00	GP1M1 GP1M0 LCDL1 Function 0 0 General Purpose Input-GPI1 0 1 LCDL1 1 0 General Purpose Output-GPO1 1 1 ALE-Address Latch Enable
D[1:0]	GP0M[1:0]	00	GP0M1 GP0M0 LCDL0 Function 0 0 General Purpose Input-GPI0 0 1 LCDL0 1 0 General Purpose Output-GPO0 1 1 *DACK0 - Indicates Memory Refresh

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

VADEM VG-230
 SUB-NOTEBOOK ENGINE
 TECHNICAL REFERENCE

Name: **GPIO Control Register**
 Type: **Read/Write**
 Index: **33H**

Bit	Name	Default	Function
D[7:4]	Reserved	0H	Reserved Bits
D3	GPIO3	0	General Purpose I/O bit 3. When programmed as GPO, this bit is read/write and appears on the LCDL3 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL3 pin. Otherwise, this bit will read back low.
D2	GPIO2	0	General Purpose I/O bit 2. When programmed as GPO, this bit is read/write and appears on the LCDL2 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL2 pin. Otherwise, this bit will read back low.
D1	GPIO1	0	General Purpose I/O bit 1. When programmed as GPO, this bit is read/write and appears on the LCDL1 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL1 pin. Otherwise, this bit will read back low.
D0	GPIO0	0	General Purpose I/O bit 0. When programmed as GPO, this bit is read/write and appears on the LCDL0 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL0 pin. Otherwise, this bit will read back low.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

DCS-30V MEGAV
SUB-NOTEBOOK ENGINE
POWERFUL, LIGHTWEIGHT

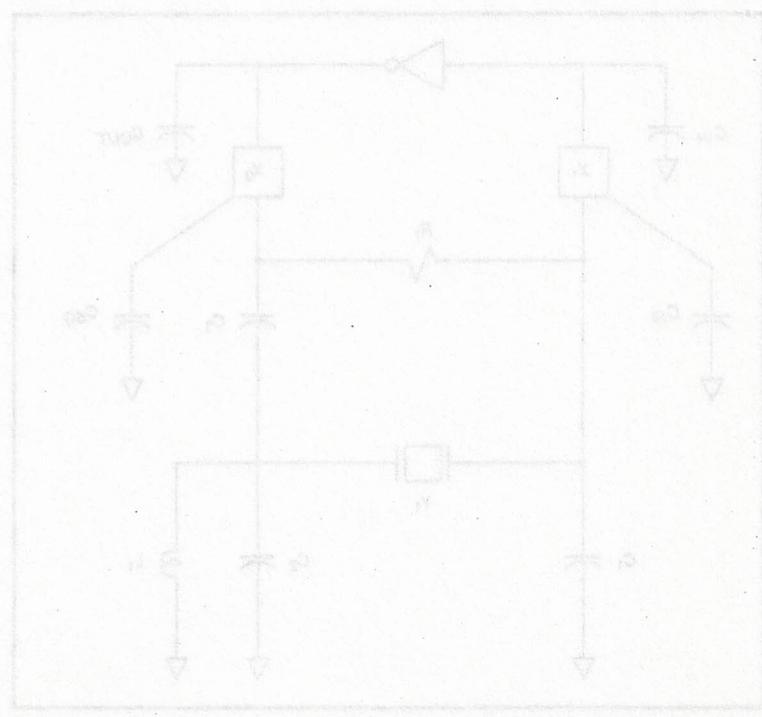
The LCDL[3:0] pins can also be used to bring out the following internal signals.

- **SYSCLK** This clock is used as the timebase for external memory and I/O access
- **ALE** Address latch enable
- ***DACK0** The refresh signal

The following table lists the functions of each pin:

400 Line LCD Pins	Internal Signal	GPIO
LCDL3	not used	GPIO3
LCDL2	SYSCLK	GPIO2
LCDL1	ALE	GPIO1
LCDL0	*DACK0	GPIO0

HIGH FREQUENCY ACUT OUTLINE DRAWING



VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

3.0 IMPLEMENTATION NOTES

3.1 Crystal/Oscillator Selection

The VG-230 requires three crystals for operations, a 32.215905/28.63636MHz, a 3.6864MHz and a 32.768KHz. For reliable operation of the VG-230 it is critical to select the correct crystal and bias circuitry. The following information is provided to aid in the selection of the crystal and associated external components.

3.1.1 Selection of 32.215905/28.63636 MHz Crystal Oscillators

The general circuit for an overtone crystal oscillator using a CMOS gate inverter is shown in Figure 3.1-1. C_{IN} is the symbol used to represent the inverter input capacitance. C_{SI} represents the PC layout stray capacitance at the input. C_{OUT} is the symbol used to represent the inverter output capacitance. C_{SO} represents the PC layout stray capacitance at the output. R_f is a general linear bias for the inverter usually selected in the range from $1M\Omega$ to $10M\Omega$. Normally this resistor exists within the ASIC, therefore, an external resistor is not needed. C_3 is used only as a DC block for inductor isolation usually selected in the range from $0.001\mu F$ to $0.01\mu F$. Y_1 is the crystal to be operated in the overtone mode. C_1 , C_2 and L_1 complete the feedback network for the inverter. If the crystal were to be operated in the fundamental mode, L_1 would not be used. The combination of C_2 and L_1 forms a tank circuit which is usually set to resonate at a frequency midway between the crystal's fundamental frequency and its third overtone frequency. The result is that, at the fundamental frequency, the feedback network has inadequate gain due to the inductive impedance of the tank circuit and this frequency is suppressed. At the overtone frequency, conditions for oscillation can be achieved because the impedance of the tank circuit is capacitive.

HIGH FREQUENCY XTAL OSCILLATOR CONFIGURATION

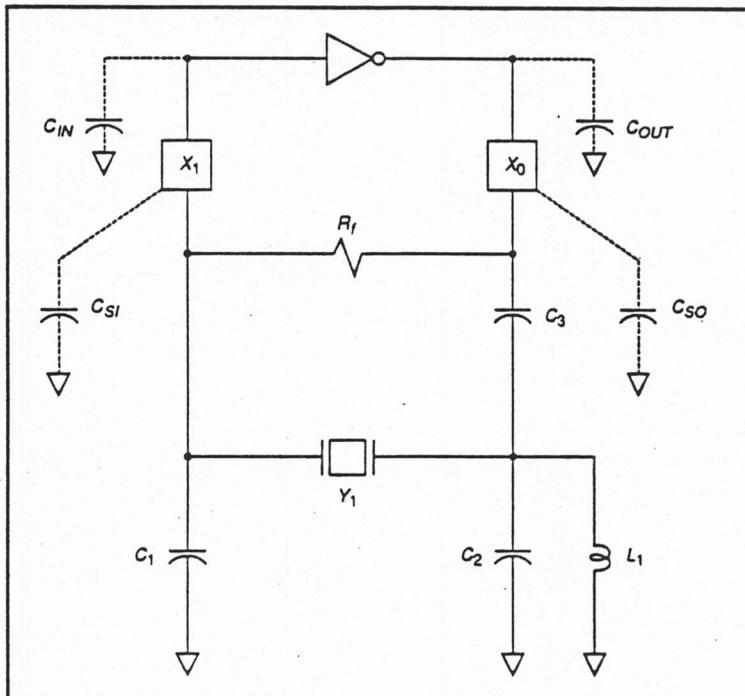


Figure 3.1-1

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

R_f and C_3 are not critical and are generally selected from the above ranges such that overall oscillator AC performance is not affected. Approximate values for C_1 , C_2 and L_1 can be calculated from the following equations:

In the following, C_L is the manufacturer's specified crystal load capacitance, f_3 is the crystal's third overtone frequency, and f_1 is the crystal's fundamental frequency.

$$\text{Let } C_{X_1} = C_1 + C_{IN} + C_{SI} = \text{Total Capacitance at } X_1 \quad (\text{A})$$

$$C_{X_o} = C_2 + C_{OUT} + C_{SO} = \text{Total Capacitance at } X_o \quad (\text{B})$$

$$\text{Then } \frac{1}{2\pi\sqrt{L_1 \cdot C_{X_o}}} = \frac{f_1 + f_3}{2} \quad (\text{C})$$

$$C_{EO} = C_{X_o} - \frac{1}{(2\pi \cdot f_3)^2 \cdot L_1} \quad (\text{D})$$

$$C_L = \frac{C_{EO} \cdot C_{X_1}}{C_{EO} + C_{X_1}} \quad (\text{E})$$

$$1.1 < \frac{C_{EO}}{C_{X_1}} < 1.5 \quad (\text{F})$$

(= feedback network gain)

The above equations can be simplified. Let $C_{EO}=1.3 \cdot C_{X_1}$ to provide enough gain for reliable oscillation.

Substitute into equation (E) to yield:

$$C_{X_1} = 1.75 \cdot C_L \quad (\text{G})$$

$$C_{EO} = 2.28 \cdot C_L \quad (\text{H})$$

Example calculation: at 40 MHz

$$\text{Since } f_1 = \frac{f_3}{2}, \text{ solving (C) for } L_1$$

and substituting into (D) yields:

$$C_{EO} = .56 \cdot C_{X_o} \quad (\text{I})$$

$$\text{and therefore } C_{X_o} = 4.11 \cdot C_L \quad (\text{J})$$

Substituting (H) and (J) into (D) and solving for L_1 yields:

$$L_1 = \frac{1}{72 \cdot C_L \cdot f_3^2} \quad (\text{K})$$

Substituting (G) into (A) and (J) into (B) yields:

$$C_1 = 1.75 \cdot C_L - C_{IN} - C_{SI} \quad (\text{L})$$

$$C_2 = 4.11 \cdot C_L - C_{OUT} - C_{SO} \quad (\text{M})$$

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

VADEM VG-230
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

Equations (K), (L) and (M) will determine the values of the critical components. C_{IN} and C_{OUT} should be taken from the Vadem VG-230 Data Manual, and C_L from the crystal data sheet. C_S1 and C_S0 must be determined from the PC layout.

After the first-order values for C_1 , C_2 and L_1 have been determined using the equations above, the values can be optimized to approximate a 50/50 duty cycle of the output clock as a function of supply voltage by iteratively varying component values on an actual printed circuit layout:

First, select a reasonable reference point for the oscillator duty cycle which is below the desired operating duty cycle. At its start voltage, the shorter of the oscillator's high time and low time is usually approximately 25% of the duty cycle (25/75 or 75/25 duty cycle). A reference point of 40/60 (or 60/40 depending on whether the high time or low time starts out longer) is a good choice.

Next, for each component, find the component value for which the output clock duty cycle first reaches the reference point and for which the supply voltage is minimized. A small number of iterations through the components in the network results not only in an oscillator with a constant output duty cycle over a wide operating voltage range, but also usually results in an operating duty cycle better than 45/55 (55/45) and a stable circuit design that can tolerate at least 20% variance in component values with minimal performance impact.

The circuit should be kept close to the chip to minimize parasitic and cross-talk effects. Also, the circuit should not oscillate without the crystal. Finally, as noted in the first suggested reference, the circuit shown should be considered a starting point and not used without optimization and thorough testing in the configuration actually used.

Suggested References:

1. Frerking, Marvin E., *Crystal Oscillator Design and Temperature Compensation*,
Van Nostrand Reinhold, 1978.
2. Parzen, Benjamin, *Design of Crystal and Other Harmonic Oscillators*,
John Wiley & Sons, 1983.
3. Williamson, Tom, *Oscillators for Microcontrollers*,
Application Note AP-155, Intel Corporation, June 1983.

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

osg-ov MEDAV
SUB-NOTEBOOK ENGINE
TECHNICAL REFERENCE

3.1.2 Selection of 3.6864MHz Crystal

The 3.6864MHz crystal is used as the timebase for the internal 82C50 SIO. Internally this clock is divided by two, to 1.8432MHz, to drive the 82C50 cell. Figure 3.1-2 shows the configuration for the external crystal. Listed below are the recommended crystal specifications:

Frequency:	3.6864MHz
Tolerance:	50ppm
Aging:	5ppm/year
Series Resistance:	150ohms (max)
Drive Level:	1mW (min)
Shunt Capacitance:	7pF
Load Capacitance:	16pF

SIO CRYSTAL OSCILLATOR

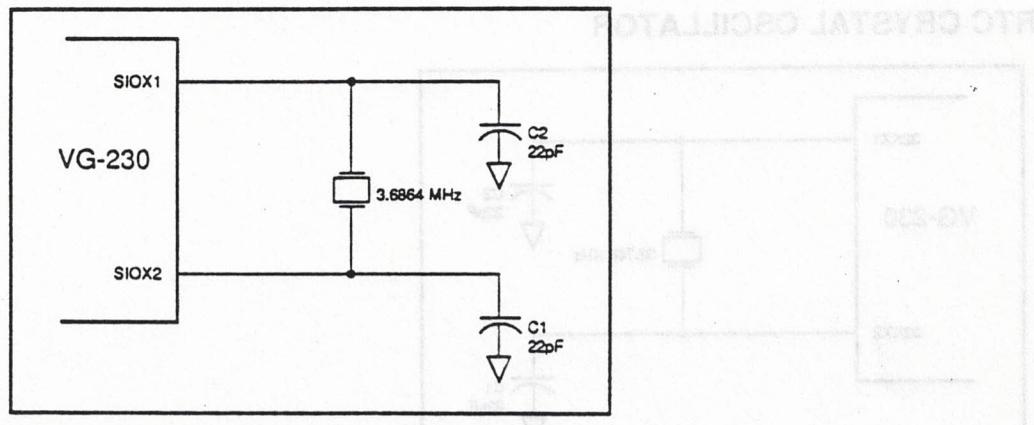


Figure 3.1-2

3.1.3 Selection of 32.768KHz Crystal

The 32.768KHz crystal is used for the RTC timebase, power management timers, and SUSPEND refresh of the DRAM array. This crystal will always oscillate when power is applied to the VG-230. The suggested configuration for the 32KHz oscillator is show in figure 3.1-3. We recommend the following crystal parameters:

Frequency	32.768KHz \pm 30ppm
Quality Factor	Q=80,000 - 100,000
Load Capacitance	CL = 8 - 13pF
Series Resistance	RS = 20 - 40K
Shunt Capacitance	C0 = 1.0 - 1.5pF
Motional Capacitance	C1 = .0025pF - .0035pF
Capacitance Ratio	C0/C1 = 400 - 520
Drive Level:	1mW (min)
Aging:	3ppm/year

RTC CRYSTAL OSCILLATOR

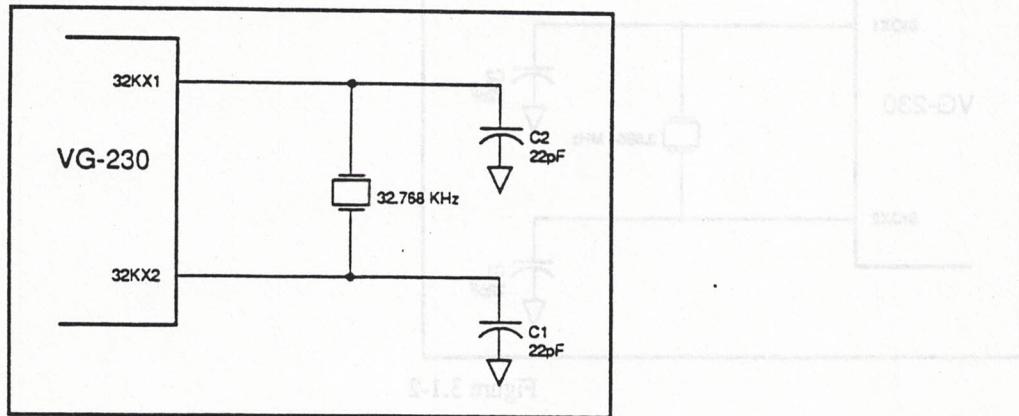


Figure 3.1-3

VADEM VG-230

SUB-NOTEBOOK ENGINE

TECHNICAL REFERENCE

OSR-0V M30AV
S30AV M30AV
S30AV M30AV
S30AV M30AV

3.2 Bus loading Specifications

The VG-230 has been designed for a small portable systems. Its single bus architecture provides maximum functionality in a 160 pin package. The inherent limitation of this architecture is the amount of devices that can placed on the unbuffered bus. The address and data lines are designed to provide the following drive:

A[25:0]	8mA	200pF
D[15:0]	8mA	200pF
MC[9:0]	8mA	200pF
*SIORD, *SIOWR	4mA	100pF
*SMRD, *SMWR	4mA	100pF

In addition the designer should be aware of the following drive capabilities:

AEN, TC, *DACK	4mA	100pF
SCAN[7:0]	8mA	200pF
*ROMCE[1:0]	4mA	100pF
*RESOUT	12mA	200pF
*CE1A, *CE2A	8mA	200pF
*REGA	8mA	200pF
LCDU[3:0], LCDL[3:0]	8mA	200pF
LCD Control outputs	8mA	200pF
All RS232 outputs	4mA	100pF
All VP signals	4mA	100pF
SPKR	8mA	200pF

3.3 Layout Considerations

Proper layout techniques will insure proper operation of the VG-230. These techniques will also help in meeting FCC part 15 and similar approvals. The VG-230 is fabricated using a 0.8 micron high speed CMOS process. Care must be taken in the layout to provide a low inductance power path. Proper bypassing and multilayer designs are a must for proper operation. All power pins should be connected directly to the power planes using as short a trace as possible. 0.1 to 0.33 uF ceramic monolithic surface mount capacitors should be placed as close to the device as possible. The capacitors should be low ESR types, such as X7R type.

RAM arrays, ROM arrays, and PCMCIA PC cards should be properly bypassed and located as close as possible to the VG-230. Crystals should also be located as close as possible to the XTAL pins.

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

3.4 Battery Life Calculation

The battery life of a given system is determined by the current drain of the system and the capacity of the battery. Capacity of the battery is expressed in Ampere-Hour (Ah). This number is determined by the battery manufacturer assuming the current draw is at one-tenth of the rated capacity at a specific temperature. Table 3.4-1 shows the capacity of a Ni-Cad battery versus discharge rate and temperature.

Capacity Coefficient (K)

Discharge Rate	Temperature					
	C -20	-10	0	10	20	40
F -4	14	32	50	68	104	
C/5	0.70	0.80	0.90	1.10	1.10	0.95
C/2	0.65	0.75	0.85	1.05	1.05	0.90
C	0.50	0.70	0.80	0.95	0.95	0.85
1.5C	0.47	0.65	0.75	0.92	0.92	0.80
2C	0.40	0.60	0.70	0.88	0.88	0.75

Table 3.4-1

VADEM VG-230

SUB-NOTEBOOK ENGINE TECHNICAL REFERENCE

A battery's Actual Capacity (C_a) is a function of its Nominal Capacity (C):

$$C_a = K \cdot C$$

where the Capacity Coefficient (K) is a function of the battery's discharge rate and temperature.

After the Actual Capacity is determined using the battery manufacturer's data sheet, the battery life calculation for a system proceeds as follows:

The total Energy (E) available for the system is:

$$E = n \cdot V_c \cdot C_a$$

where n is the number of cells and V_c is the voltage for each cell.

The theoretical power consumption (P_s) for a given supply voltage can be calculated as follows:

$$P_s = V_s \cdot I_s$$

Where V_s is the regulated output Supply Voltage and I_s is the output Supply Current for the same supply voltage. Due to losses, the Actual Power (P_a) consumed for a given supply voltage is higher than the theoretical power by a factor equal to the efficiency of the power supply (η). Therefore, the Actual Power consumed is:

$$P_a = \frac{P_s}{\eta}$$

In a system with multiple regulated output voltages, the efficiency of each supply voltage may differ. Therefore, the Total Power (P_t) is equal to the sum of the Actual Power consumed for each supply voltage:

$$\begin{aligned} P_t &= \frac{P_{s_1}}{\eta_1} + \frac{P_{s_2}}{\eta_2} + \dots + \frac{P_{s_m}}{\eta_m} = \\ &= \sum_m \frac{P_{s_i}}{\eta_i}, \text{ where } m \text{ is the number of supply voltages} \end{aligned}$$

Finally, the Battery Life in hours (L) can be calculated by the following formula:

$$L = \frac{E}{P_t}$$

The power consumption for a conventional CMOS system is dependent on the rates of its clocks. By reducing clock rates, power consumption will drop. Therefore, battery life can be extended if the system clocks and/or idling peripherals can be shut off when the system is not active. The VG-230's power management technology is designed to keep the system in DOZE mode whenever possible. This mode is totally transparent to the user, since the clocks and/or peripherals will return to ON mode as soon as activity is detected.

In a typical application, the system will be in ON mode only a very small percentage of the time. To calculate the battery life of a VG-230 system, the designer can effectively neglect the ON mode power consumption and use the DOZE mode power consumption. Table 3.4-2 shows the typical current consumption of the VG-230 under different power management modes:

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VG-230 Power Consumption

	ON	DOZE	SLEEP	OFF
8 MHz	60ma	35ma	100 μ a	100 μ a
16MHz	90ma	35ma	100 μ a	100 μ a

Table 3.4-2

For the purpose of battery life calculation, the current consumption of the VG-230 at 16 MHz is 35 ma.

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4.0 NON-MASKABLE INTERRUPTS AND SYSTEM MANAGEMENT MODE (SMM)

The VG-230 uses Non-Maskable Interrupts (NMI) to provide enhancements to the standard PC architecture. These enhancements include:

- Power Management
- Internally scanned keyboard
- System Management Mode (SMM)

NMI DISTRIBUTION

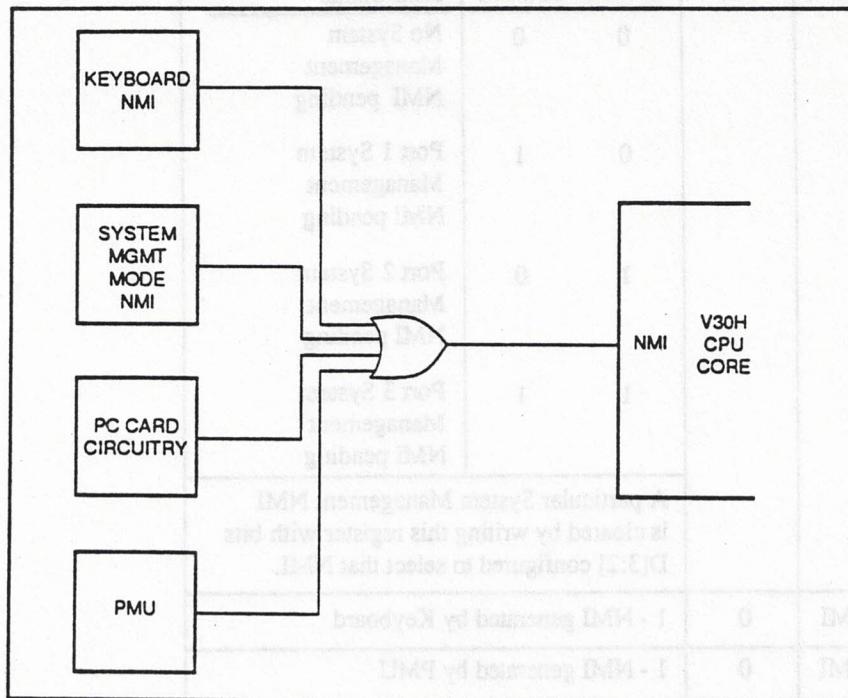


Figure 4.0-1

There are several NMI sources within the VG-230. When an NMI occurs the NMI handler can determine the source of the NMI by first reading the Main NMI Status Register located at index 19H. The method of clearing the NMI depends on the source of the NMI.

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Name: Sub-Notebook Engine Main NMI Status Register

Type: Read/Write

Address: 19H

Bit	Name	Default	Function	
D[7:4]	TA[3:0]	X	NMI Trap Address bits. ISA[3:0] are latched when an NMI is generated by the System Management Unit to drive these bits.	
D[3:2]	ENMI[1:0]	00	ENMI1	ENMO0
			0	0
			0	1
			1	0
			1	1
A particular System Management NMI is cleared by writing this register with bits D[3:2] configured to select that NMI.				
D1	KBDNMI	0	1 - NMI generated by Keyboard	
D0	PMUNMI	0	1 - NMI generated by PMU	

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4.1 Power Management NMIs

Transparent power management is accomplished through a combination of automatic state transitions and NMI service routines. The PMU generates several types of NMIs to request state transition or I/O status. The following NMI sources are available:

Name: PMU NMI Mask Register

Type: Read/Write

Address: C4H

Bit	Name	Default	Function
D7	Reserved	0	Reserved bit
D6	MSK_NMI	1	Mask NMI input to PMU
D5	MSK_SUSPEND	1	Mask SUSPEND timeout
D4	MSK_SLEEP	1	Mask SLEEP timeout
D3	Reserved	1	Reserved bit
D2	MSK_LB	1	Mask LB input
D1	MSK_EXT	1	Mask EXT input
D0	Reserved	1	Reserved bit

When an NMI occurs and the Main NMI status register indicates that a power management NMI is the source, the NMI handler must check the PMU status register to determine the source of the NMI.

Note: MSK_NMI should always be set to 0 on initialization.

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Name: PMU Status Register

Type: Read/Write

Index: C0H

Bit	Name	Default	Function
D7	Resume	0	Resuming from SUSPEND (warmstart)
D[6:5]	WU[1:0]	00	Wakeup code bits
D[4:2]	NMI[2:0]	000	NMI cause code bits
D[1:0]	STATE[1:0]	00	State bits

Note: Only D0 and D1 are affected by a write.

State Code									Function
7	6	5	4	3	2	1	0		
X	X	X	X	X	X	0	0	command to ON	
X	X	X	X	X	X	0	1	command to DOZE	
X	X	X	X	X	X	1	0	command to SLEEP	
X	X	X	X	X	X	1	1	command to SUSPEND	
1	1	1	1	1	1	1	1	command to OFF	

Note: The NMI cause, state and wakeup codes are decoded as follows for a read to C0H.

Wakeup		NMI		State	
Code	Cause	Code	Cause	Code	Cause
00	None	000	None, or INMI	00	ON
01	EXT	001	EXT	01	DOZE
10	RTC	010	LB	10	SLEEP
11	RI	011	Reserved	11	SUSPEND
		100	SLEEP Timeout		
		101	SUSPEND Timeout		
		110	SLEEP to ON (Activity)		
		111	Reserved		

Any of the PMU's NMIs are cleared by reading the NMIMASK register at index C4H.

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4.2 Keyboard NMIs

The NMIs referred to as Keyboard NMIs are generated in conjunction with the keyboard scanning function. See section 2.8 for more information on the keyboard scan hardware.

Name: Sub-Notebook Engine Shift and NMI Status Register Register
Type: Read/Write
Address: INDEX 0CH

Bit	Name	Default	Function
D7	KEYNMI	0	1 - NMI caused by Keyboard Input. Writing this register with bit D7 set high will clear both the NMI signal and the KEYNMI bit.
D6	STMONMI	0	1 - NMI caused by Keyboard Scan Time Out. Writing this register with bit D6 set high will clear both the NMI signal and the STMONMI bit.
D5	PPIBNMI	0	1 - NMI caused by write to PPIB port requesting Keyboard Diagnostics. Writing this register with bit D5 set high will clear both the NMI signal and the PPIBNMI bit.
D4	KNMIEN	0	1 - Enable Keyboard Input NMIs.
D3	SNMIEN	0	1 - Enable Periodic NMIs generated by the Scan Timer.
D2	PNMIEN	0	1 - Enable NMIs caused by writes to PPIB port requesting Keyboard Diagnostics.
D1	Reserved	0	Reserved for future use.
D0	SH4	0	SHFT4 input status. 0 - SHFT4 switch position is closed. 1 - SHFT4 switch position is open. Note: In PC/XT serial I/F mode, this register bit is ignored.

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4.3 System Management Mode NMIs

The VG-230 provides a mechanism for monitoring access to any I/O device. Hardware within the VG-230 allows the CPU to be interrupted on any access to an I/O port. Up to three I/O ports may be monitored. This feature is useful for emulation of I/O ports or monitoring of selected I/O for power management.

There are three sets of NMI Trap registers. The address of the I/O device to be monitored is programmed into PxTA[0:9] located in the NMI Trap low register and NMI trap high register. The number of bytes in the address range is programmed into the high register. The type of R/W access used to generate the NMI is selected in NMI Trap high register. Also selectable is whether 16 bit or 10 bit I/O decode is used.

Name: Sub-Notebook Engine Port 1 NMI Trap Address Low Register
Type: Read/Write
Index: 1AH

Bit	Name	Default	Function
D[7:0]	P1TA[7:0]	00H	Lower 8 address bits of the I/O address which will be emulated.

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Name: Sub-Notebook Engine Port 1 NMI Trap Address High Register
 Type: Read/Write
 Index: 1BH

Bit	Name	Default	Function		
D[7:6]	P1EN[1:0]	00	P1EN1	P1EN0	Port 1 Emulation NMI Mode
			0	0	Disable Port 1 NMIs.
			0	1	Generate NMI on IORD from Port 1 address.
			1	0	Generate NMI on IOWR to Port 1 address.
			1	1	Generate NMI on IORD from or IOWR to Port 1 address.
D[5:4]	P1RNG[1:0]	00	P1RNG1	P1RNG0	Port 1 Address Range
			0	0	2 Bytes
			0	1	4 Bytes
			1	0	8 Bytes
			1	1	16 Bytes
D3	P1MIR	0	0 - Disable address mirroring. Port 1 decoding is based upon ISA[15:0], and is enabled only when ISA[15:10] are all low. 1 - Enable address mirroring. Port 1 decoding is based only upon ISA[9:0].		
D2	Reserved	0	Reserved for future use.		
D[1:0]	P1TA[9:8]	00	Upper 2 address bits of the I/O address which will be emulated.		

When access is made to an enabled NMI trap address, an NMI is generated. The NMI handler can determine the NMI source by reading the Main NMI status register at index 19H. If the NMI source is from the trap logic, the handler can clear the NMI by writing to the appropriate ENMI[0:1] bits.

Note: Additional information on using System Management Mode NMIs can be found in the VG-230 BIOS Developer's Manual.

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5.0 ICE / TEST SUPPORT

Integrated into the VG-230 is support for debugging by means of a standard V30H hardware emulator (ICE). To enable this feature, two VG-230 devices are connected in a Master/Slave arrangement. The collective pinout of both devices is re-assigned to interface to the target system and to the V30H hardware emulator. The VG-230 may also be electrically isolated (outputs driven tristate) for debugging purposes. Briefly, the procedures are as follows:

- **ICE_MASTER Mode**

To enter ICE_MASTER mode, the TEST pin has to be driven high while A[25:22] are passively pulled to 0101 via pull-up/pull-down resistors during system power up reset. To return to normal operation, system power up reset is required with TEST pin being low.

- **ICE_SLAVE Mode**

To enter ICE_SLAVE mode, the TEST pin has to be driven high while A[25:22] are passively pulled to 0110 via pull-up/pull-down resistors during system power up reset. To return to normal operation, system power up reset is required with TEST pin being low.

- **Output Tristate Mode**

To enter Output Tristate mode, the TEST pin has to be driven high while A[25:22] are passively pulled to 1111 via pull-up/pull-down resistors during system power up reset. All outputs will then be tristated except the NRESOUT signal (pin 35 - driven low). To return to normal operation, system power up reset is required with TEST pin being low.

Operation Modes	TEST	A[25:22]
Normal (VG-230)	0	0000
ICE_MASTER	1	0101
IEC_SLAVE	1	0110
Output Tristated	1	1111

For additional information and implementation schematics refer to the following:

VG-230 ICE Adapter User's Manual

Notes: A detailed description of the VG-230 ICE adapter can be found in the VG-230 ICE Adapter User's Manual.

Notes: A detailed description of the VG-230 ICE adapter can be found in the VG-230 ICE Adapter User's Manual.

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