



VADEM

mebaV 1991 © Vadem Corporation
All Rights Reserved

or, revolution, allows the customer to bevelled at mebaV yg bedizmali komoncjal
tadi to aneksi to mamegutihinga voi ton, zan ali tel mebaV yg basuraq si yahidikom
to rohulqal qd beberg si tamed qM. sas qd mord. loren qsa duduq bant to argh
rondaq qd nigh qd ravigat mebaV. mebaV lo argh masing to jasaq qda telur, murni, ba
zawar, modir, emu qd

VADEM VG-230

mebaV evlaseqer wadi ur gudis ramaq bennakom adhaebat
SUB-NOTEBOOK ENGINE

DATA MANUAL

MEGA-
TEL 218, mebaV 1991
TURK ALI, mebaV
MEGA-TEL 218
TELE-TEL 200, mebaV

NOVEMBER 1992



Electronic Marketing Specialist
P.O. Box 593229 • Orlando, FL 32859
(407) 855-0843



Copyright © 1992 Vadem
All Rights Reserved

Information furnished by Vadem is believed to be accurate and reliable. However, no responsibility is assumed by Vadem for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Vadem. Vadem reserves the right to change specifications at any time without notice.

Trademarks mentioned herein belong to their respective companies.



1885 Lundy Ave., Ste. 201
San Jose, CA 95131
Tel: 408 943-9301
Fax: 408 943-9735

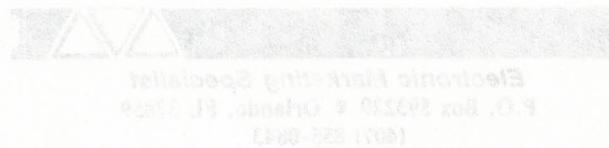


TABLE OF CONTENTS

PREFACE	
Product Overview	1
Key Features	1
CHAPTER 1	
Pin Assignment	5
CHAPTER 2	
Functional Description	17
Overview	17
Single-Bus Architecture	17
Processor.....	18
PC Card Controller	18
Keyboard	18
System Management Unit	19
Power Management Unit	19
System Power Management	20
LCD Power Management	21
PC Card Power Management	21
Serial Port Power Management.....	22
LCD Controller.....	23
Memory Controller and Memory Manager	24
Basic Peripherals and Core Logic	27
Serial Port	27
Parallel Port	27
Real Time Clock	27
DMA Controller	27
Interrupt Controller	27
Timer	28
Clocks	28
ICE Support	28
General Purpose I/O	28

CHAPTER 3

Keyboard Mode Register	08H	48
Keyboard Scan Control Register	09H	48
Keyboard Return Status Low Register	0AH	49
Keyboard Return Status High Register	0BH	49
Keyboard Shift and NMI Status Register	0CH	50
ICU Mode Register	0DH	51
DMA Mode Register	0EH	52
SIO Mode Register	10H	53
SIO Power Control Register	11H	53
Timer Mode Register	13H	54
PIO Mode Register	18H	54
Main NMI Status Register	19H	55
Port 1 NMI Trap Address Low Register	1AH	55
Port 1 NMI Trap Address High Register	1BH	56
Port 2 NMI Trap Address Low Register	1CH	56
Port 2 NMI Trap Address High Register	1DH	57
Port 3 NMI Trap Address Low Register	1EH	57
Port 3 NMI Trap Address High Register	1FH	57
PC Card Controller Mode Register	20H	58
PC Card Slot 0 Control Register	21H	59
PC Card Slot 0 Status Register	22H	60
PC Card Slot 0 Interrupt Mask Register	23H	61
PC Card Slot 0 I/O High Address Register	24H	61
PC Card Slot 0 I/O Low Address Register	25H	61
PC Card Slot 0 I/O Address Range Register	26H	62
PC Card Slot 1 Control Register	27H	63
PC Card Slot 1 Status Register	28H	64
PC Card Slot 1 Interrupt Mask Register	29H	65
PC Card Slot 1 I/O High Address Register	2AH	65
PC Card Slot 1 I/O Low Address Register	2BH	65
PC Card Slot 1 I/O Address Range Register	2CH	66
PC Card Power Control Register	2DH	67
PC Card Activity Timer Register	2EH	68

BIOS Time Base Low Register	30H	68
BIOS Time Base High Register	31H	68
GPIO Mode Register	32H	69
GPIO Control Register	33H	70
Top of Memory Register	38H	71
ICU Shadow Register	40H	71
RTC Seconds Register	70H	72
RTC Minutes Register	71H	72
RTC Hours Register	72H	72
RTC Day Low Register	73H	73
RTC Day High Register	74H	73
RTC Alarm Seconds Register	75H	73
RTC Alarm Minutes Register	76H	74
RTC Alarm Hours Register	77H	74
RTC Alarm Day Register	78H	74
RTC Mode Register	79H	75
RTC Status Register	7AH	75
PMU Status Register	C0H	76
PMU Supply Register	C1H	77
PMU Control Register	C2H	77
PMU Activity Mask Register	C3H	78
PMU NMI Mask Register	C4H	78
PMU I/O Range (IORNG) Register	C5H	79
PMU Power (PWR) Registers	79	
PMU Power On (PWRON) Register	C6H	79
PMU Power Doze (PWRDOZE) Register	C7H	79
PMU Power Sleep (PWRSLEEP) Register	C8H	79
PMU Power Suspend (PWRSUSPEND) Register	C9H	79
PMU Polarity Register	CAH	80
PMU Output Register	CBH	80
PMU Timer Registers	80	
PMU DOZE Timer Register	CCH	81
PMU SLEEP Timer Register	CDH	81

PMU SUSPEND Timer Register	CEH	82
PMU LCD Timer Register	CFH	82
PMU LCD Sequence Register	D4H	83
PMU Resume Status	DAH	83
PMU Activity Status	DBH	83
CGA LCD Indexed Register Summary		84
CGA Index Register	3D4H	84
CGA Data Register	3D5H	84
Mode Select Register A	3D8H	84
Status Register	3DAH	84
Mode Select Register B	3DEH	84
Register Indices		85
Cursor Start Raster Register	0AH	86
Cursor End Raster Register	0BH	86
Display Start Address MSB Register	0CH	87
Display Start Address LSB Register	0DH	87
Cursor Location Address MSB Register	0EH	87
Cursor Location Address LSB Register	0FH	87
Window Start MSB Register	C0H	88
Window Start LSB Register	C1H	88
LCD Display Control Register	C2H	89
LCD Panel Resolution Register	CAH	90
Gray Scale Register	CBH	90
LCD Mode Register	CCH	91
Ink Plane Register	CDH	92
Mode Select Register A	3D8H	93
Status Register	3DAH	93
Mode Select Register B	3DEH	94

	CHAPTER 4	
18	Specifications	95
18	Overview	95
18	Processor	95
18	Memory	95
18	I/O	96
18	Configurable I/O	96
18	Power Management	97
18	LCD Controller	97
18	Electrical Characteristics	98
18	DC Characteristics	98
18	Mechanical Specifications	98
18	Absolute Maximum Ratings	99
18	Operating Conditions	99
18	Capacitance DC Specifications	99
18	ICC Specifications	99
18	Electrostatic Discharge Characteristics	99
	CHAPTER 5	
18	Timing Tables	101
18	Memory Cycles	101
18	PC Card Memory Cycles	102
18	PC Card I/O Cycles	102
18	DMA Cycles	103
18	XT Bus Cycles	103
18	IOCHRDY Timing	103
18	Keyboard Timing	103
18	LCD Timing Cycles	104

CHAPTER 6

Timing Diagrams	105
Memory Cycles	105
SRAM / PSRAM.....	105
DRAM Timing	105
ROM Timing	106
DRAM Refresh Timing.....	106
PSRAM Refresh Timing	106
PC Card	107
PC Card Memory Timing	107
PC Card I/O Timing	108
DMA.....	109
XT Bus Cycle Timing	110
IOCHRDY Timing	110
Data Router (16 Bit)	110
PIO Timing	111
Keyboard	111
XT Serial I/F Timing.....	111
LCD	111
LCD Interface Timing.....	111
LCD Power Sequencing Timing	112
DMA to DRAM Timing	112
A.C. Test Conditions	113

List of Figures

Figure P-1	VG-230 Block Diagram	2
Figure P-2	System Block Diagram #1	3
Figure P-3	System Block Diagram #2	4
Figure 1-1	VG-230 Pin Assignment	5
Figure 2-1	VG-230 Memory Map	26
Figure 4-1	VG-230 Package Outline	100

List of Tables

Table 1-1	VG-230 Pin Descriptions	6
Table 1-2	System RAM Control Outputs	15
Table 2-1	Addressing Modes	17
Table 2-2	System Power Management Modes	20
Table 2-3	LCD Power Management Modes	21
Table 2-4	PC Card Power Management Modes	21
Table 2-5	Serial Port Power Management Modes	22
Table 2-6	Example of Supported LCDs	23
Table 2-7	VG-230 Memory Combination	24
Table 3-1	VG-230 I/O Map	29
Table 3-2	VG-230 Indexed Register Summary	39
Table 3-3	PMU Timer Registers	80

Product Overview

The Vadem VG-230 is a one-chip PC platform which provides a highly battery-efficient basis for OEMs to develop cost sensitive, DOS-based personal electronic products. The chip contains all standard XT peripherals, additional high-value peripherals and an ISA bus. For long battery life, the VG-230 offers extensive and proven power management capability. In addition to a +5V version, a version is offered which operates at +3V.

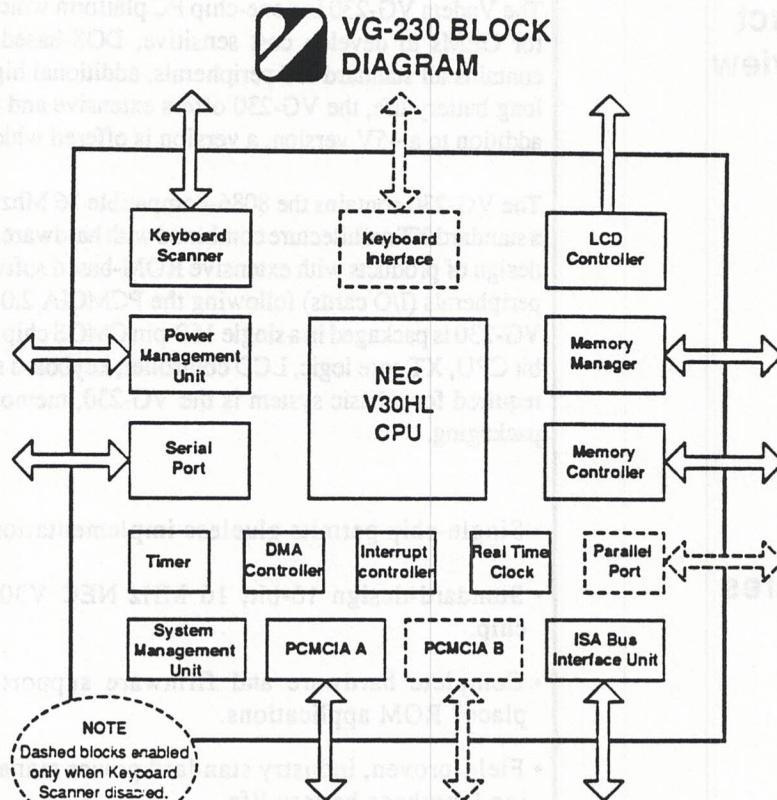
The VG-230 contains the 8086-compatible 16 MHz NEC V30HL processor. It also embodies a standard XT architecture combined with hardware and software features facilitating the rapid design of products with extensive ROM-based software. PC Card mass storage and miniature peripherals (I/O cards) following the PCMCIA 2.0 (JEIDA 4.1) standard are supported. The VG-230 is packaged in a single 160-pin CMOS chip and handles all PC functions including 16-bit CPU, XT core logic, LCD controller, keyboard scanner and PC Card controller. All that is required for a basic system is the VG-230, memory, power supply, display and associated packaging.

Key Features

- Single-chip permits glueless implementation of a fully compatible PC-XT.
- Standard-design 16-bit, 16 MHz NEC V30HL processor core integrated on-chip.
- Complete hardware and firmware support for memory-saving "execute-in-place" ROM applications.
- Field-proven, industry standard power management based on activity monitoring lengthens battery life.
- Scans up to 101 keys without an external keyboard controller.
- Integrated CGA LCD controller and 640x400 AT&T standard controller. Supports a wide variety of panel resolutions from below CGA to 400-line displays.
- LCD controller supports hardware "ink plane" for pen-based applications.
- Dual PCMCIA 2.0 (JEIDA 4.1) PC Card slot support allowing "hot" insertion/removal (with external buffers).
- Integrated serial port, real-time clock, programmable interrupt controller, DMA controller and internal timer.
- Deactivating keyboard scan enables a second PCMCIA card slot, a bi-directional parallel port and a standard XT keyboard interface.
- Support for DRAM, SRAM and PSRAM memory.
- Supports up to eight 8-bit RAM banks and up to six 16-bit RAM banks.
- ICE support simplifies debugging of system designs.
- Optionally combines with external VG-660 single-chip LCD VGA controller to drive 640x480 and lower resolution VGA compatible LCD panels.

**VADEM VG-230
SUB-NOTEBOOK
ENGINE**

**VG-230 Block Diagram
Figure P-1**



NOTE
Dashed blocks enabled
only when Keyboard
Scanner disabled.

VADEM VG-230

SUB-NOTEBOOK ENGINE

System Block Diagram
Figure P-2

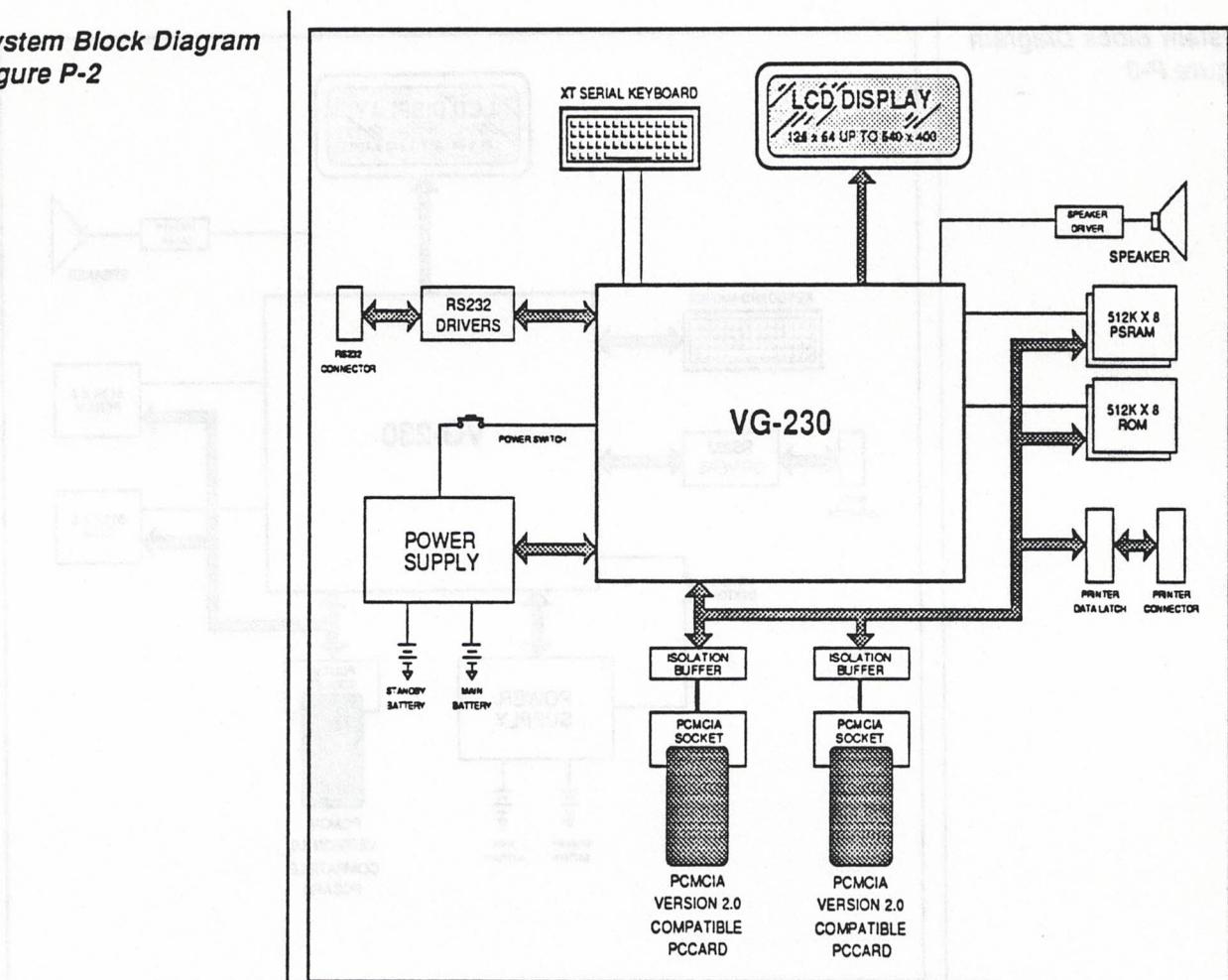


Figure P-2 depicts a pocket PC configuration. Dual PC cards provide mass storage for application programs and data. A standard parallel port and serial port provide notebook-type features. The keyboard is scanned by an external keyboard controller, which frees up pins for the parallel port and second PC card. The LCD controller supports panels from 128 x 128 to 640 x 400. This configuration would probably use a 640 x 200 panel. Two 512K x 8 PSRAMs provide system and internal RAM disk storage. 1M byte of ROM provides BIOS, ROMDOS, utility and application program storage.

VADEM VG-230

SUB-NOTEBOOK ENGINE

DES-05 MEDIACV
XCOESTOH-SU
BHDMS

System Block Diagram
Figure P-3

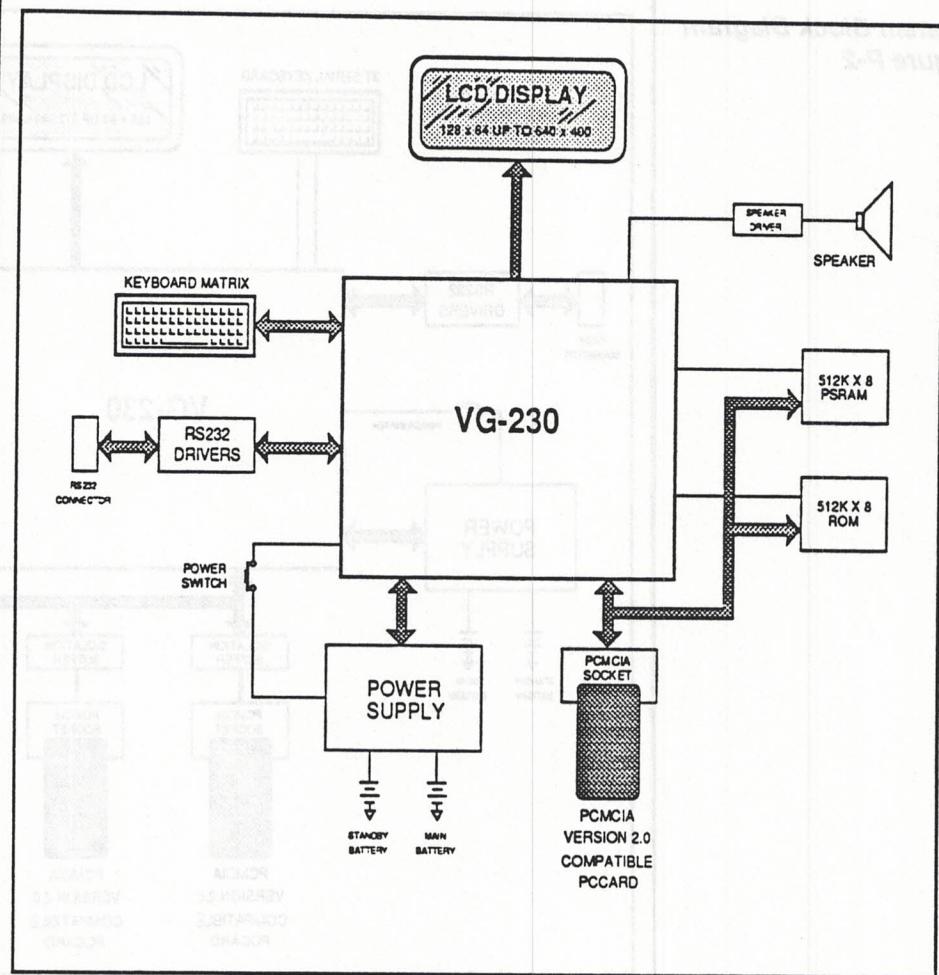


Figure P-3 depicts a minimal system configuration for a pocket organizer type product. A single PC card provides mass storage for applications and data. The internally scanned keyboard reduces parts count and power consumption. Although a full range of LCD panels are supported, a smaller display may be desirable for this type of product. A single chip provides 512K of PSRAM for system RAM and an internal RAM disk. A single 4M ROM chip provides 512K of BIOS, DOS and application storage.

VADEM VG-230

SUB-NOTEBOOK ENGINE

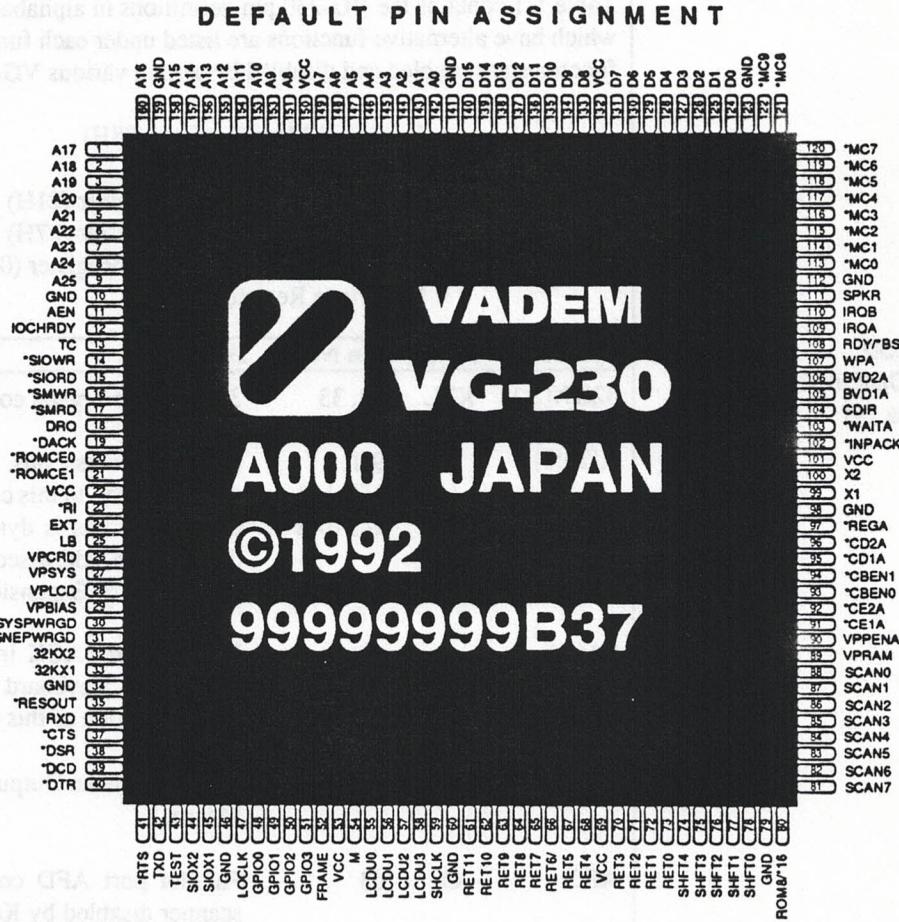
Chapter 1

Pin Assignment

VG-230 Pin

Assignment

Figure 1-1



ALTERNATIVE PIN DEFINITIONS

PIN #	DEFAULT	ALTERNATIVE(S)	PIN #	DEFAULT	ALTERNATIVE(S)
48	GPIO0	LCDL0, *DACK0	74	SHFT4	*CD1B
49	GPIO1	LCDL1, ALE	75	SHFT3	*CD2B
50	GPIO2	LCDL2, SYSCLK	76	SHFT2	BVD1B, *STSCHGB
51	GPIO3	LCDL3	77	SHFT1	BVD2B, *SPKRB
54	M	*DACK0	78	SHFT0	*INPACKB
61	RET11	PDOE	81	SCAN7	KBCLK
62	RET10	VPPENB	82	SCAN6	KBDAT, IRQ1
63	RET9	AFD	83	SCAN5	*CE1B
64	RET8	SLCT	84	SCAN4	*CE2B
65	RET7	*ERR	85	SCAN3	*REGB
66	RET6	SEL	86	SCAN2	PDCLKU, PDCLKB
67	RET5	PE	87	SCAN1	INIT
68	RET4	ACK	88	SCAN0	STB
70	RET3	BUSY	105	BVD1A	STSCHGA
71	RET2	*RDY/BSYA, IREQB	106	BVD2A	*SPKRA
72	RET1	WPB	107	WPA	*IOS16A
73	RETO	*WAITB	108	RDY/BSYA	*IREQA

NOTE: The VG-230 does not contain pull-up/pull-down resistors.
All unused inputs should be terminated.

VADEM VG-230

SUB-NOTEBOOK

ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Table 1-1 contains the VG-230 pin definitions in alphabetical order by pin name. Pins which have alternative functions are listed under each function's symbol. Alternative functions are enabled and disabled by setting various VG-230 registers. These are:

- Keyboard Mode Register (08H)
- GPIO Mode Register (32H)
- PC Card Slot 0 Control Register (21H)
- PC Card Slot 1 Control Register (27H)
- LCD Configuration Control Register (07H)
- PIO Mode Register (18H)

VG-230
Pin Descriptions
Table 1-1

Symbol	Type	Pin No.	Description
32KX[2:1]	XTL	32, 33	32.768 KHz crystal connection.
A[25:0]	O	9-1, 158-151, 149-142	System Address Bus. All external memory and I/O devices attach to this common address bus. The function of this bus is dynamically set according to the device type addressed: DRAM, SRAM, PC Card, ROM, I/O, or Expansion memory.
*ACK	I	68	Parallel port *ACK input (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET4.
AEN	O	11	Address Enable. Output from 8237A DMA Controller Macro.
AFD	O	63	Parallel port AFD control output (when keyboard scanner disabled by Keyboard Mode Register, 08H). AFD must be inverted using a 74XX05-type open collector device. The default definition of this pin is RET4.
ALE	O	49	Address Latch Enable signal (when enabled by GPIO Mode Register, 32H). Alternatively, LCDL1 for 400-line LCD panels may be enabled using this register. The default definition of this pin is GPIO1.
BUSY	I	70	Parallel port BUSY input (when the keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET3.
BVD[2:1]A	I	106, 105	Battery voltage status inputs for slot 'A' PC memory cards. May be re-defined for I/O cards to *SPKRA and STSCHGA respectively by the PC Card Slot 0 Control Register (21H).

VADEM VG-230

SUB-NOTEBOOK ENGINE

VG-230
Pin Descriptions
(cont.)
Table 1-1

Symbol	Type	Pin No.	Description
BVD[2:1]B	I	77, 76	Battery voltage status inputs for slot 'B' PC memory cards (when keyboard scanner disabled by Keyboard Mode Register, 08H). Pins [2:1] may be set to *SPKRB and STSCHGB respectively for I/O cards by using the PC Card Slot 1 Control Register (27H). The default definitions of these pins are SHFT[1:2] respectively.
*CBEN[1:0]	O	94, 93	Enable signal for PC Card Odd and Even Byte data buffers.
CDIR	O	104	Direction control for PC Card Odd and Even Byte data buffers.
*CD[2:1]A	I	96, 95	Card detect status inputs from slot 'A' PC Card.
*CD[2:1]B	I	75, 74	Card detect status inputs from slot 'B' PC Card (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definitions of these pins are SHFT[3:4] respectively.
*CE[2:1]A	O	92, 91	PC Card Even/Odd byte chip select signals for slot 'A'.
*CE[2:1]B	O	84, 83	PC Card Even/Odd byte chip select signals for slot 'B' (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definitions of these pins are SCAN[4:5] respectively.
*CTS	I	37	Serial Port clear to send.
D[15:0]	I/O	140-133, 131-124	Bi-directional System Data Bus. All external memory and I/O devices attach to this common data bus. 8 bit devices will reside on the D[7:0] half of the system data bus.
*DACK	O	19	DMA Acknowledge. Output from 8237A DMA Controller Macro. Selected from one of *DACK[3:1] depending upon which of DRQ[3:1] is programmed by user.
*DACK0	O	48	Internal *DACK0 signal REFRESH (when enabled by GPIO Mode Register, 32H). Alternatively, LCDL0 for 400-line LCD panels may be enabled by this register. The default definition of this pin is GPIO0.
*DACK0	O	54	Internal *DACK0 signal REFRESH (when LCD controller disabled by LCD Configuration Control Register, 07H). The default definition of this pin is M.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VG-230
SUB-NOTEBOOK
ENGINE

VG-230 Pin Descriptions (cont.)

Table 1-1

Symbol	Type	Pin No.	Description
*DCD	I	39	Serial Port data carrier detect.
DRQ	I	18	DMA Request. Input to 8237A DMA Controller Macro. User programmable to be one of DRQ[3:1].
*DSR	I	38	Serial Port data set ready.
*DTR	O	40	Serial Port data transmit ready.
*ERR	I	65	Parallel port *ERR input (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET7.
EXT	I	24	External switch input. To activate SUSPEND/RESUME.
FRAME	O	52	Frame clock to LCD.
GPIO[3:0]	I/O	51-48	General Purpose Input/Output signals. Data direction is set by the GPIO Mode Register (32H). This register also enables other definitions for these pins. See LCDL, SYSCLK, ALE and *DACK0 for further information.
INIT	O	87	Parallel port INIT control output (when keyboard scanner disabled by Keyboard Mode Register, 08H). This output must be inverted using a 74XX05 type open collector device. The default definition of this pin is SCAN1.
*INPACKA	I	102	Input acknowledge from slot 'A' PC I/O cards.
*INPACKB	I	78	Input acknowledge from slot 'B' PC I/O Cards (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is SHFT0.
IOCHRDY	I	12	I/O Channel Ready. Input OR'ed with internal ready sources to insert CPU wait states.
*IOIS16A	I	107	Register width status from slot 'A' PC I/O Cards. Enabled by the PC Card Slot 0 Control Register. The default definition of this pin is WPA.

VADEM VG-230

SUB-NOTEBOOK ENGINE

QCS-QV MEGAV
ROBERT CHIEN

VG-230
Pin Descriptions
(cont.)
Table 1-1

Symbol	Type	Pin No.	Description
*IOIS16B	I	72	Register width status from slot 'B' PC I/O Cards (when keyboard scanner disabled by Keyboard Mode Register, 08H and I/O mode enabled using PC Card Slot 1 Control Register, 27H). When the keyboard scanner is disabled, the default definition of this pin is WPB. When the scanner is enabled, the definition of this pin is RET1.
IRQ1	I/O	82	Interrupt signal from external keyboard controller (when reads from VG-230 keyboard registers disabled by Keyboard Mode Register, 08H). When reads are enabled, pin definitions SCAN6 (default) or KBDAT may be set by the Keyboard Mode Register.
IRQA, IRQB	I	109, 110	System interrupt request. Interrupt request inputs to internal 8259A Macro. User programmable to be one of IRQ[7:2].
KBCLK	I/O	81	External keyboard KBCLK input (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is SCAN7.
KBDAT	I/O	82	External keyboard KBDAT input (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is SCAN6.
LB	I	25	Low Battery warning input.
LCDL[3:0]	O	51-48	Display data for lower half of 400 line LCDs (when enabled by GPIO Mode Register, 32H). This register may also be used to select other definitions for these pins. See LCDL, SYSLCK, ALE, *DACK0 and GPIO (default) for further information.
LCDU[3:0]	O	58-55	Display data for 200-line LCDs or for the upper half of 400 line LCDs.
LOCLK	O	47	Load clock to LCD.
M	O	54	Low frequency clock to LCD. When the LCD controller is disabled by the LCD Configuration Control Register (07H), this pin becomes *DACK0.
*MC[9:0]	O	122-113	System RAM control. Outputs defined in Table 1-2.

VADEM VG-230
SUB-NOTEBOOK
ENGINE

VADEM VG-230
 SUB-NOTEBOOK
 ENGINE

VG-230
Pin Descriptions
 (cont.)

Table 1-1

Symbol	Type	Pin No.	Description
*PDCLKB	O	86	Active low bidirectional parallel port data clock (when keyboard scanner disabled by Keyboard Mode Register, 08H and bidirectional operation enabled by PIO Mode Register, 18H). Asserted during accesses to the Parallel Port Data Register. *PDCLKB must be qualified externally with *SIOWR using a 74XX32 'OR' gate to write data and with PDOE to control a 74XX244 to read data. The default definition of this pin is SCAN2.
PDCLKU	O	86	Unidirectional parallel port data clock (when keyboard scanner disabled by Keyboard Mode Register, 08H). Internally qualified with *SIOWR to drive directly the CLK pin of an external 74XX374 octal D F/F for latching printer data. When the PIO Mode Register (18H) enables bidirectional operation, this pin becomes *PDCLKB. The default definition of this pin is SCAN2.
PDOE	O	61	Parallel Port Output Enable (when keyboard scanner disabled by Keyboard Mode Register, 08H and bidirectional operation enabled by PIO Mode Register, 18H). The default definition of this pin is RET11.
PE	I	67	Parallel port PE input (when keyboard scanner disabled by Keyboard Mode Register, 08H and bidirectional operation enabled by PIO Mode Register, 18H). The default definition of this pin is RET5.
RDY/*BSYA	I	108	Ready/*Busy status input from slot 'A' PC memory cards. PC Card Slot 0 Control Register (21H) may be used to redefine this pin as *IREQA for I/O cards.
RDY/*BSYB	I	71	Ready/*Busy status input from slot 'B' PC Memory Card (when keyboard scanner disabled by Keyboard Mode Register, 08H). PC Card Slot 1 Control Register (27H) may be used to redefine this pin as *IREQB for I/O cards. The default definition of this pin is RET2.
*REGA	O	97	PC Card register select signal for slot 'A.'
*REGB	O	85	PC Card register select signal for slot 'B' (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is SCAN3.

VADEM VG-230

SUB-NOTEBOOK ENGINE

085-0V MEGAV
HOOTON-BUS
SWITCH

VG-230
Pin Descriptions
(cont.)
Table 1-1

Symbol	Type	Pin No.	Description
*RESOUT	O	35	Active low system RESET output.
RET[11:0]	I	61-68, 70-73	Return inputs from external key matrix. The Keyboard Mode Register (08H) also enables other definitions for these pins. See PDOE, VPPENB, AFD, SLCT, *ERR, SEL, PE, *ACK, BUSY, RDY/*BSYB, *IREQB, WPB, *IOIS16B and *WAITB for more information.
*RI	I	23	Serial Port ring indicator.
ROM8/*16	I	80	Strap pin option. Allowing selection of BIOS ROM width. When strapped low, BIOS ROM is 16 bits wide.
*ROMCE[1:0]	O	21, 20	ROM chip enable outputs. *ROMCE0 is always asserted for memory accesses to the BIOS ROM (address range F000:0-FFFF:F). Assertion of ROM chip enable outputs [1:0] for other address ranges may be specified using the VG-230's EMS addressing.
*RTS	O	41	Serial Port request to send.
RXD	I	36	Serial Port receive data.
SCAN[7:0]	I/O	81-88	Scan outputs for external key matrix. The Keyboard Mode Register (08H) also enables other definitions for these pins. See KBCLK, KBDAT, *CE[2:1]B, *REGB, PDCLKB, *PDCLKU, INIT and STB for more information.
SEL	I	66	Parallel port SEL input (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET6.
SHCLK	O	59	Shift clock to LCD.
SHFT[4:0]	I/O	74-78	Shift key return inputs from external key matrix. The Keyboard Mode Register (08H) also enables other definitions for these pins. See *CD[2:1]B, BVD[2:1]B, *STSCHGB, *SPKRB and *INPACKB for more information.
*SIORD	O	15	System I/O Read strobe. This output is used to inform external I/O devices to put their data onto the data bus. The VG-230 Sub-Notebook Engine may be programmed to inhibit this output during I/O read cycles to the VG-230 Sub-Notebook Engine internal devices.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VG-230
SUB-NOTEBOOK
ENGINE

VG-230
Pin Descriptions
(cont.)
Table 1-1

Symbol	Type	Pin No.	Description
*SIOWR	O	14	System I/O Write strobe. This output is used to inform external I/O devices that data is available on the data bus. The VG-230 Sub-Notebook Engine may be programmed to inhibit this output during I/O write cycles to the VG-230 Sub-Notebook Engine internal devices.
SIOX[2:1]	XTL	44, 45	Serial Port crystal input/output.
SLCT	O	64	Parallel port SLCT control output (when keyboard scanner disabled by Keyboard Mode Register, 08H). This output must be inverted using a 74XX05-type open collector device. The default definition of this pin is RET8.
*SMRD	O	17	System Memory Read strobe. This output is used to inform external memory devices to put their data on the data bus. *SMRD is not asserted during reads from system RAM or PC Cards.
*SMWR	O	16	System Memory Write strobe. This output is used to inform expansion memory devices that data is available on the data bus. *SMWR is not asserted during writes to system RAM or PC Cards.
SNEPWRGD	I	31	VG-230 Sub-Notebook Engine power good input. This pin should be driven low when power to the VG-230 falls below the recommended operating thresholds. SNEPWRGD is used to initialize the internal registers, peripherals, RTC, and microprocessor of the VG-230. It will also generate a system reset on the *RESETOUT output.
SPKR	O	111	Speaker data output. This output should be buffered and then input to a low pass filter. The output of the filter connects to a speaker.
*SPKRA	I	106	Speaker signal from slot 'A' PC I/O cards. Enabled by the PC Card Slot 0 Control Register (21H). The default definition of this pin is BVD2A.
*SPKRB	I	77	Speaker signal from slot 'B' PC I/O cards (when keyboard scanner disabled by Keyboard Mode Register, 08H, and I/O mode enabled by PC Card Slot 1 Control Register, 27H). When the keyboard scanner is disabled, the default definition of this pin is BVD2B. When the scanner is enabled, the definition of this pin is SHIFT1.

VADEM VG-230

SUB-NOTEBOOK ENGINE

GEIGER MEGAV
NOISE-ON-BUS
ENDS

VG-230
Pin Descriptions
(cont.)
Table 1-1

Symbol	Type	Pin No.	Description
STB	O	88	Parallel port STB control output (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is SCAN0.
*STSCHGA	I	105	Status changed signal from slot 'A' PC I/O cards. Enabled by the PC Card Slot 0 Control Register (21H). The default definition of this pin is BVD1A.
*STSCHGB	I	76	Status changed signal from slot 'B' PC I/O cards (when keyboard scanner disabled by Keyboard Mode Register, 08H, and I/O mode enabled using PC Card Slot 1 Control Register, 27H). When the keyboard scanner is disabled, the default definition of this pin is BVD1B. When the scanner is enabled, the definition of this pin is SHFT2.
SYSCLK	O	50	XT Bus Clock signal (when enabled by GPIO Mode Register, 32H). Alternatively, LCDL2 for 400-line LCD panels may be enabled by this register. The default definition of this pin is GPIO2.
SYSPWRGD	I	30	System Power Good input. This pin should be driven low when the system VCC falls below the recommended operating thresholds. SYSPWRGD is used to initialize the external system peripherals, via the *RESET-SOUT signal, and re-start the internal VG-230 Sub-Notebook Engine clocks.
TC	O	13	Terminal Count. Output from 8237A DMA Controller Macro.
TEST	I	43	Test Mode. (See VG-230 Technical Reference Manual)
TXD	O	42	Serial Port transmit data.
VPBIAS	O	29	BIAS power gate for LCD panel.
VPCRD	O	26	VCC power gate for PC Cards.
VPLCD	O	28	VCC power gate for LCD panel.
VPPENA	O	90	Program Voltage Enable for slot 'A' PC Card.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

VG-230

Pin Descriptions

(cont.)

Table 1-1

Symbol	Type	Pin No.	Description
VPPENB	O	62	Program Voltage Enable output to power source for slot 'B' PC Card (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET10.
VPRAM	O	89	VCC power gate for RAM array.
VPSYS	O	27	Main System power gate for system power supply.
*WAITA	I	103	Extend bus cycle for slot 'A' PC Cards.
*WAITB	I	73	Wait status input from slot 'B' PC Card (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET0.
WPA	I	107	Write protect input from slot 'A' PC memory cards. PC Card Slot 0 Control Register (21H) may be used to redefine this pin as *IOIS16A for I/O cards.
WPB	I	72	Write protect status input from slot 'B' PC memory Cards (when keyboard scanner disabled by Keyboard Mode Register, 08H). PC Card Slot 1 Control Register (27H) may be used to redefine this pin as *IOIS16B for I/O cards. The default definition of this pin is RET1.
X[2:1]	XTL	100, 99	Main clock crystal inputs. X1 is an input for a passive crystal circuit. X1 may be driven at either 32.215905 MHz or 28.63636 MHz. X2 is the inverted output of X1.
84	I	—	TEST
85	O	—	GXT
86	O	—	24SERV
87	O	—	ACREQ
88	O	—	ACMTV
89	O	—	ACOTV

VADEM VG-230

SUB-NOTEBOOK ENGINE

**System RAM
Control Outputs**
Table 1-2

Table 1-2 following lists system outputs for controlling RAM.

	DRAM		SRAM		PSRAM	
	8	16	8	16	8	16
*MC0	*CAS0	*CAS0	*CS0	*CS0	*CS0	*CS0
*MC1	*CAS1	*CAS1	*CS1	*CS1	*CS1	*CS1
*MC2	*CAS2	*CAS2	*CS2	*CS2	*CS2	*CS2
*MC3	*CAS3	*CAS3	*CS3	*CS3	*CS3	*CS3
*MC4	*CAS4	*CAS4	*CS4	*CS4	*CS4	*CS4 (*REFL)
*MC5	*CAS5	*RASL	*CS5	*CS5	*CS5	*CS5 (*REFH)
*MC6	*RASL	*RASH	*CS6	*OEL	*CS6	*OEL (*REFL)
*MC7	*RASH	*OE	*CS7	*OEH	*OEL	*OEH (*REFH)
*MC8	*OE	*WEL	*OE	*WEL	*OEH	*WEL (*OE)
*MC9	*WE	*WEH	*WE	*WEH	*WE	*WEH

Notes:

*RASH, *OEH, and *WEH are asserted during Odd Byte and Word accesses for 16 bit RAM arrays, or during accesses to Odd numbered banks (1,3,5 ...) for 8 bit RAM arrays. *RASL, *OEL, and *WEL are asserted during Even Byte and Word accesses for 16 bit RAM arrays, or during accesses to Even numbered banks (0,2,4...) for 8 bit RAM arrays.

The functions of MC[8:4] are defined differently depending upon the density of PSRAM interfaced to the VG-230 Sub-Notebook Engine. For 128Kx8 PSRAM arrays, *REFL drives the even addressed and *REFH the odd addressed PSRAM *REF pins (16 bit systems) or the even numbered (0,2,4...) and odd numbered (1,3,5...) PSRAM *REF pins (8 bit systems). For 32Kx8 and 512Kx8 PSRAM arrays, *OEH and *OEL replace *REFH and *REFL and function in the same manner.

For PC memory cards, MC8 is defined as *OE and MC9 as *WE.

Overview

This section describes the main functional blocks of the VG-230 Sub-Notebook Engine. The VG-230 is designed for easy development of cost-sensitive, battery operated products which contain substantial amounts of ROM-based software. In addition to the functional blocks which support basic XT compatibility, also provided are a matrix keyboard scanner, a CGA/AT&T LCD controller, a sophisticated memory manager which is programmed using a compatible superset of LIM 4.0 registers, PCMCIA 2.0 controllers, an industry-proven power management unit, a system management unit to aid in integration of non-standard peripherals, a serial port and a parallel port. Standard V30H ICE support for faster debugging is also integrated (See Figure P-1 for the block diagram).

Single-Bus Architecture

The VG-230 Sub-Notebook Engine embodies a Single Bus Architecture (pat. pend.). All external memory and I/O devices share the same address bus and data bus. A control bus is reserved for interfacing Expansion Memory and Expansion I/O devices. Expansion in this case means memory or I/O devices not directly controlled by the VG-230 Sub-Notebook Engine.

The Address Bus operates in 5 modes depending upon the device type accessed. Logic internal to the VG-230 Sub-Notebook Engine enables the appropriate addressing mechanism for the selected device. The addressing modes are in Table 2-1.

The Single Bus supports 8 or 16 bit memory, 8 bit I/O, 16 bit PC memory cards and 8 or 16 bit PC I/O cards. The data width of System RAM and System ROM are set by VG-230 Sub-Notebook Engine register bits and a configuration pin. When 8-bit system RAM or 8-bit system ROM configurations are selected, these devices are installed on the lower half of the data bus, D[7:0].

VG-230
Addressing Modes
Table 2-1

Device Type	Address Format	Address Type
System RAM		
DRAM	Multiplexed Row/Column	Mappable RAM Memory Address
SRAM/PSRAM	Latched	Mappable RAM Memory Address
System ROM0	Latched	Mappable ROM0 Memory Address
System ROM1	Latched	Mappable ROM1 Memory Address
PC Memory Card 1	Latched	Mappable PC Card1 Memory Address
PC Memory Card 2	Latched	Mappable PC Card2 Memory Address

VADEM VG-230

SUB-NOTEBOOK ENGINE

Processor

The VG-230 Sub-Notebook Engine is built around a standard, fully 8086-compatible NEC V30HL CPU macro. With its maximum clock rate of 16 MHz, the V30HL rivals all industry standard processors in speed. It is especially designed for low power consumption, and supports complete clock stoppage under power management. The V30HL is designed to operate over a range including +3V and +5V.

PC Card Controller

The VG-230 Sub-Notebook Engine PC Card Controller provides support for up to two PCMCIA 2.0 (JEIDA 4.1) card slots. Both I/O and memory cards are supported, as is the memory-saving XIP ("execute-in-place") standard. A single PC Card slot is always supported by the VG-230. A second PC Card slot is supported when the internal Keyboard Scanner is disabled.

Access to PC Card memory on the VG-230 uses a superset of LIM 4.0. Memory mapping for PC Cards follows the same approach as memory mapping for expanded memory and uses the same registers. This flexibility simplifies driver design, allowing generic routines to access any memory type. For I/O cards, an I/O window can be defined anywhere within the 64KB address space. I/O is not paged.

The PC Card Controller provides power management functions for PC Cards. When enabled by software, power may be automatically removed from the Cards after a programmable period of inactivity. Optionally, the PC Card Controller may generate an interrupt to inform the CPU that the PC Card is idle. Software may then remove power to the Card if desired. Power also can be removed from the Cards when the Power Management Unit (see Table 2-2) indicates SLEEP mode.

Besides generating an interrupt to inform the CPU of the PC Card's activity status, the PC Card Controller also may generate an interrupt (when enabled by software) for the following conditions:

- Low Battery warning from PC Card
- Battery Fail Alarm from PC Card
- Card Removal
- IREQ signal from I/O Cards
- Status changed signal (STSCHG) from I/O Cards

Each of the above sources is individually maskable by system software.

The PC Card Controller supports "hot" insertion and removal of PC Cards when external buffers are added.

Keyboard

The VG-230 Sub-Notebook Engine provides two types of Keyboard interfaces:

- Internal Keyboard Scanner to control switch matrix
- PC/XT serial keyboard interface to connect to a stand-alone PC/XT keyboard subsystem.

When the Keyboard Scanner is enabled, it supports an external key matrix composed of up to 101 keys. Of these keys, 96 are organized in an 8 x 12 matrix and 5 are dedicated shift keys. When the Keyboard Scanner is disabled, some of the pins it controls are assigned to

VADEM VG-230

SUB-NOTEBOOK ENGINE

080-0V MEDEV
XOCETON-BUS
AM313

System Management Unit

other internal functions. These functions are the Parallel Port, the PC/XT serial Keyboard interface, and control for a second PC Card Slot. The PC/XT Serial Keyboard Interface itself may also be disabled, allowing use of a separate keyboard controller. In this mode the KBDAT pin is defined as IRQ1.

The System Management Unit (SMU) of the VG-230 Sub-Notebook Engine helps solve certain system issues arising in super-portable PC compatibles. For example, power managing peripheral devices might require shutting them down. Using the SMU and appropriate firmware, a VG-230 based system can intercept application accesses to the shutdown device, reapply power, restore any lost set-up parameters, and only then restore control to the application, shielding it from the need to know the power state of the device. Another use might be to make a non-standard I/O device look to applications like a standard PC device. In this case, the SMU would intervene in I/O situations, invoking a firmware routine which would emulate the standard device's behavior in software.

In general, when software-enabled, the SMU monitors the CPU, looking for I/O activity on up to three selectable port ranges. When execution of an I/O instruction on a target range is imminent, the SMU hardware interrupts the CPU. After invoking system management functions written in standard 8086 code, it guarantees resumption of the interrupted routine at the proper point. In other words, the functioning of the system management firmware can be made completely invisible to user software.

Power Management Unit

The Power Management Unit (PMU) of the VG-230 Sub-Notebook Engine is based on the field-proven Vadem VG-647 (Intel™ 82347) notebook power management chip. It reduces overall system power consumption, lengthening battery life significantly. Several types of system activity are monitored and the appropriate power management mode (ON, DOZE, SLEEP, SUSPEND or OFF) is selected based on built-in criteria refined through the VG-647 experience. From ON to DOZE and then to SLEEP, the CPU clock may be slowed or stopped. In SUSPEND, power is removed from all functional system blocks except the VG-230 and system RAM. In OFF, only the VG-230 is powered.

When entering SUSPEND, software must set the CPUOSC divisor bits of the BCG Mode Register to select the slowest CPU clock frequency. It is important to note that following a hard reset or a RESUME from SUSPEND or OFF modes, the PMU registers are write protected. Software must read the PMU Supply Register at Index C1H to unlock these registers.

The PMU also manages power to the various peripherals. For example, control of the LCD power is shared between the PMU and the LCD Controller. The PMU performs activity monitoring and generates a Power On/Off signal to the LCD Controller. The LCD controller uses this signal to trigger LCD power sequencing.

The PMU also monitors the battery voltage status and produces a maskable interrupt on Low Battery.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

System Power Management

The VG-230 contains power management logic which controls five separate functional blocks; System, RAM, LCD, PC Card, and the Serial port.

This is the primary means of controlling power in the VG-230 and the overall system. System power management is composed of five basic power states; ON, DOZE, SLEEP, SUSPEND, and OFF. The table following indicates the different modes and their effect upon the system.

System Power Management Modes

Table 2-2

Mode	OSC	CPU Clock	I/O Pins	Memory I/F	Wakeup By
ON	On	Full Speed	Active	Active	--
DOZE	On	Stopped (Static mode) or Divided by 8 or 16 (Slow Clock mode)	Active	Active	Static mode: Interrupt or DMA Request or Slow clock mode: Interrupt, DMA Request, or programmed activity (See Note 2)
SLEEP	On	Stopped (Static mode) or Divided by 8 or 16 (Slow clock mode)	Active (See Note 1)	Active	Static mode: Interrupt or DMA Request or Slow clock mode: Interrupt, DMA Request, or programmed activity (See Note 2)
SUSPEND	Stopped	Stopped	Input pins inactive, Outputs driven Hi-Z	Active, providing automatic refresh	EXT or RI inputs, or internal RTC alarm
OFF	Stopped	Stopped	Input pins inactive, Outputs driven Hi-Z	Off, Driven Hi-Z	EXT or RI inputs, or internal RTC alarm

Note 1: During SLEEP mode, the behavior of the system control logic is the same as DOZE mode behavior. In SLEEP mode, however, functional blocks such as the PC Card and LCD may be automatically powered down on entering the mode.

Note 2: An interrupt or DMA request does not cause the VG-230 to exit the current power management mode. Instead, the CPU clock will temporarily return to full speed to service the interrupt or DMA cycle. Only programmed activity will force a return to the ON state.

VADEM VG-230

SUB-NOTEBOOK ENGINE

DCR-OV MEGAV
XOOBETOH-EUE
SMICHE

LCD Power Management

The LCD controller supports two power states: ON and SLEEP. The LCD SLEEP state may be triggered independently of the System power management control. An internal activity timer monitors keyboard activity and write operations to the video display buffer. When the programmable time-out expires, the LCD panel is automatically powered down. Alternatively, the LCD may be powered down when the system enters SLEEP mode. For proper system operation, software must power-down the LCD prior to entering SUSPEND mode. The table following indicates the two LCD power modes and their effect upon the system.

LCD Power Management
Table 2-3

Mode	LCD Clock	LCD	Display RAM	LCD I/F	Wakeup By
ON	Full Speed	On	Active	Active	-
SLEEP	Stopped	Off	Accessible by CPU but LCD Display is off	Driven Low	Keyboard Input or Write to Video Memory

PC Card Power Management

The PC Card controller also supports two power states; ON and SLEEP. The PC Card SLEEP state may be triggered independently of the System power management control. An internal activity timer monitors accesses to the PC Cards and may interrupt system software when the programmable time-out expires, or alternatively may automatically remove power to the PC Cards. The PC Card power management logic also allows PC Cards to be powered down when the system enters SLEEP mode. The table following indicates the two PC Card power modes and their effect upon the system.

PC Card Power Management Modes
Table 2-4

Mode	PC Card	PC Card I/F	Wakeup By
ON	On	Active	--
SLEEP	Off	Hi-Z	Software command

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Serial Port Power Management

The serial port provides power management in the form of both internal serial clock control and control of the serial port oscillator. Power reduction may be realized under normal operation by stopping the internal serial clock. Control of the serial clock oscillator must be controlled by software due to the latencies involved with restarting the oscillator. The Serial Port SLEEP State may be triggered independently of the System power management control. An internal activity timer monitors accesses to the serial port transmit buffer and/or serial inputs and may automatically stop the serial port clock. The table following indicates the three serial port power modes and their effect upon the system.

Serial Port Power Management Modes
Table 2-5

Mode	OSC	Serial Port Clock	Wakeup By
ON	On	Full Speed	--
SLEEP with oscillator enabled	On	Stopped	Write to Transmit Buffer and/or Activity on Serial Port inputs
SLEEP with oscillator disabled	Off	Stopped	Software command

WAKEUP BY	OSC	SC Cfg	SC Cmd Rq	WAKE
Activity	On	On	On	On

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

LCD Controller

The LCD Controller supports all CGA Text and Graphics display modes as well as AT&T 640x400 two-color graphics mode. AT&T "double-scanning" of 200 line graphics text and graphics is also supported. For lower-resolution panels, the controller provides hardware support for windowing into the CGA or AT&T frame. This allows software to utilize 200 or 400 line display modes regardless of panel size.

For 200 line panels or smaller, an Ink Plane feature useful for pen-based applications is supported. A separate 200 line buffer receives ink traces which are superimposed on the main display buffer. This feature is available when 200 line panels or smaller are used.

The LCD Controller supports a global enable/disable function. While disabled, all clocks within the LCD Controller are stopped to reduce power consumption, and the LCD Controller will not respond to either I/O or memory operations, except accesses to the LCD Configuration Control Register.

The LCD Controller uses main system memory. This provides very high video performance and eliminates the need for a separate display memory. The uppermost bank of RAM is used as the display buffer. CPU accesses to B800:0H are mapped by the VG-230 hardware to this bank.

VG-230 Examples of Supported LCDs

Table 2-6

Table 2-6 lists some of the LCDs that are supported by the VG-230 Sub-Notebook Engine. For unlisted panels or sizes, please contact Vadem.

640x400	Sharp Optrex Hitachi	LM6406F DMF666AN LMG6111XTFR
640x200	Casio Epson Hitachi Matsushita Sanyo	MD232TS01-00 TCMA9108 9043D LMG6273XNFR EDMDG648A 33D LCM5205
640x100	Hitachi	LM266XW
480x128	Toshiba	TLX1241
320x200	Epson	EG7500B-LS
320x240	Contact Vadem	Contact Vadem
240x128	Optrex Sharp	DFM66ON LM24009W, LM24010Z
240x64	Sharp Hitachi	LM24013W LM258XB
128x128	Optrex	DMF6116
128x64	Optrex	DFM697N

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM AG-230
SUB-NOTEBOOK
ENGINE

Memory Controller and Memory Manager

The VG-230 supports DRAM, SRAM, PSRAM, ROM and FLASH memory devices. Timing for accesses to memory is based on the processor clock, CPUCLK.

In general, memory device types and sizes cannot be mixed. FLASH banks, however, can be installed above SRAM or PSRAM banks as long as data width and device sizes are consistent. The memory controller automatically allocates memory from the uppermost RAM bank for LCD video memory functions.

Memory management hardware is provided which facilitates the use of large ROMs, PCMCIA 2.0 (JEIDA 4.1) compatible cards, and expanded memory. As a compatible superset of LIM 4.0, its command set is easy to support. The memory manager is also compatible with the PCMCIA 2.0 LIM XIP ("execute-in-place") specification for applications which execute directly out of ROM.

- Over and above base memory, five categories of memory are addressable.
 - Expanded memory (64MB address space).
 - Heavy-access ROM (highly power efficient, 1MB address space limitation).
 - Normal-access ROM (64MB address space).
 - PCMCIA 2.0 Card A (64MB address space).
 - PCMCIA 2.0 Card B (64MB address space).
- Addressing is paged, via 26 mapping registers.
 - Except for the non-mappable 32KB display memory (B800:0H-BFFF:FF), each 16KB "page" of the 1MB 8086 address space between 8000:0H and EFFF:FF is represented by its own mapping register.
 - Each mapping register includes a memory type specifier, which determine what memory category (expanded memory, heavy-access ROM, normal-access ROM, PC Card A or PC Card B) is being mapped to its page.
 - Mapping may be enabled/disabled globally, or on a page-by-page basis.
- Two ROM Chip Select outputs, *ROMCE0 and *ROMCE1, are available.
 - *ROMCE0 (heavy-access ROM) is always generated during BIOS ROM accesses (addresses F000:0H through FFFF:FF) and may also be generated during accesses to the ROM0 memory address space as specified in the Memory Mapping Registers.
 - *ROMCE1 (normal-access ROM) is an optional ROM Chip Select which may be used to implement ROM disks, ROMDOS, or embedded XIP applications.

VG-230 Memory Combinations
Table 2-7

RAM Package	32K		128K		256K		512K		1M		4M		Max # RAM Banks	
	8	16	8	16	8	16	8	16	8	16	8	16	8	16
Bit Width	---	---	---	---	1.5M	2.5M	3M	5M	6M	10M	24M	40M	8	16
DRAM	---	---	---	---	1.5M	2.5M	3M	5M	6M	10M	24M	40M	6	6
SRAM	256K	384K	1M	1.5M	---	--	4M	6M	---	---	---	---	8	6
PSRAM	224K	384K	768K	1M	---	---	3.5M	6M	---	---	---	---	7	6

VADEM VG-230

SUB-NOTEBOOK ENGINE

des av M3QAV
XOOBETOM-BUA
SMTDIA

Software may open a window into any of the five VG-230 memory categories using Memory Mapping Registers. Each Mapping Register controls a 16 Kbyte page in the 1MB memory address space which is directly addressed by the 8086-compatible V30 CPU (see diagram on next page). Memory Mapping Registers may also be disabled. In this case, the 16KB page controlled by the Register directly addresses the standard 1MB V30/8086 memory address space.

Each Memory Mapping Register pair is composed of 16 bits. Of these, 12 bits define the offset into the memory space and are used to generate the memory address on the A25 - A14 lines, 3 bits define which of the five memory spaces will be accessed, and 1 bit acts as a page map enable/disable.

Accessing the VG-230 Memory Mapping Registers involves three bytes in the CPU I/O address space. A particular Memory Mapping Register is accessed by first writing its CPU segment address into the Map Address Register at I/O address 06CH, and then reading from or writing to the Map Low Byte Data Register at I/O address 06EH or the Map High Byte Data Register at I/O address 06FH.

memory as defined
in I/O map 1AAR
is defined 2MB
total in (V30/8086)
area at 810

Map Address Register	Map Low Byte Data Register	Map High Byte Data Register
H00000	H00000	H00000
H00001	H00001	H00001
H00002	H00002	H00002
H00003	H00003	H00003
H00004	H00004	H00004
H00005	H00005	H00005
H00006	H00006	H00006
H00007	H00007	H00007
H00008	H00008	H00008
H00009	H00009	H00009
H0000A	H0000A	H0000A
H0000B	H0000B	H0000B
H0000C	H0000C	H0000C
H0000D	H0000D	H0000D
H0000E	H0000E	H0000E
H0000F	H0000F	H0000F
H00010	H00000	H00000
H00011	H00000	H00000
H00012	H00000	H00000
H00013	H00000	H00000
H00014	H00000	H00000
H00015	H00000	H00000
H00016	H00000	H00000
H00017	H00000	H00000
H00018	H00000	H00000
H00019	H00000	H00000
H0001A	H00000	H00000
H0001B	H00000	H00000
H0001C	H00000	H00000
H0001D	H00000	H00000
H0001E	H00000	H00000
H0001F	H00000	H00000
H00020	H00000	H00000
H00021	H00000	H00000
H00022	H00000	H00000
H00023	H00000	H00000
H00024	H00000	H00000
H00025	H00000	H00000
H00026	H00000	H00000
H00027	H00000	H00000
H00028	H00000	H00000
H00029	H00000	H00000
H0002A	H00000	H00000
H0002B	H00000	H00000
H0002C	H00000	H00000
H0002D	H00000	H00000
H0002E	H00000	H00000
H0002F	H00000	H00000
H00030	H00000	H00000
H00031	H00000	H00000
H00032	H00000	H00000
H00033	H00000	H00000
H00034	H00000	H00000
H00035	H00000	H00000
H00036	H00000	H00000
H00037	H00000	H00000
H00038	H00000	H00000
H00039	H00000	H00000
H0003A	H00000	H00000
H0003B	H00000	H00000
H0003C	H00000	H00000
H0003D	H00000	H00000
H0003E	H00000	H00000
H0003F	H00000	H00000
H00040	H00000	H00000
H00041	H00000	H00000
H00042	H00000	H00000
H00043	H00000	H00000
H00044	H00000	H00000
H00045	H00000	H00000
H00046	H00000	H00000
H00047	H00000	H00000
H00048	H00000	H00000
H00049	H00000	H00000
H0004A	H00000	H00000
H0004B	H00000	H00000
H0004C	H00000	H00000
H0004D	H00000	H00000
H0004E	H00000	H00000
H0004F	H00000	H00000
H00050	H00000	H00000
H00051	H00000	H00000
H00052	H00000	H00000
H00053	H00000	H00000
H00054	H00000	H00000
H00055	H00000	H00000
H00056	H00000	H00000
H00057	H00000	H00000
H00058	H00000	H00000
H00059	H00000	H00000
H0005A	H00000	H00000
H0005B	H00000	H00000
H0005C	H00000	H00000
H0005D	H00000	H00000
H0005E	H00000	H00000
H0005F	H00000	H00000
H00060	H00000	H00000
H00061	H00000	H00000
H00062	H00000	H00000
H00063	H00000	H00000
H00064	H00000	H00000
H00065	H00000	H00000
H00066	H00000	H00000
H00067	H00000	H00000
H00068	H00000	H00000
H00069	H00000	H00000
H0006A	H00000	H00000
H0006B	H00000	H00000
H0006C	H00000	H00000
H0006D	H00000	H00000
H0006E	H00000	H00000
H0006F	H00000	H00000
H00070	H00000	H00000
H00071	H00000	H00000
H00072	H00000	H00000
H00073	H00000	H00000
H00074	H00000	H00000
H00075	H00000	H00000
H00076	H00000	H00000
H00077	H00000	H00000
H00078	H00000	H00000
H00079	H00000	H00000
H0007A	H00000	H00000
H0007B	H00000	H00000
H0007C	H00000	H00000
H0007D	H00000	H00000
H0007E	H00000	H00000
H0007F	H00000	H00000
H00080	H00000	H00000
H00081	H00000	H00000
H00082	H00000	H00000
H00083	H00000	H00000
H00084	H00000	H00000
H00085	H00000	H00000
H00086	H00000	H00000
H00087	H00000	H00000
H00088	H00000	H00000
H00089	H00000	H00000
H0008A	H00000	H00000
H0008B	H00000	H00000
H0008C	H00000	H00000
H0008D	H00000	H00000
H0008E	H00000	H00000
H0008F	H00000	H00000
H00090	H00000	H00000
H00091	H00000	H00000
H00092	H00000	H00000
H00093	H00000	H00000
H00094	H00000	H00000
H00095	H00000	H00000
H00096	H00000	H00000
H00097	H00000	H00000
H00098	H00000	H00000
H00099	H00000	H00000
H0009A	H00000	H00000
H0009B	H00000	H00000
H0009C	H00000	H00000
H0009D	H00000	H00000
H0009E	H00000	H00000
H0009F	H00000	H00000
H0009A0	H00000	H00000
H0009A1	H00000	H00000
H0009A2	H00000	H00000
H0009A3	H00000	H00000
H0009A4	H00000	H00000
H0009A5	H00000	H00000
H0009A6	H00000	H00000
H0009A7	H00000	H00000
H0009A8	H00000	H00000
H0009A9	H00000	H00000
H0009AA	H00000	H00000
H0009AB	H00000	H00000
H0009AC	H00000	H00000
H0009AD	H00000	H00000
H0009AE	H00000	H00000
H0009AF	H00000	H00000
H0009A0	H00000	H00000
H0009A1	H00000	H00000
H0009A2	H00000	H00000
H0009A3	H00000	H00000
H0009A4	H00000	H00000
H0009A5	H00000	H00000
H0009A6	H00000	H00000
H0009A7	H00000	H00000
H0009A8	H00000	H00000
H0009A9	H00000	H00000
H0009AA	H00000	H00000
H0009AB	H00000	H00000
H0009AC	H00000	H00000
H0009AD	H00000	H00000
H0009AE	H00000	H00000
H0009AF	H00000	H00000
H0009A0	H00000	H00000
H0009A1	H00000	H00000
H0009A2	H00000	H00000
H0009A3	H00000	H00000
H0009A4	H00000	H00000
H0009A5	H00000	H00000
H0009A6	H00000	H00000
H0009A7	H00000	H00000
H0009A8	H00000	H00000
H0009A9	H00000	H00000
H0009AA	H00000	H00000
H0009AB	H00000	H00000
H0009AC	H00000	H00000
H0009AD	H00000	H00000
H0009AE	H00000	H00000
H0009AF	H00000	H00000
H0009A0	H00000	H00000
H0009A1	H00000	H00000
H0009A2	H00000	H00000
H0009A3	H00000	H00000
H0009A4	H00000	H00000
H0009A5	H00000	H00000
H0009A6	H00000	H00000
H0009A7	H00000	H00000
H0009A8	H00000	H00000
H0009A9	H00000	H00000
H0009AA	H00000	H00000
H0009AB	H00000	H00000
H0009AC	H00000	H00000
H0009AD	H00000	H00000
H0009AE	H00000	H00000
H0009AF	H00000	H00000
H0009A0	H00000	H00000
H0009A1	H00000	H00000
H0009A2	H00000	H00000
H0009A3	H00000	H00000
H0009A4	H00000	H00000
H0009A5	H00000	H00000
H0009A6	H00000	H00000
H0009A7	H00000	H00000
H0009A8	H00000	H00000
H0009A9	H00000	H00000
H0009AA	H00000	H00000
H0009AB	H00000	H00000
H0009AC	H00000	H00000
H0009AD	H00000	H00000
H0009AE	H00000	H00000
H0009AF	H00000	H00000
H0009A0	H00000	H00000
H0009A1	H00000	H00000
H0009A2	H00000	H00000
H0009A3	H00000	H00000
H0009A4	H00000	H00000
H0009A5	H00000	H00000
H0009A6	H00000	H00000
H0009A7	H00000	H00000
H0009A8	H00000	H00000
H0009A9	H00000	H00000
H0009AA	H00000	H00000
H0009AB	H00000	H00000
H0009AC	H00000	H00000
H0009AD	H00000	H00000
H0009AE	H00000	H00000
H0009AF	H00000	H00000
H0009A0	H00000	H00000
H0009A1	H00000	H00000
H0009A2	H00000	H00000
H0009A3	H00000	H00000
H0009A4	H00000	H00000
H0009A5	H00000	H00000
H0009A6	H00000	H00000
H0009A7	H00000	H00000
H0009A8	H00000	H00000
H0009A9	H00000	H00000
H0009AA	H00000	H00000
H0009AB	H00000	H00000
H0009AC	H00000	H00000
H0009AD	H00000	H00000
H0009AE	H00000	H00000
H0009AF	H00000	H00000
H0009A0	H00000	H00000
H0009A1	H00000	H00000
H0009A2	H00000	H00000
H0009A3	H00000	H00000
H0009A4	H00000	H00000
H0009A5	H00000	H00000
H0009A6	H00000	H00000
H0009A7	H00000	H00000
H0009A8	H00000	H00000
H0009A9	H00000	H00000
H0009AA	H00000	H00000
H0009AB	H00000	H00000
H0009AC	H00000	H00000
H0009AD	H00000	H00000
H0009AE	H00000	H00000
H0009AF	H00000	H00000
H0009A0	H00000	H00000
H0009A1	H00000	H00000
H0009A2	H00000	H00000
H0009A3	H00000	H00000
H0009A4	H00000	H00000
H0009A5	H00000	H00000
H0009A6	H00000	H00000
H0009A7	H00000	H00000
H0009A8	H00000	H00000
H0009A9	H00000	H00000
H0009AA	H00000	H00000
H0009AB	H00000	H00000
H0009AC	H00000	H00000
H0009AD	H00000	H00000
H0009AE	H00000	H00000
H0009AF	H00000	H00000
H0009A0	H00000	H00000
H0009A1	H00000	H00000
H0009A2	H00000	H00000
H0009A3	H00000	H00000
H0009A4	H00000	H00000
H0009A5	H00000	H00000
H0009A6	H00000	H00000
H0009A7	H00000	H00

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM AG-230
SUB-NOTEBOOK
ENGINE

VG-230

Memory Map

Figure 2-1

FFFF:FH	ROM BIOS
F000:0H	
EFFF:FH	Mapping Registers 23-26
E000:0H	
DFFF:FH	Mapping Registers 19-22
D000:0H	
CFFF:FH	Mapping Registers 15-18
C000:0H	
BFFF:FH	CGA Buffer
B800:0H	
B7FF:FH	Mapping Registers 13-14
B000:0H	
AFFF:FH	Mapping Registers 9-12
A000:0H	
9FFF:FH	Mapping Registers 5-8
9000:0H	
8FFF:FH	Mapping Registers 1-4
8000:0H	
7FFF:FH	
	Reserved for System RAM
0000:0H	

Defined as system
RAM when Global
EMS enable bit
(MAPEN) at index
04H is zero.

VADEM VG-230

SUB-NOTEBOOK ENGINE

Basic Peripherals and Core Logic

The VG-230 Sub-Notebook Engine contains the following PC Core logic and other peripherals:

- Serial Port
- Parallel Port
- Real Time Clock (RTC)
- Standard PC Core logic peripherals
- DMA Controller
- Interrupt Controller
- Timer
- Keyboard Interface

Serial Port

The Serial Port is based upon the 8250 UART. Software may configure the SIO Port to appear at either COM1 or COM2. Alternatively, the Serial Port may be disabled.

Parallel Port

The Parallel Port is PC/XT compatible and is only enabled when the Keyboard Scanner is disabled. An external 74XX374 is required for latching parallel data. The parallel port is also software configurable to appear at LPT1, LPT2 or LPT3 and supports the standard PC/XT PIO interrupt (IRQ7). Optionally, the parallel port may be configured for full 8 bit bidirectional capability with the addition of external components.

The Parallel Port may be similarly configured to appear at a non-standard I/O address. This allows use of the port's pins by dedicated applications for general purpose input and general purpose output (GPI and GPO).

Real Time Clock

The VG-230 Sub-Notebook Engine's Real Time Clock (RTC), besides timekeeping, provides 64 bytes of CMOS RAM to store system set-up information.

DMA Controller

An 8237A PC/XT compatible DMA Controller is included. One DMA channel is provided for the external system bus. System software may configure this channel to be one of DRQ/*DACK1, DRQ/*DACK2 or DRQ/*DACK3. Channel 0 (DRQ/*DACK0) of the DMA controller is reserved by the VG-230. When setting up refresh, Port 42H of the 8254 timer must be initialized before refresh will begin.

Interrupt Controller

The Interrupt Controller is PC/XT compatible and based upon the 8259 PIC. The VG-230 provides two external interrupt request inputs, IRQA and IRQB. System software may assign each of these lines to any of IRQ2 through IRQ7 using the ICU Mode Register (0DH).

The remaining interrupt lines are inputs internally assigned as follows:

- IRQ0 System Timer Interrupt
- IRQ1 Keyboard
- IRQ2 RTC Alarm
- IRQ3 SIO programmed to appear at 2F8H-2FFH
- IRQ4 SIO programmed to appear at 3F8H-3FFH
- IRQ7 Parallel Port

**VADEM VG-230
SUB-NOTEBOOK
ENGINE**

Timer

The VG-230 Sub-Notebook Engine's Timer is based on the PC/XT compatible 8254. The Timer clock is generated by dividing the clock source to produce a 1.19318 MHz TCLK.

Channel 0	Reserved for System Timer (18 Hz periodic interrupt)
Channel 1	Reserved for Memory Refresh (DRQ0 generation)
Channel 2	Controls the System Speaker

Clocks

The VG-230 Sub-Notebook Engine requires three clock sources:

Main clock 32.215905 MHz or 28.63636 MHz

SIO clock via DMA to COM to I/O

Power Management Unit/

RTC clock 32.768 KHz

The Main clock generates the processor clock (CPUCLK), the LCD Controller's clock (VIDCLK) and the Timer clock (TCLK). The RTC and PMU share the same time base, which is the only oscillator running when the VG-230 Sub-Notebook Engine is in the SUSPEND or OFF Power Management modes.

ICE Support

The VG-230 supports standard in-circuit emulation to simplify debugging of system motherboards. Any available ICE which is compatible with the VEC V30HL may be used. An ICE adaptor board (Vadem part no. VG-230-ICE) connects between the system motherboard and the ICE. This arrangement brings out the local V-30 processor bus to the ICE without changing the standard VG-230 pinout or functionality.

General Purpose I/O

The VG-230 provides four general purpose I/O bits for user defined functions. These GPIO pins are available when 200 line or lower LCD panels are used.

Also, the Parallel Port (available when the VG-230's internal keyboard scanner is disabled) may be configured to appear at a non-standard address. This allows use of the port's pins by dedicated applications for general purpose input and general purpose output (GPI and GPO).

Overview

IBM compatible registers and peripherals are located at the standard addresses. Internal registers specific to the VG-230 Sub-Notebook Engine are accessed via an Index Register located at 026H, and are read or written through a Data Register located at 027H.

VG-230 I/O Map
Table 3-1

Register / Peripheral	I/O Address
8237 DMA Controller	000H - 00FH
8259 Interrupt Controller	020H - 021H
VG-230 Sub-Notebook Engine Index Register	026H
VG-230 Sub-Notebook Engine Data Register	027H
8254 Timer	040H - 043H
XT PPIA Keyboard Data	060H
XT PPIB Keyboard Control	061H
XT PPIC System Status	062H
Memory Map Address Register	06CH
Memory Map Data Registers	06EH - 06FH
DMA Page Registers	081H - 083H
XT NMI Mask Register	0AOH
	Data
Parallel Port Data, Status and Control Registers	170H 278H 378H 3BCH
	171H 279H 379H 3BDH
	172H 27AH 37AH 3BEH
Serial Port	2F8H - 2FFH 3F8H - 3FFH
CGA LCD Controller	3D0H - 3DFH

VADEM VG-230

SUB-NOTEBOOK ENGINE

VG-230 Register Summary

Name: **PC/XT Compatible DMA Controller Registers**
Type: Read/Write
Address: 000H-00FH

Bit	Name	Default	Function
D[7:0]			(See 8237 Data sheet for descriptions of register bits)

Name: **PC/XT Compatible Interrupt Controller Registers**
Type: Read/Write
Address: 020H-021H

Bit	Name	Default	Function
D[7:0]			(See 8259 Data sheet for descriptions of register bits)

Name: **Index Register**
Type: Read/Write
Address: 026H

Bit	Name	Default	Function
D[7:0]	DA[7:0]	00H	Data register address bits

Name: **Data Register**
Type: Read/Write
Address: 027H

Bit	Name	Default	Function
D[7:0]	DD[7:0]		Data read from or written to register addressed by VG-230 Sub-Notebook Index Register

VADEM VG-230

SUB-NOTEBOOK ENGINE

OS-8V MEDEV
SUB-NOTEBOOK
ENGINE

Name: PC/XT Compatible Timer/Counter Registers
Type: Read/Write
Address: 040H-043H

Bit	Name	Default	Function
D[7:0]			(See 8237 Data sheet for descriptions of register bits)

Note: When initializing the 8254 timer following a hard reset, channel 2 must be initialized before channel 0 (Timer Interrupt) or channel 1 (Memory Refresh) will operate.

Name: PC/XT Compatible PPIA Keyboard Data Register
Type: Read/Write
Address: 060H

Bit	Name	Default	Function
D[7:0]	KSC[7:0]	00H	Keyboard Scan Code Normally, the PC/XT keyboard data register is read only. This register is written by the BIOS with the translated keyboard scan code when the Keyboard Controller is programmed into the keyboard scan mode. When the *KBDENA bit of the Keyboard Mode Register is set high, this register is disabled. In this configuration, accesses to this register will be directed to the external bus D[15:0].

8254 Channel 0 Address	0	ENQ#	SG
8254 Channel 1 Address	0	TACNTR	TC
8254 Channel 2 Address	0	ETACNT	TC

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: PC/XT Compatible PPIB Keyboard Control Register
 Type: Read/Write
 Address: 061H

Bit	Name	Default	Function
D7	RSTKBD	0	0 - Enable Keyboard 1 - Clear Keyboard Data Port and IRQ1
D6	KCLKEN	0	0 - Force Keyboard Clock Low 1 - Enable Keyboard Clock
<p>KCLKEN is pulsed low by software to request that the keyboard perform diagnostics. In the keyboard scan mode, KCLKEN may be used to generate an NMI. Following a write to the PPIB port with the KCLKEN bit reset low, an NMI will be generated on the next write to the PPIB port with the KCLKEN bit set high. At this time the BIOS will perform a keyboard scan operation and return the results to the PPIA port.</p>			
D5	*IOCEN	0	0 - Enable I/O Channel Parity 1 - Disable I/O Channel Parity
D4	*PAREN	0	1 - Disable RAM Parity
D3	HISWS	0	0 - Enable System Switches SW1 - SW4 1 - Enable System Switches SW5 - SW8
D2	Spare	0	Spare Read/Write bit
D1	SPKDAT	0	0 - Disable Speaker Output 1 - Enable Speaker Output
D0	TGATE	0	0 - Disable Timer Channel 2 1 - Enable Timer Channel 2

VADEM VG-230
SUB-NOTEBOOK
ENGINE

0CS-0V M30AV
 KDOBETOH-BUZ
 EMDNA

Name: PC/XT Compatible PPIC System Status Register
 Type: Read Only
 Address: 062H

Bit	Name	Default	Function
D7	PARERR	0	Onboard Parity Status (Forced low to indicate NO RAM Parity Errors)
D6	IOERR	0	I/O Channel Parity Status (Forced low to indicate NO I/O Channel Parity Errors)
D5	TOUT2	X	State of 8254 TOUT2 (Speaker Clock)
D4	*SPKR	1	Inverted state of the SPKR output pin 0 - Speaker is ON 1 - Speaker is OFF
D3	SW4_8	1	SW4 - RAM Size High (Hardwired High) SW8 - Drive Count High (Set by bit in Keyboard Mode Register)
D2	SW3_7	1	SW3 - RAM Size Low (Hardwired High) SW7 - Drive Count Low (Set by bit in Keyboard Mode Register)
D1	SW2_6	0	SW2 - Coprocessor Installed (Hardwired Low) SW6 - Display High (Set by bit in Keyboard Mode Register)
D0	SW1_5	1	SW1 - Loop on POST (Hardwired High) SW5 - Display Low (Set by bit in Keyboard Mode Register)

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: Map Address Register

Type: Read/Write

Address: 06CH

Bit	Name	Default	Function
D[7:2]	PA[7:2]	00H	Page address of the Mapping register to access through the Map Data registers. Valid entries are: 80, 84, 88, & 8C 90, 94, 98, & 9C A0, A4, A8, & AC B0 & B4 C0, C4, C8, & CC D0, D4, D8, & DC E0, E4, E8, & EC
D[1:0]	N/U	0	Not used. Ignored when written and zero when read.

Name: Map Low Byte Data Register

Type: Read/Write

Address: 06EH

Bit	Name	Default	Function
D[7:0]	MAP[21:14]	00H	Least significant byte of the memory map address

VADEM VG-230

SUB-NOTEBOOK ENGINE

OSR OV MEGAV
1000MHz-800
MHz

Name: Map High Byte Data Register
 Type: Read/Write
 Address: 06FH

Bit	Name	Default	Function			Page Memory Device Type
D7	PEN	0	0 - Disable mapping for this page 1 - Enable mapping for this page			
D[6:4]	DTYP[2:0]	000	DTYP2	DTYP1	DTYP0	None (external bus cycle)
			0	0	0	
			0	0	1	
			0	1	0	
			0	1	1	
			1	0	0	
			1	0	1	
			1	1	0	
			1	1	1	
D[3:0]	MAP[25:22]	0H	Most significant nibble of memory map address			

Name: PC/XT Compatible DMA Page Registers
 Type: Read/Write
 Address: 081H-083H

Bit	Name	Default	Function
D[7:4]	N/U	0H	Not Used
D[3:0]	A[19:16]	0H	DMA memory page address. I/O port address as follows: Channel 1: 083H Channel 2: 081H Channel 3: 082H

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: PC/XT Compatible NMI Mask Register
 Type: Read/Write
 Address: 0A0H

Bit	Name	Default	Function
D7	NMIENA	0	0 - Disable NMIs 1 - Enable NMIs
D[6:0]	N/U	00H	Not Used

Name: PC/XT Compatible Parallel Port Data Register
 Type: Read/Write
 Address: 170H, 278H, 378H, or 3BCH
 (Depending on setting of PPSEL bits of PIO Mode Register & KBDMODE bit of Keyboard Mode Register)

Bit	Name	Default	Function
D[7:0]	PD[7:0]	00H	<p>Parallel Data. In uni-directional mode, during reads from the Parallel Port Data Register, data is sourced from the PD[7:0] bits. During writes, data is captured in both this register and an external octal "D" type F/F controlled by the PDCLK pin.</p> <p>In bi-directional mode, the BIDIR bit of the PIO mode register is set high. The PPDIR bit of the Parallel Port Control Register determines the source of the data read from this port. When the PPDIR bit is low, data is read from the internal source. When PPDIR is high, the external parallel port data is read.</p>

VADEM VG-230

SUB-NOTEBOOK ENGINE

OSD BY MEDAV
SUB-NOTEBOOK
ENGINE

Name: PC/XT Compatible Parallel Port Status Register
 Type: Read Only
 Address: 171H, 279H, 379H, or 3BDH
 (Depending on setting of PPSEL bits of PIO Mode Register & KBDMODE bit of Keyboard Mode Register)

Bit	Name	Default	Function
D7	*BUSY	X	Inverted state of the BUSY input pin.
D6	*ACK	X	Driven directly from the *ACK input pin
D5	PE	X	Driven directly from the PE input pin.
D4	SEL	X	Driven directly from the SEL input pin.
D3	*ERROR	X	Driven directly from the *ERR input pin.
D2	IRQSTA	0	Interrupt Status. 1 - PIO Interrupt Pending
D[1:0]	N/U	00	Not Used. Always read back Low.

Line 12#	0	171H	101
Line 13#	0	279H	101
Line 14#	0	379H	101
Line 15#	0	3BDH	101

Address	Function	Value	Hex
171H	Parallel Port Status Register	00000000	00H

VADEM VG-230
SUB-NOTEBOOK
ENGINE

VADEM VG-230
 SUB-NOTEBOOK
 ENGINE

Name: PC/XT Compatible Parallel Port Control Register
 Type: Read/Write
 Address: 172H, 27AH, 37AH, or 3BEH
 (Depending on setting of PPSEL bits of PIO Mode Register & KBDMODE bit of Keyboard Mode Register)

Bit	Name	Default	Function
D[7:6]	N/U	000	Not Used. Ignored when written and Zero when read.
D5	PPDIR	0	Parallel Port direction control. When the BIDIR bit of the PIO Mode register is set high, the parallel port is configured for bi-directional operation and this bit is used to externally control the OE of the printer data latch and read-back path as follows: 0 - Write data to external parallel I/O device. (PDOE output driven low) 1 - Read data from external parallel I/O device. (PDOE output driven high) This bit is a don't care when the BIDIR bit is reset low.
D4	IRQENA	0	PIO Interrupt Enable. 1 - Enabled 0 - Disabled
D3	SELECT	0	Inverted and drives *SLCT output pin.
D2	*INIT	0	Directly drives *INIT output pin.
D1	AUTOFD	0	Inverted and drives *AFD output pin.
D0	STROBE	0	Inverted and drives *STB output pin.

Name: 8250 Serial Port Registers
 Type: Read/Write
 Address: 2F8H - 2FFH or 3F8H - 3FFH
 (Depending on setting of SPSEL bit of SIO Mode Register)

Bit	Name	Default	Function
D[7:0]			See 8250 Data Sheet for register definitions.

VADEM VG-230

SUB-NOTEBOOK ENGINE

OSG-3V MEGAV
NOOBESTON-SUB
ENGINE

**VG-230 Indexed
Register Summary**
Table 3-2

Following is the list of indexed registers specific to the VG-230 Sub-Notebook Engine:

REGISTER	INDEX
Revision Register	00H
Bus Cycle Generator Mode Register	01H
Bus Cycle Generator Wait State Control 1 Register	02H
Bus Cycle Generator Wait State Control 2 Register	03H
Memory Control 1 Register	04H
Memory Control 2 Register	05H
Alt. Display Buffer Start Address Register	06H
LCD Configuration Control Register	07H*
Keyboard Mode Register	08H
Keyboard Scan Control Register	09H
Keyboard Return Status Low Register	0AH
Keyboard Return Status High Register	0BH
Keyboard Shift and NMI Status Register	0CH
ICU Mode Register	0DH
DMA Mode Register	0EH
SIO Mode Register	10H
SIO Power Control Register	11H
Timer Mode Register	13H
PIO Mode Register	18H
Main NMI Status Register	19H
Port 1 NMI Trap Address Low Register	1AH
Port 1 NMI Trap Address High Register	1BH
Port 2 NMI Trap Address Low Register	1CH
Port 2 NMI Trap Address High Register	1DH
Port 3 NMI Trap Address Low Register	1EH
Port 3 NMI Trap Address High Register	1FH
PC Card Controller Mode Register	20H
PC Card Slot 0 Control Register	21H
PC Card Slot 0 Status Register	22H
PC Card Slot 0 Interrupt Mask Register	23H
PC Card Slot 0 I/O High Address Register	24H
PC Card Slot 0 I/O Low Address Register	25H
PC Card Slot 0 I/O Address Range Register	26H
PC Card Slot 1 Control Register	27H
PC Card Slot 1 Status Register	28H
PC Card Slot 1 Interrupt Mask Register	29H
PC Card Slot 1 I/O High Address Register	2AH
PC Card Slot 1 I/O Low Address Register	2BH
PC Card Slot 1 I/O Address Range Register	2CH
PC Card Power Control Register	2DH
PC Card Activity Timer Register	2EH
Reserved	2FH

*Note: Additional indexed registers have been added to the "6845" in the CGA space to support LCD operation.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

REGISTER	INDEX
BIOS Time Base Low Register	30H
BIOS Time Base High Register	31H
GPIO Mode Register	32H
GPIO Control Register	33H
Reserved	34H - 6FH
Top of Memory Register	38H
ICU Shadow Register	40H
RTC Seconds Register	70H
RTC Minutes Register	71H
RTC Hours Register	72H
RTC Day Low Register	73H
RTC Day High Register	74H
RTC Alarm Seconds Register	75H
RTC Alarm Minutes Register	76H
RTC Alarm Hours Register	77H
RTC Alarm Day Register	78H
RTC Mode Register	79H
RTC Status Register	7AH
Reserved	7BH - 7FH
RTC CMOS RAM	80H - BFH
PMU Status Register	C0H
PMU Supply Register	C1H
PMU Control Register	C2H
PMU Activity Mask Register	C3H
PMU NMI Mask Register	C4H
PMU I/O Range Register	C5H
PMU Power On Register	C6H
PMU Power Doze Register	C7H
PMU Power Sleep Register	C8H
PMU Power Suspend Register	C9H
PMU Polarity Register	CAH
PMU Output Register	CBH
PMU Doze Timer Register	CCH
PMU Sleep Timer Register	CDH
PMU Suspend Timer Register	CEH
PMU LCD Timer Register	CFH
LCD Sequence Register	D4H
PMU Resume Status	DAH
PMU Activity Status Register	DBH
Reserved	DCH - FFH

* Note: Addressed registers have been defined to the CCA
before to support LCD operation.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: **Revision Register**
Type: **Read Only**
Index: **00H**

Bit	Name	Default	Function
D[7:0]	REVD[7:0]		VG-230 Sub-Notebook Engine Silicon Revision Number

CGCCLK15	0	0	CGCCLK15	0	CGCCLK15	0
CGCCLK14	0	0	CGCCLK14	0	CGCCLK14	0
CGCCLK13	0	0	CGCCLK13	0	CGCCLK13	0
CGCCLK12	0	0	CGCCLK12	0	CGCCLK12	0
CGCCLK11	0	0	CGCCLK11	0	CGCCLK11	0
CGCCLK10	0	0	CGCCLK10	0	CGCCLK10	0
CGCCLK9	0	0	CGCCLK9	0	CGCCLK9	0
CGCCLK8	0	0	CGCCLK8	0	CGCCLK8	0
CGCCLK7	0	0	CGCCLK7	0	CGCCLK7	0
CGCCLK6	0	0	CGCCLK6	0	CGCCLK6	0
CGCCLK5	0	0	CGCCLK5	0	CGCCLK5	0
CGCCLK4	0	0	CGCCLK4	0	CGCCLK4	0
CGCCLK3	0	0	CGCCLK3	0	CGCCLK3	0
CGCCLK2	0	0	CGCCLK2	0	CGCCLK2	0
CGCCLK1	0	0	CGCCLK1	0	CGCCLK1	0
CGCCLK0	0	0	CGCCLK0	0	CGCCLK0	0

CGCCLK15	0	0	CGCCLK15	0	CGCCLK15	0
CGCCLK14	0	0	CGCCLK14	0	CGCCLK14	0
CGCCLK13	0	0	CGCCLK13	0	CGCCLK13	0
CGCCLK12	0	0	CGCCLK12	0	CGCCLK12	0
CGCCLK11	0	0	CGCCLK11	0	CGCCLK11	0
CGCCLK10	0	0	CGCCLK10	0	CGCCLK10	0
CGCCLK9	0	0	CGCCLK9	0	CGCCLK9	0
CGCCLK8	0	0	CGCCLK8	0	CGCCLK8	0
CGCCLK7	0	0	CGCCLK7	0	CGCCLK7	0
CGCCLK6	0	0	CGCCLK6	0	CGCCLK6	0
CGCCLK5	0	0	CGCCLK5	0	CGCCLK5	0
CGCCLK4	0	0	CGCCLK4	0	CGCCLK4	0
CGCCLK3	0	0	CGCCLK3	0	CGCCLK3	0
CGCCLK2	0	0	CGCCLK2	0	CGCCLK2	0
CGCCLK1	0	0	CGCCLK1	0	CGCCLK1	0
CGCCLK0	0	0	CGCCLK0	0	CGCCLK0	0

VADEM VG-230
SUB-NOTEBOOK
ENGINE

VADEM VG-230
 Sub-Notebook
 Engine

Name: Bus Cycle Generator Mode Register
 Type: Read/Write
 Index: 01H

Bit	Name	Default	Function			
D[7:5]	CDIV[2:0]	010	CDIV2	CDIV1	CDIV0	CPUCLK Divisor
			0	0	0	CPUOSC /2
			0	0	1	CPUOSC /3
			0	1	0	CPUOSC /4
			0	1	1	CPUOSC /6
			1	0	0	CPUOSC /8
			1	0	1	Reserved
			1	1	0	Reserved
			1	1	1	Reserved
D4	CLK14/*16	0	0 - Max. CPUCLK frequency = 16 Mhz (32Mhz input clock) 1 - Max. CPUCLK frequency = 14.3 Mhz (28.6 Mhz input clock)			
D3	LTCHADR	0	0 - Disable A[25:0] latches A[25:0] valid for all CPU cycles 1 - Enable A[25:0] latches A[25:11] invalid for DRAM cycles and A[25:20] only valid for PC Card or ROM1 cycles.			
D2	BINH	0	0 - Enable external bus for all bus cycles 1 - Disable external bus during accesses to internal devices			
D[1:0]	SDIV[1:0]	10	SDIV1	SDIV0	SYSCLK Divisor	
			0	0	CPUCLK /4	
			0	1	CPUCLK /3	
			1	0	CPUCLK /2	
			1	1	CPUCLK	

VADEM VG-230
SUB-NOTEBOOK
ENGINE

02H-BV MEGAV
 SUB-NOTEBOOK ENGINE

Name: **Bus Cycle Generator Wait State Control 1 Register**
 Type: **Read/Write**
 Index: **02H**

Bit	Name	Default	Function		
D[7:6]	ROMW[1:0]	11	ROMW1	ROMW0	ROM Wait States
			0	0	0 CPUCLK Wait States
			0	1	1 CPUCLK Wait States
			1	0	2 CPUCLK Wait States
D[5:4]	RAMW[1:0]	01	RAMW1	RAMW0	RAM Wait States
			0	0	0 CPUCLK Wait States
			0	1	1 CPUCLK Wait States
			1	0	2 CPUCLK Wait States
			1	1	3 CPUCLK Wait States
D[3:2]	IOW[1:0]	01	IOW1	IOW0	I/O Wait States
			0	0	0 SYSCLK Wait States
			0	1	1 SYSCLK Wait States
			1	0	2 SYSCLK Wait States
			1	1	3 SYSCLK Wait States
D[1:0]	EXMW[1:0]	00	EXMW1	EXMW0	Expansion Memory Wait States
			0	0	0 SYSCLK Wait States
			0	1	1 SYSCLK Wait States
			1	0	2 SYSCLK Wait States
			1	1	3 SYSCLK Wait States

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: Bus Cycle Generator Wait State Control 2 Register
 Type: Read/Write
 Index: 03H

Bit	Name	Default	Function		
D[7:5]	PCAW[2:0]	111	PCW2	PCW1	PCW0
			0	0	0
			0	0	1
			0	1	0
			0	1	1
			1	0	0
			1	0	1
			1	1	0
			1	1	1
D4	Reserved	0	Reserved for future use		
D[3:1]	PCBW[2:0]	111	PC Card 'B' Wait States. Decoding is same as for PC Card 'A'.		
D0	PCIODLY	0	0 - No I/O command delay. 1 - PC Card I/O Command Delay one Bus Clock (SYSCLK) cycle		

VADEM VG-230
SUB-NOTEBOOK
ENGINE

0CS-0V MEGAV
 NOC-BTC4-BUS

Name: **Memory Control 1 Register**

Type: **Read/Write**

Index: **04H**

Bit	Name	Default	Function			
D7	MAPEN	0	0 - Disable Memory Mapping 1 - Enable Memory			
D[6:4]	BANK[2:0]	111	BANK2 BANK1 BANK0			No. of RAM Banks Installed
			0	0	0	1 Note: FLASH
			0	0	1	2 banks can be installed
			0	1	0	3 above SRAM or
			0	1	1	4 PSRAM banks as long
			1	0	0	5 as data widths and de-
			1	0	1	6 vice sizes are consistent.
			1	1	0	In this case, the BANK
			1	1	1	7 setting must not
						8 include the number of
						FLASH banks.
D[3:0]	MTYP[3:0]	0H	MTYP3	MTYP2	MTYP1	MTYP0 Density and Type
			0	0	0	0 32K x 8 SRAM
			0	0	0	1 128K x 8 SRAM
			0	0	1	0 512K x 8 SRAM
			0	0	1	1 32K x 8 PSRAM
			0	1	0	0 128K x 8 PSRAM
			0	1	0	1 512K x 8 PSRAM
			0	1	1	0 256K x 1/4 DRAM
			0	1	1	1 512K x 8 DRAM
			1	0	0	0 1M x 1/4 DRAM
			1	0	0	1 4M x 1/4 DRAM
			1	0	1	0 256K x 16 DRAM
			1	0	1	1 Reserved for
			1	1	X	X future use

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: Memory Control 2 Register
Type: Read/Write
Index: 05H

Bit	Name	Default	Function
D7	RAMSIZ	0	0 - RAM is 16 bits wide 1 - RAM is 8 bits wide
D6	ROMOSIZ	X	Read Only bit reflecting state of ROM8/*16 pin 0 - BIOS ROM is 16 bits wide 1 - BIOS ROM is 8 bits wide
D5	ROM1SIZ	1	0 - Option ROM is 16 bits wide 1 - Option ROM is 8 bits wide
D4	SLWREF	0	0 - Normal Refresh Rate DRAM 1 - Slow Refresh Rate DRAM
D3	SRFDRAM	0	1 - Self Refresh DRAM. During Suspend, CAS before RAS cycles are not generated. Refresh is performed by DRAM
D[2:1]	Reserved	0	Reserved for future use
D0	*MRASDLY	0	0 - Delay mapper memory cycles until CPU T3 state 1 - Begin mapper memory cycles at CPU T2 state

VADEM VG-230
SUB-NOTEBOOK
ENGINE

OS-8V NEGAV
 XCOOTOM-SUE
 ENOMS

Name: **Alternate Display Buffer Start Address Register**
 Type: **Read/Write**
 Index: **06H**

Bit	Name	Default	Function
D7	ALTDDBREN	0	Alternate Display Buffer Refresh Enable 0 - Use top 32 Kbytes of upper memory bank for LCD Controller display refresh operations. 1 - Use 32 Kbytes beginning at offset into upper memory bank specified by DBA[21:15] for LCD Controller display refresh operations.
D[6:0]	DBA[21:15]	0	Alternate Display Buffer Start Address

Name: **LCD Configuration Control Register**
 Type: **Read/Write**
 Index: **07H**

Bit	Name	Default	Function
D7	*ENALCD	0	Sub-Notebook Engine LCD Enable/Disable Bit 0 - Enable SNE LCD Controller 1 - Disable SNE LCD Controller
D[6:5]	VIDSPD[1:0]	00	These bits determine the access speed of system RAM during video refresh cycles as follows: VIDSPD1 VIDSPD0 Clocks per video cycle
		0 0	4-8 bit RAM / 5-16 bit RAM (normal)
		0 1	5-8 bit RAM / 6-16 bit RAM (slow)
		1 0	3-8 bit RAM / 4-16 bit RAM (fast)
		1 1	Reserved
D[4:0]	Reserved	0H	Reserved for future use.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: **Keyboard Mode Register**
Type: **Read/Write**
Index: **08H**

Bit	Name	Default	Function		
D[7:4]	SW[8:5]	0H	Software programmable bits used to select the setting of system switches SW[8:5] (display type and floppy drive count).		
D3	KBDMODE	0	0 - Select Keyboard Scanner pin configuration 1 - Redefine Keyboard Scanner pins		
D2	*KBDENA	0	0 - Enable PC/XT serial keyboard I/F 1 - Disable PC/XT serial keyboard I/F Only meaningful when Keyboard Scanner pins are redefined (KBDMODE=1). Setting *KBDENA high directs port 60H accesses to the external data bus D[15:0] and further redefines KBDAT pin as IRQ1.		
D[1:0]	SCLK[1:0]	00	SCLK1	SCLK0	NMI Scan Rate
			0	0	51.2 Hz
			0	1	64 Hz
			1	0	85.3 Hz
			1	1	128 Hz

Name: **Keyboard Scan Control Register**
Type: **Read/Write**
Index: **09H**

Bit	Name	Default	Function	
D[7:0]	S[7:0]	00H	SCAN[7:0] output enabled. 0 - Associated SCAN[7:0] pin is driven Hi-Z. 1 - Associated SCAN[7:0] pin driven low.	
Note: In PC/XT serial I/F mode the Keyboard Scan logic is disabled (S[7:0] forced low) allowing the SCAN[7:0] output buffers to be controlled by other logic.				

VADEM VG-230

SUB-NOTEBOOK ENGINE

DRS-GV MEGAW
DOSEWOM-EU
SUSIUS

Name: **Keyboard Return Status Low Register**
Type: **Read Only**
Index: **0AH**

Bit	Name	Default	Function
D[7:0]	R[7:0]	FFH	RET[7:0] input status. 0 - Associated RET[7:0] switch position is closed. 1 - Associated RET[7:0] switch position is open.

Note: In PC/XT serial I/F mode this register is ignored.

Name: **Keyboard Return Status High Register**
Type: **Read Only**
Index: **0BH**

Bit	Name	Default	Function
D[7:4]	SH[3:0]	FH	SHFT[3:0] input status. 0 - Associated SHFT[3:0] switch position is closed. 1 - Associated SHFT[3:0] switch position is open.
D[3:0]	R[11:8]	FH	RET[11:8] input status. 0 - Associated RET[11:8] switch position is closed. 1 - Associated RET[11:8] switch position is open.

Note: In PC/XT serial I/F mode, this register is ignored.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: Keyboard Shift and NMI Status Register
Type: Read/Write
Index: 0CH

Bit	Name	Default	Function
D7	KEYNMI	0	1 - NMI caused by Keyboard Input. Writing this register with bit D7 set high will clear both the NMI signal and the KEYNMI bit.
D6	STMONMI	0	1 - NMI caused by Keyboard Scan Time Out. Writing this register with bit D6 set high will clear both the NMI signal and the STMONMI bit.
D5	PPIBNMI	0	1 - NMI caused by write to PPIB port requesting Keyboard Diagnostics. Writing this register with bit D5 set high will clear both the NMI signal and the PPIBNMI bit.
D4	KNMIEN	0	1 - Enable Keyboard Input NMIs.
D3	SNMIEN	0	1 - Enable Periodic NMIs generated by the Scan Timer.
D2	PNMIEN	0	1 - Enable NMIs caused by writes to PPIB port requesting Keyboard Diagnostics.
D1	Reserved	0	Reserved for future use.
D0	SH4	0	SHFT4 input status. 0 - SHFT4 switch position is closed. 1 - SHFT4 switch position is open. Note: In PC/XT serial I/F mode, this register bit is ignored.

VADEM VG-230
SUB-NOTEBOOK
ENGINE

descrIMCAV
 NOSETOURUS
 EALIQUA

Name: **ICU Mode Register**
 Type: **Read/Write**
 Index: **0DH**

Bit	Name	Default	Function			IRQA Interrupt Channel Select
D[7:5]	IRAS[2:0]	101	IRAS2	IRAS1	IRAS0	
			0	0	0	Illegal
			0	0	1	Illegal
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	7
D4	Reserved	0	Reserved for future use.			
D[3:1]	IRBS[2:0]	110	IRBS2	IRBS1	IRBS0	IRQB Interrupt Channel Select
			0	0	0	Illegal
			0	0	1	Illegal
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	7
D0	Reserved	0	Reserved for future use.			

VADEM VG-230
SUB-NOTEBOOK
ENGINE

VADEM VG-230
 SUB-NOTEBOOK
 ENGINE

Name: **DMA Mode Register**
 Type: **Read/Write**
 Index: **0EH**

Bit	Name	Default	Function	Refresh Wait States
D[7:5]	REFW[2:0]	111	REFW2 REFW1 REFW0	
			0 0 0	0
			0 0 1	1
			0 1 0	2
			0 1 1	3
			1 0 0	4
			1 0 1	5
			1 1 0	6
			1 1 1	7
D4	STPDCLK	0	0 - DMA clock runs always 1 - DMA clock runs only during DMA cycles	
D[3:2]	WDLY[1:0]	01	WDLY1 WDLY0	IOWR/MWR Command Delay
			0 0	0 SYSCLK cycles
			0 1	1 SYSCLK cycles
			1 0	2 SYSCLK cycles
			1 1	3 SYSCLK cycles
Note: For each SYSCLK cycle command delay specified by WDLY[1:0] one bus wait state will be added to the DMA cycle.				
D[1:0]	DRQS[1:0]	10	DRQS1 DRQS0	DMA Channel Select
			0 0	Illegal
			0 1	DRQ1/*DACK1
			1 0	DRQ2/*DACK2
			1 1	DRQ3/*DACK3

VADEM VG-230

SUB-NOTEBOOK ENGINE

DATA SHEET
NO. 00000000000000000000000000000000

Name: **SIO Mode Register**
 Type: **Read/Write**
 Index: **10H**

Bit	Name	Default	Function
D7	SIOENA	1	0 - Disable internal Serial Port 1 - Enable internal Serial Port
D6	STPSCLK	0	0 - Enable SIO crystal oscillator 1 - Disable SIO crystal oscillator
D5	SPSEL	0	0 - SIO Port appears at I/O 3F8H - 3FFH and uses IRQ4 1 - SIO Port appears at I/O 2F8H - 2FFH and uses IRQ3
D[4:0]	Reserved	00H	Reserved for future use.

Name: **SIO Power Control Register**
 Type: **Read/Write**
 Index: **11H**

Bit	Name	Default	Function
D7	INPMSK	0	0 - Retrigger Serial Port clock timer on high to low transition of RXD, *DCD, *RI, *DSR, or *CTS inputs. 1 - Mask above inputs from retriggering Serial Port clock
D6	TXDMSK	0	0 - Retrigger Serial Port clock timer on writes to transmit buffer 1 - Mask above writes from retriggering Serial Port clock
D5	Reserved	0	Reserved for future use
D4	TCLKSEL	0	0 - Timer range is from 1 to 15 seconds (1 sec. resolution) 1 - Timer range is from 8 sec. to 2 min. (8 sec. resolution)
D[3:0]	TMO[3:0]	0H	SIO Clock time-out value. Setting this register to 0 disables the timer.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: **Timer Mode Register**
Type: **Read/Write**
Index: **13H**

Bit	Name	Default	Function
D[7:1]	Reserved	0	Reserved for future use
D0	STPTCLK	0	0 - 8254 Timer clock, TCLK, runs always 1 - 8254 Timer clock, TCLK, stopped during Doze/Sleep

Name: **PIO Mode Register**
Type: **Read/Write**
Index: **18H**

Bit	Name	Default	Function																				
D7	PIOENA	0	0 - Disable internal Parallel Port 1 - Enable internal Parallel Port (This bit is valid only if Keyboard Scan function is disabled. Otherwise, Parallel Port is forced to be disabled.)																				
D6	Reserved	0	Reserved for future use																				
D[5:4]	PPSEL[1:0]	00	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th> <th>PPSEL1</th> <th>PPSEL0</th> <th>Parallel Port I/O Address</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>278H-27AH</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>378H-37AH</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>3BCH-3BEH</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>170H-172H</td> </tr> </tbody> </table>		PPSEL1	PPSEL0	Parallel Port I/O Address	0	0	0	278H-27AH	0	0	1	378H-37AH	1	0	0	3BCH-3BEH	1	1	1	170H-172H
	PPSEL1	PPSEL0	Parallel Port I/O Address																				
0	0	0	278H-27AH																				
0	0	1	378H-37AH																				
1	0	0	3BCH-3BEH																				
1	1	1	170H-172H																				
D3	BIDIR	0H	0 - Parallel Port is uni-directional (output only) 1 - Parallel Port is bi-directional. Setting the PPDIR bit of the Parallel Port Control register forces reads from the Parallel port data registers to be sourced from the external data bus.																				
D[2:0]	Reserved	0H	Reserved for future use																				

VADEM VG-230

SUB-NOTEBOOK ENGINE

DES-av MEGAV
NO CBT/OW/EN
T

Name: **Main NMI Status Register**
 Type: **Read/Write**
 Index: **19H**

Bit	Name	Default	Function	
D[7:4]	TA[3:0]	X	NMI Trap Address bits. ISA[3:0] are latched when an NMI is generated by the System Management Unit to drive these bits.	
D[3:2]	ENMI[1:0]	00	ENMI1	System Management NMI Status
			0 0	No System Management NMI pending
			0 1	Port 1 System Management NMI pending
			1 0	Port 2 System Management NMI pending
			1 1	Port 3 System Management NMI pending
			A particular System Management NMI is cleared by writing this register with bits D[3:2] configured to select that NMI.	
D1	KBDNMI	0	1 - NMI generated by Keyboard	
D0	PMUNMI	0	1 - NMI generated by PMU	

Name: **Port 1 NMI Trap Address Low Register**
 Type: **Read/Write**
 Index: **1AH**

Bit	Name	Default	Function
D[7:0]	P1TA[7:0]	00H	Lower 8 address bits of the I/O address which will be emulated.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: Port 1 NMI Trap Address High Register
Type: Read/Write
Index: 1BH

Bit	Name	Default	Function		
D[7:6]	P1EN[1:0]	00	P1EN1	P1EN0	Port 1 Emulation NMI Mode
			0	0	Disable Port 1 NMIs.
			0	1	Generate NMI on IORD from Port 1 address.
			1	0	Generate NMI on IOWR to Port 1 address.
			1	1	Generate NMI on IORD from or IOWR to Port 1 address.
D[5:4]	P1RNG[1:0]	00	P1RNG1	P1RNG0	Port 1 Address Range
			0	0	2 Bytes
			0	1	4 Bytes
			1	0	8 Bytes
			1	1	16 Bytes
D3	P1MIR	0	0 - Disable address mirroring. Port 1 decoding is based upon ISA[15:0], and is enabled only when ISA[15:10] are all low. 1 - Enable address mirroring. Port 1 decoding is based only upon ISA[9:0].		
D2	Reserved	0	Reserved for future use.		
D[1:0]	P1TA[9:8]	00	Upper 2 address bits of the I/O address which will be emulated.		

Name: Port 2 NMI Trap Address Low Register
Type: Read/Write
Index: 1CH
(See Port 1 NMI Trap Address Low Register for bit definitions)

Bit	Name	Default	Function
D[7:0]	P2TA[7:0]	00H	

**VADEM VG-230
SUB-NOTEBOOK
ENGINE**

Name: Port 2 NMI Trap Address High Register
Type: Read/Write
Index: 1DH
(See Port 1 NMI Trap Address High Register for bit definitions)

Bit	Name	Default	Function
D[7:6]	P2EN[1:0]	00	
D[5:4]	P2RNG[1:0]	00	
D3	P2MIR	0	
D2	Reserved	0	Reserved for future use.
D[1:0]	P2TA[9:8]	00	

Name: Port 3 NMI Trap Address Low Register
Type: Read/Write
Index: 1EH
(See Port 1 NMI Trap Address Low Register for bit definitions)

Bit	Name	Default	Function
D[7:0]	P3TA[7:0]	00H	

Name: Port 3 NMI Trap Address High Register
Type: Read/Write
Index: 1FH
(See Port 1 NMI Trap Address High Register for bit definitions)

Bit	Name	Default	Function
D[7:6]	P3EN[1:0]	00	
D[5:4]	P3RNG[1:0]	00	
D3	P3MIR	0	
D2	Reserved	0	Reserved for future use.
D[1:0]	P3TA[9:8]	00	

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: PC Card Controller Mode Register
 Type: Read/Write
 Index: 20H

Bit	Name	Default	Function		
D7	*SLOT0EN	0	0 - Enable PC Card Slot 0		
D6	*SLOT1EN	1	0 - Enable PC Card Slot 1 Note: In order to enable PC Card Slot 1, the Keyboard Scan function must be disabled.		
D[5:4]	IRSTS[1:0]	11	IRSTS1	IRSTS0	Interrupt Channel Select for Controller Status Interrupts
			0	0	NMI
			0	1	IRQ2
			1	0	IRQ6
			1	1	IRQ7
D3	S0PGMEN	0	1 - Enable Slot 0 Programming Voltage (VPPENA)		
D2	Reserved	0	Reserved bits		
D1	S1PGMEN	0	1 - Enable Slot 1 Programming Voltage (VPPENB)		
D0	Reserved	0	Reserved bits		
Note: Programming controls are automatically disabled when a card is removed from its socket or when Vcc to the cards has been removed.					

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Power Management	00	00	00	00	00	00	00	00
Keyboard Scan	00	00	00	00	00	00	00	00
PCI Bus Control	00	00	00	00	00	00	00	00
PCI Bus Control	00	00	00	00	00	00	00	00

VADEM VG-230

SUB-NOTEBOOK ENGINE

DE2-DV MEDAV
XOOGHOMA-SUS
EQUITY

Name: PC Card Slot 0 Control Register
Type: Read/Write
Index: 21H

Bit	Name	Default	Function		
D7	IO8BIT	0	1 - PC Card Slot 0 supports 8 bit I/O only. Data is transferred from the PC I/O Card on the low order data bus (D[7:0]).		
D6	IO/*M	0	0 - PC Card Slot 0 configured for Memory I/F 1 - PC Card Slot 0 configured for I/O I/F		
			While either one of *CD[2:1]A is high indicating a PC Card is not installed, or the PC Card is powered OFF, this bit is automatically reset low and the controller is forced into the Memory I/F Mode.		
D5	*REG	0	0 - Direct PC Card access to REG (Attribute) memory 1 - Direct PC Card access to Common memory	Normally, the *REGA output pin is driven directly from this bit. During DMA Cycles, this bit is ignored and the *REGA output is driven high.	
D[4:2]	IRCRD[2:0]	111	IRCRD2	IRCR0	IRCRD0
			0	0	X
			0	1	0
			0	1	1
			1	0	0
			1	0	1
			1	1	0
			1	1	1
D[1:0]	CDLY[1:0]	01	CDLY1	CDLY0	PC Card Memory Command Delay
			0	0	0 CPUCLK cycle
			0	1	1 CPUCLK cycle
			1	0	2 CPUCLK cycle
			1	1	3 CPUCLK cycle

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: **PC Card Slot 0 Status Register**
 Type: **Read/Write**
 Index: **22H**

Bit	Name	Default	Function
D7	*BUSY/ *CRDINT	1	Read Only bit reflecting state of RDY/*BSYA input during Memory Mode or latched *IREQA for I/O Mode. 0 - Card Busy (Memory) Card Interrupt Pending (I/O) In I/O mode this bit may be set by writing this register with bit D7 set high.
D6	BVD2/ *AUDIO	1	Read Only bit reflecting state of BVD2A input during Memory Mode or *AUDIOA for I/O Mode. 0 - Battery Low (Memory) Card Speaker Active (I/O) In Memory mode, this bit is driven directly from the BVD2 input pin when Low Battery interrupts are masked OFF. Or, it is driven from the latched BVD2 input when Low Battery interrupts are enabled. When interrupts are enabled, writing this register with bit D6 set high clears the Low Battery Interrupt and sets this bit. In I/O mode the state of the I/O card signal may be read here.
D5	BVD1/ *STSCHG	1	Read Only bit reflecting state of BVD1A input during Memory Mode or *STSCHGA for I/O Mode. 0 - Battery Fail (Memory) Status Change (I/O) This bit is driven directly from the BVD1/*STSCHG input when Battery Fail interrupts are masked OFF. Or, it is driven from the latched BVD1/*STSCHG input when Battery Fail interrupts are enabled. When interrupts are enabled, writing this register with bit D5 set high clears the Battery Fail or Status Changed Interrupt and sets this bit.
D4	*PRESENT	X	Read Only bit reflecting state of *CD[2:1]A inputs 0 - Card Present (Low when both *CD[2:1]A are low) While Card A is removed from its socket, PC Card Slot 0 Status bits D[7:5] will be forced high, and D1 will be forced low.
D3	*CRDCHG	1	Card Change status bit. *CRDCHG is reset on the rising edge of either *CD[2:1]A. 0 - Card has been Changed This bit is set and the Card Change Interrupt is cleared by writing this register with bit D3 set high.
D2	*CRDTM0	1	Card Activity Time-Out. 0 - Card Time-Out Writing this register with bit D2 set high sets this bit and clears the Card Time-Out interrupt.
D1	WP/NU	X	Read Only bit reflecting state of WPA input during Memory Mode. This pin reads back low in I/O Mode. 1 - Card Write Protected
D0	CRDOFF	0	1 - Power to PC Card slot 0 and 1 is OFF.

VADEM VG-230

SUB-NOTEBOOK ENGINE

DCS-DV MEGAV
NOOS ETOVA RUS
EOL 2004

Name: PC Card Slot 0 Interrupt Mask Register
 Type: Read/Write
 Index: 23H

Bit	Name	Default	Function
D7	IREQMSK	1	0 - Enable interrupts generated from Slot 0 I/O Cards
D6	LBMSK	0	0 - Enable Slot 0 low battery warning interrupts (Memory Mode) or disable PC Card Audio Output (I/O Mode). When this bit is reset Low in I/O Mode, the PC Card Audio signal is disabled and will read back High in the Status Register.
D5	LLBMSK	0	0 - Enable Slot 0 Battery Fail Alarm Interrupts (Memory Mode) or Enable Slot 0 Status Changed Interrupts (I/O Mode)
D4	Reserved	0	Reserved bit
D3	CHGMSK	0	0 - Enable interrupts for Card Removal from Slot 0
D[2:1]	Reserved	00	Reserved bits
D0	PULSED	0	0 - Controller supports Level Mode Interrupts from PC I/O Cards 1 - Controller supports Pulsed Mode Interrupts from PC I/O Cards

Name: PC Card Slot 0 I/O High Address Register
 Type: Read/Write
 Index: 24H

Bit	Name	Default	Function
D[7:0]	A[15:8]	00H	Upper address bits for slot 0 PC Card base I/O address.

Name: PC Card Slot 0 I/O Low Address Register
 Type: Read/Write
 Index: 25H

Bit	Name	Default	Function
D[7:3]	A[7:3]	00H	Low address bits for slot 0 PC Card base I/O address.
D[2:0]	Reserved	000	Reserved bits

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: PC Card Slot 0 I/O Address Range Register
 Type: Read/Write
 Index: 26H

Bit	Name	Default	Function	I/O Range					
D[7:3]	A[7:3]MSK	00H	Mask bits for lower address bits. Each bit allows its corresponding address bit to be masked from the address comparison as follows:	A7MSK	A6MSK	A5MSK	A4MSK	A3MSK	
				0	0	0	0	0	8 Bytes
				0	0	0	0	1	16 Bytes
				0	0	0	1	1	32 Bytes
				0	0	1	1	1	64 Bytes
				0	1	1	1	1	128 Bytes
				1	1	1	1	1	256 Bytes
D[2:1]	Reserved	000	Reserved bits						
D0	*INPMASK	0	Card A input acknowledge mask bit. 0 - Ignore PC I/O card *INPACK signal. PC card data buffers enabled whenever chip select is asserted. 1 - Enable PC I/O Card *INPACK signal. PC card data buffers enabled only when chip select is asserted and *INPACK is returned from PC I/O card.						

Register	Default	Range	Name	Bit
00H	[8:0]	[0:0]	PC Card Slot 0 I/O Address Range Register	26H

Register	Default	Range	Name	Bit
00H	[15:8]	[0:0]	PC Card Slot 0 I/O Address Range Register	26H

VADEM VG-230

SUB-NOTEBOOK ENGINE

PC Card Slot 1 Control Register

Name: PC Card Slot 1 Control Register
 Type: Read/Write
 Index: 27H

Bit	Name	Default	Function																																
D7	I08BIT	0	1 - PC Card Slot 0 supports 8 bit I/O only. Data is transferred from the PC I/O Card on the low order data bus (D[7:0]).																																
D6	I0/*M	0	0 - PC Card Slot 0 configured for Memory I/F 1 - PC Card Slot 0 configured for I/O I/F																																
			While either one of *CD[2:1]B is high indicating a PC Card is not installed, or the PC Card is powered OFF, this bit is automatically reset low and the controller is forced into the Memory I/F Mode.																																
D5	*REG	0	0 - Direct PC Card access to REG (Attribute) memory 1 - Direct PC Card access to Common memory Normally, the *REGB output pin is driven directly from this bit. During DMA Cycles, this bit is ignored and the *REGB output is driven high.																																
D[4:2]	IRCRD[2:0]	111	<table> <thead> <tr> <th>IRCRD2</th> <th>IRCR0</th> <th>IRCRD0</th> <th>Interrupt Channel Select for PC Card (IREQ)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>X</td> <td>Illegal</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>IRQ2</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>IRQ3</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>IRQ4</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>IRQ5</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>IRQ6</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>IRQ7</td> </tr> </tbody> </table>	IRCRD2	IRCR0	IRCRD0	Interrupt Channel Select for PC Card (IREQ)	0	0	X	Illegal	0	1	0	IRQ2	0	1	1	IRQ3	1	0	0	IRQ4	1	0	1	IRQ5	1	1	0	IRQ6	1	1	1	IRQ7
IRCRD2	IRCR0	IRCRD0	Interrupt Channel Select for PC Card (IREQ)																																
0	0	X	Illegal																																
0	1	0	IRQ2																																
0	1	1	IRQ3																																
1	0	0	IRQ4																																
1	0	1	IRQ5																																
1	1	0	IRQ6																																
1	1	1	IRQ7																																
D[1:0]	CDLY[1:0]	01	<table> <thead> <tr> <th>CDLY1</th> <th>CDLY0</th> <th>PC Card Memory Command Delay</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0 CPUCLK cycle</td> </tr> <tr> <td>0</td> <td>1</td> <td>1 CPUCLK cycle</td> </tr> <tr> <td>1</td> <td>0</td> <td>2 CPUCLK cycle</td> </tr> <tr> <td>1</td> <td>1</td> <td>3 CPUCLK cycle</td> </tr> </tbody> </table>	CDLY1	CDLY0	PC Card Memory Command Delay	0	0	0 CPUCLK cycle	0	1	1 CPUCLK cycle	1	0	2 CPUCLK cycle	1	1	3 CPUCLK cycle																	
CDLY1	CDLY0	PC Card Memory Command Delay																																	
0	0	0 CPUCLK cycle																																	
0	1	1 CPUCLK cycle																																	
1	0	2 CPUCLK cycle																																	
1	1	3 CPUCLK cycle																																	

VADEM VG-230

SUB-NOTEBOOK ENGINE

Name: PC Card Slot 1 Status Register
 Type: Read/Write
 Index: 28H

Bit	Name	Default	Function
D7	*BUSY/ *CRDINT	1	Read Only bit reflecting state of RDY/*BSYB input during Memory Mode or latched *IREQB for I/O Mode. 0 - Card Busy (Memory) Card Interrupt Pending (I/O) In I/O mode this bit may be set by writing this register with bit D7 set high.
D6	BVD2/ *AUDIO	1	Read Only bit reflecting state of BVD2B input during Memory Mode or *AUDIOA for I/O Mode. 0 - Battery Low (Memory) Card Speaker Active (I/O) In Memory mode, this bit is driven directly from the BVD2 input pin when Low Battery interrupts are masked OFF. Or, it is driven from the latched BVD2 input when Low Battery interrupts are enabled. When interrupts are enabled, writing this register with bit D6 set high clears the Low Battery Interrupt and sets this bit. In I/O mode the state of the I/O card signal may be read here.
D5	BVD1/ *STSCHG	1	Read Only bit reflecting state of BVD1B input during Memory Mode or *STSCHGB for I/O Mode. 0 - Battery Fail (Memory) Status Change (I/O) This bit is driven directly from the BVD1/*STSCHG input when Battery Fail interrupts are masked OFF. Or, it is driven from the latched BVD1/*STSCHG input when Battery Fail interrupts are enabled. When interrupts are enabled, writing this register with bit D5 set high clears the Battery Fail or Status Changed Interrupt and sets this bit.
D4	*PRESENT		Read Only bit reflecting state of *CD[2:1]B inputs 0 - Card Present (Low when both *CD[2:1]B are low) While Card B is removed from its socket, PC Card Slot 0 Status bits D[7:5] will be forced high, and D1 will be forced low.
D3	*CRDCHG	1	Card Change status bit. *CRDCHG is reset on the rising edge of either *CD[2:1]B. 0 - Card has been Changed This bit is set and the Card Change Interrupt is cleared by writing this register with bit D3 set high.
D2	*CRDTM0	1	Card Activity Time-Out. 0 - Card Time-Out Writing this register with bit D2 set high sets this bit and clears the Card Time-Out interrupt.
D1	WP/NU		Read Only bit reflecting state of WPA input during Memory Mode. This pin reads back low in I/O Mode. 1 - Card Write Protected
D0	CRDOFF	0	1 - Power to PC Card slot 0 and 1 is OFF.

VADEM VG-230

SUB-NOTEBOOK ENGINE

OCS-0V MEGAV
SUB-NOTEBOOK ENGINE

Name: PC Card Slot 1 Interrupt Mask Register
 Type: Read/Write
 Index: 29H

Bit	Name	Default	Function
D7	IREQMSK	1	0 - Enable interrupts generated from Slot 0 I/O Cards
D6	LBMSK	0	0 - Enable Slot 1 low battery warning interrupts (Memory Modes) or disable PC Card Audio Output (I/O Mode). When this bit is reset Low in I/O Mode, the PC Card Audio signal is disabled and will read back High in the Status Register.
D5	LLBMSK	0	0 - Enable Slot 1 Battery Fail Alarm Interrupts (Memory Mode) 1 - Enable Slot 1 Status Changed Interrupts (I/O Mode)
D4	Reserved	0	Reserved bit
D3	CHGMSK	0	0 - Enable interrupts for Card Removal from Slot 1
D[2:1]	Reserved	00	Reserved bits
D0	PULSED	00	0 - Controller supports Level Mode interrupts from PC I/O Cards 1 - Controller supports Pulsed Mode interrupts from PC I/O Cards

Name: PC Card Slot 1 I/O High Address Register
 Type: Read/Write
 Index: 2AH

Bit	Name	Default	Function
D[7:0]	A[15:8]	00H	Upper address bits for slot 1 PC Card base I/O address.

Name: PC Card Slot 1 I/O Low Address Register
 Type: Read/Write
 Index: 2BH

Bit	Name	Default	Function
D[7:3]	A[7:3]	00H	Low address bits for slot 1 PC Card base I/O address.
D[2:0]	Reserved	000	Reserved bits

VADEM VG-230
SUB-NOTEBOOK
ENGINE

VADEM VG-230
 SUB-NOTEBOOK
 ENGINE

Name: PC Card Slot 1 I/O Address Range Register
 Type: Read/Write
 Index: 2CH

Bit	Name	Default	Function	I/O Range					
D[7:3]	A[7:3]MSK	00H	Mask bits for lower address bits. Each bit allows its corresponding address bit to be masked from the address comparison as follows:	A7MSK	A6MSK	A5MSK	A4MSK	A3MSK	
				0	0	0	0	0	8 Bytes
				0	0	0	0	1	16 Bytes
				0	0	0	1	1	32 Bytes
				0	0	1	1	1	64 Bytes
				0	1	1	1	1	128 Bytes
				1	1	1	1	1	256 Bytes
D[2:1]	Reserved	000	Reserved bits						
D0	*INPMASK	0	Card A input acknowledge mask bit. 0 - Ignore PC I/O card *INPACK signal. PC card data buffers enabled whenever chip select is asserted. 1 - Enable PC I/O Card *INPACK signal. PC card data buffers enabled only when chip select is asserted and *INPACK is returned from PC I/O card.						

Function	DepPin	Yours	Pin
Card access I/O address	000	[8:24]	10:30

Function	DepPin	Yours	Pin
Card access I/O address	000	[8:24]	10:30

VADEM VG-230

SUB-NOTEBOOK ENGINE

OS-9V-MEDIA
NOOBSTON-BUS
EMBED

Name: PC Card Power Control Register
Type: Read/Write
Index: 2DH

Bit	Name	Default	Function
D7	TMOMSK	1	0 - Enable interrupts for Activity Time-Out 1 - VP output from PMU does not control power to PC Cards
D6	VOPEN	0	0 - VP output is Or'ed with Activity timer to control power to PC Cards 1 - VPCRD output is defined as High = ON
D5	POL	1	0 - VPCRD output is defined as Low = ON 1 - VPCRD output is defined as High = ON
D4	VPCRD	0	PC Card On/Off bit This bit is ignored when Time-Out interrupts are disabled or when both PC Card Slots are empty. When Time-Out interrupts are disabled, power to the PC Card is automatically removed when the PC Card Activity timer expires. When Time-Out interrupts are enabled, this bit is used by software to control power to the PC Cards.
D[3:0]	Reserved	0H	Reserved bit

Software	Hardware	ROM	ROM
Initial value of 2000 bits to end word	0000	INITIATE	PROG
Initial value of word 2000 bits to end word	0000	INITIATE	PROG

VADEM VG-230

SUB-NOTEBOOK ENGINE

VG-230
SUB-NOTEBOOK
ENGINE

Name: PC Card Activity Timer Register
Type: Read/Write
Index: 2EH

Bit	Name	Default	Function
D7	TMRES	0	0 - Timer supports from 15 to 225 sec. (15 sec. resolution) 1 - Timer supports from 1 to 15 min. (1 min. resolution)
D[6:4]	Reserved	000	Reserved bits
D[3:0]	TMO[3:0]	0H	TMO[3:0] select the Activity Time-Out value. Setting TMO[3:0] all low will disable the timer.

Note: When Activity Time-Out interrupts are disabled and the Activity Timer expires, power to the PC Cards will automatically be removed. Subsequent activity to the PC Cards WILL NOT restore power to the Slots. In order for power to be restored, software must first write any value to the PC Card Activity Timer Register.

Name: BIOS Time Base Low Register
Type: Read Only
Index: 30H

Bit	Name	Default	Function
D[7:0]	TMR[7:0]	00H	Low byte of the BIOS Timer count.

Name: BIOS Time Base High Register
Type: Read Only
Index: 31H

Bit	Name	Default	Function
D[7:0]	TMR[15:8]	00H	High byte of the BIOS Timer count. The BIOS Time Base Registers are driven by a 16 bit up counter clocked from the 1.19Mhz TCLK signal.

VADEM VG-230

SUB-NOTEBOOK ENGINE

DCS-av M3GAV
NOOGASTON-BUS
SHM04H

Name: **GPIO Mode Register**
Type: **Read/Write**
Index: **32H**

Bit	Name	Default	Function		
D[7:6]	GP3M[1:0]	00	GP3M1	GP3M0	LCDL3 Function
			0	0	General Purpose Input-GPI3
			0	1	LCDL3
			1	0	General Purpose Output-GPO3
			1	1	Reserved
D[5:4]	GP2M[1:0]	00	GP2M1	GP2M0	LCDL2 Function
			0	0	General Purpose Input-GPI2
			0	1	LCDL2
			1	0	General Purpose Output-GPO2
			1	1	SYSCLK-XT Bus Clock
D[3:2]	GP1M[1:0]	00	GP1M1	GP1M0	LCDL1 Function
			0	0	General Purpose Input-GPI1
			0	1	LCDL1
			1	0	General Purpose Output-GPO1
			1	1	ALE-Address Latch Enable
D[1:0]	GP0M[1:0]	00	GP0M1	GP0M0	LCDL0 Function
			0	0	General Purpose Input-GPI0
			0	1	LCDL0
			1	0	General Purpose Output-GPO0
			1	1	*DACK0 - Indicates Memory Refresh

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: **GPIO Control Register**
Type: **Read/Write**
Index: **33H**

Bit	Name	Default	Function
D[7:4]	Reserved	0H	Reserved Bits
D3	GPIO3	0	General Purpose I/O bit 3. When programmed as GPO, this bit is read/write and appears on the LCDL3 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL3 pin. Otherwise, this bit will read back low.
D2	GPIO2	0	General Purpose I/O bit 2. When programmed as GPO, this bit is read/write and appears on the LCDL2 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL2 pin. Otherwise, this bit will read back low.
D1	GPIO1	0	General Purpose I/O bit 1. When programmed as GPO, this bit is read/write and appears on the LCDL1 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL1 pin. Otherwise, this bit will read back low.
D0	GPIO0	0	General Purpose I/O bit 0. When programmed as GPO, this bit is read/write and appears on the LCDL0 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL0 pin. Otherwise, this bit will read back low.

VADEM VG-230

SUB-NOTEBOOK ENGINE

DATA SHEET
NO. 00000000000000000000000000000000

Name: **Top of Memory Register**
 Type: **Read/Write**
 Index: **38H**

Bit	Name	Default	Function
D7	BUF16K	0	0 - Display Buffer size is 32 Kbytes 1 - Display Buffer size is 16 Kbytes
D6	Spare	0	Spare R/W bit
D[5:0]	BA[19:14]	101000	Top of memory. For addresses below 640 K, these bits are set to indicate the start of physical RAM reserved for the display buffer or other uses. Once set, all memory accesses to addresses equal to or greater than the value written to these bits will be inhibited except through the CGA address space (B8000H - BFFFFH), or mapping registers.

Name: **ICU Shadow Register**
 Type: **Read Only**
 Index: **40H**

Bit	Name	Default	Function
D[7:4]	Reserved	FH	Reserved bits read back high.
D3	ICU_BUSY	0	0 - ICU not busy 1 - ICU busy. This bit is set high while either the INIT or POLL bits are high.
D2	INIT	0	0 - ICU not being initialized. 1 - ICU is being initialized. This bit is set high when ICW1 is written to the ICU and cleared when ICW4 is written to the ICU.
D1	POLL	0	0 - ICU is not programmed into Polled Mode 1 - ICU is programmed into Polled Mode. Writing Port 20H of the ICU will set or clear this bit. Reading Port 20H of the ICU will clear this bit.
D0	ISR	0	0 - Reading the ICU ISR/IRR register returns IRR value. 1 - Reading the ICU ISR/IRR register returns ISR value.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: RTC Seconds Register
Type: Read/Write
Index: 70H

Bit	Name	Default	Function
D[7:6]	Reserved	00	Reserved bits. Read back low.
D[5:0]	SEC[5:0]	00H	Binary value representing the seconds count. Valid settings are from 00H to 3BH.

Name: RTC Minutes Register
Type: Read/Write
Index: 71H

Bit	Name	Default	Function
D[7:6]	Reserved	00	Reserved bits. Read back low.
D[5:0]	MIN[5:0]	00H	Binary value representing the minutes count. Valid settings are from 00H to 3BH.

Name: RTC Hours Register
Type: Read/Write
Index: 72H

Bit	Name	Default	Function
D[7:5]	Reserved	000	Reserved bits. Read back low.
D[4:0]	HR[4:0]	00H	Binary value representing the hours count of a 24-hour clock. Valid settings are from 00H to 17H.

VADEM VG-230

SUB-NOTEBOOK ENGINE

CGS-0V MEGAV
NOOBESTOH-SU2
EADPME

Name: **RTC Day Low Register**

Type: **Read/Write**

Index: **73H**

Bit	Name	Default	Function
D[7:0]	DAY[7:0]	00H	Binary value representing the low day count. Valid settings are from 00H to FFH.

Name: **RTC Day High Register**

Type: **Read/Write**

Index: **74H**

Bit	Name	Default	Function
D[7:4]	Reserved	0H	Reserved bits. Read back low.
D[3:0]	DAY[11:8]	0H	Binary value representing the high day count. Valid settings are from 00H to 0FH.

Name: **RTC Alarm Seconds Register**

Type: **Read/Write**

Index: **75H**

Bit	Name	Default	Function
D[7:6]	Reserved	00	Reserved bits. Read back low.
D[5:0]	ALRS[5:0]	00H	Binary value representing the Alarm seconds count. Valid settings are from 00H to 3BH.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: **RTC Alarm Minutes Register**
Type: **Read/Write**
Index: **76H**

Bit	Name	Default	Function
D[7:6]	Reserved	00	Reserved bits. Read back low.
D[5:0]	ALRM[5:0]	00H	Binary value representing the Alarm minutes count. Valid settings are from 00H to 3BH.

Name: **RTC Alarm Hours Register**
Type: **Read/Write**
Index: **77H**

Bit	Name	Default	Function
D[7:5]	Reserved	00	Reserved bits. Read back low.
D[4:0]	ALRH[5:0]	00H	Binary value representing the Alarm hours count. Valid settings are from 00H to 17H.

Name: **RTC Alarm Day Register**
Type: **Read/Write**
Index: **78H**

Bit	Name	Default	Function
D[7:5]	Reserved	000	Reserved bits. Read back low.
D[4:0]	ALRD[4:0]	00H	Binary value representing the Alarm day count. Valid settings are from 00H to 1FH. This value is compared with the least significant 5 bits of the RTC Low Day counter.

VADEM VG-230

SUB-NOTEBOOK ENGINE

CCC-JV-MICAV
NOOBSTON-HUB
ENGINE

Name: **RTC Mode Register**
 Type: **Read/Write**
 Index: **79H**

Bit	Name	Default	Function
D7	*RTCEN	0	0 - Enable RTC Clock Index Registers 70-78H access 1 - Disable RTC Clock Index Registers 70-78H access
D6	*RAMEN	0	0 - Enable RTC CMOS RAM access 1 - Disable RTC CMOS RAM access
D5	UPDATE	0	0 - RTC Clock Running 1 - Pause RTC Clock for setting of Time and/or Alarm values.
D[4:2]	Reserved	0H	Reserved bits. Read back low.
D1	ALRMINT	0	0 - Disable RTC Alarm interrupts 1 - Enable RTC Alarm interrupts
D0	PERINT	0	0 - Disable 1Hz periodic interrupts 1 - Enable 1Hz periodic interrupts

Name: **RTC Status Register**
 Type: **Read/Write**
 Index: **7AH**

Bit	Name	Default	Function
D7	VALID	0	0 - Power to RTC and CMOS RAM has been lost. Contents are not valid. 1 - RTC Clock and CMOS RAM contents valid. System software sets the VALID bit following initialization of the RTC. VALID is cleared when power to VG-230 has been removed.
D[6:2]	Reserved	0	Reserved bit. Read back low.
D1	ALARM	0	0 - No RTC Clock Alarm Pending. 1 - RTC Clock Alarm Pending. Writing this register with bit D1 set high will clear both the RTCINT signal and the ALARM status bit.
D0	Periodic	0	0 - No Periodic Interrupt Pending. 1 - Periodic Interrupt Pending. Writing this register with bit D0 set high will clear both the RTCINT signal and the Periodic Status Bit.

VADEM VG-230

SUB-NOTEBOOK ENGINE

088-0G MEGAV
SUB-NOTEBOOK
ENGINE

Name: PMU Status Register
Type: Read/Write
Index: C0H

Bit	Name	Default	Function
D7	Resume	0	Resuming from SUSPEND (warmstart)
D[6:5]	WU[1:0]	00	Wakeup code bits
D[4:2]	NMI[2:0]	000	NMI cause code bits
D[1:0]	STATE[1:0]	00	State bits

Note: Only D0 and D1 are affected by a write.

The following table lists the State Codes for a Write to C0H.

State Code									Function
7	6	5	4	3	2	1	0		
X	X	X	X	X	X	0	0	command to ON	
X	X	X	X	X	X	0	1	command to DOZE	
X	X	X	X	X	X	1	0	command to SLEEP	
X	X	X	X	X	X	1	1	command to SUSPEND	
1	1	1	1	1	1	1	1	command to OFF	

Note: The NMI cause, state and wakeup codes are decoded as follows for a read to C0H.

Wakeup		NMI		State	
Code	Cause	Code	Cause	Code	State
00	None	000	None, or INMI	00	ON
01	EXT	001	EXT	01	DOZE
10	RTC	010	LB	10	SLEEP
11	RI	011	Reserved	11	SUSPEND
		100	SLEEP Timeout		
		101	SUSPEND Timeout		
		110	SLEEP to ON (Activity)		
		111	Reserved		

VADEM VG-230

SUB-NOTEBOOK ENGINE

des-ov MEGAV
DIGIBUS-DUE
ENGINE

Name: PMU Supply Register
 Type: Read Only
 Index: C1H

Bit	Name	Default	Function
D[7:4]	Reserved	0H	Reserved bits
D3	ACTIVITY	0	System activity
D2	Reserved	0	Reserved bit
D1	LB	X	Low battery
D0	LOCKOUT	1	Register write protected

Note: Following a hard reset or RESUME from SUSPEND or OFF modes, the PMU registers are write protected. Software must first read this register before attempting to write any PMU register.

Name: PMU Control Register
 Type: Read/Write
 Index: C2H

Bit	Name	Default	Function
D7	FSTCLK0	0	1 = Disable clock slow down in DOZE and SLEEP modes
D[6:4]	RING[2:0]	001	Bits RI pulses required for turn-on
		000	Disable RI
		001	1
		010	2
		011	3
		100	4
		101	5
		110	6
		111	7
D3	STATIC	0	Static CPU and RAM, clock stops in DOZE and SLEEP
D2	SLWREF	0	1 = slow refresh
D[1:0]	Reserved	00	Reserved bit

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: PMU Activity Mask Register

Type: Read/Write

Index: C3H

Bit	Name	Default	Function
D7	MSK_IORNG	1	Mask access to I/O ports defined by IORNG[6:0]
D6	MSK_VIDM	0	Mask access to video memory
D5	MSK_HD	0	Mask access to hard disk I/O
D4	MSK_FLP	0	Mask access to port 3F5
D3	MSK_SIO	0	Mask access to COM 1-2
D2	MSK_RTC	1	Mask access to port 70H, 71H
D1	MSK_KBD	0	Mask keyboard port 60H reads
D0	MSK_PIO	0	Mask access to LPT 1, 2, 3

Note: The activity monitor ACTIVITY output is the logical OR of all unmasked activity sources. This register affects only the ACTIVITY output.

Name: PMU NMI Mask Register

Type: Read/Write

Index: C4H

Bit	Name	Default	Function
D7	Reserved	0	Reserved bit
D6	MSK_NMI	1	Mask NMI input to PMU
D5	MSK_SUSPEND	1	Mask SUSPEND timeout
D4	MSK_SLEEP	1	Mask SLEEP timeout
D3	Reserved	1	Reserved bit
D2	MSK_LB	1	Mask LB input
D1	MSK_EXT	1	Mask EXT input
D0	Reserved	1	Reserved bit

Note: An NMI generated by the PMU is cleared by reading the NMI Mask Register.

VADEM VG-230

SUB-NOTEBOOK ENGINE

000-0V MEGAV
NOOBTON-SUB

Name: PMU I/O Range (IORNG) Register

Type: Read/Write
Index: C5H

Bit	Name	Default	Function
D7	RNGSIZE	0	0 = 16 byte range, 1 = 8 byte range
D6	IORNG6	0	Maskable I/O range base
D5	IORNG5	0	Maskable I/O range base
D4	IORNG4	0	Maskable I/O range base
D3	IORNG3	0	Maskable I/O range base
D2	IORNG2	0	Maskable I/O range base
D1	IORNG1	0	Maskable I/O range base
D0	IORNG0	0	Maskable I/O range base

Note: IORNG[6:0] are the base address bits A[9:3] for the maskable I/O port range in the activity monitor. RNGSIZE is the size of the range. IORNG0 is ignored when RNGSIZE is low.

PMU Power (PWR) Registers

Name: PMU POWER ON (PWRON) Register
Type: Read/Write
Index: C6H

Name: PMU POWER DOZE (PWRDOZE) Register
Type: Read/Write
Index: C7H

Name: PMU POWER SLEEP (PWRSLEEP) Register
Type: Read/Write
Index: C8H

Name: PMU POWER SUSPEND (PWRSSUSPEND) Register
Type: Read/Write
Index: C9H

Register	Default	Index
PWRON	FEH	C6H
PWRDOZE	FFH	C7H
PWRSLEEP	0CH	C8H
PWRSSUSPEND	00H	C9H

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

In each power management state, bits VP7, VP3, VP2 and VP0 of the appropriate PWR register correspond directly to the power control output signals of the VG-230. All other bits are unused. VP0 controls the VPLCD and VPBIAS signals after being logically ANDed with the LCD timer output. VP2 controls VPSYS, VP3 controls VPCRD and VP7 controls VPRAM. All bits are logically XNORed with the POLARITY register prior to driving the output signals.

Name: PMU Polarity Register
Type: Read/Write
Index: CAH

This register controls the polarity of the VP outputs. If a logic low is required for a VP signal to turn an external device on, the corresponding bit in the POLARITY register must be set low. If a high is required, the bit must be set high. The polarity of VPLCD and VPBIAS are both set by bit 0 of this register. The default value is FFH.

Name: PMU Output Register
Type: Read
Index: CBH

This read-only register reflects the bit values of the PWR register belonging to the active power management state. For each bit (VP0, VP2, VP3 and VP7) which is ON in the appropriate PWR register, the corresponding bit in the OUTPUT register will also be ON. Thus, the OUTPUT register reflects the state of the VG-230 VP signals (VPLCD, BPBIAS, VPSYS, VPCRD and VPRAM), without taking POLARITY register settings into consideration.

PMU Timer Registers

The PMU has four timers which may be set independently by means of registers. Each has its own range of allowable settings and its own default setting.

PMU Timer Registers
Table 3-3

Timer Name	Timer Range	Default Setting	Register Index
DOZE	1/8 - 14 sec	4 sec	CCH
SLEEP	1 - 15 min	2 min	CDH
SUSPEND	5 - 75 min	0 (disabled)	CEH
LCD	1 - 15 min	2 min	CFH

VADEM VG-230

SUB-NOTEBOOK ENGINE

OSG OV MEGAV
NOOBESTH-SUB
MEGAV

Name: PMU DOZE Timer Register
Type: Read/Write
Index: CCH

Bit	Name	Default	Function			
D[7:4]	Reserved	0000	Reserved bits			
D[3:0]	DOZTM[3:0]	1010	Bit	Time	Bit	Time
			0000	Disabled	1000	1 sec
			0001	1/8 sec	1001	2 sec
			0010	1/4 sec	1010	4 sec
			0011	3/8 sec	1011	6 sec
			0100	1/2 sec	1100	8 sec
			0101	5/8 sec	1101	10 sec
			0110	3/4 sec	1110	12 sec
			0111	7/8 sec	1111	14 sec

Name: PMU SLEEP Timer Register
Type: Read/Write
Index: CDH

Bit	Name	Default	Function			
D[7:4]	Reserved	0000	Reserved bits			
D[3:0]	SLPTM[3:0]	0010	Bit	Time	Bit	Time
			0000	Disabled	1000	8 min
			0001	1 min	1001	9 min
			0010	2 min	1010	10 min
			0011	3 min	1011	11 min
			0100	4 min	1100	12 min
			0101	5 min	1101	13 min
			0110	6 min	1110	14 min
			0111	7 min	1111	15 min

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: PMU SUSPEND Timer Register
 Type: Read/Write
 Index: CEH

Bit	Name	Default	Function			
D[7:4]	Reserved	0000	Reserved bits			
D[3:0]	SUSTM[3:0]	0000	Bit	Time	Bit	Time
			0000	Disabled	1000	40 min
			0001	5 min	1001	45 min
			0010	10 min	1010	50 min
			0011	15 min	1011	55 min
			0100	20 min	1100	60 min
			0101	25 min	1101	65 min
			0110	30 min	1110	70 min
			0111	35 min	1111	75 min

Name: PMU LCD Timer Register
 Type: Read/Write
 Index: CFH

Bit	Name	Default	Function			
D[7:4]	Reserved	0000	Reserved bits			
D[3:0]	LCDTM[3:0]	0010	Bit	Time	Bit	Time
			0000	Disabled	1000	8 min
			0001	1 min	1001	9 min
			0010	2 min	1010	10 min
			0011	3 min	1011	11 min
			0100	4 min	1100	12 min
			0101	5 min	1101	13 min
			0110	6 min	1110	14 min
			0111	7 min	1111	15 min

VADEM VG-230

SUB-NOTEBOOK ENGINE

DEB-0V MEGAV
HOOBETCH-BUS

Name: PMU LCD Sequence Register
 Type: Read/Write
 Index: D4H

Bit	Name	Default	Function
D[7:5]	Reserved	--	Reserved bits
D4	SEQEN	0	Automatic sequencing enable. When SEQEN bit is set, the VG-230 performs the LCD power up/down sequencing.
D[3:2]	N/U	--	Not used
D[1:0]	Reserved	--	Reserved bits

Name: PMU Resume Status
 Type: Read/Write
 Index: DAH

Bit	Name	Default	Function
D[7:2]	Reserved	00H	Reserved bits
D1	PMUREF	0	Read only bit polled by software to determine the end of the Resume Operation. 1 = PMU Refreshing
D0	CLKSPD	0	CPU Clock speed divider during DOZE or SLEEP mode. 0 = divided by 4; 1 = divided by 8.

Name: PMU Activity Status
 Type: Read Only
 Index: DBH

Bit	Name	Default	Function
D7	IORNGACT	0	Activity to programmable I/O range
D6	VIDACT	0	Video memory activity
D5	HDACT	0	Hard disk I/O activity
D4	FLPACT	0	Floppy I/O activity
D3	COMACT	0	COM1/COM2 activity
D2	RTCACT	0	I/O Address 70-71H activity
D1	KBDACT	0	Keyboard I/O activity
D0	PIOACT	0	LPT1/LPT2/LPT3 I/O activity

Note: The activity status register is cleared following deassertion of the SNEPWRGD signal, or after being read by the CPU.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VG-230 Sub-Notebook Engine CGA LCD Indexed Register Sum- mary

The following registers are implemented in the VG-230 Sub-Notebook Engine to assure IBM CGA compatibility. These registers are accessed through an index and a data register. The index register is at 3D4 and the data register is at 3D5. Both registers are read/write and are shadowed at 3D0/3D1, 3D2/3D3 and 3D6/3D7 respectively. The address is decoded using A0-9 and AEN=0 (the PC/XT uses only A0-9). The 6845 registers R1-R9 are used to program the display characteristics for a CRT. They have no meaning for an LCD and are therefore not implemented here.

Name:	CGA Index Register	Read/Write
Type:	Read/Write	
Address:	3D4	

Note: The Index register is shadowed at 3D0, 3D2 and 3D6

Name:	CGA Data Register	Read/Write
Type:	Read/Write	
Address:	3D5	

Note: The Index register is shadowed at 3D1, 3D3 and 3D7

Name:	Mode Select Register A	Read/Write
Type:	Read/Write	
Address:	3D8H	

Name:	Status Register	Read
Type:	Read	
Address:	3DAH	

Name:	Mode Select Register B	Read/Write
Type:	Read/Write	
Address:	3DEH	

Index	Register	Address	Name	Function
D1	TOACH	0	TOACH	TO Address
D2	TRACT	0	TRACT	TRACT
D3	CWACT	0	CWACT	CW Address
D5	RTACT	0	RTACT	RT Address
D6	KBDGCT	0	KBDGCT	Keyboard Control
D7	LIOACT	0	LIOACT	LIO Address

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

VG-230 Register Indices

The following register indices select among the CGA LCD indexed registers:

<u>REGISTER</u>	<u>INDEX</u>
Cursor Start Raster Register	0AH
Cursor End Raster Register	0BH
Display Start Address MSB Register	0CH
Display Start Address LSB Register	0DH
Cursor Location Address MSB Register	0EH
Cursor Location Address LSB Register	0FH
The following registers control VG-230 extended LCD features: windowing, LCD type, timeout delays, LCD resolution and the ink plane.	
Window Start MSB Register	C0H
Window Start LSB Register	C1H
LCD Display Control Register	C2H
LCD Panel Resolution Register	CAH
LCD Mode Register	CCH
Ink Plane Register	CDH

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: **Cursor Start Raster Register**

Type: **Read/Write**

Index: **0AH**

Bit	Name	Default	Function
D[7:6]	Reserved	00	Not used
D5	*CURON	0	0 = Cursor displayed 1 = Cursor not displayed
D[4:0]	SC[4:0]	00H	Select raster to start cursor 00 = line 0, 01 = line 1, 02 = line 2, etc.

Name: **Cursor End Raster Register**

Type: **Read/Write**

Index: **0BH**

Bit	Name	Default	Function
D[7:5]	Reserved	000	Not used
D[4:0]	EC[4:0]	0H	Select raster to end cursor 00 = line 0, 01 = line 1, 02 = line 2, etc.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VG-230
SUB-NOTEBOOK
ENGINE

Name: **Display Start Address MSB Register**
 Type: **Read/Write**
 Index: **0CH**

Bit	Address
D[7:6]	Not used
D5	13
D4	12
D3	11
D2	10
D1	9
D0	8

Note: Holds the upper byte of address for the character at the upper left corner of a normal CGA display. See Window Start MSB Register.

Name: **Display Start Address LSB Register**
 Type: **Read/Write**
 Index: **0DH**

Bit	Address
D7	7
D6	6
D5	5
D4	4
D3	3
D2	2
D1	1
D0	0

Note: Holds the lower byte of address for the character at the upper left corner of a normal CGA display. See Window Start LSB Register.

Name: **Cursor Location Address MSB Register**
 Type: **Read/Write**
 Index: **0EH**

Bit	Address
D[7:6]	Not used
D5	13
D4	12
D3	11
D2	10
D1	9
D0	8

Note: Holds the upper byte of the cursor location address.

Name: **Cursor Location Address LSB Register**
 Type: **Read/Write**
 Index: **0FH**

Bit	Address
D7	7
D6	6
D5	5
D4	4
D3	3
D2	2
D1	1
D0	0

Note: Holds the lower byte of the cursor location address.

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: **Window Start MSB Register**
Type: **Read/Write**
Index: **C0H**

Bit	Address
D[7:5]	Not used
D4	12
D3	11
D2	10
D1	9
D0	8

Note: The Window Start registers contain the memory address for the upper left corner of the LCD panel. Writes to index 0CH are automatically copied to this register.

Name: **Window Start LSB Register**
Type: **Read/Write**
Index: **C1H**

Bit	Address
D7	7
D6	6
D5	5
D4	4
D3	3
D2	2
D1	1
D0	0

Note: Writes to index 0DH are automatically copied to this register.

Bit	Address
D[7:6]	Not used
D5	15
D4	14
D3	13
D2	12
D1	11
D0	10

Note: High nibble power pins
of the current position
address

VADEM VG-230
SUB-NOTEBOOK
ENGINE

OS-9V MEGAV
 SUB-NOTEBOOK
 ENGINE

Name: LCD Display Control Register
 Type: Read/Write
 Index: C2H

Bit	Name	Default	Function
D[7:6]	ATTBLK[1:0]	00	Controls blink rate for character blink attribute
			Bit 7 Bit 6
			0 0 Steady
			0 1 1/64 frame
			1 0 1/32 frame
			1 1 1/16 frame
D[5:4]	CURBLK[1:0]	00	Controls blink rate for the cursor in conjunction with bit 5 of the Cursor Start Scan Line Register.
			Bit 5 Bit 4
			0 0 Steady
			0 1 1/64 frame
			1 0 1/32 frame
			1 1 1/16 frame
D[3:1]	Reserved	000	Reserved bits
D0	RVVD	0	Reverse video for entire LCD 0 = normal polarity 1 = LCD in reverse video

VADEM VG-230

SUB-NOTEBOOK ENGINE

DE5-DV-ME-320
SUB-NOTEBOOK
ENGINE

Name: LCD Panel Resolution Register
 Type: Read/Write
 Index: CAH

Bit	Name	Default	Function																						
D[7:6]	LCDW[1:0]	00	LCD data bus width 00=4 bit, 01=2 bit, 10=1 bit, 11=not used																						
D[5:0]	LCDR[5:0]	000000	<table> <thead> <tr> <th>LCDR[5:0]</th> <th>Panel Resolution</th> </tr> </thead> <tbody> <tr><td>000000</td><td>640 x 400</td></tr> <tr><td>000000</td><td>640 x 200</td></tr> <tr><td>000010</td><td>640 x 100</td></tr> <tr><td>001001</td><td>480 x 128</td></tr> <tr><td>010001</td><td>240 x 128</td></tr> <tr><td>010011</td><td>240 x 64</td></tr> <tr><td>011001</td><td>128 x 128</td></tr> <tr><td>011011</td><td>128 x 64</td></tr> <tr><td>100000</td><td>320 x 200</td></tr> <tr><td>100101</td><td>320 x 240</td></tr> </tbody> </table>	LCDR[5:0]	Panel Resolution	000000	640 x 400	000000	640 x 200	000010	640 x 100	001001	480 x 128	010001	240 x 128	010011	240 x 64	011001	128 x 128	011011	128 x 64	100000	320 x 200	100101	320 x 240
LCDR[5:0]	Panel Resolution																								
000000	640 x 400																								
000000	640 x 200																								
000010	640 x 100																								
001001	480 x 128																								
010001	240 x 128																								
010011	240 x 64																								
011001	128 x 128																								
011011	128 x 64																								
100000	320 x 200																								
100101	320 x 240																								

Name: Gray Scale Register
 Type: Read/Write
 Index: CBH

Bit	Name	Default	Function															
D[7:4]	Reserved	0H	Reserved bits															
D[3:2]	OPT240[1:0]	00	<table> <thead> <tr> <th>OPT240[1:0]</th> <th>Option</th> <th>Function</th> </tr> </thead> <tbody> <tr><td>00</td><td>Display the 200 CGA lines in the top 200 lines of the panel. Remaining 40 lines are fetched from subsequent memory.</td><td></td></tr> <tr><td>01</td><td>As above, but remaining 40 lines are blanked.</td><td></td></tr> <tr><td>10</td><td>Reserved.</td><td></td></tr> <tr><td>11</td><td>Center the 200 CGA lines in the 240 panel lines. Remaining 40 lines (20 above and 20 below image) are blanked.</td><td></td></tr> </tbody> </table>	OPT240[1:0]	Option	Function	00	Display the 200 CGA lines in the top 200 lines of the panel. Remaining 40 lines are fetched from subsequent memory.		01	As above, but remaining 40 lines are blanked.		10	Reserved.		11	Center the 200 CGA lines in the 240 panel lines. Remaining 40 lines (20 above and 20 below image) are blanked.	
OPT240[1:0]	Option	Function																
00	Display the 200 CGA lines in the top 200 lines of the panel. Remaining 40 lines are fetched from subsequent memory.																	
01	As above, but remaining 40 lines are blanked.																	
10	Reserved.																	
11	Center the 200 CGA lines in the 240 panel lines. Remaining 40 lines (20 above and 20 below image) are blanked.																	
D[1:0]	GRAY[1:0]	00	Selects 1 of 4 color to gray scale mappers.															

VADEM VG-230

SUB-NOTEBOOK ENGINE

OSD-OV MEGAV
NOOBSTOOL-BUS
EMMVAE

Name: LCD Mode Register
Type: Read/Write
Index: CCH

Bit	Name	Default	Function					
D7	SEL60HZ	0	Frame Rate for LCD Widths					
			SEL60HZ	Clock	640;320	480;240	128	
			Value	MHz	Hz	Hz	Hz	
			0	14.3	69	72	67	
			0	16	72	75	70	
			1	14.3	60	62	58	
			1	16	59	62	57	
D6	Reserved	0	Reserved bit					
D[5:3]	DLY[2:0]	000	LCD Sequencing Delay Setting					Sequencing Delay
			DLY2	DLY1	DLY0			
			0	0	0	7.5 ms		
			0	0	1	15 ms		
			0	1	0	30 ms		
			0	1	1	60 ms		
			1	0	0	120 ms		
			1	0	1	240 ms		
			1	1	X	Reserved		
D2	400LINE	0	400 Line select 0 - LCD is 640x200 resolution or lower 1 - LCD is 640x400 lines					
D1	Toshiba	0	1 - Toshiba LOADCLK Timing					
D0	Sharp	0	1 - Sharp LOADCLK Timing					
Note: For physical 400-line panels, the lower 4 data bits to the panel (LCDL[3:0]) must be explicitly enabled using the GPIO Mode Register (index 32H).								

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Name: Ink Plane Register

Type: Read/Write

Index: CDH

Bit	Name	Default	Function
D7	INKEN	0	0 - Disable Ink Plane 1 - Enable Ink Plane When this bit is set and the VG-230 is programmed into 400 line mode, the lower half screen data will be logically superimposed on the upper half screen data to drive the LCDU[3:0] outputs.
D[6:2]	Reserved	0	Reserved bits.
D[1:0]	IMOD[1:0]	00	Selects method of combining upper half screen data and lower half screen data. IMOD1 IMOD0 0 0 - Modulate 0 1 - OR 1 0 - XOR 1 1 - Reserved

Name: Mode Select Register A

Type: Read/Write

Address: 3D8H

0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

VADEM VG-230

SUB-NOTEBOOK ENGINE

VG-230 SUB-
NOTEBOOK ENGINE

Bit	Name	Default	Function
D[7:6]	Reserved	00	Reserved bits
D5	BLINK	0	0 - MSB of Attribute Byte is intensity 1 - MSB of Attribute Byte is blink
D4	GRES0	0	0 - 320x200 APA 1 - 640x200 APA or 640x400 APA
D3	VIDE	0	0 = Video disabled 1 = Video enabled Note: Used by power management logic only, does not actually control video.
D2	Reserved	0	Reserved bit
D1	GRAPH	0	0 = Character mode 1 = Graphics mode
D0	CRES	0	0 = 40x25 Alpha 1 = 80x25 Alpha

Name: Status Register
Type: Read
Address: 3DAH

Bit	Name	Default	Function
D[7:4]	Reserved	FH	Reserved bits
D3	VSYNC	0	Simulated vertical retrace time
D2	Reserved	1	Reserved bit
D1	Reserved	0	Reserved bit
D0	HSYNC	0	Simulated horizontal retrace time

Name: Mode Select Register B
Type: Read/Write
Address: 3DEH

VADEM VG-230
SUB-NOTEBOOK
ENGINE

VADEM VG-230
 SUB-NOTEBOOK
 ENGINE

Bit	Name	Default	Function
D7	Reserved	0	Reserved bit
D6	UNDRLN	0	0 = Underline disabled, grayscaling enabled 1 = Underline enabled, grayscaling disabled
D[5:4]	Reserved	00	Reserved bits
D3	PAGSEL	0	0 = Select low page for display 1 = Select high page for display
D[2:1]	Reserved	00	Reserved bits
D0	GRES1	0	0 = 640x200 APA, two 16K alpha pages. 1 = 640x400 APA, one 32K alpha page.

GRAPH, CRES and GRES[1:0] are used to select the ATT mode.

GRAPH	CRES	GRES1	GRES0	Mode
0	0	X	X	40X25 Alpha
0	1	X	X	80X25 Alpha
1	X	X	0	320X200 APA
1	X	0	1	640X200 APA
1	X	1	1	640X400 APA

VADEM VG-230

SUB-NOTEBOOK ENGINE

Chapter 4

Specifications

Overview

This chapter details the device specifications and characteristics of the VG-230 Sub-Notebook Engine.

Specifications

Processor

Type	V30HL		
Max Input Clock Frequency	32.215905 MHz		
Input Clock Frequencies Supported	32.215905 MHz	28.63636 MHz	
(Maximum)	16.0 MHz (+ 2)	14.3 MHz (+ 2)	
	10.7 MHz (+ 3)	9.54 MHz (+ 3)	
CPU Clock Frequencies	8.00 MHz (+ 4)	7.12 MHz (+ 4)	
(Minimum)	5.33 MHz (+ 6)	4.77 MHz (+ 6)	
	4.00 MHz (+ 8)	3.58 MHz (+ 8)	

Memory

Organization	8 or 16 bit			
Type	DRAM	SRAM	PSRAM	ROM
Density	256Kx1	32Kx8	32Kx8	32Kx8 and Larger
	256Kx4	128Kx8	128Kx8	(Through use of
	256Kx16	512Kx8	512Kx8	memory mapping
	512Kx8			registers).
Max. Number of Banks	6 (8 bit) 6 (16 bit)	8 (8 bit) 6 (16 bit)	7 (8 bit) 6 (16 bit)	
Wait States	0 - 4 (programmable)			

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

I/O

Serial Port	8250 Based. Programmable as COM1 or COM2.
Interrupts	8259 Based. 2 channels available on bus (programmable).
DMA	8237 Based. 1 channel available on bus (programmable).
Timer	8254 Based. Provides Speaker I/F.
RTC	Includes 64 bytes of CMOS RAM.
Expansion	Supported through Single Bus. I/O channel is user-programmable to operate at CPU frequency or 1/2, 1/3, or 1/4 CPU frequency.

Configurable I/O

	<u>Configuration 1</u>	<u>Configuration 2</u>
Keyboard I/F*	Built-in keyboard scanner supporting 8x12 key matrix with 5 dedicated shift keys (101 keys total)	PC/XT compatible two line serial keyboard I/F
Parallel Port	None	PC/XT Compatible. (Requires external parallel data latch)
PC Card I/F	One PCMCIA 2.0 Memory or I/O Card Slot supported	Two PCMCIA 2.0 Memory or I/O Card Slots supported.

*Keyboard I/F itself may be disabled to allow implementation of separate keyboard controller.

VADEM VG-230

SUB-NOTEBOOK ENGINE

DCS-2V MEGAV
HOTSWAP BUSES
ENGINE

Power Management

CPU Clock Control	Divide by 4 or 8 Stop Clock
Power Control Pins (VP Pins)	2 for LCD 1 for PC Cards 1 for RAM 1 for System On/Off
Modes	On, Doze, Sleep, Suspend, and Off
Battery Monitoring	1 level (LB)
Suspend/Resume Control	Via EXT switch, RTC Alarm, Ring Indicator

LCD Controller

Supported Modes	AT&T 400 line Graphics, Double-Scan Text and Graphics, CGA Text and Graphics
Displays Supported	640x400, 640x200, 640x100, 480x128, 320x200, 240x128, 240x64, 128x128, and 128x64

VADEM VG-230

SUB-NOTEBOOK ENGINE

Electrical Characteristics

DC Characteristics

Parameter	Symbol	Min	Max	Units
Supply Voltage		5V +/- 5%		
Input Low Voltage	V _{IL}	-	0.8	volt.
Input High Voltage	V _{IH}	2.0	-	volt.
Output Low Voltage (TTL & CMOS)	V _{OL}	0	0.45	volt.
Output High Voltage (TTL)	V _{OH_T}	2.4	-	volt.
Output High Voltage (CMOS)	V _{OH_C}	3.5	-	volt.
Input Low Current	I _{IL}	-	-200	μ A
Input High Current Vin = 2.4v, Vcc = 5.5v	I _{IH1}	-	20	μ A
Input High Current Vin = 5.5v, Vcc = 5.5v	I _{IH2}	-	200	μ A
Output Short Circuit Current Vo = 0v	I _{os}	-	-100	mA
Input Clamp Voltage II = 020mA, Vcc = 4.5v	V _{IC}	-	-1.5	volt.
Output Leakage Current (Hi-Z)	I _{OLZ1}	-100	100	μ A
Output Leakage Current (Bi-Dir)	I _{OLZ2}	-200	200	μ A
Clock Input Low Voltage	V _{ILC}	-	0.4	volt.
Clock Input High Voltage	V _{ILH}	4.0	-	volt.

Mechanical Specifications

Package 160 pin QFP

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Absolute Maximum Ratings

Case Temperature Under Bias	-25C to +100C
Case Storage Temperature	-40C to +125 C
DC Supply Voltage (VCC)	0 to 7.0V
Voltage to any pin with respect to ground	-0.5V to VCC +0.5V

Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply Voltage (5 volt)	4.75	5.25	V
Freq	Operating Frequency	-	32.216	MHz
Ta	Ambient Temperature	0	70	C

Capacitance DC Specifications

Symbol	Parameter	Min.	Max.	Unit	Note
Cin	Input Capacitance	-	10	pF	1
Cout	Output Capacitance	-	10	pF	1

ICC Specifications

Symbol	Parameter	Typ.	Max.	Unit	Note
ICC ₁	Supply Current @ 8 MHz	60	120	mA	2
ICC ₂	Supply Current @ 16 MHz	90	180	mA	2
ICC ₃	Supply Current under Power Mgmt.	120	240	µA	3

Electrostatic Discharge Characteristics

Symbol	Parameter	Value	Test Condition
Vzap	E.S.D. Tolerance	>2000V	Mil-STD 883 Meth. 3015

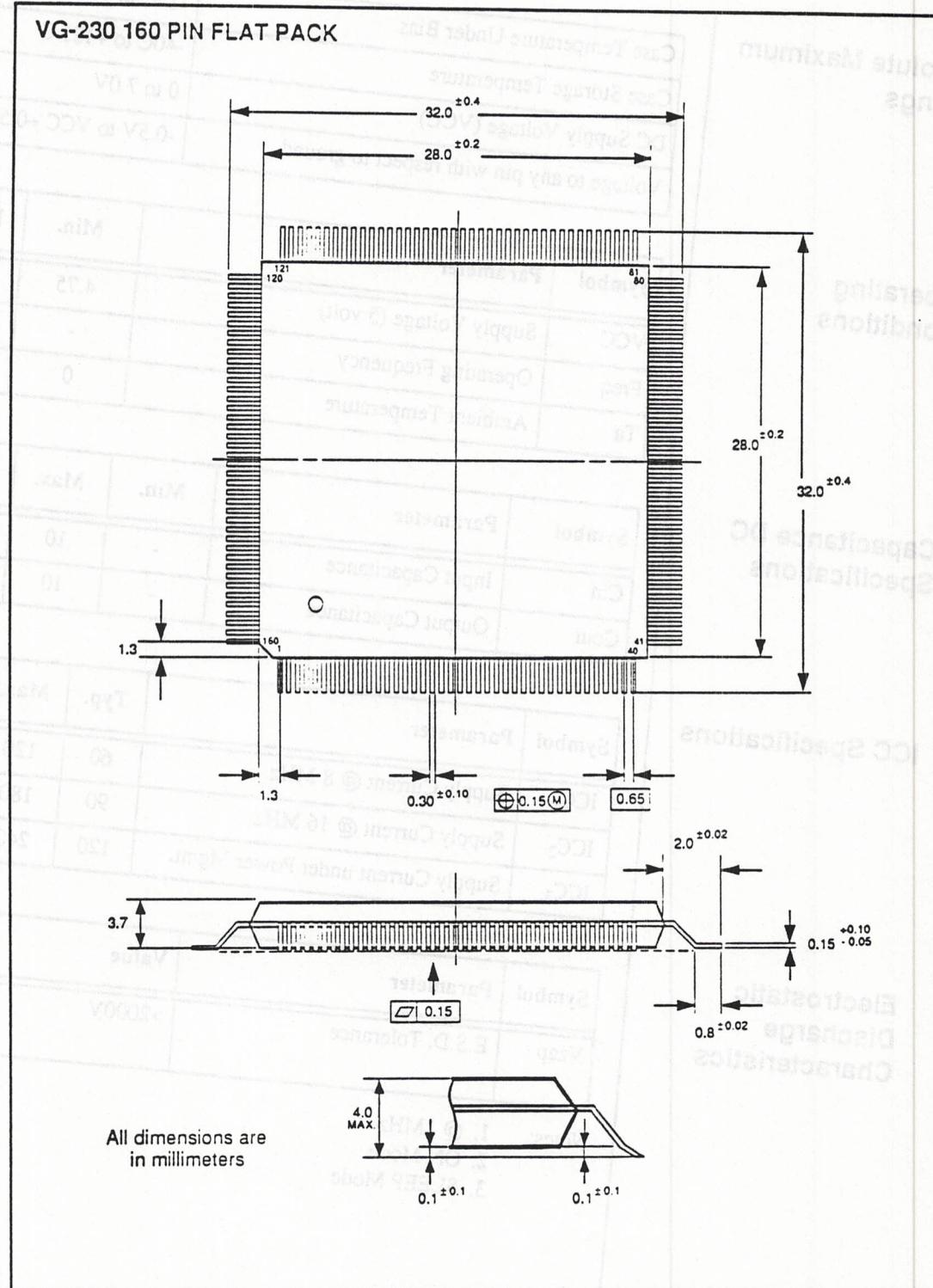
Notes:

1. @ 1MHz
2. ON Mode
3. SLEEP Mode

VADEM VG-230

SUB-NOTEBOOK ENGINE

VG-230
Outline Diagram
Figure 4-1



Memory Cycle
Timing

MEMORY CYCLE TIMING					
		Min	Typ	Max	Unit
T100	ADDR setup to $\overline{CS} \downarrow / \overline{RAS} \downarrow$	5	---	---	ns
T101	\overline{CS} to \overline{OE} delay	---	$1/2$ CPU TCYC	---	ns
T102	\overline{CS} pulse width / \overline{RAS} pulse width	2 CPU TCYC	---	---	ns
T103	Data valid from \overline{OE}	---	---	70	ns
T104	Data valid from \overline{CS}	---	---	104	ns
T105	Data hold from $\overline{CS} / \overline{CAS}$	0	---	---	ns
T106	Data off time from $\overline{CS} / \overline{CAS}$	---	---	$1/2$ CPU TCYC	ns
T107	$\overline{CS} / \overline{RAS}$ precharge	2 CPU TCYC	---	---	ns
T108	Data setup to $\overline{CS} \uparrow$	85	---	---	ns
T109	Data hold from $\overline{CS} \uparrow$	25	---	---	ns
T110	ADR hold from \overline{RAS}	30	---	40	ns
T111	ADR setup to \overline{CAS}	20	---	---	ns
T112	\overline{RAS} to \overline{CAS} delay	---	1 CPU TCYC	---	ns
T113	\overline{CAS} pulse width	1 CPU TCYC	---	---	ns
T114	\overline{RAS} to data valid	---	---	104	ns
T115	\overline{CAS} to data valid	---	---	40	ns
T116	Data setup to $\overline{CAS} \downarrow$	25	---	---	ns
T117	Data hold from $\overline{CAS} \downarrow$	85	---	---	ns
T118	\overline{WE} setup to $\overline{CAS} \downarrow$	25	---	---	ns
T119	ADDR valid to $\overline{ROMCE0}$ or $\overline{ROMCE1}$	0	---	5	ns
T120	\overline{ROMCE} pulse width	2 CPU TCYC	---	---	ns
T121	\overline{ROMCE} to data valid	---	---	108	ns
T122	\overline{CAS} to \overline{RAS} setup (CBR refresh cycle)	---	1 CPU TCYC	---	ns
T123	Pulse width $\overline{REF} / \overline{OE}$ refresh cycle	---	2 CPU TCYC	---	ns
T124	$\overline{REF} / \overline{OE}$ (refresh cycle) to next \overline{CS}	200	---	---	ns
T125	\overline{WE} low to \overline{CE} high	$1/2$ CPU TCYC	---	---	ns

VADEM VG-230

SUB-NOTEBOOK ENGINE

PC Card Memory Cycle Timing

PC CARD MEMORY CYCLE TIMING			
		Min	Max
		Unit	
T201	\overline{CE} valid from ADDRESS	41	---
T202	\overline{OE} valid from ADDRESS	51	---
T203	\overline{CE} pulse width	155	---
T204	ADDRESS hold from \overline{CE}	19	---
T205	$\overline{OE} / \overline{WE}$ pulse width	124	---
T206	CBEN valid from ADDRESS	---	49
T207	CDIR valid from ADDRESS	---	19
T208	Data valid from $\overline{OE} \downarrow$	---	T205-15
T209	Data hold from $\overline{OE} \uparrow$	10	---
T210	Data valid from \overline{CE}	---	15
T211	Data hold from \overline{CE}	5	---
T212	CBEN pulse width	155	---
T213	\overline{WAIT} valid from \overline{CE}	---	50
T214	$\overline{CE} \uparrow$ from $\overline{WAIT} \uparrow$	104	166

PC Card I/O Cycle Timing

PC CARD I/O CYCLE TIMING			
		Min	Max
		Unit	
T215	\overline{CE} pulse width for I/O Access	403	---
T216	$\overline{CE} \downarrow$ to $\overline{SIORD} / \overline{SIOWR} \downarrow$	74	---
T217	$\overline{INPACK} \downarrow$ to $\overline{CBEN} \downarrow$	---	10
T218	$\overline{SIORD} / \overline{SIOWR}$ Pulse width	248	---
T219	ADR valid to $\overline{IOIS16} \downarrow$	---	70
T220	Data valid from $\overline{SIORD} \downarrow$	---	T218-15
T221	Data hold from $\overline{SIORD} \uparrow$	10	---
T222	Data setup from \overline{CE}	---	15
T223	Data hold from \overline{CE}	5	---
T224	\overline{WAIT} delay from \overline{CE}	---	124
T225	$\overline{WAIT} \uparrow$ to $\overline{CE} \uparrow$	124	---

VADEM VG-230
SUB-NOTEBOOK
ENGINE

OC-IV MEGAV
 XGEGSTOM-BUS
 ENGINE

**DMA Cycle
 Timing**

DMA CYCLE TIMING			
		Min	Max
		Unit	
T301	AEN to ADDRESS valid	---	125
T302	AEN to DACK delay	---	65
T303	ADDRESS valid to $\overline{\text{SIORD}} / \overline{\text{SMRD}}$	63	---
T304	ADDRESS valid to $\overline{\text{SIOWR}} / \overline{\text{SMWR}}$	190	---
T305	$\overline{\text{SIORD}} / \overline{\text{SIOWR}} / \overline{\text{SMRD}} / \overline{\text{SMWR}}$ to IOCHRDY	---	25
T306	IOCHRDY release to $\overline{\text{SIOWR}} / \overline{\text{SMWR}} \uparrow$	144	---
T307	$\overline{\text{SIORD}} / \overline{\text{SMRD}}$ hold from $\overline{\text{SIOWR}} / \overline{\text{SMWR}}$	59	---
T308	DRQ hold from DACK	0	---
T309	ADDRESS hold from $\overline{\text{SIORD}} / \overline{\text{SMRD}}$	105	---
T310	DACK hold from $\overline{\text{SIORD}} / \overline{\text{SMRD}}$	65	---
T311	AEN hold from DACK	26	---

XT Bus Timing

XT BUS TIMING			
		Min	Max
		Unit	
T400	ADR setup to $\overline{\text{SIORD}} / \overline{\text{SIOWR}}$, $\overline{\text{SMRD}} / \overline{\text{SMWR}}$	107	---
T401	Pulse width $\overline{\text{SIORD}} / \overline{\text{SIOWR}}$, $\overline{\text{SMRD}} / \overline{\text{SMWR}}$	248	---
T402	ADR hold from $\overline{\text{SIORD}} / \overline{\text{WR}}$, $\overline{\text{SMRD}} / \overline{\text{MWR}}$	99	---
T403	Data valid from $\overline{\text{SIORD}} / \overline{\text{SMRD}}$	---	T401-15
T404	Data hold from $\overline{\text{SIORD}} / \overline{\text{SMRD}}$	10	---
T405	Data setup to $\overline{\text{SIOWR}} / \overline{\text{SMWR}}$	35	---
T406	Data hold from $\overline{\text{SIOWR}} / \overline{\text{SMWR}}$	79	---

**IOCHRDY
 Timing**

IOCHRDY TIMING			
		Min	Max
		Unit	
T407	IOCHRDY delay from $\overline{\text{SIORD}} / \overline{\text{SIOWR}}$, $\overline{\text{SMRD}} / \overline{\text{SMWR}}$	---	25
T408	$\overline{\text{SIORD}} / \overline{\text{SIOWR}}, \overline{\text{SMRD}} / \overline{\text{SMWR}}$ delay from IOCHRDY	144	---

**Keyboard
 Timing**

KEYBOARD TIMING			
		Min	Max
		Unit	
T500	Data setup to KEYCLK \downarrow	10	---
T501	Data hold to KEYCLK \downarrow	5	---

VADEM VG-230

SUB-NOTEBOOK ENGINE

LCD Timing

LCD TIMING				
		Min	Max	Notes
T600	SHCLK high time	3T	---	1
T601	SHCLK low time	3.5T	---	2
T602	SHCLK cycle time	6.5T	6.5T	2
T603	LOCLK width, generic timing	3T	---	3
	LOCLK width, Sharp timing	2.5T	---	3
	LOCLK width, Toshiba timing	5T	---	3
T604	M delay	---	20ns	---
T605	FRAME setup	800ns	---	---
T606	FRAME hold	800ns	---	---
T607	DATA setup	4.5T	---	---
T608	DATA hold	2T	---	---
T609	Toshiba load delay	2T	---	---
T610	Shift to load delay	0.5T	---	---
T611	Sharp load to shift delay	0.5T	---	---
T612	Power sequencing delay	7.5ms	250ms	4

Notes:

1. T is the video clock period T_v multiplied by a factor which is a function of LCD resolution as shown in Table 1.
2. These times are dependent on the SEL60HZ and CLK14/*16 bits. Alternate cycles are lengthened by the number of T units shown in Table 2.
3. These times are dependent on the SEL60HZ and CLK14/*16 bits, and are lengthened by the number of T units shown in Table 2.
4. See table in LCD Mode Register description.

LCD Resolution	T, periods
640 x 200	1
640 x 100	
480 x 128	2
320 x 200	
240 x 64	
128 x 128	
240 x 128	4
128 x 64	

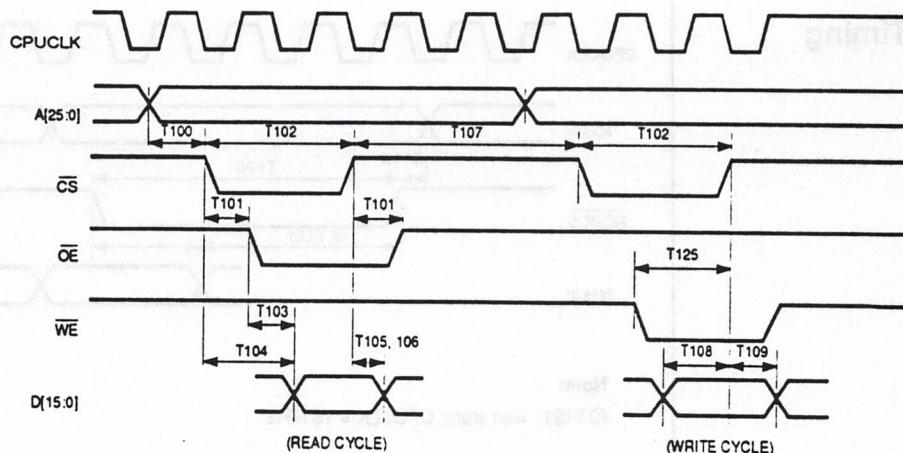
SEL60HZ	CLK14/*16	Add. Time
0	0	1T
0	1	0
1	0	4T
1	1	2T

Table 2

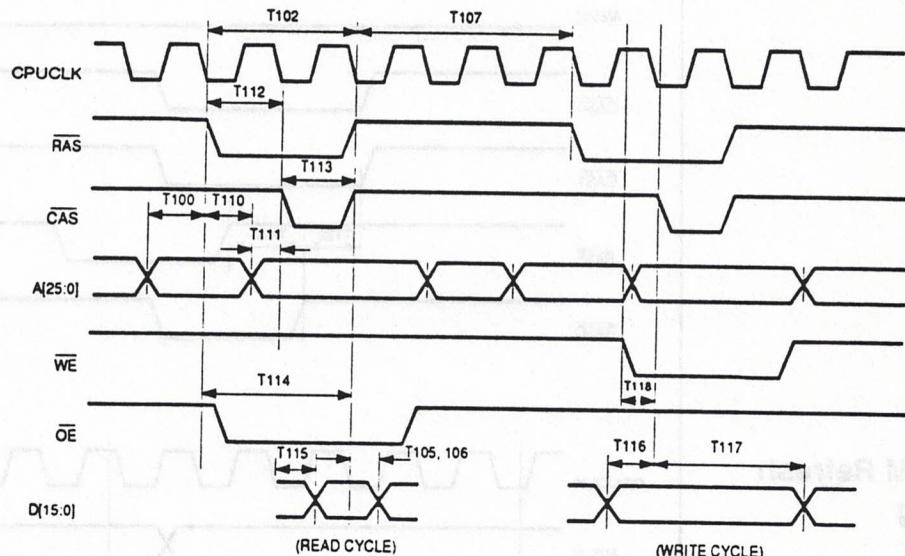
Table 1

Memory Cycle Timing SRAM / PSRAM

The following are timing diagrams for VG-230 functions.



DRAM Timing

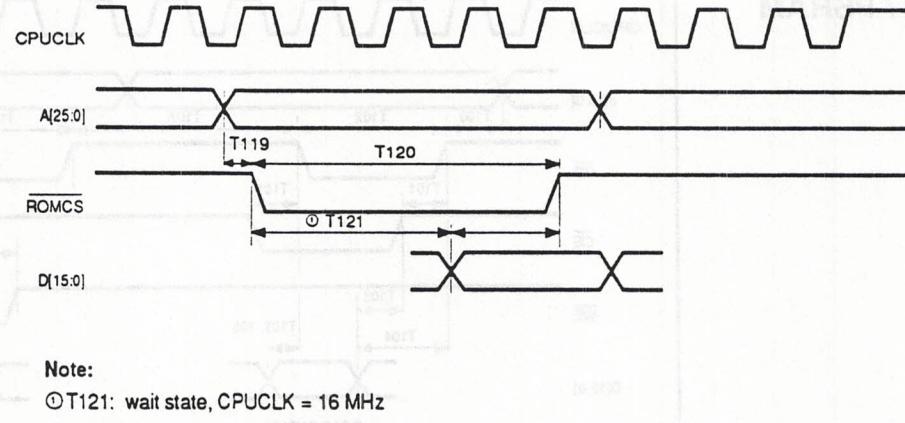


(CPUCLK for reference only)

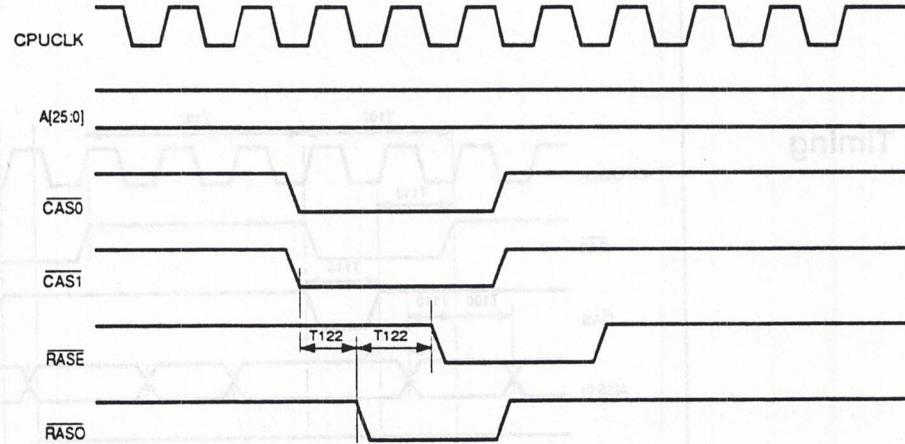
VADEM VG-230

SUB-NOTEBOOK ENGINE

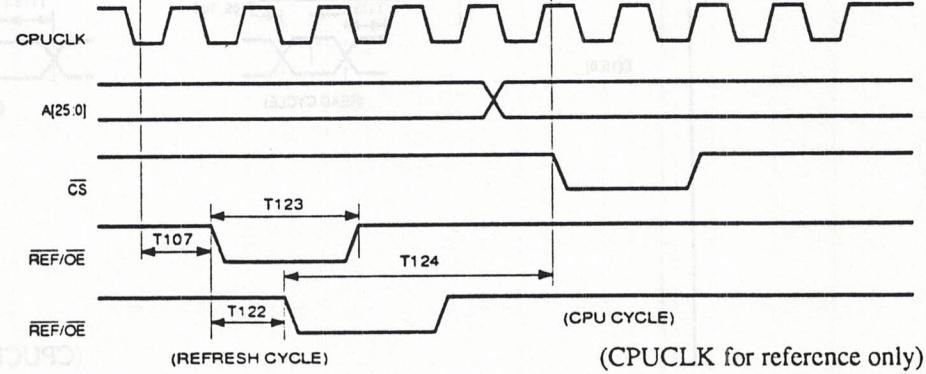
ROM Timing



DRAM Refresh Timing



PSRAM Refresh Timing



(CPU CLK for reference only)

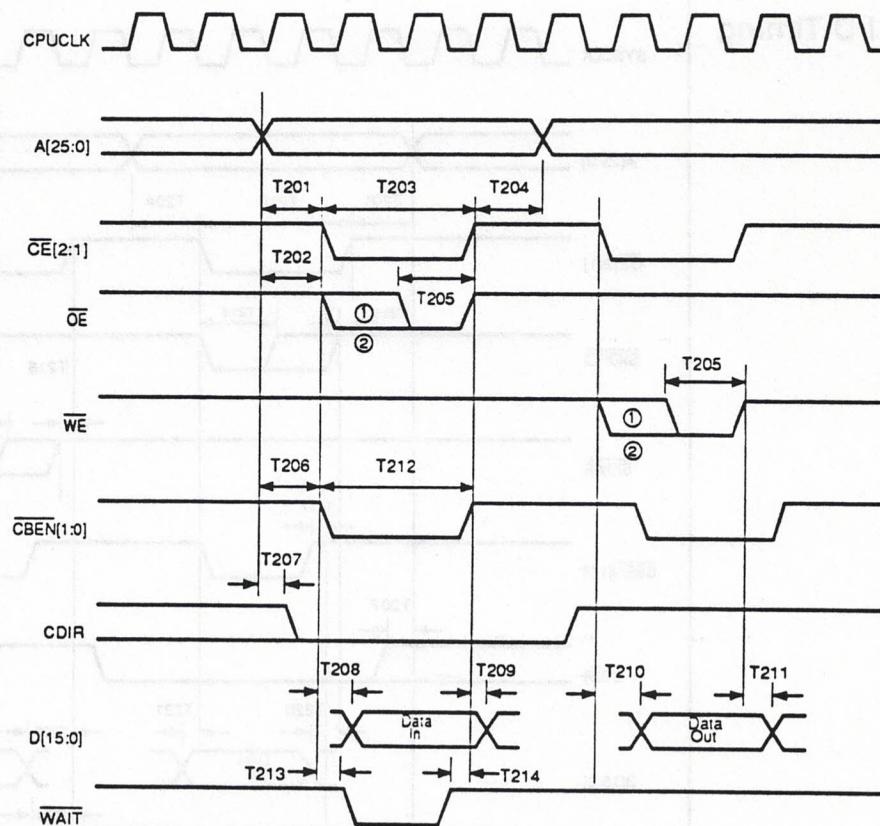
VADEM VG-230

SUB-NOTEBOOK ENGINE

020-MEGAV
X008704-BUS
B4013

PC Card

PC Card Memory Timing



Notes:

- ① $\overline{OE}/\overline{WE}$ may be delayed 0, 1, 2, or 3 clocks from the falling edge of \overline{CE} under software control.
- ② When enabling $\overline{OE}/\overline{WE}$ command delay, an additional number of wait states are added to the PC Card Memory cycle to match the $\overline{OE}/\overline{WE}$ delay value.

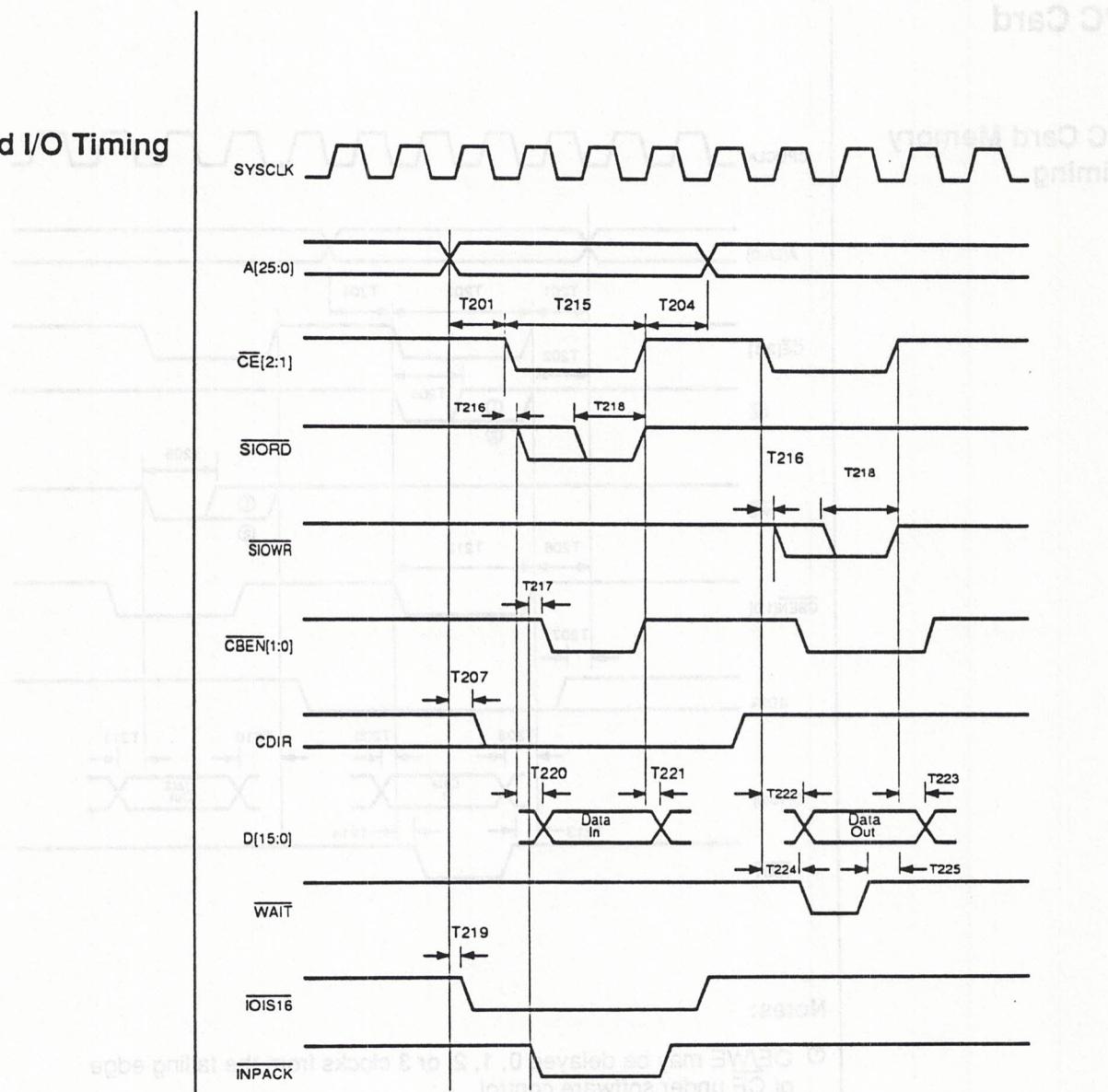
(CPUCLK for reference only)

VADEM VG-230

SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

PC Card I/O Timing



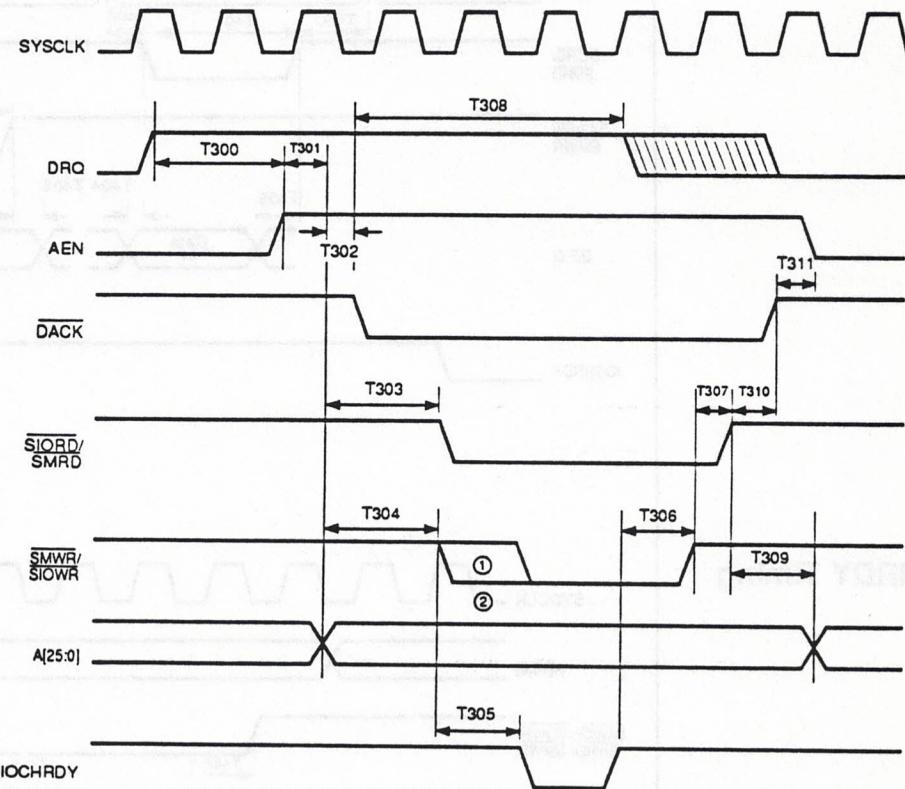
(SYSCLK for reference only)

VADEM VG-230

SUB-NOTEBOOK ENGINE

DE5-ov-MEDAV
HOOBETOM-BUS
THERM

DMA Timing



Notes:

- ① SIOWR/SMWR leading edge may be delayed 0, 1, 2, or 3 clocks after the leading edge of SIORD/SMRD.
- ② For all DMA cycles, SIOWR/SMWR is active for at least 3 clock cycles.

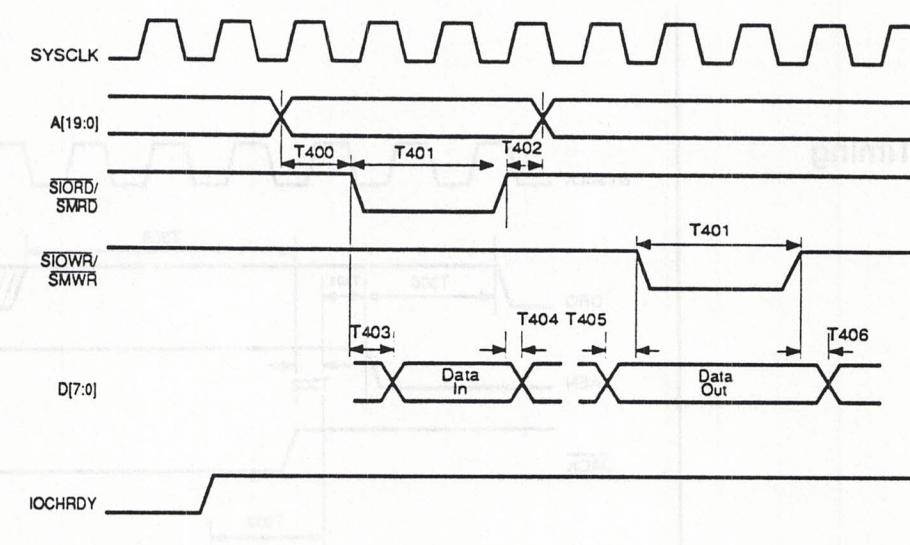
(SYSCLK for reference only)

VADEM VG-230

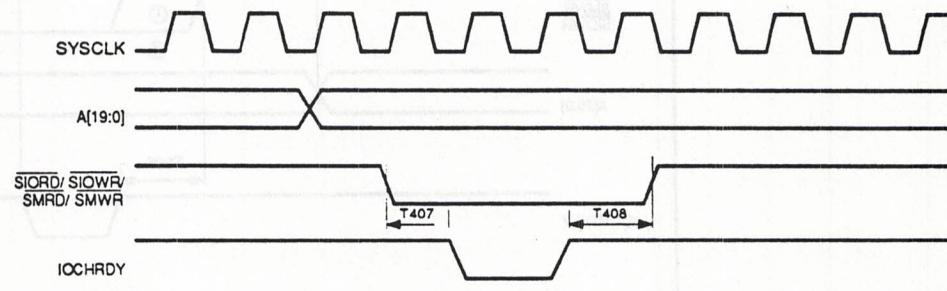
SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

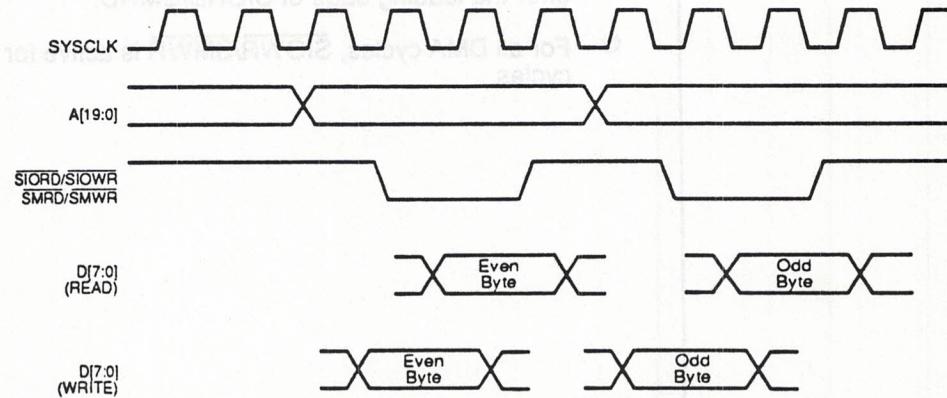
XT Bus Timing



IOCHRDY Timing



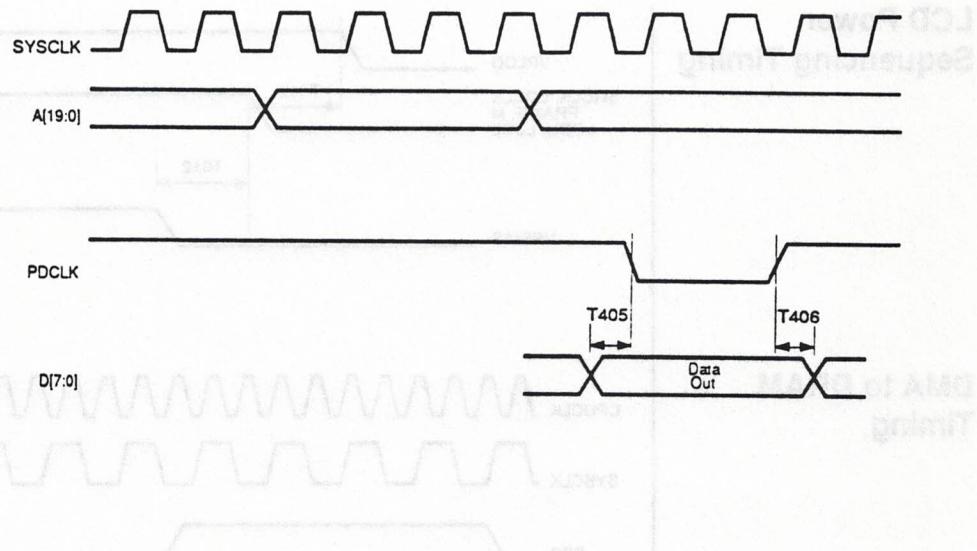
Data Router (16 Bit)



(SYSCLK for reference only)

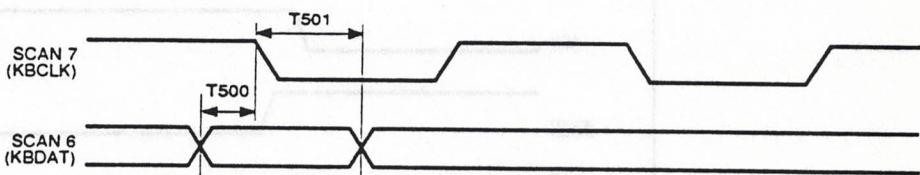
VADEM VG-230
SUB-NOTEBOOK
ENGINE

PIO Timing



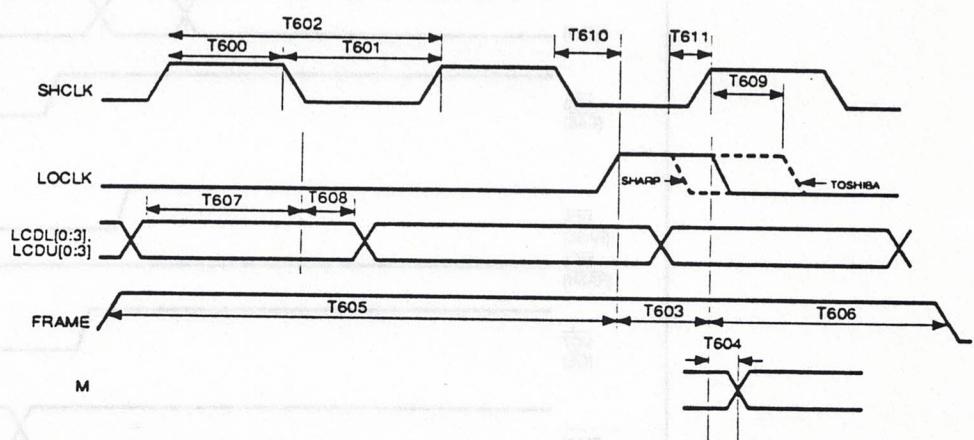
Keyboard

XT Serial I/F Timing



LCD

LCD Interface Timing



(Vice Governor of the Bank of Indonesia)

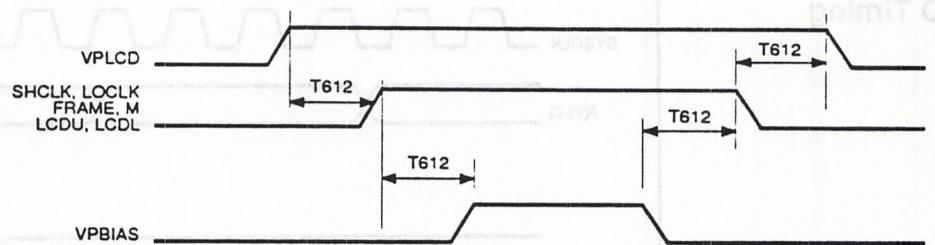
(SYSCLK for reference only)

VADEM VG-230

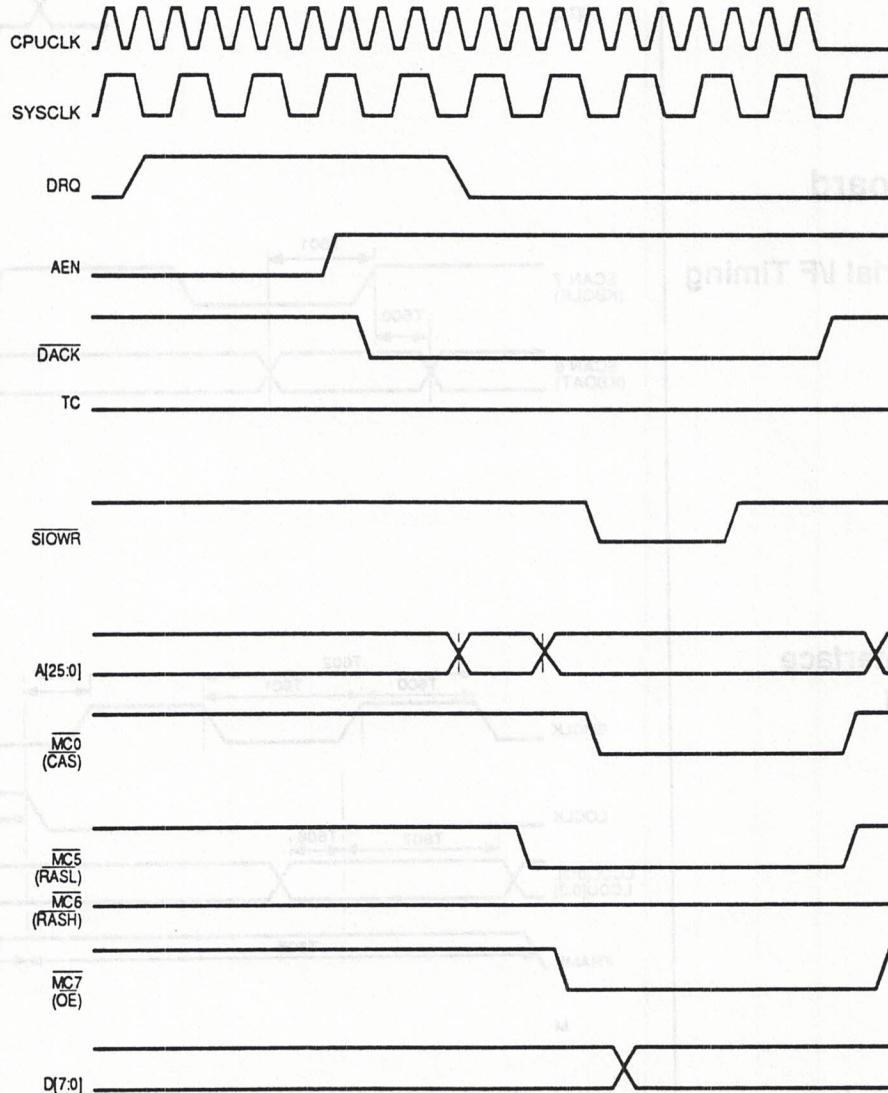
SUB-NOTEBOOK ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

LCD Power Sequencing Timing



DMA to DRAM Timing



(CPUCLK for reference only)

VADEM VG-230
SUB-NOTEBOOK
ENGINE

000-00000000
VADEM VG-230
SUB-NOTEBOOK
ENGINE

**A.C. Test
Conditions**

Output Load	I(load) = $\pm 200 \mu\text{A}$ C(load) = 50pF
Input Rise and Fall Times	5 ns. maximum
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference level	Inputs: 1V and 2V Outputs: 0.8 V and 2 V

VADEM VG-230
SUB-NOTEBOOK
ENGINE

VADEM VG-230
SUB-NOTEBOOK
ENGINE

Au 000 Au
(long) = 300 mm
(C Long) = 20mm

Outer Face

A.C. Jet
Conditions

Input Power 250Watt

VAC or VCA

Input Power 12V

VS max V1
VS max V2.0
Oblongs

Timing Measurement
Revolutions/min



1885 Lundy Avenue
San Jose, California 95131
Tel 408-943-9301
Fax 408-943-9735

The information and specifications contained herein are subject to change without notice.
All trademarks referred to herein are the property of their respective owners.