

TM8100A

Advanced 386SX Palmtop Single Chip

TECHNICAL REFERENCE MANUAL

Rev. 1.0

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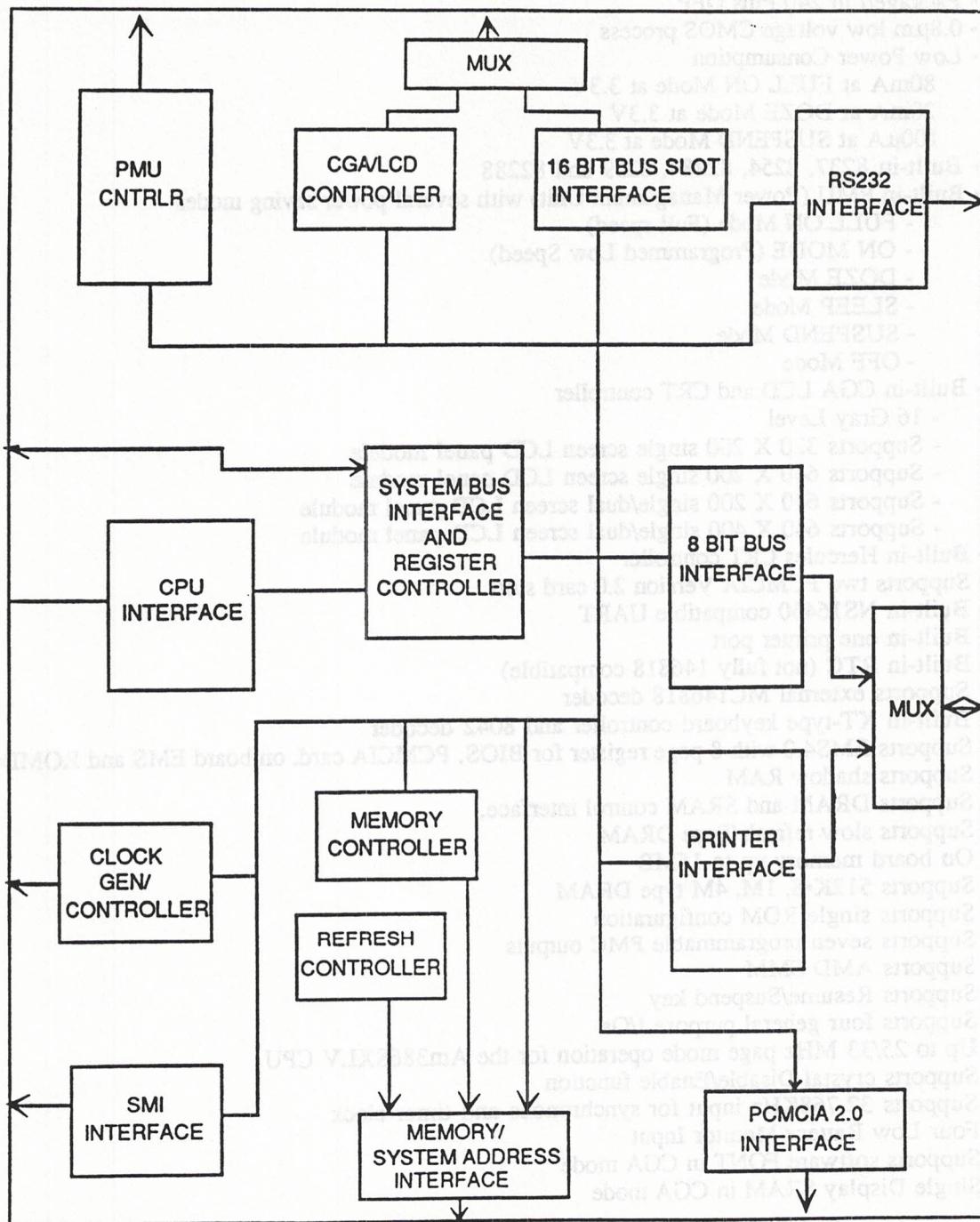
TABLE OF CONTENTS

Features	3
TM8100A Internal Block Diagram	4
System Block Diagram	
Palmtop System Block Diagram	5
Notebook System Block Diagram	6
Mechanical Specifications	
As function sequence.....	7
As pin number sequence.....	8
Pins Descriptions	9
CPU Interface.....	9
System Interface	9
Memory Interface.....	10
PCMCIA Interface.....	11
SMI Interface.....	11
Display Interface.....	12
RS-232 Interface.....	12
Keyboard & RTC Interface.....	13
Power Management Control Unit Interface.....	13
Printer Interface.....	13
Miscellaneous Interface	14
Multiplexing in the TM8100A.....	14
Functional Description	15
1.0 Memory.....	15
1.1 Memory Controller	15
1.2 Shadow RAM	16
1.3 EMS Memory Operation	16
1.4 ROM Control.....	17
2.0 CLK Control.....	17
3.0 Power Management Unit	18
3.1 Power Saving Mode Flow Chart.....	20
3.2 Power Management Control Register	20
3.3 Power Management Control Pin (PMC)	21
3.4 SMM Function	21
3.4 General Purpose I/O Pins.....	22
3.5 Suspend Input Pin	22
3.6 ACIN Pin	22
3.7 Battery Low Detect	22
3.8 Other Power Saving Features	23
4.0 Display Controller.....	23
5.0 UART	23
6.0 Printer.....	24
7.0 Internal RTC	24
8.0 PCMCIA	24
9.0 Register descriptions	26
10.0 LCD Controller Register Description	60
10.1 Access to Display Registers	60
10.2 Memory Map	60
10.3 Color Mapping	63
11.0 6845 Registers	66

FEATURES

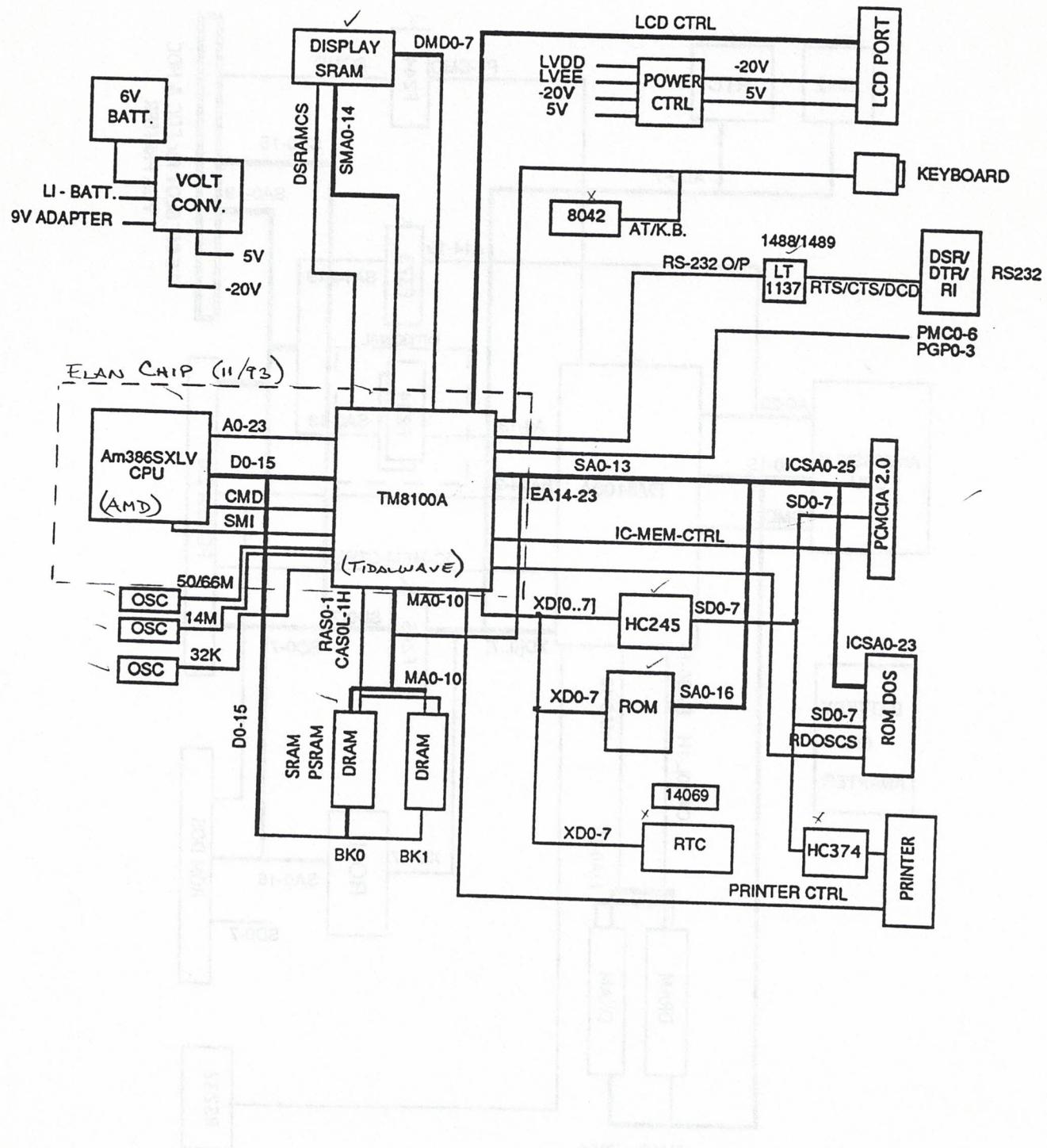
- Fully compatible With IBM PC/AT
- Supports AMD Am386SXLV CPU
- System operation voltage from 3.3V to 5.5V
- Packaged in 240 Pins QFP
- 0.8 μ m low voltage CMOS process
- Low Power Consumption
 - 80mA at FULL ON Mode at 3.3V
 - 20mA at DOZE Mode at 3.3V
 - 100 μ A at SUSPEND Mode at 3.3V
- Built-in 8237, 8254, 82284, 8259 and 82288
- Built-in PMU (Power Management Unit) with several power saving modes
 - FULL ON Mode (Full speed)
 - ON MODE (Programmed Low Speed)
 - DOZE Mode
 - SLEEP Mode
 - SUSPEND Mode
 - OFF Mode
- Built-in CGA LCD and CRT controller
 - 16 Gray Level
 - Supports 320 X 200 single screen LCD panel module
 - Supports 640 X 200 single screen LCD panel module
 - Supports 640 X 200 single/dual screen LCD panel module
 - Supports 640 X 400 single/dual screen LCD panel module
- Built-in Hercules CRT controller
- Supports two PCMCIA Version 2.0 card slots
- Built-in NS16450 compatible UART
- Built-in one printer port
- Built-in RTC (not fully 146818 compatible)
- Supports external MC146818 decoder
- Built-in XT-type keyboard controller and 8042 decoder
- Supports EMS4.0 with 8 page register for BIOS, PCMCIA card, on board EMS and ROMDOS access
- Supports shadow RAM
- Supports DRAM and SRAM control interface.
- Supports slow refresh Type DRAM
- On board memory up to 16MB
- Supports 512K*8, 1M, 4M type DRAM
- Supports single ROM configuration
- Supports seven programmable PMC outputs
- Supports AMD SMM
- Supports Resume/Suspend key
- Supports four general purpose I/Os
- Up to 25/33 MHz page mode operation for the Am386SXLV CPU
- Supports crystal Disable/Enable function
- Supports 32.768KHz input for synchronous and timer clock
- Four Low Battery Monitor Input
- Supports software FONT in CGA mode
- Single Display SRAM in CGA mode

TM8100A INTERNAL BLOCK DIAGRAM



SYSTEM BLOCK DIAGRAM

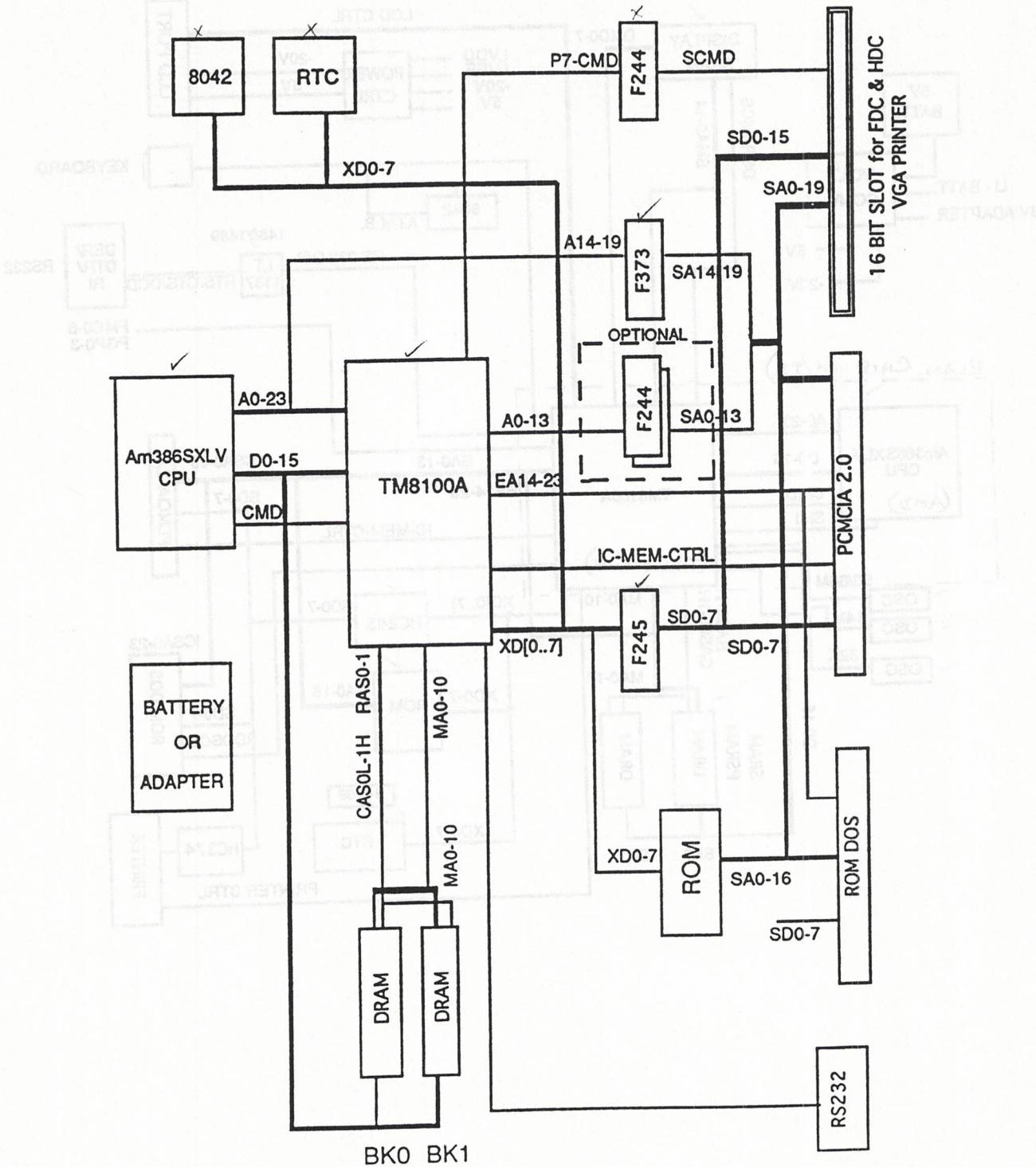
Palmtop System Block Diagram



Notebook System Block Diagram

SYSTEM BLOCK DIAGRAM

Notebook System Block Diagram



As pin number sequence

1	GND	VCC	239
2	X14MIN	X32MIN	238
3	BHE	CASHT	237
4	DSMA0/A17	CASIL	236
5	DSHA1/LA16	CASOH	235
6	DSHA2/LA19	CASOL	234
7	DSMA3/LA20	BAW	233
8	DSMA4/LA21	GND	232
9	DSMA5/LA22	RAS1	231
10	DSMA6/LA23	RAS0	230
11	BHE	MCE2/WP1/IC-HDC	229
12	D1	BV012/SPKP	228
13	D2	REG2/BV011/STSC	227
14	D3	REG1	226
15	D4	WAIT	225
16	D5	VPP1	224
17	D6	RDY1/IC-B0	223
18	D7	CD1	222
19	D8	SPKR	221
20	D9	MA10/SSA13	219
21	D10	MA1/SSA23	218
22	D11	MA1/SSA20	216
23	D12	MA1/SSA19	215
24	D13	MA1/SSA18	214
25	D14	MA1/SSA17	213
26	D15	MA1/SSA16	212
27	A23	MA2/SSA15	208
28	A22	MA2/SSA14	207
29	A21	MA0/SSA12	206
30	A20	DTR	205
31	A19	RTS	204
32	A18	SCUT	203
33	A17	DSR	202
34	A16	DOO	201
35	GND	GND	199
36	VCC	FIN	198
37	GND	CTS	197
38	VCC	SPCLK	196
39	GND	PHC1	195
40	VCC	PHC2	194
41	A15	PMCO	193
42	A14	ACK/RQ12	192
43	A13	ERROR/RQ10	190
44	A12	SUSPEND	189
45	A11	BL4	179
46	A10	BL3	178
47	A9	BL2	177
48	A8	BL1	176
49	A7	LVDD/PMC3	175
50	A6	LVEE	174
51	A5	LPH1	173
52	A4	LPH2	172
53	A3	PGP0	171
54	A2	PGP1	170
55	ADS	BALE	169
56	A15	IOCHRDY/IC-WAIT	168
57	A14	TC	167
58	A13	AEN	166
59	A12	-REFRESH	165
60	A11	DACK2	164
61	A10	DRC2	163
62	A9	'SMEMW	162
63	A8	'SMEMR	161
64	A7	-X1OW	160
65	A6	-X1OR	159
66	A5	SYSCLK/PMC6	158
67	A4	OSC3.5M	157
68	A3	SUSPEND	156
69	A2	RESETIN	155
70	A1	BRESET	154
71	GND	GND	153
72	VCC	XD0	152
73	GND	GND	151
74	VCC	VCC	150
75	GND	XD1	149
76	VCC	XD2	148
77	GND	XD3	147
78	VCC	XD4	146
79	GND	XD5	145
80	VCC	XD6	144
81	GND	XD7	143
82	VCC	SDD0IRL	142
83	GND	EPCS	141
84	VCC	GND	140
85	GND	RDOSCS	139
86	VCC	SA0	138
87	GND	SA1	137
88	VCC	SA2	136
89	GND	SA3	135
90	VCC	VCC	134
91	GND	SA4	133
92	VCC	GND	132
93	GND	SA5	131
94	VCC	SA6	130
95	GND	SA7	129
96	VCC	SA8	128
97	GND	GND	127
98	VCC	SA9	126
99	GND	SA10	125
100	VCC	SA11	124
101	GND	SA12	123
102	VCC	PGP2/	122
103	GND	OSC14	121
104	VCC	GND	120
105	GND	X32KIN	119
106	VCC	X32KOUT	118
107	GND	KBDAT/8042CS	117
108	VCC	A20GATE	116
109	GND	RC	115
110	VCC	IR08	114
111	GND	IR06	113
112	VCC	IR03	112
113	GND	IR01	111
114	VCC	RC	110
115	GND	IR08	109
116	VCC	IR06	108
117	GND	IR04	107
118	VCC	IR02	106
119	GND	IR00	105
120	VCC	IR05	104

PINS DESCRIPTIONS

CPU Interface:

Pin Name	Pin No.	I/O	Function	U/D	Drive
D0-D15	5-20	B	Data from/to Am386SXLV CPU		4
A0	47	I	Address from CPU	D	
A1-A12	48,45-35	B	Address from CPU		4
A13-A15	34-32	B	Address from CPU		1
A16-A19	28-25	B	Address from CPU		1
A20-A23	24-21	I	Address from CPU	D	
W/R#	55	I	CPU status signal inputs	U	
D/C#	56	I	CPU status signal inputs	U	
MIO#	57	I	CPU status signal inputs	U	
ADS#	46	I	CPU address strobe	U	
HOLD	3	O	CPU hold request		1
HLDA	4	I	CPU hold acknowledge		
INTR	50	O	Interrupt Request to CPU		1
CLK2	59	O	Clock output to CPU		16
READY#	2	O	Ready output to CPU		8
RESCPU	52	O	Reset output to CPU		2
NMI	51	O	Non maskable interrupt output to CPU		1
BHE#	65	I	Bus High Enable	U	
SMI#	49	B	System management interrupt		2
SMIRDY#	54	O	SMI ready		2
SMIADS#	53	I	SMI address status	U	

System Interface:

Pin Name	Pin No	I/O	Function	Second Function	U/D	Drive
SA0	138	O	System address 0-3			16
SA1-SA4	137-135,133	B	System address 4	ISD [8:11]		8
SA5-SA8,SA12	131-128 123	B	System address 5-8	ISD [12:15], WPB		8
SA9-SA11	126-124	O	System address 9-12	ICDIR, MCEAH, MCEBH		16
SA13	219	O	System Address 13	MA10		8
SA14-SA17	206-209	O	System Address 14-17	MA0-3		8
SA18-SA21	212-215	O	System Address 18-21	MA4-7		8
SA22-SA23	217-218	O	System Address 22-23	MA8-9		8
SYSCLK	158	O	System Clock	PMC6, WPB, RDYB		
XD0-XD7	152, 149-143	B	System Data			8
IR1	114	I	IRQ 1		U	
IR3	113	I	IRQ 3		U	
IR6	112	I	IRQ		U	
IR8#	111	I	IRQ 8		D	
OSC3.5M	157	O	OSC3.5M	MDDIR		2
DAK2#	164	O	DMA acknowledge 2			2
DRQ2	163	I	DMA request 2		D	
AEN	166	O	DMA address enable			4
TC	167	O	Terminal count			2
DAK1#	187	B	DMA acknowledge 1	Printer's AFD#		4

System Interface Continued:

Pin Name	Pin No.	I/O	Function	2nd Function	U/D	Drive
DRQ1	188	I	DMA request 1	Printer's PE	U	
IRQ11	190	I	IRQ 11	Printer's SLCT	U	
IRQ12	192	I	IRQ 12	Printer's ACK	U	
IOCHCK#	185	B	I/O Channel Check	Printer's 3BCW		1
ENDIRL	142	O	SD Bus Direction Control			1
IOCHRDY	168	I	IO Channel Ready		U	
OSC14M	122	O	14M clock output	PGP2		4
BALE	169	O	Address Latch Enable			4
XIOR#	159	O	I/O Read Command			8
XIOW#	160	O	I/O Write Command			8
SMEMR#	161	O	Memory Read Command.			8
SMEMW#	162	O	Memory Write Command			8
BRESET	154	O	System reset			4
REFRESH#	165	O	Refresh			2
IRQ4	99	I	IRQ 4	D10 for LCD, BVDB1		4
IRQ5	98	I	IRQ 5	D11 for LCD, RDYB		4
IRQ7	189	I	IRQ 7	Printer's BUSY	U	
IRQ9	97	I	IRQ 9	D12 for LCD, BVDB2		4
IRQ10	191	I	IRQ 10	Printer's ERROR	U	
IRQ14	95	I	IRQ 14	DSCE#- display, BVDB2		2
IRQ15	104	I	IRQ 15	M-alternate for LCD		4
LA17-LA23	66-73	O	LA 17-23	DSMA0-6- display		2
SD9-SD15	82-89	B	System Data 8-15	DSMD0-7- display		8
DRQ0	103	I	DMA request 0	DO/I- display		4
DRQ3	93	I	DMA request 3	DSWE#- display		4
DRQ5	102	I	DMA request 5	DO/R- display		4
DRQ7	100	I	DMA request 7	DO/B- display		4
DAK0#	73	O	DMA ACK 0	DSMA7- display		2
DAK5#	75	O	DMA ACK 5	DSMA8- display		2
DAK6#	76	O	DMA ACK 6	DSMA9- display		2
DAK7#	77	O	DMA ACK 7	DSMA10- display		2
MEMR#	78	B	Memory Read	DSMA11		
MEMW#	79	B	Memory Write	DSMA12		
MEMCS16#	80	O	Memory Chip Select 16bit	DSMA13		
MIOCS16#	81	O	I/O Chip Select 16-bit	DSMA14		

Memory Interface:

Pin Name	Pin No.	I/O	Function	2nd Function	U/D	Drive
RAS0#	230	O	DRAM RAS0			8
RAS1#	231	O	DRAM RAS0			8
CAS1L#	236	O	DRAM CAS1L	SRAM bank 0 CS		4
CAS1H#	237	O	DRAM CAS1H.	SRAM bank 1 CS		4
CAS0L#	234	O	DRAM CAS1L	SRAM bank 2 CS		4
CAS0H#	235	O	DRAM CAS1H	SRAM bank 3 CS		4
MA0-3	206-209	O	Memory address bit 0-3	SA[14-17]		8
MA4-7	212-215	O	Memory address bit 4-7	SA[18-21]		8
MA8-9	217-218	O	Memory address bit 8-9	SA[22-23]		8
MA10	219	O	Memory address bit 10	SA13		8
BMW#	233	O	Memory Write			2
NDOS#	139	O	ROM DOS chip select			2
NEPS#	141	O	EPROM address 0			2

PCMCIA Interface:

Pin Name	Pin No.	I/O	Function	2nd Function	U/D	Drive
MCEAL#	222	O	Socket A Low byte Enable			1
VPPA	224	O	Socket A VPP Control output			2
REGA#	226	O	Socket A REG Control output			1
CDA#	221	I	Socket A Card detector input			
WAITA#	225	I	Socket A WAIT input			
RDYA	223	I	Socket A Ready input			
WPA	229	B	Card write protect	MCEBL		2
BVDA2#	228	I	Socket A BVD2			
BVDA1#	227	B	Socket A BVD1	REGB		4
ISD8-ISD11	137-135,133	B	ISD 8-11	SA1-SA4		8
ISD12-ISD15	131-128	B	ISD 12-15	SA5-SA8		8
MCEBL#	229	O	Socket B low byte enable	WPA		2
MCEAH#	125	O	Socket A high byte enable	SA10		16
MCEBH#	124	O	Socket B high byte enable	SA11		16
WPB	123	B	Card B write protect	SA12		8
WPB	158	B	Card B write protect	System Clock		4
REGB#	175	O	Socket B REG Control Output	LVDD-display, PMC3		2
REGB#	227	O	Socket B REG Control Output	BVDA1#		4
WPA	196	B	Card write protect	SPCLK-UART		2
BVDB1	99	B	Socket B BVD1	D10-display, IRQ4		4
BVDB1	106	B	Socket B BVD1	CP1/HDRV-display, PMC4		4
BVDB1	97	B	Socket B BVD1	D12-display, IRQ9		4
RDYB	98	B	Socket B Ready Input	D11-display, IRQ5		4
RDTB	105	B		CP2/VD0-display, PMC5		4
VPPB	96	O	Socket B VPP control output	D13-display, SBHE		4

SMI Interface:

Pin Name	Pin No.	I/O	Function	2nd Function	U/D	Drive
SMI#	49	B	System management interrupt			2
SMIRDY#	54	O	SMI ready			2
SMIADS#	53	I	SMI address status		U	

Display Interface:

Pin Name	Pin No.	I/O	Function	2nd Function	U/D	Drive
DSMD0-7	82-89	B	Display SRAM data bit 0-7	System data 8-15		8
DSMA0-6	66-72	O	Display SRAM address 0-6	LA17-23		2
DSMA7	73	O	Display SRAM address 7	DACK 0#		2
DSMA8	75	O	Display SRAM address 8	DACK 5#		2
DSMA9	76	O	Display SRAM address 9	DACK 9#		2
DSMA10	77	O	Display SRAM address 10	DACK 7#		2
DSMA11	78	O	Display SRAM address 11	MEMR		4
DSMA12	79	O	Display SRAM address 12	MEMW		4
DSMA13	80	B	Display SRAM address 13	MEMCS16		2
DSMA14	81	B	Display SRAM address 14	IOCS16		2
DSWE#	93	B	Display SRAM write	DRQ3		2
DSOE#	94	O	Display SRAM output	NDK3		2
DSCE#	95	B	Display SRAM chip	IRQ14		2
D3/I	102	B	Display data Intensity	DMA request 5		4
D0/R	101	B	Display data Red	DMA request 6		4
D1/G	100	B	Display data Green	DMA request 7		4
D2/B	103	B	Display data Blue	DMA request 0		4
M	104	B	Alternate signal for LCD	IRQ15		4
D10	99	B	LCD data for Dual screen	IRQ4 or BVDB1	D	4
D11	98	B	LCD data for Dual screen	IRQ5 or RDYB	D	4
D12	97	B	LCD data for Dual screen	IRQ9 or BVDB2	D	4
D13	96	O	LCD data for Dual screen	SBHE or VPPB		4
CP1/HDRV	106	B	LCD data latch signal	PMC4 or BVDB1		4
CP2/VDO	105	B	LCD clock signal	PMCS5 or RDTB		4
FRM/VDRV	107	B	FRAME/Vertical HSYN	PGP3 or PGP3		4
LVEE	174	O	LCD VEE Voltage Control	PMCS5		2
LVDD	175	O	LCD VDD control	REGB or PMC3		2

RS-232 Interface:

Pin Name	Pin No.	I/O	Function	2nd Function	U/D	Drive
DTR#	205	O	Data terminal ready			1
RTS#	204	O	Request to send			1
CSOUT#	203	O	Serial out			1
CTS#	197	I	Clear to send			
DSR#	202	I	Data set ready			
DCD#	201	I	Data carrier detect			
SIN	199	I	Serial in			
RI#	198	I	Ring indicator			
SPCLK	196	B	Clock Input for UART	WP for socket A		2

Keyboard & RTC Interface:

Pin Name	Pin No.	I/O	Function	2nd Function	U/D	Drive
PCLK	117	B	8042 input PCLK	KBCLK		4
8042CS#	115	B	8042 Chip Select	KBDAT		1
RC#	116	I	8042 RC input			
A20GAGE	118	I	Address A20 GAGE			
RTCAS#	110	O	146818 Address strobe			1
RTCDS#	108	O	146818 Data strobe			1
RTCRW#	109	O	146818 Data R/W			1
KBCLK	1117	B		PCLK		4
KBDAT	115	B		8042CS#		1

Power Management Control Unit Interface:

Pin Name	Pin No.	I/O	Function	2nd Function	U/D	Drive
PMC0	193	O	PMC 0			2
PMC1	194	O	PMC 1	RESET 80387SX		2
PMC2	195	B	PMC 2	ERROR 80387SX		2
PMC3	175	O	PMC 3	LVDD-display, REGB		2
PMC4	106	B	PMC 4	CP1/HDRV- display, BVDB1		4
PMC4	173	B	PMC 4	CP2/VD0-display, RDTB		4
PMC5	105	B	PMC 5	LPH1#		4
PMC5	174	O	PMC 5	LVEE-display		2
PMC6	158	B	PMC 6	SYSCLK		4
PGP0	171	B	Programmable I/O 0			2
PGP1	170	B	Programmable I/O 1			2
PGP2	122	O	Programmable I/O 2	OSC14M		4
PGP3	107	B	Programmable I/O 3	FRM/VDRV- display		4
BL1#	176	I	Main Battery Low First warning			
BL2 #	177	I	Main Battery Low Second warning			
BL3#	178	I	Lithium Battery Low warning			
BL4#	179	I	Main Battery Lost warning			
LPH1#	173	B	Latched POWER control pin 1	PMC4		4
LPH2#	172	B	Latched POWER control pin 2			4

Printer Interface:

Pin Name	Pin No.	I/O	Function	2nd Function	U/D	Drive
AFD#	187	B	AFD	DAK1#		4
PE	188	I	PE	DRQ1	U	.
STB#	184	B	STB			4
SLIN#	186	B	SLIN			4
BUSY	189	I	BUSY	IRQ7	U	
ERROR#	191	I	ERROR	IRQ10	U	
SLCT	190	I	SLCT	IRQ11	U	
ACK#	192	I	ACK	IRQ12	U	
3BCW	185	B	3BCW	I/O channel check		1
INIT#	183	B	Printer's INIT			4

Miscellaneous Interface:

Pin Name	Pin No.	I/O	Function	U/D	Drive
ACIN	182	I	AC power in (disable all PMC function)		
SPKR	220	O	Speaker output		4
X32M	239	I	32.MHz oscillator input		
X1IN	63	I	14.318/28.636MHz crystal input		
X1OUT	62	O	14.318/28.636MHz crystal output		
X32K	119	I	32.768KHz oscillator input		
DIS_CLK	238	O	Disable external 32 MHz OSC		2
RESIN#	155	I	Hardware reset input		
SUSPEND	156	I	Toggle System from FULL ON Mode to/from SUSPEND Mode		

Multiplexing in the TM8100A

The TM8100A offers a large number of functions in a 240-pin PQFP package. This functionality is achieved by sharing pins among different functions. Thus, some trade-offs are involved in how the TM8100A and Am386SXLV CPU are used to implement several portable architectures.

Some of the trade-offs involved are described below:

MUXed Pins

CPU Interface	No MUXing
System Interface	Printer Display Interface Printer
Memory Interface	SRAM Chip Selects MA and SA
PCMCIA Interface	Other PCMCIA pins Display Interface
Display Interface	System Interface PCMCIA Interface
RS-232 Interface	No MUXing
Keyboard and RTC	No MUXing
Power Management	Coprocessor if PCMCIA, CGA

Functionality Trade-offs

Always have	CPU AT compatible logic Memory Interface Serial port (16450)
CGA	8-bit slot and PCMCIA sockets or 16-bit AT-Bus and PCMCIA with 1 external 373
16-bit PCMCIA with CGA and parallel port enabled	SA1-12 used for ISD[8:15] and other control pins Requires 1 external 373 to generate SA[1:12]
Parallel	No DAK1#, DRQ1#, IOCHCK# No IRQ7, 10, 11, 12
Full 16-bit PCMCIA slot	No CGA, no parallel port

The CPU interface is not multiplexed. Some of the memory interface signals are multiplexed to provide interface for DRAMs as well as SRAMs. This is done by multiplexing the SRAM chip selects with some MA pins. Some of the MA signals are used as SAs as described in the datasheet.

A number of trade-offs are involved when selecting the options related with the CGA and the PCMCIA controllers. With the CGA enabled, the PCMCIA controller can only support 8-bit slots which is not practical as 16-bit is the norm in PCMCIA. To use CGA, and support 16-bit PCMCIA slots and 16-bit AT Bus, one would have to add 1 16-bit or 2 8-bit 373's to generate SA[1:12] from MA[1:12]. The SA pins which become available are used for ISD[8:15] and other PCMCIA control signals. In a design that does not use the internal CGA, the external 373's are not required.

Serial port is not multiplexed with any other function. The parallel port uses the DMA channel 1 signals, I/O channel check signal, and some of the interrupt signals. For applications like handheld and pocket computer, the parallel port may or may not be required.

The TM8100 supports 7 power management control outputs and 4 programmable I/O ranges. Three PMC outputs and 2 programmable I/O range(PGP) signals are not MUXed. Availability of the other PMC and PGP signals depends of the specific system design.

FUNCTIONAL DESCRIPTION

The TM8100A is an excellent solution for a portable PC system such as a palmtop, pen based, PDA or personal communicator. The TM8100A can be configured with different pin assignments and different display modes to allow system designers the maximum flexibility to implement a cost effective portable system.

- (A) Handheld Application : PMU + PCMCIAx2 + 8 Bit Slot + CGA LCD + RS232 + Printer
- (B) Pocket PC Application : PMU + PCMCIAx2 + 16 Bit Slot + RS232
- (C) Sub Notebook Application: : PMU + PCMCIAx2 + 16 bit Slot + RS232 + External VGA + External Super I/O

1.0 MEMORY

1.1 Memory Controller

Three different operating modes are supported by the TM8100A: DRAM, SRAM and slow refresh DRAM. CAS before RAS type of refresh is used for DRAM refresh to reduce power consumption. The Switch 1 Register (Index = 66H) determines the memory configuration. The refresh function is disabled when SRAM is used. The TM8100A supports both 8-bit and 16-bit ROM.

Mode Operation Mode Switch

MOD1	MOD0	Function
1	0	Page mode
1	1	Reserved
0	0	0 wait state operation
0	1	One wait state

Memory Configuration

MS2	MS1	MS0	Bank0	Bank1	Total Memory
0	0	1	512•8	-	1M
0	1	0	512•8	512•8	2M
0	1	1	1M	-	2M
1	0	0	1M	1M	4M
1	0	1	4M	-	8M
1	1	0	4M	4M	16M

1.1.1 Slow Refresh DRAM:

1. Bit 1 of Miscellaneous Control Register (Index = A7H) must be set to 1 to enable the slow refresh function. However, system designers must ensure that the DRAM used is capable of supporting slow refresh.
2. It is recommended that if slow refresh is used, bit 0 of Miscellaneous Control Register (Index = A7H) be set to 1 to select the 32KHz clock input as the refresh source to reduce power consumption.
3. Refresh speed can be adjusted by Added 1 Register (Index = 64H):

REFSEL1 Bit 1, Reg. 64H	REFSEL0 Bit 0, Reg. 64H	Refresh Interval
0	0	Normal refresh interval divided by 8
0	1	Normal refresh interval divided by 6
1	0	Normal refresh interval divided by 4
1	1	Normal refresh interval divided by 2

DRAM Speed Requirements:

Operating Mode	Clock Speed	DRAM Speed
Page Mode	20 MHz	80 ns
Page Mode	25 MHz	70 ns
0 Wait	16 MHz	80 ns
0 Wait	20 MHz	60 ns
1 Wait	25 MHz	80 ns

Wait State Selection

When the TM8100A is operating in Page mode, wait states can be added under various conditions. Page hit 0 wait state read, 1 wait state write. These are summarized below:

FCYCWAIT Bit 5, Reg. 63H	PFWS Bit 5, Reg. 65H	DRAM first cycle wait state in page mode
0	0	1 (Default)
0	1	2
1	0	3
1	1	3

BKMISS Bit 6, Reg. 63H	MISOUT Bit 4, Reg. 62H	DRAM Bank miss wait state in page mode
0	0	3 (Default)
0	1	4
1	0	5
1	1	5

1.1.2 SRAM:

1. Selection of SRAM: to use SRAM, bit 0 of Switch 2 Register (Index = 70H) must be set to 1.
2. Memory mapping:

SRAM Control Signal	TM8100A Pin Name (No.)	Note
CS0: Bank 0 Chip select	CAS1L (236)	Select 0 to 512KB
CS1: Bank 1 Chip select	CAS1H (237)	512KB to 1MB
CS2: Bank 2 Chip select	CAS0L (234)	1MB to 1.5MB
CS3: Bank 3 Chip select	CAS0H (235)	1.5MB to 2MB
Address	SA0-SA18	
Data	N/A	Direct connected to CPU

1.2 Shadow RAM:

To enable shadow RAM:

1. Select the ROM window that would be shadowed by programming shadow RAM enable register 1 and 2 (Index = 68H, 69H)
2. If shadowed RAM need to be writeable, set bit 7 in ROM Configuration Register (Index = 65H) to 1.
2. Enable Shadow RAM by setting bit 4 in ROM Configuration Register (Index = 65H) to 1.

1.3 EMS Memory Operation

The TM8100A supports 15 MB of EMS memory. The EMS can be used not only to access on board ROM such as ROM Windows or ROMDOS but also as PCMCIA mapping, SMI mapping, and on board BIOS.

Eight EMS windows, each with 16KB, can be programmed within the range C0000H to EFFFFH. Another four windows, each with 16KB, can be allocated in A0000H to AFFFFH. Each 16KB window can map to anywhere between 1MB to 16MB. The relative registers must be properly programmed before use.

Whenever the EMS operation is enabled, the EMS memory range would be protected from non EMS memory access. In other words, the EMS memory range can only be accessed via EMS mapping by that selected windows. Each individual window can be assigned to different device.

To Enable EMS, follow the steps below;

1. Program the EMS Address Select Register (Index = 6DH) to program the I/O address for EMS pages.
2. Program the EMS Address Extension Register-2 (Index = 6EH)
3. Program the EMS Address Extension Register-1 (Index = 6CH)
4. Set the EMS memory range by programming bit 4 to bit 7 in the Miscellaneous Register (Index = 6FH). The memory range will be protected from other access except EMS, that is, the memory range can only be visible through EMS.
5. Program each Page Register
6. Program the EMS Device Selection Register 1 and 2 (Index = 71H, 72H) Each page of EMS within the TM8100A can be assigned a unique device.
7. Set bit 7 of the ROM Configuration Register (Index = 65H) to enable the EMS

EMS1 uses the same I/O addresses for Page Registers and Address Extension Registers. A selection bit in the EMS1 Control Register (Index = 74H) must be programmed to determine whether EMS or EMS1 is being programmed. The programming flow chart for EMS1 is the same as EMS. EMS function can be enabled in the DMA cycle by setting bit 7 of the I/O Wait State Register (Index = 61H) to 1.

1.4 ROM Control:

Signal Name	Pin No.	Write Enable Control Register	Wait State Control Register	Address decode Control Register
NEPS in Non EMS Cycle	141	Bit 6, 63H	Bit 4,7; 60H	Bit 0,1,2,3 65H
NEPS in EMS Cycle	141	Bit 6, 63H	Bit 0,1; 62H	Bit 0,1,2,3 65H
NDOS	139	Bit 7, 63H	Bit 0,1; 62H	by EMS

The TM8100A can support either 8 bit or 16 bit ROM access. To enable 16 bit ROM access, bit 1 in register (Index = 51H) must be set and 16 bit PCMCIA must be enabled.

2.0 CLK CONTROL

There are three clock sources used by the TM8100A, they are:

Main Clock: (Pin 239). Used by the CPU and memory controller inside the TM8100A when the system runs at high speed (selected by bit 6 in the I/O Wait State Register, (Index = 61H)). A system designer can use an external oscillator to generate this clock and the TM8100A provides a control pin DIS-CLK to control the on/off of the external oscillator. The DIS-CLK is defaulted at low and can be programmed to become logic high in ON Mode or DOZE mode (selected by bit 2 in the Miscellaneous Control Register, (Index = ADH)). A special mode is provided to **eliminate the 14.745MHz clock by using a 28.636MHz clock as the MAIN clock**. To use this special mode, set bit 7 in Switch 1 Register (Index = 66H) to 1.

14.745MHz: (Pin 62, 63). Used by the LCD controller, DMA (8237) Timer (8254) and 16450. This clock source also generates the clock for ON mode and Low Speed clock. This clock is generated by an on-chip crystal oscillator. This clock is stopped when the system enters SLEEP mode. 14.745MHz is used instead of 14.318MHz in order to generate the exact clock frequency for 16450. However this might result in the system timer becoming inaccurate; therefore a modification in BIOS should be done to compensate for this time difference. The crystal restart time can be programmed via bit 0-4 in Register (Index = 8FH).

32.768KHz: (Pin 119). This clock is used by the PMU, internal RTC, and refresh source in SLEEP mode.

CPU CLOCK: The status of the CPU speed in FULL ON mode can be read back from bit 7 in Register (Index = A3H). The clock speed in the ON mode can be programmed by bit 0, bit 1 in Miscellaneous Control Register (Index = ADH)

To conserve power consumption of the ASIC in DOZE, SLEEP, and SUSPEND mode, the MAIN CLOCK will be turned off by a controller signal DIS_CLK (pin 238). This signal is used to turn on/off the external oscillator. To further reduce the power consumption in SLEEP and SUSPEND mode, the 14.745MHz clock will be turned off automatically by disabling the on-chip crystal oscillator. The 32K clock is used to generate DRAM refresh in SLEEP and SUSPEND mode. However, in order to reduce the power consumption due to DRAM refresh, the designer can use the 32K clock instead of the regular 8254 as the main refresh source.

Note: Clock to CPU will be forced to DC under the following conditions : (1) System enters DOZE mode (2) By software command. (3) By SUSPEND pin input.

3.0 POWER MANAGEMENT UNIT

This unit monitors all system activities and determines what operating mode and speed the system should be running to save power.

Monitored activities

DMA Requests	Pin 238						
Keyboard Interrupt	Pin 238						
EMS Cycle	Pin 238						
ACIN-AC adapter input	Pin 238						
Interrupts	Pin 238						
Parallel Port Access	Pin 238						
Floppy Disk Access	Pin 238						
Hard Drive Access	Pin 238						
Serial Port ACcess	Pin 238						
Programmable I/O Device Activity	Pin 238						
Video Memory Access	Pin 238						
Programmable Memory Range Write Access	Pin 238						

MODE

POWER ON

DESCRIPTION

After POWER ON, self test system enters FULL ON Mode

FULL ON

The FULL ON Mode indicates the nominal operating condition where all clocks are running at full speed and all peripheral devices are powered up. FULL ON Mode is entered into after POWER ON self test. The system will remain in FULL ON Mode as long as activities are detected by the activity monitor. FULL ON can be entered into from ON and DOZE Modes by detection of an activity (for example, a keyboard input). FULL ON can be entered into from SLEEP or SUSPEND by (IOPIN, Pin 156) SUSPEND pin input. This feature gives the system an "instant on" feature whereby the state is saved before SUSPEND and a resume brings the system to FULL ON in the same state in which it was suspended.

ON

ON Mode is the first level of power management. The system will enter ON Mode from FULL ON Mode after 1/512 to 1/2 or 1/16 to 16 seconds of inactivity. In ON Mode, the CPU clock is slowed to 14 MHz, thus reducing the system clock to 7 MHz. All other clocks and peripherals are maintained at their FULL ON Mode. Detection of activity will send system into FULL ON Mode.

DOZE	DOZE Mode is the second level of power management where the CPU, system clock, and DMA clock are put in stop clock. All other clocks and peripherals may be reduced in frequency or powered down. DOZE Mode is entered into from ON Mode after 1/16 to 16 or 1/2 to 128 seconds of inactivity. Detection of activity will cause the system to enter FULL ON Mode.
SLEEP	SLEEP Mode is the third level of power management where additional clocks may be stopped and power may be disconnected from one or more peripheral devices. SLEEP is entered into from DOZE after 4 seconds to 64 minutes of inactivity. FULL ON can not be entered into from the SLEEP Mode by keyboard activity. Any other activity will send the system into FULL ON Mode as will SUSPEND pin input.
SUSPEND	SUSPEND Mode represents the forth and deepest level of power conservation wherein a special BIOS routine is invoked to save the current state of the system for complete restoration at some later time. Once the system has been saved, the vast majority of the system may be shut down for optimum power conservation while still retaining restorability. SUSPEND is entered into from SLEEP after 1/16 to 16 seconds of inactivity. FULL ON can be entered into from SUSPEND by SUSPEND pin input or Modem ring.
POWER OFF	The system will enter this mode from SUSPEND Mode after 1 to 256 minutes of inactivity.

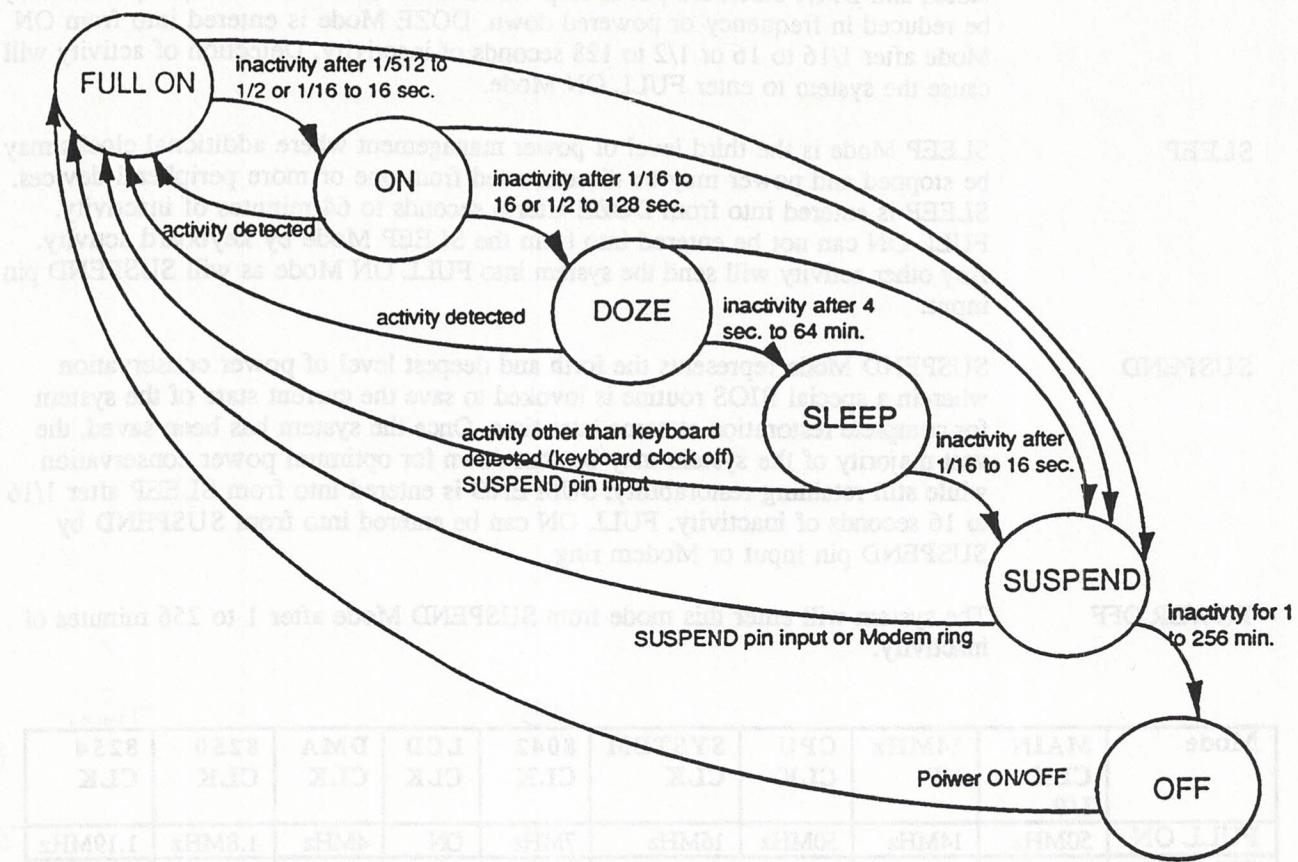
KB

Mode	MAIN CLK I/P	14MHz I/P	CPU CLK	SYSTEM CLK	8042 CLK	LCD CLK	DMA CLK	8250 CLK	8254 CLK	BL
FULL ON	50MHz	14MHz	50MHz	16MHz	7MHz	ON	4MHz	1.8MHz	1.19MHz	ON
ON	DC	14MHz	14MHz	7MHz	7MHz	ON	4MHz	1.8MHz	1.19MHz	ON
DOZE	DC	14MHz	DC	DC	7MHz	ON	DC	1.8MHz	1.19MHz	ON
SLEEP	DC	14MHz	DC	DC	DC	ON	DC	DC	1.19MHz	OFF
SUSPEND	DC	DC	DC	DC	DC	OFF	DC	DC	DC	OFF

Notes:

- 1 The 8042 clock is disabled in SLEEP mode, therefore, the system can not wake up by keystroke.
- 2 CPU is running in high speed only in FULL ON mode
- 3 All power management features will be disabled when AC power is detected by ACIN high, a register is provided to implement "software ACIN" by writing "1" to bit 5 in register (Index =70H).

3.1 Power Management State Diagram



3.2 Power Management Control Register : (Index = 80H, 81H, 82H)

The TM8100A supports seven programmable PMC output pins. Each pin is individually controlled by a bit in the PMC Control Register. The PMC output control pins are used to control power on/off of different peripherals such as LCD, PCMCIA sockets, RS232, and HDD. The CPU can program the output state of each PMC output pin to a different mode (FULL ON, ON, DOZE, SLEEP, SUSPEND). When the system changes state, due to a different activity, the PMC output pins are changed accordingly.

To enable the power management feature, follow the steps below:

1. Select the activities that the system should consider active by programming the Activity Mask Register 1 and 2 (Index = 75H, 76H).
2. Program the I/O port the system wants to monitor by programming I/O Activity Address Register (Index = 8CH, 8DH) if bit 4 or bit 5 in the Activity Mask Register (Index = 76H) is set.
3. Program the memory write address range (Index = 9AH, 9BH) if bit 7 in the Activity Mask Register (Index = 76H) is set.
4. If ACIN should be considered as activity then bit 4 of Miscellaneous Register 3 (Index = ADH) should be set to 1.
5. The bit 7 (INT) of Activity Mask Register 1 (Index = 75H) does not monitor Timer and Keyboard interrupt.
6. If NMI or SMI should be generated during mode change then bit 0 through bit 4 in the SMI Enable Register (Index = 82H) should be enabled.
7. If Timer interrupt (IRQ0) should be invoked in DOZE mode then bit 3 in the EMS1 Control Register (Index = 74H) should be set.
8. Program the FULL ON mode Timer (Index = 83H)
9. Program the ON mode Timer (Index = 84H)
10. Program the DOZE mode Timer (Index = 85H)
11. Program the SLEEP mode Timer (Index = 86H)
12. Program the SUSPEND mode Timer (Index = 87H)

Notes:

- 1: Activity status can be read back from Activity Status Register-1 or -2 (Index = A0H, A1H)
- 2: The Current PMU Mode can be read back from bit 0 to bit 2 in the Status Register-1 (Index = A4H)
- 3: The Previous PMU Mode can be read back from bit 4 to bit 6 in Status Register-0 (Index = A3H)
- 4: Software can command the PMU to enter any mode by programming the Mode Register (Index = 88H)

3.3 Power Management Control Pin (PMC)

	Pin No.	Other Function	Full On	DOZE	SLEEP	SUSPEND	Inverted ?	Default State
PMC0	193	None	bit0, 80H	bit 4, 80H	bit 0, 81H	bit 4, 81H	No	Low
PMC1	194	None	bit1, 80H	bit 5, 80H	bit 1, 81H	bit 5, 81H	Yes	High
PMC2	195	None	bit2, 80H	bit 6, 80H	bit 2, 81H	bit 6, 81H	No	Low
Disable 14M Signal		Internal Signal	bit3, 80H	bit 7, 80H	bit 3, 81H	bit 7, 81H		
PMC3	99	DD10	bit0, ABH	bit 1, ABH	bit 2, ABH	bit 3, ABH	Yes	High
PMC4	98	DD11	bit4, ABH	bit 5, ABH	bit 6, ABH	bit 7, ABH	No	Low
PMCS	97	DD12	bit0, ACH	bit 1, ACH	bit 2, ACH	bit 3, ACH	Yes	High
PMC6	158	SYCLK	bit4, ACH	bit 5, ACH	bit 6, ACH	bit 7, ACH	No	Low

3.4 SMM Function

The TM8100A supports AMD's SMI function. There are several events that can generate SMI, they are;

1. Battery Low Detector input
2. Programmable I/O port (I/O trap)
3. Hard disk access
4. Floppy disk access
5. Operating Mode change state
6. IRQ0 (system timer)

To Set-up SMM

- 1: Bit 0 in register (Index = 6BH) must be set to 1.
- 2: To set SMI memory range as 16K, set bit 7 in Wait State Control Register 2 (Index = 63H) to 0.
- 3: To set SMI memory range as 64K, set bit 7 in Wait State Control Register 2 (Index = 63H) to 1.
4. Always set bit 3 in register (Index = 64H) to 1.

To generate SMI from:

Battery Low Detector Input

To generate an SMI during a battery low condition then bit 5 through bit 7 in the SMI Enable Register (Index = 82H) should be enabled. When an SMI is generated, software can read from the SMI Status Register (Index = A5H) to determine the source of SMI.

The battery low message can be displayed via SMI which will be application program independent.

Hard Disk and Floppy Disk Access and Programmable I/O Port

The TM8100A has the capability of controlling the power of peripheral devices such as hard disk, floppy disk and programmed I/O by programming time out limits in HDD< FDD and PIO programming registers. (Index = 46H, 47H). When properly programmed, the TM8100A will generate an SMI to CPU when the timer expires and the state will be saved and power to the HDD, FDD, or PIO will be turned off.

The TM8100A can be programmed to generate an SMI when a CPU I/O cycle is executed to the I/O address of the HDD (1F0-1F7), FDD (32F0-3F7), or PIO. The SMI routine can determine whether to turn on the power of the peripheral device and enable the timer. If the peripheral was turned off an I/O trap and I/O restart will occur. Once turned off, the timer starts counting. Once the timer expires, the device power will be automatically turned off by the corresponding PMC output.

To control peripheral power, follow the programming steps below:

1. Program the programmable I/O address (Index = 45H) for the I/O port that needs to be monitored.
2. Program the Time-out limit for HDD, FDD, and PIO by programming registers (Index = 46H, 47H)
3. Program the SMI EMS Page Register (Index = A9H, AAH)
4. Enable SMI by Enable Registers (Index = 40H, 41H)
5. Set bit 7 of EMS1 Socket Selection Register (Index = A9H) to 1 to enable SMI instead of NMI
6. Set bit 6 of EMS1 Socket Selection Register (Index = A9H) to 1 to enable SMI.

Notes:

- 1: When an SMI is generated due to I/O trap (programmed I/O address), software can read the bus cycle executed (read or write, byte or word) from SMI I/O Status Register (Index = 42H).
- 2: When an SMI is generated, software can read from the SMI Status Register (Index = 43H) to determine the source of SMI.

Power Management Mode Change

To generate SMI during a mode change, bit 0 through bit 4 in the SMI Enable Register (Index = 82H) should be enabled. When an SMI is generated, software can read from the SMI Status Register (Index = A5H) to determine the source of SMI.

IRO0 (System Timer) to Generate an SMI in DOZE Mode

Set bit 6 in the Miscellaneous Control Register (Index = ADH) to 1.

3.4 General Purpose I/O Pins

The TM8100A has four general purpose pins (PGP0-PGP3) that can be individually programmed as inputs or outputs. System designers can use these pins as decoder outputs for other peripheral devices or as status input pins. The default state for these pins is input at power on.

PGPx	Pin Multiplex with	I/O Control	Input Data Port	Output Address Register Index	Command Register Index
PGP0	None	bit 6, 70H	bit 0, A3H	89H	bit 0,1 91H
PGP1	None	bit 2, 74H	bit 3, A4H	9CH	bit 2,3, 91H
PGP2	OSC (Default=PGP2)	O/P only	None	94H	bit 4,5, 91H
PGP3	FRM (Default)	O/P only	None	95H	bit 6,7, 91H

3.5 Suspend Input Pin

This pin is a special hardware input pin, it is used to switch from FULL ON, ON, DOZE mode to SUSPEND mode or SLEEP mode/SUSPEND mode to FULL ON mode. A low to high edge pulse at this input will trigger mode change.

3.6 ACIN Pin

The ACIN pin is a special hardware input pin. This pin is used to disable all power management function when detected High

3.7 Battery Low Detect

The TM8100A supports four battery low detector inputs (BL1, BL2, BL3, BL4). BL1 is the first warning, BL2 is the second warning, BL4 is the indicator of battery dead. BL3 is used as the warning for the backup battery. A logic high at BL1, BL2, BL3, BL4 input represent normal conditions, A logic low indicates a warning condition. The TM8100A can be programmed to generate NMI or SMI when BL1 is active. When the TM8100A detects a logic low at the BL2 input, the system can be programmed to enter SLEEP mode automatically, this feature is useful to conserve RAM content when the battery runs low. The BL4 is used to detect the battery dead condition, once this condition is detected, the TM8100A will automatically enter SLEEP mode and set output pin LHP2 to Low.

BLx	Mask Bit	SMI Enable Bit	Status bit	Comment
BL1	None	bit 5, 82H	bit 1, A3H	
BL2	Bit 6, 74H	bit 6, 82H	bit 2, A3H	
BL3	None	bit 7, 82H	bit 3, A3H	
BL4	Bit 7, 74H	None	None	Set LPH2 to Low

3.8 Other Power Saving Features

1. Setting bit 4 in Configuration Register-0 (Index = 44H) to 1 will prevent data toggling within the TM8100A during DRAM cycle except DMA.
2. Setting bit 2 in Miscellaneous Control Register (Index = A7H) to 1 will disable REF pin from toggling in SLEEP mode.

4.0 DISPLAY CONTROLLER

The TM8100A supports a CGA LCD controller. Only one external SRAM is needed to implement a complete CGA LCD display subsystem. Several resolution of LCD are supported, they are;

640x200	single scan, double scan
640x400	single scan, double scan
320x200	single scan, double scan
X•Y	single scan X<= 640, Y<= 200

The CGA LCD controller is enabled at power up, the system designer can disable the controller by setting bit 2 and bit 3 in Switch-2 Register (Index = 70H).

When only single scan LCD is used, pin DD10, DD11 DD12, DD13 can be configured as different functionality as described in the Pin Configuration section.

5.0 UART

A 16450 compatible UART is built inside the TM8100A. The UART is disabled after power up. Software must enable it before using the UART.

Follow the steps below to enable UART.

1. Program the UART I/O address (COM1 or COM2) by program bit 5, 6, 7 in the RTC Alarm Enable Register (Index = 77H).
2. Select the clock source for UART by programming bit 1 of UART Clock Enable Register (Index = 92H).
3. Enable clock to UART by setting bit 0 in UART Clock Enable Register (Index = 92H) to 1.
4. Enable UART by setting bit 4 in RTC Alarm Enable Register (Index = 77H) to 1.

Note:

If the 14.318MHz crystal is selected as the clock source to UART, then 2.89% variation of frequency will be observed. To avoid such inaccuracy, change the 14.318MHz clock to 14.745MHz or use the clock from external pin (196).

6.0 PRINTER

An IBM AT compatible printer port is built inside the TM8100A.

Care must be taken in the connection of printer control signals to the printer if the TM8100A should be running at 3.3V. It is strongly recommended to interface the printer port to external connectors at 5V (through external buffers) because some peripheral devices might not work at 3.3V and latch-up problem might occur.

7.0 INTERNAL RTC:

To enable internal RTC, follow the steps below:

1. Program the Half-Day Registers (Index = 7AH, 7BH), this counter has a base unit of 12 hours.
2. Program the Second Register (Index = 78H, 79H).
3. Set RTC control bits (bit 6, bit 7 in the TM8100A Status Register (Index = A4H)).
4. Set RTC enable bit, bit 2 in Switch 2 Register (Index = 70H).

To enable RTC Alarm

1. Program the Alarm Half Day Registers (Index = 7EH, 7FH), this counter has a base unit of 12 hours.
2. Program the Alarm Second Register (Index = 7CH, 7DH).
3. Set bit 7 in Miscellaneous Control Register (Index = ADH) to 1.
4. RTC Alarm control bits; bit 0,1,2 in RTC Alarm Enable Register (Index = 77H).

Note: Before updating the internal RTC, software has to be checked to ensure that RTC is not in the update cycle (bit 4 Register (Index = A4H)).

8.0 PCMCIA:

Chip Control Registers: These registers act to control card interface, power, interrupts, and pin configuration.

Status Registers: These registers act to keep status of card.

I/O Registers: These registers are used to configure I/O window addresses, 16-bit cycles, and set card as an I/O card.

Memory Registers: These registers are used to configure type of memory access (common or attribute), 16-bit memory cycles, and EMS device selection.

Socket A:	Description	Register Index	Alternate Register
Memory	REGA pin I/O address	8AH	
	Card in Socket A can accept 16 bit memory cycle	Bit 0, 0AH	
	EMS device selection register	A8H, bit 0-3, A9H	
Chip Control	VPPA pin I/O address	8BH	07H
	Interrupt re-direction Control Register	06H	
	RI from socket A can wake up system	Bit 0, 08H	
	Set Pin BVDA1 as RI	Bit 6, 08H	
	CD pin change state enable INT	Bit 0, 0DH	
	RDY pin change from low to high enable INT	Bit 2, 0DH	
	BVDA1 pin change from high to low enable INT	Bit 4, 0DH	
	BVDA2 pin change from high to low enable INT	Bit 6, 0DH	
Status	Status	A2H	
	Status Interrupt re-direction control register	0EH	
	Card Change Status	Bit 0, A6H	
	RI from socket A waked up system	Bit 0, 09H	
	Socket Status Change register	A6H	
I/O	I/O window 1 address Low Byte	96H	
	I/O window 1 address High Byte	97H	
	I/O window 1 MASK address Low Byte	98H	
	I/O window 1 MASK address High Byte	99H	

Socket A	Description	Register Index	Alternate Register
I/O Continued	I/O window 1 address Start Low Byte	00H	
	I/O window 1 address End Low Byte	01H	
	I/O window 1 address High Byte	02H	
	I/O window 2 address Start Low Byte	03H	
	I/O window 2 address End Low Byte	04H	
	I/O window 2 address High Byte	05H	
	Card in Socket A can accept 16 bit I/O cycle	Bit 2, 0AH	
	Set Card in Socket as I/O card	bit 4,5, 74H	
Socket B:	Description	Register Index	
Memory	Socket B Installed	Bit 7, 70H	
	REGB pin I/O address	9EH	
	Card in Socket B can accept 16 bit memory cycle	Bit 1, 0AH	
Chip Control	EMS device selection register	A8H, bit 0-3, A9H	
	VPPB pin I/O address	17H	
	Interrupt re-direction Control Register	16H	
	RI from socket B can wake up system	Bit 1, 08H	
	Set Pin BVDB1 as RI	Bit 7, 08H	
	CD pin change state enable INT	Bit 1, 0DH	
	RDY pin change from low to high enable INT	Bit 3, 0DH	
	BVDB1 pin change from high to low enable INT	Bit 5, 0DH	
Status	BVDB2 pin change from high to low enable INT	Bit 7, 0DH	
	Status	0CH	
	RI from socket B waked up system	Bit 1, 09H	
	Status Interrupt re-direction control register	0EH	
	Card Change Status	Bit 0, A6H	
I/O	Socket Status Change register	A6H	
	I/O window 1 address Start Low Byte	10H	
	I/O window 1 address End Low Byte	11H	
	I/O window 1 address High Byte	12H	
	I/O window 2 address Start Low Byte	13H	
	I/O window 2 address End Low Byte	14H	
	I/O window 2 address High Byte	15H	
	Card in Socket B can accept 16 bit I/O cycle	Bit 3, 0AH	
	Set Card in Socket as I/O card	bit 2, 16H	

For more information on PCMCIA PC Cards, refer to "PCMCIA PC Card Standard Release 2.0" published by Personal Computer Memory Card International Association. (408)720-0107.

9.0 REGISTER DESCRIPTIONS

NMI/SMI Registers

The following registers are used to configure SMI functionality of the TM8100A controller.

SMI Mask Register	Index = 40H	see page	29
SMI Function Enable Register	Index = 41H		30
SMI I/O Status Register	Index = 42H		30
SMI Status Register	Index = 43H		30
SMI PIO Address Register	Index = 45H		31
SMI PIO Timer Register	Index = 46H		31
SMI HD and FD Timer Register	Index = 47H		31
Version Register	Index = 64H (Read only)		37
Added 1 Register	Index = 64H (Write only)		37
Pin Selection Register	Index = 6BH		39
Programmable NMI or SMI Enable Register	Index = 82H		46
NMI/SMI Status Register-Read Only	Index = A5H		53
NMI/SMI Enable Register-Write Only	Index = A5H		53
SMI EMS Page Register	Index = AAH		54
NMI Register	Index = 070H		29
Wait State Control Register-2	Index = 63H		37

EMS Registers

The following registers are used to configure EMS operation.

EMSA Address Extension Register 1 Bit 21-22	Index = 67H	see page	39
EMSA/B Address Extension Register 1 Bit 23	Index = 6CH		40
EMSA/B Address Select Register	Index = 6DH		40
EMSA/B Address Extension Register-2	Index = 6EH		41
EMSA Device Selection Register-1	Index = 71H		42
EMSA Device Selection Register-2	Index = 72H		43
EMSB Device Selection Register-2	Index = 73H		43
EMSB Control Register	Index = 74H		44
EMSA Socket Selection Register	Index = A8H		54
EMSB Socket Selection Register	Index = A9H		54
SMI EMS Page Register	Index = AAH		54
Miscellaneous Register	Index = 6FH		41

SLOT I/O and Memory Registers

SLOT Memory Wait State Select Register-2	Index = 50H	see page	33
Command Delay Register	Index = 60H		34
SLOT Memory Wait State Register	Index = 62H		36

Memory Registers

Switch 1 Register	Index = 66H	see page	38
Shadow RAM Enable Register-1	Index = 68H		39
Shadow RAM Enable Register-2	Index = 69H		39
Switch 2 Register	Index = 70H		42
Wait State Control Register-2	Index = 63H		37
Added 1 Register	Index = 64H		37
ROM Configuration Register	Index = 65H		38
ROM Configuration Register-2	Index = 51H		34
Pin Configuration Register A	Index = 48H		32
Command Delay Register	Index = 60H		34
Programmable Memory Write Active Low Address Register	Index = 9AH		50
Programmable Memory Write Active High Address Register	Index = 9BH		50

RTC Registers

RTC Alarm Enable	Index = 77H	see page	45
RTC Second (LSB) Register	Index = 78H		45
RTC Second (MSB) Register	Index = 79H		45
RTC Half-day Register	Index = 7AH		45
RTC Half-day Register	Index = 7BH		45
RTC Alarm Second (LSB) Register	Index = 7CH		45
RTC Alarm Second (MSB) Register	Index = 7DH		45
RTC Alarm Half-day (LSB) Register	Index = 7EH		45
RTC Alarm Half-day (MSB) Register	Index = 7FH		45

Power Control Registers

Programmable Power Control Register-1	Index = 80H	see page	45
Programmable Power Control Register-2	Index = 81H		46
Programmable NMI or SMI Enable Register	Index = 82H		46
FULL ON Mode Programmable Timer Register	Index = 83H		46
ON Mode Programmable Timer Register	Index = 84H		46
DOZE Mode Programmable Timer Register	Index = 85H		46
SLEEP Mode Programmable Timer Register	Index = 86H		46
SUSPEND Mode Programmable Timer Register	Index = 87H		47
Software Mode Control Register	Index = 88H		47
Programmable Power Control Register-3	Index = ABH		55
Programmable Power Control Register-4	Index = ACH		55

PCMCIA Registers

SLOT Memory Wait State Select Register	Index = 50H	see page	33
Configuration Register B	Index = 49H		32
EMSA Device Selection Register-1	Index = 71H		42
EMSA Device Selection Register-2	Index = 72H		43
Programmable PCMCIA I/O Window Address Register (Low Byte)	Index = 96H		49
Programmable PCMCIA I/O Window Address Register (High Byte)	Index = 97H		49
Programmable PCMCIA I/O Window Mask Register (Low Byte)	Index = 98H		49
Programmable PCMCIA I/O Window Mask Register (High Byte)	Index = 99H		49
PCMCIA Socket 1 Status Register	Index = A2H		52
Socket Status Change Register	Index = A6H		53
EMSA Socket Selection Register	Index = A8H		54
EMSB Socket Selection Register	Index = A9H		54
PCMCIA Interrupt Selection Register	Index = AEH		55
PCMCIA Socket A I/O Window 1 Address Start Low Byte Register	Index = 00H		56
PCMCIA Socket A I/O Window 1 Address End Low Byte Register	Index = 01H		56
PCMCIA Socket A I/O Window 1 Address High Byte Register	Index = 02H		56
PCMCIA Socket A I/O Window 2 Address Start Low Byte Register	Index = 03H		56
PCMCIA Socket A I/O Window 2 Address End Low Byte Register	Index = 04H		56
PCMCIA Socket A I/O Window 2 Address High Byte Register	Index = 05H		56
PCMCIA Interrupt Redirection Control (Socket A) Register	Index = 06H		56
ICCARD Socket A VPP Control Register	Index = 07H		57
Programmable Resume Mask Register-3	Index = 08H		57
Resume Status Register	Index = 09H		57
PMU Control Register	Index = 0AH		57
PCMCIA Socket B Register	Index = 0CH		57
PCMCIA Interrupt Enable Register	Index = 0DH		58

Programmable Socket Status Interrupt Selection Register	Index = 0EH	58
PCMCIA Socket B I/O Window 1 Address Start Low Byte Register	Index = 10H	58
PCMCIA Socket B I/O Window 1 Address End Low Byte Register	Index = 11H	58
PCMCIA Socket B I/O Window 1 Address High Byte Register	Index = 12H	58
PCMCIA Socket B I/O Window 2 Address Start Low Byte Register	Index = 13H	58
PCMCIA Socket B I/O Window 2 Address End Low Byte Register	Index = 14H	58
PCMCIA Socket B I/O Window 2 Address High Byte Register	Index = 15H	58
PCMCIA Interrupt Redirection Control (Socket B) Register	Index = 16H	59
ICCARD Socket B VPP Control Register	Index = 17H	59

Miscellaneous Configuration and Status Registers

Port B Register	Index = 61H	see page	35
Configuration Register 0	Index = 44H		30
Pin Configuration Register A	Index = 48H		32
Configuration Register B	Index = 49H		32
Pin Selection Register	Index = 6BH		39
Miscellaneous Register	Index = 6FH		41
PGP Pin Command Select Register	Index = 91H		48
Clock Control Register	Index = 8FH		48
Internal UART Clock Enable Register	Index = 92H		49
Auto Low Speed Control Register	Index = 9FH		51
TM8100A Status Register-0	Index = A3H		52
TM8100A Status Register-1	Index = A4H		52
Miscellaneous Control Register	Index = A7H		54
Miscellaneous Control Register-3	Index = ADH		55
CPU Control Register	Index = AFH		56

I/O Registers

I/O Wait State Register	Index = 61H	see page	35
Wait State Control Register	Index = 63H		37
Programmable General Purpose I/O Register-0	Index = 89H		47
Programmable Socket A VPPA Address Decoder Register	Index = 8BH		47
LHP1 Programmable I/O Address Register	Index = 90H		48
Programmable General Purpose I/O Register-2	Index = 94H		49
Programmable General Purpose I/O Register-3	Index = 95H		49
Programmable General Purpose I/O Register-1	Index = 9CH		50
Programmable Socket B REGA Address Decoder Register	Index = 9EH		50
Programmable I/O Activity Address Register-0	Index = 8CH		47
Programmable I/O Activity Address Register-1	Index = 8DH		47

Activity Mask Registers

		see page	
Programmable Activity Mask Register-1	Index = 75H	44	
Programmable Activity Mask Register-2	Index = 76H	44	
Programmable I/O Activity Address Register-0	Index = 8CH	47	
Programmable I/O Activity Address Register-1	Index = 8DH	47	
Programmable Memory Write Activity Low Address Register	Index = 9AH	50	
Programmable Memory Write Activity High Address Register	Index = 9BH	50	
Activity Monitor Status Register-1	Index = A0H	51	
Activity Monitor Status Register-2	Index = A1H	51	

The registers within the TM8100A are accessed through indirect addressing.. An Index Register with an I/O address 22H must first be written to the index value of the particular register being configured. The configuration data can then be written or read out from that configuration register through I/O address 23H.

Index Register : (Index = 22H)

This register is used to point to the actual register used by the CPU. Read/write.

Data Register : (Index = 23H)

This register is used to read from or write data to the actual register pointed to by the Index Register.

Port B Register : (Index = 61H)

BIT	NAME	R/W	FUNCTION
0	T2G	RW	Timer 2 gate (speaker)
1	SPKD	RW	Speaker data
2	ENRAMPCK	RW	Enable system memory parity check (same as SW2 register bit 0), 0 = Enable
3	EIC	R/W	Enable I/O channel check , 0 = Enable
4	RFD	R	Refresh detected
5	T2OUT	R	Timer 2 output
6	IOCHK	R	I/O channel check
7	PCK	R	Parity check

NMI Register : (Index = 070H)

BIT	NAME	R/W	Function
0-6	RESERVED	W	Reserved.
7	ENMI	W	0 = Enable NMI, Default =1

SMI Mask Register : (Index = 40H)

This register is used to mask different SMI sources, in other words, default = 0H will disable all SMI generation, a High in each bit will enable its corresponding SMI.

BIT	NAME	R/W	Function
0	HDDMASK	RW	MASK the SMI function on HDD access (1F0-1F7)
1	FDDMASK	RW	MASK the SMI function on FDD access (3F0-3F7)
2	PIOMASK	RW	MASK the SMI function on a programmable I/O port access
3-7	RESERVED	R/W	Reserved

SMI Function Enable Register : (Index = 41H)

This register is used to control the generation of individual SMI functions, a 1 in each bit will enable its corresponding SMI, a 0 will disable its corresponding function. Default = 0H

BIT	NAME	R/W	Function
0	ENHD	RW	Enable HDD SMI
1	ENFD	RW	Enable FDD SMI
2	ENPIO	RW	Enable PIO SMI
3-7	RESERVED	R/W	Reserved

SMI I/O Status Register : (Index = 42H)

This register contains the states of the CPU BUS when a PIO SMI is generated. Software can read this register to determine the type of bus cycle executed.

BIT	NAME	R/W	Function
0	XAO	R	State of XAO when a PIO SMI was generated
1	BHE	R	State of BHE when a PIO SMI was generated
2	IOR	R	State IOR when a PIO SMI was generated
3	IOW	R	State of IOW when a PIO SMI was generated
4-7	RESERVED	R	Reserved

SMI Status Register : (Index = 43H)

This register contains the status of the SMI source. A 1 in each bit indicates the corresponding source has requested a SMI. After reading, software is responsible for clearing the register by writing 0H.

BIT	NAME	R/W	Function
0	HDSMI	RW	Hard Disk had requested a SMI
1	FDSMI	RW	Floppy Disk had requested a SMI
2	PIOSMI	RW	PIO had requested a SMI
3-4	RESERVED	RW	Reserved
5	PMCSMI	RW	Mode changes had requested a SMI
6	IRQ0SMI	RW	IRQ0 had requested a SMI
7	RESERVED	RW	Reserved

Configuration Register 0 : (Index = 44H)

BIT	NAME	R/W	Function
0	IRQEN	RW	If bit is set (one), IRQ14 will clear Hard disk timer
1	LASEL	RW	If set, LA17-23 will be latched by the TM8100A
2	RESERVED	R/W	Internal use only-must be low
3	ICDIREN	RW	One will set pin 142 (SDDIRL) to function as PCMCIA data bus direction control, default is direction control for SD Bus
4	DISDEN	RW	If set, Data read from DRAM in CPU cycle will not propagate through the TM8100A. Default is 0
5	PM3SEL	RW	One will set pin 175 to function as PMC3, default is LVDD, if Bit 4 of Pin configuration Register B (Index = 49) is 0
6	CLRDISP	R/W	Reserved-must be low
7.	SMIACT	R/W	Internal used-must be set high

SMI PIO Address Register : (Index = 45H)

This register is used to program the SMI PIO address A9 to A2. The PIO will decode a minimum of a four bytes window where A0 and A1 are not decoded. However, A2, A3, and A4 can also be masked by bit 0 and bit 1 of Register (Index = 46H).

BIT	NAME	R/W	Function
0	PXA9	R/W	PIO address bit A9
1	PXA8	R/W	PIO address bit A8
2	PXA7	R/W	PIO address bit A7
3	PXA6	R/W	PIO address bit A6
4	PXA5	R/W	PIO address bit A5
5	PXA4	R/W	PIO address bit A4
6	PXA3	R/W	PIO address bit A3
7	PXA2	R/W	PIO address bit A2

SMI PIO Timer Register : (Index = 46H)

This register is used to program the SMI PIO time out period.

BIT	NAME	R/W	Function
0	PIOT0	R/W	SMI PIO timer setting bit 0
1	PIOT1	R/W	SMI PIO timer setting bit 1
2	PIOT2	R/W	SMI PIO timer setting bit 2
3-5	RESERVED	R/W	Reserved
6	RA1	R/W	PIO decode range select 1
7	RA0	R/W	PIO decode range select 0

PIOT2	PIOT1	PIOT0	Period	RA1	RA0	RANGE
0	0	0	128 ms	0	0	4 Byte
0	0	1	256 ms	0	1	8 Byte
0	1	0	512 ms	1	0	16 Byte
0	1	1	1 sec	1	1	32 Byte
1	0	0	2 sec			
1	0	1	4 sec			
1	1	0	8 sec			
1	1	1	16 sec			

SMI HD and FD Timer Register : (Index = 47H)

This register is used to program the SMI HD and FD time out periods.

Bit	NAME	R/W	Function
0	HDT0	R/W	SMI HD timer setting bit 0
1	HDT1	R/W	SMI HD timer setting bit 1
2	HDT2	R/W	SMI HD timer setting bit 2
3	RESERVED	R/W	Reserved
4	FDT0	R/W	SMI FD timer setting bit 0
5	FDT1	R/W	SMI FD timer setting bit 1
6	FDT2	R/W	SMI FD timer setting bit 2
7	RESERVED	R/W	Reserved

HDT2 or FDT2	HDT1 or FDT1	HDT1 or FDT1	Period
0	0	0	128 ms
0	0	1	256 ms
0	1	0	512 ms
0	1	1	1 s
1	0	0	2 s
1	0	1	4 s
1	1	0	8 s
1	1	1	16 s

Pin Configuration Register A : (Index = 48H)

Default = 0H

BIT	NAME	R/W	Function
0	PMSEL	W	Re configure Pin D10 (99), D11 (98), D12 (97), D131 (96)
1	LSRWCNTL	W	Enable 8250 LSR write function, Should be 1 to remain compatibility
2	DISCMD	W	Disable MEMR, MEMW command during On-Board Memory Cycle
3	SLOT16	W	Re-configure Pin A1-A12,SA1-SA12
4	ICRDSEL	W	Re-configure Pin CP2 (105), FRM (107), CP1 (106)
5	CARDAEN	W	Set Pin SPCLK (196) become Write Protect (WP) for PCMCIA Socket A
6	CARDBEN	W	Re-configure Pin D10 (99), D11 (98), D12 (97), D131 (96)
7	DISREG2	W	Re-configure Pin 227

Configuration Register B : (Index = 49H)

Default = 0H

BIT	NAME	R/W	Function
0	WPBSEL	W	Set Pin SYSCLK(158) as Write Protect (WP) for PCMCIA Socket B
1	RESERVED	W	Reserved
2	PMC4EN	W	Set LPH1(173) to function as PMC4
3	PMC5EN	W	Set LVEE(174) to function as PMC3
4	REGBEN	W	Set LVDD(175) to function as REGB
5	LPH1PMC4	W	Select LPH1 or PMC4
6	RESERVED	W	Reserved
7	RESERVED	W	Reserved

ICRDSEL Bit 4 in Reg. 48H	IS16BIT Bit 2 in Reg. 70H	CP1 Pin 106	CP2 Pin 105	FRM Pin 107
1	0	BVD1B	RDYB	BVD2B
0	1	PMC4	PMC5	PGP3
0	0	CP1	CP2	FRM

SLOT16	AEN	SA9	SA10	SA11	SA12	A9	A10	A11	A12
0	X	SA9	SA10	SA11	SA12	A9	A10	A11	A12
1	L	ICDIR	MCEAH	MCEBH	WPB	A9	A10	A11	A12
1	H	ICDIR	MCEAH	MCEBH	WPB	SA9	SA10	SA11	SA12

SLOT16	IS16BIT	A1-A8	SA1-SA8
1	1	A1-A8	SA1-SA8
1	0	A1-A8 OR SA1-SA8	IC CARD HIGH BYTE DATA

PM3SEL Bit 5 Reg. 44H	REGBEN Bit 4 Reg. 49H	Pin 175 Function as
X	1	RGB (REG for PCMCIA Socket B)
1	0	PMC3
0	0	LVDD

CARDAEN Bit 5 Reg. 48H	Pin 196 Function as
1	WPA (Write Protect for PCMCIA Socket A)
0	SPCK (Clock for UART)

ICDIR Bit 3 Reg. 44H	Pin 142 Function as
1	PCMCIA Data direction Control
0	SDDIR, XD bus direction Control

SMDDIR Bit 3 Reg. A7H	Pin 157 Function as
1	MDDIR, Memory Bus direction Control
0	3.5MHz Clock Output

ENOSCI4M Bit 7 Reg. A7H		Pin 122 Function as
1		OSC output. Same frequency as X14MIN (Pin 63)
0		PGP2

PMC5EN Bit 3 Reg. 49H		Pin 174 Function as
1		PMCS (Programmable Power Management Control 5)
0		LVEE

LPHIPMC4 Bit 5 Reg. 49H		Bit 1 Reg. 49H	Pin 54 Function as
1		1	
1		0	
0		X	SMIRDY

LPHIPMC4 Bit 5 Reg. 49H		PMC4EN Bit 2 Reg. 49H	Pin 173 Function as
X		1	PMC4
1		0	
0		0	LPH1

WPBSEL Bit 0 Reg. 49H		ENSYSCLK Bit 6 Reg. A7H	Pin 158 Function as
1		1	RDYB (Ready For PCMCIA Socket B)
1		0	WPB (Write Protect for PCMCIA Socket B)
0		1	SYSCLK
0		0	PMC6

R387SEL Bit 5 Reg. 6BH		Pin 195 Function as	Pin 175 Function as
0		PMC2	PMC3
1		80387SX RESET	80387SX ERROR

CARD2EN Bit 7 Reg. 70H		Pin 227 Function as	Pin 229 Function as	Pin 170 Function as
0		BVDA1	WPA	PGP1
1		REGB	MCEBL	CD2

DISD Bit 7 Reg. 8FH	LS16BIT Bit 2 Reg. 70H	CARDBEN Bit 6 Reg. 48H	PMSEL Bit 0 Reg. 48H	D10 Pin 99	D11 Pin 98	D12 Pin 97	D13 Pin 96
1	X	X	X	IRQ4	IRQ5	IRQ9	SBHE
X	1	X	X	IRQ4	IRQ5	IRQ9	SBHE
0	0	1	X	BVD1B	RDYB	BVD2B	VPPB
0	0	0	1	PMC3	PMC4	PMC5	PGP3
0	0	0	0	D10	D11	D12	SBHE

SLOT Memory Wait State Select Register-2 : (Index = 50H)
Default = 0H

BIT	NAME	R/W	Function
0	RDOSWS0	W	ROM (accessed by NDOS) wait state select 0
1	RDOSWS1	W	ROM (accessed by NDOS) wait state select 1
2	RDOSWSEN	W	ROM (accessed by NDOS) wait state enable
3	CARDWS0	W	8 bit PCMCIA Memory wait state select 0
4	CARDWS1	W	8 bit PCMCIA Memory wait state select 1
5	CARDWSEN	W	8 bit PCMCIA Memory wait state enable
6	RDOSCMDL	W	ROM (accessed by NDOS) command delay
7	CARDCMDL	W	8 bit PCMCIA Memory command delay

The following table shows the ROM wait state controls (ROMS which are accessed through signal "NDOS").

RDOSWSEN	RDOSWSI	RDOSWS0	ROM (accessed by NDOS) wait state
1	0	0	1 Wait
1	0	1	2 Wait
1	1	0	3 Wait
1	1	1	4 Wait
0	x	x	Controlled by bit 0, 1 in Register Index = 62H

The following table shows the 8 bit memory wait state controls for PCMCIA

CARDWSEN	CARDWSI	CARDWS0	8 bit PCMCIA memory cycle wait state
1	0	0	1 Wait
1	0	1	2 Wait
1	1	0	3 Wait
1	1	1	4 Wait
0	x	x	Controlled by bit 0, 1 in Register Index = 62H

RDOSWSEN	RDOSCMDL Bit 6 Reg. 50H	8MCD, Bit 2 Reg. 60H	ROM (accessed by NDOS) Memory Cycle Command Delay
0	X	0	1 SYSCLK cycle
0	X	1	0.5 SYSCLK cycle
1	1	X	0 Delay

CARDWSEN	RDOSCMDL Bit 6 Reg. 50H	8MCD, Bit 2 Reg. 60H	8 bit PCMCIA Memory Cycle Command Delay
0	X	0	1 SYSCLK cycle
0	X	1	0.5 SYSCLK cycle
1	1	X	0 Delay

ROM Configuration Register-2 : (Index = 51H)

Default = 0H

BIT	NAME	R/W	Function
0	ENROMA	W	NEPS is active(low) when address is within A0000 - AFFFF
1	ROM16	W	Select 16 bit ROM configuration. This bit is valid only when the 16 bit PCMCIA is enabled. (Pin SA1-SA8 are re-configured)

Command Delay Register : (Index = 60H)

This register is used to select different command delay to slot I/O and memory command.

BIT	NAME	R/W	Function
0	IOCD0	W	Bus I/O cycle command delay 0.
1	IOCD1	W	Bus I/O cycle command delay 1.
2	8MCD	W	8 bit slot memory cycle command delay 0.
3	X	W	Reserved-must be 0.
4	ROMWS0	W	EPROM wait state select 0.
5	X	W	Reserved-must be 0.
6	REFWS	W	Refresh wait state select 0.
7	ROMWS1	W	EPROM wait state select 1.

I/O command delay select: Act on address from 1F0 to 3FF.

IOCD1	IOCD0	Delayed by how many SYSCLK cycle(s)
0	0	1 (default, start of 2nd TC)
0	1	2 (start of 3rd TC)
1	X	0.5 (middle of TCI)

8 bit slot memory command delay select:

8MCD	Delayed by how many SYSCLK cycle(s)
0 (Default)	Delayed one clock cycle till start of 2nd TC
1	Delayed by half clock cycle till middle of TC

EPROM wait state select : The wait state control the wait state of ROMs which are controlled by signal NEPS (pin 141) during Non EMS cycles. In EMS cycles, the ROM wait states are controlled by Slot Memory Wait State Register (Index = 62H).

ROMWS1	ROMWS0	Delayed by how many SYSCLK cycle(s)
1	0	1
0	1	2
1	1	Not allowed
0	0 (Default)	3

Refresh cycle wait state select 0:

REFWS	Delayed by how many SYSCLK cycle(s)
1	Refresh cycle read command delayed by 2 SYSCLK cycles.
0 (Default)	Refresh cycle read command delayed by 3 SYSCLK cycles

I/O Wait State Register: (Index = 61H) .

This register defines the wait state for different I/O addresses.

Bit	NAME	R/W	Function
0	FDWS0	W	Wait state select 0 for FD.
1	FDWS1	W	Wait state select 1 for FD.
2	HDWS0	W	Wait state select 0 for HD.
3	HDWS1	W	Wait state select 1 for HD.
4	IOWS0	W	Select 0 for I/O wait state
5	IOWS1	W	Select 1 for I/O wait state
6	SPEED	W	CPU clock speed select, default is low speed (low)
7	DMAEMS	W	0: Disable EMS during DMA cycle (Default).1: Enable EMS in DMA cycle.

Floppy Disk (FD) wait state select: Act on address from 3F0 - 3F7.

FDWS1	FDWS0	Delayed by No. of SYSCLK cycle(s)
0	0	5 (Default)
0	1	4
1	0	3
1	1	2

Hard Disk (HD) wait state select: Act on address from 1F0 - 1F8.

HDWS1	HDWS0	Delayed by No. of SYSCLK cycle(s)
0	0	5 (Default)
0	1	4
1	0	3
1	1	2

I/O wait state select : Act on address from 100 to 3FF except from 3F0 - 3F7 & 1F0 - 1F8 and EMS I/O base address.

IOWS1	IOWS0	Delayed by No. of SYSCLK cycle(s)
0	0	5 (Default)
0	1	4
1	0	3
1	1	2

Note:

The wait state selected in the Wait State Register must be greater than the command delay specified in the Command Delay Register. The wait state of the other I/O address are controlled by the I/O Wait State Register.

Slot Memory Wait State Register : (Index = 62H)

This register defines the wait state for different slot memory addresses.

BIT	NAME	R/W	Function
0	8BMWS0	W	Wait state select 0 for 8 bit slot Memory
1	8BMWS1	W	Wait state select 1 for 8 bit slot Memory
2	16BMWS0	W	Wait state select 0 for 16 bit slot Memory
3	16BMWS1	W	Wait state select 1 for 16 bit slot Memory
4	MISOUT	W	Page mode bank miss & time-out wait state select, Low will select three wait states, High will select four wait states
5	NFROMEN	W	BIOS ROM Accessed by pin NEPS write enable. Default is disable (0)
6	NFRDOSEN	W	ROM Accessed by pin NDOS write enable. Default is disable (0)
7	CLKCHG	W	Reserved-must be low

8 bit slot memory wait state select:	
080000 ---- 09FFFF	if the address is on the slot
0A0000 ---- 0DFFFF	if the address is on the slot
100000 ---- FDFFFF	if the address is on the slot

BMWS1	8BMWS0	Delayed by No. of SYSCLK cycle(s)
0	0	5 (Default)
0	1	4
1	0	3
1	1	2

16 bit slot memory wait state select:	
080000 ---- 09FFFF	If the address is on the slot.
100000 ---- FDFFFF	If the address is on the slot.

16BMWS1	16BMWS0	Delayed by No. of SYSCLK cycle(s)
0	0	4 (Default)
0	1	3
1	0	2
1	1	1

Notes:

- On chip I/O accesses and 8042, RTC all have four wait states and one command delay
- Interrupt acknowledge cycle is one command delay and five wait states.

Wait State Control Register 2 (Index = 63H)

BIT	NAME	R/W	Function
0	SHUTD	W	Wait state select for shutdown cycle. default = 0, 16CLK cycle, if set the shutdown cycle will extend to 32 CLK cycle
1	RESERVED	W	Reserved
2	16IOWAIT	W	Wait state select for 16 bit I/O cycle. Default 16 bit I/O cycle will be one wait. If this bit is set, 16 bit I/O cycle will be two waits.
3	100WAIT	W	Wait state select 1 for I/O cycle with I/O address below 100H. Default I/O cycle with address below 100H will be four waits. If this bit is set, I/O cycle will be two waits.
4	M2WAIT	W	If DRAM is selected to run at one wait, setting this bit will force the DRAM to run at two waits. This bit has no effect on other DRAM modes
5	FCYCWAIT	W	Set DRAM first cycle wait state in page mode
6	BKMISS	W	Set DRAM bank miss wait state in page mode
7	SMISIZE	W	SMI Memory range select. Default is 16KB, when set SMI memory size will be 64KB

FCYCWAIT Bit 5, Reg. 63H	PFWS Bit 5, Reg. 65H	DRAM first cycle wait state in page mode
0	0	1 (Default)
0	1	2
1	0	3
1	1	3

BKMISS Bit 6, Reg. 63H	MISOUT Bit 4, Reg. 62H	DRAM Bank miss wait state in page mode
0	0	3 (Default)
0	1	4
1	0	5
1	1	5

Version Register: (Index = 64H) Read Only

BIT	NAME	R/W	Function
0--3	VER0-3	R	Version register
4--6	RESERVED	R	Reserved
7	RSMI	R	SMI active

Added 1 Register: (Index = 64H) Default = 0H, write only.

BIT	NAME	R/W	Function
0	REFSEL0	W	Refresh Interval select 0
1	REFSEL1	W	Refresh Interval select 1
2	RESERVED	W	Reserved-must be 0
3	SMIDEV	W	Must be set to 1 for SMI
4	512KPI	W	Reserved
5-6	RESERVED	W	Reserved-must be 0
7	RESERVED	W	Reserved-must be 1

REFSEL1	REFSEL0	Refresh Interval
0	0	Normal refresh interval divided by 8
0	1	Normal refresh interval divided by 6
1	0	Normal refresh interval divided by 4
1	1	Normal refresh interval divided by 2

ROM Configuration Register : (Index = 65H)

BIT	NAME	R/W	Function
0	ENROMF	R/W	NEPS is active (Low) when address is within F0000-FFFFF Default is enabled (0)
1	ENROME	R/W	NEPS is active (Low) when address is within E0000-EFFFF Default is disabled (0)
2	ENROMD	R/W	NEPS is active (Low) when address is within D0000-DFFFF Default is disabled (0)
3	ENROMC	R/W	NEPS is active (Low) when address is within C0000-CFFFF Default is disabled (0)
4	SHADOW	R/W	Shadow RAM enable. default = 0 disabled
5	PFWS	R/W	Page mode first cycle wait state select Default = 0(1 wait), if set then two wait states are added
6	ENEMSA	R/W	EMSA enable bit. Default = 0 = disable
7	DISW	R/W	Shadow RAM write protect. Default = 0 = protected

Switch 1 Register : (Index = 66H)

This register controls the memory size and operating mode of the TM8100A. Bit 5, 6, and 7 can be read in from appropriate pins during the reset period.

BIT	NAME	R/W	Function	I/O PIN
0	MS0	R/W	Memory operation mode select 0	
1	MS1	R/W	Memory operation mode select 1	
2	MSEL0	R/W	Memory bank configuration select 0	
3	MSEL1	R/W	Memory bank configuration select 1	
4	MSEL2	R/W	Memory bank configuration select 2	
5	P9EN	R/W	Select 386SX CPU .0==> 286CPU, 1==> 386SX	DTR
6	NA	R/W	Pipeline mode selection.(High enable pipeline mode)	RTS
7	CKSEL	R/W	Main Clock is 28.636MHz	DACK2

The TM8100 has a special mode to eliminate the needs for a 14.745MHZ crystal. If bit 7 is set, the TM8100A will assume that the MAIN clock input is 28.636MHz, and the TM8100A will automatically divide the MAIN clock by two and use the new clock to replace the clock source from the crystal oscillator.

Memory operation mode switch:

MS1	MS0	MODE
0	0	Non page mode zero wait
0	1	Non page mode one wait (Reserved)
1	0	Page mode
1	1	Reserved

Memory configuration:

MS2	MS1	MS0	Total Memory	BANK0	BANK1
0	0	1	1M	512	X
0	1	0	2M	512	512
0	1	1	2M	1M	X
1	0	0	4M	1M	1M
1	0	1	8M	4M	X
1	1	0	16M	4M	4M

CKSEL = 0

SPEED	CPU CLK	SYNSCLK	8042 CLK	DMA CLK	8254 CLK	8250
HIGH	32	16	7.15	3.6	1.19	1.79
LOW	14.318	7.15	7.15	3.6	1.19	1.79

SPEED	CPU CLK	SYSCLK	8042 CLK	DMA CLK	8254 CLK	8250
HIGH	28.636	14.3	7.15	3.6	1.19	1.79
LOW	14.3	7.15	7.15	3.6	1.193	1.79

EMSA Address Extension Register-1 : (Index = 67H)
 EMSA Address Extension Register for page 4-7

BIT	NAME	R/W	Function
0	E4A21	R/W	EMSA page 4 address extension Bit 21
1	E4A22	R/W	EMSA page 4 address extension Bit 22
2	E5A21	R/W	EMSA page 5 address extension Bit 21
3	E5A22	R/W	EMSA page 5 address extension Bit 22
4	E6A21	R/W	EMSA page 6 address extension Bit 21
5	E6A22	R/W	EMSA page 6 address extension Bit 22
6	E7A21	R/W	EMSA page 7 address extension Bit 21
7	E7A22	R/W	EMSA page 7 address extension Bit 22

Shadow RAM Enable Register-1 : (Index = 68H)
 This register control the shadow RAM mapping range. Default = 0H, disable.

BIT	NAME	R/W	Function
0	SC03	R/W	Enable shadow RAM at C0000-C3FFF
1	SC47	R/W	Enable shadow RAM at C4000-C7FFF
2	SC8B	R/W	Enable shadow RAM at C8000-CBFFF
3	SCCF	R/W	Enable shadow RAM at CC000-CFFFF
4	SD03	R/W	Enable shadow RAM at D0000-D3FFF
5	SD47	R/W	Enable shadow RAM at D0000-D7FFF
6	SD8B	R/W	Enable shadow RAM at D8000-DBFFF
7	SDCF	R/W	Enable shadow RAM at DC000-DFFFF

Shadow RAM Enable Register-2 : (Index = 69H)
 This register control the shadow RAM mapping range. Default = 0H, disable.

BIT	NAME	R/W	Function
0	SE03	R/W	Enable shadow RAM at E0000-E3FFF
1	SE47	R/W	Enable shadow RAM at E4000-E7FFF
2	SE8B	R/W	Enable shadow RAM at E8000-EBFFF
3	SEDF	R/W	Enable shadow RAM at EC000-EFFFF
4	SF03	R/W	Enable shadow RAM at F0000-F3FFF
5	SF47	R/W	Enable shadow RAM at F0000-F7FFF
6	SF8B	R/W	Enable shadow RAM at F8000-FBFFF
7	SFCF	R/W	Enable shadow RAM at FC000-FFFFF

Pin Selection Register : (Index = 6BH)

BIT	NAME	R/W	Function
0	AMDSMI	W	Must be set to 1 for AMD CPU to enable SMI function
5	R387SEL	W	When Set, PMC2 becomes 387RESET and PMC3 becomes 387ERROR
6	PARTSEL	W	When set, LPH1 & LPH2 become PTYL & PTYH
1-4,7	RESERVED	W	Reserved

EMSA/B Address Extension Register-1 : (Index = 6CH)

EMSA/B Address Extension Register for address bit EA23.

BIT	NAME	R/W	Function
0	E0A23	R/W	EMSA/B page 0 address extension Bit 23
1	E1A23	R/W	EMSA/Bpage 1 address extension Bit 23
2	E2A23	R/W	EMSA/Bpage 2 address extension Bit 23
3	E3A23	R/W	EMSA/Bpage 3 address extension Bit 23
4	E4A23	R/W	EMSA/Bpage 4 address extension Bit 23
5	E5A23	R/W	EMSA/Bpage 5 address extension Bit 23
6	E6A23	R/W	EMSA/Bpage 6 address extension Bit 23
7	E7A23	R/W	EMSA/Bpage 7 address extension Bit 23

EMSA/B Address Select Register : (Index = 6DH)

This register selects the base I/O addresses and page addresses.

BIT	NAME	R/W	Function
0	EMIO0	R/W	EMSA/Bpage register(s) I/O address select 0
1	EMIO1	R/W	EMSA/Bpage register(s) I/O address select 1
2	EMIO2	R/W	EMSA/Bpage register(s) I/O address select 2
3	EMIO3	R/W	EMSA/Bpage register(s) I/O address select 3
4	EMBA0	R/W	EMSA/Bbase address select 0
5	EMBA1	R/W	EMSA/Bbase address select 1
6	EMBA2	R/W	EMSA/Bbase address select 2
7	EMBA3	R/W	EMSA/Bbase address select 3

EMSA/B Page Register I/O address

BIT	Page register I/O address			
3 2 1 0	Page 0	Page 2	Page 4	Page 6
0 0 0 0	208H/209H	4208H/4209H	8208H/8209H	C208H/C209H
0 0 0 1	218H/219H	4218H/4219H	8218H/8219H	C218H/C219H
0 1 0 1	258H/259H	4258H/4259H	8258H/8259H	C258H/C259H
0 1 1 0	268H/269H	4268H/4269H	8268H/8269H	C268H/C269H
1 0 1 0	2A8H/2A9H	42A8H/42A9H	82A8H/82A9H	C2A8H/C2A9H
1 0 1 1	2B8H/2B9H	42B8H/42B9H	82B8H/82B9H	C2B8H/C2B9H
1 1 1 0	2E8H/2E9H	42E8H/42E9H	82E8H/82E9H	C2E8H/C2E9H

BIT	Page register I/O address			
3 2 1 0	Page 1	Page 3	Page 5	Page 7
0 0 0 0	2208/2209H	6208/6209H	A208/A209H	E208/E209H
0 0 0 1	2218/2219H	6218/6219H	A218/A219H	E218/E219H
0 1 0 1	2258/2259H	6258/6259H	A258/A259H	E258/E259H
0 1 1 0	2268/2269H	6268/6269H	A268/A269H	E268/E269H
1 0 1 0	22A8/22A9H	62A8/62A9H	A2A8/A2A9H	E2A8/E2A9H
1 0 1 1	22B8/22B9H	62B8/62B9H	A2B8/A2B9H	E2B8/E2B9H
1 1 1 0	22E8/22E9H	62E8/62E9H	A2E8/A2E9H	E2E8/E2E9H

EMSA/B Base Registers

BIT	Page register I/O address							
7 6 5 4	page 0	page 1	page 2	page 3	page 4	page 5	page 6	page 7
0 0 0 0	C0000	C4000	C8000	CC000	D0000	D4000	D8000	DC000
0 0 0 1	C4000	C8000	CC000	D0000	D4000	D8000	DC000	E0000
0 0 1 0	C8000	CC000	D0000	D4000	D8000	DC000	E0000	E4000
0 0 1 1	CC000	D0000	D4000	D8000	DC000	E0000	E4000	E8000
0 1 0 0	D0000	D4000	D8000	DC000	E0000	E4000	E8000	EC000
0 1 0 1	D4000	D8000	DC000	E0000	E4000	E8000	EC8000	F0000

Page Register

BIT	NAME	R/W	Function
0	EA14	R/W	EMSA/Btranslate address Bit A14
1	EA15	R/W	EMSA/Btranslate address Bit A15
2	EA16	R/W	EMSA/Btranslate address Bit A16
3	EA17	R/W	EMSA/Btranslate address Bit A17
4	EA18	R/W	EMSA/Btranslate address Bit A18
5	EA19	R/W	EMSA/Btranslate address Bit A19
6	EA20	R/W	EMSA/Btranslate address Bit A20
7	PAGEEN	R/W	0 = page disable, 1 = page enable

EMSA/B Address Extension Register-2 : (Index = 6EH)

This register contains the upper two bits for the EMSA/B Page Register.

BIT	R/W	Function
0	R/W	EMSA/Bpage 0 address extension Bit 21
1	R/W	EMSA/Bpage 0 address extension Bit 22
2	R/W	EMSA/Bpage 1 address extension Bit 21
3	R/W	EMSA/Bpage 1 address extension Bit 22
4	R/W	EMSA/Bpage 2 address extension Bit 21
5	R/W	EMSA/Bpage 2 address extension Bit 22
6	R/W	EMSA/Bpage 3 address extension Bit 21
7	R/W	EMSA/Bpage 3 address extension Bit 22

Note:

To program EMSA/B, Software must first program Register (Index = 6DH) to select the base I/O address and base Page Registers address. Before EMSA/B can be enabled, the Page Register and the Address Extension Register (Index =6EH) must be programmed.

Miscellaneous Register : (Index = 6FH)

BIT	NAME	R/W	Function
0	GATEA20	R/W	A20GATE control, 1: A20 = CPUA20, Default A20 = 0
1	RESCPU	R/W	CPU reset. A low to high transition in this bit will automatically reset CPU. The reset will last for 16 PROCLK cycles.
2	DMWS	R/W	DMA wait state, 0=>1 wait (Default), 1 =>2 waits
3	MRDLY	R/W	DMA MEMR DELAY 1: Delay MEMR command by one DMACK cycle 0: NO delay for MEMR Default).
4	EMSZ0	R/W	EMS memory range Select 0
5	EMSZ1	R/W	EMS memory range Select 1
6	EMSZ2	R/W	EMS memory range Select 2
7	EMSZ3	R/W	EMS memory range Select 3

BIT	EMS memory range	BIT	EMS memory range
7 6 5 4	None	7 6 5 4	8 MB
0 0 0 0	1 MB	1 0 0 1	9 MB
0 0 0 1	2 MB	1 0 1 0	10 MB
0 0 1 1	3 MB	1 0 1 1	11 MB
0 1 0 0	4 MB	1 1 0 0	12 MB
0 1 0 1	5 MB	1 1 0 1	13 MB
0 1 1 0	6 MB	1 1 1 0	14 MB
0 1 1 1	7 MB	1 1 1 1	15 MB

Switch 2 Register : (Index = 70H)

BIT	NAME	R/W	Function
0	MTS	R/W	Memory type select 0, Default = 0, DRAM, 1 = SRAM
1	ENRTC	R/W	Enable internal RTC when set. Default = 0
2	IS16BIT	R/W	Slot type select; 0: 16 BIT SLOT/6330 display
3	SLOT1	R/W	Slot type select 1: 8 BIT SLOT/printer port
4	RESERVED	R/W	Reserved
5	SACIN	R/W	Software ACIN input, When set, all PMU functions will be disabled
6	PGP0DIR	R/W	PGP 0 PIN Direction .0--> input , 1 --> output,
7	CARD2EN	R/W	Socket Card 2 installed; 0 (Default): not installed , 1: installed

SLOT1	IS16BIT	Description
0	0	CGA LCD and Printer are enabled
0	1	Printer port enabled, CGA LCD disabled
1	0	CGA LCD enabled, Printer disabled
1	1	Printer and CGA LCD are both disabled and 16 BIT slot is enabled

EMSA Device Selection Register-1 : (Index = 71H)

This register selects the peripheral device each EMSA page will control.

BIT	NAME	R/W	Function
0	EMDP00	R/W	EMSA page 0 for device type select Bit 0
1	EMDP01	R/W	EMSA page 0 for device type select Bit 1
2	EMDP10	R/W	EMSA page 1 for device type select Bit 0
3	EMDP11	R/W	EMSA page 1 for device type select Bit 1
4	EMDP20	R/W	EMSA page 2 for device type select Bit 0
5	EMDP21	R/W	EMSA page 2 for device type select Bit 1
6	EMDP30	R/W	EMSA page 3 for device type select Bit 0
7	EMDP31	R/W	EMSA page 3 for device type select Bit 1

Note: PCMCIA Socket A and Socket B EMSA pages are selected by Index = A8H

Page 0 EMSA device select:

BIT	Selected device.
1 0	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA Card
1 1	EMS BIOS

Page 2 EMSA device select:

BIT	Selected device.
5 4	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA Card
1 1	EMS BIOS

Page 1 EMSA device select:

BIT	Selected device
3 2	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA Card
1 1	EMS BIOS

Page 3 EMSA device select:

BIT	Selected device
7 6	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA Card
1 1	EMS BIOS

EMSA Device Selection Register-2 : (Index = 72H)
 This register select the peripheral device each EMSA page will control.

BIT	NAME	R/W	Function
0	EMDP40	R/W	EMSA page 4 for device type select Bit 0
1	EMDP41	R/W	EMSA page 4 for device type select Bit 1
2	EMDP50	R/W	EMSA page 5 for device type select Bit 0
3	EMDP51	R/W	EMSA page 5 for device type select Bit 1
4	EMDP60	R/W	EMSA page 6 for device type select Bit 0
5	EMDP61	R/W	EMSA page 6 for device type select Bit 1
6	EMDP70	R/W	EMSA page 7 for device type select Bit 0
7	EMDP71	R/W	EMSA page 7 for device type select Bit 1

Page 4 EMSA device select:

BIT	Selected device
1 0	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA Card
1 1	EMS BIOS

Page 6 EMSA device select:

BIT	Selected device
5 4	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA Card
1 1	EMS BIOS

Page 5 EMSA device select:

BIT	Selected device
3 2	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA Card
1 1	EMS BIOS

Page 7 EMSA device select:

BIT	Selected device
7 6	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA Card
1 1	EMS BIOS

EMSB Device Selection Register-2 : (Index = 73H)
 This register select the peripheral device each EMSB page will control

BIT	NAME	R/W	Function
0	EM1DP00	R/W	EMSB page 0 for device type select Bit 0
1	EM1DP01	R/W	EMSB page 0 for device type select Bit 1
2	EM1DP10	R/W	EMSB page 1 for device type select Bit 0
3	EM1DP11	R/W	EMSB page 1 for device type select Bit 1
4	EM1DP20	R/W	EMSB page 2 for device type select Bit 0
5	EM1DP21	R/W	EMSB page 2 for device type select Bit 1
6	EM1DP30	R/W	EMSB page 3 for device type select Bit 0
7	EM1DP31	R/W	EMSB page 3 for device type select Bit 1

Note: PCMCIA Socket A and Socket B EMSB pages are selected by Index = A9H

Page 0 EMSB device select:

BIT	Selected device
1 0	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA CARD
1 1	EMS BIOS

Page 2 EMSB device select:

BIT	Selected device
5 4	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA CARD
1 1	EMS BIOS

Page 1 EMSB device select:

BIT	Selected device
3 2	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA CARD
1 1	EMS BIOS

Page 3 EMSB device select:

BIT	Selected device
7 6	
0 0	ROMDOS
0 1	Reserved
1 0	PCMCIA CARD
1 1	EMS BIOS

EMSB Control Register : (Index = 74H)

Default = 0H.

BIT	NAME	R/W	Function
0	ENEMSB	R/W	Enable EMSB
1	EMSABSEL	R/W	EMSA & EMSB select Bit (Default = 0 --> EMSB)
2	PGP1DIR	R/W	PGP 1 Pin Direction 0-> input, 1 --> output,
3	ENPMCIRQ0	R/W	Enable IRQ0 active in DOZE mode.
4	IC_IOSEL	R/W	If set to 1, Card in socket one is an I/O card, default is set to 0
5	IC_IOEN	R/W	IC Card's I/O function Enable
6	NENLB2	R/W	If set to 1, LB2 input is masked
7	NENLB4	R/W	If set to 1, LB2 input is masked

Note:

EMSB uses the same I/O address for the Page Register and Address Extension Register as EMSA page 0-3, If EMSA/BSEL is set to 1, then an I/O cycle will access EMSA, otherwise an I/O cycle will access EMSB.

Programmable Activity Mask Register-1 : (Index = 75H)

Default is enabled.

BIT	NAME	R/W	Function
0	DRQ5-7	R/W	Activity (high) on DRQ5-7 will be counted as activity
1	DRQ1	R/W	Activity (high) on DRQ1 will be counted as activity
2	DRQ2	R/W	Activity (high) on DRQ2 will be counted as activity
3	DRQ3	R/W	Activity (high) on DRQ3 will be counted as activity
4	KB	R/W	Keyboard Interrupt will be counted as activity
5	EMS	R/W	EMS cycle will be counted as activity
6	ACIN	R/W	AC adapter input will be counted as activity
7	INT	R/W	Interrupt will be counted as activity

Programmable Activity Mask Register-2 : (Index = 76H)

Default is enabled. Memory Range Register is on Index = 9AH and 9BH.

BIT	NAME	R/W	Function
0	LPT	R/W	LPT1, LPT2, LPT3. (378-37F, 278-27F, 3B8-3BF) will be counted as activity
1	FD	R/W	Floppy Driver. (I/O Port = 3F0-3F7) will be counted as activity
2	HD	R/W	Hard disk. (I/O Port = 1F0-1F7) will be counted as activity
3	COM	R/W	COM1, COM2, COM3, COM4. (I/O Port = 3F8-3FF, 2F8-2FF) will be counted as activity
4	PIO0	R/W	Programmable I/O Devices Register 0 will be counted as activity. Refer to Index = 8CH.
5	PIO1	R/W	Programmable I/O Devices Register 1 will be counted as activity. Refer to Index = 8DH.
6	VD	R/W	Video memory Write . -> A0000-BFFFF memory write will be counted as activity
7	PMW	R/W	Programmable memory range write access will be counted as activity

RTC Alarm Enable Register : (Index = 77H)

Default = 00H.

BIT	NAME	R/W	Function
0	ENDAY	R/W	Enable internal RTC day-alarm
1	ENSEC	R/W	Enable internal RTC second-alarm
2	ENALIRQ	R/W	Enable Alarm Interrupt
3	AUTOFF	R/W	Enable CPU Auto power down mode
4	UART_EN	R/W	Internal UART enable
5	UART_IOP	R/W	"0" will select internal UART I/O address as 3F8-3FF "1" will select internal UART I/O address as 2F8-2FF
6	UART_IR3	R/W	Select internal UART IRQ =IR3
7	UART_IR4	R/W	Select internal UART IRQ =IR4

RTC Second (LSB) Register : (Index = 78H)

Default = 00H, read/write.

RTC Second (MSB) Register : (Index = 79H)

The default value is 00H, read/write.

RTC Half-Day (LSB) Register : (Index = 7AH)

Default = 00H, read/write.

RTC Half-Day (MSB) Register : (Index = 7BH)

Default = 00H, read/write.

RTC ALARM Second (LSB) Register : (Index = 7CH)

Default = 00H, read/write.

RTC ALARM Second (MSB) Register : (Index = 7DH)

Default = 00H read/write.

RTC ALARM Half-Day (LSB) Register : (Index = 7EH)

Default = 00H, read/write.

RTC ALARM Half -Day (MSB) Register : (Index = 7FH)

Default = 00H, read/write.

Programmable Power Control Register -1 : (Index = 80H)

This register controls the PMC0, PMC1, PMC2, and LVDD output pins in FULL ON mode and DOZE mode. The initial default = 00H.

BIT	NAME	R/W	Function
0	FO-0	R/W	Control PMC0 in FULL ON and ON Mode
1	FO-1	R/W	Control PMC1 in FULL ON and ON Mode
2	FO-2	R/W	Control PMC2 in FULL ON and ON Mode
3	FO-14M	R/W	Disable the 14.318M crystal oscillator in SLEEP Mode
4	DZ-0	R/W	Control PMC0 in DOZE Mode
5	DZ-1	R/W	Control PMC1 in DOZE Mode
6	DZ-2	R/W	Control PMC2 in DOZE Mode
7	DZ-14M	R/W	Disable the 14.318M crystal oscillator in SUSPEND Mode

Programmable Power Control Register-2: (Index = 81H)

This register control the PMC0, PMC1, PMC2, and LVDD output pins in Full On mode and DOZE mode. The initial default = 00H.

BIT	NAME	R/W	Function
0	SP-0	R/W	Control PMC0 in SLEEP Mode.
1	SP-1	R/W	Control PMC1 in SLEEP Mode.
2	SP-2	R/W	Control PMC2 in SLEEP Mode.
3	SP-14M	R/W	Disable the 14.318M crystal oscillator in FULL ON Mode
4	SU-0	R/W	Control PMC0 in SUSPEND Mode.
5	SU-1	R/W	Control PMC1 in SUSPEND Mode.
6	SU-2	R/W	Control PMC2 in SUSPEND Mode.
7	SU-14M	R/W	Disable the 14.318M crystal oscillator in FULL ON Mode

Note:

Even PMC pin (PMC0, 2, 4, 6) initial state after power on is low, when bit is set to low, the corresponding PMC output is Low. Odd PMC pin (PMC1, 3, 5, 7) initial state after power on is high, when bit is set to low, the corresponding PMC output is High

Programmable NMI or SMI Enable Register : (Index = 82H)

This register is used to enable the generation of NMI or SMI during different conditions such as Mode change or Battery low. The initial default = 00H (disabled). SMI or NMI is selected by Bit 7 of Register (Index = A9).

BIT	NAME	R/W	Function
0	RESU	R/W	RESUME pin will generate NMI or SMI
1	ON	R/W	PMU will generate NMI or SMI before entering DOZE mode from ON mode
2	DZ	R/W	PMU will generate NMI or SMI before entering SLEEP mode from DOZE mode
3	SLP	R/W	PMU will generate NMI or SMI before entering SUSPEND mode from SLEEP mode
4	SUS	R/W	PMU will generate NMI or SMI before entering OFF mode from SUSPEND mode
5	BL1	R/W	Battery low warning 1 generates a NMI.
6	BL2	R/W	Battery low warning 2 generates a NMI and force enter to sleep mode
7	BL3	R/W	Lithium backup battery low warning generates a NMI

FULL ON Mode Programmable Timer Register : (Index = 83H)

Default = 00H. This register is used to program the time-out period from FULL ON mode to ON mode. The minimum period is 1/512 second, the maximum is 0.5 second. A value of 00H will disable the timer. If during timer counting period, any activities are detected, the counter is reset to 0 automatically.

Read/write.

ON Mode Programmable Timer Register : (Index = 84H)

Default = 00H. This register is used to program the time-out period from ON mode to DOZE mode. The minimum period is 1/16 second, the maximum is 16 second. A value of 00H will disable the timer. If during timer counting period, any activities are detected, the counter is reset to 0 automatically and return to FULL ON mode. Read/write.

DOZE Mode Programmable Timer Register : (Index = 85H)

Default = 00H. This register is used to program the time-out period from DOZE mode to SLEEP mode. The minimum period is 4 second, the maximum is 64 minutes. A value of 00H will disable the timer. If during timer counting period, any activities are detected, the counter is reset to 0 automatically and return to FULL ON mode. Read/write.

SLEEP Mode Programmable Timer Register : (Index = 86H)

Default = 00H. This register is used to program the time-out period from SLEEP mode to SUSPEND mode. The minimum period is 1/16 second, the maximum is 16 seconds. A value of 00H will disable the timer. If during timer counting period, special activity such as RESUME key or designated interrupts are detected, the counter is reset to 0 automatically, and the system returns to FULL ON mode. Read/write.

SUSPEND Mode Programmable Timer Register : (Index = 87H)

Default = 00H. This register is used to program the time-out period from SUSPEND mode to OFF mode. The minimum period is 1 minute, the maximum is 256 minutes. A value of 00H will disable timer. If during timer counting period, special activity such as RESUME key or designated interrupts are detected, the counter is reset to 0 automatically and the system returns to FULL ON mode. Read/write.

Software Mode Control Register : (Index = 88H)

Default = 00H, write only.

BIT	NAME	R/W	FUNCTION
0	SPC0	W	Software command control Bit 0
1	SPC1	W	Software command control Bit 1
2	SPC2	W	Software command control Bit 2
3-7	RESERVED	W	Reserved

SPC2	SPC1	SPC0	Mode
0	0	0	software command the system enter to FULL-ON mode
1	0	0	software command the system enter to ON mode
0	0	1	software command the system enter to DOZE on mode
0	1	1	software command the system enter to SLEEP mode
0	1	0	software command the system enter to SUSPEND mode

Programmable General Purpose I/O Register 0 [PGP0] : (Index = 89H)

This register is used by the software to program the I/O address that Pin PGP0 will respond to. In other words, if this register is programmed as 1FH then PGP0 will respond to an I/O cycle with address F8-FF. Default = 00H, write only. When used as output pin, the PGP0 can be programmed to be gated with I/O read or I/O write or both or not gated with any command (Programmed by Register (Index = 91)). When used as output, the value of PGP0 output is the same as CPU data 0 except when PGP0 output is not gated with any I/O command, then the output value of PGP0 will be the invert of bit 7(DX).

DX	A9	A8	A7	A6	A5	A4	A3
----	----	----	----	----	----	----	----

Reserved Register : (Index = 8AH)**Programmable Socket A VPPA Address Decode Register : (Index = 8BH)**
Reserved, must be 0.

A9	A8	A7	A6	A5	A4	A3	A2
----	----	----	----	----	----	----	----

Programmable I/O Activity Address Register 0 : (Index = 8CH)

This register is used by the PMU software to program the I/O address that the Activity Monitor will check (Register 76 bit 4). Default = 00H, write only.

X	A9	A8	A7	A6	A5	A4	A3
---	----	----	----	----	----	----	----

Programmable I/O Activity Address Register 1: (Index = 8DH)

This register is used by the PMU software to program the I/O address that the Activity Monitor will check (Register 76 bit 5). Default = 00H, write only.

X	A9	A8	A7	A6	A5	A4	A3
---	----	----	----	----	----	----	----

Clock Control Register : (Index = 8FH)

This register is used to program the crystal restart delay time & CPU restart delay time.

BIT	NAME	R/W	Function
0	XST0	W	Crystal restart time select 0
1	XST1	W	Crystal restart time select 1
2	XST2	W	Crystal restart time select 2
3	RESERVED	W	Reserved
4	D1MS	W	From Non-FULL-ON mode back to FULL-ON will add 1 ms delay, that is CPU clock will be delayed by 1 ms. Default = 0, No delay
5	ICIRQ5	W	IRQ5 input select. When Set to one, Pin IRQ5 is don't care and 8259 IR5 is connected to PC card's IRQ
6	ICIRQ7	W	IRQ7 input select. When Set to one, Pin IRQ7 is don't care and 8259 IR7 is connected to PC card's IRQ
7	DISD	W	Pin DD10..DD13 Function control. If set to one, DD10..DD13 will function as IRQ4, IRQ5, IRQ9, SBHE regardless of the bit setting (bit 2, 3) in register 70 if bit 6 in register 48H is zero. Default = 0

XST2	XST1	XST0	Crystal restart time for 14.318MHz
0	0	0	4 ms
0	0	1	8 ms
0	1	0	16 ms
0	1	1	32 ms
1	0	0	64 ms
1	0	1	128 ms
1	1	0	256 ms
1	1	1	1 Sec

LHP1 Programmable I/O Address Register : (Index = 90H)

This register is used by software to program the I/O address for pin LHP1. Default = 00H, write only.

A9	A8	A7	A6	A5	A4	A3	A2
----	----	----	----	----	----	----	----

PGP Pin Command Select Register : (Index = 91H)

Default = 00H, write only.

BIT	NAME	R/W	Function
0	PG0-IO0	W	Program general purpose pin 0 gate control Bit 0
1	PG0-IO1	W	Program general purpose pin 0 gate control Bit 1
2	PG1-IO0	W	Program general purpose pin 1 gate control Bit 0
3	PG1-IO1	W	Program general purpose pin 1 gate control Bit 1
4	PG2-IO0	W	Program general purpose pin 2 gate control Bit 0
5	PG2-IO1	W	Program general purpose pin 2 gate control Bit 1
6	PG3-IO0	W	Program general purpose pin 3 gate control Bit 0
7	PG3-IO1	W	Program general purpose pin 3 gate control Bit 1

PG0-IO0	PG0-IO1	PGP0 Output
0	0	PGP0 output equals register (Index = 89) bit 7's invert
0	1	PGP0 will gate with I/O Write Command
1	0	PGP0 will gate with I/O Read Command
1	1	PGP0 will gate with I/O Read or Write Command

PG1-IO0	PG1-IO1	PGP1 Output
0	0	PGP1 output equals register (Index = 89) bit 7's invert
0	1	PGP1 will gate with I/O Write Command
1	0	PGP1 will gate with I/O Read Command
1	1	PGP1 will gate with I/O Read or Write Command

PG2-IO0	PG2-IO1	PGP2 Output
0	0	If register (Index = 9C) bit 7 is set then in AUTOOFF mode, PGP2 output will be forced low
0	1	PGP2 will gate with I/O Write Command
1	0	PGP2 will gate with I/O Read Command
1	1	PGP2 will gate with I/O Read or Write Command

PG3-IO0	PG3-IO1	PGP3 Output
0	0	If register (Index = 9C) bit 7 is set then in AUTOOFF mode, PGP3 output will be forced low.
0	1	PGP3 will gate with I/O Write Command
1	0	PGP3 will gate with I/O Read Command
1	1	PGP3 will gate with I/O Read or Write Command

Internal UART Clock Enable Register : (Index = 92H)
Default = 00H, write only.

BIT	NAME	R/W	Function
0	ENCLK	W	Enable clock to internal UART
1	CKSEL	W	Select clock source for UART, When set high, clock comes from pin 196 (X184M). Default = 0, use 14.318M as clock source
2-7	RESERVED	W	Reserved

Reserved Register : (Index = 93H)
Write only, must be 0H.

Programmable General Purpose I/O Register-2 [PGP2] : (Index = 94H)

This register is used by the software to program the I/O address for Pin PGP2, in other words, if this register is programmed as 1FH, then PGP2 will respond to an I/O cycle with address F8-FF. Default = 00H, write only. When used as an output pin, PGP2 can be programmed to be gated with I/O read or I/O write or both or not gated with any command (Programmed by Register (Index = 91H)). When used as an output, the value of PGP2 output is the same as CPU data 0 except when PGP2 output is not gated with any I/O command, then the output value of PGP2 will be forced low when in OFF Mode.

DX	A9	A8	A7	A6	A5	A4	A3
----	----	----	----	----	----	----	----

Programmable General Purpose I/O Register-3 [PGP3] : (Index = 95H)

This register is used by the software to program the I/O address for Pin PGP3 , in other words, if this register is programmed as 1FH, then PGP3 will respond to an I/O cycle with address F8-FF. The default value is 00H write only. When used as output pin, the PGP3 can be programmed to be gated with I/O read or I/O write or both or not gated with any command(Programmed by register (Index = 91H)). When used as an output, the value of PGP3 output is the same as CPU data 0 except when PGP3 output is not gated with any I/O command, then the output value of PGP3 will be forced low in the OFF mode.

DX	A9	A8	A7	A6	A5	A4	A3
----	----	----	----	----	----	----	----

Programmable PCMCIA I/O Window Address Register (Low Byte) : (Index = 96H)
Reserved, must be 0.

Programmable PCMCIA I/O Window Address Register (High Byte) : (Index = 97H)
Reserved, must be 0.

Programmable PCMCIA I/O Window Mask Register (Low Byte) : (Index = 98H)
Reserved, must be 0.

Programmable PCMCIA I/O Window Mask Register (High Byte) : (Index = 99H)
Reserved, must be 0.

Programmable Memory Write Activity Low Address Register : (Index = 9AH)

This register specifies the low memory address that the activity monitor will count as an activity. This activity is enable/mask by bit 7 of Register (Index = 76H). Default = 00H, write only.

BIT	NAME	R/W	Function
0	ENHIT	W	Enable memory write activity
1	RESERVED	W	Reserved
2	LSA14	W	Memory address SA14
3	LSA15	W	Memory address SA15
4	LSA16	W	Memory address SA16
5	LSA17	W	Memory address SA17
6	LSA18	W	Memory address SA18
7	LSA19	W	Memory address SA19

Programmable Memory Write Activity High Address Register : (Index = 9BH)

This register specifies the low memory address that the activity monitor will count as an activity. This activity is enable/mask by bit 7 of register (Index = 76H). Default = 00H, write only.

BIT	NAME	R/W	Function
0-2	SC2-SC0	W	Counter select Bit 2-0
3	RESERVED	W	Reserved
4	HSA16	W	Memory address SA16
5	HSA17	W	Memory address SA17
6	HSA18	W	Memory address SA18
7	HSA19	W	Memory address SA19

BIT 2 1 0	HIT Count Limit
0 0 0	1
0 0 1	2
0 1 0	4
0 1 1	8
1 0 0	16
1 0 1	32
1 1 0	64
1 1 1	128

If the Hit count limit is set to 2, then if more than two memory write cycles fall into the range specified by the address range then it will be counted as an activity. If bit 0 of register (Index = 9AH) is not set then this function will be disabled.

Programmable General Purpose I/O Register-1 [PGP1] : (Index = 9CH)

This register is used by the software to program the I/O address for Pin PGP1, in other words, if this register is programmed as 1FH, then PGP1 will respond to an I/O cycle with address F8-FF. When used as an output pin, the PGP1 can be programmed to be gated with I/O read or I/O write or both or not gated with any command (Programmed by register (Index = 91)). When used as output, the value of PGP1 output is the same as CPU data 0 except when PGP1 output is not gated with any I/O command, then the output value of PGP1 will be the invert of bit 7(DX). Default = 00H, write only

DX	A9	A8	A7	A6	A5	A4	A3
----	----	----	----	----	----	----	----

(Index = 9DH) : Reserved must be 40H.

Programmable Socket B REGB Address Decoder Register : (Index = 9EH)

This register is used by the software to program the I/O address for Pin REGB. The Logic level of REGB is the same as CPU data 0. Default = 00H, write only

A9	A8	A7	A6	A5	A4	A3	A2
----	----	----	----	----	----	----	----

Auto Low Speed Control Register: (Index = 9FH)

This register control the Auto Low Speed interval. Default = 00H, write only.

BIT	NAME	R/W	Function
0	T0	W	Trigger period 0
1	T1	W	Trigger period 1
2	Low Speed 0	W	Stop period Bit 0
3	Low Speed 1	W	Stop period Bit 1
4-7	RESERVED		Reserved

Trigger period select:

T1	T0	Trigger period
0	0	15 SEC
0	1	30 SEC
1	0	1 MIN
1	1	2 MIN

Low Speed period select:

Low Speed 1	Low Speed 0	Low Speed period
0	0	0.25 SEC
0	1	0.5 SEC
1	0	1 SEC
1	1	2 SEC

Activity Monitor Status Register-1 : (Index = A0H) High : Activity Active.

This register contains the activity status of all system peripherals and signals. A one indicates activity. Software has to clear this register after a read by writing 0H.

BIT	NAME	R/W	Function
0	DRQ57	RW	DRQ5-7 was detected active
1	DRQ1	RW	DRQ1 was detected active
2	DRQ2	RW	DRQ2 was detected active
3	DRQ3	RW	DRQ3 was detected active
4	KB	RW	Keyboard was detected active
5	EMS	RW	EMS was detected active
6	ACIN	RW	AC adapter input was detected active
7	INT	RW	Interrupt was detected active

Note: INT includes all interrupts from IRQ2 till IRQ15 except IRQ0 (TIMER) and IRQ1

Activity Monitor Status Register-2 : (Index = A1H) High : Activity Active.

This register contains the activity status of all system peripherals and signals. A 1 indicate activity. Software has to clear this register after a read by writing 0H.

BIT	NAME	R/W	Function
0	LPT_	R/W	LPT1, LPT2, LPT3, (378-37F, 278-27F, 3B8-3BF) was detected active
1	FD	R/W	Floppy Driver (I/O Port = 3F0-3F7)was detected active
2	HD	R/W	Hard disk (I/O Port = 1F0-1F7) was detected active.
3	COM	R/W	COM1,COM2,COM3,COM4. (I/O Port = 3F8-3FF, 2F8-2FF) was detected active
4	PIO0	R	Programmable I/O Devices Register 0 was detected active
5	PIO1	R	Programmable I/O Devices Register 1 was detected active
6	VD	R	Video memory Write -> B0000-BFFFF memory write was detected active
7	PMW	R	Programmable memory range write access was detected active

PCMCIA Socket 1 Status Register : (Index = A2H)

When socket A is configured as a memory card, this register contains the status information of WP, BVD1, BVD2, and READY.

BIT	NAME	R/W	Function
0	WP	R	PCMCIA Socket 1 Write Protect (high = write protect)
1	BVD2	R	PCMCIA Socket 1 battery low detect 2
2	BVD1	R	PCMCIA Socket 1 battery low detect 1
3	RESERVED	R	Reserved
4	READY	R	PCMCIA Socket 1 READY
5	CD	R	PCMCIA Socket 1 Card insertion detected
6	RESERVED	R	Reserved
7	LPH1	R	Status of LPH1

TM8100A Status Register-0 : (Index = A3H).

BIT	NAME	R/W	Function
0	PG0IN	R	Programmable General Purpose I/O Pin 0 (PGP0) Input Data
1	BL1IN	R	Battery low detect pin 1 (BL1) input data
2	BL2IN	R	Battery low detect pin 1 (BL2) input data
3	BL3IN	R	Battery low detect pin 2 (BL3) input data
4	LIND0	R	Last mode state indicator 0
5	LIND1	R	Last mode state indicator 1
6	LIND2	R	Last mode state indicator 2
7	SPEED	R	CPU speed indicator 1 indicates high speed

LIND2	LIND1	LIND0	Last mode state
0	0	0	FULL ON mode
1	0	0	ON mode
0	0	1	DOZE mode
0	1	0	SLEEP mode
0	1	1	SUSPEND mode

TM8100A Status Register-1 : (Index = A4H).

BIT	NAME	R/W	Function
0	PIND0	R	PRESENT state indicator 0
1	PIND1	R	PRESENT state indicator 1
2	PIND2	R	PRESENT state indicator 2
3	PG1IN	R	Pin PGP1 Input Data. or as socket 2 card change status
4	UPRTC	R	Indicate RTC timer in update cycle
5	DISRTC0	R/W	Internal RTC control 0 (Default = 0, disable)
6	DISRTC1	R/W	Internal RTC control 1 (Default = 0, disable).
7	ACIN	R	ACIN input status

PIND2	PIND1	PIND0	Present mode state
0	0	0	FULL ON mode
1	0	0	ON mode
0	0	1	DOZE mode
0	1	0	SLEEP mode
0	1	1	SUSPEND mode

Note:

If DISRTC0 is set to one then the AUTO Low Speed function described in register 9FH is also disabled.

NMI/SMI Status Register : (Index = A5H) Read Only

The register contains the information on which function generates the NMISMI signals. The initial value is 00H. If any NMI/SMI has been generated, the cooresponding bit will be set to 1, thus the system can keep track of the NMI/SMI status. Whenever the CPU reads this register, all the bits will reset to 0 after the read operation.

BIT	NAME	R/W	Function
0	RESUME	R	The NMI is generated by RESUME
1	ON	R	The NMI is generated when ON mode enters DOZE mode
2	DZ	R	The NMI is generated when DOZE mode enters SLEEP mode
3	SP	R	The NMI is generated when SLEEP mode enters SUSPEND mode
4	SU	R	The NMI is generated when SUSPEND mode enters OFF mode
5	BL1	R	The BL1 (Main Battery low first warning) generates NMI
6	BL2	R	The BL2 (Main Battery low second warning) generates NMI
7	BL3	R	The BL3 (Lithium Battery low warning) generates NMI

NMI/SMI Enable Mode Change Register : (Index = A5H) Write Only

This register is used to enable the mode change function. If the TM8100A is programmed to generate a NMI or SMI when the ON mode timer expires, the PMU will generate the NMISMI signals but not move to DOZE mode unless the cooresponding bit in this register is set to 1 to enable the mode change function. In this example, the PMU will not go into DOZE mode until a logic 1 is written into bit 1. If RESUME, BL1, BL2, BL3, or related bits are programmed, the TM8100A will generate NMI or SMI on both rising or falling edge changes. An NMI or SMI routine is required to write a 1 in the cooresponding bit to enable the next generation of NMI or SMI. Otherwise the NMI or SMI will not be generated anymore.

BIT	NAME	R/W	Function
0	RESUME	R	Enable the generation of NMI/SMI while SUSPEND input has a rising or falling edge change.
1	ON	R	Enable the NMI/SMI, activating mode change from ON mode to DOZE mode
2	DZ	R	Enable the NMI/SMI, activating mode change from DOZE mode to SLEEP mode
3	SP	R	Enable the NMI/SMI, activating mode change from SLEEP mode to SUSPEND mode
4	SU	R	Enable the NMI/SMI, activating mode change from SUSPEND mode to OFF mode
5	BL1	R	Enable the generation og NMI/SMI while BL1 has a rising or falling edge change
6	BL2	R	Enable the generation og NMI/SMI while BL2 has a rising or falling edge change
7	BL3	R	Enable the generation og NMI/SMI while BL3 has a rising or falling edge change

Socket Status Change Register : (Index = A6H)

Bit	NAME	R/W	Function
0	ICCDACHG	R	Socket A 'CD' bit had been changed from last read
1	ICCDBCHG	R	Socket B 'CD' bit had been changed from last read
2	ARDYCHG	R	Socket A 'READY' bit had been changed from last read
3	BRDYCHG	R	Socket B 'READY' bit had been changed from last read
4	AICBL1CHG	R	Socket A 'BVDA1' bit had been changed from last read
5	BICBL1CHG	R	Socket B 'BVDB1' bit had been changed from last read
6	AICBL2CHG	R	Socket A 'BVDA2' bit had been changed from last read
7	BICBL2CHG	R	Socket B 'BVDB2' bit had been changed from last read

bit 0 will be set to 1 if ICCARD socket A 'CDA' has been changed from 1 to 0 or 0 to 1
 bit 1 will be set to 1 if ICCARD socket B 'CDB' has been changed from 1 to 0 or 0 to 1
 bit 2 will be set to 1 if ICCARD socket A 'RDYA' has been changed from 0 to 1
 bit 3 will be set to 1 if ICCARD socket B 'RDYB' has been changed from 0 to 1
 bit 4 will be set to 1 if ICCARD socket A 'BVDA1' has been changed from 1 to 0
 bit 5 will be set to 1 if ICCARD socket B 'BVDB1' has been changed from 1 to 0
 bit 6 will be set to 1 if ICCARD socket A 'BVDA2' has been changed from 1 to 0
 bit 7 will be set to 1 if ICCARD socket B 'BVDB2' has been changed from 1 to 0

Miscellaneous Control Register : (Index = A7H)

Default = 00H. User should be aware if Bit 0 is set to 1, 8254 clock can not be stopped in SUSPEND Mode, in order to keep DRAM refreshed.

BIT	NAME	R/W	Function
0	REFSEL	R/W	Select DRAM refresh source. Default = 0, use 32K clock input as refresh source, 1 will select 8254 as refresh source
1	SLREF	R/W	Enable slow refresh for DRAM refresh. Default = 0, enable, the TM8100A will perform refresh every 120µs in slow refresh mode
2	OFFREF	R/W	Disable Pin 165 "-REFRESH" toggling in SLEEP mode
3	SMDDIR	R/W	Default is 0, select MDDIR.
4	ENADIN1	R/W	If set, TM8100A will disable data propagation to Display controller in memory cycle
5	ENADIN2	R/W	If set, TM8100A will disable data propagation to UART,PMU controller in memory cycle
6	ENSYSCK	R/W	If set Pin 158 to function as PMC6. Default pin 158 is functioning as SYSCLK if bit 0 in register 49H is zero
7	ENOSC14M	R/W	0 ==> Select PGP2 Output 1 ==> select OSC14M Output

EMSA Socket Selection Register : (Index = A8H)

Default = 00H.

BIT	NAME	R/W	Function
0	EMSP0	R/W	EMSA page 0 is used for PCMCIA socket A or B (if bit set to 1)
1	EMSP1	R/W	EMSA page 1 is used for PCMCIA socket A or B (if bit set to 1)
2	EMSP2	R/W	EMSA page 2 is used for PCMCIA socket A or B (if bit set to 1)
3	EMSP3	R/W	EMSA page 3 is used for PCMCIA socket A or B (if bit set to 1)
4	EMSP4	R/W	EMSA page 4 is used for PCMCIA socket A or B (if bit set to 1)
5	EMSP5	R/W	EMSA page 5 is used for PCMCIA socket A or B (if bit set to 1)
6	EMSP6	R/W	EMSA page 6 is used for PCMCIA socket A or B (if bit set to 1)
7	EMSP7	R/W	EMSA page 7 is used for PCMCIA socket A or B (if bit set to 1)

EMSB Socket Selection Register : (Index = A9H)

BIT	NAME	R/W	Function
0	EMS1P0	R/W	EMSB page 0 is used for PCMCIA socket A or B (if bit set to 1)
1	EMS1P1	R/W	EMSB page 1 is used for PCMCIA socket A or B (if bit set to 1)
2	EMS1P2	R/W	EMSB page 2 is used for PCMCIA socket A or B (if bit set to 1)
3	EMS1P3	R/W	EMSB page 3 is used for PCMCIA socket A or B (if bit set to 1)
4	SMIA22	R/W	SMI EMS translate address A22 for SMI only
5	SMIA23	R/W	SMI EMS translate address A23 for SMI only
6	SMIEN	R/W	Enable SMI
7	ENSMI	R/W	When Set, the TM8100 will generate SMI instead of NMI

SMI EMS Page Register : (Index = AAH)

BIT	NAME	R/W	Function
0	SMIA14	R/W	SMI EMS translate address Bit A14
1	SMIA15	R/W	SMI EMS translate address Bit A15
2	SMIA16	R/W	SMI EMS translate address Bit A16
3	SMIA17	R/W	SMI EMS translate address Bit A17
4	SMIA18	R/W	SMI EMS translate address Bit A18
5	SMIA19	R/W	SMI EMS translate address Bit A19
6	SMIA20	R/W	SMI EMS translate address Bit A20
7	SMIA21	R/W	SMI EMS translate address Bit A21

Note : A special EMS with page address = 60000H is used for SMI function.

Programmable Power Control Register-3 : (Index = ABH)

This register controls the PMC3 and PMC4 output pins if they are available (CGA LCD disabled) in FULL ON mode and DOZE mode. The initial default = 00H.

BIT	NAME	R/W	Function
0	FO-3	R/W	Controls PMC3 in FULL ON and ON Mode.
1	DZ-3	R/W	Controls PMC3 in DOZE Mode.
2	SP-3	R/W	Controls PMC3 in SLEEP Mode.
3	SU-3	R/W	Controls PMC3 in SUSPEND Mode.
4	FO-4	R/W	Controls PMC4 in FULL ON and On Mode.
5	DZ-4	R/W	Controls PMC4 in DOZE and ON Mode.
6	SP-4	R/W	Controls PMC4 in SLEEP Mode.
7	SU-4	R/W	Controls PMC4 in SUSPEND Mode.

Programmable Power Control Register-4 : (Index = ACH)

This register controls the PMC5 and PMC6 output pins if they are available in FULL ON mode and DOZE mode. The initial Default = 00H.

BIT	NAME	R/W	Function
0	FO-5	R/W	Controls PMC5 in FULL ON and ON Mode
1	DZ-5	R/W	Controls PMC5 in DOZE and ON Mode
2	SP-5	R/W	Controls PMC5 in SLEEP Mode
3	SU-5	R/W	Controls PMC5 in SUSPEND Mode
4	FO-6	R/W	Controls PMC6 in FULL ON and ON Mode
5	DZ-6	R/W	Controls PMC6 in DOZE and ON Mode
6	SP-6	R/W	Controls PMC6 in SLEEP Mode
7	SU-6	R/W	Controls PMC6 in SUSPEND Mode

Miscellaneous Control Register-3 : (Index = ADH)

Default = 00H

BIT	NAME	R/W	Function
0	ONCLK0	R/W	ON mode clock select Bit 0
1	ONCLK1	R/W	ON mode clock select Bit 1
2	MAINOFF	R/W	When set, TM8100A will turn off MAIN Clock input in ON mode, otherwise the Main Clock will be turned off in DOZE Mode
3	XTKBEN	R/W	When set, XT type of keyboard interface will be enabled. Default = 0, disabled. When enabled, PCLK (pin 117) becomes KBCK and 8042CS (pin 115) becomes KBDATA
4	ENACIN	R/W	When set, ACIN will be treated as activity
5	KEY0ISEL	R/W	
6	IRQ0SMIEN	R/W	When Set, 8254 channel 0 will generate SMI instead of normal IRQ0
7	INT8SEL	R/W	When set, 8259's IRQ8 is wired to internal RTC instead of external pin

BIT 1 0	ON Mode clock speed selection
0 0	7.15 MHz
1 0	1.75 MHz
0 1	3.55 MHz
1 1	0.9 MHz

PCMCIA Interrupt Selection Register : (Index = AEH)

Default = 00H

BIT	NAME	R/W	Function
0	INTSEL	R/W	When set, card change in socket will generate IRQ11 instead of IRQ10
1	ENCCHGINT	R/W	Enable Card changes in socket will generate an interrupt

CPU Control Register : (Index = AFH)

Bit	NAME	R/W	Function
0	EXTIROACT	R/W	Extend IR0 run time in DOZE mode , this bit is effective only if IR=74 BIT3 =1
1	RESERVED	R/W	Reserved
2	RESERVED	R/W	Reserved
3	RESERVED	R/W	Reserved
4	RESERVED	R/W	Reserved
5	BLILOWSP	R/W	Set CPU clock speed to low speed if BL1 is LOW, default =0
6	CHG-FU-SET	R/W	Change FULL ON timer from (1/512 --1/2) to (1/16--16)
7	CHG-ON-	R/W	Change ON timer from (1/16 --16) to (1/4--64)

Registers For Rev B.

PCMCIA Socket A I/O Window 1 Address Start Low Byte Register : (Index = 00H)
Default = 00H, read/write.

PCMCIA Socket A I/O Window 1 Address End low byte Register : (Index = 01H)
Default = 00H, read/write.

PCMCIA Socket A I/O Window 1 Address High byte Register : (Index = 02H)
Default = 00H, read/write.

PCMCIA Socket A I/O Window 2 Address Start Low Byte Register : (Index = 03H)
Default = 00H, read/write.

PCMCIA Socket A I/O Window 2 Address End Low Byte Register : (Index = 04H)
Default = 00H, read/write.

PCMCIA Socket A I/O Window 2 Address High Byte Register : (Index = 05H)
Default = 00H, read/write.

PCMCIA Interrupt Redirection Control Register : (Index = 06H)
Default = 00H, read/write.

Bit	NAME	R/W	Function
0	ICAIOWIN1	R/W	Enable Socket A I/O window 1, default = 0 = disable
1	ICAIOWIN2	R/W	Enable Socket A I/O window 2, default = 0 = disable
2	ICAOEN	R/W	Enable Socket A as an I/O card
3	INVICAIRQ	R/W	If set, the Interrupt from I/O card will be inverted
4	ICAINTIRO	R/W	Socket A Interrupt control bit 0
5	ICAINTIR1	R/W	Socket A Interrupt control bit 1
6	ICAINTIR2	R/W	Socket A Interrupt control bit 2
7	ICAINTIR3	R/W	Socket A Interrupt control bit 3

Bit				IRQ level select
7	6	5	4	
0	0	0	0	IRQ not selected
0	0	0	1	Reserve
0	0	1	0	Reserve
0	0	1	1	IRQ 3 selected
0	1	0	0	IRQ 4 selected
0	1	0	1	IRQ 5 selected
0	1	1	0	IRQ 6 selected
0	1	1	1	IRQ 7 selected

Bit				IRQ level select
7	6	5	4	
1	0	0	0	Reserved
1	0	0	1	IRQ 9 selected
1	0	1	0	IRQ 10 selected
1	0	1	1	IRQ 11 selected
1	1	0	0	IRQ 12 selected
1	1	0	1	Reserved
1	1	1	0	IRQ 14 selected
1	1	1	1	IRQ 15 selected

ICCARD Socket A VPP Control Register : (Index = 07H)

Default = 00H, read/write. This register is defining an I/O port address for controlling the ICCARD Socket A VPP signal. Bits 7-0 define the I/O port addresses A9-A2. Data Bit 0 controls whether the VPP signal is applied or not. For example, if the ICCARD Socket A VPP Control Register is programmed to be FF, an I/O write operation to port 3FC (or 3FD, 3FE, 3FF) with value 01 will turn on the Socket A VPP supply signal. An I/O write operation to port 3FC (or 3FD, 3FE, 3FF) with value 00 will turn off the Socket A VPP supply signal.

BIT	7	6	5	4	3	2	1	0
Function	A9	A8	A7	A6	A5	A4	A3	A2

Programmable Resume Mask Register-3 : (Index = 08H)

Default = 0H. A High in each bit will disable the corresponding function.

Bit	NAME	R/W	Function
0	ICBLIA_MSK	R/W	If bit 6 (ICA_RI_EN) is 1 and Socket A is set as I/O, then Socket A 'BL1/STCH/RJ' can wake up system
1	ICBLIB_MSK	R/W	If bit 7 (ICB_RI_EN) is 1 and Socket B is set as I/O, then Socket B 'BL1/STCH/RJ' can wake up system
2	IRQ3_MSK	R/W	IRQ3 can wake up system, Default = don't mask
3	IRQ4_MSK	R/W	IRQ4 can wake up system, Default = don't mask
4	IRQ8_MSK	R/W	IRQ8 can wake up system, Default = don't mask
5	RI_MSK	R/W	TM8100 'RI' input can wake up system, default = 0
6	ICA_RI_EN	R/W	Setting Socket A 'BVD1/STSCH/RJ' input as 'ring in' Default = 0
7	ICB_RI_EN	R/W	Setting Socket B 'BVD1/STSCH/RJ' input as 'ring in' Default = 0

Resume Status Register : (Index = 09H)

Software has to clear this register by writing 0H.

Bit	NAME	R/W	Function
0	ICA_RI	R/W	System is waked up Ring-In From Socket A
1	ICB_RI	R/W	System is waked up Ring-In From Socket B
2	IRQ3	R/W	System is waked up by IRQ3
3	IRQ4	R/W	System is waked up by IRQ4
4	IRQ8	R/W	System is waked up by IRQ8
5	TM8100_RI	R/W	System is waked up by Ring-In from Internal UART
6-7	RESERVED	R/W	Reserved

PMU Control Register : (Index = 0AH)

Bit	NAME	R/W	Function
0	SOCKETA_16M	R/W	Socket A can accept 16 bit memory access
1	SOCKETB_16M	R/W	Socket B can accept 16 bit memory access
2	SOCKETA_16I	R/W	Socket A can accept 16 bit I/O access
3	SOCKETB_16I	R/W	Socket B can accept 16 bit I/O access
4-7	RESERVED	R/W	Reserved

PCMCIA Socket B Register : (Index = 0CH)

Bit	NAME	R/W	Function
0	WPB	R	Socket B write protect if bit 5 is 1
1	BVDB2	R	Socket B Battery Low Detect 2 if bit 6 is 1
2	BVDB1	R	Socket B Battery Low Detect 1 if bit 6 is 1
3	RDYB	R	Socket B RDY if bit 7 is high
4	CDB	R	Socket B Card Detect
5	VLDWPB	R	WPB valid
6	VLDVLB	R	BVDB1, BVDB2 valid
7	VLDRDYB	R	RDYB valid

PCMCIA Interrupt Enable Register : (Index = 0DH)

Default = 00H (disables IRQ generation).

Bit	NAME	R/W	Function
0	ENACDCHG	RW	Socket A 'CD' pin change will generate a IRQ
1	ENBCDCHG	RW	Socket B 'CD' pin change will generate a IRQ
2	ENARDY	RW	Socket A 'RDY' from low to high will generate a IRQ
3	ENBRDY	RW	Socket B 'RDY' from low to high will generate a IRQ
4	ENAICBL1L	RW	Socket A 'BVDA1/STSCHG' from high to low will generate a IRQ
5	ENBICBL1L	RW	Socket B 'BVDB1' from high to low will generate a IRQ
6	ENAICBL2L	RW	Socket A 'BVDA2' from high to low will generate a IRQ
7	ENBICBL2L	RW	Socket B 'BVDA2' from high to low will generate a IRQ

Programmable Socket Status Interrupt Selection Register : (Index = 0EH)

If any interrupt source is enabled by Register 0DH, An interrupt (selected by this register) will be generated.

Bit	NAME	R/W	Function
0	ICCHGIR0	RW	Socket (A + B) status change generated a IRQ control bit 0
1	ICCHGIR1	RW	Socket (A + B) status change generated a IRQ control bit 1
2	ICCHGIR2	RW	Socket (A + B) status change generated a IRQ control bit 2
3	ICCHGIR3	RW	Socket (A + B) status change generated a IRQ control bit 3
4	STSAIRQSEL	RW	Socket (A + B) status change generated a IRQ or SMI , default =0
5-7	RESERVED	RW	Reserved

Bit				IRQ level select
3	2	1	0	
0	0	0	0	IRQ not selected
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	IRQ 3 selected
0	1	0	0	IRQ 4 selected
0	1	0	1	IRQ 5 selected
0	1	1	0	Reserved
0	1	1	1	IRQ 7 selected

Bit				IRQ level select
3	2	1	0	
1	0	0	0	Reserved
1	0	0	1	IRQ 9 selected
1	0	1	0	IRQ 10 selected
1	0	1	1	IRQ 11 selected
1	1	0	0	IRQ 12 selected
1	1	0	1	Reserved
1	1	1	0	IRQ 14 selected
1	1	1	1	IRQ 15 selected

TM8100 Version 2 Compatible Register : (Index = 0FH)

Reserved, initialized to FFH.

PCMCIA Socket B I/O Window 1 Address Start Low Byte Register : (Index = 10H)

Default = 00H, read/write.

PCMCIA Socket B I/O Window 1 Address End Low Byte Register : (Index = 11H)

Default = 00H, read/write.

PCMCIA Socket B I/O Window 1 Address High Byte Register : (Index = 12H)

Default = 00H, read/write.

PCMCIA Socket B I/O Window 2 Address Start Low Byte Register : (Index = 13H)

Default = 00H, read/write.

PCMCIA Socket B I/O Window 2 Address End Low Byte Register : (Index = 14H)

Default = 00H, read/write.

PCMCIA Socket B I/O Window 2 Address High Byte Register : (Index = 15H)

Default = 00H, read/write.

PCMCIA Interrupt Redirection Control Register : (Index = 16H)
 Default = 00H, read/write.

Bit	NAME	R/W	Function
0	ICBIOWIN1	R/W	Enable Socket B I/O window 1, default = 0 = disable
1	ICBIOWIN2	R/W	Enable Socket B I/O window 2, default = 0 = disable
2	ICBIOEN	R/W	Enable Socket B as a I/O card
3	INVICAIIRQ	R/W	If set, the Interrupt from I/O card will be inverted
4	ICBINTIRO	R/W	Socket B Interrupt control bit 0
5	ICBINTIR1	R/W	Socket B Interrupt control bit 1
6	ICBINTIR2	R/W	Socket B Interrupt control bit 2
7	ICBINTIR3	R/W	Socket B Interrupt control bit 3

Bit				IRQ level select
7	6	5	4	

0	0	0	0	IRQ not selected
0	0	0	1	Reserve
0	0	1	0	Reserve
0	0	1	1	IRQ 3 selected
0	1	0	0	IRQ 4 selected
0	1	0	1	IRQ 5 selected
0	1	1	0	IRQ 6 selected
0	1	1	1	IRQ 7 selected

Bit				IRQ level select
7	6	5	4	

1	0	0	0	Reserved
1	0	0	1	IRQ 9 selected
1	0	1	0	IRQ 10 selected
1	0	1	1	IRQ 11 selected
1	1	0	0	IRQ 12 selected
1	1	0	1	Reserved
1	1	1	0	IRQ 14 selected
1	1	1	1	IRQ 15 selected

ICCARD Socket B VPP Control Register : (Index = 17H)

Default = 00H, read/write. Default = 00H, read/write. This register is defining an I/O port address for controlling the ICCARD Socket B VPP signal. Bits 7–0 define the I/O port addresses A9–A2. Data Bit 0 controls whether the VPP signal is applied or not. For example, if the ICCARD Socket B VPP Control Register is programmed to be FF, an I/O write operation to port 3FC (or 3FD, 3FE, 3FF) with value 01 will turn on the Socket B VPP supply signal. An I/O write operation to port 3FC (or 3FD, 3FE, 3FF) with value 00 will turn off the Socket B VPP supply signal.

BIT	7	6	5	4	3	2	1	0
Function	A9	A8	A7	A6	A5	A4	A3	A2

10.0 LCD CONTROLLER REGISTER DESCRIPTION

10.1 Access to Display Registers

The registers in the CGA LCD controller are accessed through indirect addressing, an Index Register with an I/O address 3D4 or 3B4 should be written first with the index value of the particular register, then data can be written or read out from the Data Register through I/O address 3D5 or 3B5. Registers in the display controller are protected to unauthorized accessed. To enable programming, software must first write 3B4 for HGA or 3D4 for CGA with data equal 12 and immediately after the write cycle perform a I/O read cycle from address 3B5 for HGA and 3D5 for CGA. To disable programming, software must first write 3B4 for HGA or 3D4 for CGA with data equal 13 and immediately after the write cycle perform a I/O read cycle from address 3B5 for HGA and 3D5 for CGA.

Index Register : (Index = 3B4H)

This register is used to point to the actual register by CPU for HGA. Write only.

Data Register : (Index = 3B5H)

This register is used to read from or write data into the actual register pointed by Index Register for HGA controller. Read/write.

Index Register : (Index = 3D4H)

This register is used to point to the actual register by CPU for CGA. Write only.

Data Register : (Index = 3D5H)

This register is used to read from or write data into the actual register pointed by Index Register for CGA controller. Read/write.

10.2 Memory Map

A Single 32KB SRAM is used to implement complete CGA display sub-system, the memory mapping of this SRAM is as follows:

B8000	BBFFF	16K	CGA
BC000	BCFFF	4K	Free (Reserved by system BIOS)
BD000	BDFFF	4K	Special character
BE000	BEFFF	4K	HGA character code
BF000	BF7FF	2K	CGA character code (2K-5x7)
BF800	BFFF	2K	CGA character code (2K-7x7)

CGA mode (text or graphic)

B8000	BBFFF	16K	CGA
BC000	BCFFF	4K	Free
BD000	BDFFF	4K	Free
BE000	BEFFF	4K	Free
BF000	BF7FF	2K	CGA character code (2K-5x7)
BF800	BFFF	2K	CGA character code (2K-7x7)

CGA Special Character (text or graphic)

B8000	BBFFF	16K	CGA
BC000	BCFFF	4K	Free
BD000	BDFFF	4K	Special character code
BE000	BEFFF	4K	Free
BF000	BFFF	4K	Free

HGA Mode (text or graphic)

B8000	BBFFF	16K	CGA
BC000	BCFFF	4K	Free
BD000	BDFFF	4K	Free
BE000	BEFFF	4K	HGA character code
BF000	BFFF	4K	Free

CGA TEXT MODE :

4K Display Area	B8000 ~ B8FFF
4K	B9000 ~ B9FFF
4K	BA000 ~ BAFFF
4K	BB000 ~ BBFFF
4K	BC000 ~ BCFFF
4K	BD000 ~ BDFFF
4K	BE000 ~ BEFFF
5x7 CGA code	BF000 ~ BF7FF
2K	
7x7 CGA code	BF800 ~ BFFFF

SRAM	CODE
SRAM A0	RA0
SRAM A1	RA1
SRAM A2	RA2
SRAM A3	CA0
SRAM A4	CA1
SRAM A5	CA2
SRAM A6	CA3
SRAM A7	CA4
SRAM A8	CA5
SRAM A9	CA6
SRAM A10	CA7
SRAM A11	RA3
SRAM A12	1
SRAM A13	1
SRAM A14	1

HGA TEXT MODE :

4K Display Area	B8000 ~ B8FFF
4K	B9000 ~ B9FFF
4K	BA000 ~ BAFFF
4K	BB000 ~ BBFFF
4K	BC000 ~ BCFFF
4K	BD000 ~ BDFFF
4K	BE000 ~ BEFFF
4K HGA code	BF000 ~ BF7FF
4K	BF800 ~ BFFFF

SRAM	CODE
SRAM A0	RA0
SRAM A1	RA1
SRAM A2	RA2
SRAM A3	CA0
SRAM A4	CA1
SRAM A5	CA2
SRAM A6	CA3
SRAM A7	CA4
SRAM A8	CA5
SRAM A9	CA6
SRAM A10	CA7
SRAM A11	RA3
SRAM A12	0
SRAM A13	1
SRAM A14	1

CGA TEXT MODE (Special Character)

4K Display Area	B8000 ~ B8FFF	SRAM	CODE
4K	B9000 ~ B9FFF	SRAM A0	RA0
4K	BA000 ~ BAFFF	SRAM A1	RA1
4K	BB000 ~ BBFFF	SRAM A2	RA2
4K	BC000 ~ BCFFF	SRAM A3	CA0
4K CGA Special Code	BD000 ~ BDFFF	SRAM A4	CA1
4K	BE000 ~ BEFFF	SRAM A5	CA2
4K	BF000 ~ BFFFF	SRAM A6	CA3
		SRAM A7	CA4
		SRAM A8	CA5
		SRAM A9	CA6
		SRAM A10	CA7
		SRAM A11	RA3
		SRAM A12	1
		SRAM A13	0
		SRAM A14	1

MEMORY ADDRESS REFERENCE

DRAM	SRAM	CODE
BMA0	SRAM A0	RA0
BMA1	SRAM A1	RA1
BMA2	SRAM A2	RA2
BMA3	SRAM A3	CA0
BMA4	SRAM A4	CA1
BMA5	SRAM A5	CA2
BMA6	SRAM A6	CA3
BMA7	SRAM A7	CA4
NRAS	SRAM A8	CA5
NCAS	SRAM A9	CA6
ERMZ	SRAM A10	CA7
CGA	SRAM A11	RA3
RA0	SRAM A12	CGA
RA1	SRAM A13	NSPCH
RA2	SRAM A14	1
WZ	N SRAM WE	
EASC	N SRAM OE	
RA3	N SRAM CE	

Clock Reference

Mode	Normal	Power Save Mode*
640x200 LCD	9.54M	7.15 M
320x200 LCD	4.77M	3.58 M
640x400 LCD	14.318M	9.54 M
CGA CRT	14.318MHz	-

Note: Enabled by bit 6, Screen Control Register-2 (Index = 19H).

Signals State in Sleep and Suspend Mode

Signals	State
CP1(HSYN), CP2, S, M, I, R, G, B, BMA0-- BMA14, RDO0-3, BMD0-7	Low
LVDD, LVEE, NVSC	

Enable Software Switch Register : (Index = 12H)
The default value is 00H, write only.

Disable Software Switch Register : (Index = 13H)
The default value is 00H, write only.

Color Mapping Register : (Index = 14H to 17H, and Index = 1CH to 1FH)

10.3 Color Mapping

Sixteen gray levels in CGA Text mode are supported by the LCD controller. However, the effect of gray scale is depended on the quality of the LCD, Backlite, and application software. To get better gray levels, the TM8100A provide a "Color Mapping" function to let software adjust the mapping of color to the gray level displayed by the LCD controller. The mapping table is described below.

COLOR MAPPING TABLE :

I	R	G	B	INDEX = 3D4H	NIBBLE
0	0	0	0	14 H	Low
0	0	0	1	14 H	High
0	0	1	0	15 H	Low
0	0	1	1	15 H	High
0	1	0	0	16 H	Low
0	1	0	1	16 H	High
0	1	1	0	17 H	Low
0	1	1	1	17 H	High
1	0	0	0	1C H	Low
1	0	0	1	1C H	High
1	0	1	0	1D H	Low
1	0	1	1	1D H	High
1	1	0	0	1E H	Low
1	1	0	1	1E H	High
1	1	1	0	1F H	Low

Example:

Write 3D4 12h
Read 3D5
Write 3D4 14h
Write 3D5 EFH

IRGB

Gray level 0000 will be changed to gray level 1111
Gray level 0001 will be changed to gray level 1110

Screen Control Restore : (Index = 18H)

Write Only, default = 00H.

Bit 7 & Bit 6 : LCD Panel select

Bit 7	Bit 6	LCD Panel
0	0	640 x 200, Dual screen.
0	1	640 x 200, Single screen & smaller.
1	0	640 x 400, Dual screen.
1	1	640 x 400, Single screen.

Bit 5 : Memory Type Select.

- 0 => SRAM type (default).
- 1 => DRAM type.

Bit 4 : Display Type Select.

- 0 => CRT type (default).
- 1 => LCD type.

Bit 3 : Setup RA3.

0 => Set RA3 = 0 (7x7) (default).

1 => Set RA3 = 1 (5x7).

Bit 2 : Setup color emulation.

0 => Normal display (default).

1 => Color emulation (CGA CRT mode only).

Bit 1 : Setup auto screen blanking.

0 => Normal display (default).

1 => Auto screen blanking.

Bit 0 : Display mode.

0 => CGA mode (default).

1 => HGA mode.

Screen Control Register 2 : (Index = 19H)

Bit 7 : Clock Source.

0 => 14.318 MHz clock mode (default).

1 => 16 MHz clock source.

Bit 6 : Power Saving mode.

0 => None (default).

1 => Power saving mode (In DOZE mode and TEXT mode).
(T320 : 4.77MHz - (7.15) / 2MHz) (9.54MHz - 7.15MHz)

Bit 5 : Display Disable.

0 => Enable (default).

1 => Chip Disable.

Bit 4 : Color Map Enable.

0 => Normal Display (default).

1 => Color Map Enable.

Bit 3 & Bit 2 : LCD Panel select

Bit 3	Bit 2	LCD Panel
0	0	Set 4 Minute in ASB mode.
0	1	Set 2 Minute in ASB mode.
1	0	Set 1 Minute in ASB mode.
1	1	None (default).

Bit 1 : Gray Scaling Adjustment.

0 => Disable gray scaling modification.

1 => Enable gray scaling adjustment (default).

Bit 0 : Power Down Mode.

0 => Disable (default).

1 => Enable power mode.

Screen Adjust Register (Low Byte) : (Index = 1AH).

This register is used to implement the horizontal scrolling function, software can use this register to quickly scroll horizontally. Write Only. Default = 00H.

Screen Adjust Register (High Byte) : (Index = 1BH)

This register is used to implement the horizontal scrolling function, software can use this register to quickly scroll horizontally. Write Only. Default = 00H. For Example, if the software wants to scroll the screen to 0201H then:

Write 3d4 1Ah

Write 3d5 01h

Write 3d4 1Bh

Write 3d5 02h

(screen will be moved to 0201).

Control Register-1 : (Index = 20H)

Write only, default = 00H.

Bit 4 : Truncation.

0 => No truncation (Disable) (default).

1 => Truncation (Enable) . (LCD mode only) , When enabled, the LCD controller will not display any characters on the right of truncation point specified by Truncation Start Register (Index = 21H)

Bit 3 : Protect BC000 - BFFFF memory read and write.

0 => BC000 - BFFFF (16K) Memory can be read or written by system (default).

1 => Protect BC000 - BFFFF (16K) Character code (CGA mode only).
(Memory cannot be read or written by system).

Bit 2 : RA3 setup.

0 => Disable (RA3 -will be constant)(default).

1 => Enable (RA3) (CGA Text Mode only).

Bit 1 & Bit 0 : Printer I/O Port select:

Bit 1	Bit 0	Printer I/O port.
---	---	-----
0	0	DISABLE.
0	1	3BX (default).
1	0	37X.
1	1	27X.

Truncation Start Register : (Index = 21H)

This register specifies the first number of character that is truncated. Write Only, Default = 00H.

Truncation Stop Register : (Index = CUT22)

This register specifies the last number of character that is truncated. Write Only Default = 00H. If the display system only displays 42 character per row, then software can program the LCD controller as below to conserve power consumption.

For Example : (LCD mode)

Write 3d4 20h

Write 3d5 10h

Write 3d4 22h

Write 3d5 42h (character before number 66 is truncated).

11.0 6845 REGISTERS

REGISTER NAME	Address	CGA			
		Text mode		Graphics mode	
		40 x 25	80 x 25	320 x 200	640 x 200
Mode Control	3x8 hex	28 hex	0A hex	0A hex	1A hex
Color Select	3D9 hex	00 hex	00 hex	00 hex	07 hex
Configuration	3BF hex	---	---	---	---
Horizontal Total	0	38 hex	71 hex	38 hex	38 hex
Horizontal Display	1	28 hex	50 hex	28 hex	28 hex
H SYNC Position	2	2D hex	5A hex	2D hex	2D hex
H SYNC With	3	0A hex	0A hex	0A hex	0A hex
Vertical Total	4	1F hex	1F hex	7F hex	7F hex
Vertical Total Adjust	5	06 hex	06 hex	06 hex	06 hex
Vertical Display	6	19 hex	19 hex	64 hex	64 hex
V SYNC Position	7	1C hex	1C hex	70 hex	70 hex
Interlace Mode	8	02 hex	02 hex	02 hex	02 hex
Max. Scan Line	9	07 hex	07 hex	01 hex	01 hex
Cursor Begin	A	06 hex	06 hex	00 hex	00 hex
Cursor End	B	07 hex	07 hex	00 hex	00 hex
Start Address High	C	00 hex	00 hex	00 hex	00 hex
Start Address Low	D	00 hex	00 hex	00 hex	00 hex
Cursor Address High	E	00 hex	00 hex	00 hex	00 hex
Cursor Address Low	F	00 hex	00 hex	00 hex	00 hex
COLOR EMULATION					
REGISTER NAME	Index	Text mode		Graphics mode	
		40 x 25	80 x 25	320 x 200	640 x 200
		28 hex	0A hex	0A hex	1A hex
Mode Control	3x8 hex	00 hex	00 hex	00 hex	07 hex
Color Select	3D9 hex	---	---	---	---
Configuration	3BF hex	---	---	---	---
Horizontal Total	0	38 hex	71 hex	38 hex	38 hex
Horizontal Display	1	28 hex	50 hex	28 hex	28 hex
H SYNC Position	2	2D hex	5A hex	2D hex	2D hex
H SYNC With	3	0A hex	0A hex	0A hex	0A hex
Vertical Total	4	1F hex	1F hex	7F hex	7F hex
Vertical Total Adjust	5	06 hex	06 hex	06 hex	06 hex
Vertical Display	6	19 hex	19 hex	64 hex	64 hex
V SYNC Position	7	1C hex	1C hex	70 hex	70 hex
Interlace Mode	8	02 hex	02 hex	02 hex	02 hex
Max. Scan Line	9	07 hex	07 hex	01 hex	01 hex
Cursor Begin	A	06 hex	06 hex	00 hex	00 hex
Cursor End	B	07 hex	07 hex	00 hex	00 hex
Start Address High	C	00 hex	00 hex	00 hex	00 hex
Start Address Low	D	00 hex	00 hex	00 hex	00 hex
Cursor Address High	E	00 hex	00 hex	00 hex	00 hex
Cursor Address Low	F	00 hex	00 hex	00 hex	00 hex

REGISTER NAME	Index in Hex	HERCULES	
		Text mode 80 x 25	Graphics mode 720 x 348
Mode Control	3D8 or 3B8	28 hex	0A hex
Color Select	3D9	---	---
Configuration	3BF	00 hex	03 hex
Horizontal Total	0	61 hex	35 hex
Horizontal Display	1	50 hex	2D hex
H SYNC Position	2	52 hex	2E hex
H SYNC With	3	0F hex	07 hex
Vertical Total	4	19 hex	5B hex
Vertical Total Adjust	5	06 hex	02 hex
Vertical Display	6	19 hex	57 hex
V SYNC Position	7	19 hex	57 hex
Interlace Mode	8	02 hex	02 hex
Max. Scan Line	9	0D hex	03 hex
Cursor Begin	A	0B hex	00 hex
Cursor End	B	0C hex	00 hex
Start Address High	C	00 hex	00 hex
Start Address Low	D	00 hex	00 hex
Cursor Address High	E	00 hex	00 hex
Cursor Address Low	F	00 hex	00 hex

Printer Register

The Printer port can be configured as LPT1, LPT2, LPT3 or disabled. The setting is determined by bit 1 and bit of Display Control Register (Index = 20H) in display section.

Printer Data Register : (I/O address = 3BCH, or 378H, or 278H)
Default = 00H, read/write.

Printer Status Register : (I/O address = 3BDH, or 379H, or 279H)
Read only.

Printer Control Register : (I/O address = 3BEH, or 37AH, or 27AH)
Default = 00H, read/write.

Configuration Register : (I/O address = 3BFH, HGA Only)
Default = 00H, write only.

RS232 Registers

If the UART is selected as COM 1 the I/O address is from 3F8 to 3FF, for COM2, the I/O addresses are form 2F8 to 2FF. The selection of COM1 and COM2 is by bit 5 of register (Index = 77H).

Transmitter Holding Register : (I/O address = 3F8H), (DLAB=0)
This register contains the data waiting to be transferred. Bit 7 is MSB, bit 0 is the LSB. Write only.

Receiver Buffer Register : (I/O address = 3F8H), (DLAB=0)
This register contains the data received. Bit 7 is MSB, bit 0 is the LSB. Read only.

Divisor Latch (Low Byte) : (I/O address = 3F8H), (DLAB =1)
Programmable BAUD rate generator that is capable of dividing 1.843M (I/P OSC) from 1 to 216 -1 two 8-bit register store the divisor, this register contains the low byte. Read/write.

Divisor Latch (high Byte) : (I/O address = 3F9H), (DLAB =1)
Programmable BAUD rate generator that is capable of dividing 1.843M (I/P OSC) from 1 to 216 -1 two 8-bit register store the divisor, this register contains the high byte. Read/write.

Interrupt Enable Register : (I/O address = 3F9H), (DLAB=0)

BIT	NAME	R/W	Function
0	ERDI	W	Enable receiver DATA ready interrupt
1	ETDEI	W	Enable Transmitter holding register empty interrupt
2	ELSI	W	Enable receiver line status interrupt
3	EMSI	W	Enable Modem status interrupt
4-7	X	W	Reserved = 0

Interrupt Identification Register : (I/O address = 3FAH)

BIT	NAME	R/W	Function
0	IP	R	0 if interrupt pending
1	ID0	R	Interrupt ID Bit 0
2	ID1	R	Interrupt ID Bit 1
3-7	X	R	Reserved = 0

ID1	ID0	Priority	Interrupt type (Need Bit 0 = 0)
1	1	1	Receiver LINE status
1	0	2	Received DATA ready
0	1	3	Transmitter holding register empty
0	0	4	Modem status

Line Control Register : (I/O address = 3FBH)

BIT	NAME	R/W	Function
0	WLBO	R/W	Word length selection bit 0
1	WLBI	R/W	Word length selection bit 1
2	STP	R/W	Stop Bit. Default = 0, 1 stop bit , if set to 1 will enable 1.5 stop bit if word line = 5, 2 stop bit if word line = 6,7,8
3	PE	R/W	Parity Enable(set to one will enable parity)
4	EPS	R/W	Even parity(set to one will enable even parity)
5	SP	R/W	Stuck Parity(set to one will enable)
6	SB	R/W	Set - break Bit
7	DLAB	R/W	divisor latch access Bit

BIT 1	BIT 0	Word length (Bits)
0	0	5
0	1	6
1	0	7
1	1	8

Modem Control Register : (I/O address = 3FCH)

BIT	NAME	R/W	Function
0	DTR	R/W	Control /DTR O/P (if set will enable DTR)
1	RTS	R/W	Control /RTS O/P (if set will enable RTS)
2	OUT1	R/W	Reserved
3	OUT2	R/W	Reserved
4	LOOP	R/W	For local loop back diagnostic test
5-7	X	R/W	Reserved =0

Line Status Register : (I/O address = 3FDH)

BIT	NAME	R/W	Function
0	DR	R	Data ready
1	OE	R	Overrun error if set to 1
2	PE	R	Parity error if set to 1
3	FE	R	Framing error if set to 1
4	BI	R	Break interrupt if set to 1
5	THRE	R	Transmitter holding register empty if set to 1
6	TEMT	R	Transmitter empty if set to 1
7	RESERVED	R	Reserved

Modem Status Register : (I/O address = 3FEH)

BIT	NAME	R/W	Function
0	DCTS	R	Delta clear to send
1	DDSR	R	Delta data set ready
2	TERI	R	Trailing edge of ring indicator from Modem
3	DRLSD	R	Delta data carrier detect
4	CTS	R	Status of -CTS from Modem
5	DSR	R	Status of -DSR from Modem
6	RI	R	Status of -CTS from Modem
7	RLSD	R	Status of -DCD from Modem

Scratch Pad Register : (I/O address = 3FFH)

BIT	NAME	R/W	Function
0-7		R/W	

