TURTLE PROJECT

VALIANT Designs LTD
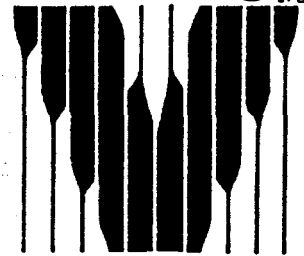
TITLE

TEST SPECIFICATION FOR MK IV COMMUNICATOR BOARD

DOCUMENT Nº VDL1/102

ISSUE Nº	PREPARED	CHECKED	APPROVED	COMMENTS
A	DAE	DC	DC	10/8/84

TEST SPECIFICATION FOR MK IV COMMUNICATOR BOARD

VALIANT DESIGNS SPECIFICATION NO.:   VDL1/102

ISSUE	A					
BUILD	30025					
DATE	10/8/84					
PREPARED	DAE					
CHANGE NOTE	−					

VALIANT DESIGNS LTD., Unit 13, Park House, 140 Battersea
Park Road, Battersea, LONDON SW11 4NB

I N D E X
****

1.0 INTRODUCTION

The purpose of this document is to define
test procedures for the MK IV Communicator.

Because of the nature of the unit, whereby 'slow' inputs
are translated into a fast data stream of infra-red
pulses, it is assumed that a reception unit is available
to receive the infra-red output and translate it into
a 'static' digital signal suitable for input into either
a computer or ATE system.

The document is split into three sections - A, B, and C:

Section A relates to   circuit testing where individual
components, or parts of circuits, may be tested.

Section B relates to functional testing, where the unit
is tested as a fully functional unit.

Section C defines the dynamic behaviour of those circuit
functions which are not adequately covered in the first
two sections.

2.0 FUNCTIONAL DESCRIPTION

The Communicator is a single board unit, designed to
receive either parallel or serial data from a host
computer and to translate that data into a pulse
position encoded infra red transmission.

With reference to the block diagram of Fig. 1, the
Central Computer block comprises a single chip
microcomputer programmed to carry out all major control,
decoding and encoding operations within the unit.

Via the DIL switch, the unit may be configured for
either serial or parallel reception modes.   When
operating in the serial mode, the computer functions as
an asynchronous serial receiver, baud rate selection
being a firmware time measurement function reliant on
the correct initialisation codes being transmitted to
the unit immediately following power up.   As a self
check procedure, the unit will only become functional
if the correct two byte initialisation codes are
received, and this applies to both parallel and serial
operation.

The Serial Interface block comprises line receiver
circuitry converting RS423/232 bipolar voltage signals
into TTL equivalent for input to the computer, and three
        bipolar voltage outputs providing the RS232
RTS function, RTS, and a handshake line IROP.
The bipolar I/O 0V reference is not at the same potential
as the main digital 0V within the unit, being nominally
at +6V.

The Parallel Interface block comprises an 8 bit latch
into which data is strobed from the host system and
which connects on output directly to the computer;
a pulse stretcher to ensure that short duration strobes
are detected by the processor; and two handshake lines
equivalent to the IEE 488 NRFD and NDAC functions.
By means of the DIL switch and external cabling
options, the logic status of the strobe, NDAC and
NRFD lines may be customised according to the host
system requirements.
All lines are TTL compatible.

The I.R. Pulser stage comprises a dual D Type Flip-Flop
which provides a single 2.5 microsecond pulse following
a clock input from the computer.
The output from this feeds directly to the I.R. Output
Stage.

The I.R. output stage comprises a CMOS to TTL buffer
stage, TTL to FET driver stage and I.R. output array
pulsed via the FET transistor.

The Led Indicator consists of a simple driver circuit
and   controlled directly from the computer to
indicate power application, initialisation and transmission
activities.

The power supply provides a nominal $\pm$ 12V supply and
+ 5V supply and is driven from a D.C. power adaptor
providing 24V D.C.

SECTION A: CIRCUIT TESTING

3.0   POWER SUPPLY AND CONSUMPTION TEST

Special Note: The power supply test should be implemented on a short duration power application basis in order to prevent possible component burn up. This specifically relates to R26, whereby any failure to re-set the I.R. output stage will cause excessive power dissipation in this component, due to this stage being permanently enabled.

3.1   Apply 24 Volts DC to unit between Sk2/2 (positive) and Sk2/1 with current limit set to 200 milliamp.

3.2   Confirm that the current consumption lies between 70mA and 200mA.

3.3   Confirm that the voltage across D8 is 12 ± 1 Volts.

3.4   Confirm that the voltage between PSR1 Pin 2 and PSR1 Pin 3 is $5V \pm 0.25V$ (PSR1 Pin 2 is positive).

3.5   Confirm that the voltage across R15 is $12V \pm 1V$.

4.0   SERIAL INTERFACE OUTPUT CIRCUIT TEST

4.1   Set DIL switch position 1 to off.

4.2   Apply 24V DC to board with 200mA current limit.

4.3   Short IC1 Pin 4 to 0V.

4.4   Apply TTL level 'O' to IC1/Pins 21,37,38 and confirm
        that the outputs at PL3/2, PL3/3 and PL3/5 w.r.t. 0V
        are all greater than +8 volts.

4.5   Apply TTL level '1' (or otherwise float) to IC1/
        Pins 21,37,38 and confirm that the outputs at PL3/2,
        PL3/3 and PL3/5 w.r.t. 0V are between 0V and -1V.

4.0   SERIAL INTERFACE OUTPUT CIRCUIT TEST

4.1   Set DIL switch position 1 to off.

4.2   Apply 24V DC to board with 200mA current limit.

4.3   Short IC1 Pin 4 to 0V.

4.4   Apply TTL level '0' to IC1/Pins 37, 38 and confirm
        that the outputs at PL3/3 and PL3/5 w.r.t. 0V are
        all greater than +8 volts.

4.5   Apply TTL level '1' (or otherwise float) to IC1/
        Pins 37, 38 and confirm that the outputs at PL3/3 and
        PL3/5 w.r.t. 0V are between 0V and -1V.

4.6   Apply TTL level '0' to IC1 Pin 21 and confirm that
        the output at PL3/2 w.r.t. 0V is more positive than
        +8 volts.

4.7   Apply TTL level '1' (or otherwise float) to IC1 Pin 21
        and confirm that the output at PL3/2 w.r.t. 0V is more
        negative than -8 volts.

5.0   SERIAL INTERFACE INPUT CIRCUIT TEST

5.1   Apply 24V DC to board with 200mA current limit.

5.2   Short IC1 Pin 4 to 0V.

5.3   Apply to P3/1 -0.4 volts w.r.t. PL3/4.
        (Note: This input is required to be floating as signal
                0V at PL3/4 is 6V above the main board 0V)
        Confirm that the signal at IC1 Pin 1 is TTL level '1'.

5.4   Apply to PL3/1 +0.4V w.r.t. PL3/4 and confirm that the
        signal at IC1 Pin 1 is TTL level '0'.

6.0   PARALLEL INTERFACE CIRCUIT TEST

6.1   Set DIL switch as follows:
            Position 3 to on
            Position 4 to on

6.2   Apply 24V DC to board with 200mA current limit.

6.3   Short IC1 Pin 4 to 0V.

6.4   Strobe Input Test

       6.4.1   Apply TTL logic '1' to PL1/15.

       6.4.2   Confirm that IC4 Pin 11 is at TTL logic '1'.

       6.4.3   Confirm that IC6 Pins 14 and 7 are within
               0.1 volts of the +5v supply.

       6.4.4   Confirm that the level at IC1 Pins 23 and 6 is
               at logic 1.

       6.4.5   Confirm that the level at IC3 Pin 11 is at
               logic '1'.

       6.4.6   Set PL1/15 to logic 0.
               Confirm that the following positions are all at
               logic 0:
                        IC6 Pins 14 and 7
                        IC1 Pins 23 and 6
                        IC3 Pin 11

6.5   Latch Test

       6.5.1   Apply the following codes to the input pins as
               detailed below and confirm that the same code is
               present on the output pins following application
               of the strobe pulse, as instructed in clause 6.5.2.
               All levels are TTL.

Data Line	Input	Output	Applied Code					
			1	2	3	4	5	6
DAT 1	PL1/1	IC1/27	0	1	0	1	1	0
DAT 2	PL1/2	IC1/28	0	1	1	0	1	0
DAT 3	PL1/3	IC1/29	0	1	0	1	0	1
DAT 4	PL1/4	IC1/30	0	1	1	0	0	1
DAT 5	PL1/5	IC1/31	0	1	0	1	1	0
DAT 6	PL1/6	IC1/32	0	1	1	0	1	0
DAT 7	PL1/7	IC1/33	0	1	0	1	0	1
DAT 8	PL1/8	IC1/34	0	1	1	0	0	1

6.5.2 With Strobe at PL1/15 at logic 1, set to logic 0,
then back to logic 1.
Data is clocked into latch on rising edge of
Strobe when SW1 Positions 3 and 4 are set to on.

6.6   Control Line Test

6.6.1 With reference to the tables below, apply the
TTL input combinations as listed and confirm
that the outputs conform accordingly.

a) NDAC Output

Inputs		Output
IC1/37	PL1/11	PL1/13
0	FLOAT	1
1	FLOAT	0
0	0	0
1	0	1

b) NRFD Output

Inputs		Output
IC1/38	PL1/12	PL1/14
0	FLOAT	1
1	FLOAT	0
0	0	0
1	0	1

7.0   LED INDICATOR TEST

7.1   Apply 24V DC to board with 200mA current limit.

7.2   Short IC1 Pin 4 to 0V.

7.3   Confirm that TR2 collector is within 0.3V of 0V.

7.4   Set IC1 Pin 36 to logic '0'.

7.5   Confirm that TR2 collector is at +12Vp potential.

8.0   I.R. DRIVER CONTROL STAGE TEST

Note: Although the microcomputer reset pin is held low through-
out In-circuit testing, causing port outputs to be held
in a high impedance '1' state, the Address Latch Enable
(ALE) line from IC1 Pin 11 continues output.
For this test, this line requires external over-riding
control, subjecting the IC output to possible back
driving stress.   In order to avoid stress on this
component, the duration of the test will have to be
limited to a 'safe' operating period.

8.1   Apply 24V DC to board with 200mA current limit.

8.2   Short IC1 Pin 4 to 0V.

8.3   Short TR1 Gate to -12V rail.

8.4   Confirm that the voltage at the node R13/R21 w.r.t. 0V
is between +1.42V and +1.70V.

8.5   Confirm that the output nodes are at the logic states
as defined in the table below against each control
input condition.

Comment	Control Inputs		Outputs		
	IC1/35	IC1/11	IC2/9	IC6/10	IC5/5
Initial Condition Free Run ALE	1	⎍⎍⎍	0	0	1
*	0	0	0	0	1
Control Clock	1	0	1	0	1
*	0	0	1	0	1
ALE Clock	0	1	0	1	0
*	0	0	0	1	0
ALE Clock	0	1	0	0	1
*	0	0	0	0	1
ALE Free Run	0	⎍⎍⎍	0	0	1

*   No output change

9.0   I.R. OUTPUT STAGE TEST

Note: Pulse application to the I.R. output stage must be
        limited to less than 20us to avoid over-stressing
        of stage.

9.1   Apply 24DC to board with 200mA current limit.

9.2   Short IC1 Pin 4 to 0V.

9.3   Confirm that the voltage at IC5 Pin 5 is logic 1.

9.4   Confirm that the voltage at IC5 Pin 6 is within 5V
        of the -12V rail.

9.5   Confirm that the differential voltage across R1 is
        less than 30mV.

9.6   Set IC5 Pin 5 to logic 0 (Refer to section note above).

9.7   Confirm that the voltage at IC5 Pin 6 is within 3V of
        +12Vp.

9.8   Confirm that the differential voltage across R1 is
        greater than 4 volts but less than 7 volts.

9.9   Set IC5 Pin 5 to logic 1.

SECTION B: FUNCTIONAL TESTS

This section defines the Functional Test requirements of the Unit. It assumes the availability of an I.R. Reception Unit capable of receiving, decoding and transmitting the resultant code word(s) back to the host system via an 8 bit parallel interface. It assumes that the Unit has passed at least the power supply test of section 3.0.

10.0 PARALLEL INTERFACE OPERATION

10.1 Equipment Set Up Procedure

a) Connect Communicator to parallel output port of Host System, via Parallel Cable defined in Appendix A.

b) Set SW1 as follows: Position 1 off
                         Position 2 off
                         Position 3 on
                         Position 4 on

c) Connect I.R. Reception Unit into input port of Host System via second Parallel Cable defined in Appendix A.

10.2 Apply power to Communicator and I.R. Reception Unit.

10.3 Confirm that the Indicator Led within the Communicator is illuminated.

10.4 Output the initialisation code words 0DH and 55H to the Communicator according to signal control sequence defined in section 13.0.

10.5 Ensure that the unit has initialised by confirming that the Indicator Led has extinguished.

10.6 For each double byte output sequence to the Communicator, read and confirm that the codes received by the I.R. Reception Unit are those defined according to the table below.
Refer to Appendix B for details on operation of the I.R. Reception Unit.

Outputs to Communicator		Received Code	
1st Byte	2nd Byte	1st Byte	2nd Byte
00H	00H	00H	00H
FFH	FFH	FFH	03H
55H	02H	55H	06H
AAH	01H	AAH	05H

11.0   SERIAL INTERFACE OPERATION

11.1   Equipment Set Up Procedure

a)   Connect Communicator into serial RS232 output
     port of Host System via serial cable defined in
     Appendix C.

b)   Set SW1 Position 1 to ON

              Position 2 to OFF

              Position 3 Don't Care

              Position 4 Don't Care

c)   Connect I.R. Reception Unit into input port
     of Host System via parallel cable, type according
     to Appendix A.

d)   Set Host System serial I/O baud rate to either 2.4k
     or 4.8k;   set to 8 data bits;   parity and
     stop bits are don't care.

11.2   Apply power to Communicator and I.R. Reception Unit.

11.3   Confirm that the Indicator Led within the Communicator
       is illuminated.

11.4   Ouput from the Host System the two initialisation
       characters 0DH and 55H according to the signalling
       requirements defined in section 14.0

11.5   Ensure that the Unit has initialised by confirming
       that the Indicator Led has extinguished.

11.6   For each single byte transfer to the Communicator,
       read and confirm that the codes received by the I.R.
       Reception Unit are those defined according to the table
       below.
       Refer to Appendix B for details on operation of the
       I.R. Reception Unit.

Serial Output to Communicator	Received Code	
	1st Byte	2nd Byte
00H	00H	03H
FFH	FFH	03H
55H	55H	03H
ABH	ABH	07H

SECTION C: DYNAMIC PERFORMANCE

This section details the dynamic operation of the unit under normal operating conditions.

12.0   SYSTEM CLOCK

All system (firmware) operations are timed against the ALE output clock from IC1 Pin 11.
This clock is itself derived from a 6MHz oscillator circuit formed by the on-chip IC1 circuitry and externally connected crystal.

The ALE output is required to be of 2.5 microsecond -0.05% period, with a high to low ratio of very approximately 1 to 4.

13.0 PARALLEL INTERFACE OPERATION

The Parallel Interface is essentially designed to function
as a 'cut-down' IEEE 488 listener only port, consisting
of DAT1 to DAT8, DAV, NDAC and NRFD. However, in the
majority of instances, utilisation of all these lines
is not necessary, such that in the minimal interface
case only DAT1 to DAT8 and DAV may be used.

The signal lines conform in terms of logic sense to
the IEEE specification on input/output to IC1 as
follows:

> Input: DAT1 to DAT8 = IC1 Pin 27 through to Pin 34 respectively
>
> Input: DAV   = IC1 Pins 6 and 23
>
> Output: NDAC   = IC1 Pin 37
>
> Output: NRFD   = IC1 Pin 38

Figure 2 shows the operational sequence of this interface.

To provide additional flexibility of this interface,
each control line passes through an exclusive or-gate -
providing the option to invert the logic sense of the
signal presented at the board plug PL1.

As may be seen from the figure an additional signal
denoted DAV(PL1/15) is shown with a minimum timing of
0.5 microseconds, as may be expected from a Centronics
type interface. In such circumstances, it is unlikely
that the microcomputer would detect this signal except
on rare occasions. Accordingly, the signal is pulse
stretched prior to input to IC1.
When operating this interface against a host system
that can be 'hand shaked', DAV (or Strobe) may be held
in its active state until the Communicator has signalled
back to the host system via NDAC that it has received
DAV true. At this point, the Host may clear the signal
and allow the Communicator to read the data from the
eight bit latch
It is also worth noting that the clocking edge for data
into the latch may also be selected according to requirement,
although it would normally be set to the trailing edge
of DAV.

A further facility offered by the interface is the
NRFD (or Not Ready For Data) line, and this may be used
by the Host System to ensure that data is only outputted
when this line indicates readiness of the Communicator
to receive. However, for a trailing edge DAV clock,
this facility need not be used.

The facilities offered by the interface allow operation
against very fast strobed ports, or, at the opposite
extreme, very slow hand shaked systems.

14.0   SERIAL INTERFACE OPERATON

14.1

This interface primarily conforms to the signal type
and form normally attributed to RS232.
Three signals are provided:

      Received Data (RxD)   (Input)

      Ready to Send (RTS)   (Output)

      Inverted Ready to Send ($\overline{\text{RTS}}$)   – not normally used (Outpu

All signals are referenced against the serial interface
Signal 0V, which is held some 6V above the main
digital 0 Volts within the Communicator.
Accordingly, CAUTION must be exercised when subjecting
the Communicator to testing to ensure that the two
0 Volt systems are not unbalanced by means of test
equipment earthing.   It is recommended that the serial
interface is transmitted via an isolation Receiver-
Transmitter in order that the main Test Equipment be
grounded.

In order to account for those host systems which
specify RS423 signal levels rather than RS232, the
two outputs are voltage limited to conform to the
former.   However, under normal circumstances, both
interfaces are compatible.   Figure 3 details voltage
levels for the interface.

14.2   Received Data

Serial Data is received via a buffer circuit designed
to convert RS232/423 voltage levels to TTL before input
to the microcomputer input PL1 Pin 1.
With reference to Figure 3, it may be seen that the input
line is quiescently logic 1.
The signal start is denoted by a logic 0 start bit,
followed by 7 or 8 data bits (The Communicator requires
DIL switch setting for data bit selection).
The status of the trailing parity bit and number of
stop bits is not firmware tested.

14.3   Request to Send (RTS)

This signal, output from IC1 Pin 37, is used to inform
the host computer that the Communicator is busy, and
is set to logic 1 shortly after a serial input has
been completed.
It is cleared, i.e. set to logic 0, when the infra-red
transmission is completed and ready to receive the next
serial input.

The $\overline{\text{RTS}}$ line output from IC1 Pin 38 is an exact
replica of the RTS signal, but inverted.

14.4   Baud Rate

There are no Communicator facilities for baud rate
selection.
The system has been designed as self adjusting, requiring
an initialisation character following power-up, but
timing limitations constrain flexibility to only two
standard rates: 2400kB and 4800kB.

15.0   INDICATOR LED OPERATION

This function has been provided to enable the user
to ascertain certain operational conditions of his
system and provide him with a level of confidence
that his system is functioning.
The Led provides three specific functions, depending
on the time of observation.

a)   **Power Up**

On power application to the Communicator, the led
will become illuminted.

b)   Following initialisation involving the transfer
of two specific codes from the Host System, the
led should normally go out, indicating that the
unit has initialised correctly.
Failure to go out would usually indicate incorrect
Host operation, cables not connected, or wrong
switch settings within the Communicator.

c)   Following initialisation, each command transmitted
to the Communicator will be encoded into an
infra-red output.
For each infra-red command output, the led will
change state, providing a toggling action.

16.0   I.R. OUTPUT OPERATION

Following reception of a command code from the host,
the microcomputer translates this command into a
string of infra-red output pulses which are time
position dependent on logic state.

The processor outputs a string of clock edges to the
dual D-Type Flip-Flop IC2.
These clock edges are converted into 2.5 microsecond
pulses by virtue of the cross-coupling of the
D-Types and the secondary ALE Clock input.

These pulses are then sent via a comparator circuit
IC6, which converts the CMOS output signal levels
from IC2 to TTL prior to input to the RS232 transmitter
interface IC5.   The function of this circuit is to
provide a full 24V supply swing on the power FET gate
terminal, in order to ensure full turn-off and turn-on.
The turn-on current through the I.R. diodes D1 to D4
is between 1.5 and 2 Amps, and may be monitored by
differential sensing across the 3.3 ohm resistor R1.

R26 is provided as a protection device to limit
the driver current in the event of above normal
pulsing periods of the I.R. output stage, as may be
experienced during unit power-up and power-down.
However, permanent turn-on situations will cause
R26 to burn out and would only occur as a result of
a unit fault.

Figure 4 shows typical waveform as would be found
at the various nodes in the circuit for a command
output from the host of 01101000.

17.0 IROP CONTROL FUNCTION

In order to allow individual and concurrent operation
of more than one Turtle robot within a confined area,
the infra-red transmissions require sequential control
in order to avoid timing conflicts.

The IROP output line has been provided to facilitate
this control and is used in conjunction with the RxD
input.   The facility is only relevant when the Communicator
is being operated in a parallel interface mode.

Normally, when sequencing control is not required,
the serial input RxD is biassed such that the input at
IC1 Pin 1 is held permanently in a logic 1 state,
thus permanently enabling transmissions.   Holding
this line in the other state will halt transmissions
until such time as the line is taken back to its
logic '1' condition.

The IROP line has been provided to indicate when the
Communicator is ready, and indeed demanding, to transmit,
such that via an external Sequencing Control Unit,
the necessary timing control may be exerted on the
RxD line in order to phase or interlace transmissions.
Accordingly, the IROP output at PL3/2 goes to logic 0
when a transmission demand is present and is cleared
only when the transmission is completed.   Refer to
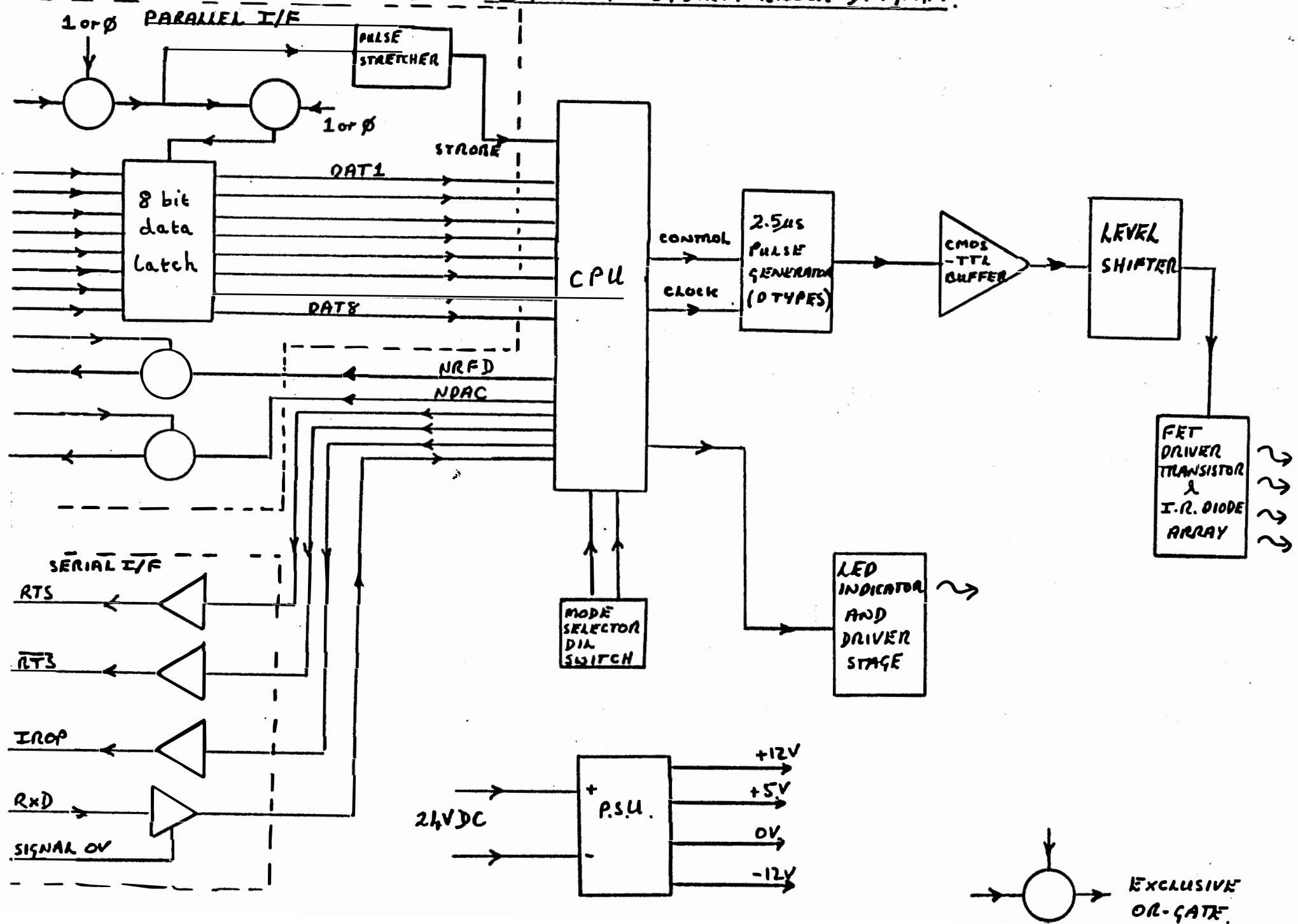Figure 5 for typical timing diagram.
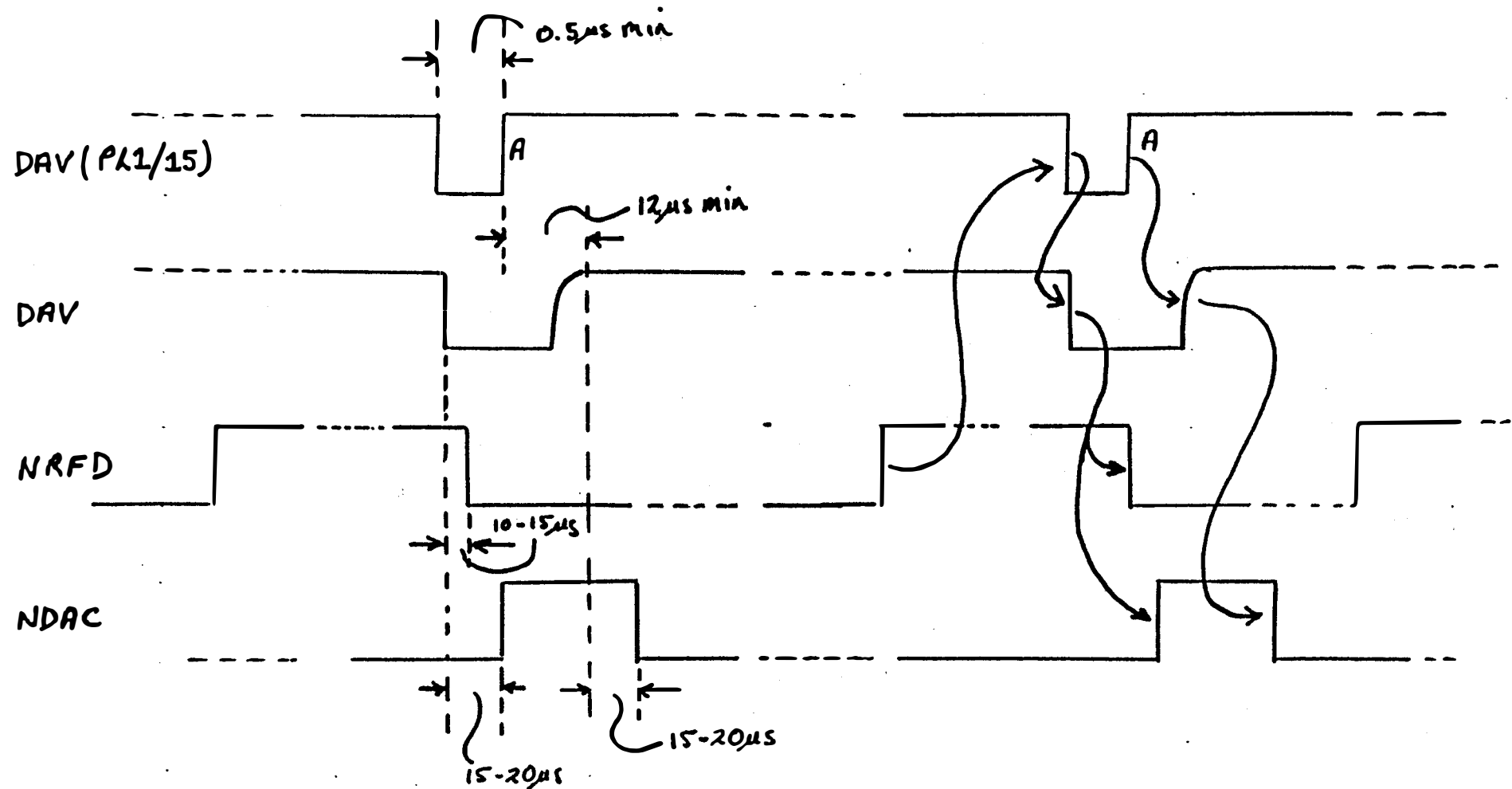
FIGURE 1. SYSTEM BLOCK DIAGRAM.

FIGURE 2 PARALLEL I/F SIGNALLING DIAGRAM.

DAV (Pl1/15)

0.5µs min

A

DAV

12µs min

NRFD

10-15µs

NDAC

15-20µs

15-20µs

A =   normal clocking edge for data storage into latch: data set up in advance of this edge.

RxD
(Pl3/1)

'0'
'1'

±25V max
±0.4V min

SIGNAL 0V (Pl3/4)

RxD
(=C1)
(Pin 1)

'1'
'0'

TS
(=C1)
(Pin 37)

'1'
'0'

A

RTS
(Pl3/3)

8V

SIGNAL 0V

DIGITAL 0V.

≈6V

0V

-1V min

≈ 1ms

12 bits

A: RTS set false during 12th bit period (regardless of whether or not 12 bits transmitted from Host)
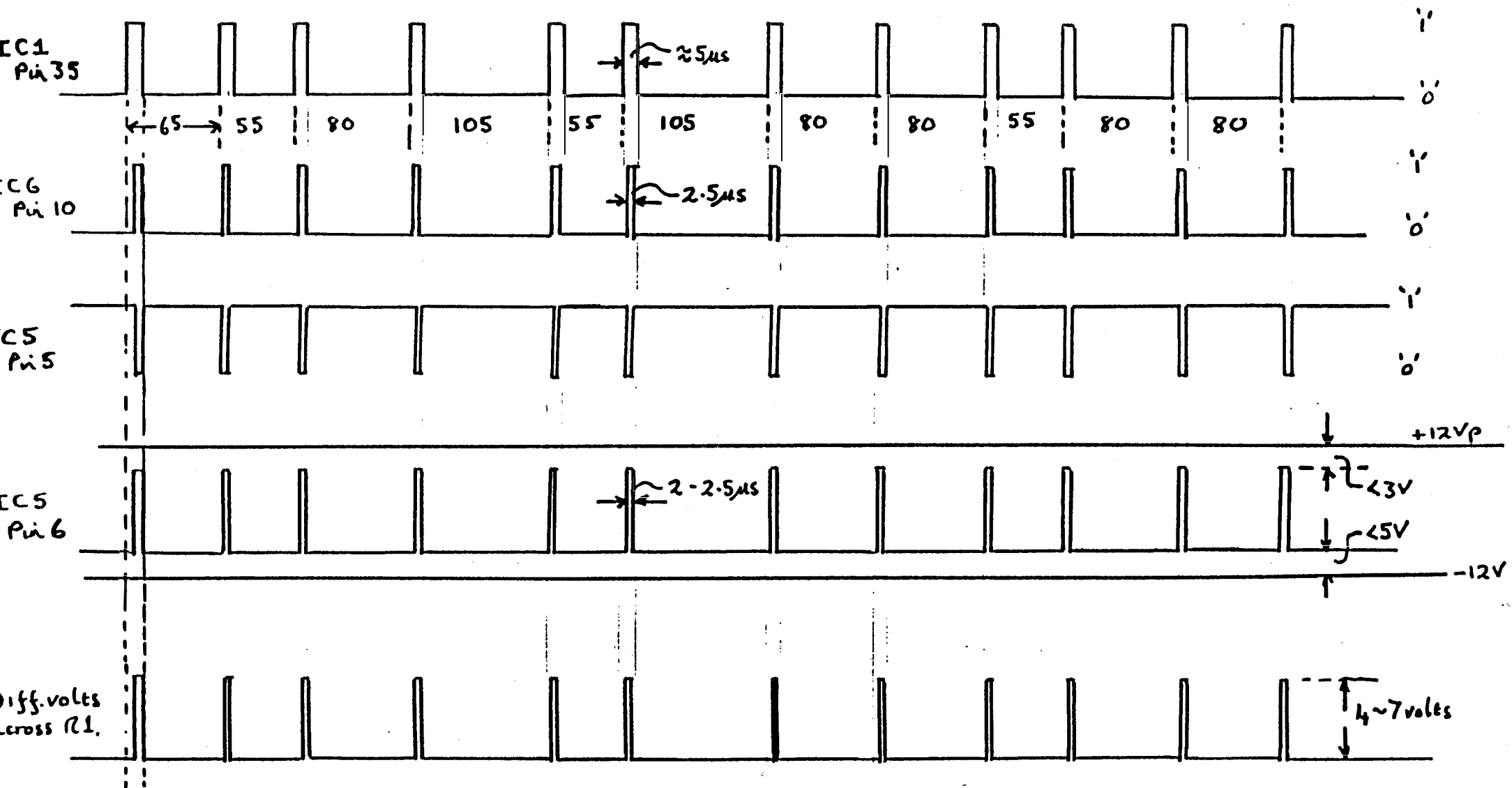
FIGURE 3 SERIAL I/F SIGNALLING DIAGRAM.

Figure 4 I.R o/p System Signalling Diagram.