

COMMODORE SEMICONDUCTOR GROUP

a division of Commodore Business Machines, Inc. 950 Americase Road, Norristawa, PA 19403 + 215/666-7950 + TWX 510-660-4168

HMOS

6510 MICROPROCESSOR WITH I/O

DESCRIPTION

The 6510 is a low-cost microprocessor capable of solving a broad range of small-systems and peripheral-control problems at minimum cost to the user.

An 8-bit B-Directional I/O Port is located on-chip with the Output Register at Address 0001 and the Data-Direction. Register at Address 0000. The I/O Port is bit-by-bit programmable.

The Three State's ixteen-bit Address Bus allows Direct Memory Accessing (DMA) and multi-processor systems sharing a common memory.

The internal processor architecture is identical to the Commodoro Semiconductor Group 6502 to provide software compatibility.

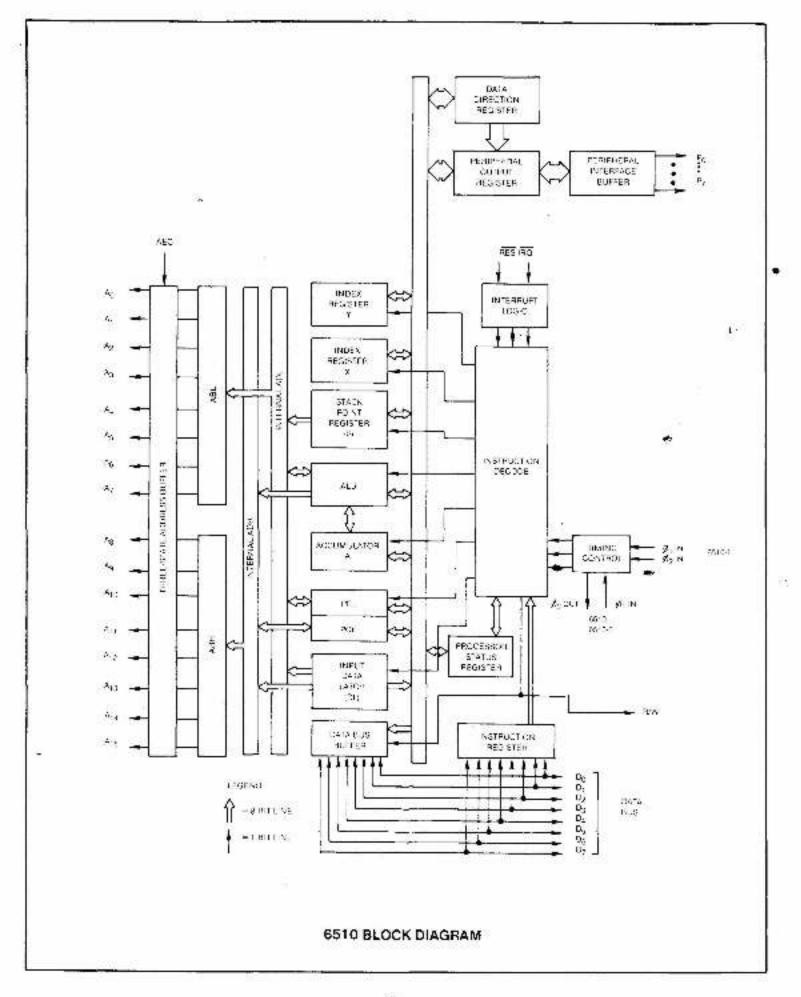
FEATURES OF THE 6510 . . .

- 8-Bit Bi-Directional I/O Port
- Single +5 voit supply
- HMOS, sflicen gate, depletion load technology.
- Eight bit parallel processing.
- 56 Instructions
- Decimal and binary anthmetic
- Thuseen addressing modes.
- True indexing papability
- Programmable stack pointer.
- Variable length stack

- Interrupt capability
- 8 Bit Bi-Directional Data Bus
- Addressable memory range of up to 65K bytes.
- · Direct memory access capability
- Bus compatible with M6800
- · Pipeline architecture
- 1 MHz 2MHz and 3 MHz operation
- Use with any type or speed memory.
- 4 MHz operation availability expected in 1986.

PIN CONFIGURATIONS

Z, N	1	40	RES	RES	30	43	₩21N	RES	38	46	Ø5 0.0
RL'Y	2	39	8g OUT	Ø.14	2	JH	HW	2214	. 2	50	B/W
190	3	38	D/W	IRO	3	39	D5 _c	160	-3	38	UP ₀
NM	4	37	cec	AEC	-1	37	D50	AHO	4	57	DB,
AEC	5	36	C5 ₁	Voc 1	5	38	DS,	Yee	5	36	DB,
VCC.	6	35	052	A ₀	6	25	UB ₂	A ₀	1 8	35	CH ₀
Au.	Ŧ	34	C d ₃	A	7	34	D5,	A	- 7	34	DB2
٥,,	0	33	03,	A ₂	e	33	98 ₅	Ag	В	33	Ce ₆
A-	28	35	685	49	.6	32	OB,	Ay	3	32	DB ₀
in a	10 6510	31	C B _d	A.	10 651		09;	Ac	0 551	0-2 3	CE,
4	71	00	C=2	An .	11	30	35	45	10	30	Po
	12	29 29	PC	A	12	25	B:	4	12	29	Pi
\\ A:	1.3	25	P_1	0.50%	13	88	F,	A_{γ}	.3	20	Pe
4:	14	27	F,	40	14	27	74	A-6	14	27	Pa
4,	15	25	Pa	49	15	26	4	1/19	5	26	P.
	13	25	74	A,5	16	26	F _k	A.16	16	25	P ₆
Ath	17	24	Pa	Ac	17	24	7. ·	241	1.7	24	Pr.
2	13	23	A.	A12	13	23	27	A12	16	23	P ₇
	13	22	A.v.	Ags	12	29	4.5	A12	19	33	Air
	20	21	YSS	738	201	21	A-2	V59	20	21	A14



6510 CHARACTERISTICS

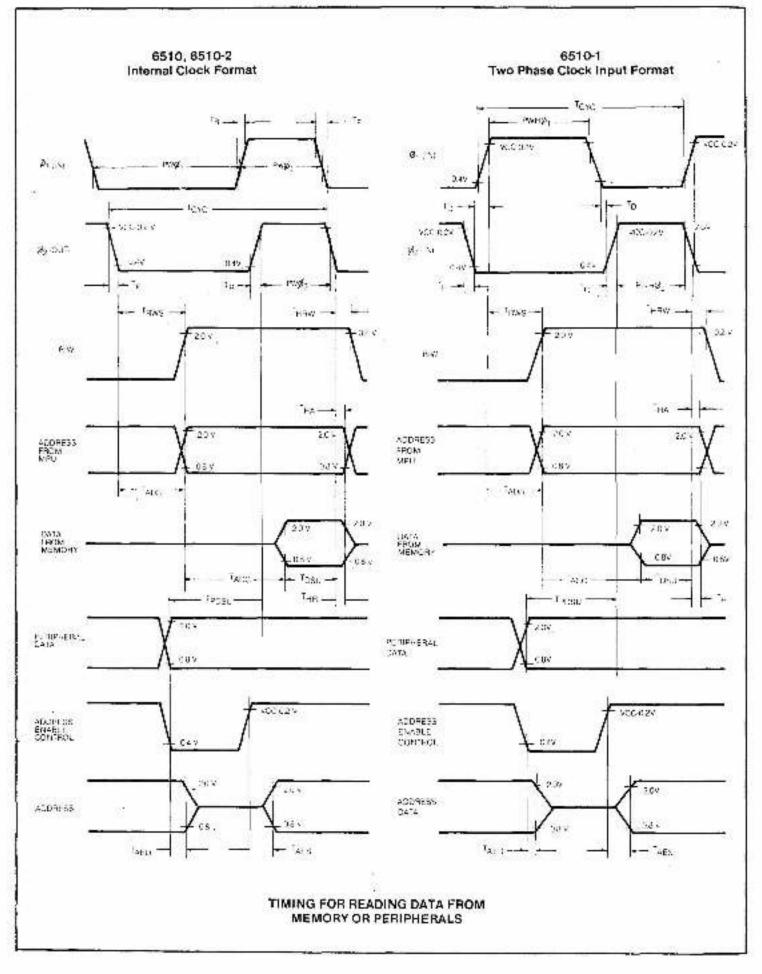
MAXIMUM RATINGS

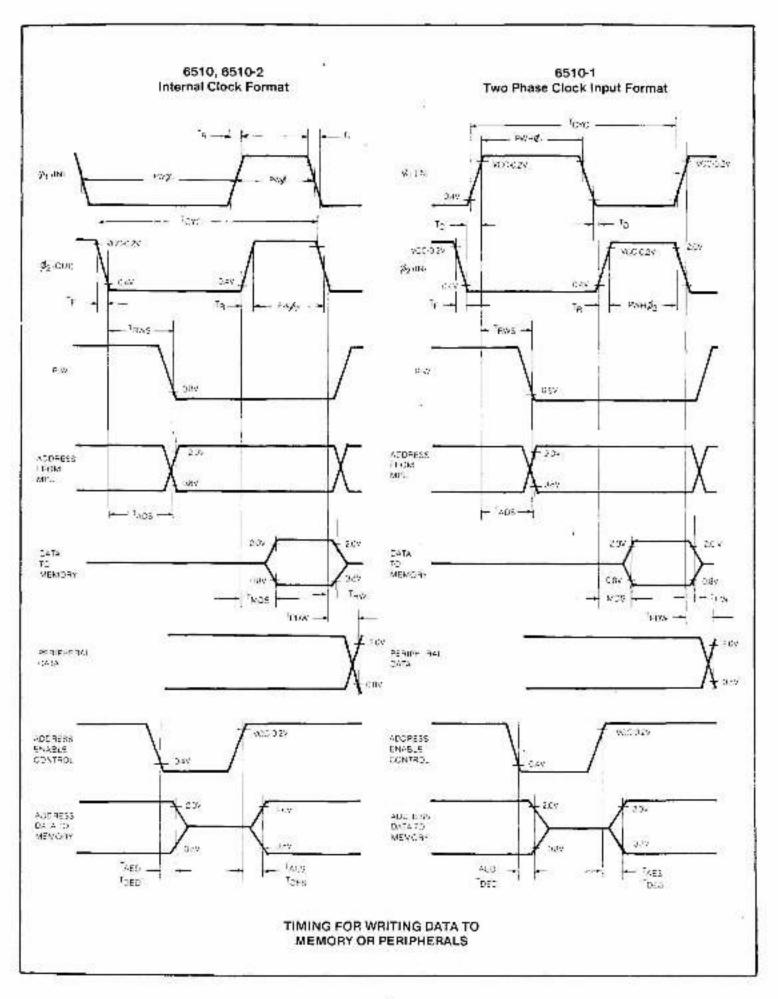
HA TNG	SYVBOL	VALUE	LNT
SUPPLY VOLTAGE	V _{ac}	-0.3 to + 7.0	Vdc
INPUT VOLTAGE	Vin	-03 to ± 7.0	Voc
OPERATING TEMPERATURE	TA	0 to +70	С
STORAGE 15M PERATURE	Tand	-50 to +150	C

The dawar contains input protection against damage due to high statio voltages or a electric fields, thowever presentions about the swen to exoclappication of voltages against than the maximum racing.

ELECTRICAL CHARACTERISTICS (Vcc = $5.0V \pm 5\%$, Vss = 0, T_A = 0° to $+70^{\circ}$ C)

CHARACIERISTIC	SYMBOL	MIN	1792	MAX.	UNIT
Input High Voltage あ. ぱられ — 6510 あ・n: — 6510, 6610-2 RES, キャキ, IPO, Data	VI-I	Von 02 74 20	-	Vcc + 1,6V - -	Vdc Vdc Vdc
mpol .pxx Voltage Ø ₁ (m) 6510-6510-2 Ø <u>1 Ø</u> 5(n) <u>66</u> 10-1 MES P _S -P, 17C Data	VIL	1	<u> </u>	0.4 0.2 0.8	Vdc Vdc Vdc
nout , eukage Current V _f = 0 to 5.25V, Vric = 5.25Vr 1930 Ø ₁ (n)	lin		-	2.5 100	µA ¢A
Trice State (Off State) Input Conert M _{IC} =04 to 2.4V, Voc. = 5.25V) DB ₂ -DB ₃ , A _V A ₁₄ , RAV	1759	84	_	10	<i>μ</i> .Α
Output High Vellage TICH — = OQLAdd, Voc = 475V) Data ASIA15, B.W. PP.	VOH	2.4		_	√dc
Old Low Vollage (I _{CL} = 1.8mAdd; Vcc = 4,75V) Data A0-A16, R/W, P ₂ -P	VOL	4	2	0.5	Vds
Fower Supply Current	KC	+	-	190	по.
Capsolance Vin = C. fg = 26 C. f = 1 MHz; Logid, F=P;	C.	2		10	2-
Data ADATo, F/W	Cout	=	1 B	15 12	
3 2	Co.	2	30 50	50 80	





AC CHARACTERISTICS

1 MHz TIMING

2 MHz TIMING

S MHZ TIMING

ELECTRICAL CHARACTER'ST CS (VCG -6V \pm 5%; VSS - CV $^+$ A = 0, -70 C). Minimum Clock Progrency + 50 IG/2

CLOCK TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Cycle Time T	Forc	:000	-	-	500	-		223		+	ns
Closer Pulco Width Ø1 (N iMeasured at VOC-02V)Ø2 N	PW-ZI PW-ZI	430 270	=	-	216 235	-	-	150 165	-	-	ns rs
rar Time, Krae Time Ø1 1N, Ø2 IN IMeastred from 0.29 to V00-0.29)	Tr. *	-	-	10			13			10	rs
Delay Time between Occks (Measured at 0.2v) 6510-1	lo:	9	1-		· c		+	.0	-	-	ra
Ø1 in Pulse Wath (Measured of 1 EV)	ചെയ്യ	400	-	1823	241	-	250	172	-	-86	га
gla Dun Pales Wight (Measured at 16V)	FWØ2	(2)	1.	510	200	_	250	130	_	170	rs
yl2 Out Pive, Fav Tone (Measured C 4V to 2,0V)*	TexTp		1.	25		-	25			25	re

READING/WRITE TIMING (LOAD-1 TTL)

CHARACTERISTIC	SYMBOL.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	XAM	UNITS
Acad Write Selve Time Irom 6510	Tows	-	193	300		:00	150		100	110	гѕ
Address Setup Time floor 65/10	TADS		100	300		330	150	-	100	125	0.8
Mornery Head Access Time	1400	-	-	57€	-	-	300		-	170	ca
Data (replica Time Ferrica	Tosu	100			60	-	-	42	-	-	09
Data Hold Time-Read	Ti-n	19	-		10		1-1	137			70
Daia Hold Time Write	tow	10	20	-	10	30	1-1	12	3.7		75
Dara Satup Time Irom 5510	-MD8		160	200		75	tre	-	15	90	l ne
Address Hold fime	THA	10	30	-	.0	31	-	17	30	5	15
R/W Hord Time	7+BW	17	50		1 0	33		10	ЭC		98
Celay Time (\$2 negative bacetion o Peripheral Data vanu	TPOW			333			190	-	-	125	rig
Pengharat Data Salop Time	Tebsu	803			:50			130	. .	\ -	716
Address Enable Setup Time	TAFS	-	-	76	-	-	75	-	1-	13	ms
Sin e produkt de de la time	THES		1 -	120		-	20	[-	12	120	115
Acdress Ossable Holg Time"	TAED	-	1 -	129		· -	195	-	-	20:	rs
Data Disable Hold Timer	ipen		-	120	-	-	130	-	-	138	18
Perunera Data rolo ime	Терн	900	1 -	-	20	-	1 - 1	10	-	-	mg_

⁻ Vote - T. Load CL-30 of

SIGNAL DESCRIPTION

Clocks (Ø1, Ø2)

The 651C requires either a two phase non overlapping block that runs at the Voc voltage level, or an external control for the internal clock generator.

Address Bus (Ac A.s)

The three state outplits are TII compatible, capable or driving one standard TTL load and 130 pt.

Data Bus (D_c-D₇)

Eight pins are used for the data buy. This is a Bill Direct and bus, transferring data to and from the dovice and penaherals. The outputs are tri-state buffers aspoble of driving one standard TTL load and 130 of.

Reset

fine input is used to reset or start the microprocessor from a power down condition. During the time that this line is hold low writing to or from the microprocessor is inhibited. When a positive edge is detected on the input the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock dyolos, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations ETEC and ETEQ. This is the start location for grogram control.

After Voc reaches 4.75 volto in a power up routine reset must be held low for at least two clock dydios. At this time the 9.6V signal will become valid.

When the reset signal goes high following these two crook cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Interrupt Request (IRQ)

This TTL level input requests that an intension sequence begin within the micropronessor. The micropronessor will complete the current instruction being executed before recognizing the request. At that time, the Interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag algainst that no further interrupts may occur. At the end of this cycle the program counter low will be logged from address EEEE and program counter high from location EEEE, therefore transferring program control to the microprovector located at those addresses.

Address Enable Control (AEC)

The Address Bus, R/W, and Data Bus are valid only when the Address Enable Control line is high; When low, the Address Bus, R/W and Data Bus are in a high impedance state. This feature allows easy DMA and multiprocessor systems.

1/O Port (Pa-Pa)

Eight pins are used for the poripheral port, which can transfer data to or from peripheral devices. The Ortput Bogister is located in RAM at Address 0001, and the Data Direction Register is at Address 0000. The outputs are capable at driving one standard TTL load and 130 of.

Read/Write (R/W)

This signal is generated by the microprocessor to control the direction of data transfers on the Data Bus. This line is high except when the microprocessor is writing to memory or a perioneral device.

ADDRESSING MODES

ACCUMULATOR ADDRESSING — This form of addressing is represented with a one over instruction, implying an operation on the accomplator.

IMMEDIATE ADDRESSING — in immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING - In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high. circler bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING — The zero page instructions above to shorter code and execution tries by only leading the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code afficiency.

INDEXED ZERO PAGE ADDRESSING -- (X, Y indexing) -- This form of addressing is used in conjunction with the index register. and is referred to as "Zero Fage, X" or "Zero Page, Y" The effective address is desculated by adding the second byte to the corrects of the index register. Since this is a form of 'Zero Page' addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order & bits of memory and crossing of page opundaries does not occur.

INDEX ABSOLUTE ADDRESSING (X-Y indexing) This form of appressing is used in conjunction with X and Y index register. and is referred to as "Absolute, X," and "Absolute "." The effective address is formed by adding the contents of X and Y to the aggress contained in the second and third overs of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING - In the implied addressing made, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING — Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits at the program counter when the counter is set at the next instruction. The range of the offset is -- 128 to 1, 127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING — In indexed indirect addressing (referred to as (Indirect, X), the second byte of the instruction is added to the contents of the X index register. discarding the carry. The result of this addition points to a memory. location on gage zero whose contents is the low order eight bils. of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both momory locations specifying the high and low order bytes of the officially address must be in page zero.

INDIRECT INDEXED ADDRESSING — In indirect indexed addressing (referred to as (Indirect, YI), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Yindex register, the result being the low order eight bits of the effective address. The narry from this addition is added to the contents of the next page zero memory location, the result being the floor order eight bits of the effective address.

ABSOLUTE INDIRECT — The second byte of the instruction. contains the low order eight bits of a memory location. The fright order eight bits of that memory location is contained in the third. byte of the instruction. The contents of the fully specified memory. location is the low order byte of the effective address." memory location contains the high order byte of the effective address which is leaded into the sixteen bits of the programcounter

INSTRUCTION SET - ALPHABETIC SEQUENCE

- ADS Add Memory to Accomplator with Carry
- AND FARIOT Memory with Appumptions ASL Shift tell One Buildemary or Appumption:
- BCC Branch or Carry Clear BCS Branch on Carry Sel
- 030 Sranon on Result Zerb.
- Test Brain Memory with Accumulation Branch on Result Minus
- SME Branch on Result not Zero.
- SPL Branch on Basul Plus
- **384** Force Broak
- Stanch on Over-ow Clear SW.
- Branch or Over ow Sul-543
- Clear Cardinate C.C
- CLO Clear Decimal Mode
- Clear Intein.or Disable B1
- CEV Clear Over ow Flag CMP Conglete Memory and Accumulator
- Compare Memory and Index A JPA.
- Compare Memory and Index 1 CEY
- CCC Decrement Memory by One.
- Decrement index X by One Decrement index Y by One
- DEY
- EBA "Expusive or" Mamory with Accumulation
- 40 horement Memory by Obs.
- 40. norement Index X by One
- 414 norament Index Y by One
- JMH Jump to New Socation
- USA. Tumb to New accessor Saving Hetern Acrtress.

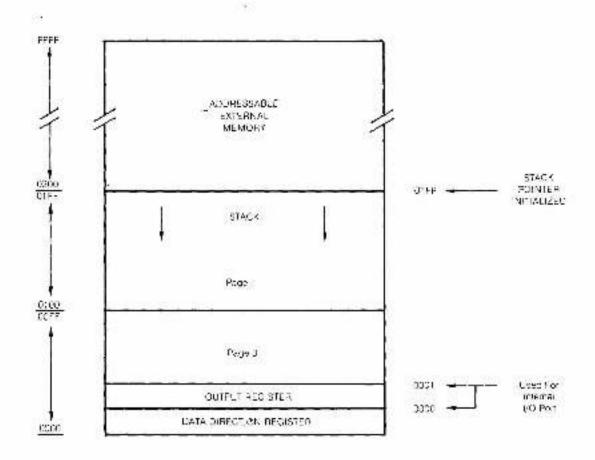
- ALC: N Load Accumulator with Memory.
- TEX Load Index X with Memory
- LDY Load Index Y with Memory
- LSB Shift One Bit Fight: Memory of Accumulators
- NOF No Operation
- ORA 10H Memory wch Accumulator
- FHA Push Acquirulator on Black
- Push Processor Status on Stack CHE
- FLA Pull Accumulator from Stack Poli Processor Surus from Stack PLP
- FQL. Rolate One Bit tielt (Melhory or Accomplator)
- GOB . Botale One Bit Right i Memrey is Appunication
- Helam from Interrupt Return from Subroutine 211
- ATS
- SRC Subtract Memory from Accumulator with Bonow
- SEC.
- Se: Carry Flag Se: Becma-Mode
- Set Interrupt Disable Status 5E1 STA
- Store Accumulator of Mediciny SIX Store Index X in Memory
- STV Store it day if in Memory
- *AX Itanale: Accumulator to Index 3
- 24 fransler Accumulator to Index Y.
- SX Transfer Stack Fornier to Index X
- XA Transfer Index X to Accumulator
- 123 Iranslet Index X to Stack Register
- fransler index Y to Accumulator

PROGRAMMING MODEL PROCESSOR STATUS RESIR ACCUMULATOR CAPPA = REG 2640 : * RESULTION) MOSK REDISTER FIG DISABLE 1 - DISABLE DEC MAL MOLE 1 - TELE 5000 00 GPM II. BEK OZMWANIC PROCESIN COUNTER POR PCT. CKSSP,CW + LETRIE NEGATIVE 1 VEC STACK POINTER INSTRUCTION SET-OF CODES, Execution Time, Memory Requirements THE STATE OF THE S THEFTHE

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New Committee Services, July Supplication, adding from the Automorphisms



6510 MEMORY MAP

APPLICATIONS NOTES

Locating the Output Register at the internal I/O Port in Page Zero enhances the powerful Zero Fage. Addressing instructions of the 6510.

By assigning the I/O Pins as induct (using the Data Direction Register) the user has the ability to change the contents of address 0001 (the Output Register) using peripheral devices. The ability to change these contents using peripheral inputs, together with Zero Page Indirect Addressing instructions, allows novel and versalile programming techniques not possible earlier.

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