# 74HC573; 74HCT573

# Octal D-type transparent latch; 3-state Rev. 03 — 17 January 2006

**Product data sheet** 

#### **General description** 1.

The 74HC573; 74HCT573 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC573; 74HCT573 has octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state true outputs for bus oriented applications. A latch enable (LE) input and an output enable (OE) input are common to all latches.

When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When OE is LOW, the contents of the 8 latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the OE input does not affect the state of the latches.

The 74HC573; 74HCT573 is functionally identical to:

- 74HC563; 74HCT563, but inverted outputs
- 74HC373; 74HCT373, but different pin arrangement

#### **Features** 2.

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors and microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to 74HC563; 74HCT563 and 74HC373; 74HCT373
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C



### 3. Quick reference data

**Table 1:** Quick reference data  $GND = 0 \ V; \ T_{amb} = 25 \ ^{\circ}C; \ t_r = t_f = 6 \ ns$ 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74HC573	3					
t <sub>PHL</sub> ,	propagation delay	$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$				
t <sub>PLH</sub>	Dn to Qn		-	14	-	ns
	LE to Qn		-	15	-	ns
Ci	input capacitance		-	3.5	-	pF
$C_{PD}$	power dissipation capacitance	per latch; V <sub>I</sub> = GND to V <sub>CC</sub>	[1] -	26	-	pF
74HCT57	73					
t <sub>PHL,</sub>	propagation delay	$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$				
t <sub>PLH</sub>	Dn to Qn		-	17	-	ns
	LE to Qn		-	15	-	ns
Ci	input capacitance		-	3.5	-	pF
$C_{PD}$	power dissipation capacitance	per latch; $V_I = GND$ to $(V_{CC} - 1.5 V)$	[1] -	26	-	pF

<sup>[1]</sup>  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

 $f_o$  = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$ 

# 4. Ordering information

**Table 2: Ordering information** 

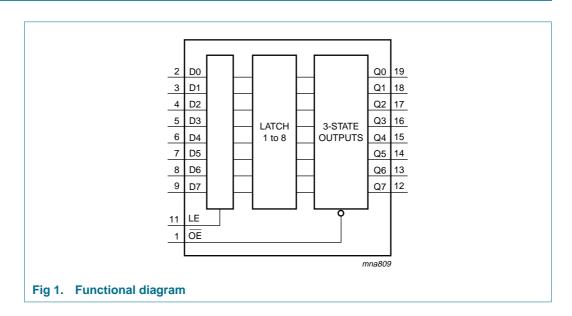
Type number	Package						
	Temperature range	Name	Description	Version			
74HC573	·			·			
74HC573N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1			
74HC573D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1			
74HC573DB	–40 °C to +125 °C	SSOP20	plastic small outline package; 20 leads; body width 5.3 mm	SOT339-1			
74HC573PW	–40 °C to +125 °C	TSSOP20	plastic small outline package; 20 leads; body width 4.4 mm	SOT360-1			
74HC573BQ	–40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85$ mm	SOT764-1			

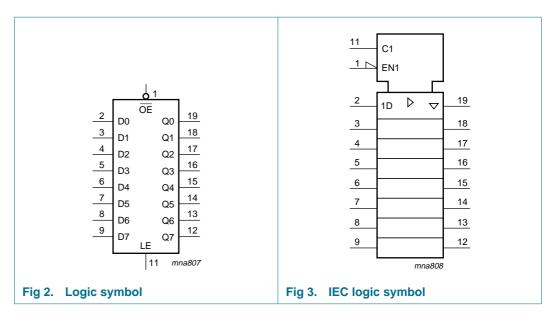


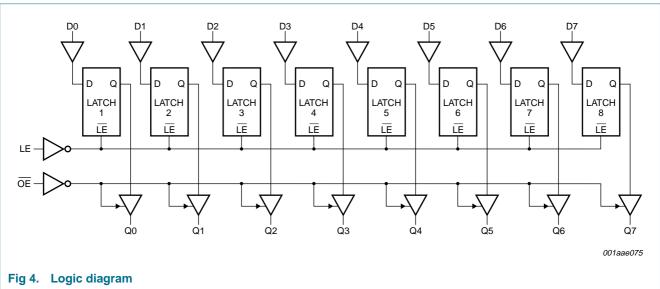
 Table 2:
 Ordering information ...continued

Type number	Package						
	Temperature range	Name	Description	Version			
74HCT573	·						
74HCT573N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1			
74HCT573D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1			
74HCT573DB	–40 °C to +125 °C	SSOP20	plastic small outline package; 20 leads; body width 5.3 mm	SOT339-1			
74HCT573PW	–40 °C to +125 °C	TSSOP20	plastic small outline package; 20 leads; body width 4.4 mm	SOT360-1			
74HCT573BQ	–40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85$ mm	SOT764-1			

# 5. Functional diagram

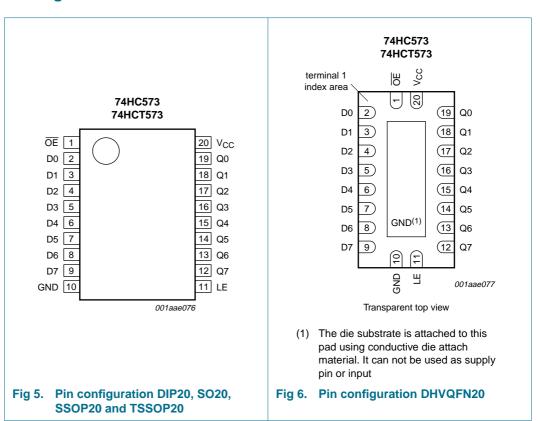






# 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
ŌĒ	1	3-state output enable input (active LOW)
D0	2	data input 0
D1	3	data input 1
D2	4	data input 2
D3	5	data input 3
D4	6	data input 4
D5	7	data input 5
D6	8	data input 6
D7	9	data input 7
GND	10	ground (0 V)
LE	11	latch enable input (active HIGH)
Q7	12	3-state latch output 7
Q6	13	3-state latch output 6
Q5	14	3-state latch output 5

74HC\_HCT573\_3



Symbol	Pin	Description
Q4	15	3-state latch output 4
Q3	16	3-state latch output 3
Q2	17	3-state latch output 2
Q1	18	3-state latch output 1
Q0	19	3-state latch output 0
V <sub>CC</sub>	20	supply voltage

# 7. Functional description

Table 4: Function table [1]

Operating mode	Control		Input	Internal	Output
	OE	LE	Dn	latches	Qn
Enable and read register	L	Н	L	L	L
(transparent mode)			Н	Н	Н
Latch and read register	L	L	1	L	L
			h	Н	Н
Latch register and disable outputs	Н	L	ļ	L	Z
			h	Н	Z

<sup>[1]</sup> H = HIGH voltage level;

# 8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$	-	±20	mA
$I_{OK}$	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$	-	±20	mA
Io	output current	$V_O = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-	±35	mA
$I_{CC}$	quiescent supply current		-	70	mA
$I_{GND}$	ground current		-	-70	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;

L = LOW voltage level;

 $<sup>\</sup>label{eq:lower} I = LOW \ voltage \ level \ one \ set-up \ time \ prior \ to \ the \ HIGH-to-LOW \ LE \ transition;$ 

Z = high-impedance OFF-state.

Table 5: Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub>	total power dissipation				
	DIP20 package		[1]	750	mW
	SO20 package		[2] _	500	mW
	SSOP20 package		[3] _	500	mW
	TSSOP20 package		[3] _	500	mW
	DHVQFN20 package		[4] _	500	mW

- [1] For DIP20 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.
- [2] For SO20 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.
- [3] For SSOP20 and TSSOP20 packages: Ptot derates linearly with 5.5 mW/K above 60  $^{\circ}\text{C}$
- [4] For DHVQFN20 package: Ptot derates linearly with 4.5 mW/K above 60 °C.

# 9. Recommended operating conditions

Table 6: Recommended operating conditions

Parameter	Conditions	Min	Тур	Max	Unit
supply voltage		2.0	5.0	6.0	V
input voltage		0	-	$V_{CC}$	V
output voltage		0	-	$V_{CC}$	V
ambient temperature		-40	+25	+125	°C
input rise and fall time	$V_{CC} = 2.0 \text{ V}$	-	-	1000	ns
	$V_{CC} = 4.5 \text{ V}$	-	6.0	500	ns
	$V_{CC} = 6.0 \text{ V}$	-	-	400	ns
3					
supply voltage		4.5	5.0	5.5	V
input voltage		0	-	$V_{CC}$	V
output voltage		0	-	V <sub>CC</sub>	V
ambient temperature		-40	+25	+125	°C
input rise and fall time	$V_{CC} = 4.5 \text{ V}$	-	6.0	500	ns
3	input voltage output voltage ambient temperature input rise and fall time  supply voltage input voltage output voltage ambient temperature	input voltage output voltage ambient temperature input rise and fall time $\frac{V_{CC} = 2.0 \text{ V}}{V_{CC} = 4.5 \text{ V}}$ supply voltage input voltage output voltage ambient temperature	input voltage 0 output voltage 0 ambient temperature $-40$ input rise and fall time $V_{CC} = 2.0 \text{ V}$ $ V_{CC} = 4.5 \text{ V}$ $-$ supply voltage 4.5 input voltage 0 output voltage 0 ambient temperature $-40$	input voltage $0 - coutput voltage = coutput voltage = coutput voltage = coutput voltage = coutput rise and fall time  $	input voltage $0  -  V_{CC}$ output voltage $0  -  V_{CC}$ ambient temperature $-40  +25  +125$ input rise and fall time $\frac{V_{CC} = 2.0 \text{ V}}{V_{CC} = 4.5 \text{ V}}  -  6.0  500$ $V_{CC} = 6.0 \text{ V}  -  -  400$ supply voltage $4.5  5.0  5.5$ input voltage $0  -  V_{CC}$ output voltage $0  -  V_{CC}$ ambient temperature $-40  +25  +125$

# 10. Static characteristics

Table 7: Static characteristics 74HC573

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T <sub>amb</sub> = 2	25 °C					
V <sub>IH</sub>	HIGH-state input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	V
		$V_{CC} = 4.5 \text{ V}$	3.15	2.4	-	V
		$V_{CC} = 6.0 \text{ V}$	4.2	3.2	-	V
V <sub>IL</sub>	LOW-state input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	V
		$V_{CC} = 4.5 \text{ V}$	-	2.1	1.35	V
		$V_{CC} = 6.0 \text{ V}$	-	2.8	1.8	V
$V_{OH}$	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$	-	-	-	
		$I_{O} = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	V
		$I_O = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	V
		$I_O = -20 \mu A; V_{CC} = 6.0 \text{ V}$	5.9	6.0	-	V
		$I_O = -6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	V
		$I_{O} = -7.8 \text{ mA}; V_{CC} = 6 \text{ V}$	5.48	5.81	-	V
V <sub>OL</sub>	LOW-state output voltage	$V_{I} = V_{IH}$ or $V_{IL}$				
		$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	0	0.1	V
		$I_O = 20 \mu A$ ; $V_{CC} = 4.5 \text{ V}$	-	0	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 \text{ V}$	-	0	0.1	V
		$I_O = 6.0 \text{ mA}$ ; $V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	V
		$I_O = 7.8 \text{ mA}; V_{CC} = 6 \text{ V}$	-	0.16	0.26	V
ILI	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6 \text{ V}$	-	-	±0.1	μΑ
l <sub>oz</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND	-	-	±0.5	μΑ
I <sub>CC</sub>	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	μΑ
Ci	input capacitance		-	3.5	-	pF
T <sub>amb</sub> = -	-40 °C to +85 °C					
V <sub>IH</sub>	HIGH-state input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		$V_{CC} = 4.5 \text{ V}$	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
V <sub>IL</sub>	LOW-state input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.8	V
V <sub>OH</sub>	HIGH-state output voltage	$V_{I} = V_{IH}$ or $V_{IL}$				
		$I_O = -20 \mu A; V_{CC} = 2.0 V$	1.9	-	-	V
		$I_O = -20 \mu A; V_{CC} = 4.5 V$	4.4	-	-	V
		$I_O = -20 \mu A$ ; $V_{CC} = 6.0 \text{ V}$	5.9	-	-	V
		$I_O = -6.0 \text{ mA}$ ; $V_{CC} = 4.5 \text{ V}$	3.84	-	-	V
		$I_O = -7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.34	-	-	V

74HC\_HCT573\_3

 Table 7:
 Static characteristics 74HC573 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{OL}$	LOW-state output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 \text{ V}$	-	-	0.1	V
		$I_{O} = 6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.33	V
		I <sub>O</sub> = 7.8 mA; V <sub>CC</sub> = 6 V	-	-	0.33	V
I <sub>LI</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6 \text{ V}$	-	-	±1.0	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND	-	-	±5.0	μΑ
I <sub>CC</sub>	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	80	μΑ
T <sub>amb</sub> = -	40 °C to +125 °C					
V <sub>IH</sub>	HIGH-state input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
V <sub>IL</sub>	LOW-state input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.8	V
V <sub>OH</sub>	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -20 \mu A; V_{CC} = 2.0 V$	1.9	-	-	V
		$I_O = -20 \mu A$ ; $V_{CC} = 4.5 \text{ V}$	4.4	-	-	V
		$I_{O} = -20 \mu A; V_{CC} = 6.0 V$	5.9	-	-	V
		$I_{O} = -6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.7	-	-	V
		$I_{O} = -7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.2	-	-	V
$V_{OL}$	LOW-state output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 V$	-	-	0.1	V
		$I_O = 6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.4	V
		$I_O = 7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	-	0.4	V
ILI	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±1.0	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND	-	-	±10.0	μΑ
I <sub>CC</sub>	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	160	μΑ

#### Table 8: Static characteristics 74HCT573

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$T_{amb} = 2$	25 °C					
$V_{IH}$	HIGH-state input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	V
$V_{IL}$	LOW-state input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	V

74HC\_HCT573\_3



At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>OH</sub>	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$				
		$I_{O} = -20 \mu\text{A}$	4.4	4.5	-	V
		$I_{O} = -6.0 \text{ mA}$	3.98	4.32	-	V
V <sub>OL</sub>	LOW-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$				
		I <sub>O</sub> = 20 μA	-	0	0.1	V
		I <sub>O</sub> = 6.0 mA	-	0.16	0.26	V
I <sub>LI</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND per input pin; other inputs at GND or $V_{CC}$ ; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	±0.5	μΑ
I <sub>CC</sub>	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	μΑ
Δl <sub>CC</sub> additional quiescent supply current		per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other inputs at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 4.5 \text{ V}$ to 5.5 V				
	Dn		-	35	126	μΑ
	LE		-	65	234	μΑ
	ŌĒ		-	125	450	μΑ
Ci	input capacitance		-	3.5	-	pF
T <sub>amb</sub> = -	40 °C to +85 °C					
V <sub>IH</sub>	HIGH-state input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	V
V <sub>IL</sub>	LOW-state input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	V
V <sub>OH</sub>	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$				
		$I_O = -20 \mu A$	4.4	-	-	V
		$I_{O} = -6.0 \text{ mA}$	3.84	-	-	V
$V_{OL}$	LOW-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$				
		$I_O = 20 \mu A$	-	-	0.1	V
		I <sub>O</sub> = 6.0 mA	-	-	0.33	V
I <sub>LI</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±1.0	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND per input pin; other inputs at GND or $V_{CC}$ ; $I_O = 0$ A; $V_{CC} = 5.5$ V			±5.0	μΑ
Icc	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	80	μΑ
Δl <sub>CC</sub>	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V				
	Dn		-	-	158	μΑ
	LE		-	-	293	μΑ
	ŌĒ		-	-	563	μΑ



At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T <sub>amb</sub> = -	40 °C to +125 °C					
$V_{IH}$	HIGH-state input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	V
V <sub>IL</sub>	LOW-state input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	V
V <sub>OH</sub>	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$				
		$I_{O} = -20 \mu\text{A}$	4.4	-	-	V
		$I_{O} = -6.0 \text{ mA}$	3.7	-	-	V
V <sub>OL</sub>	LOW-state output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$				
		I <sub>O</sub> = 20 μA	-	-	0.1	V
		I <sub>O</sub> = 6.0 mA	-	-	0.4	V
ILI	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±1.0	μΑ
I <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND per input pin; other inputs at GND or $V_{CC}$ ; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	±10.0	μΑ
I <sub>CC</sub>	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	160	μΑ
$\Delta I_{CC}$	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V				
	Dn		-	-	172	μΑ
	LE		-	-	319	μΑ
	ŌĒ		-	-	613	μΑ

# 11. Dynamic characteristics

Table 9: Dynamic characteristics 74HC573

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see <u>Figure 11</u>.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$T_{amb} = 2$	5 °C					
t <sub>PHL</sub> ,	propagation delay Dn to Qn	see Figure 7				
t <sub>PLH</sub>		$V_{CC} = 2.0 \text{ V}$	-	47	150	ns
		V <sub>CC</sub> = 4.5 V	-	17	30	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	14	-	ns
		V <sub>CC</sub> = 6.0 V	-	14	26	ns
t <sub>PHL</sub> ,	propagation delay LE to Qn	see Figure 8				
t <sub>PLH</sub>		V <sub>CC</sub> = 2.0 V	-	50	150	ns
		V <sub>CC</sub> = 4.5 V	-	18	30	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	15	-	ns
		V <sub>CC</sub> = 6.0 V	-	14	26	ns
t <sub>PZH</sub> ,	3-state output enable time OE to Qn	see Figure 9				
$t_{PZL}$		V <sub>CC</sub> = 2.0 V	-	44	140	ns
		V <sub>CC</sub> = 4.5 V	-	16	28	ns
		$V_{CC} = 6.0 \text{ V}$	-	13	24	ns

 Table 9:
 Dynamic characteristics 74HC573 ...continued

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
PHZ,	3-state output disable time OE to Qn	see Figure 9				
PLZ		V <sub>CC</sub> = 2.0 V	-	55	150	ns
		V <sub>CC</sub> = 4.5 V	-	20	30	ns
		V <sub>CC</sub> = 6.0 V	-	16	26	ns
THL,	output transition time	see Figure 7				
TLH		V <sub>CC</sub> = 2.0 V	-	14	60	ns
		V <sub>CC</sub> = 4.5 V	-	5	12	ns
		V <sub>CC</sub> = 6.0 V	-	4	10	ns
W	pulse width LE HIGH	see Figure 8				
		V <sub>CC</sub> = 2.0 V	80	14	-	ns
		V <sub>CC</sub> = 4.5 V	16	5	-	ns
		V <sub>CC</sub> = 6.0 V	14	4	-	ns
·su	set-up time Dn to LE	see Figure 10				
		V <sub>CC</sub> = 2.0 V	50	11	-	ns
		V <sub>CC</sub> = 4.5 V	10	4	-	ns
		V <sub>CC</sub> = 6.0 V	9	3	-	ns
h	hold time Dn to LE	see Figure 10				
		V <sub>CC</sub> = 2.0 V	5	3	-	ns
		V <sub>CC</sub> = 4.5 V	5	1	-	ns
		V <sub>CC</sub> = 6.0 V	5	1	-	ns
C <sub>PD</sub>	power dissipation capacitance	per latch; $V_I = GND$ to $V_{CC}$	<u>[1]</u> _	26	-	pF
Γ <sub>amb</sub> = -	40 to +85 °C					
PHL,	propagation delay Dn to Qn	see Figure 7				
PLH		V <sub>CC</sub> = 2.0 V	-	-	190	ns
		V <sub>CC</sub> = 4.5 V	-	-	38	ns
		V <sub>CC</sub> = 6.0 V	-	-	33	ns
PHL,	propagation delay LE to Qn	see Figure 8				
PLH		V <sub>CC</sub> = 2.0 V	-	-	190	ns
		V <sub>CC</sub> = 4.5 V	-	-	38	ns
		V <sub>CC</sub> = 6.0 V	-	-	33	ns
PZH,	3-state output enable time OE to Qn	see Figure 9				
PZL		V <sub>CC</sub> = 2.0 V	-	-	175	ns
		$V_{CC} = 4.5 \text{ V}$	-	-	35	ns
		$V_{CC} = 6.0 \text{ V}$	-	-	30	ns
PHZ,	3-state output disable time OE to Qn	see Figure 9				
PLZ		V <sub>CC</sub> = 2.0 V	-	-	190	ns
		V <sub>CC</sub> = 4.5 V	-	-	38	ns
		V <sub>CC</sub> = 6.0 V	-	-	33	ns

 Table 9:
 Dynamic characteristics 74HC573 ...continued

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
THL,	output transition time	see Figure 7				
TLH		V <sub>CC</sub> = 2.0 V	-	-	75	ns
		V <sub>CC</sub> = 4.5 V	-	-	15	ns
		V <sub>CC</sub> = 6.0 V	-	-	13	ns
W	pulse width LE HIGH	see Figure 8				
		V <sub>CC</sub> = 2.0 V	100	-	-	ns
		V <sub>CC</sub> = 4.5 V	20	-	-	ns
		V <sub>CC</sub> = 6.0 V	17	-	-	ns
su	set-up time Dn to LE	see Figure 10				
		V <sub>CC</sub> = 2.0 V	65	-	-	ns
		V <sub>CC</sub> = 4.5 V	13	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	11	-	-	ns
h	hold time Dn to LE	see Figure 10				
		V <sub>CC</sub> = 2.0 V	5	-	-	ns
		V <sub>CC</sub> = 4.5 V	5	-	-	ns
		V <sub>CC</sub> = 6.0 V	5	-	-	ns
「 <sub>amb</sub> = -	40 to +125 °C					
t <sub>PHL</sub> , propagation delay Dn to Qn		see Figure 7				
PLH		$V_{CC} = 2.0 \text{ V}$	-	-	225	ns
		$V_{CC} = 4.5 \text{ V}$	-	-	45	ns
		$V_{CC} = 6.0 \text{ V}$	-	-	38	ns
PHL,	propagation delay LE to Qn	see Figure 8				
PLH		$V_{CC} = 2.0 \text{ V}$	-	-	225	ns
		$V_{CC} = 4.5 \text{ V}$	-	-	45	ns
		V <sub>CC</sub> = 6.0 V	-	-	38	ns
PZH,	3-state output enable time $\overline{\text{OE}}$ to Qn	see Figure 9				
PZL		V <sub>CC</sub> = 2.0 V	-	-	210	ns
		V <sub>CC</sub> = 4.5 V	-	-	42	ns
		V <sub>CC</sub> = 6.0 V	-	-	36	ns
PHZ,	3-state output disable time $\overline{OE}$ to Qn	see Figure 9				
PLZ		V <sub>CC</sub> = 2.0 V	-	-	225	ns
		V <sub>CC</sub> = 4.5 V	-	-	45	ns
		V <sub>CC</sub> = 6.0 V	-	-	38	ns
THL,	output transition time	see Figure 7				
TLH		V <sub>CC</sub> = 2.0 V	-	-	90	ns
		V <sub>CC</sub> = 4.5 V	-	-	18	ns
		V <sub>CC</sub> = 6.0 V	_	_	15	ns



Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>W</sub>	pulse width LE HIGH	see Figure 8				
		V <sub>CC</sub> = 2.0 V	120	-	-	ns
		V <sub>CC</sub> = 4.5 V	24	-	-	ns
		V <sub>CC</sub> = 6.0 V	20	-	-	ns
t <sub>su</sub>	set-up time Dn to LE	see Figure 10				
		V <sub>CC</sub> = 2.0 V	75	-	-	ns
		V <sub>CC</sub> = 4.5 V	15	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	13	-	-	ns
t <sub>h</sub>	hold time Dn to LE	see Figure 10				
		$V_{CC} = 2.0 \text{ V}$	5	-	-	ns
		V <sub>CC</sub> = 4.5 V	5	-	-	ns
		V <sub>CC</sub> = 6.0 V	5	-	-	ns

<sup>[1]</sup>  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

Table 10: Dynamic characteristics 74HCT573

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T <sub>amb</sub> = 2	5 °C					
t <sub>PHL</sub> ,	propagation delay Dn to Qn	see Figure 7				
t <sub>PLH</sub>		V <sub>CC</sub> = 4.5 V	-	20	35	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	17	-	ns
t <sub>PHL</sub> ,	propagation delay LE to Qn	see Figure 8				
t <sub>PLH</sub>		$V_{CC} = 4.5 \text{ V}$	-	18	35	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	15	-	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to Qn	V <sub>CC</sub> = 4.5 V; see <u>Figure 9</u>	-	17	30	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to Qn	V <sub>CC</sub> = 4.5 V; see <u>Figure 9</u>	-	18	30	ns
t <sub>THL</sub> , t <sub>TLH</sub>	output transition time	V <sub>CC</sub> = 4.5 V; see <u>Figure 7</u>	-	5	12	ns
t <sub>W</sub>	pulse width LE HIGH	V <sub>CC</sub> = 4.5 V; see Figure 8	16	5	-	ns
t <sub>su</sub>	set-up time Dn to LE	V <sub>CC</sub> = 4.5 V; see <u>Figure 10</u>	13	7	-	ns
t <sub>h</sub>	hold time Dn to LE	$V_{CC} = 4.5 \text{ V}$ ; see Figure 10	9	4	-	ns
C <sub>PD</sub>	power dissipation capacitance	per latch; V <sub>I</sub> = GND to (V <sub>CC</sub> – 1.5 V)	<u>[1]</u> -	26	-	pF

74HC\_HCT573\_3

Table 10: Dynamic characteristics 74HCT573 ...continued

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T <sub>amb</sub> = -	40 to +85 °C					
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay Dn to Qn	V <sub>CC</sub> = 4.5 V; see <u>Figure 7</u>	-	-	44	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay LE to Qn	V <sub>CC</sub> = 4.5 V; see <u>Figure 8</u>	-	-	44	ns
PZH,	3-state output enable time $\overline{\sf OE}$ to Qn	V <sub>CC</sub> = 4.5 V; see <u>Figure 9</u>	-	-	38	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to Qn	V <sub>CC</sub> = 4.5 V; see Figure 9	-	-	38	ns
THL,	output transition time	V <sub>CC</sub> = 4.5 V; see <u>Figure 7</u>	-	-	15	ns
t <sub>W</sub>	pulse width LE HIGH	V <sub>CC</sub> = 4.5 V; see Figure 8	20	-	-	ns
t <sub>su</sub>	set-up time Dn to LE	V <sub>CC</sub> = 4.5 V; see <u>Figure 10</u>	16	-	-	ns
t <sub>h</sub>	hold time Dn to LE	V <sub>CC</sub> = 4.5 V; see Figure 10	11	-	-	ns
T <sub>amb</sub> = -	40 to +125 °C					
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay Dn to Qn	V <sub>CC</sub> = 4.5 V; see <u>Figure 7</u>	-	-	53	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay LE to Qn	V <sub>CC</sub> = 4.5 V; see <u>Figure 8</u>	-	-	53	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	3-state output enable time $\overline{\text{OE}}$ to Qn	V <sub>CC</sub> = 4.5 V; see <u>Figure 9</u>	-	-	45	ns
t <sub>PHZ</sub> ,	3-state output disable time $\overline{\text{OE}}$ to Qn	V <sub>CC</sub> = 4.5 V; see <u>Figure 9</u>	-	-	45	ns
THL,	output transition time	V <sub>CC</sub> = 4.5 V; see <u>Figure 7</u>	-	-	18	ns
t <sub>W</sub>	pulse width LE HIGH	V <sub>CC</sub> = 4.5 V; see <u>Figure 8</u>	24	-	-	ns
t <sub>su</sub>	set-up time Dn to LE	V <sub>CC</sub> = 4.5 V; see <u>Figure 10</u>	20	-	-	ns
t <sub>h</sub>	hold time Dn to LE	V <sub>CC</sub> = 4.5 V; see Figure 10	14	-	-	ns

<sup>[1]</sup>  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \sum (C_L \times V_{CC}{}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 12. Waveforms

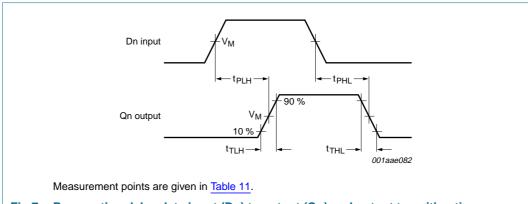
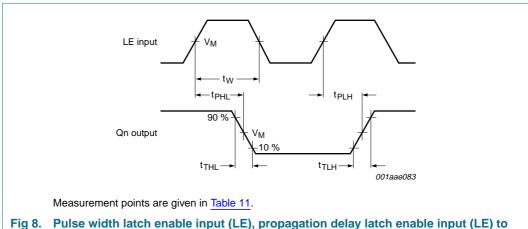
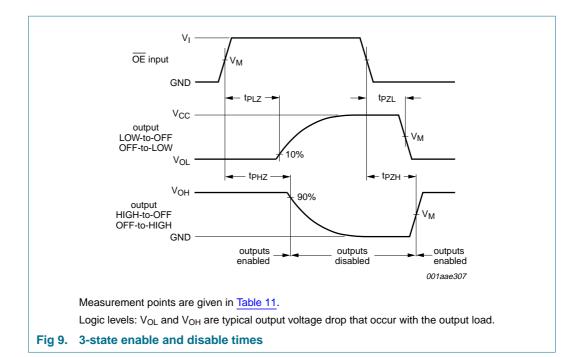
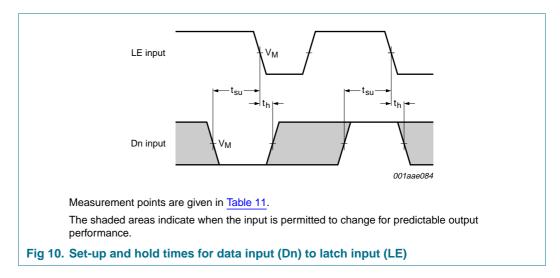


Fig 7. Propagation delay data input (Dn) to output (Qn) and output transition time



output (Qn) and output transition time





**Table 11: Measurement points** 

Туре	Input	Output
	V <sub>M</sub>	V <sub>M</sub>
74HC573	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
74HCT573	1.3 V	1.3 V

17 of 26

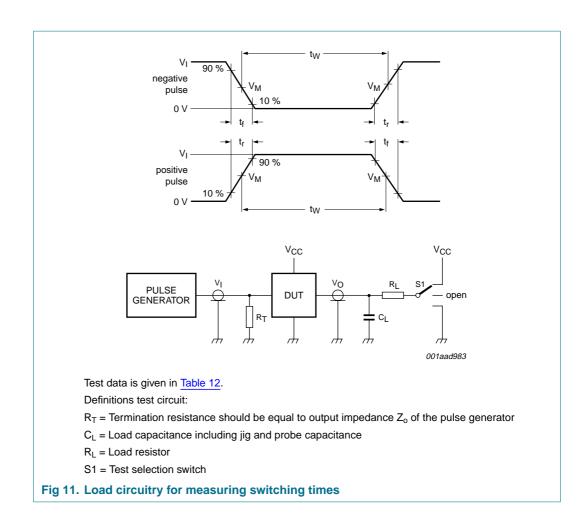


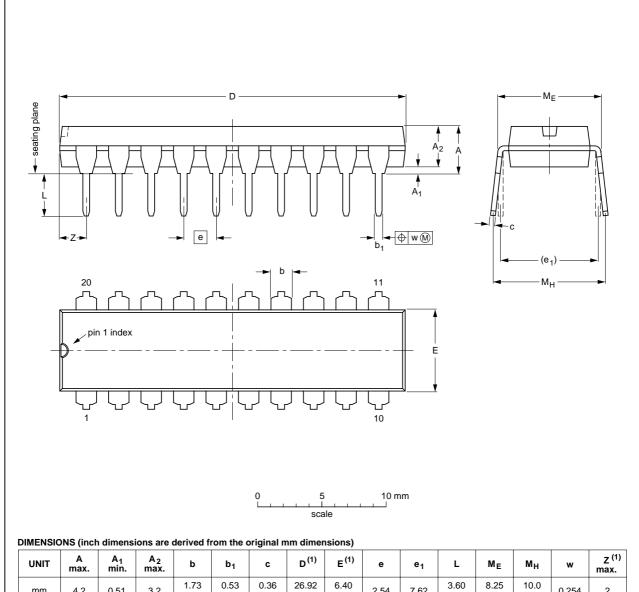
Table 12: Test data

Туре	Input		Load		S1 position			
	VI	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>	
74HC573	$V_{CC}$	6 ns	15 pF, 50 pF	1 kΩ	open	GND	$V_{CC}$	
74HCT573	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>	

# 13. Package outline

### DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	e <sub>1</sub>	L	ME	Мн	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

#### Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

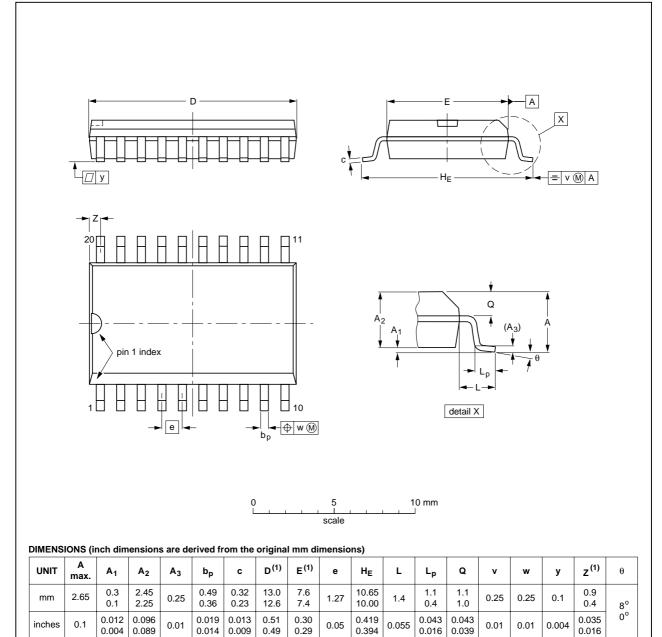
OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT146-1		MS-001	SC-603			<del>99-12-27</del> 03-02-13

Fig 12. Package outline SOT146-1 (DIP20)

74HC\_HCT573\_3

#### SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



#### inches 0.1 0.004

Note 1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.014

0.009

0.49

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT163-1	075E04	MS-013			<del>99-12-27</del> 03-02-19	

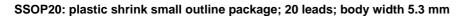
0.394

0.016

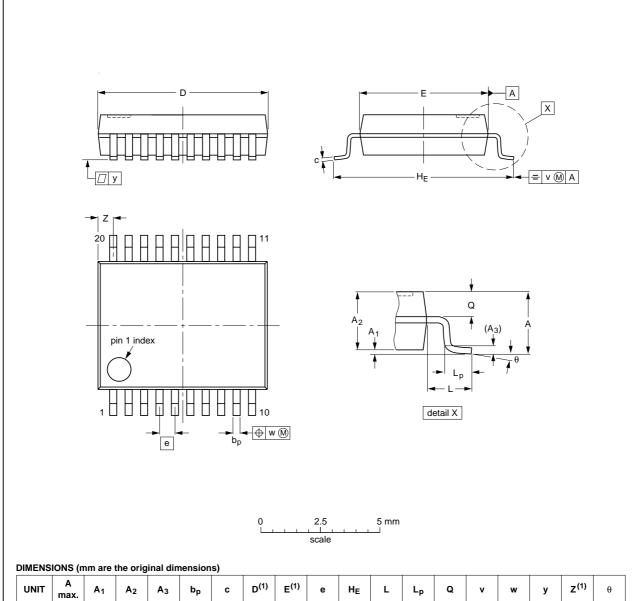
Fig 13. Package outline SOT163-1 (SO20)

0.089

74HC\_HCT573\_3



SOT339-1



 			3			-,												
UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

#### Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

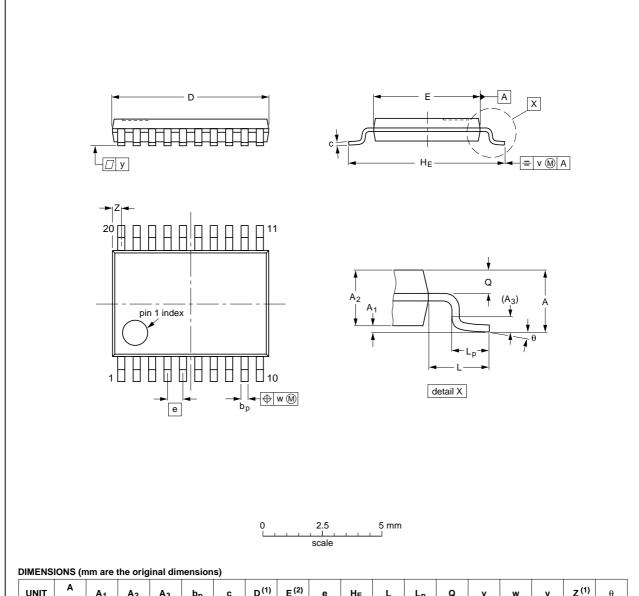
OUTLINE		REFER	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT339-1		MO-150			<del>99-12-27</del> 03-02-19

Fig 14. Package outline SOT339-1 (SSOP20)

74HC\_HCT573\_3

#### TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



_							٠-,												
	UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(2)</sup>	е	HE	L	Lp	Q	v	w	у	z <sup>(1)</sup>	θ
	mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE			REFER	EUROPEAN	ISSUE DATE		
	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
	SOT360-1		MO-153				<del>99-12-27</del> 03-02-19
			<u> </u>			·	

Fig 15. Package outline SOT360-1(TSSOP20)

74HC\_HCT573\_3

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm SOT764-1

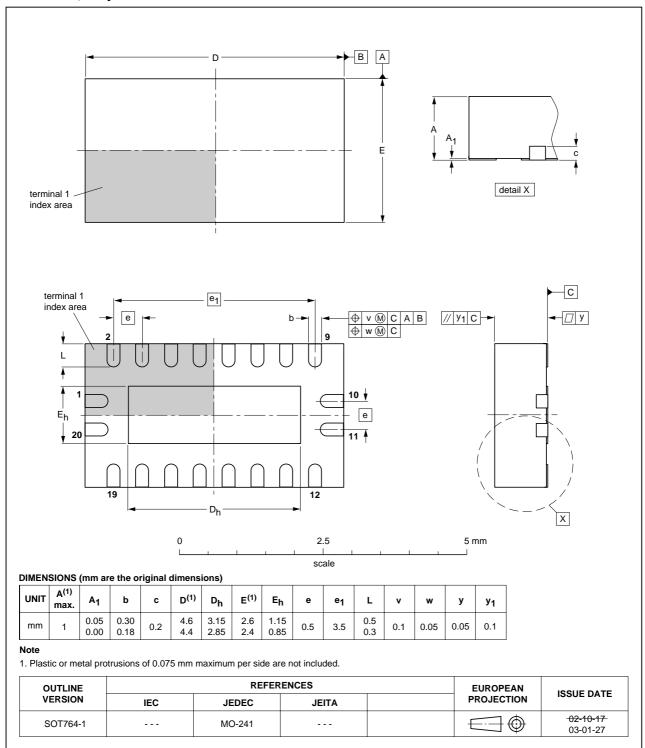


Fig 16. Package outline SOT764-1 (DHVQFN20)

74HC\_HCT573\_3



### 14. Abbreviations

#### Table 13: Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
НВМ	Human Body Model
TTL	Transistor-Transistor Logic
MM	Machine Model

# 15. Revision history

### Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes	
74HC_HCT573_3	20060117	Product data sheet	-	-	74HC_HCT573_CNV_2	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new prese information standard of Philips Semiconductors.</li> </ul>					
	<ul> <li>Added type</li> </ul>	e numbers 74HC573B	Q and 74HCT573	BQ (package Dl	HVQFN20)	
	<ul> <li>Added fam</li> </ul>	nily specification				
	<ul> <li>Added abb</li> </ul>	oreviations list				
74HC_HCT573_CNV_2	19901201	Product specification	-	-	-	



Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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### **Philips Semiconductors**

# 74HC573; 74HCT573

Octal D-type transparent latch; 3-state

### 21. Contents

1	General description
2	Features
3	Quick reference data
4	Ordering information
5	Functional diagram 3
6	Pinning information 5
6.1	Pinning
6.2	Pin description 5
7	Functional description 6
8	Limiting values 6
9	Recommended operating conditions 7
10	Static characteristics 8
11	Dynamic characteristics
12	Waveforms
13	Package outline 19
14	Abbreviations
15	Revision history 24
16	Data sheet status
17	Definitions
18	Disclaimers
19	Trademarks
20	Contact information



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