Texas Instruments

TLV320AIC23

Stereo Audio CODEC, 8- to 96-kHz, With Integrated Headphone Amplifier

Data Manual

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Digital Audio Products

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IMPORTANT NOTICE

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1 Introduction

The TLV320AIC23 is a high-performance stereo audio codec with highly integrated analog functionality. The analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) within the TLV320AIC23 use multibit sigma-delta technology with integrated oversampling digital interpolation filters. Data-transfer word lengths of 16, 20, 24, and 32 bits, with sample rates from 8 kHz to 96 kHz, are supported. The ADC sigma-delta modulator features third-order multibit architecture with up to 90-dBA signal-to-noise ratio (SNR) at audio sampling rates up to 96 kHz, enabling high-fidelity audio recording in a compact, power-saving design. The DAC sigma-delta modulator features a second-order multibit architecture with up to 100-dBA SNR at audio sampling rates up to 96 kHz, enabling high-quality digital audio-playback capability, while consuming less than 23 mW during playback only. The TLV320AIC23 is the ideal analog input/output (I/O) choice for portable digital audio-player and recorder applications, such as MP3 digital audio players.

Integrated analog features consist of stereo-line inputs with an analog bypass path, a stereo headphone amplifier, with analog volume control and mute, and a complete electret-microphone-capsule biasing and buffering solution. The headphone amplifier is capable of delivering 30 mW per channel into 32 Ω. The analog bypass path allows use of the stereo-line inputs and the headphone amplifier with analog volume control, while completely bypassing the codec, thus enabling further design flexibility, such as integrated FM tuners. A microphone bias-voltage output provides a low-noise current source for electret-capsule biasing. The AIC23 has an integrated adjustable microphone amplifier (gain adjustable from 1 to 5) and a programmable gain microphone amplifier (0 dB or 20 dB). The microphone signal can be mixed with the output signals if a sidetone is required.

While the TLV320AIC23 supports the industry-standard oversampling rates of 256 f_S and 384 f_S, unique oversampling rates of 250 f_S and 272 f_S are provided, which optimize interface considerations in designs using TI C54x digital signal processors (DSPs) and universal serial bus (USB) data interfaces. A single 12-MHz crystal can supply clocking to the DSP, USB, and codec. The TLV320AIC23 features an internal oscillator that, when connected to a 12-MHz external crystal, provides a system clock to the DSP and other peripherals at either 12 MHz or 6 MHz, using an internal clock buffer and selectable divider. Audio sample rates of 48 kHz and compact-disc (CD) standard 44.1 kHz are supported directly from a 12-MHz master clock with 250 f_S and 272 f_S oversampling rates.

Low power consumption and flexible power management allow selective shutdown of codec functions, thus extending battery life in portable applications. This design solution, coupled with the industry's smallest package, the TI proprietary MicroStar Junior™ using only 25 mm^2 of board area, makes powerful portable stereo audio designs easily realizable in a cost-effective, space-saving total analog I/O solution: the TLV320AIC23.

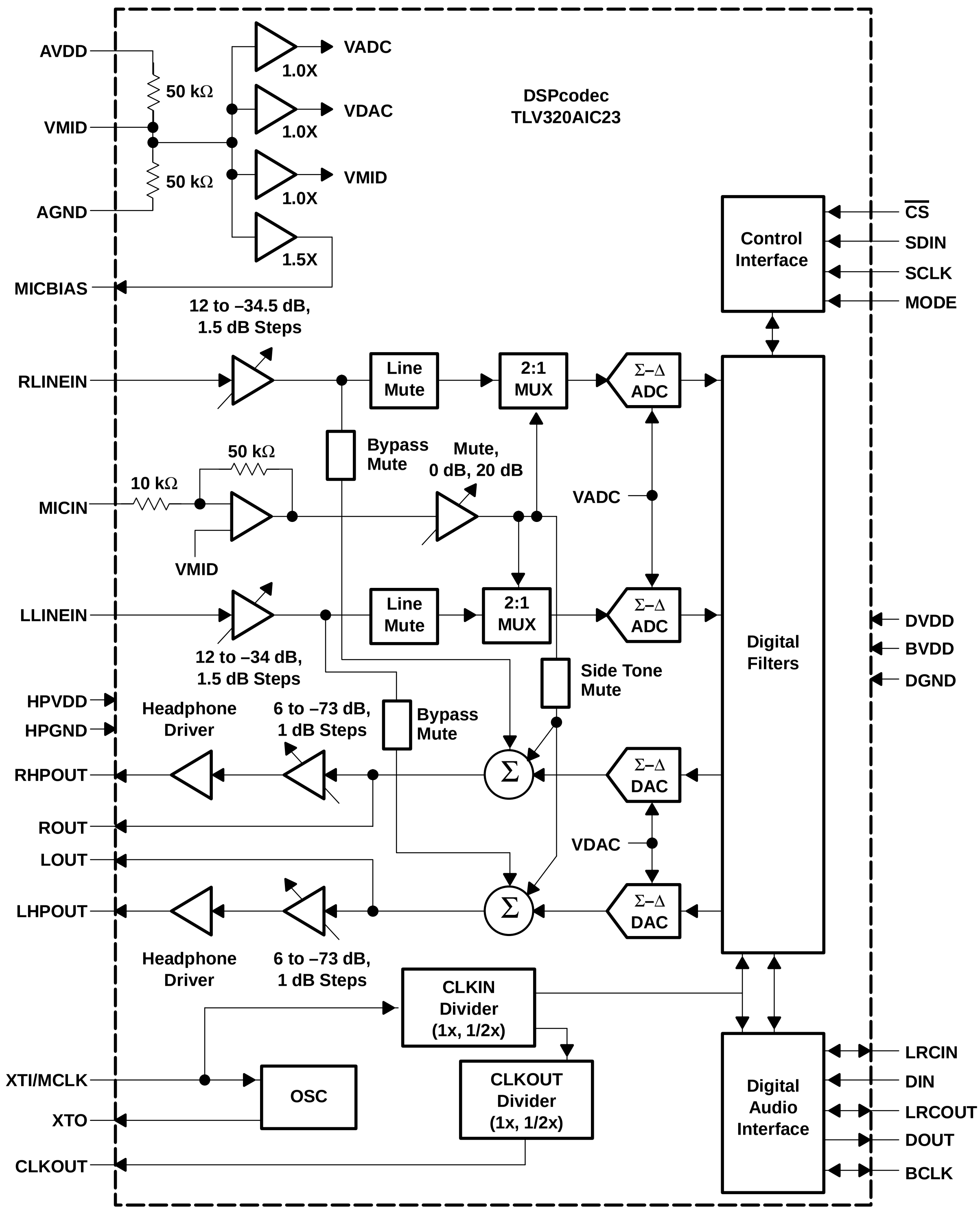
1.1 Features

- High-Performance Stereo *Codec*
  - 90-dB SNR Multibit Sigma-Delta ADC (A-weighted at 48 kHz)
  - 100-dB SNR Multibit Sigma-Delta DAC (A-weighted at 48 kHz)
  - 1.42 V – 3.6 V Core Digital Supply: Compatible With TI C54x DSP Core Voltages
  - 2.7 V – 3.6 V Buffer and Analog Supply: Compatible Both TI C54x DSP Buffer Voltages
  - 8-kHz – 96-kHz Sampling-Frequency Support
- Software Control Via TI McBSP-Compatible Multiprotocol Serial Port
  - I^2C-Compatible and SPI-Compatible Serial-Port Protocols
  - Glueless Interface to TI McBSPs
- Audio-Data Input/Output Via TI McBSP-Compatible Programmable Audio Interface
  - I^2S-Compatible Interface Requiring Only One McBSP for both ADC and DAC
  - Standard I^2S, MSB, or LSB Justified-Data Transfers
  - 16/20/24/32-Bit Word Lengths

MicroStar Junior is a trademark of Texas Instruments.

  - Audio Master/Slave Timing Capability Optimized for TI DSPs (250/272 f_S), USB mode
  - Industry-Standard Master/Slave Support Provided Also (256/384 f_S), Normal mode
  - Glueless Interface to TI McBSPs
- Integrated Total Electret-Microphone Biasing and Buffering Solution
  - Low-Noise MICBIAS pin at 3/4 AVDD for Biasing of Electret Capsules
  - Integrated Buffer Amplifier With Tunable Fixed Gain of 1 to 5
  - Additional Control-Register Selectable Buffer Gain of 0 dB or 20 dB
- Stereo-Line Inputs
  - Integrated Programmable Gain Amplifier
  - Analog Bypass Path of Codec
- ADC Multiplexed Input for Stereo-Line Inputs and Microphone
- Stereo-Line Outputs
  - Analog Stereo Mixer for DAC and Analog Bypass Path
- Analog Volume Control With Mute
- Highly Efficient Linear Headphone Amplifier
  - 30 mW into 32 Ω From a 3.3-V Analog Supply Voltage
- Flexible Power Management Under Total Software Control
  - 23-mW Power Consumption During Playback Mode
  - Standby Power Consumption <150 µW
  - Power-Down Power Consumption <15 µW
- Industry's Smallest Package: 32-Pin TI Proprietary MicroStar Junior™
  - 25 mm^2 Total Board Area
  - 28-Pin TSSOP Also Is Available (62 mm^2 Total Board Area)
- Ideally Suitable for Portable Solid-State Audio Players and Recorders

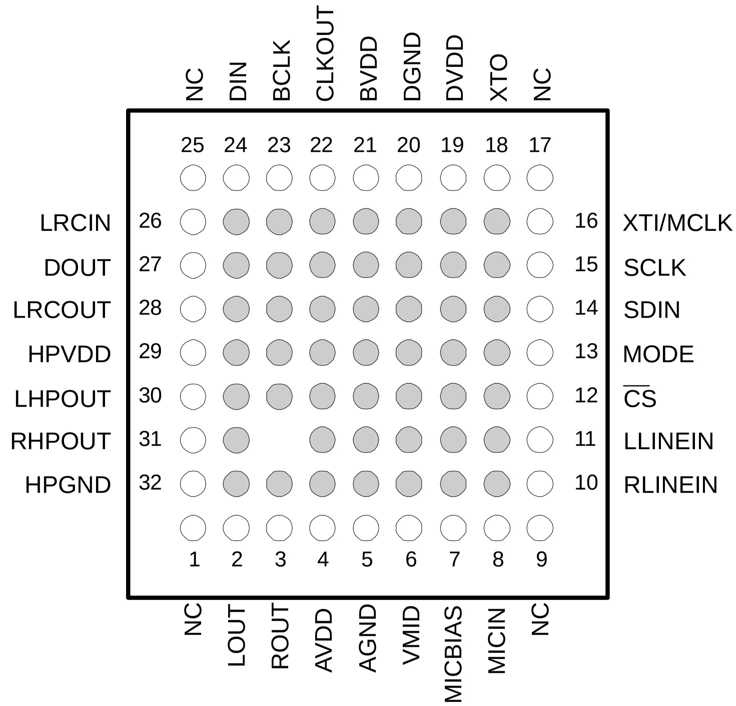
1.2 Functional Block Diagram



NOTE: MCLK, BCLK, and SCLK are all asynchronous to each other.

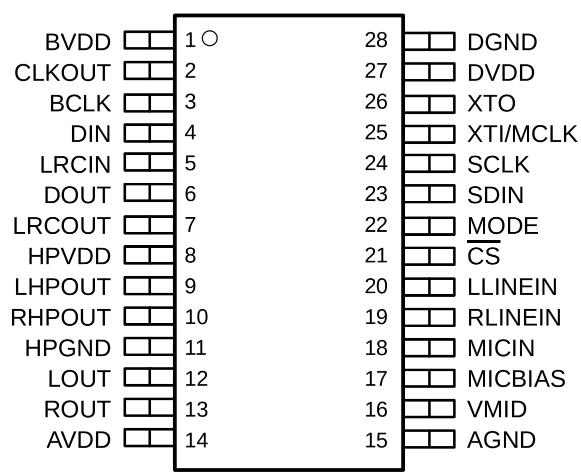
1.3 Terminal Assignments

GQE PACKAGE
(TOP VIEW)



NC – No internal connection

PW PACKAGE
(TOP VIEW)



1.4 Ordering Information

T_A	PACKAGE	
	32-Pin MicroStar Junior GQE	**28-Pin TSSOP PW**
–10°C to 70°C	TLV320AIC23GQE	TLV320AIC23PW
–40°C to 85°C	TLV320AIC23IGQE	TLV320AIC23IPW

1.5 Terminal Functions

TERMINAL				
NAME	NO.		I/O	DESCRIPTION
	GQE	PW		
AGND	5	15		Analog supply return
AVDD	4	14		Analog supply input. Voltage level is 3.3 V nominal.
BCLK	23	3	I/O	I^2S serial-bit clock. In audio master mode, the AIC23 generates this signal and sends it to the DSP. In audio slave mode, the signal is generated by the DSP.
BVDD	21	1		Buffer supply input. Voltage range is from 2.7 V to 3.6 V.
CLKOUT	22	2	O	Clock output. This is a buffered version of the XTI input and is available in 1X or 1/2X frequencies of XTI. Bit 07 in the sample rate control register controls frequency selection.
$\overline{CS}$	12	21	I	Control port input latch/address select. For SPI control mode this input acts as the data latch control. For I^2C control mode this input defines the seventh bit in the device address field. See Section 3.1 for details.
DIN	24	4	I	I^2S format serial data input to the sigma-delta stereo DAC
DGND	20	28		Digital supply return
DOUT	27	6	O	I^2S format serial data output from the sigma-delta stereo ADC
DVDD	19	27		Digital supply input. Voltage range is 3.3 V nominal.
HPGND	32	11		Analog headphone amplifier supply return
HPVDD	29	8		Analog headphone amplifier supply input. Voltage level is 3.3 V nominal.
LHPOUT	30	9	O	Left stereo mixer-channel amplified headphone output. Nominal 0-dB output level is 1 V_{RMS}. Gain of –73 dB to 6 dB is provided in 1-dB steps.
LLINEIN	11	20	I	Left stereo-line input channel. Nominal 0-dB input level is 1 V_{RMS}. Gain of –34.5 dB to 12 dB is provided in 1.5-dB steps.
LOUT	2	12	O	Left stereo mixer-channel line output. Nominal output level is 1.0 V_{RMS}.
LRCIN	26	5	I/O	I^2S DAC-word clock signal. In audio master mode, the AIC23 generates this framing signal and sends it to the DSP. In audio slave mode, the signal is generated by the DSP.
LRCOUT	28	7	I/O	I^2S ADC-word clock signal. In audio master mode, the AIC23 generates this framing signal and sends it to the DSP. In audio slave mode, the signal is generated by the DSP.
MICBIAS	7	17	O	Buffered low-noise-voltage output suitable for electret-microphone-capsule biasing. Voltage level is 3/4 AVDD nominal.
MICIN	8	18	I	Buffered amplifier input suitable for use with electret-microphone capsules. Without external resistors a default gain of 5 is provided. See Section 2.3.1.2 for details.
MODE	13	22	I	Serial-interface-mode input. See Section 3.1 for details.
NC	1, 9 17, 25			Not Used—No internal connection
RHPOUT	31	10	O	Right stereo mixer-channel amplified headphone output. Nominal 0-dB output level is 1 V_{RMS}. Gain of –73 dB to 6 dB is provided in 1-dB steps.
RLINEIN	10	19	I	Right stereo-line input channel. Nominal 0-dB input level is 1 V_{RMS}. Gain of –34.5 dB to 12 dB is provided in 1.5-dB steps.
ROUT	3	13	O	Right stereo mixer-channel line output. Nominal output level is 1.0 V_{RMS}.
SCLK	15	24	I	Control-port serial-data clock. For SPI and I^2C control modes this is the serial-clock input. See Section 3.1 for details.
SDIN	14	23	I	Control-port serial-data input. For SPI and I^2C control modes this is the serial-data input and also is used to select the control protocol after reset. See Section 3.1 for details.
VMID	6	16	I	Midrail voltage decoupling input. 10-µF and 0.1-µF capacitors should be connected in parallel to this terminal for noise filtering. Voltage level is 1/2 AVDD nominal.
XTI/MCLK	16	25	I	Crystal or external-clock input. Used for derivation of all internal clocks on the AIC23.
XTO	18	26	O	Crystal output. Connect to external crystal for applications where the AIC23 is the audio timing master. Not used in applications where external clock source is used.

2 Specifications

2.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range, AV_{DD} to AGND, DV_{DD} to DGND, BV_{DD} to DGND, HPV_{DD} to HPGND (see Note 1) . . . . . . –0.3 V to + 3.63 V
Analog supply return to digital supply return, AGND to DGND . . . . . . –0.3 V to + 3 .63 V
Input voltage range, all input signals: Digital . . . . . . –0.3 V to DV_{DD} + 0.3 V
Analog . . . . . . –0.3 V to AV_{DD} + 0.3 V
Case temperature for 10 seconds . . . . . . 240°C
Operating free-air temperature range, T_A . . . . . . –10°C to 70°C
Storage temperature range, T_{stg} . . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: DV_{DD} may not exceed BV_{DD} + 0.3V; BV_{DD} may not exceed AV_{DD} + 0.3V or HPV_{DD} + 0.3.

2.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD}, HPV_{DD} (see Note 2)	2.7	3.3	3.6	V
Digital buffer supply voltage, BV_{DD} (see Note 2)	2.7	3.3	3.6	V
Digital core supply voltage, DV_{DD} (see Note 2)	1.42	1.5	3.6	V
Analog input voltage, full scale – 0dB (AV_{DD} = 3.3 V)		1		V_{RMS}
Stereo-line output load resistance	10			kΩ
Headphone-amplifier output load resistance	0			Ω
CLKOUT digital output load capacitance		20		pF
All other digital output load capacitance		10		pF
Stereo-line output load capacitance		50		pF
XTI master clock Input			18.43	MHz
ADC or DAC conversion rate			96	kHz
Operating free-air temperature, T_A	–10		70	°C

NOTE 2: Digital voltage values are with respect to DGND; analog voltage values are with respect to AGND.

2.3 Electrical Characteristics Over Recommended Operating Conditions, AV_{DD}, HPV_{DD}, BV_{DD} = 3.3 V, DV_{DD} = 1.5 V, Slave Mode, XTI/MCLK = 256fs, f_S = 48 kHz (unless otherwise stated)

2.3.1 ADC

2.3.1.1 Line Input to ADC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input signal level (0 dB)			1		V_{RMS}
Signal-to-noise ratio, A-weighted, 0-dB gain (see Notes 3 and 4)	f_S = 48 kHz (3.3 V)	85	90		dB
	f_S = 48 kHz (2.7 V)		90		
Dynamic range, A-weighted, –60-dB full-scale input (see Note 4)	AV_{DD} = 3.3 V	85	90		dB
	AV_{DD} = 2.7 V		90		
Total harmonic distortion, –1-dB input, 0-dB gain	AV_{DD} = 3.3 V		–80		dB
	AV_{DD} = 2.7 V		80		
Power supply rejection ratio	1 kHz, 100 mV_{pp}		50		dB
ADC channel separation	1 kHz input tone		90		dB
Programmable gain	1 kHz input tone, R_{SOURCE} < 50 Ω	–34.5		12	dB
Programmable gain step size	Monotonic		1.5		dB
Mute attenuation	0 dB, 1 kHz input tone		80		dB
Input resistance	12 dB Input gain	10		20	kΩ
	0 dB input gain	30	35		
Input capacitance			10		pF

NOTES: 3. Ratio of output level with 1-kHz full-scale input, to the output level with the input short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

4. All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter results in higher THD + N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

2.3.1.2 Microphone Input to ADC, 0-dB Gain, f_S = 8 kHz (40-KΩ Source Impedance, see Section 1.2, *Functional Block Diagram*)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input signal level (0 dB)			1.0		V_{RMS}
Signal-to-noise ratio, A-weighted, 0-dB gain (see Notes 3 and 4)	AV_{DD} = 3.3 V	80	85		dB
	AV_{DD} = 2.7 V		84		
Dynamic range, A-weighted, –60-dB full-scale input (see Note 4)	AV_{DD} = 3.3 V	80	85		dB
	AV_{DD} = 2.7 V		84		
Total harmonic distortion, –1-dB input, 0-dB gain	AV_{DD} = 3.3 V		–60		dB
	AV_{DD} = 2.7 V		–60		
Power supply rejection ratio	1 kHz, 100 mV_{pp}		50		dB
Programmable gain boost	1 kHz input tone, R_{SOURCE} < 50 Ω		20		dB
Microphone-path gain	MICBOOST = 0, R_{SOURCE} < 50 Ω		14		dB
Mute attenuation	0 dB, 1 kHz input tone	60	80		dB
Input resistance		8	14		kΩ
Input capacitance			10		pF

NOTES: 3. Ratio of output level with 1-kHz full-scale input, to the output level with the input short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

4. All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter results in higher THD + N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

2.3.1.3 Microphone Bias

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Bias voltage		3/4 AVDD – 100 m	3/4 AVDD	3/4 AVDD + 100 m	V
Bias-current source				3	mA
Output noise voltage	1 kHz to 20 kHz		25		$nV/\sqrt{Hz}$

2.3.2 DAC

2.3.2.1 Line Output, Load = 10 kΩ, 50 pF

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
0-dB full-scale output voltage (FFFFFF)				1.0		V_{RMS}
Signal-to-noise ratio, A-weighted, 0-dB gain (see Notes 3, 4, and 5)	AV_{DD} = 3.3 V	f_S = 48kHz	90	100		dB
	AV_{DD} = 2.7 V	f_S = 48 kHz		100		
Dynamic range, A-weighted (see Note 4)	AV_{DD} = 3.3 V		85	90		dB
	AV_{DD} = 2.7 V			TBD		
Total harmonic distortion	AV_{DD} = 3.3 V	1 kHz, 0 dB		–88	–80	dB
		1 kHz, –3 dB		–92	–86	
	AV_{DD} = 2.7 V	1 kHz, 0 dB		–85		dB
		1 kHz, –3 dB		–88		
Power supply rejection ratio	1 kHz, 100 mV_{pp}			50		dB
DAC channel separation				100		dB

NOTES: 3. Ratio of output level with 1-kHz full-scale input, to the output level with the input short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
4. All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter results in higher THD + N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
5. Ratio of output level with 1-kHz full-scale input, to the output level with all zeros into the digital input, measured A-weighted over a 20-Hz to 20-kHz bandwidth.

2.3.3 Analog Line Input to Line Output (Bypass)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
0-dB full-scale output voltage				1.0		V_{RMS}
Signal-to-noise ratio, A-weighted, 0-dB gain (see Notes 3 and 4)	AV_{DD} = 3.3 V		90	95		dB
	AV_{DD} = 2.7 V			95		
Total harmonic distortion	AV_{DD} = 3.3 V	1 kHz, 0 dB		–86	–80	dB
		1 kHz, –3 dB		–92	–86	
	AV_{DD} = 2.7 V	1 kHz, 0 dB		–86		dB
		1 kHz, –3 dB		–92		
Power supply rejection ratio	1 kHz, 100 mV_{pp}			50		dB
DAC channel separation (left to right)	1 kHz, 0 dB			80		dB

NOTES: 3. Ratio of output level with 1-kHz full-scale input, to the output level with the input short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
4. All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter results in higher THD + N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

2.3.4 Stereo Headphone Output

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
0-dB full-scale output voltage				1.0		V_{RMS}
Maximum output power, P_O	R_L = 32 Ω			30		mW
	R_L = 16 Ω			40		
Signal-to-noise ratio, A-weighted (see Note 4)	AV_{DD} = 3.3 V		90	97		dB
Total harmonic distortion	AV_{DD} = 3.3 V, 1 kHz output	P_O = 10 mW			0.1	%
		P_O = 20 mW			1.0	
Power supply rejection ratio	1 kHz, 100 mV_{pp}			50		dB
Programmable gain	1 kHz output		–73		6	dB
Programmable-gain step size					1	dB
Mute attenuation	1 kHz output			80		dB

NOTE 4: All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter results in higher THD + N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

2.3.5 Analog Reference Levels

PARAMETER	MIN	TYP	MAX	UNIT
Reference voltage	AVDD/2 – 50 mV		AVDD/2 + 50 mV	V
Divider resistance	40	50	60	kΩ

2.3.6 Digital I/O

PARAMETER		MIN	TYP	MAX	UNIT
V_{IL}	Input low level			$0.3 \times BV_{DD}$	V
V_{IH}	Input high level	$0.7 \times BV_{DD}$			V
V_{OL}	Output low level			$0.1 \times BV_{DD}$	V
V_{OH}	Output high level	$0.9 \times BV_{DD}$			V

2.3.7 Supply Current

PARAMETER				MIN	TYP	MAX	UNIT
I_{TOT}	Total supply current, No input signal	Record and playback (all active)			23		mA
		Record and playback (osc, clk, and MIC output powered down)			18		
		Line playback only			7		
		Record only			13		
		Analog bypass (line in to line out)			4		
		Power down	Oscillator enabled		1.5		
			Oscillator disabled		0.01		

2.4 Digital-Interface Timing

PARAMETER			MIN	TYP	MAX	UNIT
$t_{w(1)}$	System-clock pulse duration, MCLK/XTI	High	18			ns
$t_{w(2)}$	System-clock pulse duration, MCLK/XTI	Low	18			ns
$t_{c(1)}$	System-clock period, MCLK/XTI		54			ns
	Duty cycle, MCLK/XTI		40/60%		60/40%	
$t_{pd(1)}$	Propagation delay, CLKOUT		0		10	ns

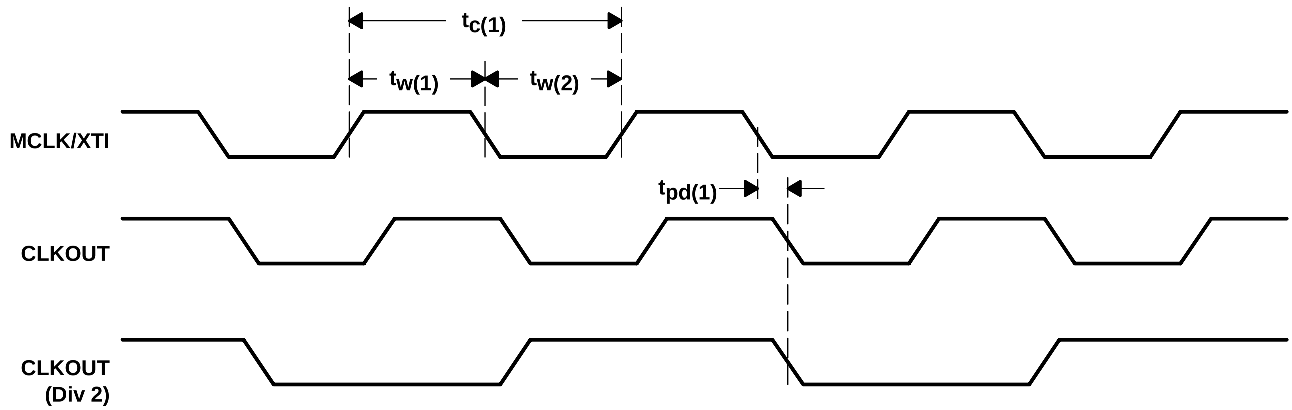


Figure 2–1. System-Clock Timing Requirements

2.4.1 Audio Interface (Master Mode)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{pd(2)}$	Propagation delay, LRCIN/LRCOUT	0		10	ns
$t_{pd(3)}$	Propagation delay, DOUT	0		10	ns
$t_{su(1)}$	Setup time, DIN	10			ns
$t_{h(1)}$	Hold time, DIN	10			ns

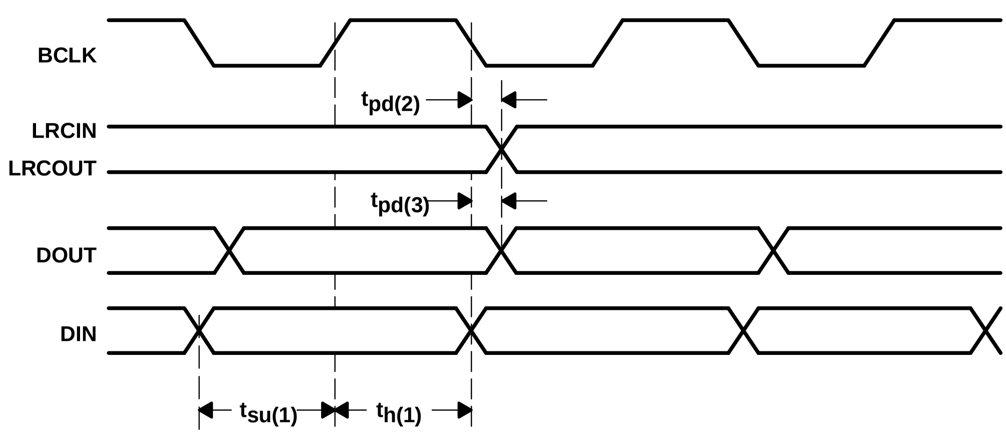


Figure 2–2. Master-Mode Timing Requirements

2.4.2 Audio Interface (Slave-Mode)

PARAMETER			MIN	TYP	MAX	UNIT
$t_{w(3)}$	Pulse duration, BCLK	High	20			ns
$t_{w(4)}$		Low	20			
$t_{c(2)}$	Clock period, BCLK		50			ns
$t_{pd(4)}$	Propagation delay, DOUT		0		10	ns
$t_{su(2)}$	Setup time, DIN		10			ns
$t_{h(2)}$	Hold time, DIN		10			ns
$t_{su(3)}$	Setup time, LRCIN		10			ns
$t_{h(3)}$	Hold time, LRCIN		10			ns

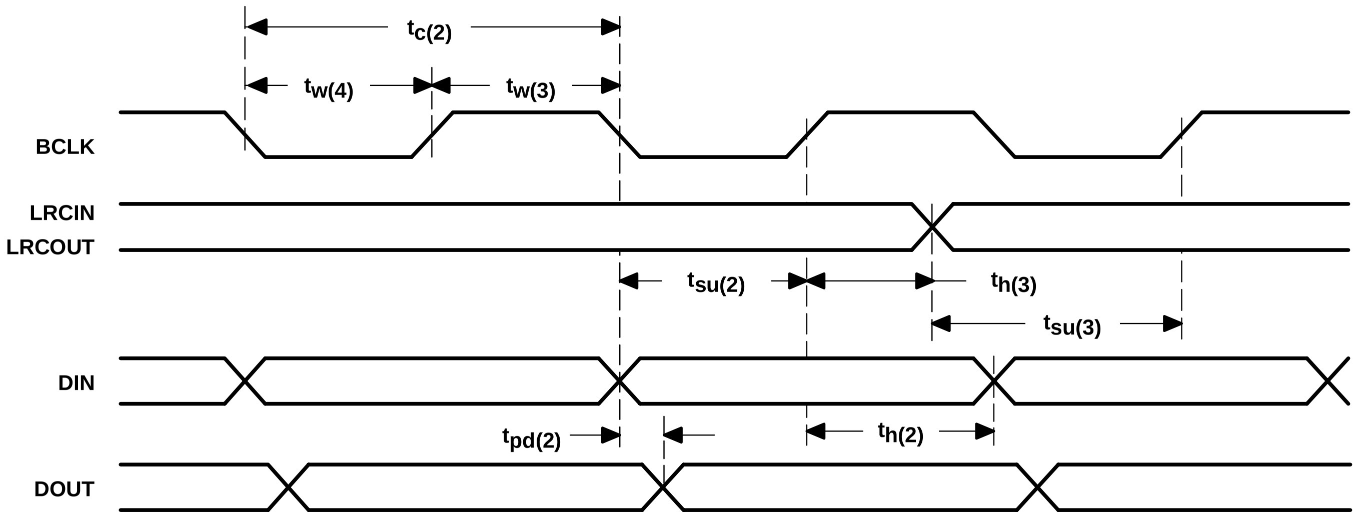


Figure 2–3. Slave-Mode Timing Requirements

2.4.3 Three-Wire Control Interface (SDIN)

PARAMETER			MIN	TYP	MAX	UNIT
$t_{w(5)}$	Clock pulse duration, SCLK	High	20			ns
$t_{w(6)}$		Low	20			
$t_{c(3)}$	Clock period, SCLK		80			ns
$t_{su(4)}$	Clock rising edge to $\overline{\text{CS}}$ rising edge, SCLK		60			ns
$t_{su(5)}$	Setup time, SDIN to SCLK		20			ns
$t_{h(4)}$	Hold time, SCLK to SDIN		20			ns
$t_{w(7)}$	Pulse duration, $\overline{\text{CS}}$	High	20			ns
$t_{w(8)}$		Low	20			

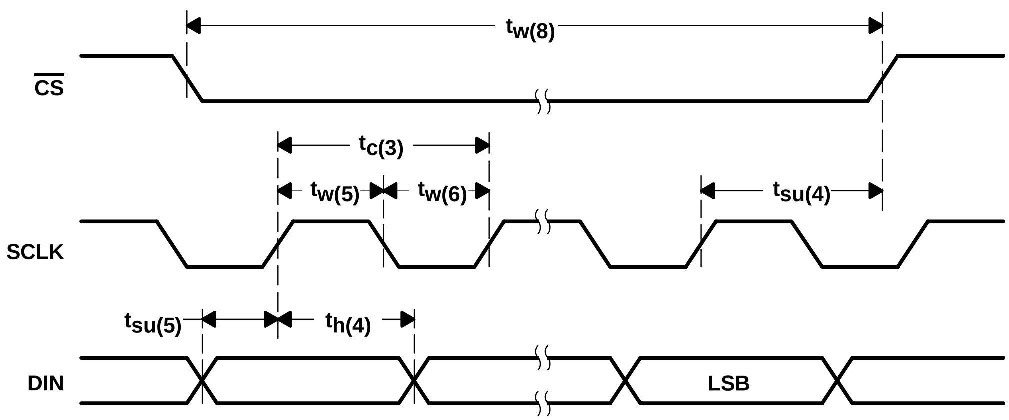


Figure 2–4. Three-Wire Control Interface Timing Requirements

2.4.4 Two-Wire Control Interface (I2C)

PARAMETER			MIN	TYP	MAX	UNIT
$t_{w(9)}$	Clock pulse duration, SCLK	High	1.3			µs
$t_{w(10)}$		Low	600			ns
f(sf)	Clock frequency, SCLK		0		400	kHz
$t_{h(5)}$	Hold time (start condition)		600			ns
$t_{su(6)}$	Setup time (start condition)		600			ns
$t_{h(6)}$	Data hold time				900	ns
$t_{su(7)}$	Data setup time		100			ns
t_r	Rise time, SDIN, SCLK				300	ns
t_f	Fall time, SDIN, SCLK				300	ns
$t_{su(8)}$	Setup time (stop condition)		600			ns

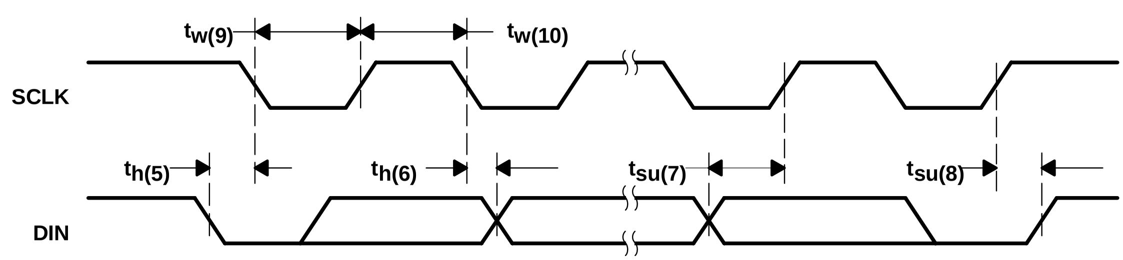


Figure 2–5. Two-Wire Control Interface Timing Requirements

3 How to Use the TLV320AIC23

3.1 Control Interfaces

The TLV320AIC23 has many programmable features. The control interface is used to program the registers of the device. The control interface complies with SPI (three-wire operation) and I^2C (two-wire operation) specifications. The state of the MODE terminal selects the control interface type. The MODE pin must be hardwired to the required level.

MODE	INTERFACE
0	I^2C
1	SPI

3.1.1 SPI

In SPI mode, SDIN carries the serial data, SCLK is the serial clock and $\overline{CS}$ latches the data word into the TLV320AIC23. The interface is compatible with microcontrollers and DSPs with an SPI interface.

A control word consists of 16 bits, starting with the MSB. The data bits are latched on the rising edge of SCLK. A rising edge on $\overline{CS}$ after the 16th rising clock edge latches the data word into the AIC (see Figure 3-1).

The control word is divided into two parts. The first part is the address block, the second part is the data block:

B[15:9] Control Address Bits
B[8:0] Control Data Bits

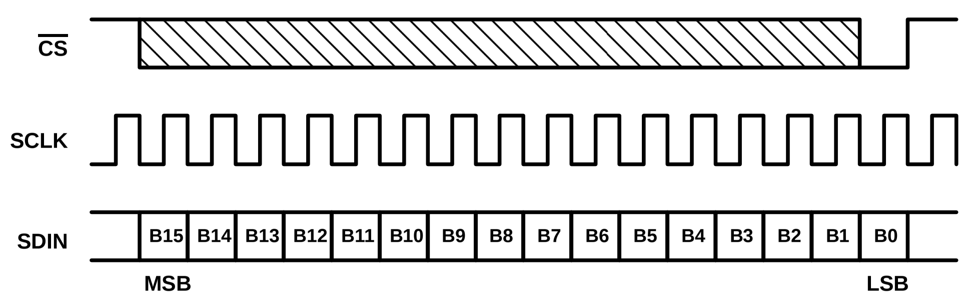


Figure 3–1. SPI Timing

3.1.2 I^2C

In I^2C mode, the data transfer uses SDIN for the serial data and SCLK for the serial clock. The start condition is a falling edge on SDIN while SCLK is high. The seven bits following the start condition determine which device on the I^2C bus receives the data. R/W determines the direction of the data transfer. The TLV320AIC23 is a write only device and responds only if R/W is 0. The device operates only as a slave device whose address is selected by setting the state of the CS pin as follows.

$\overline{CS}$ STATE (Default = 0)	ADDRESS
0	0011010
1	0011011

The device that recognizes the address responds by pulling SDIN low during the ninth clock cycle, acknowledging the data transfer. The control follows in the next two eight-bit blocks. The stop condition after the data transfer is a rising edge on SDIN when SCLK is high (see Figure 3-2).

The 16-bit control word is divided into two parts. The first part is the address block, the second part is the data block:

B[15:9] Control Address Bits
B[8:0] Control Data Bits

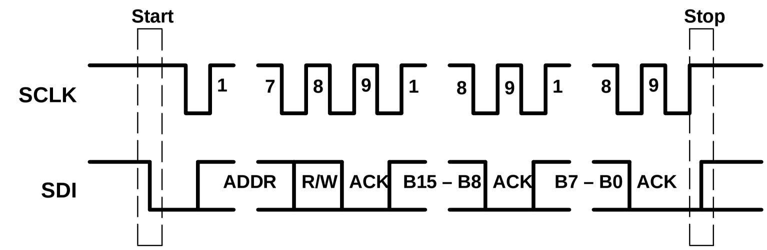


Figure 3–2. 2-Wire I²C Compatible Timing

3.1.3 Register Map

The TLV320AIC23 has the following set of registers, which are used to program the modes of operation.

ADDRESS	REGISTER
0000000	Left line input channel volume control
0000001	Right line input channel volume control
0000010	Left channel headphone volume control
0000011	Right channel headphone volume control
0000100	Analog audio path control
0000101	Digital audio path control
0000110	Power down control
0000111	Digital audio interface format
0001000	Sample rate control
0001001	Digital interface activation
0001111	Reset register

Left line input channel volume control (Address: 0000000)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	LRS	LIM	X	X	LIV4	LIV3	LIV2	LIV1	LIV0
Default	0	1	0	0	1	0	1	1	1

LRS Left/right line simultaneous volume/mute update
Simultaneous update 0 = Disabled 1 = Enabled
LIM Left line input mute 0 = Normal 1 = Muted
LIV[4:0] Left line input volume control (10111 = 0 dB default)
11111 = +12 dB down to 00000 = –34.5 dB in 1.5-dB steps
X Reserved

Right Line Input Channel Volume Control (Address: 0000001)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	RLS	RIM	X	X	RIV4	RIV3	RIV2	RIV1	RIV0
Default	0	1	0	0	1	0	1	1	1

RLS	Right/left line simultaneous volume/mute update		
	Simultaneous update	0 = Disabled	1 = Enabled
RIM	Right line input mute	0 = Normal	1 = Muted
RIV[4:0]	Right line input volume control (10111 = 0 dB default)		
	11111 = +12 dB down to 00000 = –34.5 dB in 1.5-dB steps		
X	Reserved		

Left Channel Headphone Volume Control (Address: 0000010)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	LRS	LZC	LHV6	LHV5	LHV4	LHV3	LHV2	LHV1	LHV0
Default	0	1	1	1	1	1	0	0	1

LRS	Left/right headphone channel simultaneous volume/mute update		
	Simultaneous update	0 = Disabled	1 = Enabled
LZC	Left-channel zero-cross detect		
	Zero-cross detect	0 = Off	1 = On
LHV[6:0]	Left Headphone volume control (1111001 = 0 dB default)		
	1111111 = +6 dB down to 0000000 = –73 dB in 1-dB steps		

Right Channel Headphone Volume Control (Address: 0000011)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	RLS	RZC	RHV6	RHV5	RHV4	RHV3	RHV2	RHV1	RHV0
Default	0	1	1	1	1	1	0	0	1

RLS	Right/left headphone channel simultaneous volume/mute Update		
	Simultaneous update	0 = Disabled	1 = Enabled
RZC	Right-channel zero-cross detect		
	Zero-cross detect	0 = Off	1 = On
RHV[6:0]	Right headphone volume control (1111001 = 0 dB default)		
	1111111 = +6 dB down to 0000000 = –73 dB in 1-dB steps		

Analog Audio Path Control (Address: 0000100)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	STA1	STA0	STE	DAC	BYP	INSEL	MICM	MICB
Default	0	0	0	0	1	0	0	1	0

STA[1:0]	Sidetone attenuation	00 = –6 dB	01 = –9 dB	10 = –12 dB	11 = –15 dB
STE	Sidetone enable	0 = Disabled	1 = Enabled		
DAC	DAC select	0 = DAC off	1 = DAC selected		
BYP	Bypass	0 = Disabled	1 = Enabled		
INSEL	Input select for ADC	0 = Line	1 = Microphone		
MICM	Microphone mute	0 = Normal	1 = Muted		
MICB	Microphone boost	0=OdB	1 = 20dB		
X	Reserved				

Digital Audio Path Control (Address: 0000101)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	X	DACM	DEEMP1	DEEMP0	ADCHP
Default	0	0	0	0	0	0	1	0	0

DACM	DAC soft mute	0 = Disabled	1 = Enabled		
DEEMP[1:0]	De-emphasis control	00 = Disabled	01 = 32 kHz	10 = 44.1 kHz	11 = 48 kHz
ADCHP	ADC high-pass filter	0 = Disabled	1 = Enabled		
X	Reserved				

Power Down Control (Address: 0000110)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	OFF	CLK	OSC	OUT	DAC	ADC	MIC	LINE
Default	1	0	0	0	0	0	1	1	1

OFF	Device power	0 = On	1 = Off
CLK	Clock	0 = On	1 = Off
OSC	Oscillator	0 = On	1 = Off
OUT	Outputs	0 = On	1 = Off
DAC	DAC	0 = On	1 = Off
ADC	ADC	0 = On	1 = Off
MIC	Microphone input	0 = On	1 = Off
LINE	Line input	0 = On	1 = Off
X	Reserved		

Digital Audio Interface Format (Address: 0000111)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	MS	LRSWAP	LRP	IWL1	IWL0	FOR1	FOR0
Default	0	0	0	0	0	0	0	0	1

MS	Master/slave mode	0 = Slave 1 = Master
LRSWAP	DAC left/right swap	0 = Disabled 1 = Enabled
LRP	DAC left/right phase	0 = Right channel on, LRCIN high 1 = Right channel on, LRCIN low DSP mode 1 = MSB is available on 2nd BCLK rising edge after LRCIN rising edge 0 = MSB is available on 1st BCLK rising edge after LRCIN rising edge
IWL[1:0]	Input bit length	00 = 16 bit 01 = 20 bit 10 = 24 bit 11 = 32 bit
FOR[1:0]	Data format	11 = DSP format, frame sync followed by two data words 10 = I^2S format, MSB first, left – 1 aligned 01 = MSB first, left aligned 00 = MSB first, right aligned
X	Reserved	

NOTES: 1. In Master mode, the TLV320AIC23 supplies the BCLK, LRCOUT, and LRCIN. In Slave mode, BCLK, LRCOUT, and LRCIN are supplied to the TLV320AIC23.

2. In master mode, BCLK = MCLK/4 for all sample rates except for 88.2 kHz and 96 kHz. For 88.2 kHz and 96 kHz sample rate, BCLK = MCLK.

Sample Rate Control (Address: 0001000)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	CLKOUT	CLKIN	SR3	SR2	SR1	SR0	BOSR	USB/Normal
Default	0	0	0	1	0	0	0	0	0

CLKIN	Clock input divider	0 = MCLK	1 = MCLK/2
CLKOUT	Clock output divider	0 = MCLK	1 = MCLK/2

SR[3:0]	Sampling rate control (see Sections 3.3.2.1 AND 3.3.2.2)		
BOSR	Base oversampling rate		
	USB mode:	0 = 250 f_S	1 = 272 f_S
	Normal mode:	0 = 256 f_S	1 = 384 f_S
USB/Normal	Clock mode select:	0 = Normal	1 = USB
X	Reserved		

Digital Interface Activation (Address: 0001001)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	X	X	X	X	ACT
Default	0	0	0	0	0	0	0	0	1

ACT	Activate interface	0 = Inactive	1 = Active
X	Reserved		

Reset Register (Address: 0001111)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	RES	RES	RES	RES	RES	RES	RES	RES	RES
Default	0	0	0	0	0	0	0	0	0

RES   Write 000000000 to this register triggers reset

3.2 Analog Interface

3.2.1 Line Inputs

The TLV320AIC23 has line inputs for the left and the right audio channels (RLINEIN and LLINEIN). Both line inputs have independently programmable volume controls and mutes. Active and passive filters for the two channels prevent high frequencies from folding back into the audio band.

The line-input gain is logarithmically adjustable from 12 dB to –34.5 dB in 1.5-dB steps. The ADC full-scale range is 1.0 V_{RMS} at AV_{DD} = 3.3 V. The full-scale range tracks linearly with analog supply voltage AV_{DD}. To avoid distortions, it is important not to exceed the full-scale range.

The gain is independently programmable on both left and right line-inputs. To reduce the number of software write cycles required. Both channels can be locked to the same value by setting the RLS and LRS bits (see Section 3.1.3).

The line inputs are biased internally to VMID. When the line inputs are muted or the device is set to standby mode, the line inputs are kept biased to VMID using special antithump circuitry. This reduces audible clicks that otherwise might be heard when reactivating the inputs.

For interfacing to a CD system, the line input should be scaled to 1 V_{RMS} to avoid clipping, using the circuit shown in Figure 3-3.

Where:

R1 = 5 kΩ
R2 = 5 kΩ
C1 = 47 pF
C2 = 470 nF

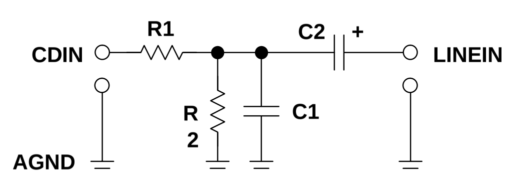


Figure 3–3. Analog Line Input Circuit

R1 and R2 divide the input signal by two, reducing the 2 V_{RMS} from the CD player to the nominal 1 V_{RMS} of the AIC23 inputs. C1 filters high-frequency noise, and C2 removes any dc component from the signal.

3.2.2 Microphone Input

MICIN is a high-impedance, low-capacitance input that is compatible with a wide range of microphones. It has a programmable volume control and a mute function. Active and passive filters prevent high frequencies from folding back into the audio band.

The MICIN signal path has two gain stages. The first stage has a nominal gain of G1 = 50 k/10 k = 5. By adding an external resistor (R_{MIC}) in series with MICIN, the gain of the first stage can be adjusted by G1 = 50 k/(10 k + R_{MIC}). For example, R_{MIC} = 40 k gives a gain of 0 dB. The second stage has a software programmable gain of 0 dB or 20 dB (see Section 3.1.3).

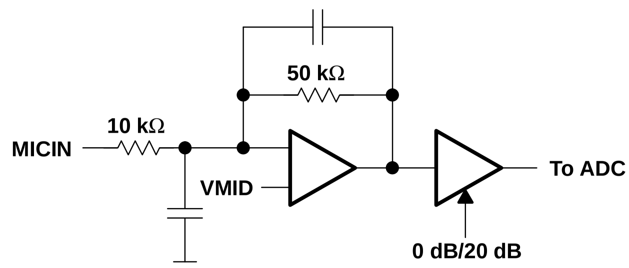


Figure 3–4. Microphone Input Circuit

The microphone input is biased internally to VMID. When the line inputs are muted, the MICIN input is kept biased to VMID using special antithump circuitry. This reduces audible clicks that may otherwise be heard when reactivating the input.

The MICBIAS output provides a low-noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. The maximum source current capability is 3 mA. This limits the smallest value of external biasing resistors that safely can be used.

The MICBIAS output is not active in standby mode.

3.2.3 Line Outputs

The TLV320AIC23 has two low-impedance line outputs (LLINEOUT and RLINEOUT) capable of driving line loads with 10-kΩ and 50-pF impedances.

The DAC full-scale output voltage is 1.0 V_{RMS} at AV_{DD} = 3.3 V. The full-scale range tracks linearly with the analog supply voltage $AV_{DD.}$ The DAC is connected to the line outputs via a low-pass filter that removes out-of-band components. No further external filtering is required in most applications.

The DAC outputs, line inputs, and the microphone signal are summed into the line outputs. These sources can be switched off independently. For example, in bypass mode, the line inputs are routed to the line outputs, bypassing the ADC and the DAC. If sidetone is enabled, the microphone signal is routed to both line outputs via a four-step programmable attenuation circuit.

The line outputs are muted by either muting the DAC (analog) or soft muting (digital) and disabling the bypass and sidetone paths (see Section 3.1.3).

3.2.4 Headphone Output

The TLV320AIC23 has stereo headphone outputs (LHPOUT and RHPOUT), and is designed to drive 16-Ω or 32-Ω headphones. The headphone output includes a high-quality volume control and mute function.

The headphone volume is logarithmically adjustable from 6 dB to –73 dB in 1-dB steps. Writing 000000 to the volume-control registers (see Section 3.1.3) mutes the headphone output. When the headphone output is muted or the device is placed in standby mode, the dc voltage is maintained at the outputs to prevent audible clicks.

A zero-cross detection circuit is provided under the control of the LZC and RZC bits. If this circuit is enabled, the volume-control values are updated only when the input signal to the gain stage is close to the analog ground level. This minimizes audible clicks as the volume is changed or the device is muted. This circuit has no time-out, so, if only dc levels are being applied to the gain stage input of more than 20 mV, the gain is not updated.

The gain is independently programmable on the left and right channels. Both channels can be locked to the same value by setting the RLS and LRS bits (see Section 3.1.3).

3.2.5 Analog Bypass Mode

The TLV320AIC23 includes a bypass mode in which the analog line inputs are directly routed to the analog line outputs, bypassing the ADC and DAC. This is enabled by selecting the bypass bit in the analog audio path control register[see Section 3.1.3).

For a true bypass mode, the output from the DAC and the sidetone should be disabled. The line input and headphone output volume controls and mutes are still operational in bypass mode. Therefore the line inputs, DAC output, and microphone input can be summed together. The maximum signal at any point in the bypass path must be no greater than $1.0V_{rms}$ at AV_{DD}=3.3V to avoid clipping and distortion. This amplitude tracks linearly with AV_{DD}.

3.2.6 Sidetone Insertion

The TLV320AIC23 has a sidetone insertion made where the microphone input is routed to the line and headphone outputs. This is useful for telephony and headset applications. The attenuation of the sidetone signal may be set to –6 dB, –9 dB, –12 dB, or –1 dB, by software selection (see Section 3.1.3). If this mode is used to sum the microphone input with the DAC output and line inputs, care must be taken not to exceed signal level to avoid clipping and distortion.

3.3 Digital Audio Interface

3.3.1 Digital Audio-Interface Modes

The TLV320AIC23 supports four audio-interface modes.

- Right justified
- Left justified
- I^2S mode
- DSP mode

The four modes are MSB first and operate with a variable word width between 16 to 32 bits (except right-justified mode, which does not support 32 bits).

The digital audio interface consists of clock signal BCLK, data signals DIN and DOUT, and synchronization signals LRCIN and LRCOUT. BCLK is an output in master mode and an input in slave mode.

3.3.1.1 Right-Justified Mode

In right-justified mode, the LSB is available on the rising edge of BCLK, preceding a falling edge on LRCIN or LRCOUT (see Figure 3-5).

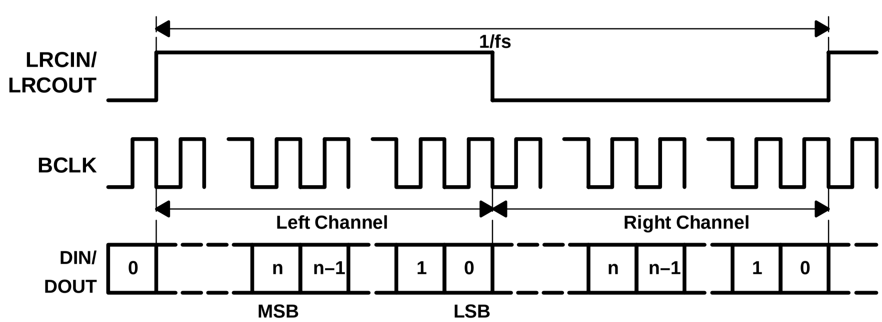


Figure 3–5. Right-Justified Mode Timing

3.3.1.2 Left-Justified Mode

In left-justified mode, the MSB is available on the rising edge of BCLK, following a rising edge on LRCIN or LRCOUT (see Figure 3-6)

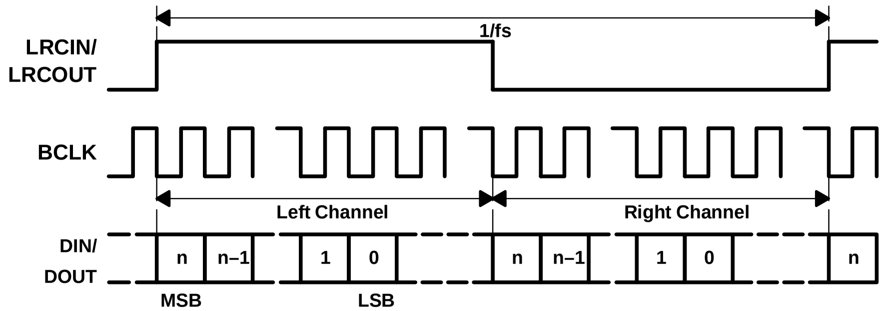


Figure 3–6. Left-Justified Mode Timing

3.3.1.3 I²S Mode

In I²S mode, the MSB is available on the second rising edge of BCLK, after the falling edge on LRCIN or LRCOUT (see Figure 3-7).

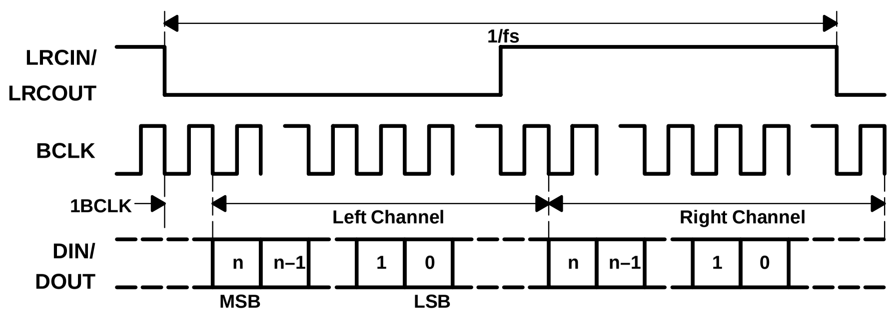


Figure 3–7. I²S Mode Timing

3.3.1.4 DSP Mode

The DSP mode is compatible with the McBSP ports of TI DSPs. LRCIN and LRCOUT must be connected to the Frame Sync signal of the McBSP. A falling edge on LRCIN or LRCOUT starts the data transfer. The left-channel data consists of the first data word, which is immediately followed by the right channel data word (see Figure 3-8). Input word length is defined by the IWL register. Figure 3–8 shows LRP = 1 (default LRP = 0).

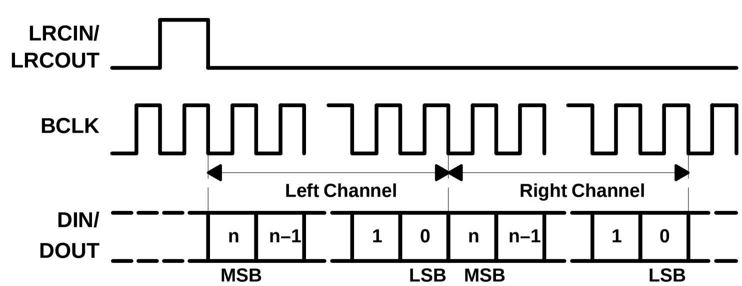


Figure 3–8. DSP Mode Timing

3.3.2 Audio Sampling Rates

The TLV320AIC23 can operate in master or slave clock mode. In the master mode, the TLV320AIC23 clock and sampling rates are derived from a 12-MHz MCLK signal. This 12-MHz clock signal is compatible with the USB specification. The TLV320AIC23 can be used directly in a USB system.

In the slave mode, an appropriate MCLK or crystal frequency and the sample rate control register settings control the TLV320AIC23 clock and sampling rates.

The settings in the sample rate control register control the clock mode and sampling rates.

Sample Rate Control (Address: 0001000)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	CLKOUT	CLKIN	SR3	SR2	SR1	SR0	BOSR	USB/Normal
Default	0	0	0	0	0	0	0	0	0

CLKOUT	Clock output divider	0 = MCLK	1 = MCLK/2
CLKIN	Clock input divider	0 = MCLK	1 = MCLK/2
SR[3:0]	Sampling rate control (see Sections 3.3.2.1 and 3.3.2.2)		
BOSR	Base oversampling rate		
	USB mode:	0 = 250 f_S	1 = 272 f_S
	Normal mode:	0 = 256 f_S	1 = 384 f_S
USB/Normal	Clock mode select:	0 = Normal	1 = USB
X	Reserved		

The clock circuit of the AIC23 has two internal dividers. The first, controlled by CLKIN, applies to the sampling-rate generator of the codec. The second, controlled by CLKOUT, applies only to the CLKOUT terminal. By setting CLKIN to 1, the entire codec is clocked with half the frequency, effectively dividing the resulting sampling rates by two. The following sampling-rate tables are based on CLKIN = MCLK.

3.3.2.1 USB-Mode Sampling Rates (MCLK = 12 MHz)

In the USB mode, the following ADC and DAC sampling rates are available:

SAMPLING RATE†		FILTER TYPE	SAMPLING-RATE CONTROL SETTINGS				
ADC (kHz)	DAC (kHz)		SR3	SR2	SR1	SR0	BOSR
96	96	3	0	1	1	1	0
88.2	88.2	2	1	1	1	1	1
48	48	0	0	0	0	0	0
44.1	44.1	1	1	0	0	0	1
32	32	0	0	1	1	0	0
8.021	8.021	1	1	0	1	1	1
8	8	0	0	0	1	1	0
48	8	0	0	0	0	1	0
44.1	8.021	1	1	0	0	1	1
8	48	0	0	0	1	0	0
8.021	44.1	1	1	0	1	0	1

† The sampling rates are derived from the 12-MHz master clock. The available oversampling rates do not produce exactly 8-kHz, 44.1-kHz, and 88.2-kHz sampling rates, but 8.021 kHz, 44.117 kHz, and 88.235 kHz, respectively. See Figures 3–17 through 3–34 for filter responses

3.3.2.2 Normal-Mode Sampling Rates

In normal mode, the following ADC and DAC sampling rates, depending on the MCLK frequency, are available:

MCLK = 12.288 MHz

SAMPLING RATE		FILTER TYPE	SAMPLING-RATE CONTROL SETTINGS				
ADC (kHz)	DAC (kHz)		SR3	SR2	SR1	SR0	BOSR
96	96	2	0	1	1	1	0
48	48	1	0	0	0	0	0
32	32	1	0	1	1	0	0
8	8	1	0	0	1	1	0
48	8	1	0	0	0	1	0
8	48	1	0	0	1	0	0

MCLK = 11.2896 MHz

SAMPLING RATE		FILTER TYPE	SAMPLING-RATE CONTROL SETTINGS				
ADC (kHz)	DAC (kHz)		SR3	SR2	SR1	SR0	BOSR
88.2	88.2	2	1	1	1	1	0
44.1	44.1	1	1	0	0	0	0
8.021	8.021	1	1	0	1	1	0
44.1	8.021	1	1	0	0	1	0
8.021	44.1	1	1	0	1	0	0

MCLK = 18.432 MHz

SAMPLING RATE		FILTER TYPE	SAMPLING-RATE CONTROL SETTINGS				
ADC (kHz)	DAC (kHz)		SR3	SR2	SR1	SR0	BOSR
96	96	2	0	1	1	1	1
48	48	1	0	0	0	0	1
32	32	1	0	1	1	0	1
8	8	1	0	0	1	1	1
48	8	1	0	0	0	1	1
8	48	1	0	0	1	0	1

MCLK = 16.9344 MHz

SAMPLING RATE		FILTER TYPE	SAMPLING-RATE CONTROL SETTINGS				
ADC (kHz)	DAC (kHz)		SR3	SR2	SR1	SR0	BOSR
88.2	88.2	2	1	1	1	1	1
44.1	44.1	1	1	0	0	0	1
8.021	8.021	1	1	0	1	1	1
44.1	8.021	1	1	0	0	1	1
8.021	44.1	1	1	0	1	0	1

3.3.3 Digital Filter Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter Characteristics (TI DSP 250 f_S Mode Operation)					
Passband	±0.05 dB	0.416 f_S			Hz
Stopband	–6 dB		0.5 f_S		Hz
Passband ripple				±0.05	dB
Stopband attenuation	f > 0.584 f_S		–60		dB
ADC Filter Characteristics (TI DSP 272 f_S and Normal Mode Operation)					
Passband	±0.05 dB	0.4535 f_S			Hz
Stopband	–6 dB		0.5 f_S		Hz
Passband ripple				±0.05	dB
Stopband attenuation	f > 0.5465 f_S		–60		dB
ADC High-Pass Filter Characteristics					
Corner frequency	–3 dB, f_S = 44.1 kHz		3.7		Hz
	–3 dB, f_S = 48 kHz		4.0		Hz
	–0.5 dB, f_S = 44.1 kHz		10.4		Hz
	–0.5 dB, f_S = 48 kHz		11.3		Hz
	–0.1 dB f_S = 44.1 kHz		21.6		Hz
	–0.1 dB, f_S = 48 kHz		23.5		Hz
DAC Filter Characteristics (48-kHz Sampling Rate)					
Passband	±0.03 dB	0.416 f_S			Hz
Stopband	–6 dB		0.5 f_S		Hz
Passband ripple				±0.03	dB
Stopband attenuation	f > 0.584 f_S		–50		dB
DAC Filter Characteristics (44.1-kHz Sampling Rate)					
Passband	±0.03 dB	0.4535 f_S			Hz
Stopband	–6 dB		0.5 fs		Hz
Passband ripple				±0.03	dB
Stopband attenuation	f > 0.5465 f_S		–50		dB

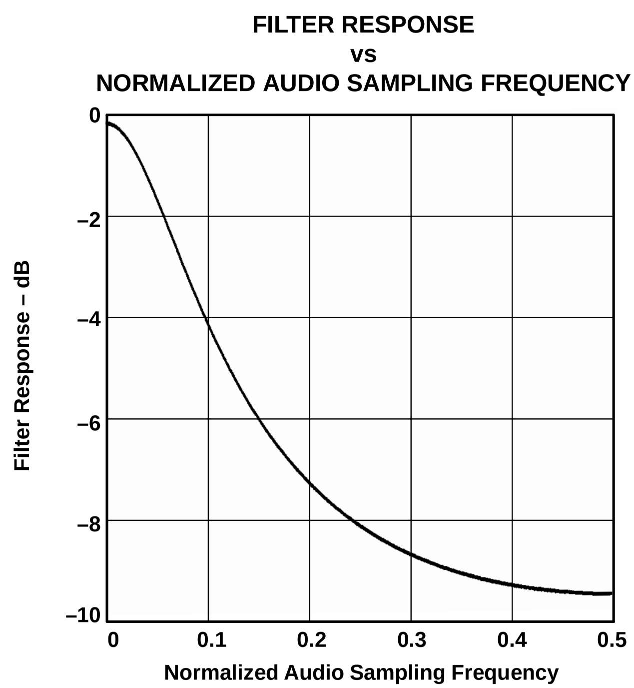


Figure 3–9. Digital De-Emphasis Filter Response – 44.1 kHz Sampling

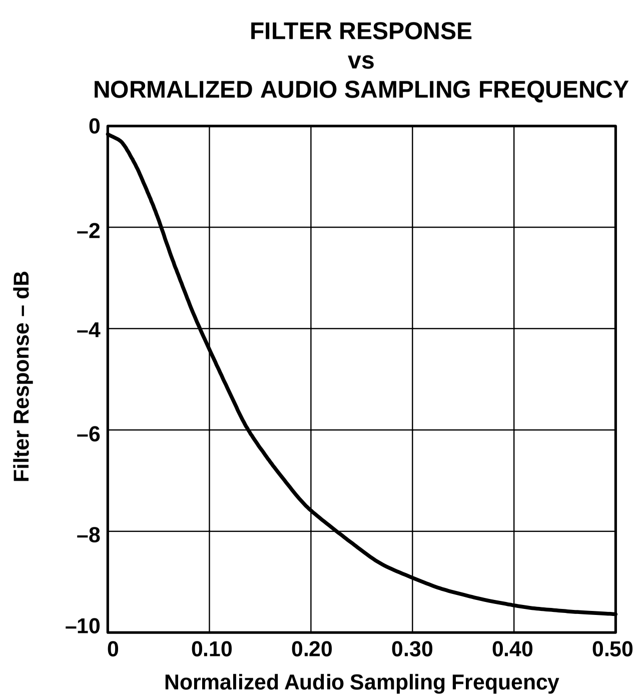


Figure 3–10. Digital De-Emphasis Filter Response – 48 kHz Sampling

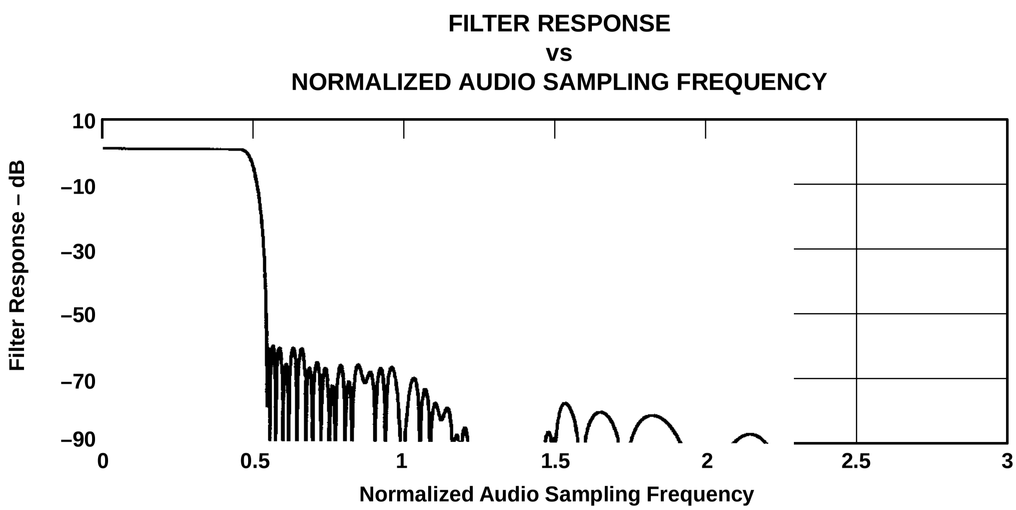


Figure 3–11. ADC Digital Filter Response I: TI DSP and Normal Modes (Group Delay = 12 Output Samples)

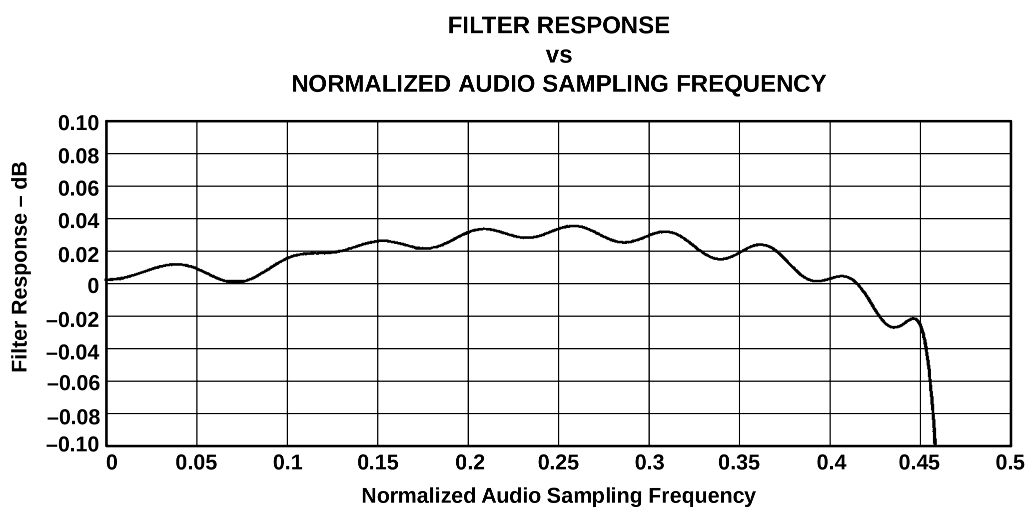


Figure 3–12. ADC Digital Filter Ripple I: TI DSP and Normal Modes (Group Delay = 20 Output Samples)

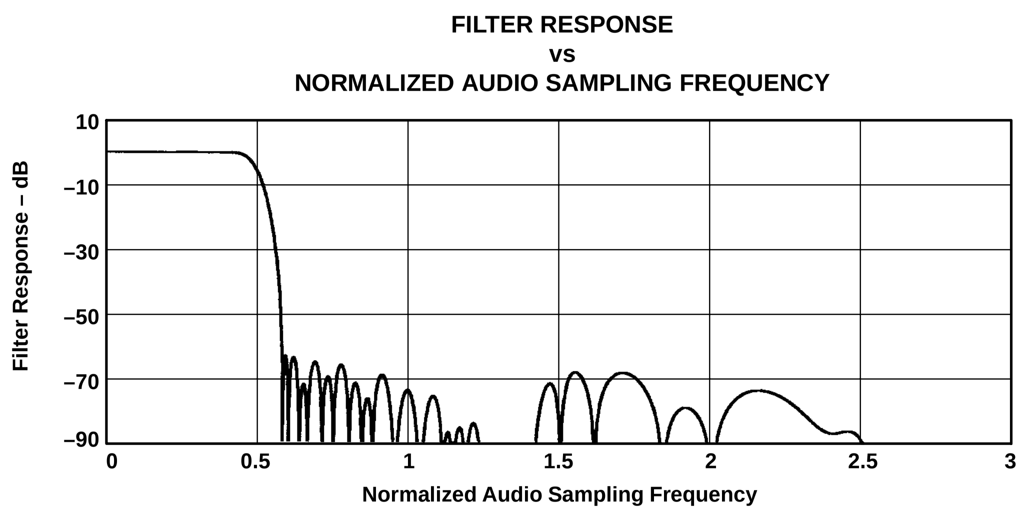


Figure 3–13. ADC Digital Filter Response II: TI DSP Mode Only

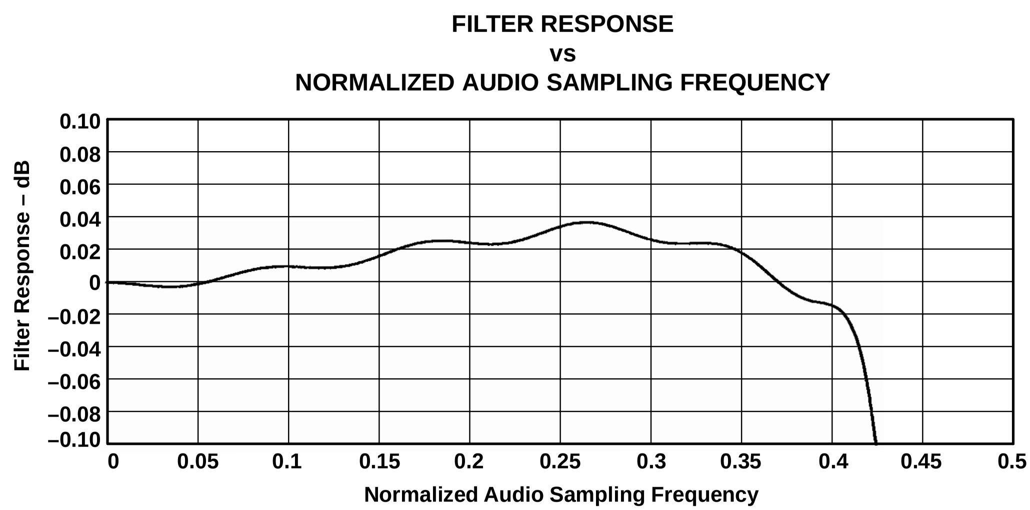


Figure 3–14. ADC Digital Filter Ripple II: TI DSP Mode Only

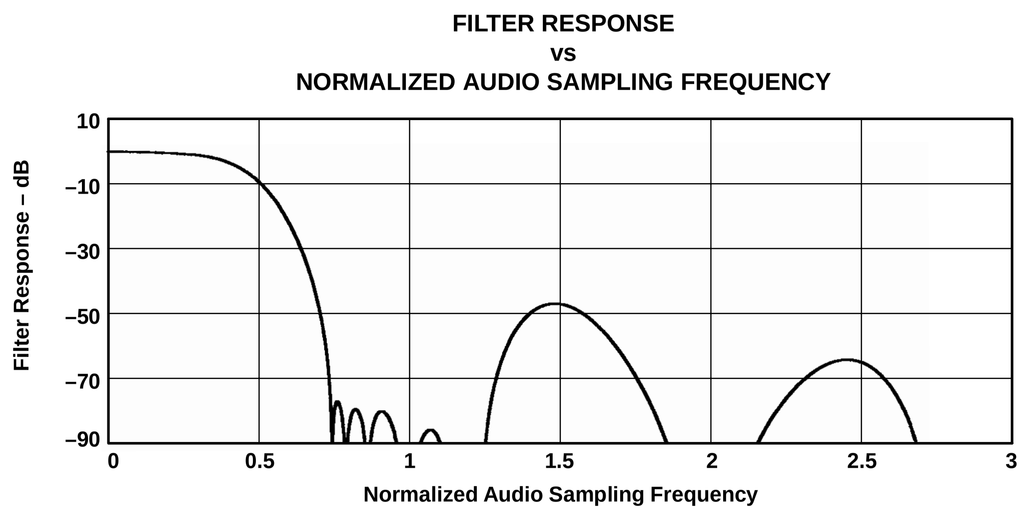


Figure 3–15. ADC Digital Filter Response III: TI DSP and Normal Modes (Group Delay = 3 Output Samples)

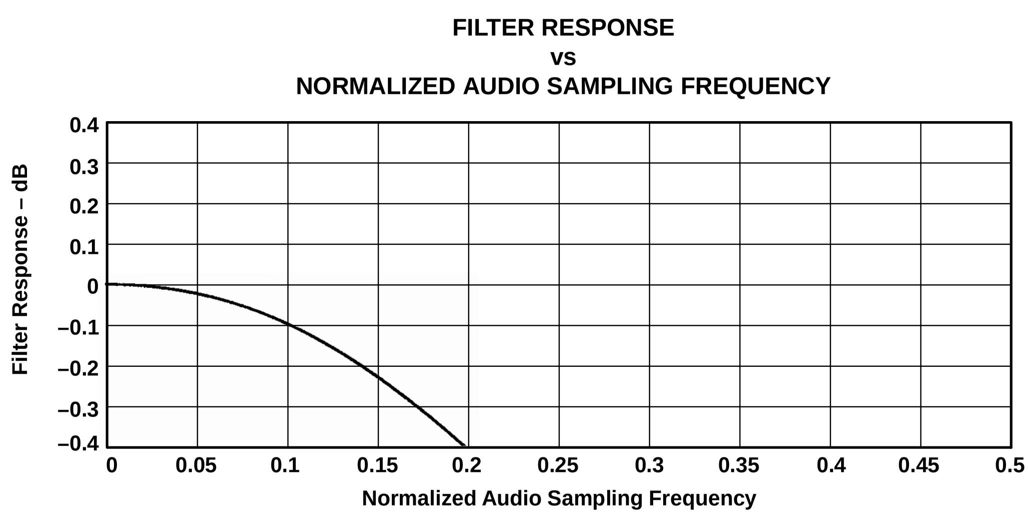


Figure 3–16. ADC Digital Filter Ripple III: TI DSP and Normal Modes

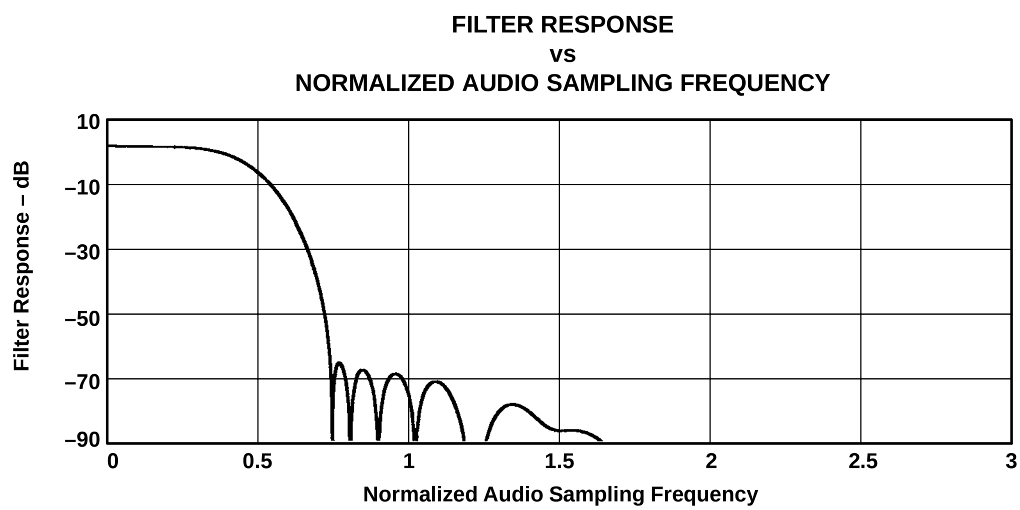


Figure 3–17. ADC Digital Filter Response IV: TI DSP Mode Only

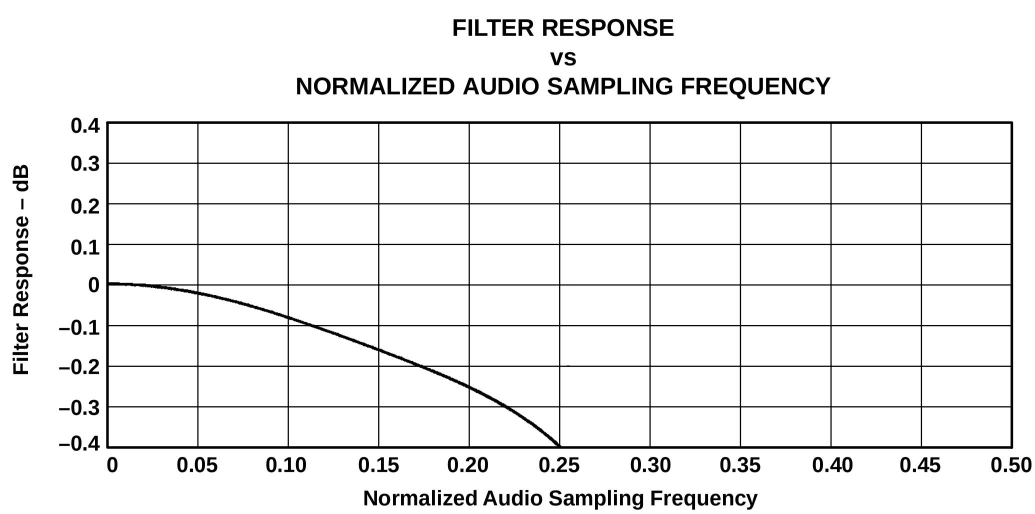


Figure 3–18. ADC Digital Filter Ripple IV: TI DSP Mode Only

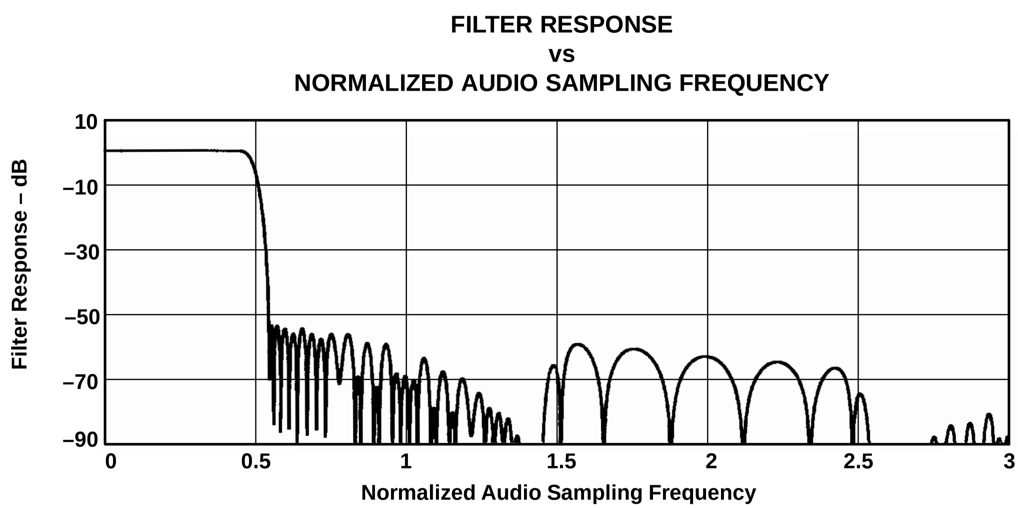


Figure 3–19. DAC Digital Filter Response I: TI DSP and Normal Modes

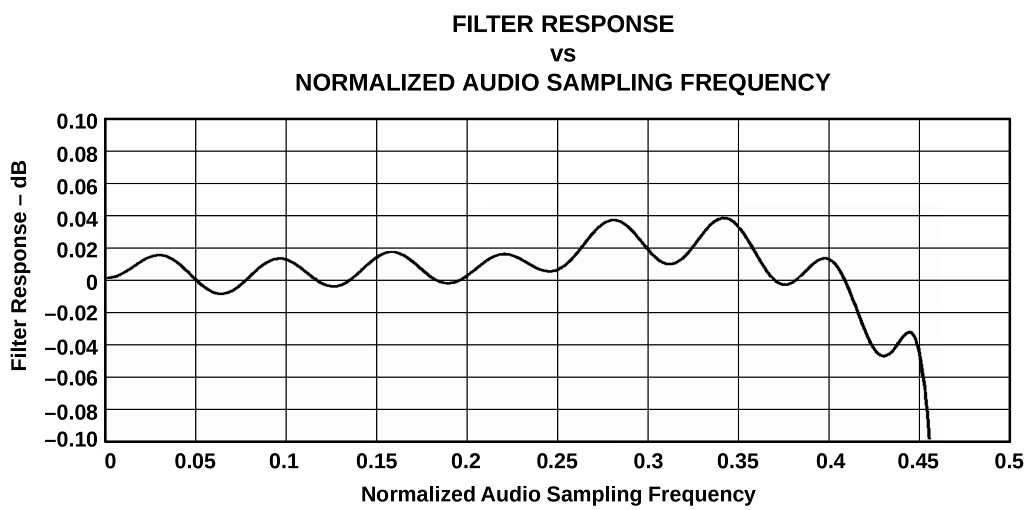


Figure 3–20. DAC Digital Filter Ripple I: TI DSP and Normal Modes

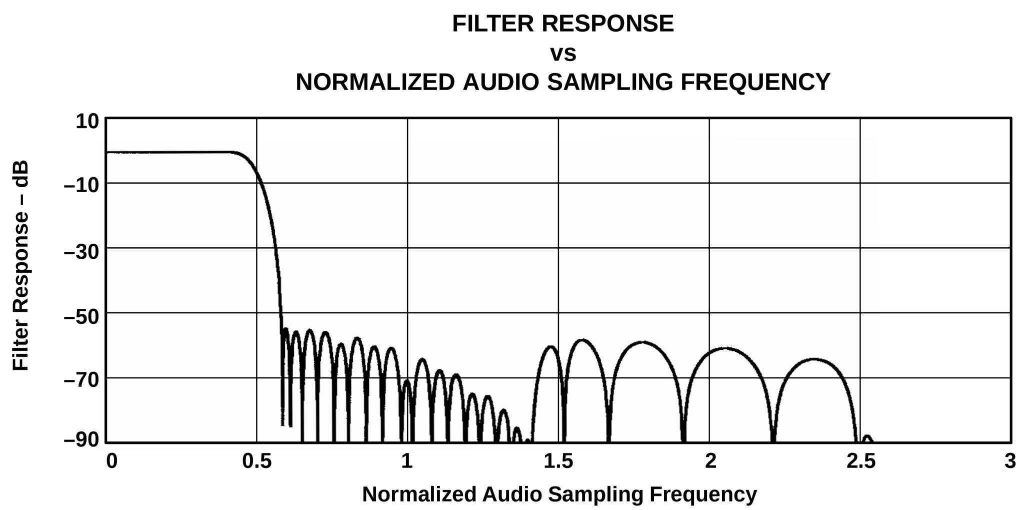


Figure 3–21. DAC Digital Filter Response II: TI DSP Mode Only

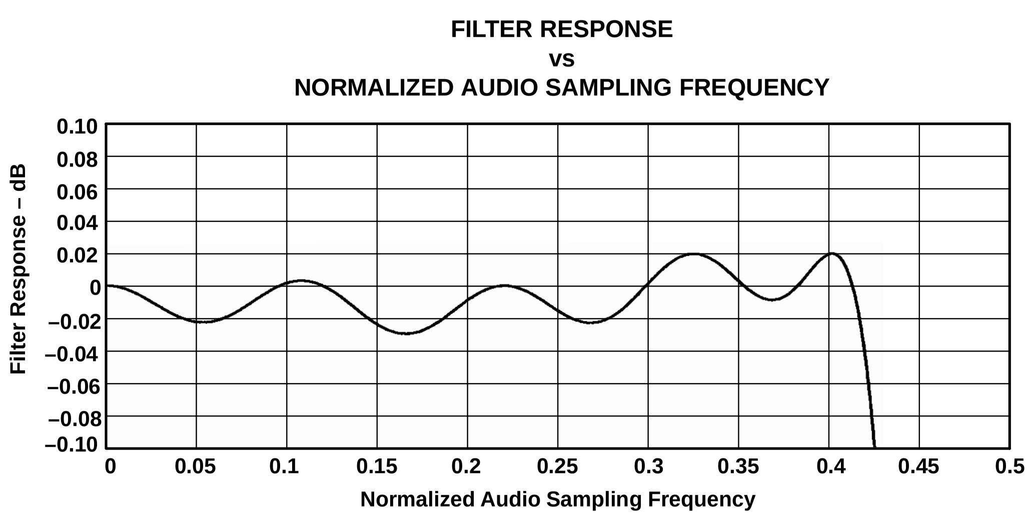


Figure 3–22. DAC Digital Filter Ripple II: TI DSP Mode Only

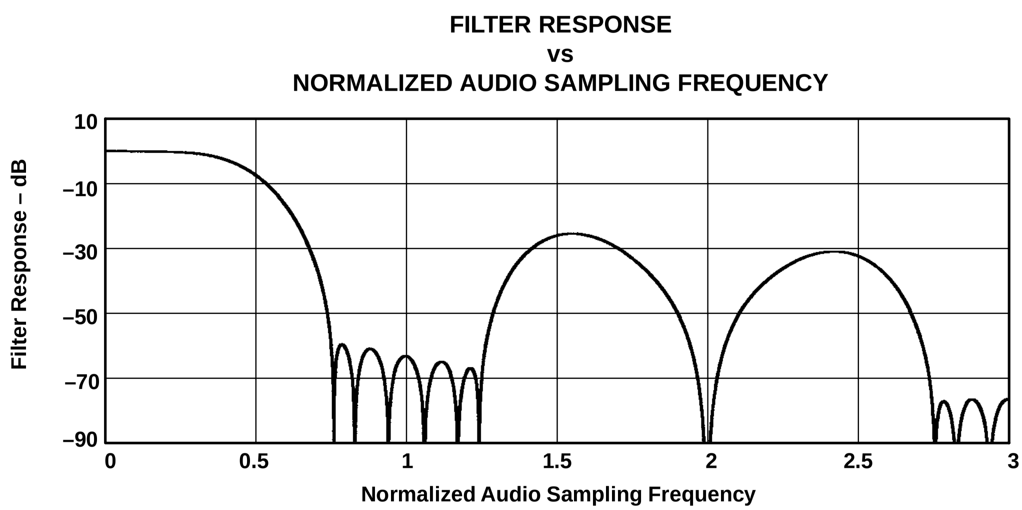


Figure 3–23. DAC Digital Filter Response III: TI DSP and Normal Modes

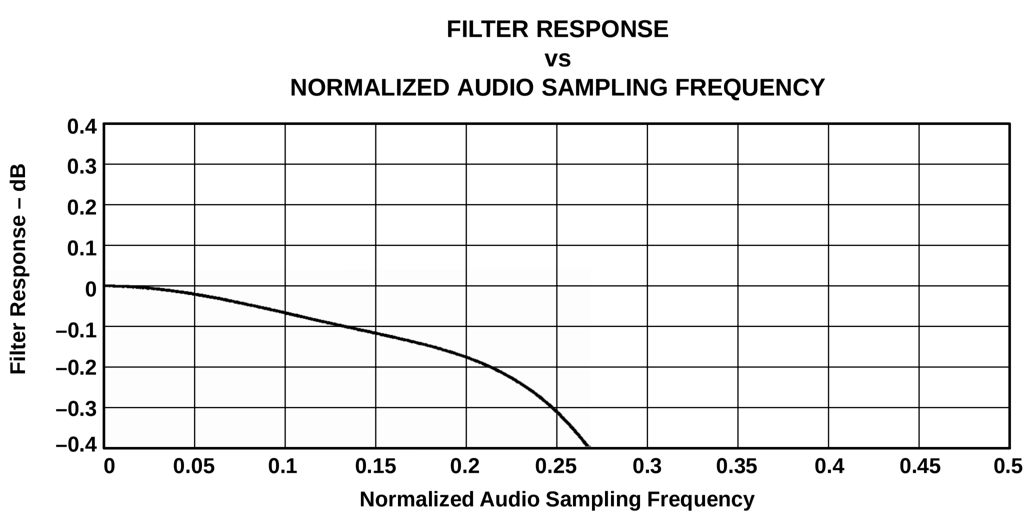


Figure 3–24. DAC Digital Filter Ripple III: TI DSP and Normal Modes

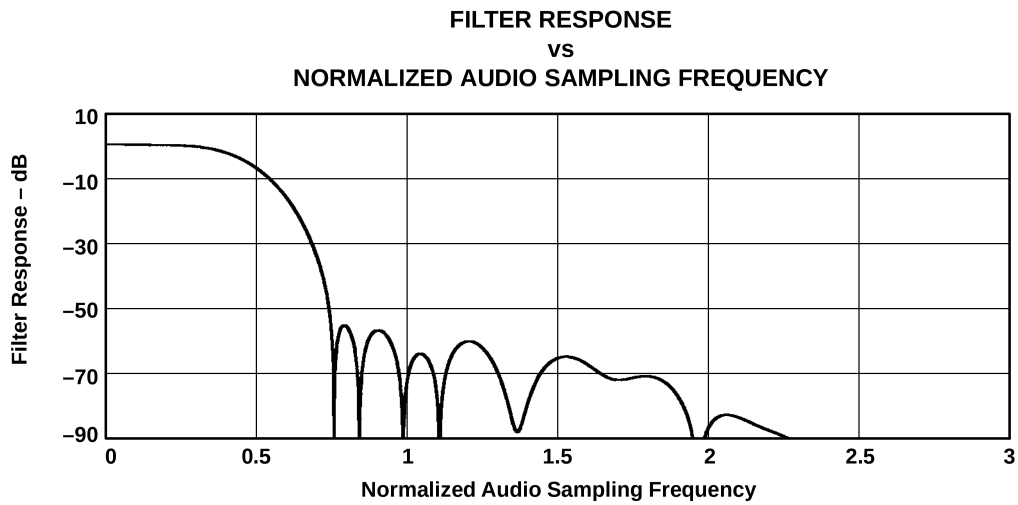


Figure 3–25. DAC Digital Filter Response IV: TI DSP Mode Only

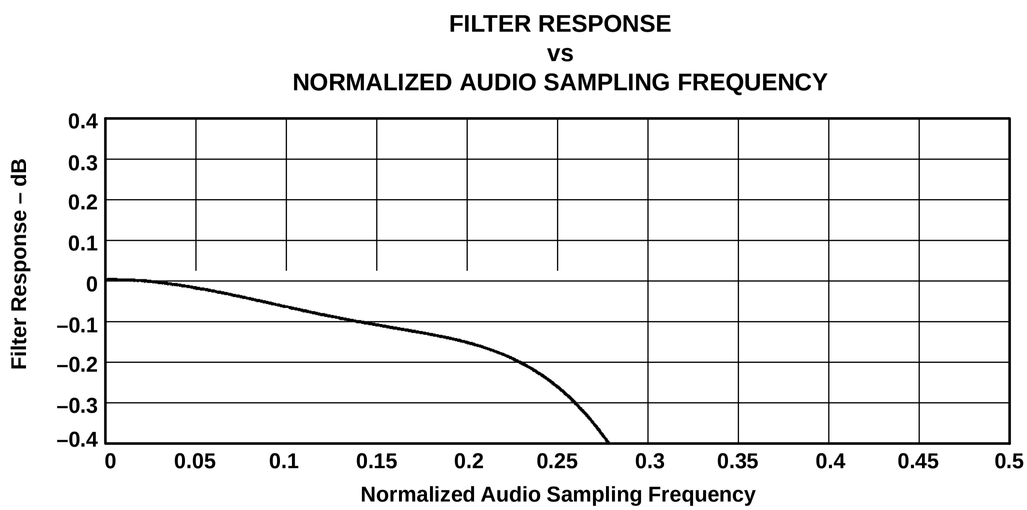
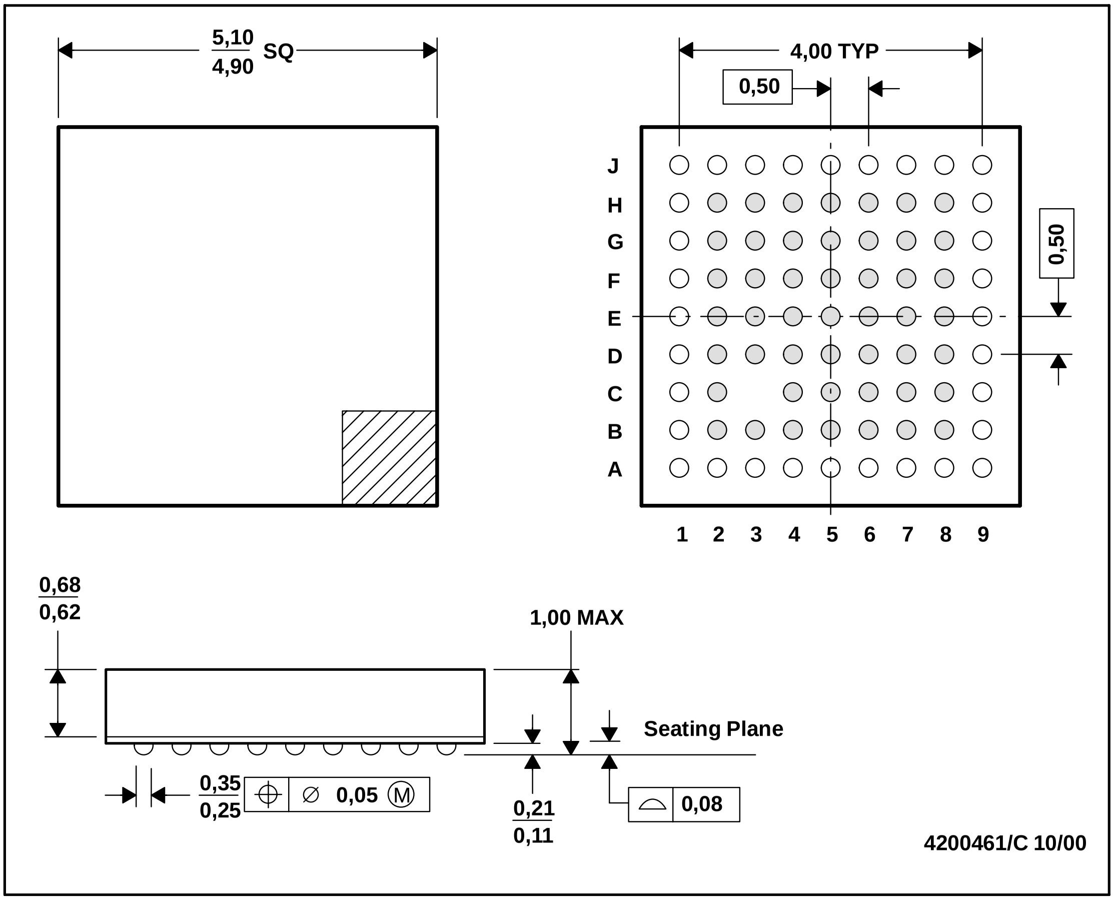


Figure 3–26. DAC Digital Filter Ripple IV: TI DSP Mode Only

Appendix A
Mechanical Data

GQE (S-PBGA-N80) PLASTIC BALL GRID ARRAY

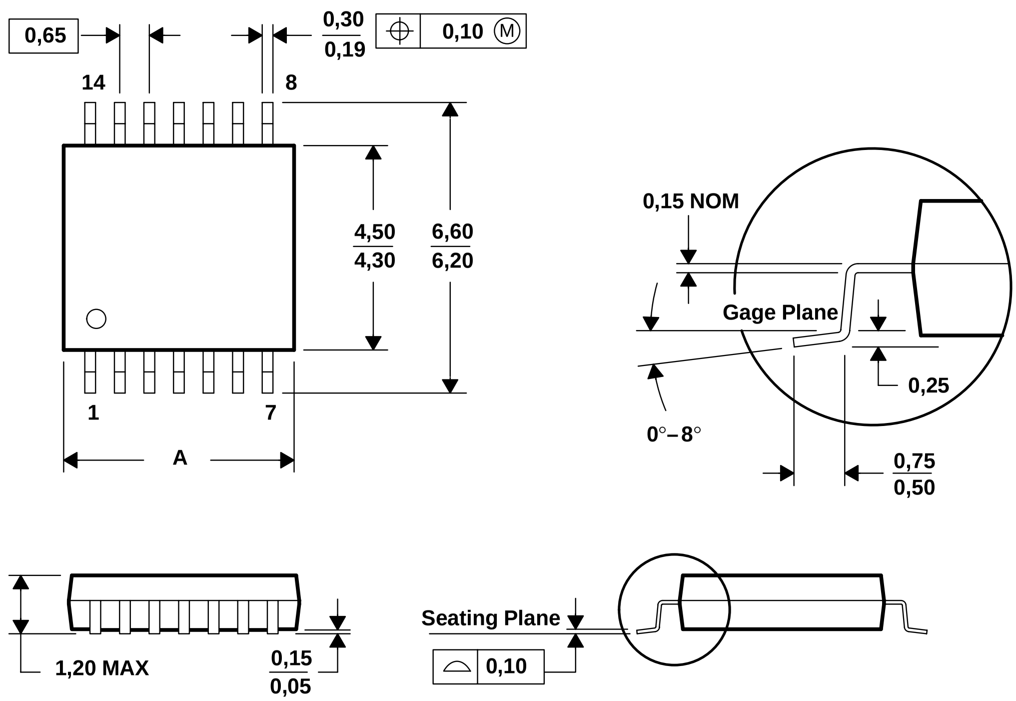


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO-225

MicroStar Junior is a trademark of Texas Instruments.

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153