POWER AND BATTERY MANAGEMENT IC FOR Li-ION POWERED SYSTEMS

FEATURES

- **Linear Charger Management for Single Li-Ion or Li-Polymer Cells**
- **Dual Input Ports for Charging From USB or From Wall Plug, Handles 100-mA / 500-mA USB Requirements**
- **Charge Current Programmable Via External Resistor**
- **1 A, 95% Efficient Step-Down Converter for I/O and Peripheral Components (VMAIN)**
- **400 mA, 90% Efficient Step-Down Converter for Processor Core (VCORE)**
- **2x 200-mA LDOs for I/O and Peripheral Components, LDO Enable via Bus**
- **Serial Interface Compatible With I^2C, Supports 100 kHz, 400-kHz Operation**
- **LOW_PWR Pin to Lower or Disable Processor Core Supply Voltage in Deep Sleep Mode**
- **70-µA Quiescent Current**
- **1% Reference Voltage**
- **Thermal Shutdown Protection**
- **HBM and CDM Capabilities of 1 kV at VIB, PG, and LED2 pins**

APPLICATIONS

- **All Single Li-Ion Cell Operated Products Requiring Multiple Supplies Including:**
  - **PDA**
  - **Cellular/Smart Phone**
  - **Internet Audio Player**
  - **Digital Still Camera**
- **Digital Radio Player**
- **Split Supply DSP and µP Solutions**

DESCRIPTION

The TPS65010 is an integrated power and battery management IC for applications powered by one Li-Ion or Li-Polymer cell, and which require multiple power rails. The TPS65010 provides two highly efficient, step-down converters targeted at providing the core voltage and peripheral, I/O rails in a processor based system. Both step-down converters enter a low power mode at light load for maximum efficiency across the widest possible range of load currents. The LOW_PWR pin allows the core converter to lower its output voltage when the application processor goes into deep sleep. The TPS65010 also integrates two 200-mA LDO voltage regulators, which are enabled via the serial interface. Each LDO operates with an input voltage range between 1.8 V and 6.5 V, allowing them to be supplied from one of the step-down converters or directly from the battery.

The TPS65010 also boasts a highly integrated and flexible Li-Ion linear charger and system power management. It offers integrated USB-port and ac-adapter supply management with autonomous power-source selection, power FET and current sensor, high accuracy current and voltage regulation, charge status, and charge termination.

The TPS65010 charger automatically selects the USB-Port or the ac-adapter as the power source for the system. In the USB configuration, the host can increase the charge current from the default value of maximum 100 mA to 500 mA via the interface. In the ac-adapter configuration an external resistor sets the maximum value of charge current.

The battery is charged in three phases: conditioning, constant current, and constant voltage. Charge is normally terminated based on minimum current. An internal charge timer provides a safety backup for charge termination. The TPS65010 automatically restarts the charge if the battery voltage falls below an internal threshold. The charger automatically enters sleep mode when both supplies are removed.

The serial interface can be used for dynamic voltage scaling, for collecting information on and controlling the battery charger status, for optionally controlling 2 LED driver outputs, a vibrator driver, masking interrupts, or for dis/enabling and setting the LDO output voltages. The interface is compatible with the fast/standard mode I^2C™ specification allowing transfers at up to 400 kHz.

I^2C is a trademark of Phillips.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER(1)
−40°C to 85°C	7 mm × 7 mm, 48-pin QFN	TPS65010RGZ

(1) The RGZ package is available in tape and reel. Add R suffix (TPS65010RGZR) to order quantities of 2500 parts per reel. Add T suffix (TPS65010RGZT) to order quantities of 250 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNIT
Input voltage on VAC pin with respect to AGND	20 V
Input voltage range on all other pins except A/PGND pins with respect to AGND	−0.3 V to 7 V
Current at AC, VBAT, VINMAIN, L1, PGND1	1800 mA
Peak current at all other pins	1000 mA
Continuous power dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A	−40°C to 85°C
Maximum junction temperature, T_J	125°C
Storage temperature, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

The TPS65010 is housed in a 48 pin QFN package with exposed leadframe on the underside. This 7 mm × 7 mm package exhibits a thermal impedance (junction-to-ambient) of 33 K/W when mounted on a JEDEC high-k board.

AMBIENT TEMPERATURE	MAX POWER DISSIPATION FOR T_J = 125°C	DERATING FACTOR ABOVE T_A = 55°C
25°C	3 W	30 mW/°C
55°C	2.1 W	

Consideration needs to be given to the maximum charge current when the assembled application board exhibits a thermal impedance which differs significantly from the JEDEC high-k board.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{(AC)}$	Supply voltage from ac adapter	4.5		5.5	V
$V_{(USB)}$	Supply voltage from USB	4.4		5.25	V
$V_{(BAT)}$	Voltage at charger output/battery	2.5		4.2	V
$C_{I(AC)}$	Input capacitor at ac input		1		µF
$C_{I(USB)}$	Input capacitor at USB input		1		µF
$C_{I(BAT)}$	Input capacitor at VBAT output		0.1		µF
$V_{I(MAIN)}$, $V_{I(CORE)}$, V_{CC}	Input voltage range step-down convertors	2.5		6.0	V
$V_{O(MAIN)}$	Output voltage range for main step-down convertor	2.5		3.3	V
$V_{I(CORE)}$	Output voltage range for core step-down convertor	0.85		1.6	
$V_{I(LDO1)}$, $V_{I(LDO2)}$	Input voltage range for LDOs	1.8		6.5	V
$V_{O(LDO1-2)}$	Output voltage range for LDOs	0.9		$V_{I(LDO1-2)}$	V
$I_{O(L1)}$	Output current at L1	1000			mA
$L_{(1)}$	Inductor at L1 (see Note 1)		6.8		µH
$C_{I(VCC)}$	Input capacitor at VCC (see Note 1)		1		µF
$C_{I(MAIN)}$	Input capacitor at VINMAIN (see Note 1)		22		µF
$C_{I(CORE)}$	Input capacitor at VINCORE (see Note 1)		10		µF
$C_{O(1)}$	Output capacitor at VMAIN (see Note 1)		22		µF
$C_{O(2)}$	Output current at L2	400			mA
$L_{(2)}$	Inductor at L2 (see Note 1)		10		µH
$C_{O(2)}$	Output capacitor at VCORE (see Note 1)		10		µF
$C_{I(1-2)}$	Input capacitor at VINLDO1, VINLDO2 (see Note 1)		1		µF
$C_{O(1-2)}$	Output capacitor at VLDO1−2 (see Note 1)		2.2		µF
$I_{O(LDO1,2)}$	Output current at VLDO1,2	200			mA
T_A	Operating ambient temperature	−40		85	°C
T_J	Operating junction temperature	−40		125	°C
$R_{(CC)}$	Resistor from $V_{I(main)}$,$V_{I(core)}$ to Vcc used for filtering, $C_{I(VCC)} = 1\ \mu F$		10	100	Ω

(1) See applications section for more information

ELECTRICAL CHARACTERISTICS

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)} = 3.6V$, $T_A = -40°C$ to 85°C, typical values are at $T_A = 25°C$ Battery charger specifications are valid in the range 0°C < T_A < 85°C unless otherwise noted

Control Signals: LOW_PWR, SCLK, SDAT (input)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	$I_{IH} = 20\ \mu A$(1)	0.8 V_{CC}		V_{CC}	V
V_{IL}	Low level input voltage	$I_{IL} = 10\ \mu A$	0		0.2 V_{CC}	V
I_{IB}	Input bias current			0.01	1.0	µA

(1) If the input voltage is higher than V_{CC}, an additional input current, limited by an internal 10-k resister, flows.

Control Signals: PB_ONOFF, $\overline{\text{HOT\_RESET}}$, BATT_COVER

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	$I_{IH} = 20\ \mu A$(1)	1.4		6	V
V_{IL}	Low level input voltage	$I_{IL} = 10\ \mu A$	0		0.4	V
$R_{(pb\_onoff)}$	Pulldown resistor at PB_ONOFF			1000		kΩ
$R_{(hot\_reset)}$	Pullup resistor at $\overline{\text{HOT\_RESET}}$, connected to VCC			1000		kΩ
$R_{(batt\_cover)}$	Pulldown resistor at BATT_COVER			2000		kΩ

ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)}$ = 3.6V, T_A = −40°C to 85°C, typical values are at T_A = 25°C Battery charger specifications are valid in the range 0°C < T_A < 85°C unless otherwise noted

Control Signals: PB_ONOFF, $\overline{\text{HOT\_RESET}}$, BATT_COVER (Continued)

$t_{(glitch)}$	De-glitch time at all 3 pins		38	56	77	ms
$t_{(batt\_cover)}$	Delay after $t_{(glitch)}$ ($\overline{\text{PWRFAIL}}$ goes low) before supplies are disabled when BATT_COVER goes low.		1.68	2.4	3.2	ms

(1) If the input voltage is higher than V_{CC}, an additional input current, limited by an internal 10-k resister, flows.

Control Signals: $\overline{\text{MPU\_RESET}}$, $\overline{\text{PWRFAIL}}$, $\overline{\text{RESPWRON}}$, $\overline{\text{INT}}$, SDAT (output)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage				6	V
V_{OL}	Low level output voltage	I_{IL} = 10 mA	0		0.3	V
$t_{d(mpu\_nreset)}$	Duration of low pulse at $\overline{\text{MPU\_RESET}}$		100			µs
$t_{d(nrespwron)}$	Duration of low pulse at $\overline{\text{RESPWRON}}$ after VLDO1 is in regulation	CHGCONFIG<7> = 0 (Default)	800	1000	1200	ms
		CHGCONFIG<7> = 1	49	69	89	
$t_{d(uvlo)}$	Time between UVLO going active ($\overline{\text{PWRFAIL}}$ going low) and supplies being disabled		1.68	2.4	3.2	ms
$t_{d(overtemp)}$	Time between chip over-temperature condition being recognized ($\overline{\text{PWRFAIL}}$ going low) and supplies being disabled		1.68	2.4	3.2	ms

Supply pin: VCC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(Q)}$	Operating quiescent current	V_I = 3.6 V, current into Main + Core + V_{CC}			50	µA
$I_{O(SD)}$	Shutdown supply current	V_I = 3.6 V, BATT_COVER = GND, current into Main + Core + V_{CC}		15	25	µA

VMAIN Step-Down Converter

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage range			2.5		6.0	V
I_O	Maximum output current			1000			mA
$I_{O(SD)}$	Shutdown supply current		BATT_COVER = GND		0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance		$V_{I(MAIN)} = V_{GS}$ = 3.6 V		110	210	mΩ
$I_{lkg(p)}$	P-channel leakage current		$V_{(DS)}$ = 6.0 V			1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance		$V_{I(MAIN)} = V_{GS}$ = 3.6 V		110	200	mΩ
$I_{lkg(N)}$	N-channel leakage current		$V_{(DS)}$ = 6.0 V			1	µA
I_L	P-channel current limit		2.5 V< $V_{I(MAIN)}$ < 6.0 V	1.4	1.75	2.1	A
f_S	Oscillator frequency			1	1.25	1.5	MHz
$V_{O(MAIN)}$	Fixed output voltage	2.5 V	$V_{I(MAIN)}$ = 2.7 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 2.7 V to 6.0 V; 0 mA ≤ I_O ≤ 1000 mA	−3%		3%	
		2.75 V	$V_{I(MAIN)}$ = 2.95 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 2.95 V to 6.0 V; 0 mA ≤ I_O ≤ 1000 mA	−3%		3%	
		3.0 V	$V_{I(MAIN)}$ = 3.2 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 3.2 V to 6.0 V; 0 mA ≤ I_O ≤ 1000 mA	−3%		3%	
		3.3 V	$V_{I(MAIN)}$ = 3.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 3.5 V to 6.0 V; 0 mA ≤ I_O ≤ 1000 mA	−3%		3%	
	Line regulation		$V_{I(MAIN)} = V_{O(MAIN)}$ + 0.5 V (min. 2.5 V) to 6.0 V, I_O = 10 mA		0.5		%/V
	Load regulation		I_O = 10 mA to 1000 mA		0.12		%/A
$R_{(VMAIN)}$	VMAIN discharge resistance				400		Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)}$ = 3.6V, T_A = −40°C to 85°C, typical values are at T_A = 25°C Battery charger specifications are valid in the range 0°C < T_A < 85°C unless otherwise noted

VCORE Step-Down Converter

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage range			2.5		6.0	V
I_O	Maximum output current			400			mA
$I_{O(SD)}$	Shutdown supply current		BATT_COVER = GND		0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance		$V_{I(CORE)} = V_{GS}$ = 3.6 V		275	530	mΩ
$I_{lkg(p)}$	P-channel leakage current		V_{DS} = 6.0 V		0.1	1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance		$V_{I(CORE)} = V_{GS}$ = 3.6 V		275	500	mΩ
$I_{lkg(N)}$	N-channel leakage current		V_{DS} = 6.0 V		0.1	1	µA
I_L	P-channel current limit		2.5 V< $V_{I(CORE)}$ < 6.0 V	600	700	900	mA
f_S	Oscillator frequency			1	1.25	1.5	MHz
$V_{O(CORE)}$	Fixed output voltage	0.85 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA, C_O = 22 µF	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA, C_O = 22 µF	−3%		3%	
		1.0 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA, C_O = 22 µF	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA, C_O = 22 µF	−3%		3%	
		1.1 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA, C_O = 22 µF	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA, C_O = 22 µF	−3%		3%	
		1.2 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA	−3%		3%	
		1.3 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA	−3%		3%	
		1.4 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA	−3%		3%	
		1.5 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA	−3%		3%	
		1.6 V	$V_{I(CORE)}$ = 2.5 V to 6.0 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 400 mA	−3%		3%	
	Line regulation		$V_{I(CORE)} = V_{O(MAIN)}$ + 0.5 V (min. 2.5 V) to 6.00 V, I_O = 10 mA		1		%/V
	Load regulation		I_O = 10 mA to 400 mA		0.002		%/mA
$R_{(VCORE)}$	VCORE discharge resistance				400		Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)}$ = 3.6V, T_A = −40°C to 85°C, typical values are at T_A = 25°C Battery charger specifications are valid in the range 0°C < T_A < 85°C unless otherwise noted

VLDO1 and VLDO2 Low-Dropout Regulators

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage range		1.8		6.5	V
V_O	LDO1 output voltage range		0.9		VINLDO1	V
V_{ref}	Reference voltage		485	500	515	mV
V_O	LDO2 output voltage range		1.8		3.0	V
I_O	Maximum output current	Full-power mode	200			mA
		Low-power mode	30			
$I_{(SC)}$	LDO1 & LDO2 short-circuit current limit	VLDO1 = GND, VLDO2 = GND			600	mA
	Dropout voltage	I_O = 200 mA, VINLDO1,2 = 1.8 V			300	mV
	Total accuracy				±3%	
	Line regulation	VINLDO1,2 = VLDO1,2 + 0.5 V (min. 2.5 V) to 6.5 V, I_O = 10 mA		0.75		%/V
	Load regulation	I_O = 10 mA to 200 mA		0.011		%/mA
	Regulation time	Load change from 10% to 90%			0.1	ms
		Low-power mode		0.1		
$I_{(QFP)}$	LDO quiescent current (each LDO)	Full-power mode		16	25	µA
$I_{(QLPM)}$	LDO quiescent current (each LDO)	Low-power mode		12	18	µA
$I_{O(SD)}$	LDO shutdown current (each LDO)			0.1	1	µA
$I_{lkg(FB)}$	Leakage current feedback			0.01	0.1	µA

Battery Charger, $V_{O(REG)} + V_{(DO-MAX)} \leq V_{(CHG)} = V_{(AC)}$ or $V_{(USB)}$, $I_{(TERM)} < I_O \leq$ 1 A, 0°C < T_A < 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(AC)}$	Input voltage range		4.5		5.5	V
$V_{(USB)}$	Input voltage range		4.35		5.25	V
$I_{CC(VCHG)}$	Supply current	$V_{(CHG)} > V_{(CHG)}min$		1.2	2	mA
$I_{CC(SLP)}$	Sleep current	Sum of currents into VBAT pin, $V_{(CHG)} < V_{(SLP-ENTRY)}$, 0°C ≤ T_J ≤ 85°C		2	5	µA
$I_{CC(STBY)}$	Standby current	Current into USB pin			40	µA
		Current into AC pin			200	
VOLTAGE REGULATION						
V_O	Output voltage	$V_{(CHG)}min \geq 4.5$ V	4.15	4.20	4.25	V
V_{DO}	Dropout voltage ($V_{(AC)}$ –VBAT)	$V_{O(REG)} + V_{(DO-MAX)} \leq V_{(CHG)}$, $I_{O(OUT)}$ = 1 A		500	800	mV
	Dropout voltage ($V_{(USB)}$ –VBAT)	$V_{O(REG)} + V_{(DO-MAX)} \leq V_{(CHG)}$, $I_{O(OUT)}$ = 0.5 A		300	500	
	Dropout voltage ($V_{(USB)}$ –VBAT)	$V_{O(REG)} + V_{(DO-MAX)} \leq V_{(CHG)}$, $I_{O(OUT)}$ = 0.1 A		100	150	

ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)}$ = 3.6V, T_A = −40°C to 85°C, typical values are at T_A = 25°C Battery charger specifications are valid in the range 0°C < T_A < 85°C unless otherwise noted

CURRENT REGULATION						
$I_{O(AC)}$	Output current range for ac operation (1)	$V_{CHG} \geq 4.5V$, $V_{I(OUT)} > V_{(LOWV)}$, $V_{(AC)} - V_{I(BAT)} > V_{(DO-MAX)}$	100		1000	mA
$V_{(SET)}$	Output current set voltage for ac operation at ISET pin. 100% output current I^2C register CHGCONFIG<4:3> = 11	$V_{(CHG)}min \geq 4.5V$, $V_{I(BAT)} > V_{(LOWV)}$, $V_{(AC)} - V_{I(BAT)} > V_{(DO-MAX)}$	2.45	2.50	2.55	V
	75% output current I^2C register CHGCONFIG<4:3> = 10		1.819	1.875	1.931	
	50% output current I^2C register CHGCONFIG<4:3> = 01		1.213	1.25	1.288	
	32% output current I^2C register CHGCONFIG<4:3> = 00		0.775	0.8	0.825	
	Output current set factor for ac operation, kset	100 mA< I_O < 1000 mA	310	330	350	
$I_{O(USB)}$	Output current range for USB operation	$V_{(CHG)}min \geq 4.35V$, $V_{I(BAT)} > V_{(LOWV)}$, $V_{(USB)} - V_{I(BAT)} > V_{(DO-MAX)}$, I^2C register CHGCONFIG<2> = 0	80		100	mA
		$V_{(CHG)}min \geq 4.5V$, $V_{I(BAT)} > V_{(LOWV)}$, $V_{USB} - V_{I(BAT)} > V_{(DO-MAX)}$, I^2C register CHGCONFIG<2> = 1	400		500	
$R_{(ISET)}$	Resistor range at ISET pin		825		8250	Ω
PRECHARGE CURRENT REGULATION, SHORT-CIRCUIT CURRENT, AND BATTERY DETECTION CURRENT						
$V_{(LOWV)}$	Precharge to fast-charge transition threshold, voltage on VBAT pin.	$V_{(CHG)}min \geq 4.5V$	2.8	3.0	3.2	V
	Deglitch time	$V_{(CHG)}min \geq 4.5V$, $V_{I(OUT)}$ decreasing below threshold; 100-ns fall time, 10-mV overdrive	250	375	500	ms
$I_{(PRECHG)}$	Precharge current (2)	$0 \leq V_{I(OUT)} < V_{(LOWV)}$, $t < t_{(PRECHG)}$	10		100	mA
$V_{(SET-PRECHG)}$	Voltage at ISET pin	$0 \leq V_{I(OUT)} < V_{(LOWV)}$, $t < t_{(PRECHG)}$	240	255	270	mV
CHARGE TAPER AND TERMINATION DETECTION						
$I_{(TAPER)}$	Taper current detect range (3)	$V_{I(OUT)} > V_{(RCH)}$, $t < t_{(TAPER)}$	10		100	mA
$V_{(SET\_TAPER)}$	Voltage at ISET pin for charge TAPER detection	$V_{I(OUT)} > V_{(RCH)}$, $t < t_{(TAPER)}$	235	250	265	mV
$V_{(SET\_TERM)}$	Voltage at ISET pin for charger termination detection (4)	$V_{I(OUT)} > V_{(RCH)}$	11	18	25	mV
	Deglitch time for $I_{(TAPER)}$	$V_{(CHG)}min \geq 4.5V$, charging current increasing or decreasing above and below; 100-ns fall time, 10-mV overdrive	250	375	500	ms
	Deglitch time for $I_{(TERM)}$	$V_{(CHG)}min \geq 4.5V$, charging current decreasing below; 100-ns fall time, 10-mV overdrive	250	375	500	ms

ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)}$ = 3.6V, T_A = −40°C to 85°C, typical values are at T_A = 25°C Battery charger specifications are valid in the range 0°C < T_A < 85°C unless otherwise noted

TEMPERATURE COMPARATOR						
$V_{(LTF)}$	Low (cold) temperature threshold		2.475	2.50	2.525	V
$V_{(HTF)}$	High (hot) temperature threshold		0.485	0.5	0.515	V
$I_{(TS)}$	TS current source		95	102	110	µA
	Deglitch time for temperature fault		250	375	500	ms
BATTERY RECHARGE THRESHOLD						
$V_{(RCH)}$	Recharge threshold	$V_{(CHG)}$min ≥ 4.5 V	$V_{O(REG)}$ –0.115	$V_{O(REG)}$ –0.1	$V_{O(REG)}$ –0.085	V
	Deglitch time	$V_{(CHG)}$min≥ 4.5 V, $V_{I(OUT)}$ decreasing below threshold; 100 ns fall time, 10 mV overdrive	250	375	500	ms
TIMERS						
$t_{(PRECHG)}$	Precharge timer	$V_{(CHG)}$min ≥ 4.5 V	1500	1800	2160	sec
$t_{(TAPER)}$	Taper timer	$V_{(CHG)}$min ≥ 4.5 V	1500	1800	2160	sec
$t_{(CHG)}$	Charge timer	$V_{(CHG)}$min ≥ 4.5 V	15000	18000	21600	sec
SLEEP AND STANDBY						
$V_{(SLP-ENTRY)}$	Sleep-mode entry threshold, /PG output = high	2.3 V ≤ $V_{I(OUT)}$ ≤ $V_{O(REG)}$			$V_{(CHG)}$ ≤ $V_{I(OUT)}$ +150 mV	V
$V_{(SLP\_EXIT)}$	Sleep-mode exit threshold, $\overline{PG}$ output = low	2.3 V ≤ $V_{I(OUT)}$ ≤ $V_{O(REG)}$	$V_{(CHG)}$ ≥ $V_{I(OUT)}$ +190 mV			V
	Deglitch time for sleep mode entry and exit	AC or USB decreasing below threshold; 100-ns fall time, 10-mV overdrive	250	375	500	ms
$t_{(USB\_DEL)}$	Delay between valid USB voltage being applied and start of charging process from USB			375		ms
CHARGER POWER-ON-RESET, UVLO, AND $V_{(IN)}$ RAMP RATE						
$V_{(CHGUVLO)}$	Charger under-voltage lockout	$V_{(CHG}$ decreasing	2.27	2.5	2.75	V
	Hysteresis			27		mV
$V_{(CHGOVLO)}$	Charger over-voltage lockout	$V_{(AC)}$ increasing		6.6		V
	Hysteresis			0.5		V
CHARGER OVER TEMPERATURE SUSPEND						
$T_{(suspend)}$	Temperature at which charger suspends operation			145		°C
$T_{(hyst)}$	Hysteresis of suspend threshold			20		°C

(1) $I_{O(AC)} = \dfrac{KSET \times V_{(SET)}}{R_{(ISET)}}$

(2) $I_{(PRECHG)} = \dfrac{KSET \times V_{(SET\_PRECHG)}}{R_{(ISET)}}$

(3) $I_{(TAPER)} = \dfrac{KSET \times V_{(SET\_TAPER)}}{R_{(ISET)}}$

(4) $I_{(TERM)} = \dfrac{KSET \times V_{(SET\_TERM)}}{R_{(ISET)}}$

ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)}$ = 3.6V, T_A = −40°C to 85°C, typical values are at T_A = 25°C Battery charger specifications are valid in the range 0°C < T_A < 85°C unless otherwise noted

Logic Signals DEFMAIN, DEFCORE, PS_SEQ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	I_{IH} = 20 µA	V_{CC}−0.5		V_{CC}	V
V_{IL}	Low level input voltage	I_{IL} = 10 µA	0		0.4	V
I_{IB}	Input bias current			0.01	1.0	µA

Logic Signals GPIO1−4

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	I_{OL} = 1 mA, configured as an open drain output			0.3	V
V_{OH}	High level output voltage	Configured as an open drain output			6	V
V_{IL}	Low level input voltage				V_{CC} x 0.2	V
V_{IH}	High level input voltage		V_{CC} x 0.7			V
I_I	Input leakage current				1	µA
$r_{SD(on)}$	Internal NMOS	V_{OL}= 0.3 V		150		Ω

Logic Signals $\overline{PG}$, LED2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	I_{OL} = 20 mA			0.5	V
V_{OH}	High level output voltage				6	V
$V_{(\overline{PG})}$	$\overline{PG}$ threshold voltage USB and AC		$V_{(BAT)}$ + xx mV			V

Vibrator Driver VIB

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	I_{OL} = 100 mA		0.3	0.5	V
V_{OH}	High level output voltage				6	V

Thermal Shutdown

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{(SD)}$	Thermal shutdown	Increasing junction temperature		160		°C

Undervoltage Lock Out

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(UVLO)}$	Undervoltage lockout threshold	$V_{(UVLO)}$ 2.5 V	Filter resistor = 10R in series with V_{CC}, V_{CC} decreasing	−3%		3%	
		$V_{(UVLO)}$ 2.75 V		−3%		3%	
		$V_{(UVLO)}$ 3.0 V		−3%		3%	
	Default value	$V_{(UVLO)}$ 3.25 V		−3%		3%	
$V_{(UVLO\_HYST)}$	UVLO comparator hysteresis		V_{CC} rising	150		200	mV

Power Good

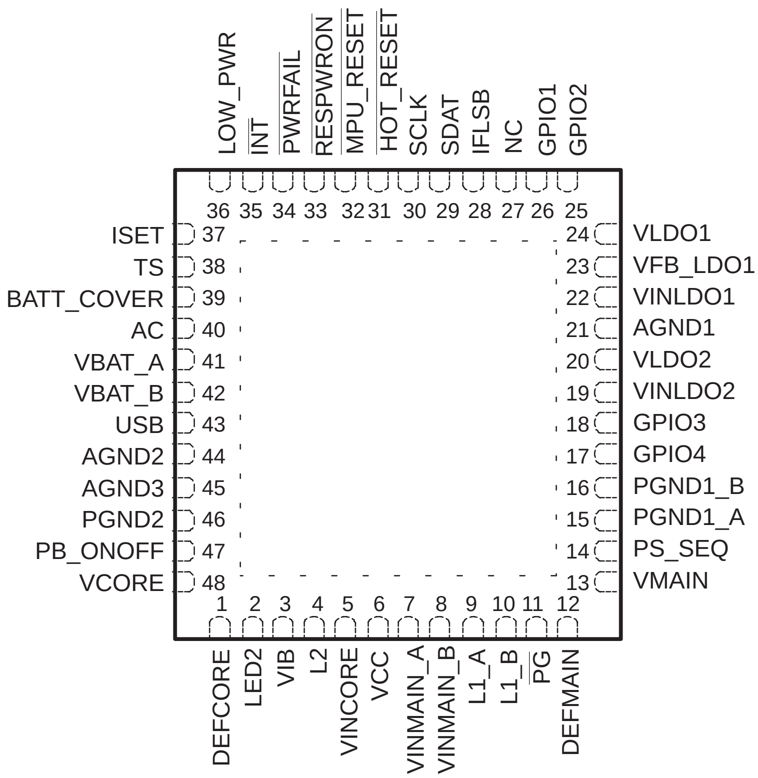
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PGOODF)}$	VMAIN, VCORE, VLDO1, VLDO2 decreasing	−12%	−10%	−8%	
$V_{(PGOODR)}$	VMAIN, VCORE, VLDO1, VLDO2 increasing	−7%	−5%	−3%	

SERIAL INTERFACE TIMING REQUIREMENTS

	MIN	MAX	UNIT
Clock frequency, f_{MAX}		400	kHz
Clock high time, $t_{wH(HIGH)}$	600		ns
Clock low time, $t_{wL(LOW)}$	1300		ns
DATA and CLK rise time, t_R		300	ns
DATA and CLK fall time, t_F		300	ns
Hold time (repeated) START condition (after this period the first clock pulse is generated), $t_{h(STA)}$	600		ns
Setup time for repeated START condition, $t_{h(DATA)}$	600		ns
Data input hold time, $t_{h(DATA)}$	0		ns
Data input setup time, $t_{su(DATA)}$	100		ns
STOP condition setup time, $t_{su(STO)}$	600		ns
Bus free time, $t_{(BUF)}$	1300		ns

PIN ASSIGNMENTS

RGZ PACKAGE
(TOP VIEW)



NC − No internal connection

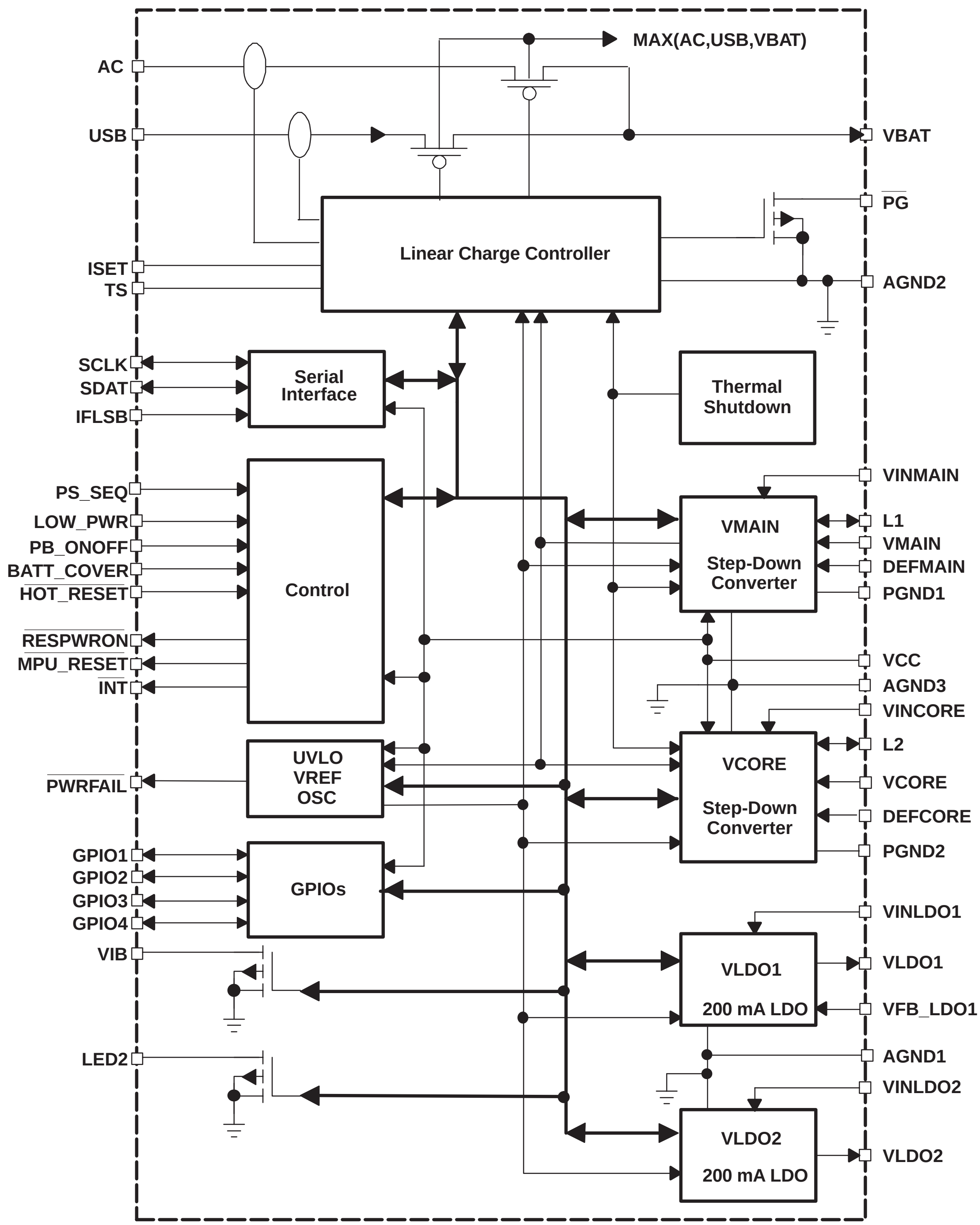
Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CHARGER SECTION			
AC	40	I	Charger input voltage from ac adapter
USB	43	I	Charger input voltage from USB port
ISET	37	I	External charge current setting resistor connection for use with ac adapter
VBAT_A, VBAT_B	41,42	I/O	Charge current output and battery voltage sense input

TS	38	I	Battery temperature sense input
$\overline{\text{PG}}$	11	O	Indicates when a valid power supply is present for the charger (open drain)
AGND2	44		Analog ground connection. All analog ground pins are connected internally on the chip.
SWITCHING REGULATOR SECTION			
AGND3	45		Analog ground connection. All analog ground pins are connected internally on the chip.
VINMAIN_A, VINMAIN_B	7,8	I	Input voltage for VMAIN step-down converter. This must be connected to the same voltage supply as VINCORE and VCC.
L1_A, L1_B	9,10		Switch pin of VMAIN converter. The VMAIN inductor is connected here.
VMAIN	13	I	VMAIN feedback voltage sense input, connect directly to VMAIN
VCC	6	I	Power supply for digital and analog circuitry of MAIN and CORE dc-dc converters. This must be connected to the same voltage supply as VINCORE and VINMAIN. Also supplies serial interface block
PGND1_A, PGND1_B	15,16		Power ground for VMAIN converter
VINCORE	5	I	Input voltage for VCORE step-down converter. This must be connected to the same voltage supply as VINMAIN and VCC.
L2	4		Switch pin of VCORE converter. The VCORE inductor is connected here.
VCORE	48	I	VCORE feedback voltage sense input, connect directly to VCORE
PGND2	46		Power ground for VCORE converter
LDO REGULATOR SECTION			
AGND1	21		Analogue ground connection. All analog ground pins are connected internally on the chip.
VINLDO1	22	I	Input voltage for LDO1
VLDO1	24	O	Output voltage for LDO1
VFB_LDO1	23	I	Feedback input from external resistive divider for LDO1
VINLDO2	19	I	Input voltage for LDO2
VLDO2	20	O	Output and feedback voltage for LDO2
DRIVER SECTION			
LED2	2	O	LED driver, with blink rate programmable via serial interface
VIB	3	O	Vibrator driver, enabled via serial interface
CONTROL AND I2C SECTION			
PS_SEQ	14	I	Sets power-up/down sequence of step-down converters
PB_ONOFF	47	I	Push button enable pin, also used to wake-up processor from *low power* mode
BATT_COVER	39	I	Indicates if battery cover is in place
$\overline{\text{HOT\_RESET}}$	31	I	Push button reset input used to reboot or wake-up processor via TPS65010
$\overline{\text{MPU\_RESET}}$	32	O	Open drain reset output generated by user activated $\overline{\text{HOT\_RESET}}$
$\overline{\text{RESPWRON}}$	33	O	Open drain system reset output, generated according to the state of the LDO1 output voltage
$\overline{\text{PWRFAIL}}$	34	O	Open drain output. Active low when UVLO comparator indicates low VBAT condition or when shutdown is about to occur due to an over temperature condition or when the battery cover is removed (BATT_COVER has gone low).
$\overline{\text{INT}}$	35	O	Indicates a charge fault or termination, or if any of the regulator outputs are below the lower tolerance level, active low (open drain)
LOW_PWR	36	I	Input signal indicating deep sleep mode, VCORE is lowered to predefined value or disabled
DEFMAIN	12	I	Input signal indicating default VMAIN voltage, 0 = 3.0 V, 1 = 3.3 V
DEFCORE	1	I	Input signal indicating default VCORE voltage, 0 = 1.5 V, 1 = 1.6 V
SCLK	30	I	Serial interface clock line
SDAT	29	I/O	Serial interface data/address
IFLSB	28	I	LSB of serial interface address used to distinguish two devices with the same address
GPIO1	26	I/O	General-purpose open-drain input/output
GPIO2	25	I/O	General-purpose open-drain input/output

GPIO3	18	I/O	General-purpose open-drain input/output
GPIO4	17	I/O	General-purpose open-drain input/output

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Efficiency	vs Output current	1−4
Quiescent current	vs Input voltage	5
Switching frequency	vs Temperature	6
Output voltage	vs Output current	7, 8
LDO1 Output voltage	vs Output current	9
LDO2 Output voltage	vs Output current	10
Line transient response (main)		11
Line transient response (core)		12
Line transient response (LDO1)		13
Line transient response (LDO2)		14
Load transient response (main)		15
Load transient response (core)		16
Load transient response (LDO1)		17
Load transient response (LDO2)		18
Output Voltage Ripple (PFM)		19
Output Voltage Ripple (PWM)		20
Startup timing		21
Dropout voltage	vs Output current	22, 23
PSRR (LDO1 and LDO2)	vs Frequency	24

EFFICIENCY vs OUTPUT CURRENT

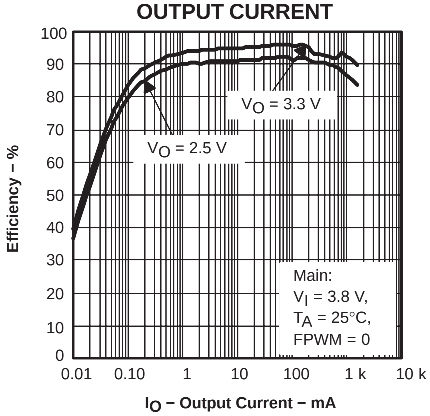


Figure 1

EFFICIENCY vs OUTPUT CURRENT

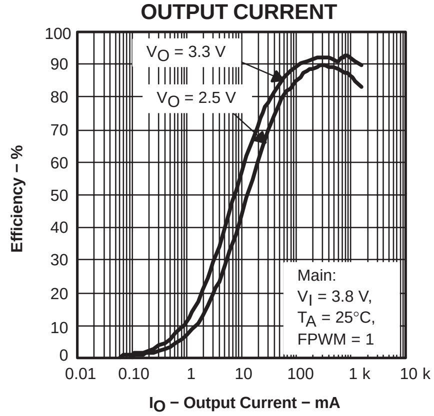


Figure 2

EFFICIENCY vs OUTPUT CURRENT

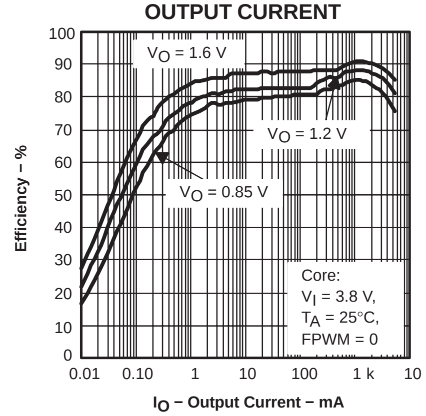


Figure 3

TYPICAL CHARACTERISTICS

EFFICIENCY vs OUTPUT CURRENT

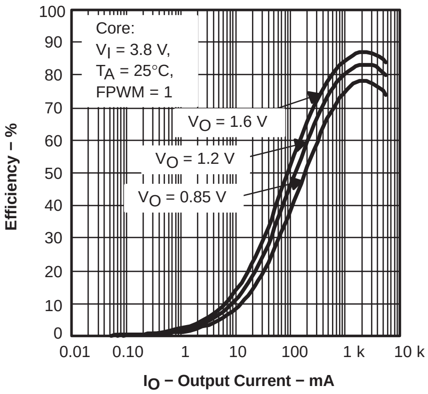


Figure 4

QUIESCENT CURRENT vs INPUT VOLTAGE

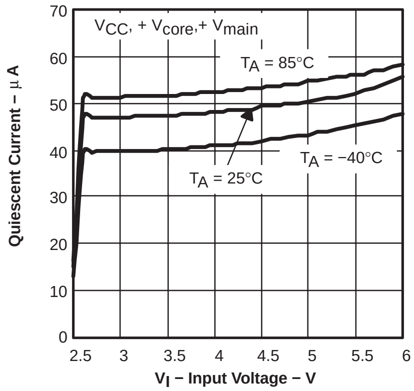


Figure 5

SWITCHING FREQUENCY vs TEMPERATURE

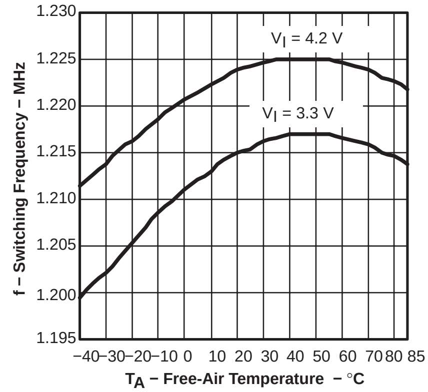


Figure 6

OUTPUT VOLTAGE vs OUTPUT CURRENT

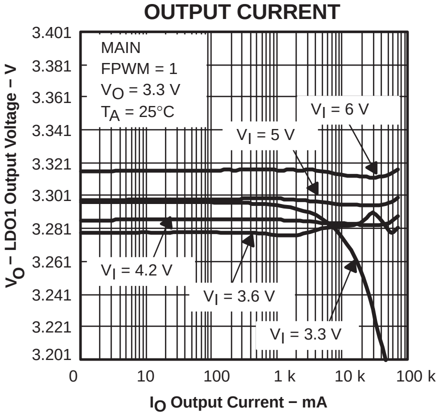


Figure 7

OUTPUT VOLTAGE vs OUTPUT CURRENT

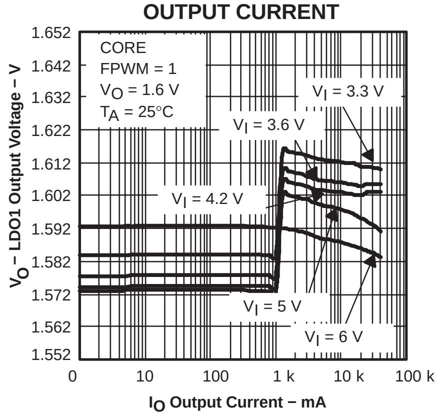


Figure 8

LDO1 OUTPUT VOLTAGE vs OUTPUT CURRENT

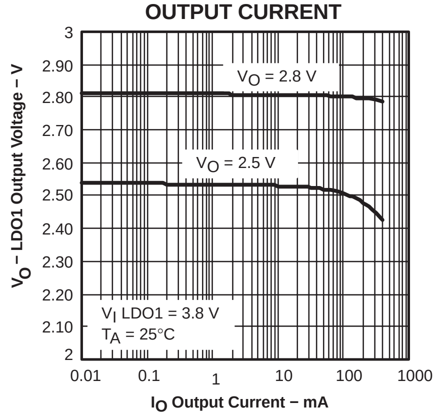


Figure 9

LDO2 OUTPUT VOLTAGE vs OUTPUT CURRENT

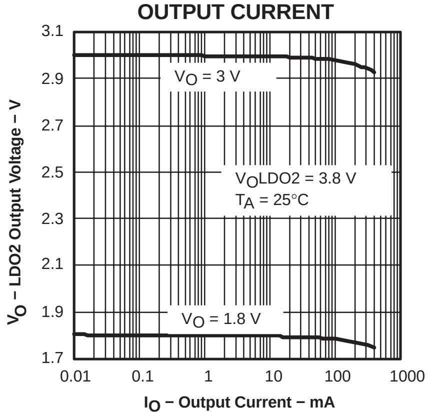


Figure 10

LINE TRANSIENT RESPONSE (MAIN)

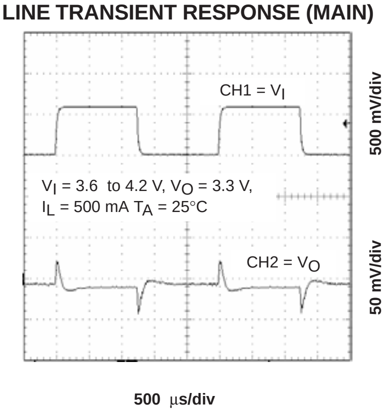


Figure 11

LINE TRANSIENT RESPONSE (CORE)

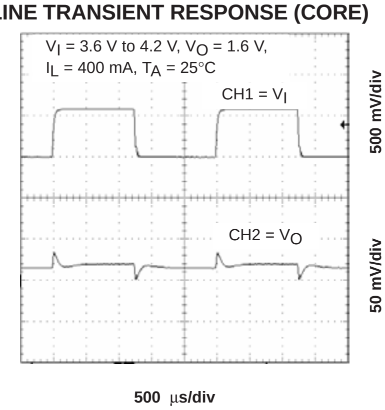


Figure 12

TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE (LDO1)

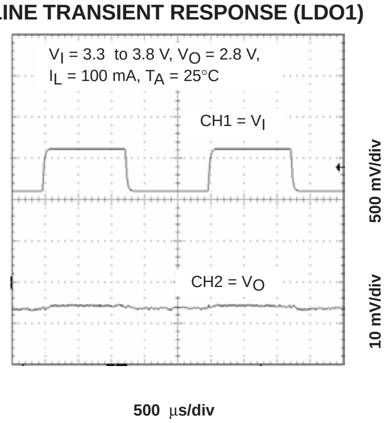


Figure 13

LINE TRANSIENT RESPONSE (LDO2)

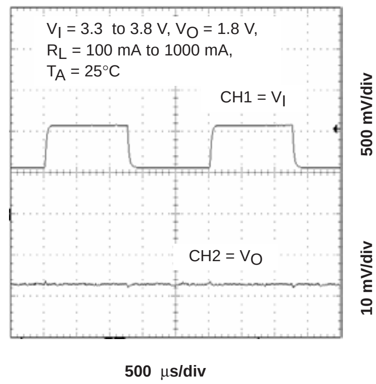


Figure 14

LOAD TRANSIENT RESPONSE (CORE)

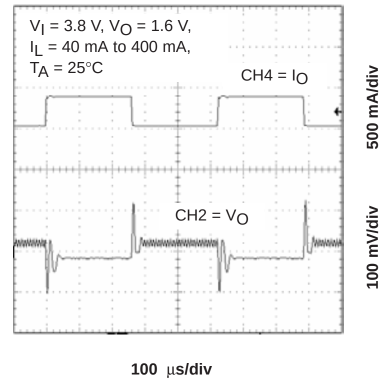


Figure 15

LOAD TRANSIENT RESPONSE (MAIN)

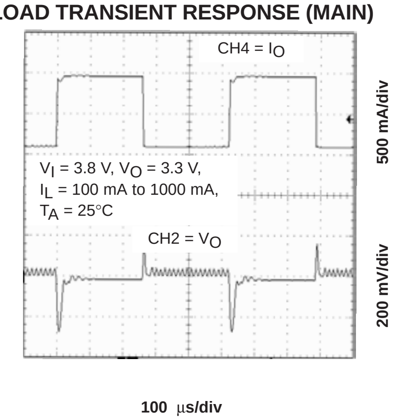


Figure 16

LOAD TRANSIENT RESPONSE (LDO1)

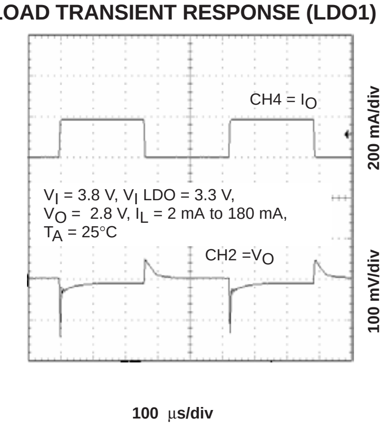


Figure 17

LOAD TRANSIENT RESPONSE (LDO2)

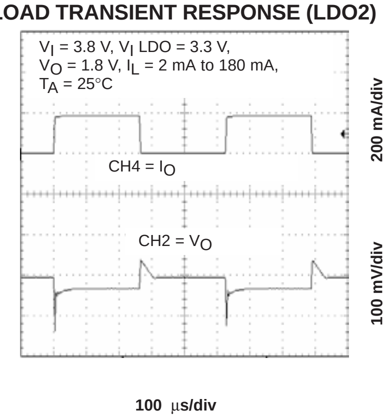
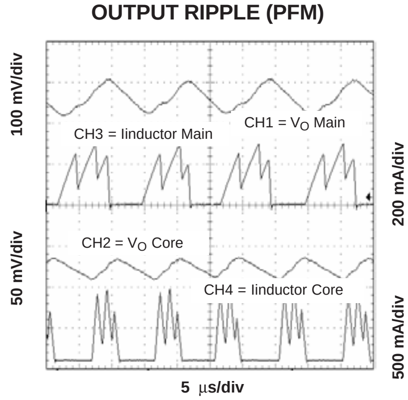


Figure 18

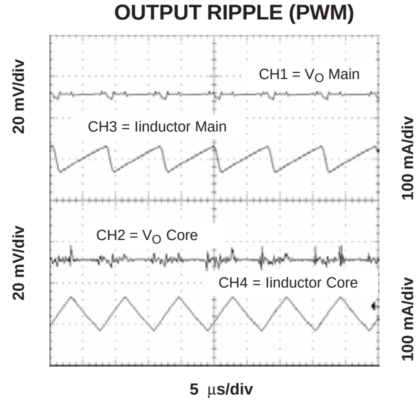
OUTPUT RIPPLE (PFM)



V_I = 3.8 V, T_A = 25°C
V_O Main = 3.3 V I_L Main = 100 mA,
V_O Core = 1.6 V, I_L Core = 40 mA

Figure 19

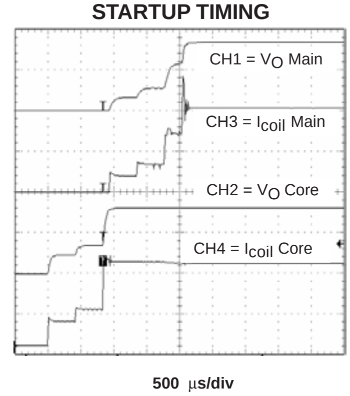
OUTPUT RIPPLE (PWM)



V_I = 3.8 V, T_A = 25°C
V_O Main = 3.3 V R_L Main = 500 mA,
V_O Core = 1.6 V, R_L Core = 400 mA

Figure 20

STARTUP TIMING



V_I = 3.8 V, V_O Main = 3.3 V,
R_L Main = 1 A, V_O Core = 1.6 V,
R_L Core = 400 mA, T_A = 25°C

Figure 21

TYPICAL CHARACTERISTICS

DROPOUT VOLTAGE vs OUTPUT CURRENT

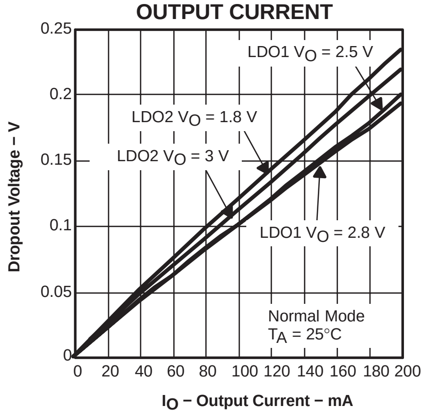


Figure 22

DROPOUT VOLTAGE vs OUTPUT CURRENT

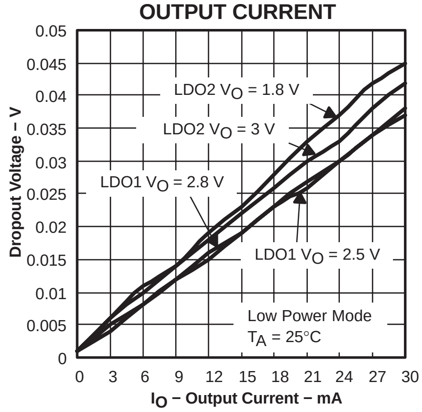


Figure 23

PSRR (LDO1, LDO2) vs FREQUENCY

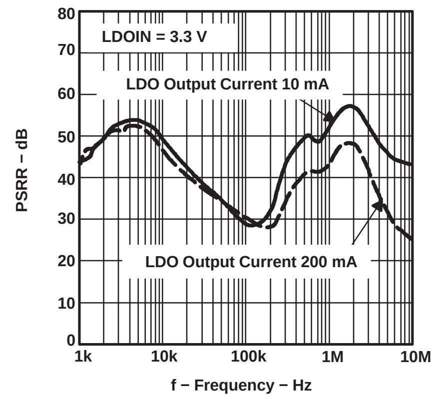


Figure 24

APPLICATION INFORMATION

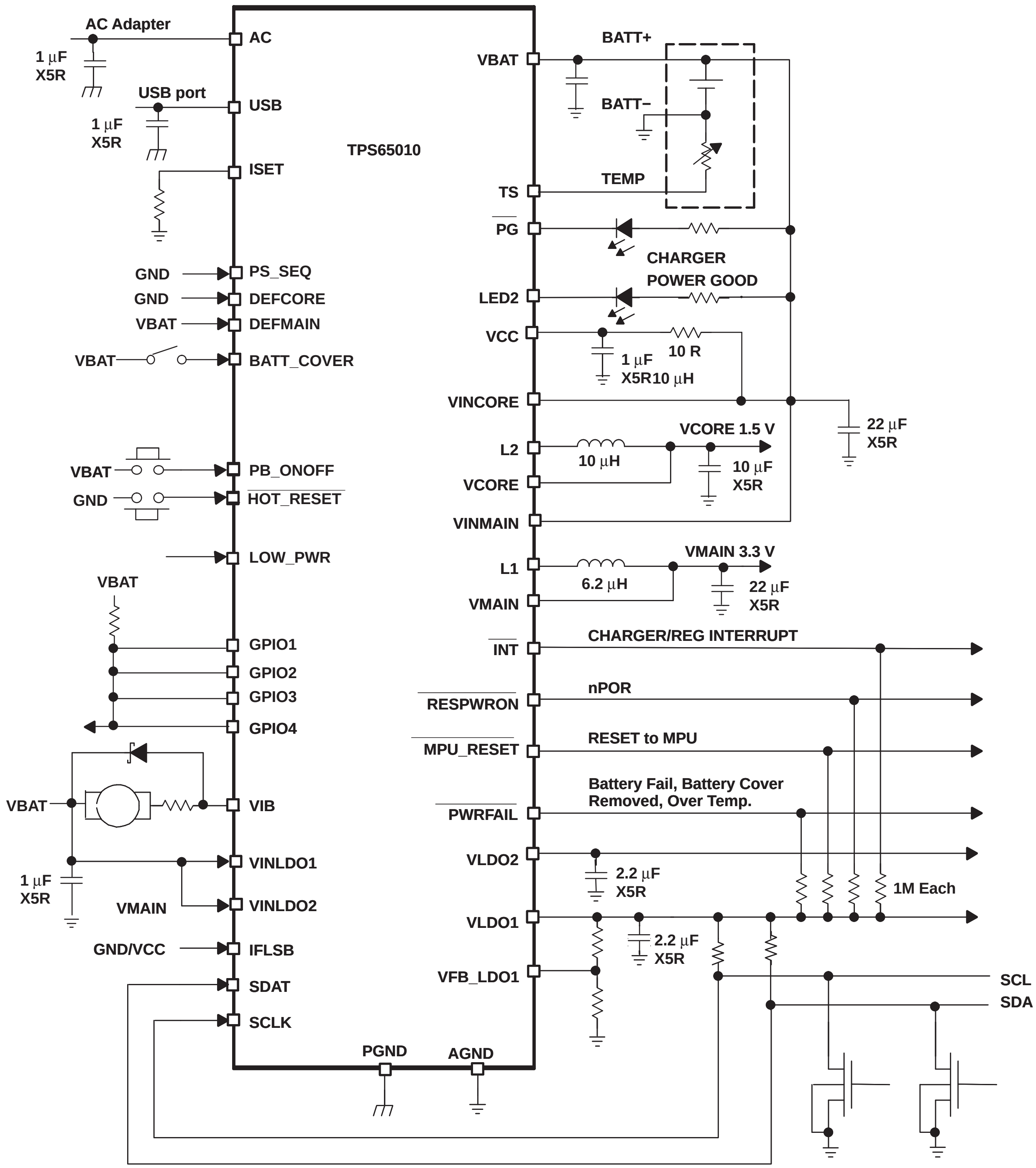


Figure 25. Typical Application Circuit

The VCORE and VMAIN converter are always enabled in a typical application. The VCORE output voltage can be disabled or reduced from 1.5 V to a lower, preset voltage under processor control. When the processor enters the sleep mode, a high signal on the LOW_PWR pin initiates the change

VCORE typically supplies the digital part of the audio codec. When the processor is in sleep or low power mode, the audio codec is powered off, so the VCORE voltage can be programmed to lower voltages without a problem. A typical audio codec (e.g., TI AIC23) consumes about 20-mA to 30-mA current from the VCORE power supply.

It is recommended to supply LDO1 from VMAIN as shown in Figure 25. If this is not done, then subsequent to a UVLO, OVERTEMP, or BATT_COVER =0 condition, the RESPWRON signal goes high before the VCORE rail has ramped and stabilized. Therefore, the processor core does not receive a power on reset signal.

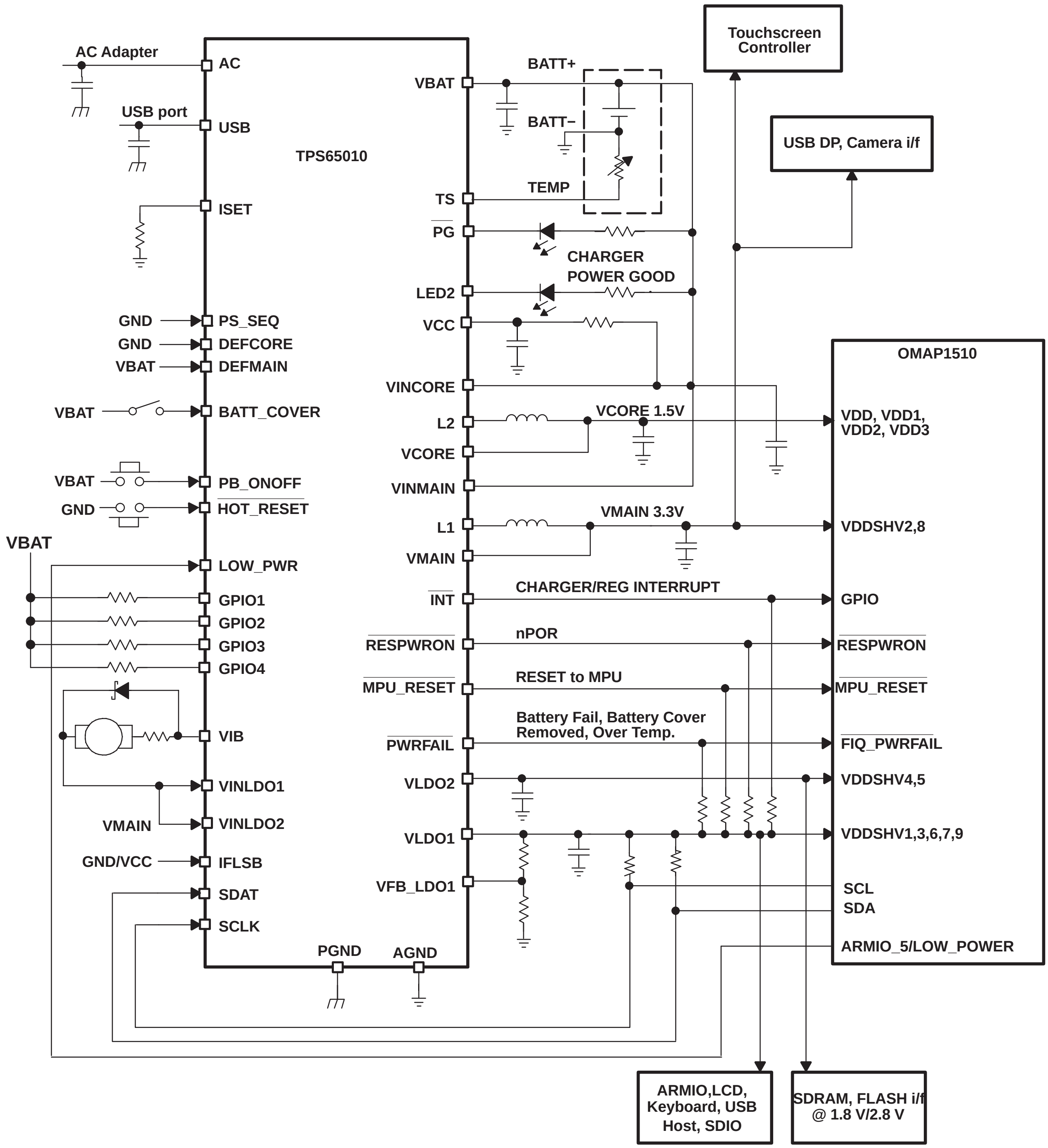


Figure 26. Typical Application Circuit in Low Power Mode

DETAILED DESCRIPTION

BATTERY CHARGER

The TPS65010 supports a precision Li-Ion or Li-Polymer charging system suitable for single-cells with either coke or graphite anodes. Charging the battery is possible even without the application processor being powered up. The TPS65010 starts charging when an input voltage on either ac or USB input is present, which is greater than the charger UVLO threshold. See Figure 27 for a typical charge profile.

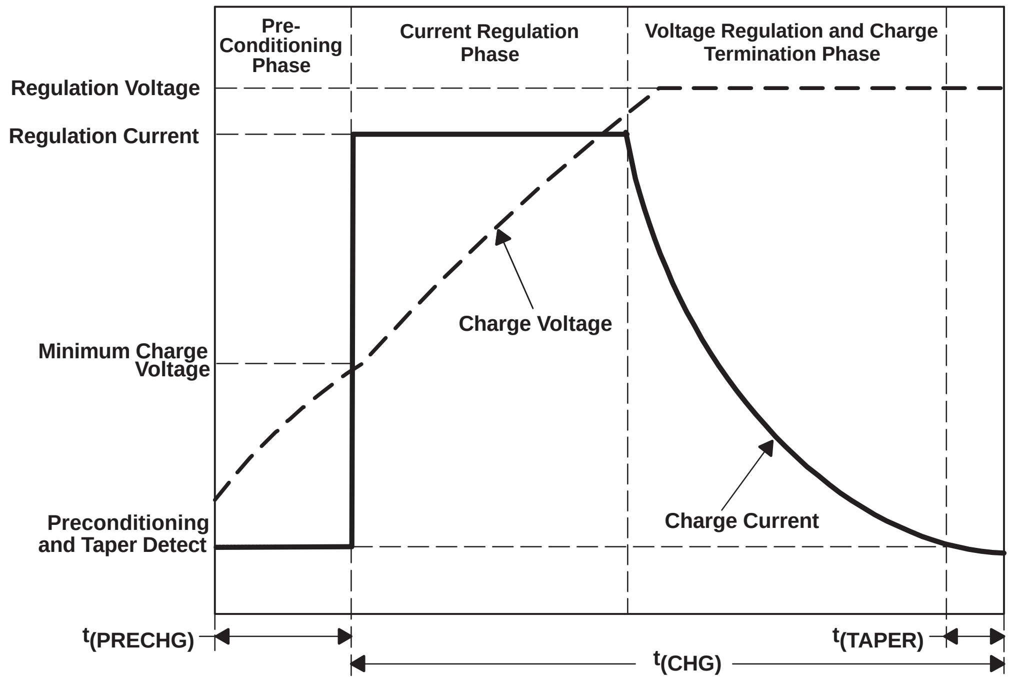


Figure 27. Typical Charging Profile

Autonomous Power Source Selection

Per default the TPS65010 attempts to charge from the ac input. If ac input is not present, the USB is selected. If both inputs are available, the ac input has priority. The charge current is initially limited to 100 mA when charging from the USB input. This can be increased to 500 mA via the serial interface. The charger can be completely disabled via the interface, and it is also possible just to disable charging from the USB port. The start of the charging process from the USB port is delayed in order to allow the application processor time to disable USB charging, for instance if a USB OTG port is recognized. The recommended input voltage for charging from the ac input is 4.5 V < VAC < 5.5 V. However, the TPS65010 is capable of withstanding (but not charging from) up to 20 V. Charging is disabled if VAC is greater than ca 6.6 V.

Temperature Qualification

The TPS65010 continuously monitors battery temperature by measuring the voltage between the TS and AGND pins. An internal current source provides the bias for most common 10K negative-temperature coefficient thermistors (NTC) (see Figure 28). The IC compares the voltage on the TS pin against the internal $V_{(LTF)}$ and $V_{(HTF)}$ thresholds to determine if charging is allowed. Once a temperature outside the $V_{(LTF)}$ and $V_{(HTF)}$ thresholds is detected the IC immediately suspends the charge. The IC suspends charge by turning off the powerFET and holding the timer value (i.e., timers are *not* reset). Charge is resumed when the temperature returns to the normal range.

The allowed temperature range for 103AT type thermistor is 0°C to 45°C. However the user may modify these thresholds by adding two external resistors. See Figure 29.

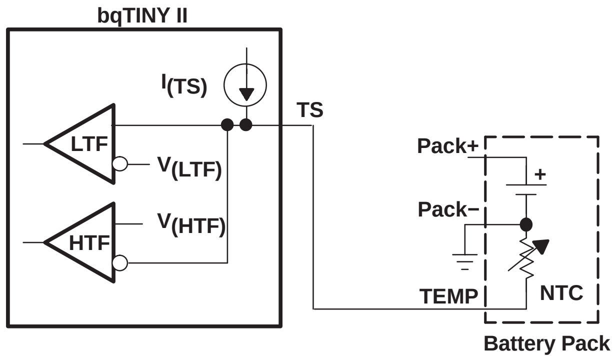


Figure 28. TS Pin Configuration

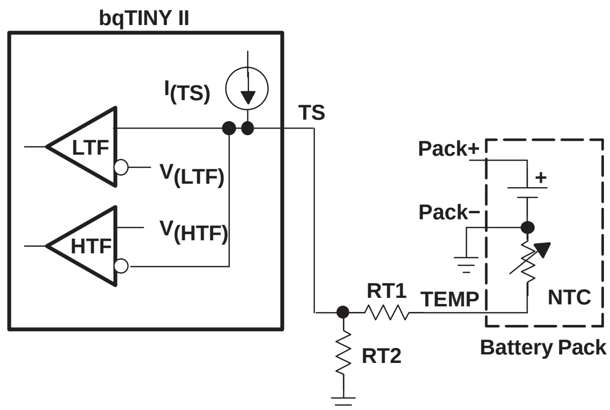


Figure 29. TS Pin Threshold

Battery Preconditioning

Upon power up, if the battery voltage is below the $V_{(LOWV)}$ threshold, the TPS65010 applies a precharge current, $I_{(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The charge current during this phase is one tenth of the value in current regulation phase which is set with $I_{O(out)}$ = KSET $\times$ $V_{(SET)}/R_{(SET)}$. The load current in preconditioning phase must be lower than $I_{(PRECHG)}$ and must allow the battery voltage to rise above $V_{(LOWV)}$ within $t_{(PRECHG)}$.

The TPS65010 activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the TPS65010 turns off the charger and indicates the fault condition in the CHGSTATUS register. In the case of a fault condition, the TPS65010 reduces the current to $I_{(DETECT)}$. $I_{(DETECT)}$ is used to detect a battery replacement condition. Fault condition is cleared by POR or battery replacement or via the serial interface.

Battery Charge Current

TPS65010 offers on-chip current regulation. When charging from an ac adapter, a resistor connected between the ISET1 and AGND pins determines the charge rate. A maximum of 1-A charger current from the ac adapter is allowed. When charging from a USB port either a 100-mA or 500-mA charge rate can be selected via the serial interface, default is 100 mA max. Two bits are available in the CHGCONFIG register in the serial interface to reduce the charge current in 25% steps. These only influence charging from the ac input and may be of use if charging is often suspended due to excessive junction temperature in the TPS65010 e.g., at high ac input voltages, and low battery voltages.

Battery Voltage Regulation

The voltage regulation feedback is through the VBAT pin. This pin is tied directly to the positive side of the battery pack. The TPS65010 monitors the battery-pack voltage between the VBAT and AGND pins. The TPS65010 is offered in a fixed-voltage version of 4.2 V.

As a safety backup, the TPS65010 also monitors the charge time in the fast-charge mode. If taper current is not detected within this time period, $t_{(CHG)}$, the TPS65010 turns off the charger and indicates FAULT in the CHGSTATUS register. In the case of a FAULT condition, the TPS65010 reduces the current to $I_{(DETECT)}$. $I_{(DETECT)}$ is used to detect a battery replacement condition. Fault condition is cleared by POR via the serial interface. Note that the safety timer is reset if the TPS65010 is forced out of the voltage regulation mode. The fast-charge timer is disabled by default to allow charging during normal operation of the end equipment. It is enabled via the CHGCONFIG register.

Charge Termination and Recharge

The TPS65010 monitors the charging current during the voltage regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected the TPS65010 initiates the taper timer, $t_{(TAPER)}$. Charge is terminated after the timer expires. The TPS65010 resets the taper timer in the event that the charge current returns above the taper threshold, $I_{(TAPER)}$. After a charge termination, the TPS65010 restarts the charge once the voltage on the VBAT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

In addition to the taper current detection, the TPS65010 terminates charge in the event that the charge current falls below the $I_{(TERM)}$ threshold. This feature allows for quick recognition of a battery removal condition.

Sleep Mode

The TPS65010 charger enters the low-power sleep mode if both input sources are removed from the circuit. This feature prevents draining the battery during the absence of input power.

$\overline{\text{PG}}$ Output

The open-drain power good ($\overline{\text{PG}}$) output indicates when a valid power supply is present for the charger. This can be either from the ac adapter input or from the USB. The output turns ON when a valid voltage is detected. A valid voltage is detected whenever the voltage on either pin AC or pin USB rises above the voltage on VBAT plus 100 mV. This output is turned off in the sleep mode. The $\overline{\text{PG}}$ pin can be used to drive an LED or communicate to the host processor. A voltage greater than the $V_{(CHGOVLO)}$ threshold (typ 6.6 V) at the AC input is not valid and does not activate the $\overline{\text{PG}}$ output

The $\overline{\text{PG}}$ output can also be programmed via the LED1_ON and LED1_PER registers in the serial interface. It can then be programmed to be permanently on, off, or to blink with defined on- and period-times. $\overline{\text{PG}}$ is controlled per default via the charger.

Thermal Considerations for Setting Charge Current

The TPS65010 is housed in a 48-pin QFN package with exposed leadframe on the underside. This 7 mm × 7 mm package exhibits a thermal impedance (junction-to-ambient) of 33 K/W when mounted on a JEDEC high-k board with zero air flow.

AMBIENT TEMPERATURE	MAX POWER DISSIPATION FOR T_J = 125°C	DERATING FACTOR ABOVE T_A = 55°C
25°C	3W	30 mW/°C
55°C	2.1W	

Consideration needs to be given to the maximum charge current when the assembled application board exhibits a thermal impedance, which differs significantly from the JEDEC high-k board. The charger has a thermal shutdown feature, which suspends charging if the TPS65010 junction temperature rises above a threshold of 145°C. This threshold is set 15°C below the threshold used to power down the TPS65010 completely.

STEP-DOWN CONVERTERS, VMAIN AND VCORE

The TPS65010 incorporates two synchronous step-down converters operating typically at 1.25 MHz fixed frequency pulse width modulation(PWM) at moderate to heavy load currents. At light load currents the converters automatically enter power save mode and operate with pulse frequency modulation (PFM). The main converter is capable of delivering 1-A output current and the core converter is capable of delivering 400 mA.

The converter output voltages are programmed via the VDCDC1 and VDCDC2 registers in the serial interface. The main converter defaults to 3.0-V or 3.3-V output voltage depending on the DEFMAIN configuration pin, if DEFMAIN is tied to ground the default is 3.0 V, if it is tied to V_{CC} the default is 3.3 V. The core converter defaults to either 1.5 V or 1.6 V depending upon whether the DEFCORE configuration pin is tied to GND or to V_{CC} respectively. Both the main and core output voltages can subsequently be reprogrammed after start-up via the serial interface. In addition, the LOW_PWR pin can be used either to lower the core voltage to a value defined in the VDCDC2 register when the application processor is in deep sleep mode or to disable the core converter. An active signal at LOW_PWR is ignored if the ENABLE_LP bit is not set in the VDCDC1 register.

The step-down converter outputs (when enabled) are monitored by power good comparators, the outputs of which are available via the serial interface. The outputs of the dc-dc converters can be optionally discharged when the dc-dc converters are disabled.

During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. After the dead time preventing current shoot through, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

The error amplifier, together with the input voltage, determines the rise time of the saw tooth generator, and therefore, any change in input voltage or output voltage directly controls the duty cycle of the converter giving a very good line and load transient regulation.

The two dc-dc converters operate synchronized to each other, with the MAIN converter as the master. A 270° phase shift between the MAIN switch turn on and the CORE switch turn on decreases the input RMS current and smaller input capacitors can be used. This is optimized for a typical application where the MAIN converter regulates a Li-Ion battery voltage of 3.7 V to 3.3 V and the CORE from 3.7 V to 1.5 V

Power Save Mode Operation

As the load current decreases, the converter enters the power save mode operation. During power save mode the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

In order to optimize the converter efficiency at light load the average current is monitored and if in PWM mode the inductor current remains below a certain threshold, then power save mode is entered. The typical threshold can be calculated as follows:

$$I_{(skipmain)} = \frac{V_{I(MAIN)}}{17\ \Omega} \qquad I_{(skipcore)} = \frac{V_{I(CORE)}}{42\ \Omega} \tag{1}$$

During the power save mode the output voltage is monitored with the comparator by the thresholds comp low and comp high. As the output voltage falls below the comp low threshold, set to typically 0.8% above the nominal V_{out}, the P-channel switch turns on. The converter then runs at 50% of the nominal switching frequency. If the load is below the delivered current then the output voltage rises until the comp high threshold is reached, typically 1.6% above the nominal Vout, whereupon all switching activity ceases, hence reducing the quiescent current to a minimum until the output voltage has dropped below comp low again. If the load current is greater than the delivered current, then the output voltage falls until it crosses the nominal output voltage threshold (comp low 2 threshold), whereupon power save mode is exited and the converter returns to PWM mode.

These control methods reduce the quiescent current to typically to 12-µA per converter and the switching frequency to a minimum achieving the highest converter efficiency. Setting the comparator thresholds to typically 0.8% and 1.6% above the nominal output voltage at light load current results in a dynamic voltage positioning achieving lower absolute voltage drops during heavy load transient changes. This allows the converters to operate with a small output capacitor of just 10 µF for the core and 22 µF for the main output and still have a low absolute voltage drop during heavy load transient changes. Refer to Figure 30 for detailed operation of the power save mode. The power save mode can be disabled through the I^2C interface to force the converters to stay in fixed frequency PWM mode.

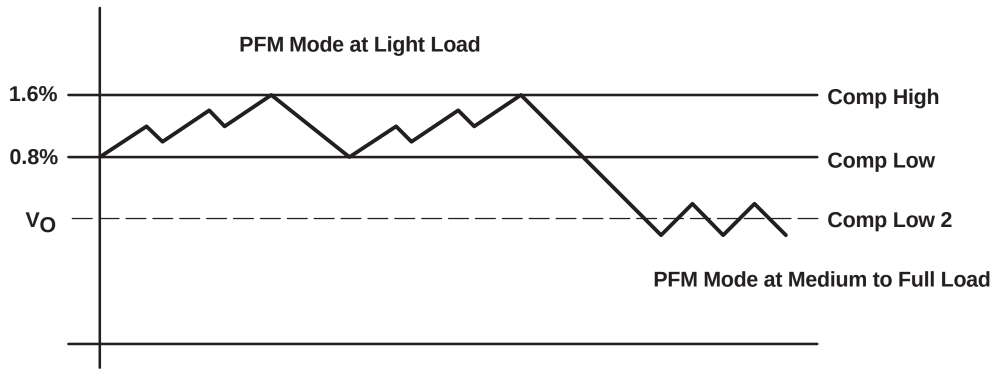


Figure 30. Power Save Mode Thresholds and Dynamic Voltage Positioning

Forced PWM

The core and main converters are forced into PWM mode by setting bit 7 in the VDCDC1 register. This feature is used to minimize ripple on the output voltages.

Dynamic Voltage Positioning

As described in the power save mode operation sections and as detailed in Figure 13, the output voltage is typically 1.2% above the nominal output voltage at light load currents as the device is in power save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. During a load transient from full load to light load the voltage overshoot is also minimized due to active regulation turning on the N-channel rectifier switch.

Soft Start

Both converters have an internal soft start circuit that limits the inrush current during start-up. The soft start is implemented as a digital circuit increasing the switch current in 4 steps up to the typical maximum switch current limit of 700 mA (core) and 1.75 A (main). Therefore, the start up time mainly depends on the output capacitor and load current.

100% Duty Cycle Low Dropout Operation

The TPS65010 converters offer a low input to output voltage difference while maintaining operation with the use of the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. i.e., The minimum input voltage to maintain regulation depends on the load current and output voltage and is calculated as:

$$V_{I(min)} = V_{O(max)} + I_{O(max)} \times \left(r_{DS(on)max} + R_L\right) \tag{2}$$

with:

$I_{O(max)}$ = maximum output current plus inductor ripple current

$r_{DS(on)max}$ = maximum P-channel switch r_{DSon}.

R_L = DC resistance of the inductor

$V_{O(max)}$ = nominal output voltage plus maximum output voltage tolerance

Active Discharge When Disabled

When the CORE and MAIN converters are disabled, due to an UVLO, BATT_COVER or OVERTEMP condition, it is possible to actively pull down the outputs. This feature is disabled per default and is individually enabled via the VDCDC1 and VDCDC2 registers in the serial interface. When this feature is enabled, the core and main outputs are discharged by a 400-Ω (typical) load.

Power Good Monitoring

Both the MAIN and CORE converters have power good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value, with 5% hysteresis. The outputs of these comparators are available in the REGSTATUS register via the serial interface. A maskable interrupt is generated when any voltage rail drops below the 10% threshold. The comparators are disabled when the converters are disabled.

Overtemperature Shutdown

The MAIN and CORE converters are automatically shut down if the temperature exceeds the trip point (see the electrical characteristics). This detection is only active if the converters are in PWM mode, either by setting FPWM = 1, or if the output current is high enough that the device runs in PWM mode automatically.

LOW-DROPOUT VOLTAGE REGULATORS

The low-dropout voltage regulators are designed to operate with low value ceramic input and output capacitors. They operate with input voltages down to 1.8 V. The LDOs offer a maximum dropout voltage of 300 mV at rated output current. Each LDO sports a current limit feature. Both LDOs are enabled per default, both LDOs can be disabled or programmed via the serial interface using the VREGS1 register. The LDO outputs (when enabled) are monitored by power good comparators, the outputs of which are available via the serial interface. The LDOs also have reverse conduction prevention when disabled. This allows the possibility to connect external regulators in parallel in systems with a backup battery.

Power Good Monitoring

Both the LDO1 and LDO2 linear regulators have power good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below it's target value, with 5% hysteresis. The outputs of these comparators are available in the REGSTATUS register via the serial interface. An interrupt is generated when any voltage rail drops below the 10% threshold. The LDO2 comparator is disabled when LDO2 is disabled. The LDO1 power good comparator is always active since it generates the system reset signal, $\overline{\text{RESPWRON}}$, see the System Reset and Control Signal Section below. This also allows the possibility to monitor VLDO1, even if it is provided by an external regulator.

Enable and Sequencing

Enabling and sequencing of the dc-dc converters and LDOs is described in the power-up sequencing section. The OMAP1510 processor from Texas Instruments requires that the core power supply is enabled before the I/O power supply, which means that the CORE converter should power up before the MAIN converter. This is achieved by connecting PS_SEQ to GND.

UNDER-VOLTAGE LOCKOUT

The undervoltage lockout circuit for the four regulators on TPS65010 prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. Basically it prevents the converter from turning on the power switch or rectifier FET under undefined conditions. The undervoltage threshold voltage is set by default to 3.25 V. After power-up, the threshold voltage can be reprogrammed through the serial interface. The undervoltage lockout comparator compares the voltage on the VCC pin with the UVLO threshold. When the VCC voltage drops below this threshold, the TPS65010 sets the $\overline{\text{PWRFAIL}}$ pin low and after a time $t_{(UVLO)}$ disables the voltage regulators in the sequence defined by PS_SEQ. The same procedure is followed when the TPS65010 detects that its junction temperature has exceeded the overtemperature threshold, typically 160°C, with a delay $t_{(overtemp)}$. The TPS65010 automatically restarts when the UVLO (or over temperature) condition is no longer present.

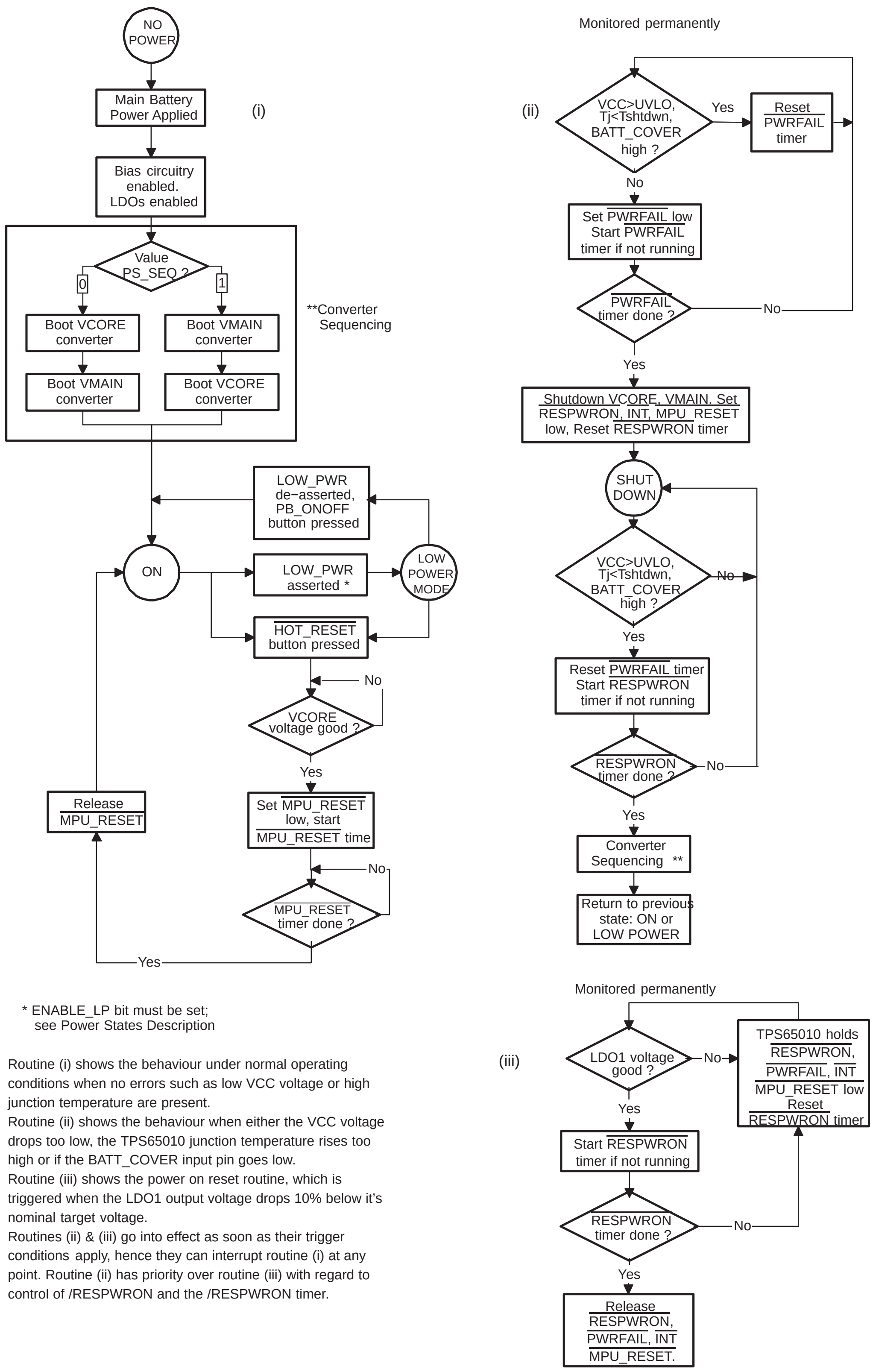
The battery charger circuit has a separate UVLO circuit with a threshold of typically 2.5 V, which is compared with the voltage on AC and USB supply pins.

POWER-UP SEQUENCING

The TPS65010 power-up sequencing is designed to allow the maximum flexibility without generating excessive logistical or system complexity. The relevant control pins are described in the following table:

PIN NAME	INPUT/ OUTPUT	FUNCTION
PS_SEQ	I	Input signal indicating power up and down sequence of the switching converters. PS_SEQ = 0 forces the core regulator to ramp up first and down last. PS_SEQ = 1 forces the main regulator to ramp up first and down last.
DEFCORE	I	Defines the default voltage of the VCORE switching converter. DEFCORE = 0 defaults VCORE to 1.5 V, DEFCORE = VCC defaults VCORE to 1.6 V.
DEFMAIN	I	Defines the default voltage of the VMAIN switching converter. DEFMAIN = 0 defaults VMAIN to 3.0 V, DEFMAIN = VCC defaults VMAIN to 3.3 V.
LOW_PWR	I	The LOW_PWR pin is used to lower VCORE to the preset voltage in the VDCDC2 register when the processor is in deep sleep mode. Alternatively VCORE can be disabled in low power mode if the LP_COREOFF bit is set in the VDCDC2 register. LOW_PWR is ignored if the ENABLE LP bit is not set in the VDCDC1 register. The TPS65010 uses the rising edge of the internal signal formed by a logical AND of LOW_PWR and ENABLE LP to enter low power mode. TPS65010 is forced out of low power mode by de-asserting LOW_PWR, by resetting ENABLE LP to 0, by activating the PB_ONOFF pin or by activating the $\overline{\text{HOT\_RESET}}$ pin. In the latter two cases it is necessary to take LOW_PWR low then high again in order to re-enter low power mode.
PB_ONOFF	I	PB_ONOFF can be used to exit the low power mode and return the core voltage to the value before low power mode was entered. If PB_ONOFF is used to exit low power mode, then LOW_PWR must first be taken low then high again in order to re−enter low power mode. A 1-MΩ pulldown resistor is integrated in TPS65010. PB_ONOFF is internally de-bounced by the TPS65010. A maskable interrupt is generated when PB_ONOFF is activated.
$\overline{\text{HOT\_RESET}}$	I	The $\overline{\text{HOT\_RESET}}$ pin has a very similar functionality to the PB_ONOFF pin. In addition it generates a reset ($\overline{\text{MPU\_RESET}}$) for the MPU when the VCORE voltage is in regulation. $\overline{\text{HOT\_RESET}}$ does not alter any TPS65010 settings unless low power mode was active in which case it is exited. A 1-MΩ pullup resistor to V_{CC} is integrated in TPS65010. $\overline{\text{HOT\_RESET}}$ is internally de-bounced by the TPS65010.
BATT_COVER	I	The BATT_COVER pin is used as an early warning that the main battery is about to be removed. BATT_COVER = V_{CC} indicates that the cover is in place, BATT_COVER = 0 indicates that the cover is not in place. TPS65010 generates a maskable interrupt when the BATT_COVER pin goes low. $\overline{\text{PWRFAIL}}$ is also held low when BATT_COVER goes low. This feature may be disabled, by tying BATT_COVER permanently to VCC. The TPS65010 shuts down all supplies $t_{(BATT\_COVER)}$ sec after BATT_COVER goes low. A 2-MΩ pulldown resistor is integrated in the TPS65010 at the BATT_COVER pin. BATT_COVER is internally de-bounced by the TPS65010.
$\overline{\text{RESPWRON}}$	O	$\overline{\text{RESPWRON}}$ is held low while the switching converters (and any LDO's defined as default on) are starting up. It is determined by the state of LDO1's output voltage; when this is good then $\overline{\text{RESPWRON}}$ is high, when VLDO1 is low then $\overline{\text{RESPWRON}}$ is low. $\overline{\text{RESPWRON}}$ is held low for $t_{n(RESPWRON)}$ sec after VLDO1 has settled.
$\overline{\text{MPU\_RESET}}$	O	$\overline{\text{MPU\_RESET}}$ can be used to reset the processor if the user activates the $\overline{\text{HOT\_RESET}}$ button. The $\overline{\text{MPU\_RESET}}$ output is active for $t_{(MPU\_nRESET)}$ sec. It also forces TPS65010 to leave low power mode. $\overline{\text{MPU\_RESET}}$ is also held low as long as $\overline{\text{RESPWRON}}$ is held low.
$\overline{\text{PWRFAIL}}$	O	$\overline{\text{PWRFAIL}}$ indicates when $V_{CC} < V_{(UVLO)}$, when the TPS65010 is about to shut down due to an internal overtemperature condition or when BATT_COVER is low. $\overline{\text{PWRFAIL}}$ is also held low as long as $\overline{\text{RESPWRON}}$ is held low.

Figure 31 shows the state diagram for the TPS65010 power sequencing. The charger function is not shown in the state diagram since this function is independent of these states.



* ENABLE_LP bit must be set;
see Power States Description

Routine (i) shows the behaviour under normal operating conditions when no errors such as low VCC voltage or high junction temperature are present.
Routine (ii) shows the behaviour when either the VCC voltage drops too low, the TPS65010 junction temperature rises too high or if the BATT_COVER input pin goes low.
Routine (iii) shows the power on reset routine, which is triggered when the LDO1 output voltage drops 10% below it's nominal target voltage.
Routines (ii) & (iii) go into effect as soon as their trigger conditions apply, hence they can interrupt routine (i) at any point. Routine (ii) has priority over routine (iii) with regard to control of /RESPWRON and the /RESPWRON timer.

Figure 31. TPS65010 Power-On State Diagram

TPS65010 Power States Description

State 1: No Power

There are no batteries connected to the TPS65010. When main power is applied, the bandgap reference, LDOs, and UVLO comparator start up. The RESPWRON, PWRFAIL, INT and MPU_RESET signals are held low. When BATT_COVER goes high (de-bounced internally by the TPS65010), indicating that the battery cover has been put in place and if VCC>UVLO, the power supplies are ramped in the sequence defined by PS_SEQ. RESPWRON, PWRFAIL, INT and MPU_RESET are released when the RESPWRON timer has timed out after $t_{n(RESPWRON)}$ sec. If VCC remains valid and no OVERTEMP condition occurs then the TPS65010 arrives in State 2: ON. If VCC<UVLO the TPS65010 keeps the bandgap reference and UVLO comparator active such that when VCC>UVLO (during battery charge) the supplies are automatically activated.

State2: ON

In this state, TPS65010 is fired up and ready to go. The switching converters can have their output voltages programmed, the LDOs can be disabled or programmed. TPS65010 can exit this state either due to an overtemperature condition, by an undervoltage condition at VCC, by BATT_COVER going low, or by the processor programming low power mode. State 2 is left temporarily if the user activates the HOT_RESET pin.

State 3: Low Power Mode

This state is entered via the processor setting the ENABLE_LP bit in the serial interface and then raising the LOW_PWR pin. The TPS65010 actually uses the rising edge of the internal signal formed by a logical AND of the LOW_PWR and ENABLE LP signals to enter low power mode. The VMAIN switching converter remains active, but the VCORE converter may be disabled in low power mode via the serial interface by setting the LP_COREOFF bit in the VDCDC2 register. If left enabled, the VCORE voltage is set to the value predefined by the CORELP0/1 bits in the VDCDC2 register. The LDO1OFF/nSLP and LDO2OFF/nSLP bits in the VREGS1 register determine whether the LDOs are turned off or put in a reduced power mode (transient speed-up circuitry disabled in order to minimize quiescent current) in low power mode. All TPS65010 features remain addressable via the serial interface. TPS65010 can exit this state either due to an under-voltage condition at VCC, due to BATT_COVER going low, due to an OVERTEMP condition, by the processor deasserting the LOW_POWER pin or by the user activating the HOT_RESET pin or the PB_ONOFF pin.

State4: Shutdown

This state is entered automatically when either the V_{CC} voltage is below UVLO the threshold, or if the TPS65010 junction temperature is too high, or if the BATT_COVER pins goes low. The shutdown state is left when the error condition no longer applies.

Table 1 indicates the typical quiescent current consumption in each power state.

Table 1. TPS65010 Typical Current Consumption

STATE	TOTAL QUIESCENT CURRENT	QUIESCENT CURRENT BREAKDOWN
1	0	
2	30 µA−70 µA	VMAIN (12 µA) + VCORE (12 µA) + LDOs (20 µA each, max 2) + UVLO + reference + PowerGood
3	30 µA−55 µA	VMAIN (12 µA) + VCORE (12 µA) + LDOs (10 µA each, max 2) + UVLO + reference + PowerGood
4	13 µA	UVLO + reference circuitry

Note that the figures for the VMAIN and the VCORE converters are at zero load, where almost no switching activity occurs. See the STEP-DOWN CONVERTER section for more information on efficiency versus load current.

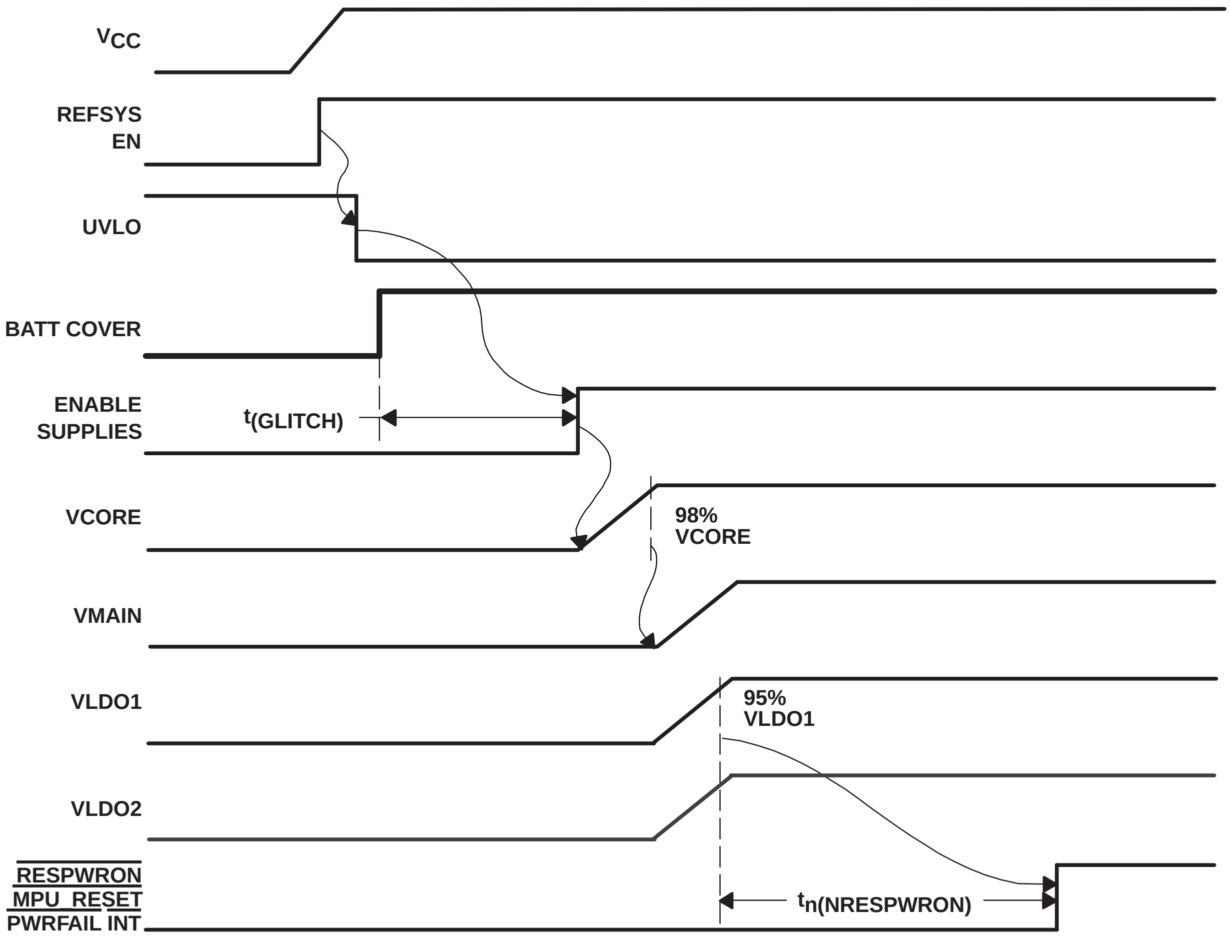


Figure 32. State 1 to State 2 Transition (PS_SEQ=0, V_{CC} > V_{UVLO} + HYST)

Valid for LDO1 supplied from VMAIN as described earilier in this *Application Section*.

If 2.4 ms after application, V_{CC} is still below the defaulrt UVLO threshold (3.425 V for V_{CC} rising), then start up is as shown in Figure 33.

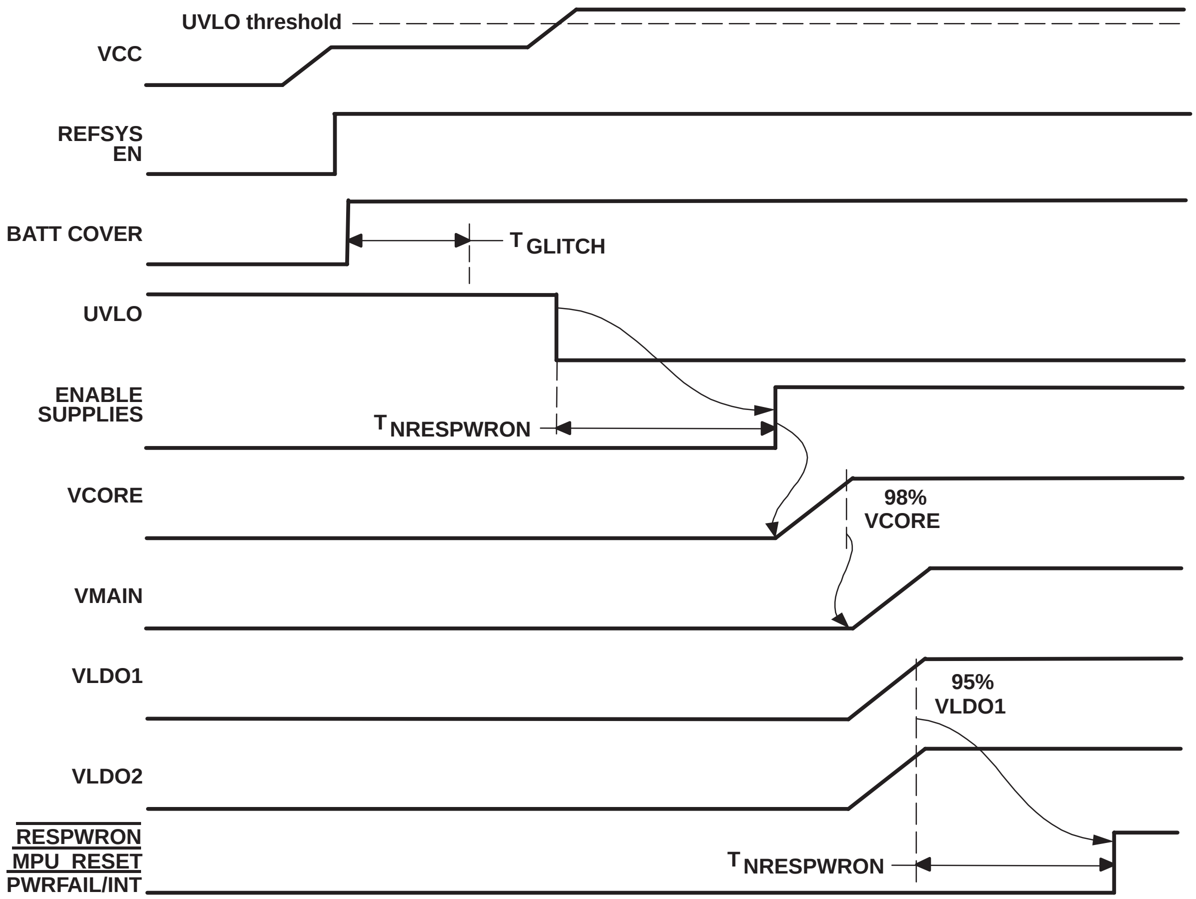


Figure 33. State1−State4−State 2 Transition (Power up behavior when V_{CC} ramp is longer than 2.4 ms)

Valid for LDO1 supplied from VMAIN as described earilier in this *Application Section*.

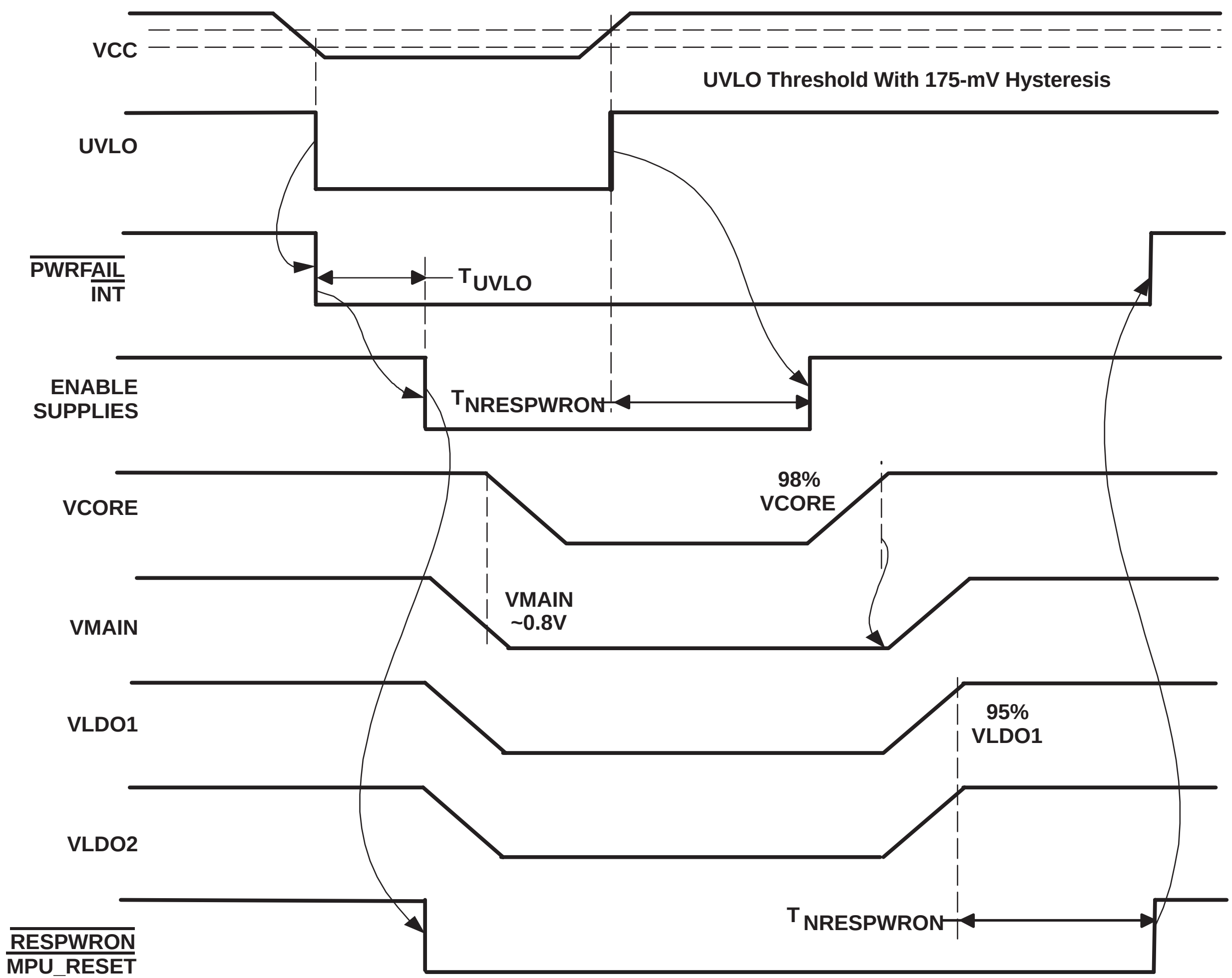


Figure 34. State2−State4−State 2 Transition

Valid for LDO1 supplied from VMAIN as described earilier in this *Application Section*.

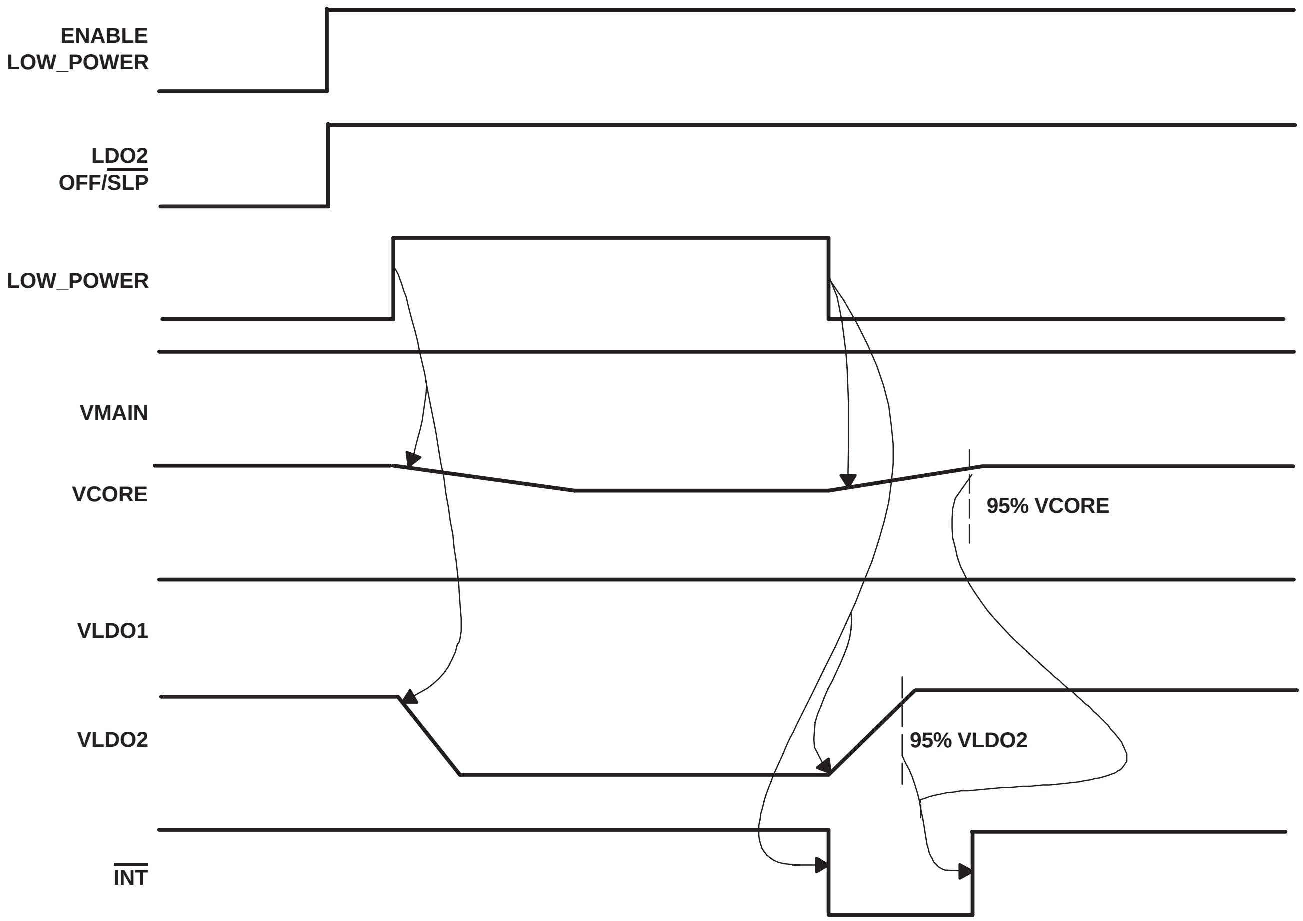


Figure 35. State 2 to State 3 Transition. VCORE Lowered, LDO2 Disabled. Subsequent State 3 to State 2 Transition When LOW POWER Is Deasserted.

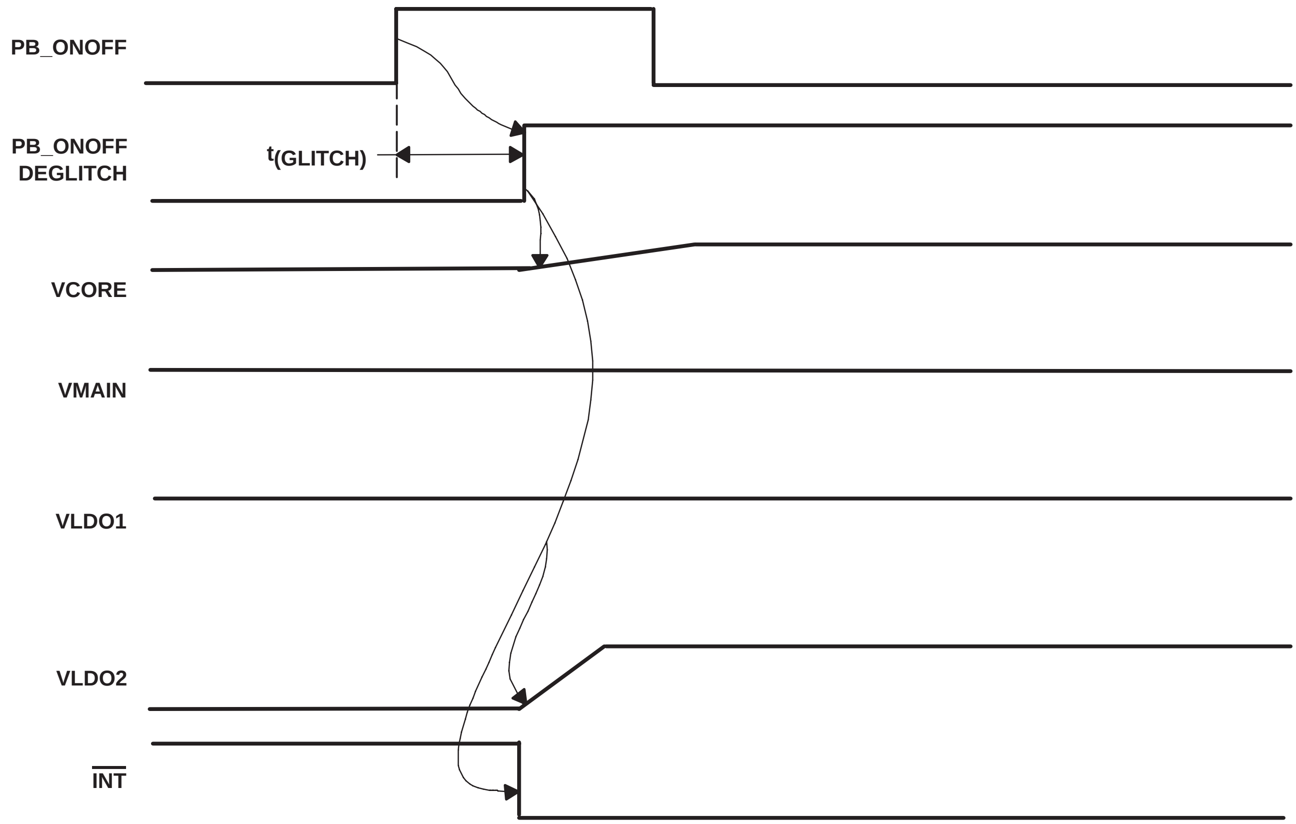


Figure 36. State 3 to State 2 Transition. PB_ONFF Activated (See Interrupt Management Section for $\overline{\text{INT}}$ Behavior)

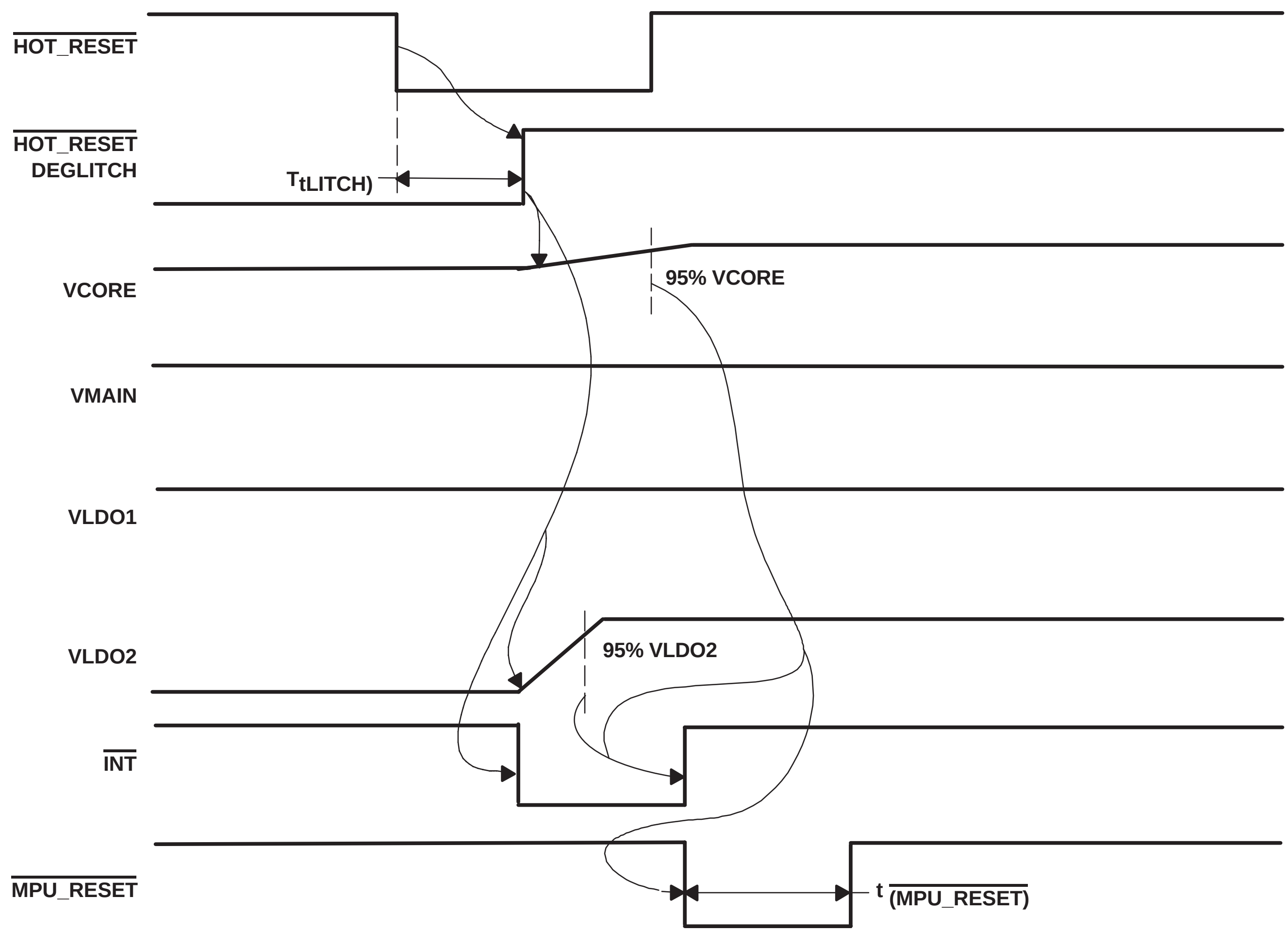


Figure 37. State 3 to State 2 Transition (HOT_RESET Activated, See Interrupt Management Section for INT Behaviour)

SYSTEM RESET AND CONTROL SIGNALS

The RESPWRON signal is used as a global reset for the application. It is an open drain output. The RESPWRON signal is generated according to the Power Good comparator linked to VLDO1 and remains low for $t_{n(RESPWRON)}$ sec after VLDO1 has stabilized. When RESPWRON is low, PWRFAIL, MPU_RESET and INT are also held low.

The PWRFAIL signal indicates when VCC < UVLO or when the TPS65010 junction temperature has exceeded a reliable value or if BATT_COVER is taken low. This open drain output can be connected at a fast interrupt pin for immediate attention by the application processor. All supplies are disabled $t_{(uvlo)}$, $t_{(overtemp)}$ or $t_{(batt\_cover)}$ sec after PWRFAIL has gone low, giving time for the application processor to shutdown cleanly.

BATT_COVER is used to detect whether the battery cover is in place or not. If the battery cover is removed, the TPS65010 generates a warning to the processor that the battery is likely to be removed and that it may be prudent to shut down the system. If not required, this feature may be disabled by connecting the BATT_COVER pin to the VCC pin. BATT_COVER is de-bounced internally. Typical de-bounce time is 56 ms. BATT_COVER has an internal 2-MΩ pull down.

The HOT_RESET input is used to generate an MPU_RESET signal for the application processor. The HOT_RESET pin could be connected to a user-activated button in the application. It can also be used to exit LOW POWER MODE, in this case the TPS65010 waits until the VCORE voltage has stabilized before generating the MPU_RESET pulse. The MPU_RESET pulse is active low for $t_{(mpu\_nreset)}$ sec. HOT_RESET has an internal 1-MΩ pull up to V_{CC}.

The PB_ONOFF input can be used to exit LOW POWER MODE. It is typically driven by a user-activated push-button in the application. Both $\overline{\text{HOT\_RESET}}$ and PB_ONOFF are de-bounced internally by the TPS65010. Typical de-bounce time is 56 ms. PB_ONOFF has an internal 1-MΩ pull down.

PB_ONOFF, BATT_COVER and UVLO events also cause a normal, maskable interrupt to be generated and are noted in the REGSTATUS register.

VIBRATOR DRIVER

The VIB open drain output is provided to drive a vibrator motor, controlled via the serial interface register VDCDC2. It has a maximum dropout of 0.5 V at 100-mA load. Typically an external resistor is required to limit the motor current, and a freewheel diode to limit the VIB overshoot voltage at turnoff.

LED2 OUTPUT

The LED2 output can be programmed in the same way as the $\overline{\text{PG}}$ output to blink or to be permanently on or off. The LED2_ON and LED2_PER registers are used to control the blink rate. For both $\overline{\text{PG}}$ and LED2, the minimum blink on time is 10 ms and this can be increased in 127 10 ms-steps to 1280 ms. For both $\overline{\text{PG}}$ and LED2, the minimum blink period is 100 ms and this can be increased in 127 100-ms steps to 12800 ms.

INTERRUPT MANAGEMENT

The open drain $\overline{\text{INT}}$ pin is used to combine and report all possible conditions via a single pin. Battery and chip temperature faults, precharge timeout, charge timeout, taper timeout and termination current are each capable of setting $\overline{\text{INT}}$ low, i.e. active. $\overline{\text{INT}}$ can also be activated if any of the regulators are below the regulation threshold. Interrupts can also be generated by any of the GPIO pins programmed to be inputs. These inputs can be programmed to generate an interrupt either at the rising or falling edge of the input signal. It is possible to mask an interrupt from any of these conditions individually by setting the appropriate bits in the MASK1, MASK2 or MASK3 registers. By default, all interrupts are masked. Interrupts are stored in the CHGSTATUS, REGSTATUS and DEFGPIO registers in the serial interface. CHGSTATUS and REGSTATUS interrupts are acknowledged by reading these registers. If a 1 is present in any location then the TPS65010 automatically sets the corresponding bit in the ACKINT1 or ACKINT2 registers and releases the $\overline{\text{INT}}$ pin. The ACKINT register contents are self-clearing when the condition, which caused the interrupt, is removed. The applications processor should not normally need to access the ACKINT1 or ACKINT2 registers.

Interrupt events are always captured; thus when an interrupt source is unmasked, $\overline{\text{INT}}$ may immediately go active due to a previous interrupt condition. This can be prevented by first reading the relevant STATUS register before unmasking the interrupt source.

If an interrupt condition occurs then the $\overline{\text{INT}}$ pin is set low. The CHGSTATUS, REGSTATUS and DEFGPIO registers should be read. Bit positions containing a 1 (or possibly a 0 in DEFGPIO) are noted by the CPU and the corresponding situation resolved. The reading of the CHGSTATUS and REGSTATUS registers automatically acknowledges any interrupt condition in those registers and blocks the path to the $\overline{\text{INT}}$ pin from the relevant bit(s). No interrupt should be missed during the read process since this process starts by latching the contents of the register before shifting them out at SDAT. Once the contents have been latched (takes a couple of nanoseconds), the register is free to capture new interrupt conditions. Hence the probability of missing anything is, for practical purposes, zero.

The following describes how registers 0x01 (CHGSTATUS) and 0x02 (REGSTATUS) are handled:

- CHGSTATUS(5,0) are positive edge set. Read of set CHGSTATUS(5,0) bits sets ACKINT1(5,0) bits.
- CHGSTATUS(7−6,4−1) are level set. Read of set CHGSTATUS(7−6,4−1) bits sets ACKINT1(7−6,4−1) bits.
- CHGSTATUS(5,0) clear when input signal low and ACKINT1(5,0) bits are already set.
- CHGSTATUS(7−6,4−1) clear when input signal is low.
- ACKINT1(7−0) clear when CHGSTATUS(7−0) is clear.

- REGSTATUS(7−5) are positive edge set. Read of set REGSTATUS(7−5) bits sets ACKINT2(7−5) bits.
- REGSTATUS(3−0) are level set. Read of set REGSTATUS(3−0) bits sets ACKINT2(3−0) bits.
- REGSTATUS(7−5) clear when input signal low and ACKINT1(7−5) bit are already set.
- REGSTATUS(3−0) clear when input signal is low.
- ACKINT2(7−0) clear when REGSTATUS(7−0) is clear.

The following describes the function of the 0x05 (ACKINT1) and 0x06 (ACKINT2) registers. These are not usually written to by the CPU since the TPS65010 internally sets/clears these registers:

- ACKINT1(7:0) – Bit is set when the corresponding CHGSTATUS set bit is read via I^{2}C.
- ACKINT1(7:0) – Bit is cleared when the corresponding CHGSTATUS set bit clears.
- ACKINT2(7:0) – Bit is set when the corresponding REGSTATUS set bit is read via I^{2}C.
- ACKINT2(7:0) – Bit is cleared when the corresponding REGSTATUS set bit clears.
- ACKINT1(7:0) – a bit set masks the corresponding CHGSTATUS bit from $\overline{\text{INT}}$.
- ACKINT2(7:0) – a bit set masks the corresponding REGSTATUS bit from $\overline{\text{INT}}$.

The following describes the function of the 0x03 (MASK1), 0x04 (MASK2) and 0x0F (MASK3) registers:

- MASK1(7:0) – a bit set in this register masks CHGSTATUS from $\overline{\text{INT}}$.
- MASK2(7:0) – a bit set in this register masks REGSTATUS from $\overline{\text{INT}}$.
- MASK3(7:4) – a bit set in this register detects a rising edge on GPIO.
- MASK3(7:4) – a bit cleared in this register detects a falling edge on GPIO.
- MASK3(3:0) – a bit set in this register clears GPIO Detect signal from $\overline{\text{INT}}$.

GPIO interrupts are located by reading the 0x10 (DEFGPIO) register. The application CPU stores, or can read from DEFGPIO<7:4>, which GPIO is set to input or output. This information together with the information on which edge the interrupt was generated (the CPU either knows this or can read it from MASK3<7:4>) determines whether the CPU is looking for a 0 or a 1 in DEFGPIO<3:0>. A GPIO interrupt is blocked from the $\overline{\text{INT}}$ pin by setting the relevant MASK3<3:0> bit; this must be done by the CPU, there is no auto-acknowledge for the GPIO interrupts.

SERIAL INTERFACE

The serial interface is compatible with the standard and fast mode I^{2}C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as V_{CC} remains above 2 V. The TPS65010 has a 7-bit address with the LSB set by the IFLSB pin, this allows the connection of two devices with the same address to the same bus. The 6 MSBs are 100100. Attempting to read data from register addresses not listed in this section results in FFh being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS65010 device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS65010 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS65010 device must leave the data line high to enable the master to generate the stop condition.

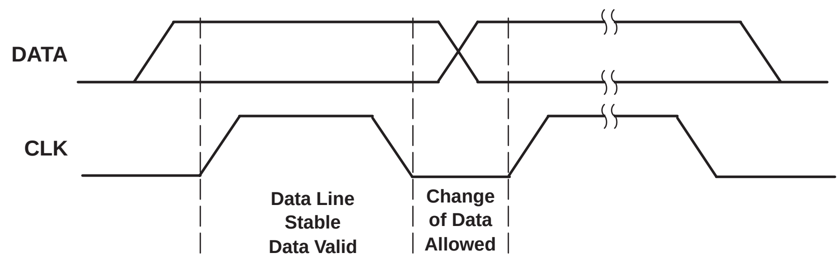


Figure 38. Bit Transfer on the Serial Interface

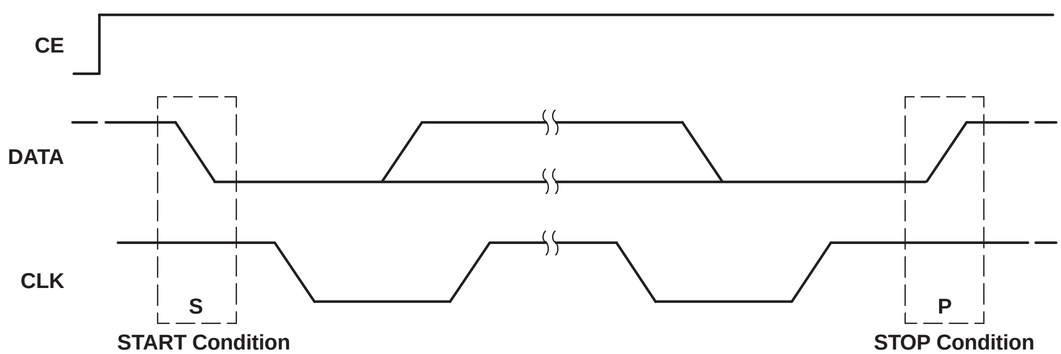
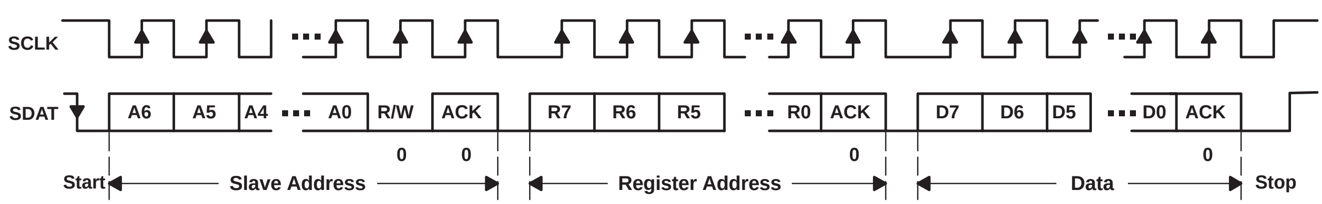
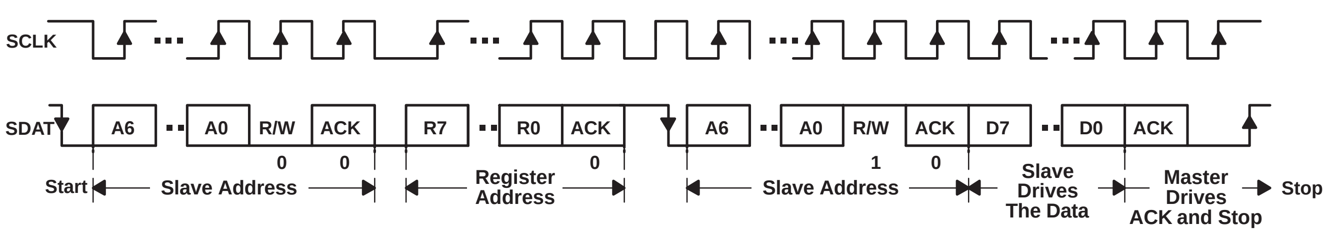


Figure 39. START and STOP Conditions



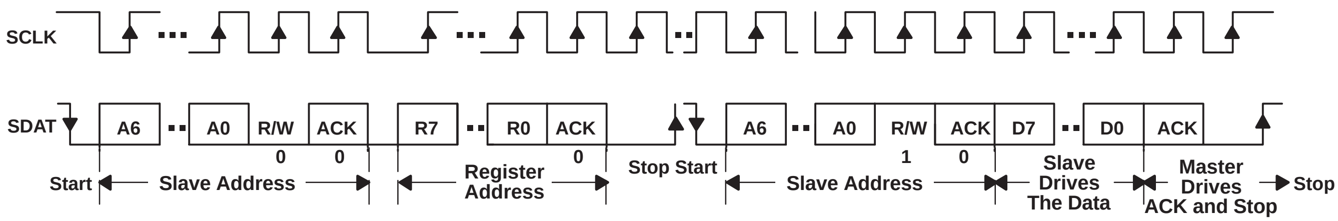
NOTE: SLAVE = TPS65010

Figure 40. Serial i/f WRITE to TPS65010 Device



NOTE: SLAVE = TPS65010

Figure 41. Serial i/f READ From TPS65010: Protocol A



NOTE: SLAVE = TPS65010

Figure 42. Serial i/f READ From TPS65010: Protocol B

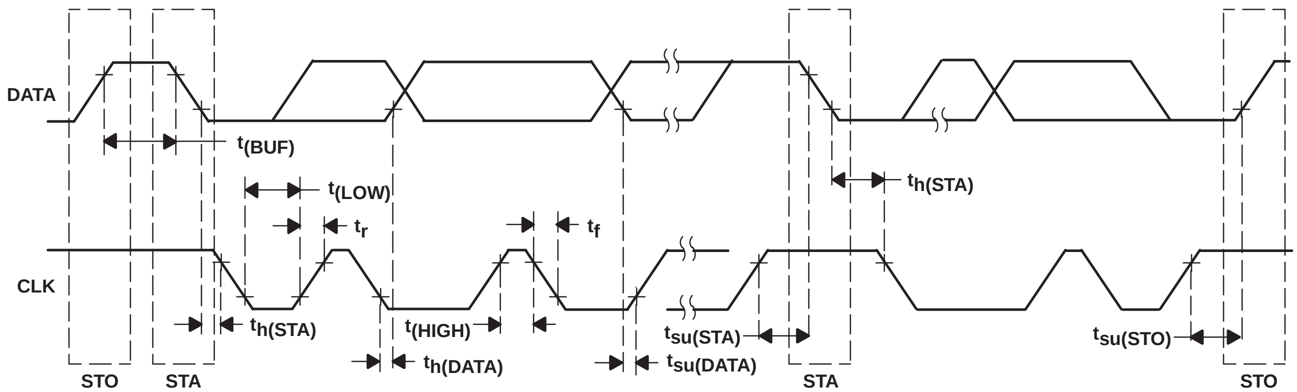


Figure 43. Serial i/f Timing Diagram

Internal Register Address: 01h—Default Value: 00h

CHGSTATUS	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	USB charge	AC charge	Thermal Suspend	Term Current	Taper Timeout	Chg Timeout	Prechg Timeout	BattTemp error
Default	0	0	0	0	0	0	0	0
Read/write	R	R	R	R	R/W	R/W	R/W	R/W

The CHGSTATUS register contents indicate the status of charge. B0=1 indicates that the battery temperature is outside of the allowed range and that charging is suspended. B1−3=1 indicates that one of the timers has timed out and charging has been terminated. B4=1 indicates that the charge termination current threshold has been crossed and charging has been terminated normally. B5=1 indicates that charging is momentarily suspended due to excessive power dissipation on chip. B6=1 indicates that the wall plug source is present and in the range valid for charging. B7=1 indicates that the USB source is present and in the range valid for charging. B6,7 remain active as long as the respective charge source is present. B1−4 may be reset via the serial interface in order to force a reset of the charger. Any attempt to write to B0 and B5−7 is ignored. A 1 in B<7:0> sets the $\overline{\text{INT}}$ pin active unless the corresponding bit in the MASK register is set.

Internal Register Address: 02h—Default Value: 00h

REGSTATUS	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	PB_ONOFF	BATT_COVER	UVLO		$\overline{\text{PGOOD}}$ LDO2	$\overline{\text{PGOOD}}$ LDO1	$\overline{\text{PGOOD}}$ MAIN	$\overline{\text{PGOOD}}$ CORE
Default	0	0	0	0	0	0	0	0
Read/write	R	R	R	R	R	R	R	R

REGSTATUS B0 to B3 indicates when any of VMAIN, VCORE or VLDO1,2 is out of regulation. This can be due to an overcurrent condition or if the input voltage to the particular regulator is less than the programmed output voltage. B5 indicates that the voltage at the VCC pin has dropped below the UVLO threshold. B6 indicates if the BATT_COVER pin has gone low. B7 indicates if the user activated the PB_ONOFF switch to request that all rails are shut down. A rising edge in the REGSTATUS register contents causes $\overline{\text{INT}}$ to be driven low if it is not masked in the MASK2 register.

Internal Register Address: 03h—Default Value: FFh

MASK1	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	Mask USB	Mask AC	Mask Thermal Suspend	Mask Term	Mask Taper	Mask Chg	Mask Prechg	Mask BattTemp
Default	1	1	1	1	1	1	1	1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The MASK1 register is used to mask all or any of the conditions in the corresponding CHGSTATUS<7:0> positions being indicated at the $\overline{\text{INT}}$ pin. Default is to mask all.

Internal Register Address: 04h—Default Value: FFh

MASK2	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	Mask PB_ONOFF	Mask BATT_COVER	Mask UVLO		Mask LDO2	Mask LDO1	Mask MAIN	Mask CORE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The MASK2 register is used to mask all or any of the conditions in the corresponding REGSTATUS<7:0> positions being indicated at the /INT pin. Default is to mask all.

Internal Register Address: 05h—Default Value: 00h

ACKINT1	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	Ack USB	Ack AC	Ack Thermal Shutdown	Ack Term	Ack Taper	Ack Chg	Ack Prechg	Ack BattTemp
Default	0	0	0	0	0	0	0	0
Read/write	R	R	R	R	R	R	R	R

The ACKINT1 register is internally used to acknowledge any of the interrupts in the corresponding CHGSTATUS<7:0> positions. When this is done, the acknowledged interrupt is no longer fed through to the $\overline{\text{INT}}$ pin, and so the $\overline{\text{INT}}$ pin becomes free to indicate the next pending interrupt. If none exists then the $\overline{\text{INT}}$ pin goes high, else it remains low. A 1 at any position in ACKINT1 is automatically cleared when the corresponding interrupt condition in CHGSTATUS is removed. The application processor should not normally need to access the ACKINT1 register.

Internal Register Address: 06h—Default Value: 00h

ACKINT2	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	Ack PB_ONOFF	Ack BATT_COVER	Ack UVLO		Ack LDO2	Ack LDO1	Ack MAIN	Ack CORE
Default	0	0	0	0	0	0	0	0
Read/write	R	R	R	R	R	R	R	R

The ACKINT2 register is internally used to acknowledge any of the interrupts in the corresponding REGSTATUS<7:0> positions. When this is done, the acknowledged interrupt is no longer fed through to the $\overline{\text{INT}}$ pin and so the $\overline{\text{INT}}$ pin becomes free to indicate the next pending interrupt. If none exists then the $\overline{\text{INT}}$ pin goes high, or else it remain lows. A 1 at any position in ACKINT2 is automatically cleared when the corresponding interrupt condition in REGSTATUS is removed. The application processor should not normally need to access the ACKINT2 register.

Internal Register Address: 07h—Default Value: 1Bh

CHGCONFIG	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	POR	Charger reset	Fast charge timer + taper timer enabled	MSB charge current	LSB charge current	USB/100 mA 500 mA	USB charge allowed	Charge enable
Default	0	0	0	1	1	0	1	1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The CHGCONFIG register is used to configure the charger. B0=1 indicates that the charger is free to charge from either of the two input sources. If both sources are present and valid, the TPS65010 charges from the ac source. B1=0 prevents any charging from the USB input. B2=0/1 sets the USB charging current to max 100 mA/500 mA.

B2 is ignored if B1=0. B3,4 are used to set the constant current in the current regulation phase. With B4B3=11, the battery is charged with the maximum current set by the external resistor at the ISET pin. Decrementing B4B3 reduces the charge current by 25% per step. B5=1 enables the fast charge timer, which is by default disabled. B6 can be used to clear all the timers in the charger and force a restart of the charge algorithm. This bit must be set and then reset via the serial interface. B7 can be set to reduce the $t_{n(RESPWRON)}$ duration from typically 1000 ms to 69 ms (±25%).

Internal Register Address: 08h—Default Value: 00h

LED1_ON	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit name & function	$\overline{\text{PG1}}$	LED1 ON6	LED1 ON5	LED1 ON4	LED1 ON3	LED1 ON2	LED1 ON1	LED1 ON 0
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Internal Register Address: 09h—Default Value: 00h

LED1_PER	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit name & function	$\overline{\text{PG2}}$	LED1 PER6	LED1 PER5	LED1 PER4	LED1 PER3	LED1 PER2	LED1 PER1	LED1 PER 0
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The LED1_ON and LED1_PER registers can be used to take control of the $\overline{\text{PG}}$ open drain output normally controlled by the charger. Control is determined by $\overline{\text{PG1}}$ and $\overline{\text{PG2}}$ according to the following table, default shown in **bold**. When programmed to blink, LED1_ON<6:0> and LED1_PER<6:0> are used to program the on- and period-time respectively of the open drain output transistor at the $\overline{\text{PG}}$ pin. The minimum on time is typically 10 ms and one LSB corresponds to a 10-ms step change in the on time. The minimum period is typically 100 ms and one LSB corresponds to a 100-ms step change in the period.

$\overline{\text{PG1}}$	$\overline{\text{PG2}}$	**BEHAVIOR OF $\overline{\text{PG}}$ OPEN DRAIN OUTPUT**
0	**0**	**Under charger control**
0	1	Blink
1	0	Off
1	1	On

Internal Register Address: 0Ah—Default Value: 00h

LED2_ON	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit name & function	LED21	LED2 ON6	LED2 ON5	LED2 ON4	LED2 ON3	LED2 ON2	LED2 ON1	LED2 ON0
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Internal Register Address: 0Bh—Default Value: 00h

LED2_PER	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit name & function	LED22	LED2 PER6	LED2 PER5	LED2 PER4	LED2 PER3	LED2 PER2	LED2 PER1	LED2 PER 0
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The LED2_ON and LED2_PER registers are used to control the LED2 open drain output. Control is determined by LED21 and LED22 according to the following table, default shown in **bold**. When programmed to blink, LED2_ON<6:0> and LED2_PER<6:0> are used to program the on- and period-time respectively The minimum on time is typically 10 ms and one LSB corresponds to a 10-ms step change in the on time. The minimum period is typically 100 ms and one LSB corresponds to a 100-ms step change in the period.

LED21	LED22	**BEHAVIOR OF LED2 OPEN DRAIN OUTPUT**
0	**0**	**Off**
0	1	Blink
1	0	Off
1	1	On

Internal Register Address: 0Ch—Default Value: 72h/73h

VDCDC1	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	FPWM	UVLO1	UVLO0	ENABLE SUPPLY	ENABLE LP	MAIN DISCHARGE	MAIN1	MAIN0
Default	0	1	1	1	0	0	1	DEFMAIN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The VDCDC1 register is used to program the VMAIN switching converter. The VMAIN converter output voltages are set according to the following table, with the default values in **bold** set by the DEFMAIN pin. The default voltage can subsequently be over-written via the serial interface after start up. The ENABLE LP bit enables the low power function of the LOW_PWR pin. The ENABLE SUPPLY bit must be left set. When the forced PWM bit FPWM = 1, the MAIN and the CORE dc-dc converter operate with forced fixed frequency PWM mode and are not allowed to switch into PFM mode. MAIN DISCHARGE is used to enable the active discharge of the VMAIN converter.

MAIN1	MAIN0	VMAIN	UVLO1	UVLO0	V_{UVLO}
0	0	2.5 V	0	0	2.5 V
0	1	2.75 V	0	1	2.75 V
1	0	**3.0 V**	1	0	3.0 V
1	1	**3.3 V**	1	1	**3.25 V**

The undervoltage threshold voltage is set by UVLO1 and UVLO0 according to the above table, with the default value in **bold**.

Internal Register Address: 0Dh—Default Value: 68/78h

VDCDC2	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	LP_COREOFF	CORE2	CORE1	CORE0	CORELP1	CORELP0	VIB	CORE DISCHARGE
Default	0	1	1	DEFCORE	1	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The VDCDC2 register is used to program the VCORE switching converter output voltage. It is programmable in 8 steps between 0.85 V and 1.6 V. The default value is governed by the DEFCORE pin; DEFCORE=0 sets an output voltage of 1.5 V. DEFCORE=1 sets an output voltage of 1.6 V. The following table shows all possible values of VCORE. The default value can subsequently be overwritten via the serial interface after start-up. CORELP1 and CORELP0 can be used to set the VCORE voltage in low power mode. In low power mode, CORE2 is effectively 0, and CORE1, CORE0 take on the values programmed at CORELP1 and CORELP0, default 10 giving VCORE = 1.1 V as default in low power mode. When low power mode is exited, VCORE reverts to the value set by CORE2, CORE1 and CORE0. If LP_COREOFF is set high, the VCORE converter is disabled in low power mode.

CORE2	CORE1	CORE0	VCORE
0	0	0	0.85 V
0	0	1	1.0 V
0	**1**	**0**	**1.1 V**
0	1	1	1.2 V
1	0	0	1.3 V
1	0	1	1.4 V
1	**1**	**0**	**1.5 V**
1	**1**	**1**	**1.6 V**

CORE DISCHARGE is used to enable the active discharge of the VCORE converter. VIB is used to enable the VIB output transistor to drive the vibrator motor.

Internal Register Address: 0Eh—Default Value: 88h

VREGS1	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	LDO2 enable	LDO2 OFF/nSLP	LDO21	LDO20	LDO1 enable	LDO1 OFF/nSLP	LDO11	LDO10
Default	1	0	0	0	1	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The VREGS1 register is used to program and enable LDO1 and LDO2 and to set their behavior when low power mode is active. The LDO output voltages can be set either on the fly, while the relevant LDO is disabled, or simultaneously when the relevant enable bit is set. Note that both LDOs are per default ON. The function of the LDOx enable and LDOx OFF/nSLP bits is shown in the following table. See the power-on sequencing section for details of low power mode.

NOTE: Programming LDO1 to a higher voltage may force a system power on reset if the increase is in the 10% or greater range.

LDOX ENABLE	LDOX OFF/NSLP	LDO STATUS IN NORMAL MODE	LDO STATUS IN LOW POWER MODE
0	X	OFF	OFF
1	0	ON, full power	ON, reduced power/performance
1	1	ON, full power	OFF

LDO11	LDO10	VLDO1
0	**0**	**ADJ**
0	1	2.5 V
1	0	2.75 V
1	1	3.0 V

The LDO1 output voltage is per default set externally; this can be changed via the serial interface if so desired.

LDO21	LDO20	VLDO2
0	**0**	**1.8 V**
0	1	2.5 V
1	0	2.75 V
1	1	3.0 V

LDO2 has a default output voltage of 1.8 V; this can be changed at the same time as it is enabled via the serial interface if so desired.

Internal Register Address: 0Fh—Default Value: 00h

MASK3	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	Edge trigger GPIO4	Edge trigger GPIO3	Edge trigger GPIO2	Edge trigger GPIO1	Mask GPIO4	Mask GPIO3	Mask GPIO2	Mask GPIO1
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The MASK3 register must be considered when any of the GPIO pins are programmed as inputs. B7−B4 determine whether the respective GPIO generates an interrupt at a rising or a falling edge, a 0 indicates that the falling edge is used and a 1 indicates that the rising edge is used. B3−B0 can be used to mask the corresponding interrupt.

Internal Register Address: 10h—Default Value: 00h

DEFGPIO	B7	B6	B5	B4	B3	B2	B1	B0
Bit name & function	IO4	IO3	IO2	IO1	Value GPIO4	Value GPIO3	Value GPIO2	Value GPIO1
Default	0	0	0	0	0	0	0	0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The DEFGPIO register is used to define the GPIO pins to be either input or output. B7−4 = 0 sets the corresponding GPIO to be an input, B7−4 = 1 sets the corresponding GPIO to be an output. If a GPIO is programmed to be an output then the signal output is determined by the corresponding B3−0 bit. The output circuit for each GPIO is an open drain NMOS requiring an external pullup resistor. Setting B3−0 = 1 activates the relevant NMOS, hence forcing a logic low signal at the GPIO pin. Setting B3−0 = 0 turns the open drain transistor OFF, hence the voltage at the GPIO pin is determined by the voltage to which the pullup resistor is connected. If a particular GPIO is programmed to be an input, then the contents of the relevant bit in B3−0 is defined by the logic level at the GPIO pin. A logic low forces a 0 and a logic high forces a 1. If a GPIO is programmed to be an input, then any attempt to write to the relevant bit in B3−0 is ignored.

DESIGN PROCEDURE

Inductor Selection for the Main and the Core Converter

The main and the core converters in the TPS65010 typically use a 6.2-µH and a 10-µH output inductor respectively. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest dc resistance is selected for highest efficiency.

Formula (3) calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with formula (3). This is needed because during heavy load transient, the inductor current rises above the value calculated under (3).

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \tag{3}$$

$$I_{L(max)} = I_{O(max)} + \frac{\Delta I_L}{2} \tag{4}$$

with:

f = Switching Frequency (1.25 MHz typical)

L = Inductor Value

ΔI_L= Peak-to-peak inductor ripple current

I_{Lmax} = Maximum inductor current

The highest inductor current occurs at maximum V_I.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS65010 (2 A for the main converter and 0.8 A for the core converter). Keep in mind that the core material from inductor to inductor differs and has an impact on the efficiency especially at high switching frequencies.

Refer to Table 2 and the typical applications for possible inductors

Table 2. Tested Inductors

DEVICE	INDUCTOR VALUE	DIMENSIONS	COMPONENT SUPPLIER
Core converter	10 µH	6,0 mm × 6,0 mm × 2,0 mm	Sumida CDRH5D18−100
	10 µH	5,0 mm × 5,0 mm × 3.0 mm	Sumida CDRH4D28−100
Main converter	4.7 µH	5,5 mm × 6,6 mm*1.0 mm	Coilcraft LPO1704−472M
	4.7 µH	5,0 mm × 5,0 mm × 3.0 mm	Sumida CDRH4D28C−4.7
	4.7 µH	5,2 mm × 5.2 mm × 2.5 mm	Coiltronics SD25−4R7
	5.3 µH	5,7 mm × 5.7 mm × 3.0 mm	Sumida CDRH5D28−5R3
	6.2 µH	5,7 mm × 5.7 mm × 3.0 mm	Sumida CDRH5D28−6R2
	6.0 µH	7.0 mm × 7.0 mm × 3.0 mm	Sumida CDRH6D28−6R0

Output Capacitor Selection

The advanced fast response voltage mode control scheme of the inductive converters implemented in the TPS65010 allow the use of small ceramic capacitors with a typical value of 22 µF for the main converter and 10 µF for the core converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. If required tantalum capacitors with an ESR < 100 mR may be used as well.

Refer to Table 3 for recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meet the application requirements. Just for completeness the RMS ripple current is calculated as:

$$I_{RMSC(out)} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{5}$$

At nominal load current, the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + ESR \right) \tag{6}$$

Where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the converters operate in power save mode and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the nominal output voltage. If the output voltage for the core converter is programmed to its lowest voltage of 0.85 V, the output capacitor must be increased to 22 µF for low output voltage ripple. This is because the current in the inductor decreases slowly during the off-time and further increases the output voltage even when the PMOS is off. This effect increases with low output voltages.

Input Capacitor Selection

Because of the nature of the buck converter, having a pulsating input current a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The main converter needs a 22-µF ceramic input capacitor and the core converter a 10-µF ceramic capacitor. The input capacitor for the main and the core converter can be combined and one 22-µF capacitor can be used instead, because the two converters operate with a phase shift of 270 degrees. The input capacitor can be increased without any limit for better input voltage filtering. The VCC pin should be separated from the input for the main and the core converter. A filter resistor of up to 100R and a 1-µF capacitor is used for decoupling the VCC pin from switching noise.

Table 3. Possible Capacitors

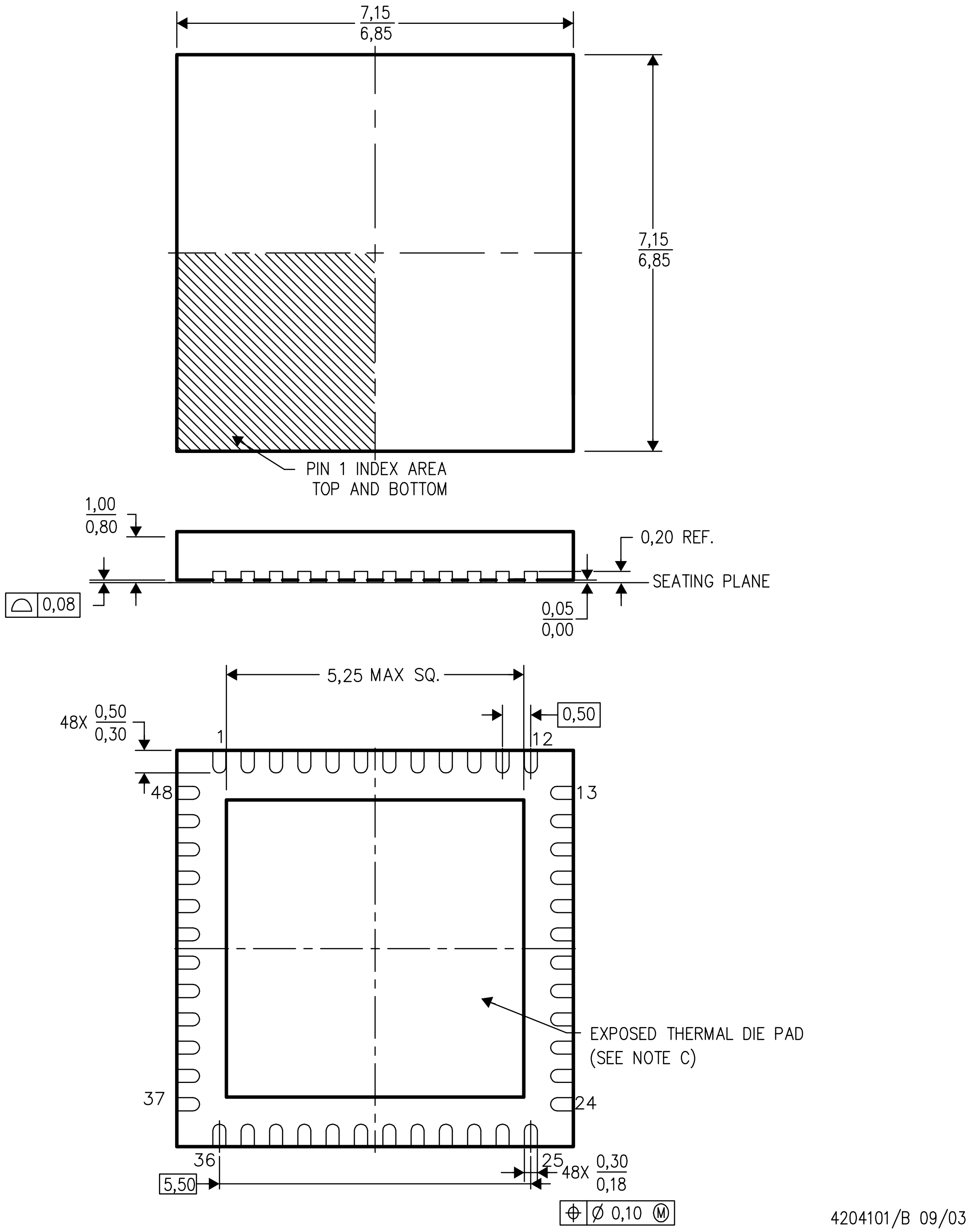
CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22 µF	1206	TDK C3216X5R0J226M	Ceramic
22 µF	1206	Taiyo Yuden JMK316BJ226ML	Ceramic
22 µF	1210	Taiyo Yuden JMK325BJ226MM	Ceramic

LDO1

Output Voltage Adjustment

The output voltage of LDO1 is set with a resistor divider at the feedback pin. The sum of the two resistors must not exceed 1 MR to minimize voltage changes due to leakage current into the feedback pin. The output voltage for LDO1 after start up is the voltage set by the external resistor divider. It can be reprogrammed with the I^2C interface to the three other values defined in the register VREGS1.

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
E. Falls within JEDEC MO–220.

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