REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		8-11-07
B	Added Crystal Circuit 1.0M Ohm Resistor Detail		11-15-07
C	Corrected Pin 62 in QuickCheck Table; changed from AVSS to VSS		3-21-08
D	Added Pin 13 (VDD33) Detail With Internal Regulator Disabled		11-17-08
E	Corrected Pin 36 (CH_SELECT) Internal Termination & Functionality		2-16-12

DOCUMENT DESCRIPTION

Schematic Checklist for the LAN8187, 64-pin TQFP Package

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Document Number	Revision
SC471210	E

Schematic Checklist for LAN8187

Information Particular for the 64-pin TQFP Package

LAN8187 TQFP Phy Interface:

1. TXP (pin 51); This pin is the transmit twisted pair output positive connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to AVDD (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

2. TXN (pin 50); This pin is the transmit twisted pair output negative connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to AVDD (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

3. For Transmit Channel connection and termination details, refer to Figure 1.

4. RXP (pin 55); This pin is the receive twisted pair input positive connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to AVDD (created from +3.3V). This pin also connects to the receive channel of the magnetics.

5. RXN (pin 54); This pin is the receive twisted pair input negative connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to AVDD (created from +3.3V). This pin also connects to the receive channel of the magnetics.

6. For Receive Channel connection and termination details, refer to Figure 2.

7. For added EMC flexibility in a LAN8187 design, the designer should include four low valued capacitors on the TXP, TXN, RXP & RXN pins. Low valued capacitors (less than 15 ρF) can be added to each line and terminated to digital ground. These components can be added to the schematic and should be designated as Do Not Populate (DNP).

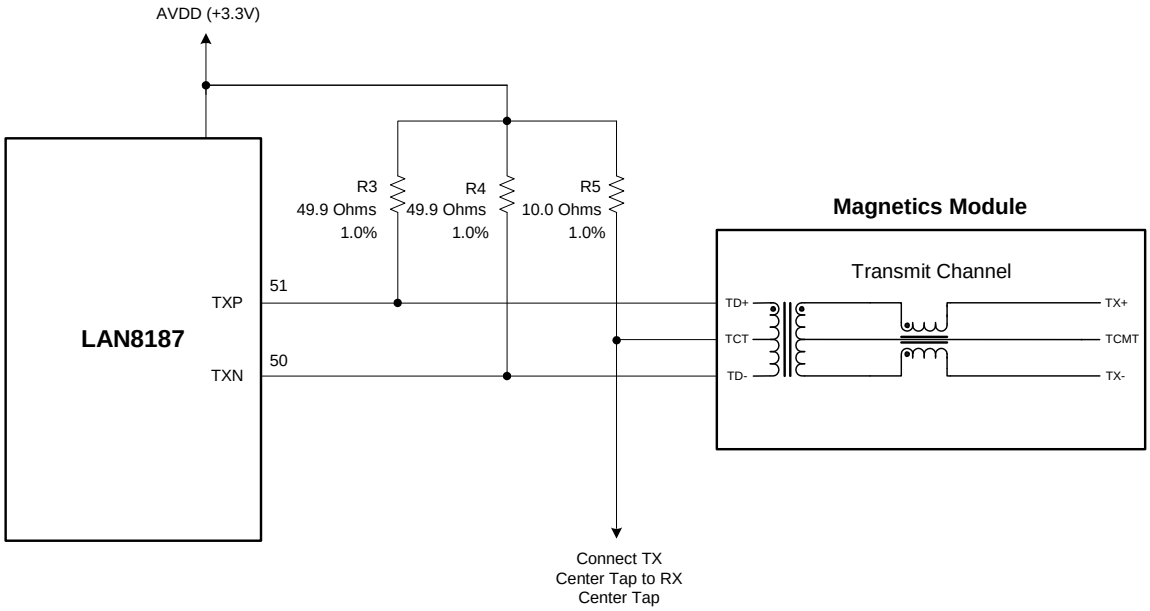


Figure 1 – Transmit Channel Connections and Terminations

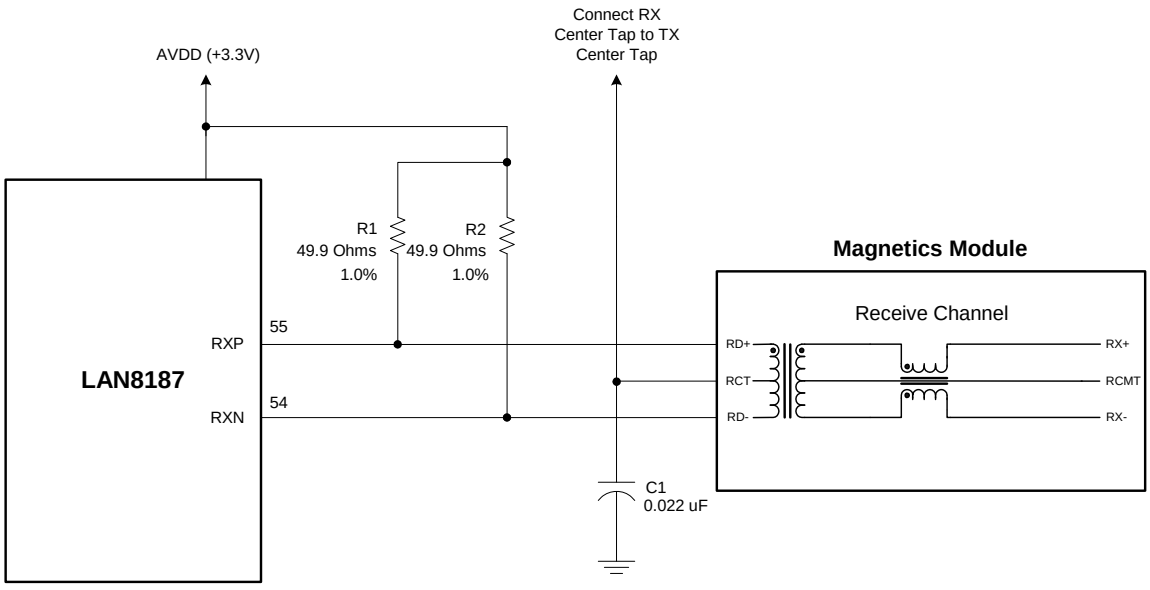


Figure 2 - Receive Channel Connections and Terminations

LAN8187 TQFP Magnetics:

1. The center tap connection on the LAN8187 side for the transmit channel must be connected to VDD_A (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.

2. The center tap connection on the LAN8187 side for the receive channel is connected to the transmit channel center tap on the magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP (pin 51) of the LAN8187 TQFP.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXN (pin 50) of the LAN8187 TQFP.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP (pin 55) of the LAN8187 TQFP.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXN (pin 54) of the LAN8187 TQFP.

10. When using the SMSC LAN8187 device in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the SMSC Applications Note 8.13 “Suggested Magnetics” for proper magnetics.

RJ45 Connector:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

Power Supply Connections:

1. The digital supply (VDD33) pin on the LAN8187 TQFP is pin 13. This pin requires a connection to +3.3V.

   Note: Pin 13 (VDD33) must always be connected to a +3.3V power supply; even in the case of having the internal +1.8V regulator of the LAN8187 disabled. Other blocks within the LAN8187 require power from +3.3V.

2. The VDD33 power pin should have one .01 μF (or smaller) capacitor to decouple the LAN8187. The capacitor size should be SMD_0603 or smaller.

3. The analog supply (AVDD) pins on the LAN8187 TQFP are 53, 57, & 61. They require a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

4. Each AVDD pin should have one .01 μF (or smaller) capacitor to decouple the LAN8187. The capacitor size should be SMD_0603 or smaller.

5. Pin 43 (VDDIO) is a variable supply voltage for the I/O pads. This pin must be connected to a voltage supply between +1.8V and +3.3V.

6. The VDDIO pin should have one .01 μF (or smaller) capacitor to decouple the LAN8187. The capacitor size should be SMD_0603 or smaller.

Ground Connections:

1. The digital ground pins (VSS) on the LAN8187 TQFP are 7, 9, 10, 15, 24, 28, 40 & 62. They need to be connected directly to a solid, contiguous ground plane.

2. The analog ground pins (AVSS) on the LAN8187 TQFP are 49, 52, 58 & 60. They also need to be connected directly to the same solid, contiguous ground plane.

3. We recommend that the Digital Ground pins and the AVSS pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

VDD_CORE:

1. VDD_CORE (pin 14), this pin is used to provide bypassing for the +1.8V core regulator. This pin requires a 0.1 μF bypass capacitor. This capacitor should be located as close as possible to its pin without using vias. In addition, pin 14 requires a bulk capacitor placed as close as possible to pin 14. The bulk capacitor must have a value of at least 4.7 μF, and have an ESR (equivalent series resistance) of no more than 1.0 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.8V supply is for internal logic only. **Do Not** power other circuits or devices with this supply.

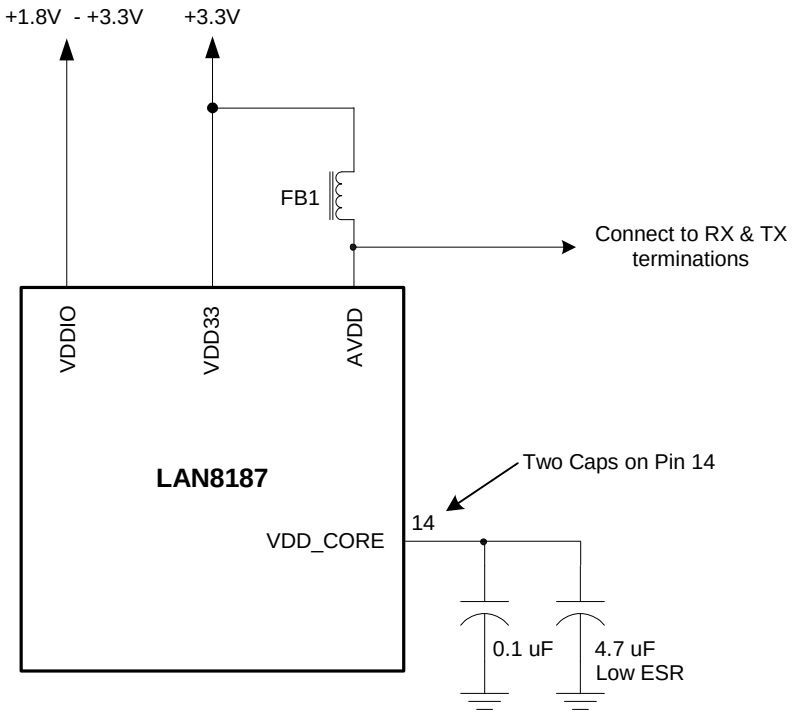


Figure 3 - LAN8187 Power Connections

Crystal Connections:

1. When using the LAN8187 TQFP in MII mode, a 25.000 MHz crystal should be used to provide the clock source. For exact specifications and tolerances refer to the latest revision LAN8187 data sheet.

2. CLKIN/XTAL1 (pin 23) on the LAN8187 TQFP is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XTAL2 (pin 22) on the LAN8187 TQFP is the clock circuit output. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

4. Since every system design is unique, the value for the capacitors are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, an additional 1.0M Ω resistor needs to be added to the crystal circuit. This resistor needs to be placed in parallel with the crystal.

Clock Oscillator Connections:

1. When using the LAN8187 TQFP in RMII mode, a 50.000 MHz clock oscillator should be used to provide the clock source. A clock oscillator is recommended for RMII mode because the clock source must drive two inputs. It must provide a 50.000 MHz clock for the phy and it is also required to provide a clock for the RMII MAC in the design. For exact specifications and tolerances refer to the latest revision LAN8187 data sheet.

2. CLKIN/XTAL1 (pin 23) on the LAN8187 TQFP is the clock circuit input.

3. XTAL2 (pin 22) on the LAN8187 TQFP is the clock circuit output. When using a single ended clock source, this pin can be left as a no-connection.

4. Since every system design is unique, the PCB design, the oscillator selected and the layout all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

EXRES1 Resistor:

1. EXRES1 (pin 59) on the LAN8187 TQFP should connect to digital ground through a 12.4K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

MII Interface:

1. When utilizing either an external MII MAC interface or an MII Connector, the following table indicates the proper connections for the 18 signals.

From:	Connects To:	
LAN8187 TQFP	**MII MAC Device**	**MII Connector**
RXD0 (pin 32)	RXD<0>	RXD<0> (contact 7)
RXD1 (pin 31)	RXD<1>	RXD<1> (contact 6)
RXD2 (pin 30)	RXD<2>	RXD<2> (contact 5)
RXD3 (pin 29)	RXD<3>	RXD<3> (contact 4)
RX_DV (pin 33)	RX_DV	RX_DV (contact 8)
RX_ER (pin 35)	RX_ER	RX_ER (contact 10)
RX_CLK (pin 34)	RX_CLK	RX_CLK (contact 9)
TX_ER (pin 46)	TX_ER	TX_ER (contact 11)
TXD0 (pin 41)	TXD<0>	TXD<0> (contact 14)
TXD1 (pin 42)	TXD<1>	TXD<1> (contact 15)
TXD2 (pin 44)	TXD<2>	TXD<2> (contact 16)
TXD3 (pin 45)	TXD<3>	TXD<3> (contact 17)
TX_EN (pin 39)	TX_EN	TX_EN (contact 13)
TX_CLK (pin 38)	TX_CLK	TX_CLK (contact 12)
CRS (pin 48)	CRS	CRS (contact 19)
COL (pin 47)	COL	COL (contact 18)
MDIO (pin 26)	MDIO	MDIO (contact 2)
MDC (pin 27)	MDC	MDC (contact 3)

2. RMII (pin 1) this defines the MII/RMII Bus operation of the LAN8187. A low on this pin configures the LAN8187 for normal MII Bus operation. This input is latched on the rising edge of reset. This pin has a weak internal pull-down and can be left as a no-connect for MII Bus operation.

3. TXER/TXD4 (pin 46) this pin provides the transmit error functionality on the MII Bus interface (if required). To enable the TXER functionality on pin 46, the RXD3/nINTSEL pin (pin 29) must be pulled down through an external 10.0K resistor to ground. The RXD3/nINTSEL pin has a weak internal pull-up and must be pulled low externally to select the TXER functionality.

4. Provisions should be made for series terminations for all outputs on the MII Interface. Series resistors will enable the designer to closely match the output driver impedance of the LAN8187 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependant and must be analyzed in-system. A suggested starting point for the value of these series resistors might be 100.0 Ω.

RMII Interface:

1. When utilizing an external RMII MAC interface, the following table indicates the proper connections for the 9 signals.

From:	Connects To:	
LAN8187 TQFP	**RMII MAC Device**	**Notes**
RXD0 (pin 32)	RXD<0>	
RXD1 (pin 31)	RXD<1>	
RXD2 (pin 30)	RXD<2>	Not Used in RMII Mode
RXD3 (pin 29)	RXD<3>	Not Used in RMII Mode
RX_DV (pin 33)	RX_DV	Not Used in RMII Mode
RX_ER (pin 35)	RX_ER	This signal is optional in RMII Mode
RX_CLK (pin 34)	RX_CLK	Not Used in RMII Mode
TX_ER (pin 46)	TX_ER	Not Used in RMII Mode
TXD0 (pin 41)	TXD<0>	
TXD1 (pin 42)	TXD<1>	
TXD2 (pin 44)	TXD<2>	Not Used in RMII Mode; TXD2 Should be grounded
TXD3 (pin 45)	TXD<3>	Not Used in RMII Mode; TXD3 Should be grounded
TX_EN (pin 39)	TX_EN	
TX_CLK (pin 38)	TX_CLK	Not Used in RMII Mode
CRS_DV (pin 47)	CRS_DV	
CRS (pin 48)	CRS	Not Used in RMII Mode
COL (pin 47)	COL	
MDIO (pin 26)	MDIO	
MDC (pin 27)	MDC	

2. RMII (pin 1) this defines the MII/RMII Bus operation of the LAN8187. A high on this pin configures the LAN8187 for RMII Bus operation. This input is latched on the rising edge of reset. Since this pin has a weak internal pull-down, an external pull-up resistor must be used to configure the LAN8187 for RMII Bus operation. A 10.0K pull-up to VDDIO on this pin will configure the phy for RMII mode.

3. Provisions should be made for series terminations for all outputs on the RMII Interface. Series resistors will enable the designer to closely match the output driver impedance of the LAN8187 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependant and must be analyzed in-system. A suggested starting point for the value of these series resistors might be 10.0 Ω.

MII/RMII Series Terminations:

	Series Terminations	
Signal	**MII Mode**	**RMII Mode**
RXD0	100 Ω	10 Ω
RXD1	100 Ω	10 Ω
RXD2	100 Ω	n/a
RXD3	100 Ω	n/a
RX_CLK	100 Ω	n/a
RX_ER	100 Ω	10 Ω
RX_DV	100 Ω	n/a
CRS_DV	n/a	10 Ω
COL	100 Ω	n/a
CRS	100 Ω	n/a
TX_CLK	100 Ω	n/a

Required External Pull-ups:

1. nINT (pin 46) requires an external pull-up resistor as this output is an Open Drain type.

2. When using the MII or the RMII interface of the LAN8187 TQFP with a MAC device on board, a pull-up resistor on the MDIO signal (pin 26) is required. A pull-up resistor of 1.5KΩ to +5V/+3.3V is required for this application.

Mode Pins:

1. The Mode pins of the LAN8187 (MODE[2:0]) control the default configuration of the 10/100 phy. Speed, Duplex, Auto-Negotiation & power down functionality can be configured through these pins. The value of these three pins are latched in upon power-up and reset. The values latched in are reflected in Register 0 & Register 4 of the LAN8187. See the LAN8187 data sheet for complete details for the operation of these pins. These three pins have weak internal pull-ups and can be left as no-connects. To set any Mode bit low, an external 10K pull-down resistor should be used.

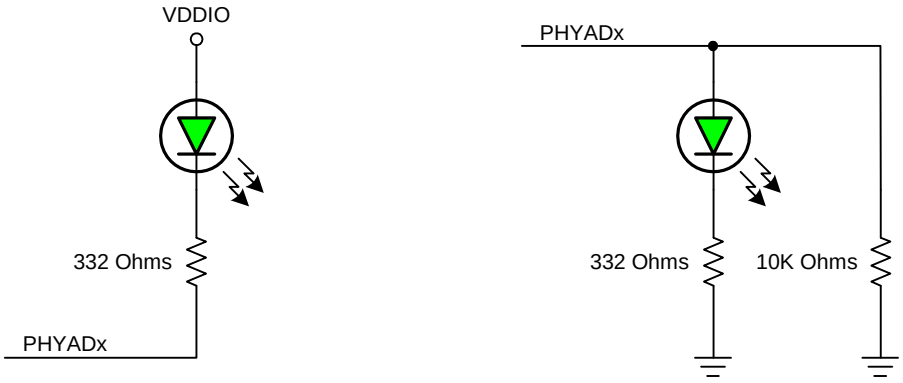
Phy Address Pins:

1. The Phy Address pins of the LAN8187 (PHYAD[4:0]) determine which of the 32 addresses the LAN8187 will respond to. The value of these five pins are latched in upon power-up and reset. The values latched in are reflected in Register 18 of the LAN8187. See the LAN8187 data sheet for complete details for the operation of these pins. These five pins have weak internal pull-ups and can be left as no-connects. To set any Phy Address bit low, an external 10K pull-down resistor should be used.

2. A basic Phy Address of 01h is usually recommended.

3. The Phy Address pins are shared with the LED functionality and one general purpose output of the LAN8187. The pinouts are as follows:

   Phy Address 0 is shared with LED SPEED100 on pin 16.
   Phy Address 1 is shared with LED LINK on pin 17.
   Phy Address 2 is shared with LED ACTIVITY on pin 19.
   Phy Address 3 is shared with LED FDUPLEX on pin 20.
   Phy Address 4 is shared with GPO1 on pin 2.



PHY Address Bit = 1

LED Output Signal from LAN8187 is Active Low

PHY Address Bit = 0

LED Output Signal from LAN8187 is Active High

Figure 4 Phy Address / LED Polarity

LED Pins:

1. The LAN8187 provides four LED signals. These indicators will display speed, duplex, link and activity information about the current state of the Phy. The LED outputs have the ability to be either active high or active low. The polarity is determined by the Phy Address latched in at reset. The LAN8187 senses each Phy Address bit and changes the polarity of the LED signal accordingly. If the address bit is set as a level one, the LED polarity will be set to an active-low. If the address bit is set as a level zero, the LED polarity will be set to an active high; see Figure 4 above. See the LAN8187 data sheet for further details on how to strap each pin for correct phy addressing and LED polarity outcomes.

2. The LED and one general purpose output pins are shared with the Phy Address functionality of the LAN8187. The pinouts are as follows:

   LED SPEED100 is shared with Phy Address 0 on pin 16.
   LED LINK is shared with Phy Address 1 on pin 17.
   LED ACTIVITY is shared with Phy Address 2 on pin 19.
   LED FDUPLEX is shared with Phy Address 3 on pin 20.
   GPO1 is shared with Phy Address 4 on pin 2.

Interrupt Functionality:

1. For added flexibility, the LAN8187 TQFP has a discrete interrupt line for embedded applications. This is advantageous as there is no interrupt facility across the standard MII Bus interface.

2. nINT (pin 46) this pin provides the interrupt signal from the LAN8187. To enable the interrupt functionality on pin 46, the RXD3/nINTSEL pin (pin 29) must be left as a no connection. The RXD3/nINTSEL pin has a weak internal pull-up and therefore can be left as a no connect to select the interrupt functionality.

Miscellaneous:

1. There are seven No-Connect pins on the LAN8187. It is very important that these pins remain as no-connects. These pins are 8, 11, 12, 18, 21, 56 & 64.

2. REG_EN (pin 63) this pin enables the internal +1.8V core regulator of the LAN8187. To enable the regulator, this pin must be pulled high with a 10.0K resistor to VDDIO. To disable the regulator, this pin should be pulled low with a 10.0K resistor to ground. Normal operation will have this pin pulled high.

3. nRST (pin 25), this pin is an active-low reset input. This signal resets all logic and registers within the LAN8187. If nRST is left unconnected the LAN8187 will rely on its internal power-on reset circuitry.

4. AMDIX_EN (pin 37) this pin controls the HP Auto MDIX functionality of the LAN8187. To enable Auto MDIX, this pin must be pulled high. This pin has a weak internal pull-up and can be left as a no-connect to enable Auto MDIX. To disable Auto MDIX, this pin should be pulled low with a 10.0K resistor to ground. This configuration pin can be overwritten by software. See the LAN8187 data sheet for further details on the HP Auto MDIX functionality.

5. CH_SELECT (pin 36) this pin steers the TX and RX channels of the LAN8187. The CH_SELECT control is enabled only when the AMDIX_EN pin (pin 37) is low (disabled). This pin (pin 36) has a weak internal pull-down and can be left as a no-connect to enable the Normal MDI operation of the TX & RX channels. To enable the Crossed MDIX operation of the TX & RX channels, this pin should be pulled high with a 10.0K resistor to +3.3V. This configuration pin can be overwritten by software. See the LAN8187 data sheet for further details on the channel select functionality.

6. Due to possible lower I/O voltages used on the LAN8187, lower strapping resistor values need to be used to ensure the strapped configuration is properly latched into the phy device upon power-on reset. Refer to the latest revision of the LAN8187 TQFP data sheet for details of proper resistor values when using lower I/O voltages on VDDIO.

7. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

8. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

LAN8187 TQFP QuickCheck Pinout Table:

Use the following table to check the LAN8187 TQFP shape in your schematic.

LAN8187 TQFP							
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GPO0/RMII	17	LINKON/PHYAD1	33	RX_DV	49	AVSS
2	GPO1/PHYAD4	18	NC4	34	RX_CLK	50	TXN
3	GPO2	19	ACTIVITY/PHYAD2	35	RX_ER/RXD4	51	TXP
4	MODE0	20	FDUPLEX/PHYAD3	36	CH_SELECT	52	AVSS
5	MODE1	21	NC5	37	AMDIX_EN	53	AVDD
6	MODE2	22	XTAL2	38	TX_CLK	54	RXN
7	VSS	23	CLKIN/XTAL1	39	TX_EN	55	RXP
8	NC1	24	VSS	40	VSS	56	NC6
9	VSS	25	nRST	41	TXD0	57	AVDD
10	VSS	26	MDIO	42	TXD1	58	AVSS
11	NC2	27	MDC	43	VDDIO	59	EXRES1
12	NC3	28	VSS	44	TXD2	60	AVSS
13	VDD33	29	RXD3/nINTSEL	45	TXD3	61	AVDD
14	VDD_CORE	30	RXD2	46	nINT/TXER	62	VSS
15	VSS	31	RXD1	47	COL/CRS_DV	63	REG_EN
16	SPEED100/PHYAD0	32	RXD0	48	CRS	64	NC7

Notes:

Reference Material:

1. SMSC LAN8187 Data Sheet; check web site for latest revision.

2. SMSC LAN8187 MII EVB Schematic, Assembly No. SCH-7058AZ; check web site for latest revision.

3. SMSC LAN8187 RMII EVB Schematic, Assembly No. SCH-7058AZ; check web site for latest revision.

4. SMSC LAN8187-LV MII EVB Schematic, Assembly No. SCH-7058AZ; check web site for latest revision.

5. SMSC LAN8187-LV RMII EVB Schematic, Assembly No. SCH-7058RAZ-LV; check web site for latest revision.

6. SMSC LAN8187 EVB PCB, Assembly No. EVB-LAN8187; order PCB from web site.

7. SMSC Suggested Magnetics Application Note 8-13; check web site for latest revision.

8. SMSC LAN8700/LAN8700I and LAN8187/LAN8187I Ethernet PHY Layout Guidelines Application Note AN 14.8; check web site for latest revision.