EVB-LAN8187

LAN8187(I) MII Customer Evaluation Board

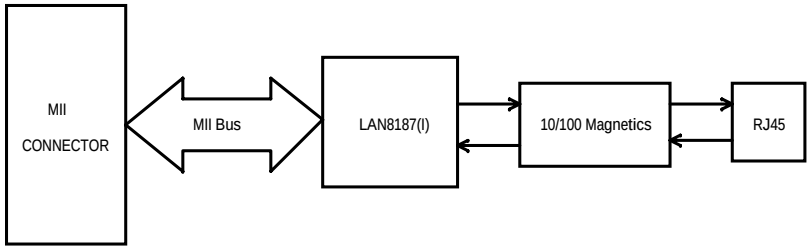
+3.3V I/O VDDIO Operation

Schematic Revision B4 Public

Design Details

Board: PCB-7058AZ-B4
Chip: LAN8187(I)
Board Form Factor:
Assembly:

EVB BLOCK DIAGRAM



Revisions	
Rev B4 Public 11/2/06	change center tap of magnetic to 75 ohms; corrected name on pin 1 to RMII; moved nINT/TXER/TXD4 on symbol; added pullup to nINT; moved caps from page 4 to page 3.; removed 150ohm DNP R63 & R64; increased the 1000pF RJ45 capacitors to 2kV; added 10ohm series resistor to XTAL.

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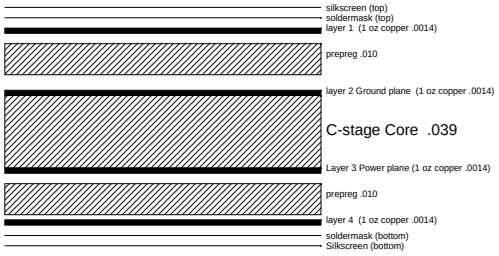
stackup



NOTES:

1. BOARD FABRICATION AND QUALITY ACCEPTANCE PER IPC-6012 CLASS 2. BOARD MUST MEET OR EXCEED QUALIFICATION TESTING AND QUALITY CONFORMACE TESTING INSPECTION SPECIFIED WITHIN.
2. MATERIAL: NEMA GRADE STANDARD FR4. LAMINATED SHEET, HTE 1 OZ COPPER CLAD, TYPE GF/GFG WOVEN GLASS BASE, FLAME RESISTANCE MEETING UL94V-0 OR BETTER. MATERIAL IN ACCORDANCE WITH IPC-4101.
3. BOARD FABRICATION SHALL APPLY DATE CODE, FABRICATOR'S CAGE CODE, I.D. AND UL MARKING TO SECONDARY SIDE WHERE INDICATED. MARKING PREFERABLY COPPER ETCHED. EPOXY INK ACCEPTABLE.
4. SOLDERMASK,USING TYPEB,PHOTO IMAGEABLE LPI FILM 0.0015 THICK. APPLY TO BOTH SIDES IN ACCORDANCE WITH IPC-SM-840 (TYPE B CLASS 3). USE APPROPIATE SOLDER MASK ARTWORK FOR EACH SIDE. PUNCTURING OF PUNCTURING OF TENTED HOLES IS PERMISSIBLE. SOLDERMASK MISREGISTRATION SHALL NOT EXCEED .004 INCH. SOLDERMASK OVERLAP PERMITTED ON CIRCULAR LANDS ONLY AND SHALL NOT EXCEED 0.001 INCH. NO OVERLAP PERMITTED ON RECTANGULAR LANDS.
5. FINISH: SOLDER MASK OVER BARE COPPER (SMOBC), HOT AIR LEVEL DEPOSIT
6. DRILL BOARDS USING DRILL DATA, DRILL PATTERN AND HOLE SCHEDULE. HOLE LOCATION MAY VARY WITHIN .004 IN. MAX ABOUT TRUE POSITION.
7. MINIMUM ANNULAR RINGS:
   .002 IN MINIMUM - EXTERNAL LAYERS.
   .001 IN MINIMUM - INTERNAL LAYERS.
8. ALL EXPOSED SURFACE LANDS AND LINES TO BE SOLDER COATED.
9. ALL HOLES ARE PLATED THROUGH UNLESS NOTED OTHERWISE. MINIMUM COPPER PLATING IN PLATED HOLES TO BE .001 IN. COPPER PLATING IN TENTED HOLES SHALL NOT PLUG HOLES WITHOUT PERMISSION FROM SMSC.
10. COMPONENT MARKINGS: SILKSCREEN BOTH SIDES USING NON-CONDUCTIVE WHITE EPOXY INK. LANDS AND EXPOSED PLATED AREAS TO BE FREE OF INK.
11. DIMENSIONS ARE AFTER ETCHING AND PLATING AND ARE BASIC UNLESS OTHERWISE INDICATED.
12. BARE BOARD ELECTRICAL TEST: BARE BOARDS SHALL BE ELECTRICALLY TESTED USING CAD GENERATED NET LIST DATA. THIS INFORMATION TO BE SUPPLIED IN IPC-D-356 FORMAT. ELECTRICAL TESTING SHALL FOLLOW THE GUIDELINES EXTABLISHED BY IPC-ET-652. GUIDELINES AND REQUIREMENTS FOR ELECTRICAL TESTING OF PRINTED WIRING BOARDS.

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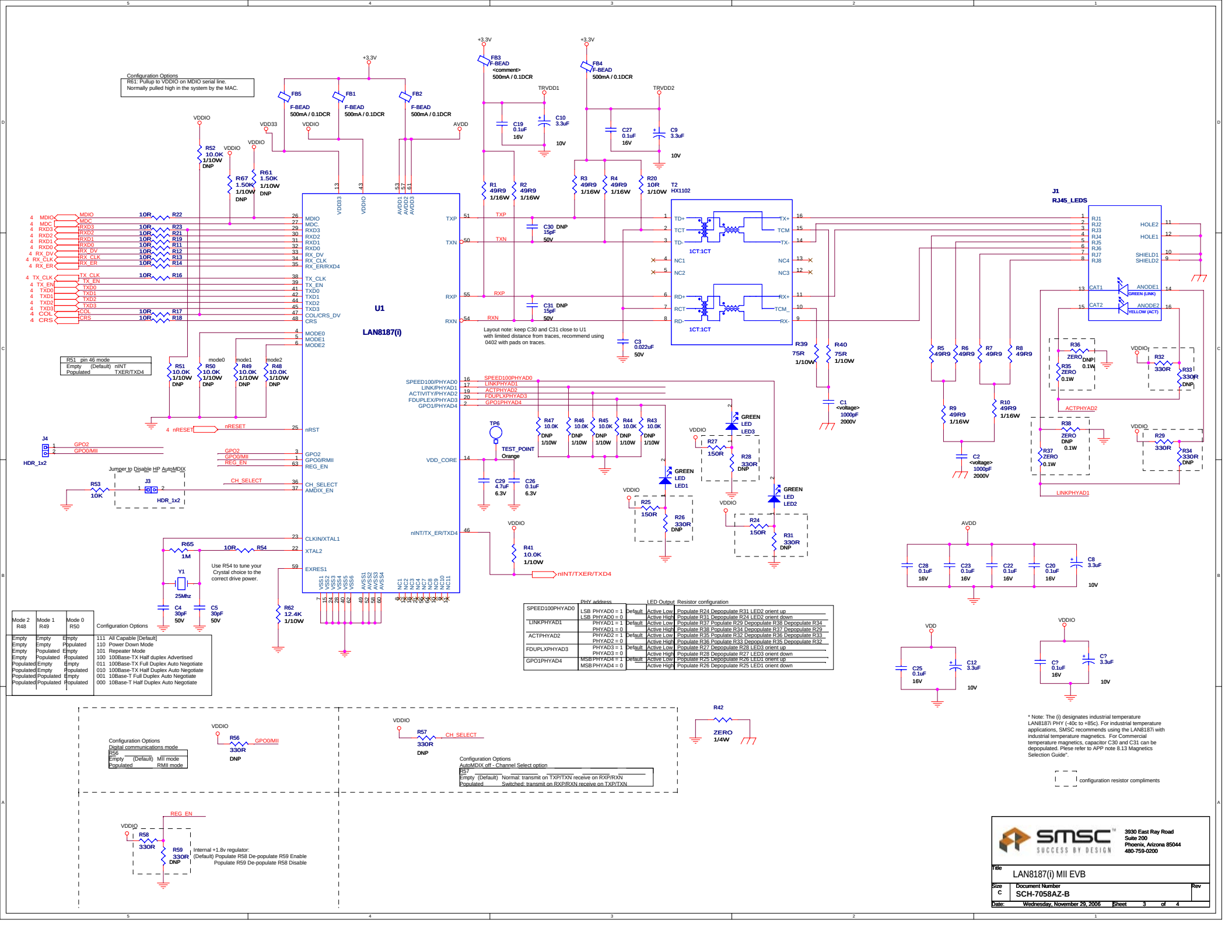
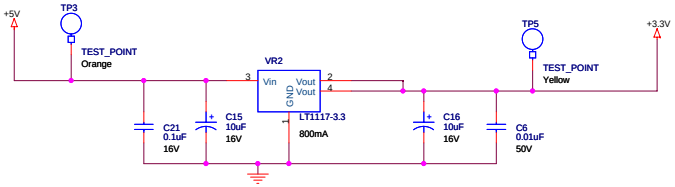
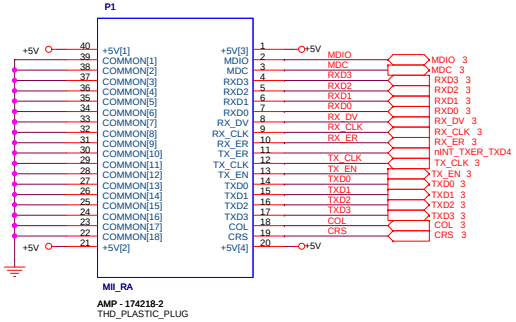


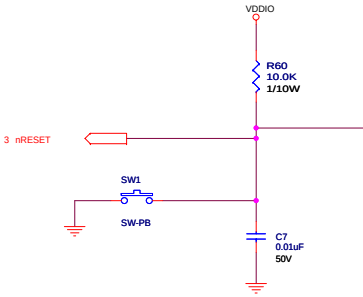
Mode 2 R48	Mode 1 R49	Mode 0 R50	Configuration Options
Empty	Empty	Empty	111 All Capable [Default]
Empty	Empty	Populated	110 Power Down Mode
Empty	Populated	Empty	101 Repeater Mode
Empty	Populated	Populated	100 100Base-TX Half duplex Advertised
Populated	Empty	Empty	011 100Base-TX Full Duplex Auto Negotiate
Populated	Empty	Populated	010 100Base-TX Half Duplex Auto Negotiate
Populated	Populated	Empty	001 10Base-T Full Duplex Auto Negotiate
Populated	Populated	Populated	000 10Base-T Half Duplex Auto Negotiate

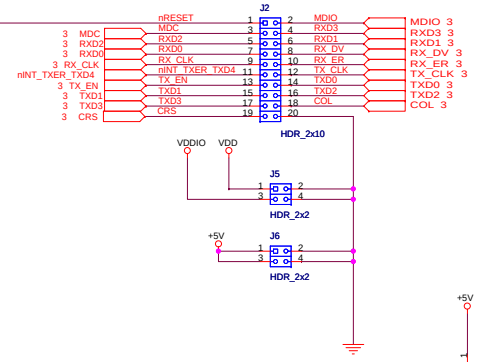
	PHY address		LED Output	Resistor configuration
SPEED100PHYAD0	LSB PHYAD0 = 1	Default	Active Low	Populate R24 Depopulate R31 LED2 orient up
	LSB PHYAD0 = 0		Active High	Populate R31 Depopulate R24 LED2 orient down
LINKPHYAD1	PHYAD1 = 1	Default	Active Low	Populate R37 Populate R29 Depopulate R38 Depopulate R34
	PHYAD1 = 0		Active High	Populate R38 Populate R34 Depopulate R37 Depopulate R29
ACTPHYAD2	PHYAD2 = 1	Default	Active Low	Populate R35 Populate R32 Depopulate R36 Depopulate R33
	PHYAD2 = 0		Active High	Populate R36 Populate R33 Depopulate R35 Depopulate R32
FDUPLXPHYAD3	PHYAD3 = 1	Default	Active Low	Populate R27 Depopulate R28 LED3 orient up
	PHYAD3 = 0		Active High	Populate R28 Depopulate R27 LED3 orient down
GPO1PHYAD4	MSB PHYAD4 = 1	Default	Active Low	Populate R25 Depopulate R26 LED1 orient up
	MSB PHYAD4 = 0		Active High	Populate R26 Depopulate R25 LED1 orient down

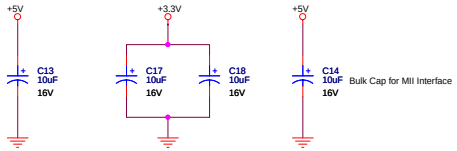
+5V MII to +3.3V Regulator

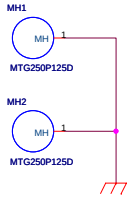


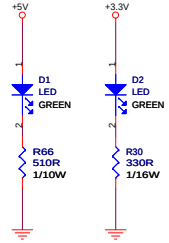












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