



EIE 2050 Digital Logic and Systems

Chapter 11: Data Storage

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Last Week

- Simple Programmable Logic Devices (SPLDs)
 - ◆ PAL, GAL, Macrocells
- Complex Programmable Logic Devices (CPLDs)
 - ◆ Class versus LUT architectures
 - ◆ Shared expander
- Macrocell Modes
 - ◆ Combinational versus Registered
- Field-Programmable Gate Arrays (FPGAs)
 - ◆ 3 components: Configurable logic blocks (CLB); Interconnections; Input/Output (I/O) blocks
 - ◆ SRAM-based FPGAs, FPGA cores
- Programmable Logic software
 - ◆ 6-step design flow: Design entry → Functional simulation → Synthesis --> Implementation (software) → Timing simulation → Downloading

Netlist

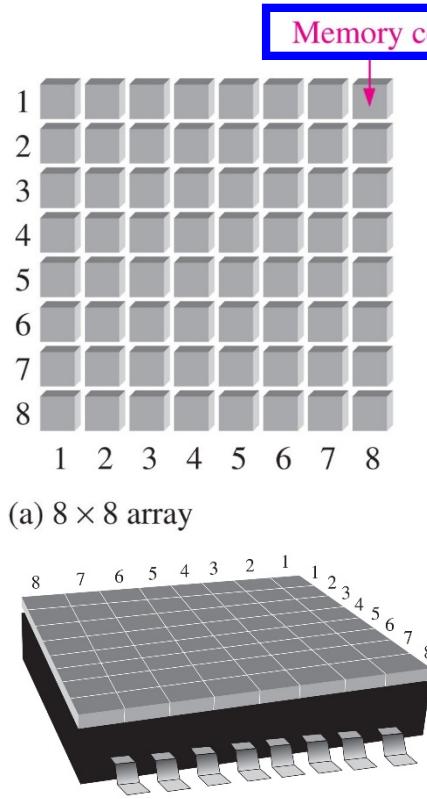


Semiconductor Memory Basics

□ Units of Binary Data

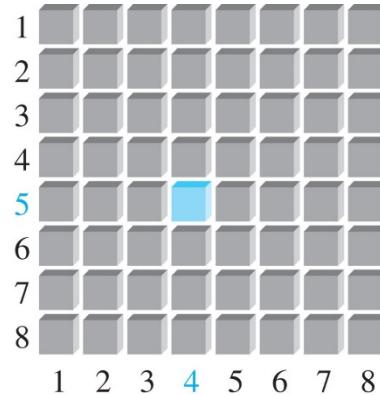
- ◆ 8 Bits = 1 Byte = 2 Nibbles

□ The Basic Memory Array

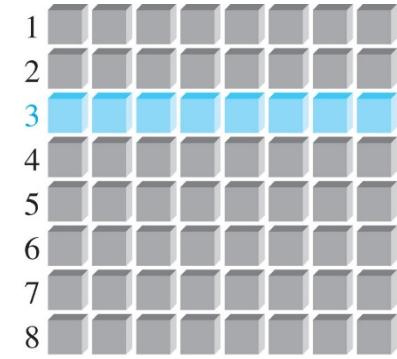


(a) Physical structure of 64-bit memory.

Memory Address and Capacity

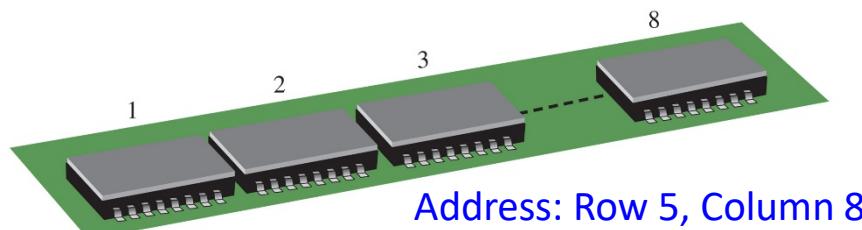


(b) The address of the blue bit
is row 5, column 4.

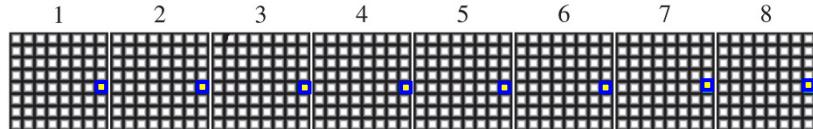


(c) The address of the blue byte
is row 3.

Capacity: 64 bits or 8 bytes



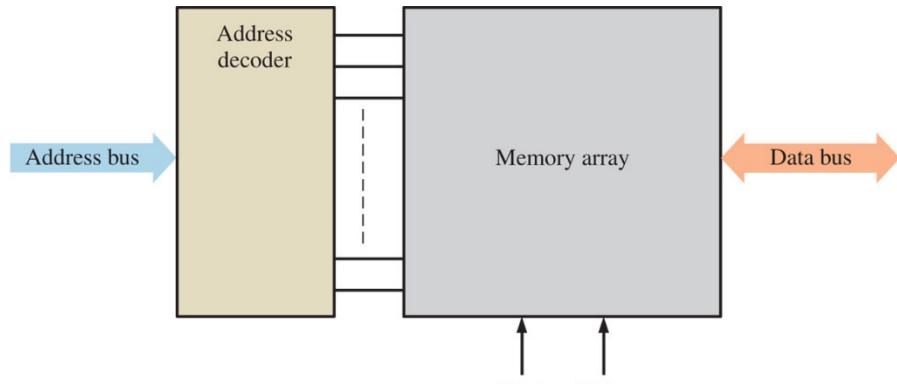
Address: Row 5, Column 8



(a) The 8×8 bit array expanded to a 64×8 bit array. This array forms a memory module.



Basic Memory Operations : Addressing

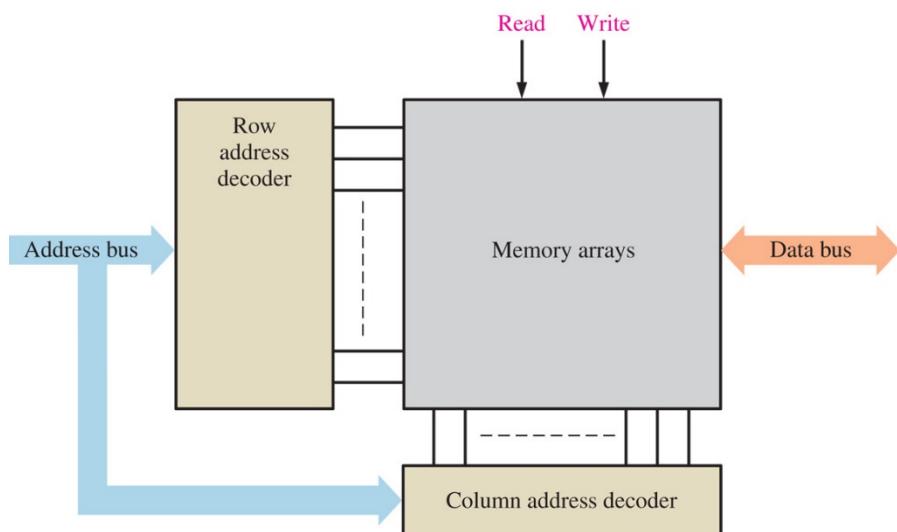


(a) Single-array memory

□ Data bus : Bidirectional

□ Address bus

- ◆ 2 address decoders in (b), one for the rows and one for the columns.
- ◆ In personal computers, a 32-bit address bus can select $4,294,967,296$ locations (2^{32}), expressed as 4G.

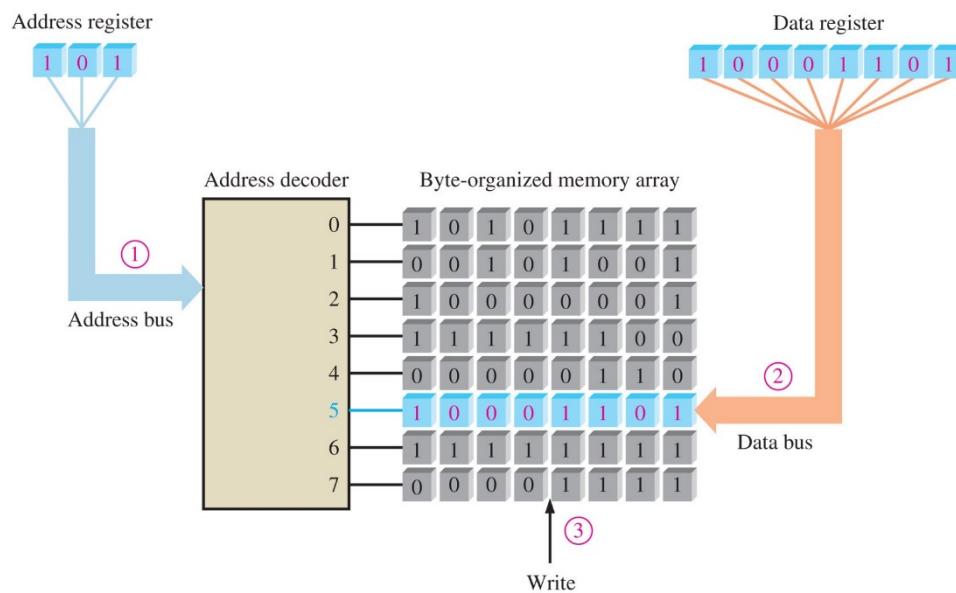


(b) Multiple-array memory



Write and Read Operations

- The address decoder decodes the address and selects the specified location in the memory.
- The memory then gets a **write** command, and the data byte held in the **data register** is placed on the **data bus** and **stored** in the selected memory address

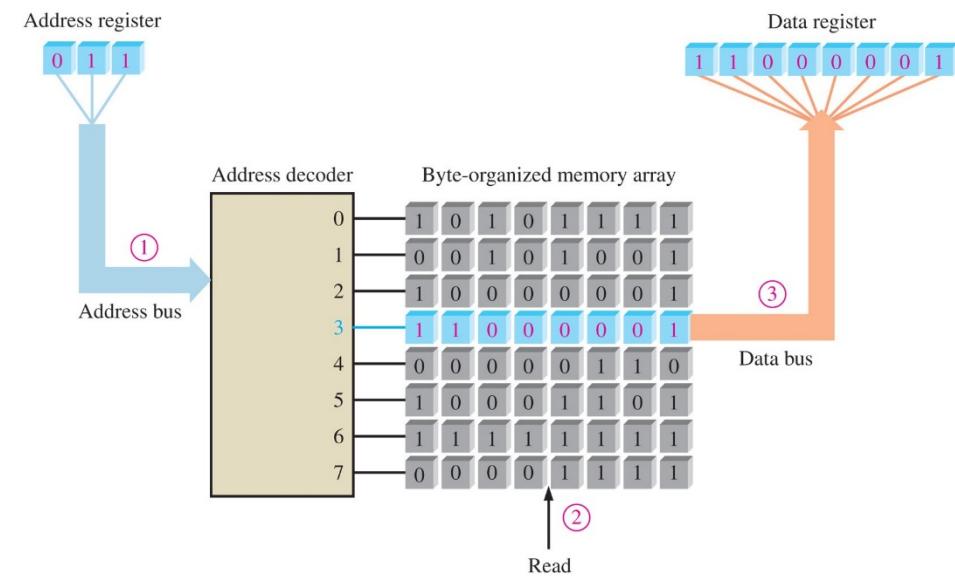


① Address code 101 is placed on the address bus and address 5 is selected.

② Data byte is placed on the data bus.

③ Write command causes the data byte to be stored in address 5, replacing previous data.

- The address decoder decodes the address and selects the specified location in the memory.
- The memory then gets a **read** command, and a “copy” of the data byte that is stored in the selected memory address is placed on the **data bus** and loaded into the **data register**.



① Address code 011 is placed on the address bus and address 3 is selected.

② Read command is applied.

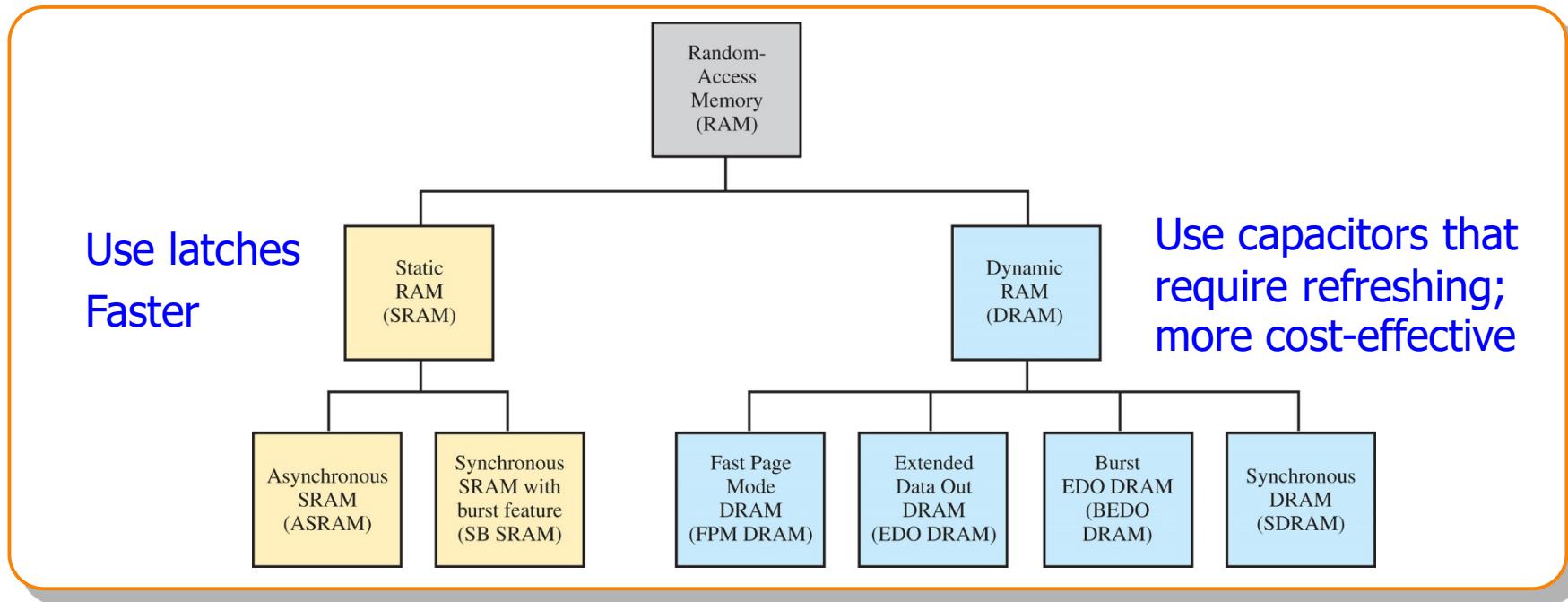
③ The contents of address 3 is placed on the data bus and shifted into data register. The contents of address 3 is not erased by the read operation.



RAMs and ROMs

□ Random-Access Memory (RAM)

- ◆ RAMs have both read and write capability
- ◆ RAMs lose stored data when power is off → **volatile** memories.



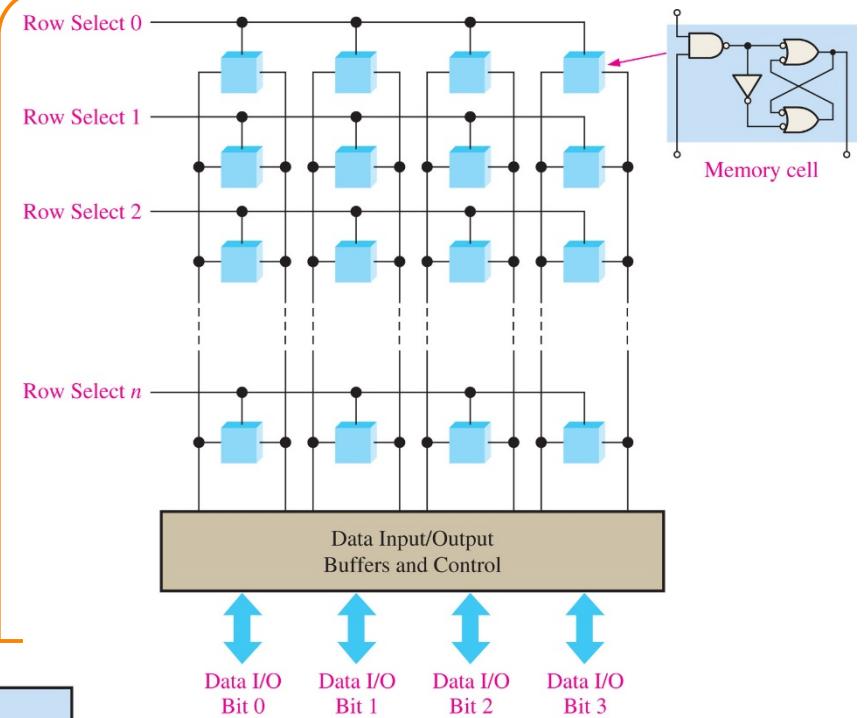
□ Read-Only Memory (ROM)

- ◆ Data can be read from a ROM, but there is no write operation
- ◆ ROMs retain stored data even if power is off → **nonvolatile** memories.



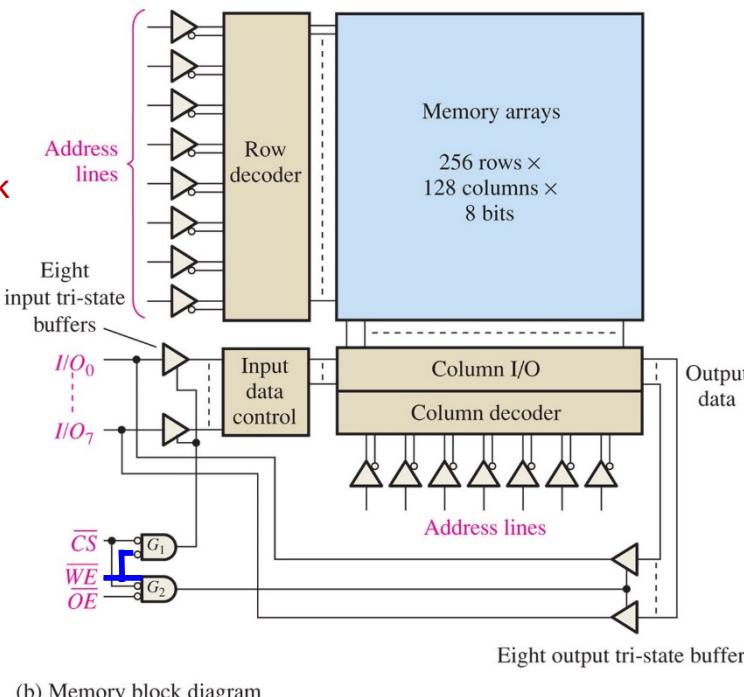
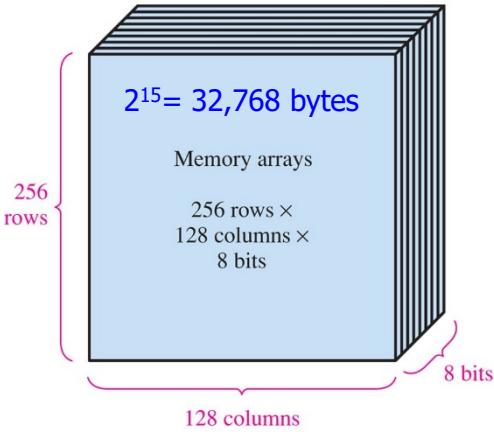
Static RAM (SRAM) I

- Basic SRAM array: All the cells in a row share the same Row Select line. Cells in the same column are connected to a single data line (Data I/O).



Basic Asynchronous SRAM Organization

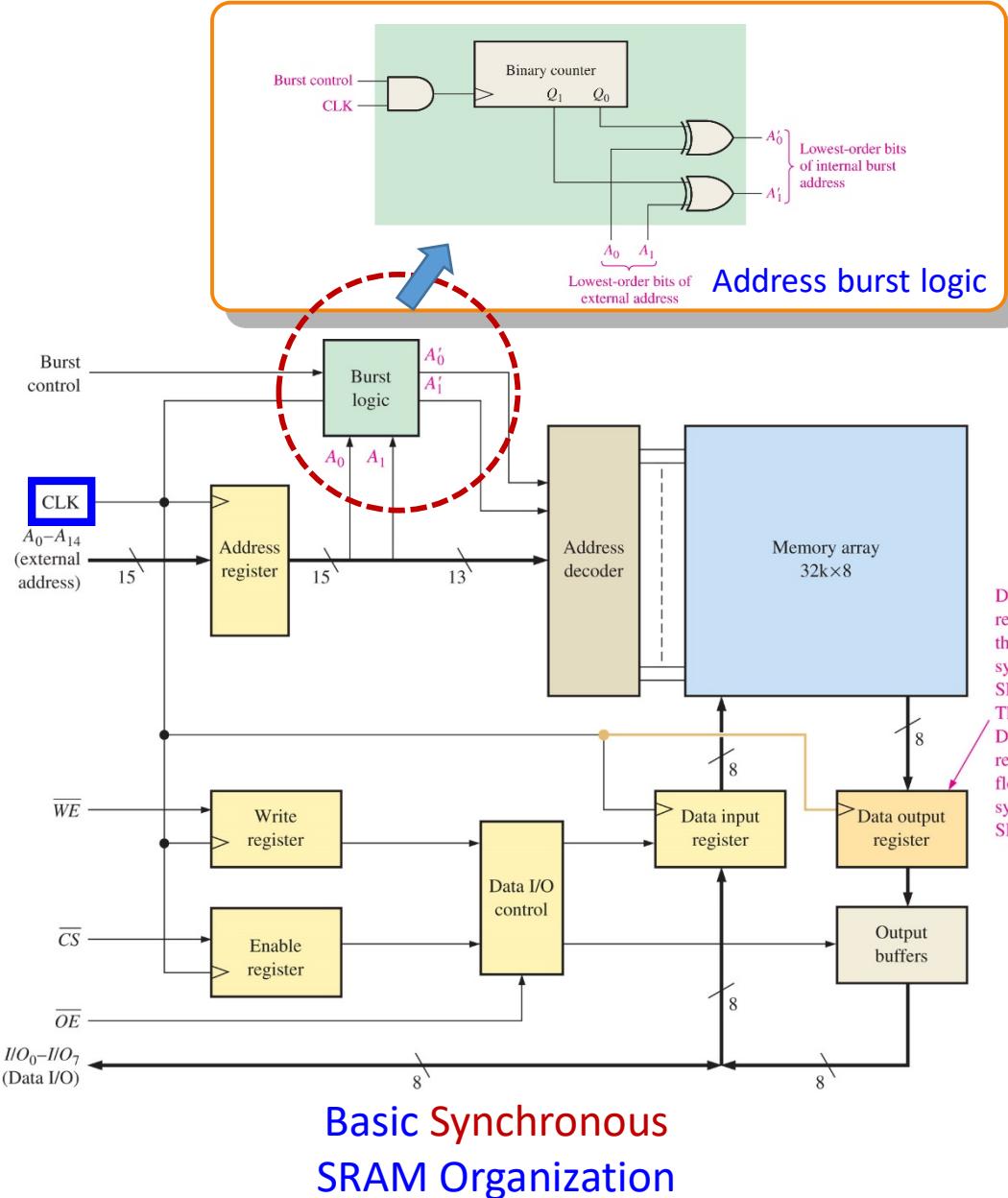
Not synchronized with a system clock



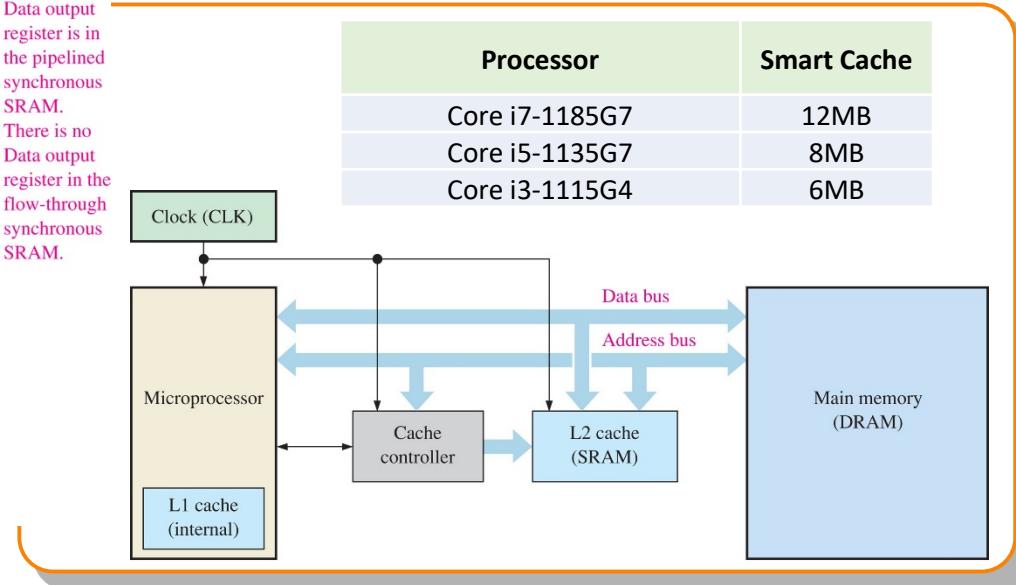
- READ: \overline{WE} is HIGH and \overline{OE} is LOW $\rightarrow G_1$ disabled and G_2 enabled
- WRITE: \overline{WE} is LOW and \overline{OE} is HIGH $\rightarrow G_1$ enabled and G_2 disabled



Static RAM (SRAM) II



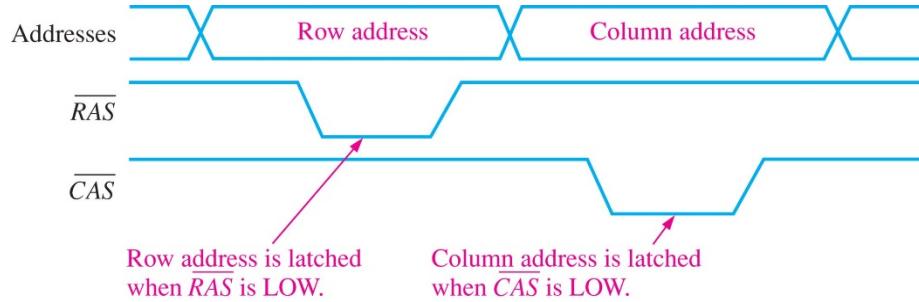
- Synchronous SRAM uses clocked registers to synchronize all inputs with the system clock.
- The Burst Feature can read or write up to **four** sequential locations using a **single** address.
- Cache Memory: small, high-speed memory (L1 and L2 Caches)



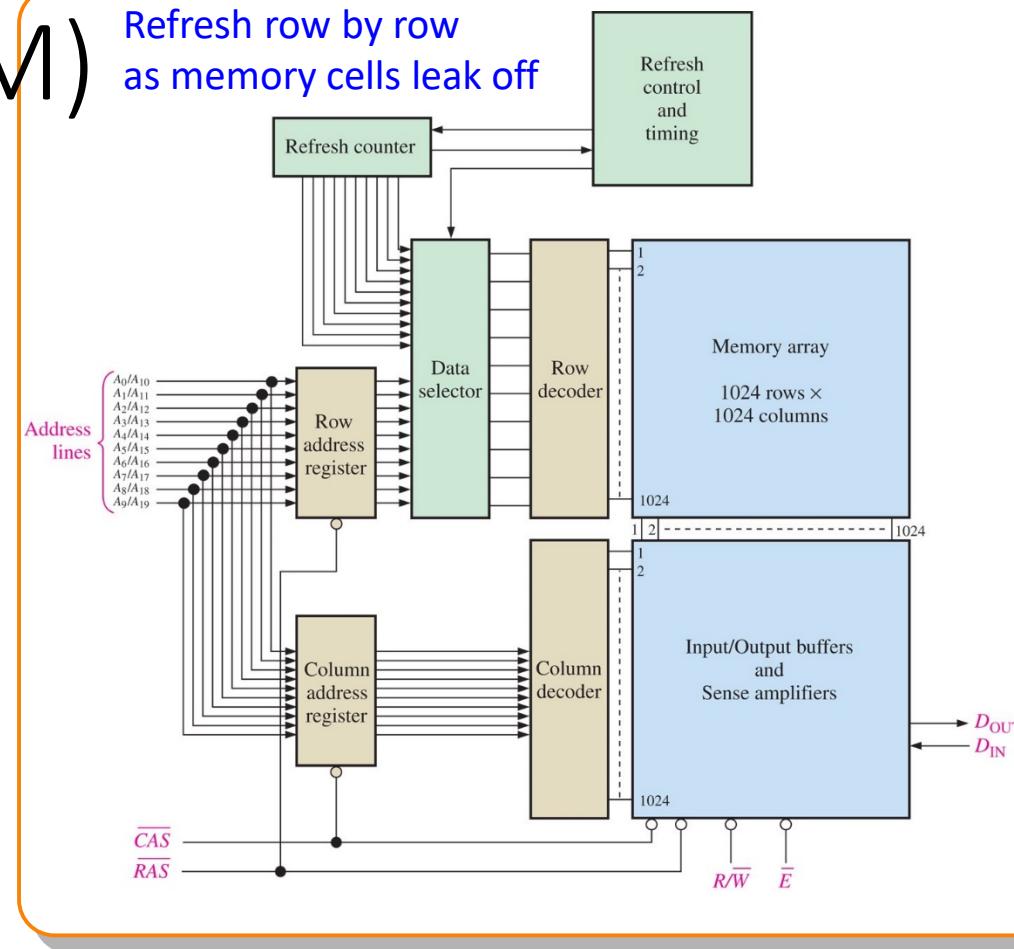
https://en.wikipedia.org/wiki/List_of_Intel_processors#Latest_desktop_and_mobile_processors_for_consumers



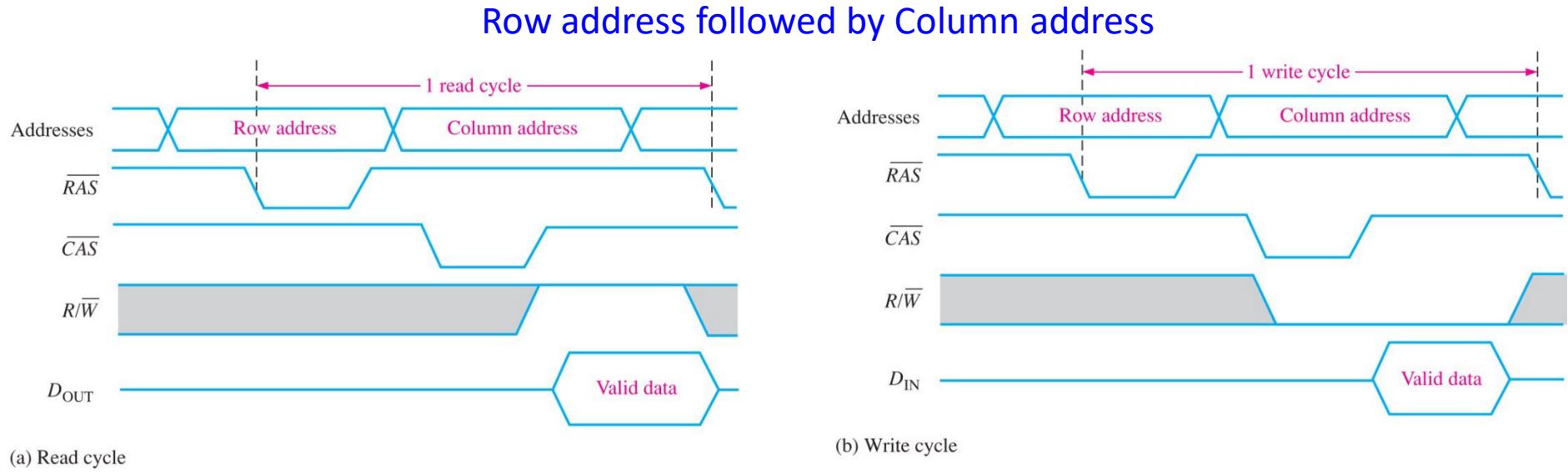
Dynamic RAM (DRAM)



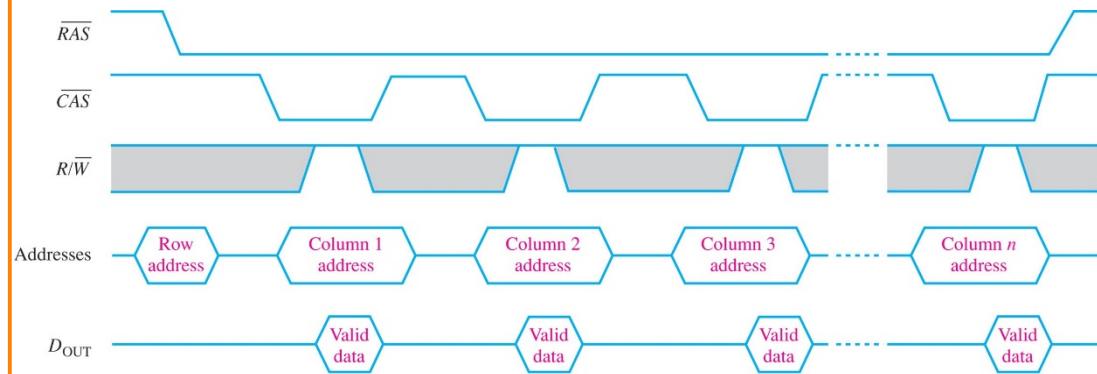
- The 10 address lines are time multiplexed at the beginning of a memory cycle by the row address select (RAS) and the column address select (CAS) into two separate 10-bit address fields.
- First, the 10-bit row address is latched into the row address register. Next, the 10-bit column address is latched into the column address register. The row address and the column address are decoded to select one of the 1M addresses ($2^{20} = 1,048,576$) in the memory array.



DRAM Read and Write Cycles



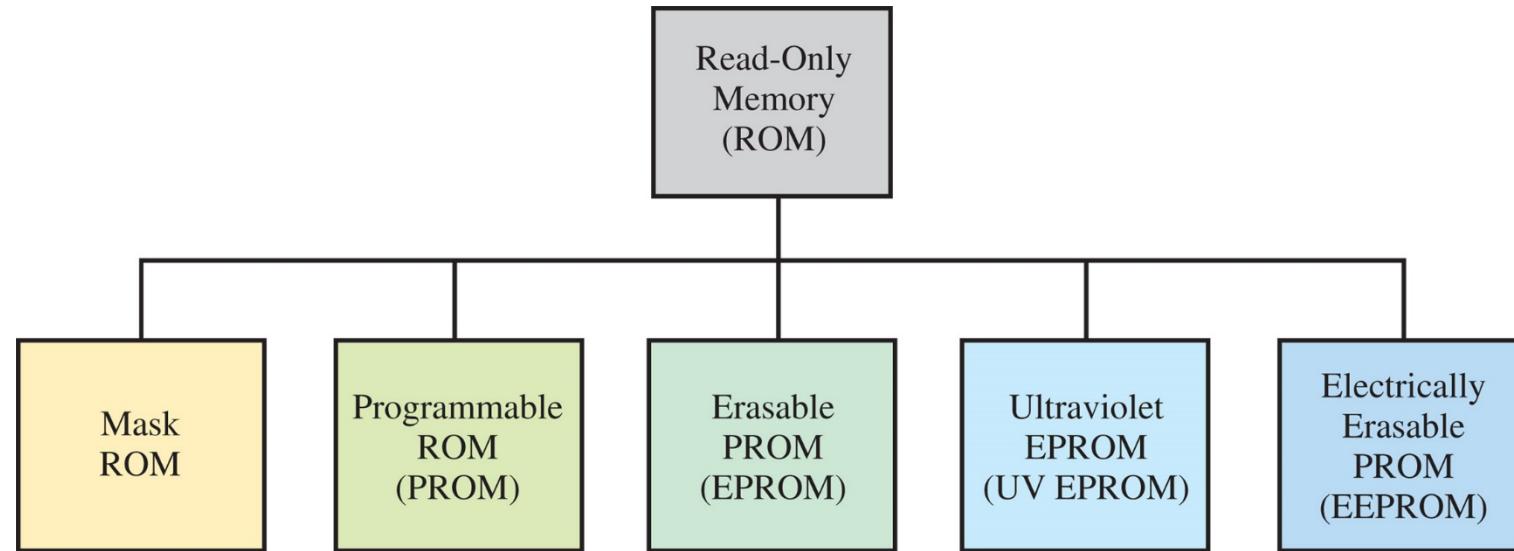
Fast Page Mode : same row but different columns



- Fast Page Mode (FPM) DRAM
- Extended Data Out (EDO) DRAM
- Burst Extended Data Out (BEDO) DRAM
- Synchronous DRAM (SDRAM)
- Double Data Rate (DDR) SDRAM



Read-Only Memory (ROM)



- A ROM contains permanently or semi-permanently stored data → Stored data will be retained even after the power is off (nonvolatile memories).
- Data stored in a ROM **cannot** be changed either (1) at all or (2) without specialized equipment.
- A ROM stores data that are used repeatedly in system applications, such as tables, conversions, or programmed instructions for system initialization and operation.

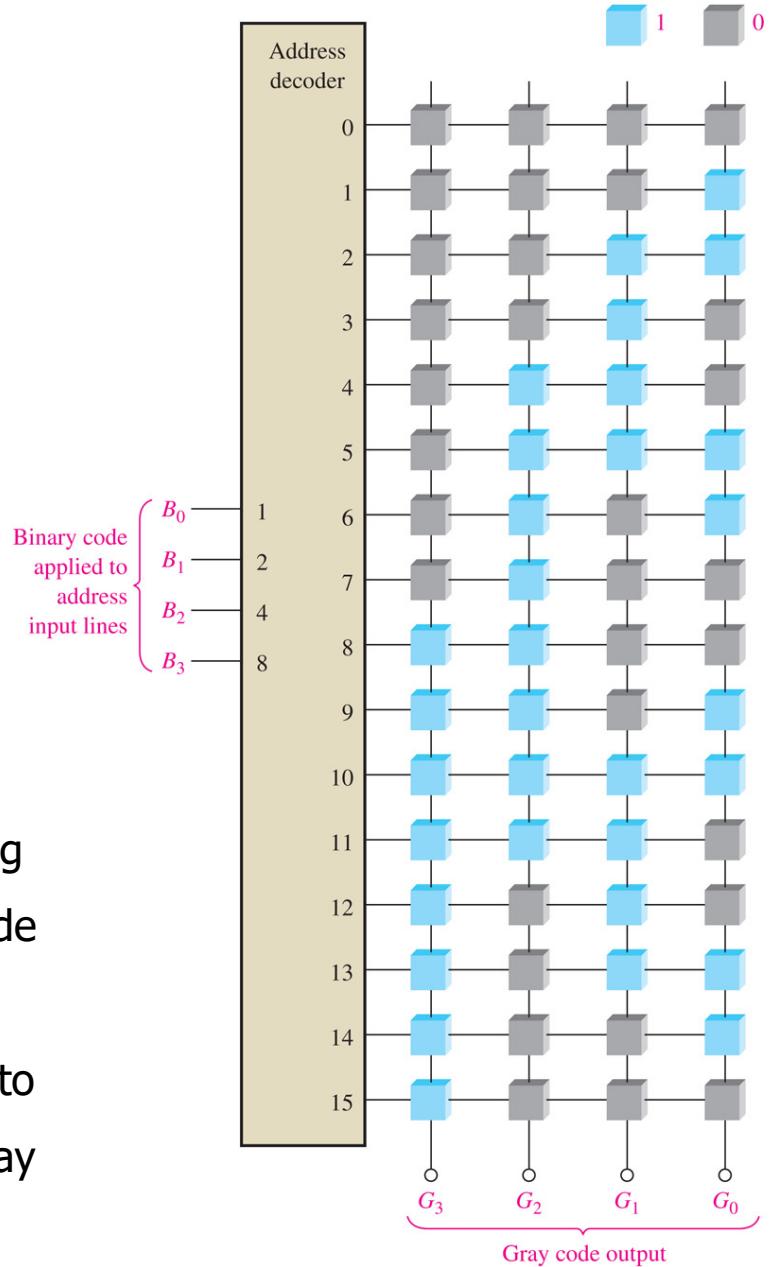


The Mask ROM

A basic ROM for a 4-bit binary-to-Gray conversion.

TABLE 11-1

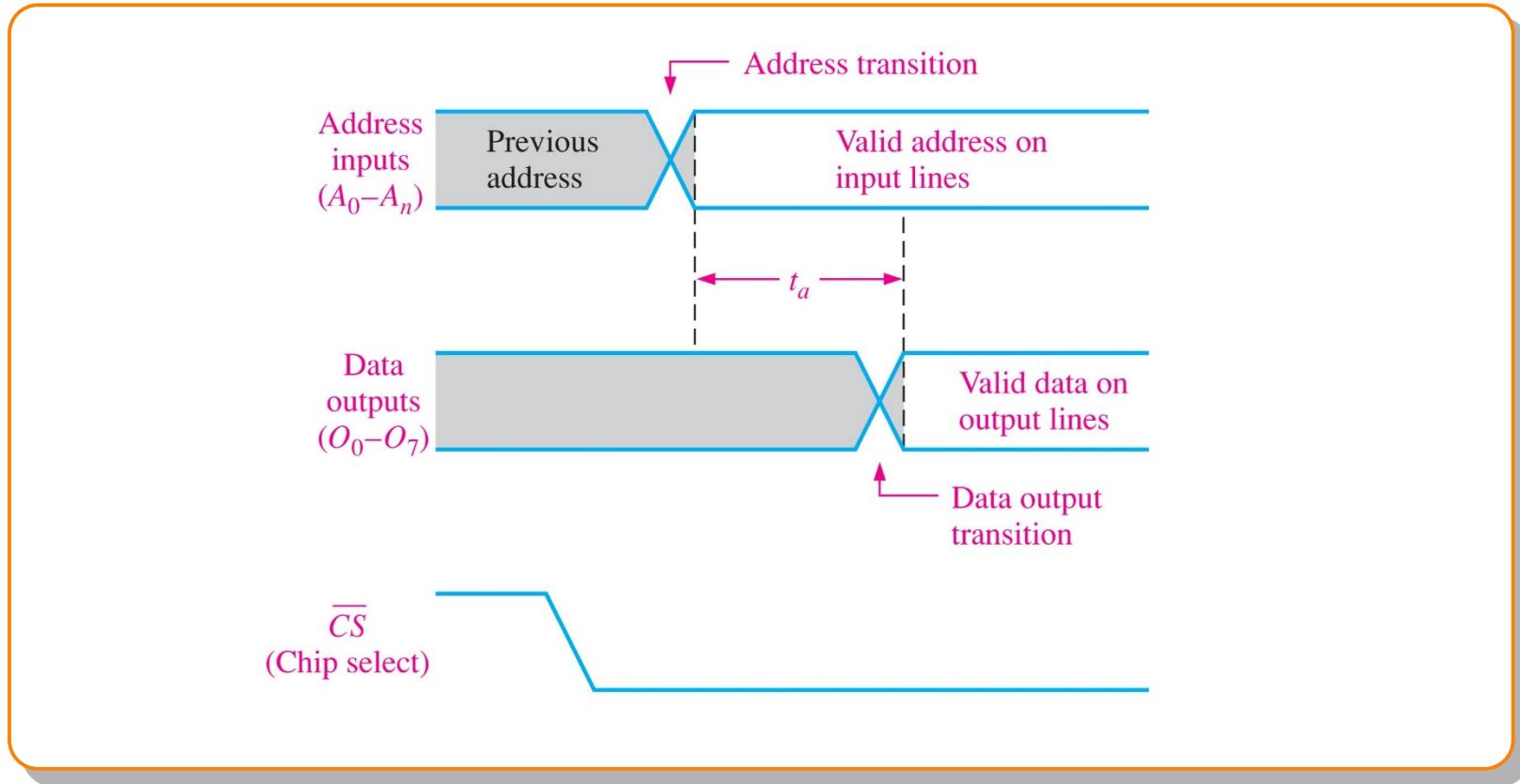
Binary				Gray			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0



- A binary code on the address input lines to the resulting 16 x 4 ROM array produces the corresponding Gray code on the output lines (columns).
- For example, when the binary number 0110 is applied to the address input lines, address 6, which stores the Gray code 0101, is selected.



ROM Access Time

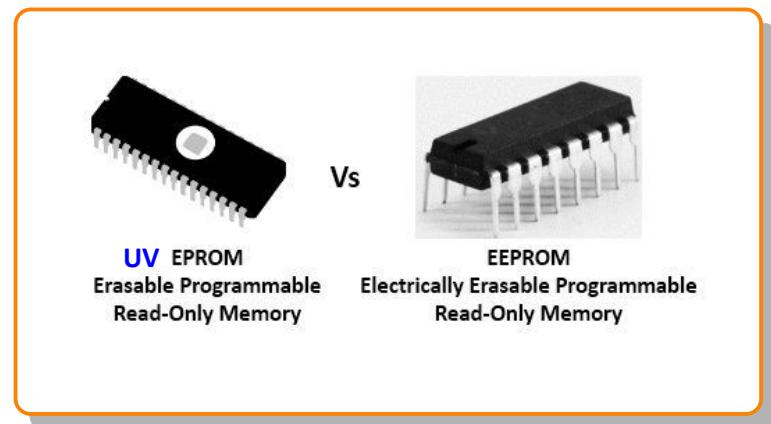


- The access time, t_a , of a ROM is the time from the application of a valid address code on the input lines until the appearance of valid output data.



Programmable ROMs

- Programmable ROM (PROM)
 - ◆ Use a fusing process to store bits → a memory link is burned open or left intact to represent a 0 or a 1. The fusing process is irreversible
- Erasable PROM (EPROM)
 - ◆ Can be reprogrammed if an existing program in the memory array is erased first.
 - ◆ Two basic types : EEPROM and UV EPROMs
- Electrically EPROM (EEPROM)
 - ◆ Erase and program with electrical pulses.
- Ultraviolet EPROM (UV EPROM)
 - ◆ Erasure is done by exposure of the memory array chip to high-intensity ultraviolet radiation through the UV window on top of the package.
 - ◆ The exposure time ranges from several minutes to an hour



The Flash Memory

- High-density read/write memories that are nonvolatile
- A flash memory cell consists of a single floating-gate MOS transistor. A data bit is stored as charge (0) or the absence of charge (1) on the floating gate.

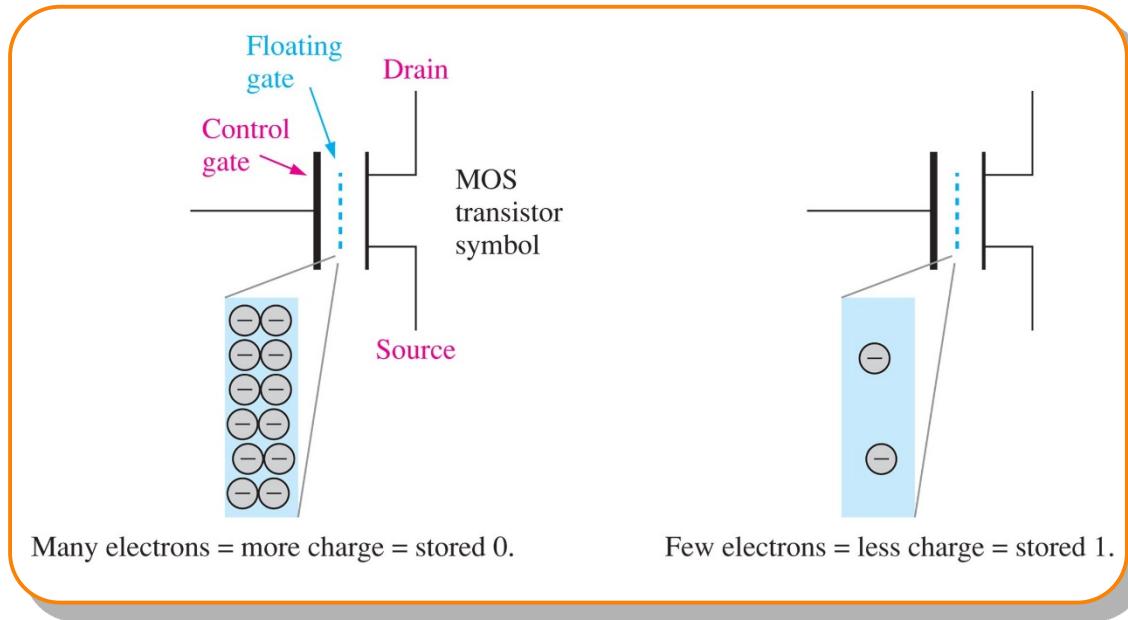
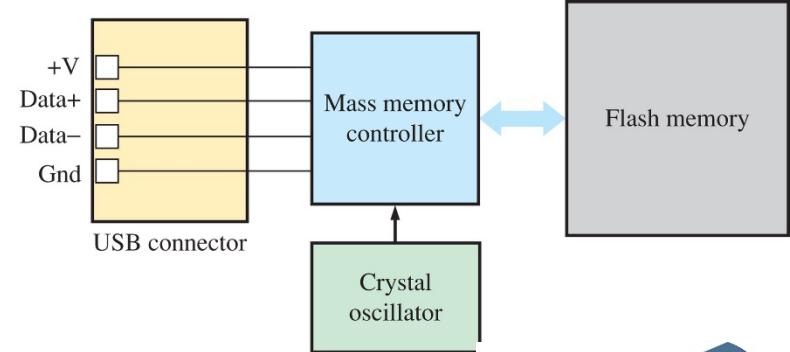


TABLE 11-2

Comparison of types of memories.

Memory Type	Nonvolatile	High-Density	One-Transistor Cell	In-System Writability
Flash	Yes	Yes	Yes	Yes
SRAM	No	No	No	Yes
DRAM	No	Yes	Yes	Yes
ROM	Yes	Yes	Yes	No
EEPROM	Yes	No	No	Yes
UV EPROM	Yes	Yes	Yes	No

A flip-flop of several transistors



(b) Basic block diagram



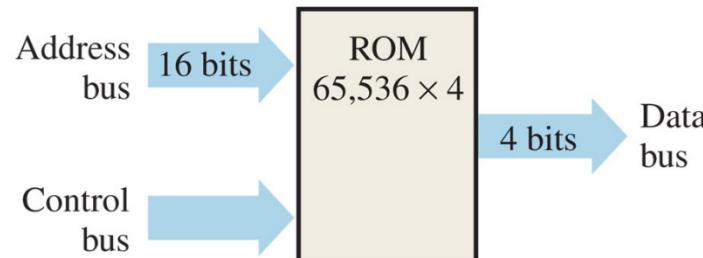
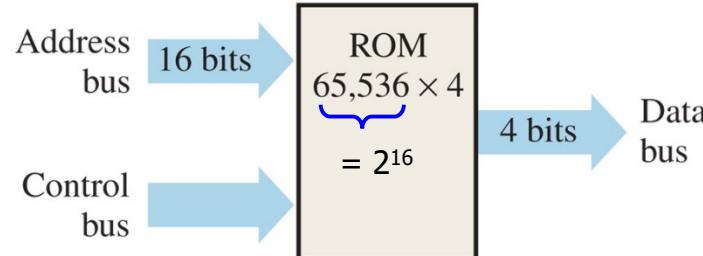
USB Flash Drive

(a) Typical USB flash drive



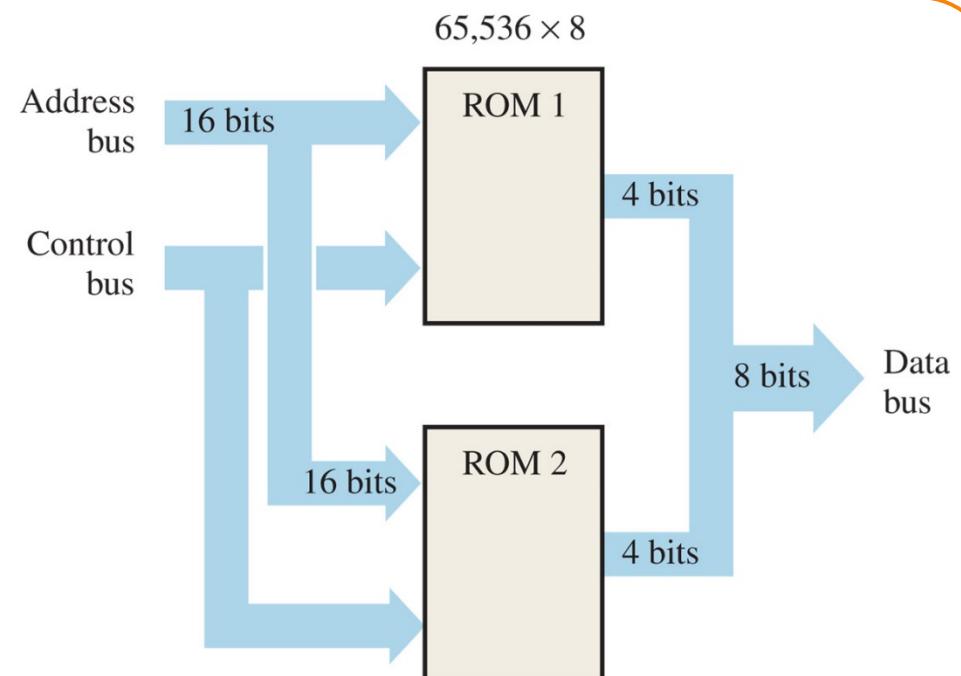
Memory Expansion

- The 16-bit address bus is commonly connected to both memories
- The 4-bit data buses from the two memories are combined to form an 8-bit data bus.
- When an address is selected, 8 bits are produced on the data bus, 4 from each memory.



(a) Two separate $65,536 \times 4$ ROMs

Without Memory Expansion : 4 bits



(b) One $65,536 \times 8$ ROM from two $65,536 \times 4$ ROMs

With Memory Expansion : 8 bits



Special Memories : First In–First Out (FIFO)

Conventional Shift Register					
Input	X	X	X	X	Output
0	0	X	X	X	→
1	1	0	X	X	→
1	1	1	0	X	→
0	0	1	1	0	→

X = unknown data bits.

In a conventional shift register, data stay to the left until “forced” through by additional data.

FIFO Shift Register					
Input	—	—	—	—	Output
0	—	—	—	0	→
1	—	—	1	0	→
1	—	1	1	0	→
0	0	1	1	0	→

— = empty positions.

In a FIFO shift register, data “fall” through (go right).

- In a conventional register, a data bit moves through the register only as new data bits are entered; in a FIFO register, a data bit **immediately** goes through the register to the right-most bit location that is empty.
- Applications: When two systems of differing data rates must communicate, data can be entered into a FIFO register at one rate and taken out at another rate.



(a) Irregular telemetry data can be stored and retransmitted at a constant rate.



(b) Data input at a slow keyboard rate can be stored and then transferred at a higher rate for processing.



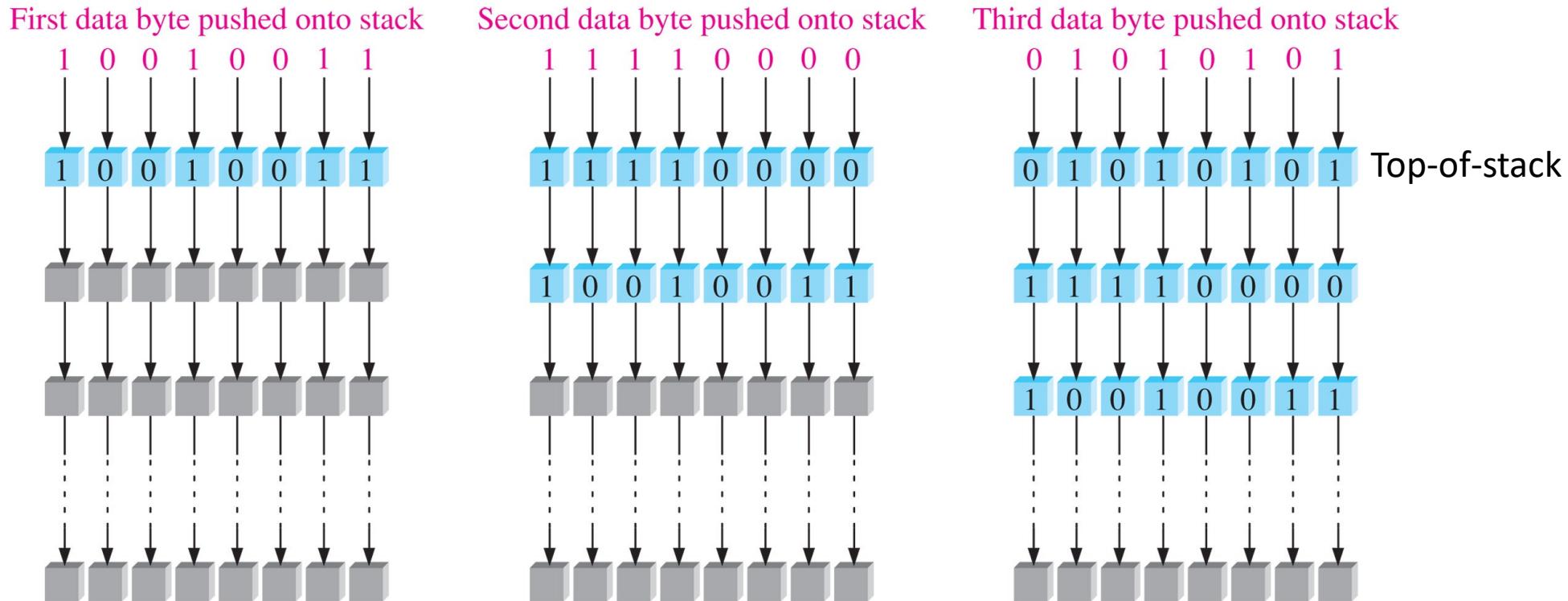
(c) Data input at a constant rate can be stored and then output in bursts.



(d) Data in bursts can be stored and reformatted into a constant-rate output.



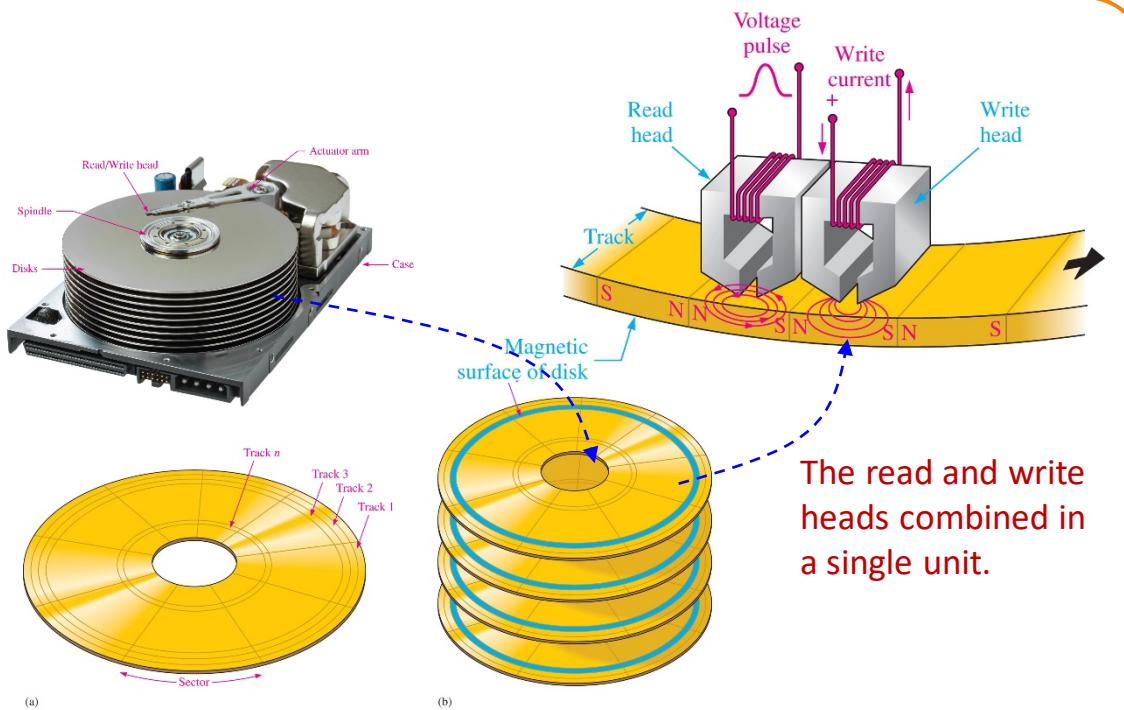
Special Memories : Last In–First Out (LIFO)



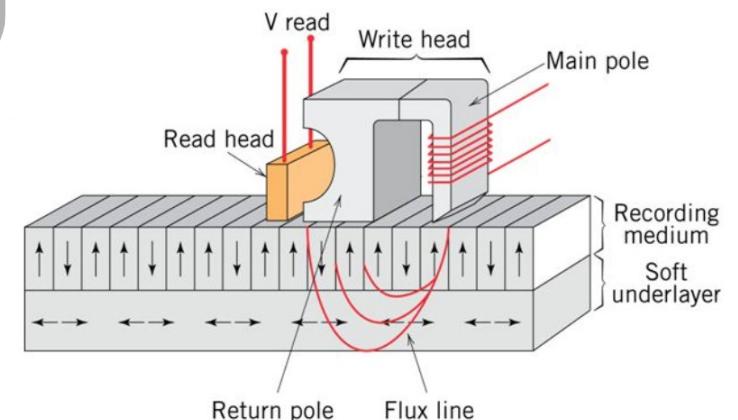
- ❑ A LIFO memory is commonly referred to as a push-down stack. In some systems, it is implemented with a group of registers with the register at the top being called the top-of-stack.
- ❑ The new data byte is always loaded into the top register and the previously stored bytes are pushed deeper into the stack.



Magnetic Hard Disks



- The direction or polarization of the magnetic domains on the disk surface is controlled by the direction of the magnetic flux lines (magnetic field) produced.
- This magnetic flux magnetizes a small spot on the disk surface in the direction of the magnetic field.
- Hard Disk performance : seek time, rotation speeds (rpm)



- A magnetized spot of one polarity represents a binary **1**, while the other polarity **0**. Once magnetized, the spot remains until written over with an opposite magnetic field.
- When the magnetic surface passes a read head, the magnetized spots produce magnetic fields in the read head, which induces voltage pulses in the winding. The polarity of these pulses \rightarrow 1 or 0

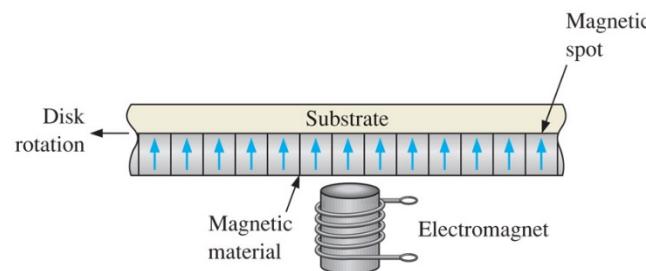


Magneto-Optical (MO) Storage

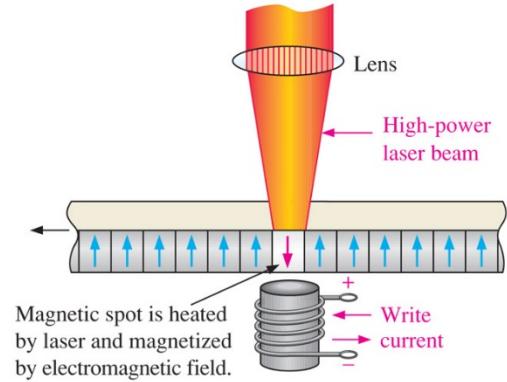
- A combination of magnetic and optical (laser) technologies



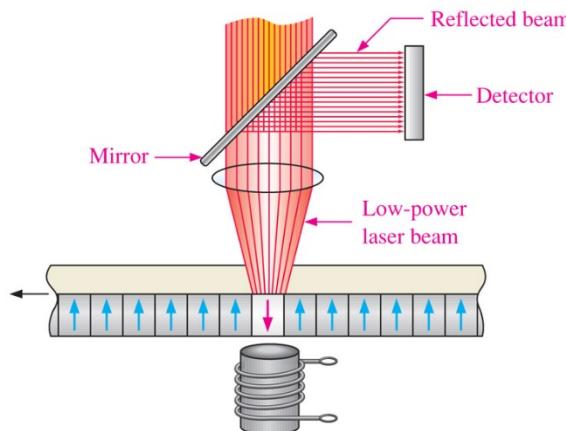
- Magnetic coating used on the MO disk requires heat to alter the magnetic polarization.
- MO is extremely stable at ambient temperature.
- To write a data bit, a high-power laser beam is focused on a tiny spot on the disk.



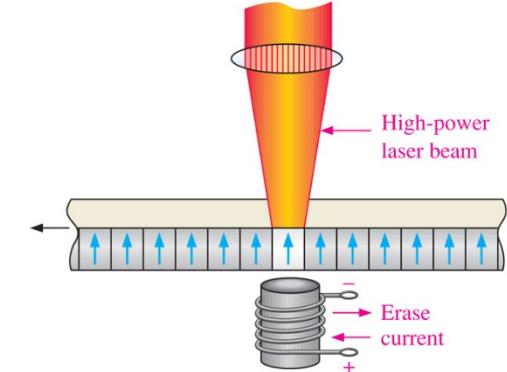
(a) Unrecorded disk



(b) Writing: A high-power laser beam heats the spot, causing the magnetic particles to align with the electromagnetic field.



(c) Reading: A low-power laser beam reflects off of the reversed-polarity magnetic particles and its polarization shifts. If the particles are not reversed, the polarization of the reflected beam is unchanged.



(d) Erasing: The electromagnetic field is reversed as the high-power laser beam heats the spot, causing the magnetic particles to be restored to the original polarity.



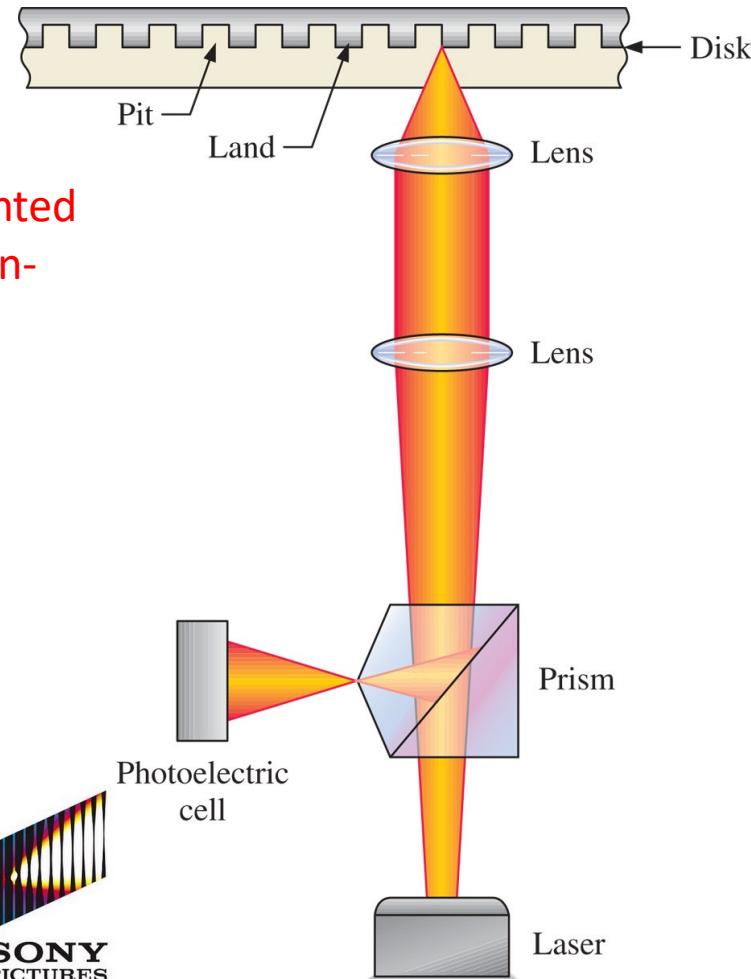
Optical Storage

- CD-ROM (Compact Disk–Read-Only Memory)
 - ◆ Capacity of 680 MB
 - ◆ The data are stored in pits and lands. Laser light reflected from a pit is 180° out-of-phase with the light reflected from the lands.
- WORM (Write Once/Read Many)
- CD-R
- CD-RW
 - ◆ The data can be erased or overwritten by heating to a temperature above the crystallization temperature but lower than the melting temperature that causes the material to revert to a crystalline state.
- DVD–ROM
 - ◆ Data on both sides with multiple layers on each side.
- Blu-Ray : Blu-Ray (SONY) versus HD DVD (Toshiba)
2002-2008



Norio Ohga (大賀 典雄)

" to contain the entire Beethoven's Ninth Symphony on one disc"



香港中文大學(深圳)

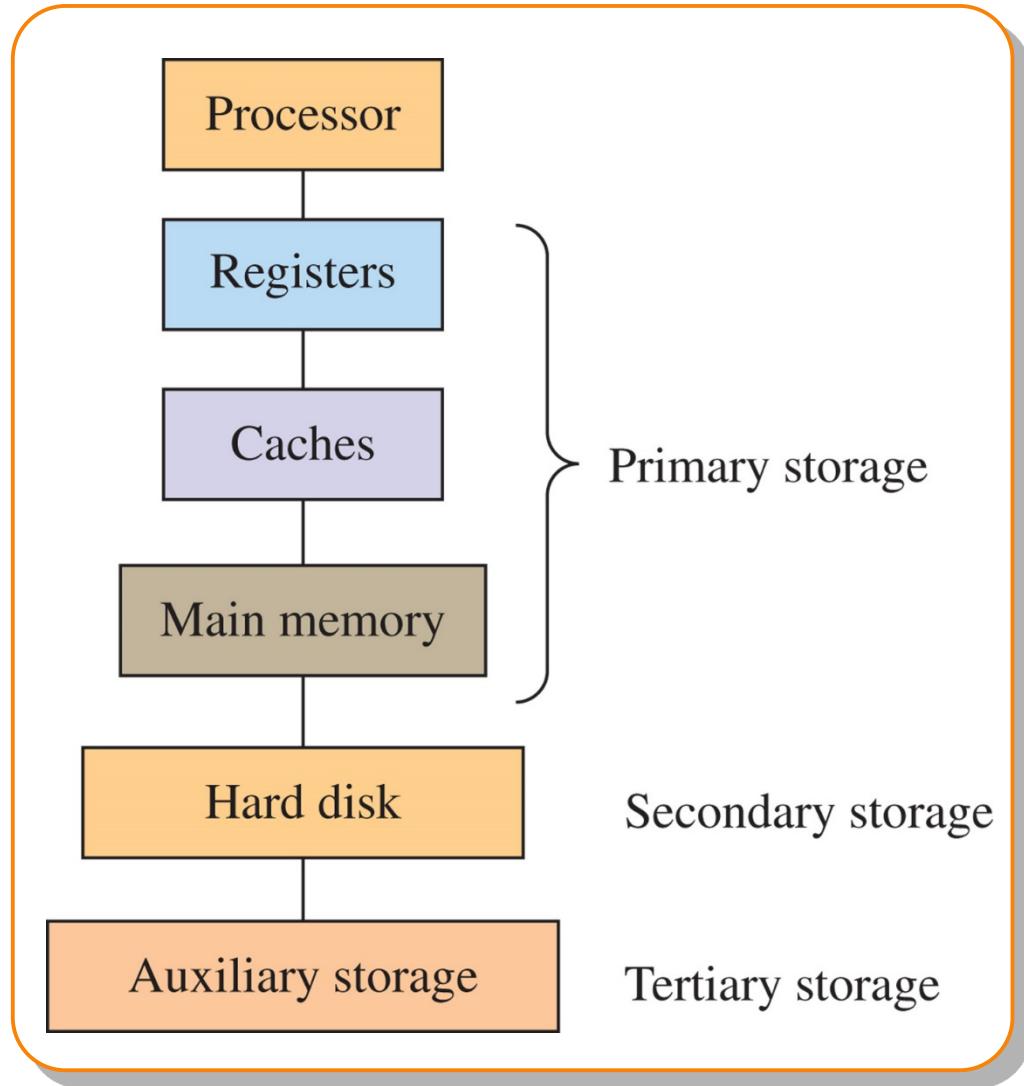
The Chinese University of Hong Kong, Shenzhen



PlayStation

Memory Hierarchy

- Memory can be classified according to its “distance” from the processor in terms of the number of machine cycles or access time required to get data for processing.
- Faster memory elements are closer to the processor as compared to slower types of memory elements.
- The cost per bit is much greater for the memory close to the processor than for the memory that is further from the processor.

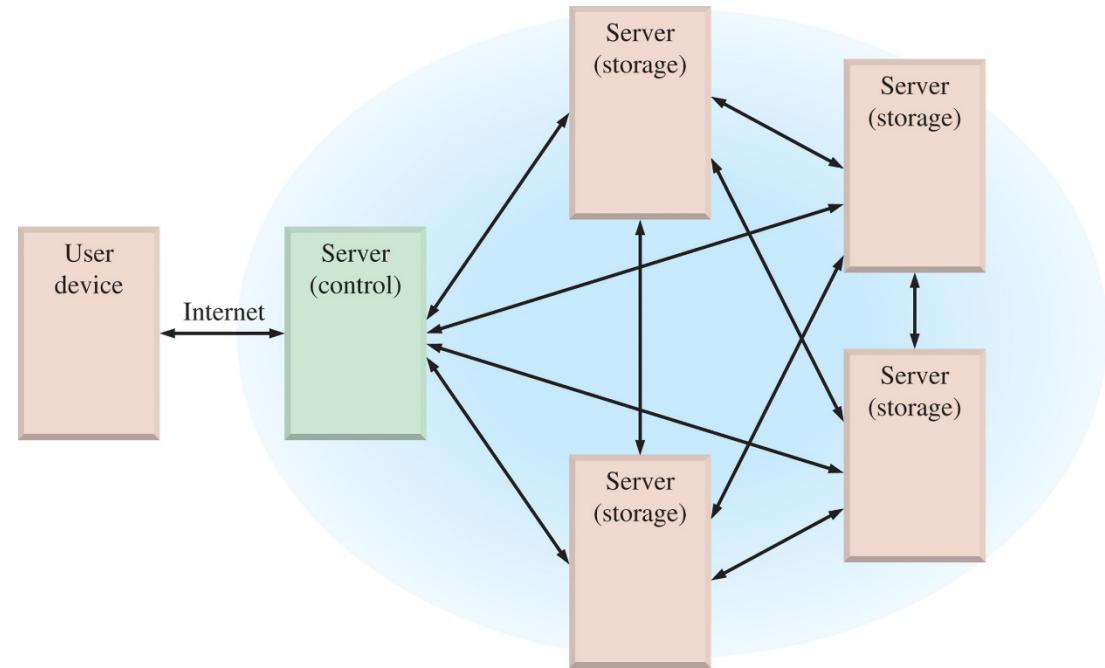


$$1 \text{ TB} = 10^{12} \text{ B} \xrightarrow{\text{terabyte}} 1 \text{ PB} = 1,000 \text{ TB} = 10^{15} \text{ B} \xrightarrow{\text{petabyte}}$$



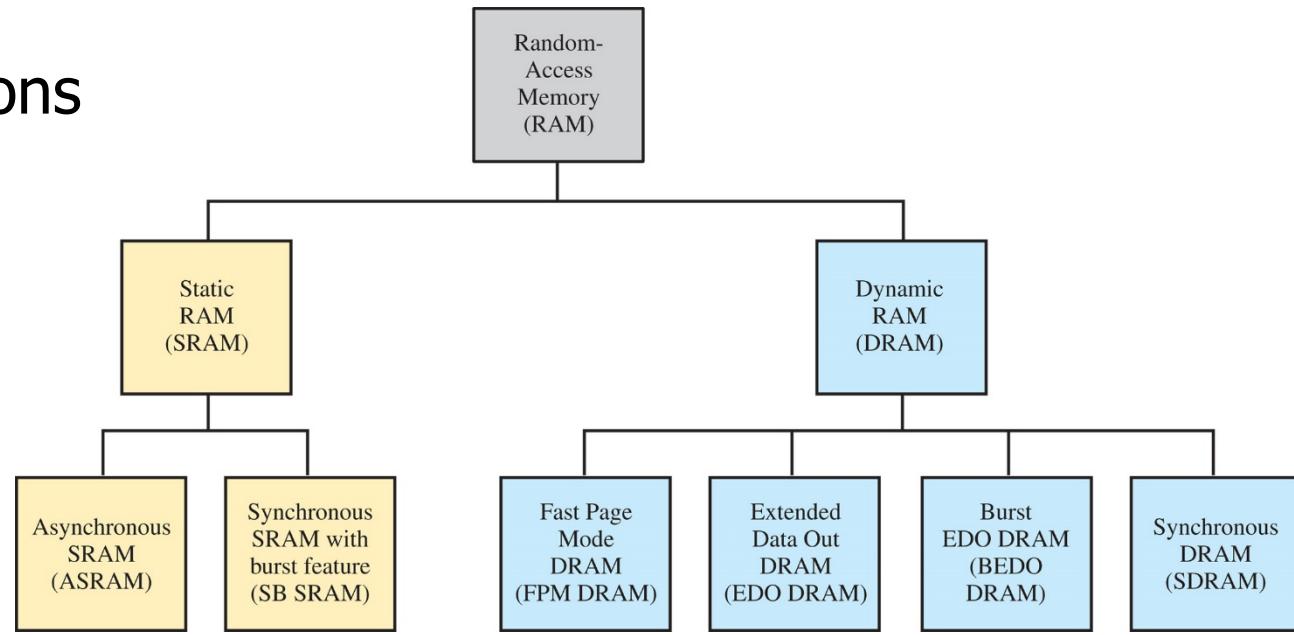
Cloud Storage

- When a client sends data to the cloud, it is stored in multiple servers. This redundancy guarantees availability of data at any time to the client and makes the system highly reliable.
- Data can be stored and retrieved in any physical location that has Internet access.
- Easy for data sharing, i.e., other people can access your data
- Cloud storage can be protected by (1) Encryption or encoding (2) Authentication and (3) Authorization.



Chapter Review

- Addressing
- Read & Write Operations
- RAM and ROM
- Flash Memory
- Special Memories
 - ◆ First In–First Out (FIFO)
 - ◆ Last In–First Out (LIFO)
- Magnetic and Optical Storage : Hard disks, Magneto-Optical storage, Optical storage
- Memory Hierarchy
- Cloud Storage



True/False Quiz

- A nibble consists of eight bits.
- A memory cell can store a byte of data.
- The location of a unit of data in a memory array is called its address.
- A data bus is bidirectional in operation.
- RAM is a random address memory.
- Data stored in a static RAM is retained even after power is removed.
- Cache is a type of memory used for intermediate or temporary storage of data.
- Dynamic RAMs must be periodically refreshed to retain data.
- ROM is a read-only memory.
- A flash memory uses a flashing beam of light to store data.
- Registers are at the top of a memory hierarchy.
- Cloud storage is accessed through the Internet.



True/False Quiz

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