



EIE 2050 Digital Logic and Systems

Chapter 1 : Introductory Concepts

Simon Pun, Ph.D.



Teaching Team

Online students please email instructors
to make one-on-one appointments

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L2 Session	Online	On-Campus
Mon 16:00-17:30	Zoom Mtg ID: 98274056989 (Passcode: 2050)	TD 105
Wed 16:00-17:30	Zoom Mtg ID: 94473534454 (Passcode: 2050)	
L3 Session	Online	On-Campus
Tue 10:30-12:00	Zoom Mtg ID: 96024558084 (Passcode: 2050)	TD 105
Thur 10:30-12:00	Zoom Mtg ID: 93339739079 (Passcode: 2050)	

- **Instructor:**

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- **Office Hour:** Fri 15:00-16:00 (CD405)

L1 Session	Online	On-Campus
Tue 9:00-10:30	Zoom Mtg ID: 99780040447 (Passcode: 2050)	TC 103
Thur 9:00-10:30	Zoom Mtg ID: 93791101089 (Passcode: 2050)	



Teaching Team (PhD TAs)

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Teaching Team (USTFs)

<ul style="list-style-type: none">• Name: Ms. Zihan Chen (陈子涵)• Office: Old Lib, 103• Email: 120090347@link.cuhk.edu.cn• Office Hour: Mon 19:00-20:00	<ul style="list-style-type: none">• Name: Mr. Shengguang Cui (崔圣光)• Office: TD 301• Email: 120090221@link.cuhk.edu.cn• Office Hour: Tue 21:00-22:00	<ul style="list-style-type: none">• Name: Ms. Chengle Zheng (郑成乐)• Office: Old Lib, 103• Email: 120090279@link.cuhk.edu.cn• Office Hour: Fri 16:00-17:00
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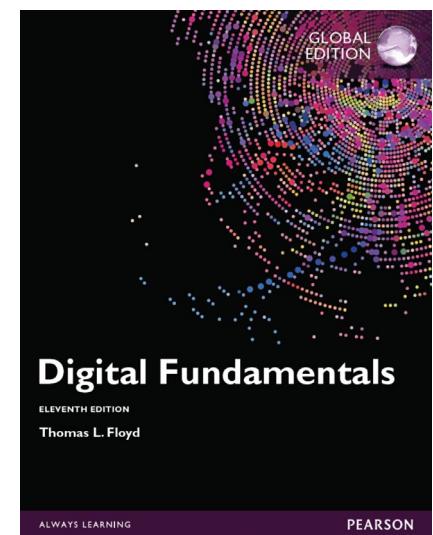
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Tue 19:00-20:00		
Tue 20:00-21:00		
Wed 18:00-19:00	Zoom Mtg ID: 98460805131 (Passcode: 2050)	
Wed 19:00-20:00		TD 301
Thur 18:00-19:00	Zoom Mtg ID: 3454503990 (Passcode: 2050)	
Thur 19:00-20:00	Zoom Mtg ID: 9833616889 (Passcode: 2050)	
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Fri 19:00-20:00		



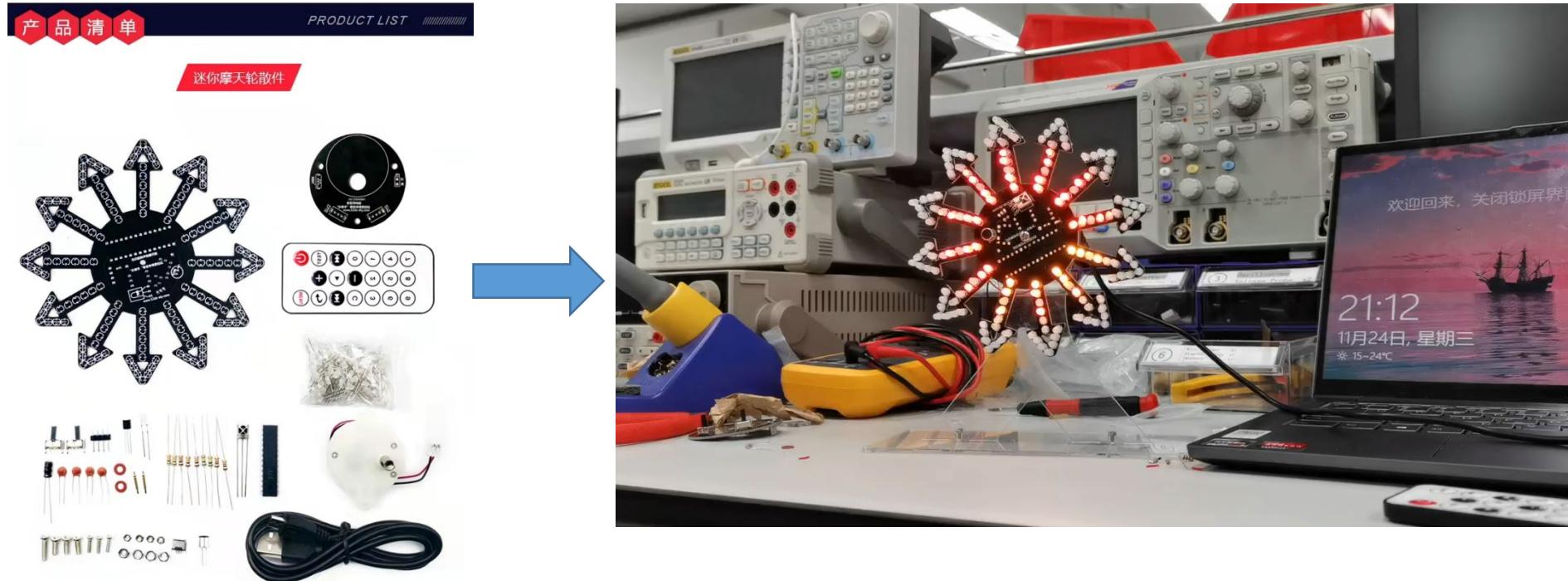
Course Outline

Description	This course gives science and engineering students exposure to the basic concepts and techniques in digital logic and system design. Topics include digital system concepts, numbering systems and codes, Boolean algebra, logic gates and logic circuit elements, logic functions and simplification, logic circuits design, latches and flip-flops, counters, registers, memory and storage systems, SPLD, CPLD, FPGA, and introduction to CAD tools and VHDL.
Textbook	Digital Fundamentals (Global Edition, 11th Edition), by Thomas Floyd, Pearson 2015.

Assessment	% weight
Assignments	10%
In-class quizzes	10%
Project	5%
Mid-term Test	30%
Final Exam	45%



Last Year's Project



From Marriage Proposals to Final Exam



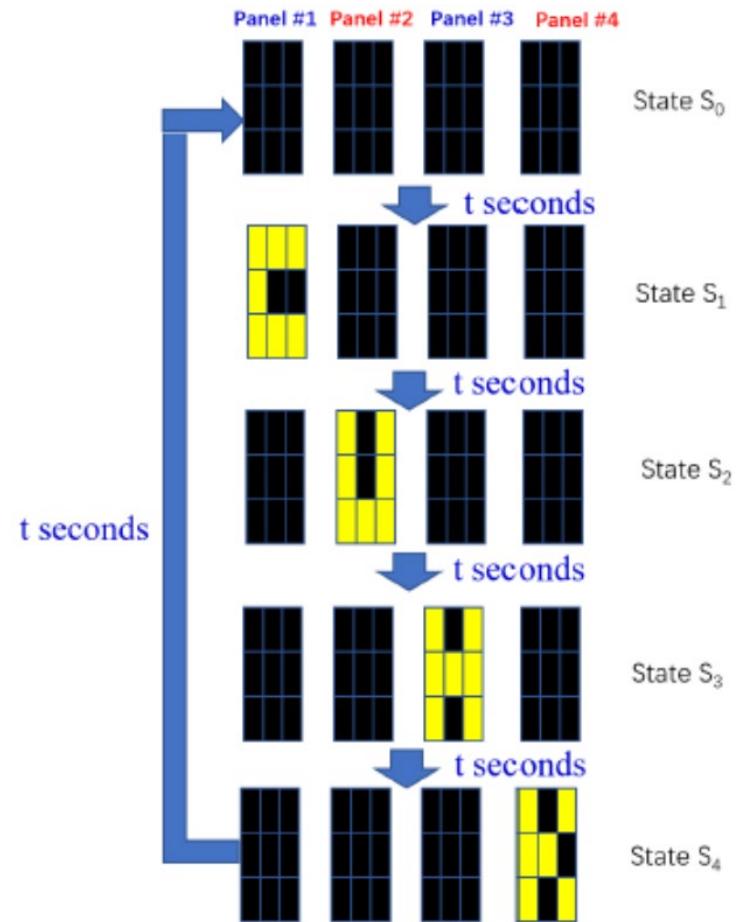
A real story
happened at
Harmonia
last year

A real problem in previous EIE 2050 final exam

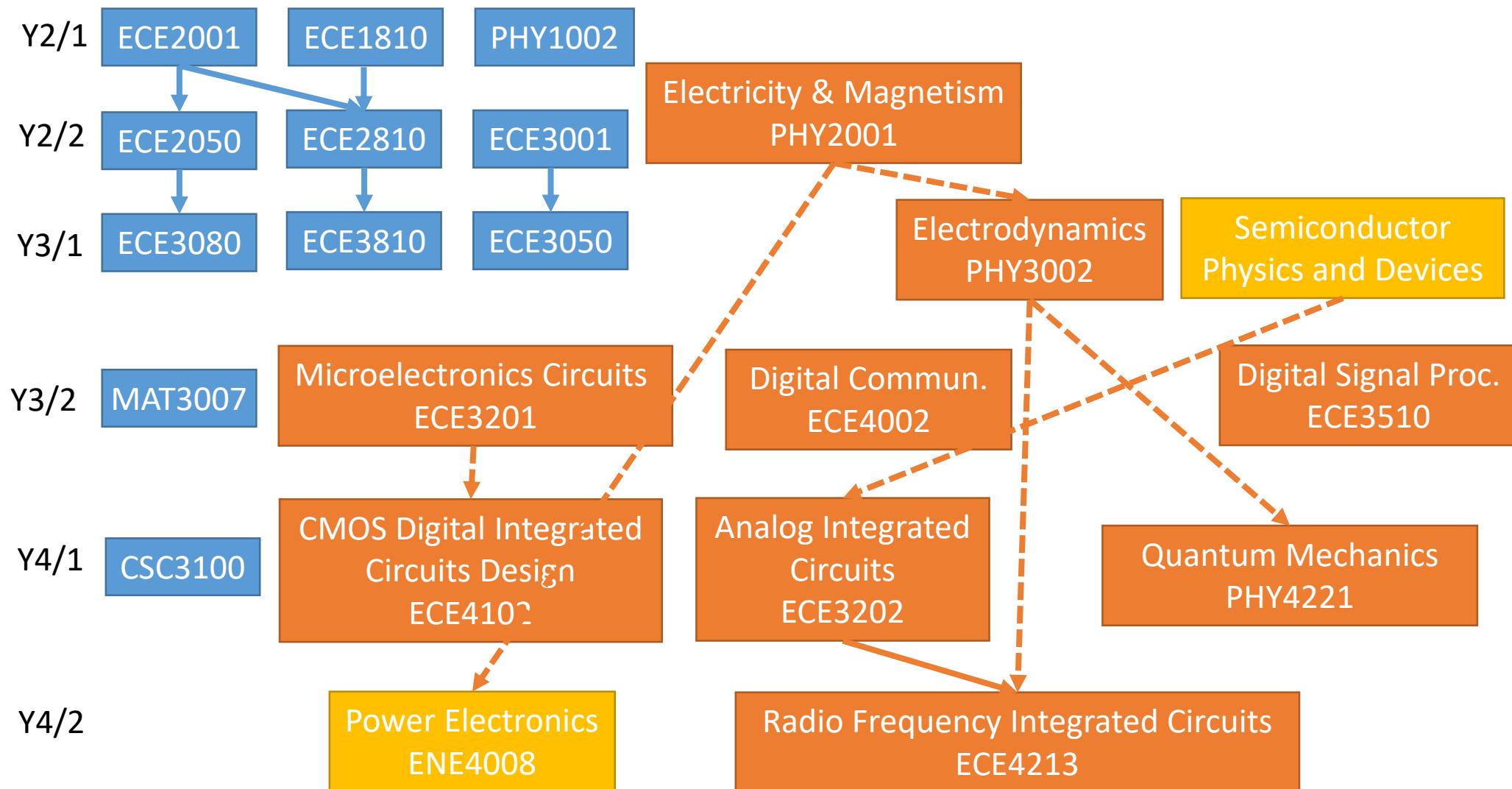
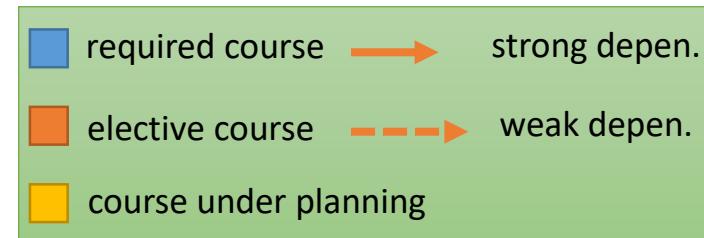
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EIE 2050 Digital Logic and Systems

10. (15 points) Four illumination panels showing “C”, “U”, “H” and “K” have been set up on the upper campus.



Course Map: Circuits



Teaching Plan

Week		Content/ topic/ activity
1	1/4 - 1/10	Ch1. Introductory concepts Digital and analog quantities, Binary digits, logic levels and digital waveforms, Basic logic operations, System concept, Fixed-function integrated circuits
2	1/11 - 1/17	Ch2. Number systems, operations and codes Number systems and conversions, Binary arithmetic and operations, Signed numbers and operations, Binary coded decimal, Digital codes, Error detection codes
	1/18 - 2/7	Holidays
3	2/8 - 2/14	Ch3. Logic gates The inverter, Logic gates (AND, OR, NAND, NOR, XOR, XNOR), Fixed-function logic
4	2/15 - 2/21	Ch4. Boolean algebra and logic simplification Boolean operations, Boolean algebra, De Morgan's theorem, Boolean analysis of logic circuits, Simplification using Boolean algebra, Standard forms, Truth tables, Karnaugh map and minimization
5	2/22 - 2/28	Ch5. Combinational logic analysis Basic combinational logic circuits and implementation, the universal property, Combinational logic with NAND and NOR gates
6	3/1 - 3/7	Ch6. Functions of combinational logic Basic adders, Parallel adders, Comparators, Decoders, Encoders, Code converter



Teaching Plan (Cont.)

Week		Content/ topic/ activity
7	3/8 - 3/14	Ch6. Functions of combinational logic & Ch7. Latches and Flip-Flops Latches, Flip-flops, Flip-flop operating characteristics, Flip-flop applications
8	3/15 - 3/21	Midterm & Ch7. Latches and Flip-Flops
9	3/22 - 3/28	Ch7. Latches and Flip-Flops & Ch8. Shift registers
10	3/29 - 4/7	Ch8. Shift registers (Qingming Festival) Basic shift register operations, Serial and parallel registers, Applications
11	4/10 - 4/14	Ch9. Counters Asynchronous counters, Synchronous counters, Design, Applications
12	4/17 - 4/21	Ch9. Counters Asynchronous counters, Synchronous counters, Design, Applications
13	4/24 - 4/28	Ch10. Programmable logic SPLD, CPLD, FPGA, CAD tools, VHDL Ch11. Data Storage Memory basics, RAM, ROM, Flash memory, Magnetic and optical storage, Memory expansion

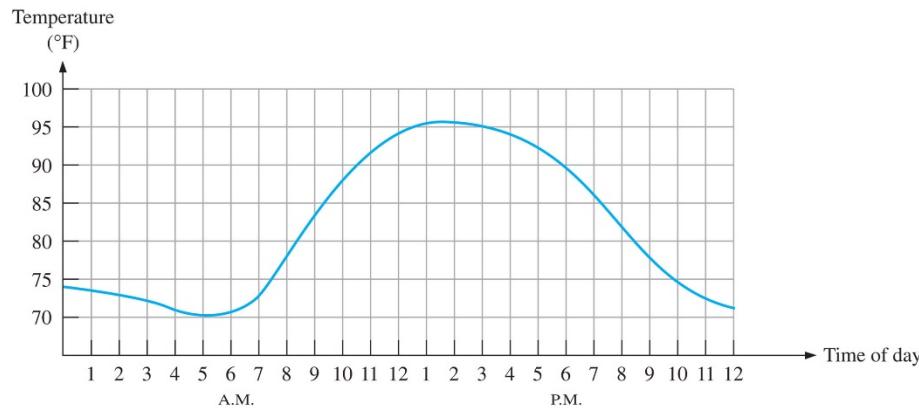


From Analog to Digital

Analog quantity : *continuous* values



Vinyl records
12 inches (~30cm), 3.5 hours



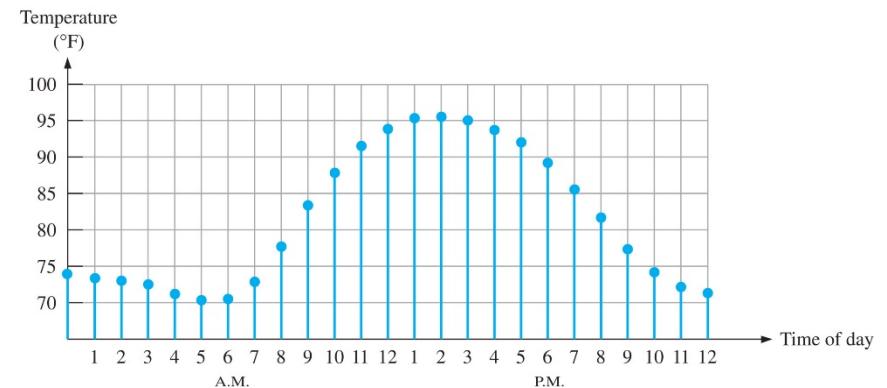
Analog temperature versus time

Digital quantity : *a discrete set* of values



Compact Disk (CD)
12cm, 74 minutes

Discretization



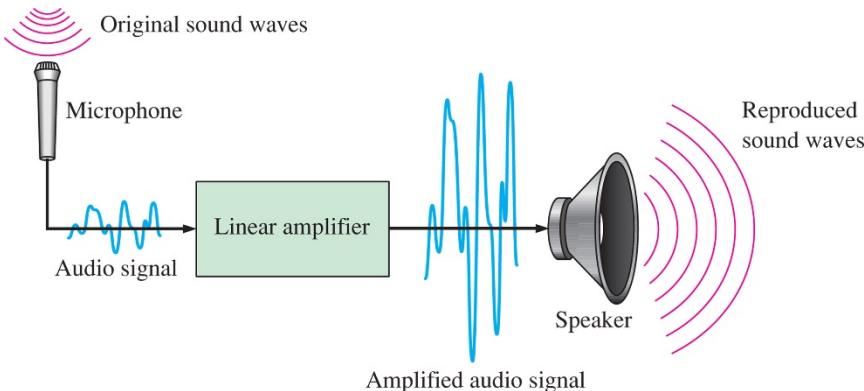
Digital temperature versus time



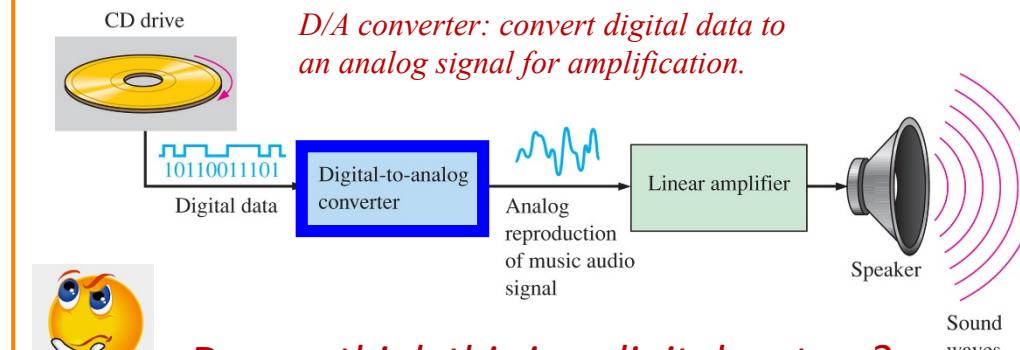
The Digital Advantages

- Digital data can be stored, processed and transmitted more efficiently and reliably
- Digital data is more noise resilient

A typical analog system



An audio system with a CD player

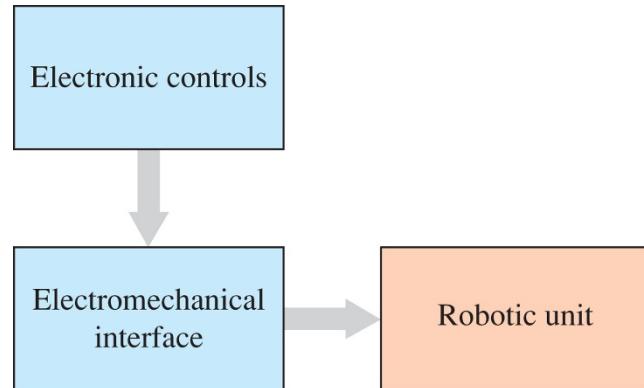


- Can you think of any disadvantages of digital systems?



Mechatronics

- **Mechatronics** = Mechanical + Electronic components
- Both digital and analog electronics are used



(a) Mechatronic system block diagram



(b) Robotic arm

- A digital computer controls functions such as braking, engine parameters, fuel flow, safety features, and monitoring.



Binary Digits and Logic Levels

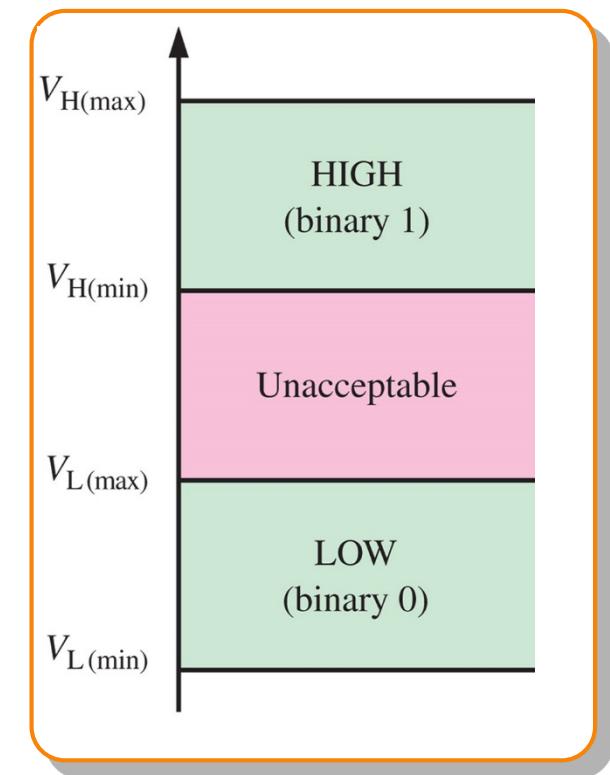
□ Binary digits

- ◆ Binary digit: a single number is either 0 or 1
- ◆ 1 is represented by the **higher voltage level → HIGH**,
- ◆ 0 is represented by the **lower voltage level → LOW**
- ◆ Negative logic : 1 → Low, 0 → High

Positive logic

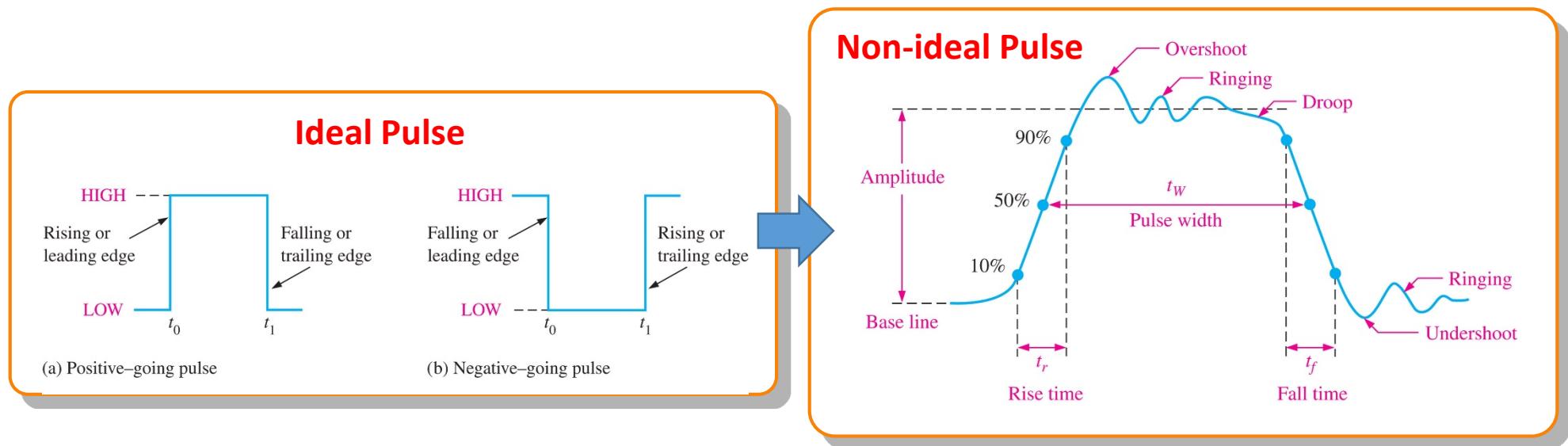
□ Logic Levels

- ◆ Def: The voltages used to represent 1 and 0
- ◆ HIGH : any voltage btw a specified minimum value and a specified maximum value;
- ◆ LOW : any voltage btw a specified minimum and a specified maximum
- ◆ $V_{H(\min)} > V_{L(\max)}$



Pulses

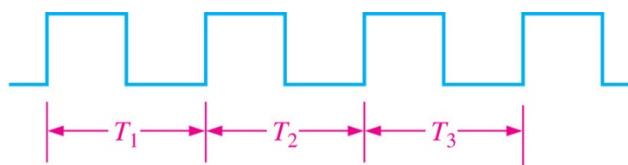
- Positive-going and negative-going pulses
- Leading/Rising edge and Falling/Trailing edge



- Non-ideal pulse:
 - ◆ Rise time : Time elapsed from 10% to 90% of the pulse amplitude
 - ◆ Fall time : Time elapsed from 90% to 10% of the pulse amplitude
 - ◆ Pulse width : Time interval btw the 50% pts on the rising and falling edges



Waveform Characteristics



Period = $T_1 = T_2 = T_3 = \dots = T_n$

Frequency = $\frac{1}{T}$

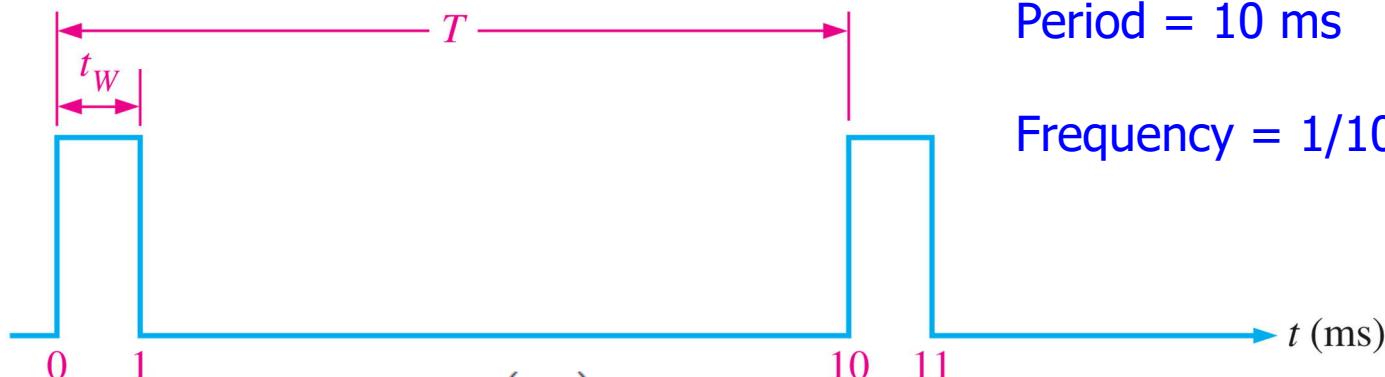
(a) Periodic (square wave)



(b) Nonperiodic

- Periodic versus Non-periodic
- Period, Frequency and Duty Cycle

$$\text{Frequency } f = \frac{1}{T} \quad \text{Period}$$

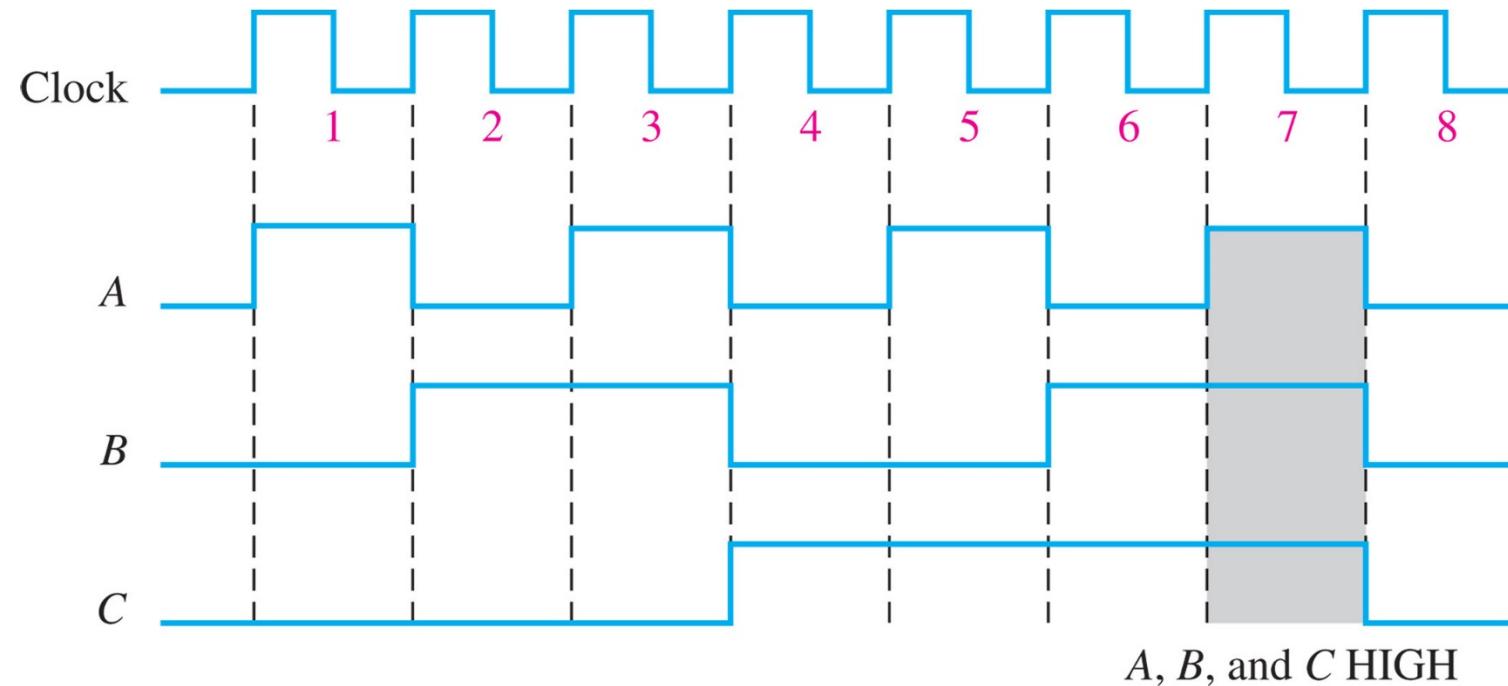


$$\text{Duty cycle} = \left(\frac{t_W}{T} \right) 100\% = (1/10) * 100\% = 10\%$$



The Clock & Timing Diagrams

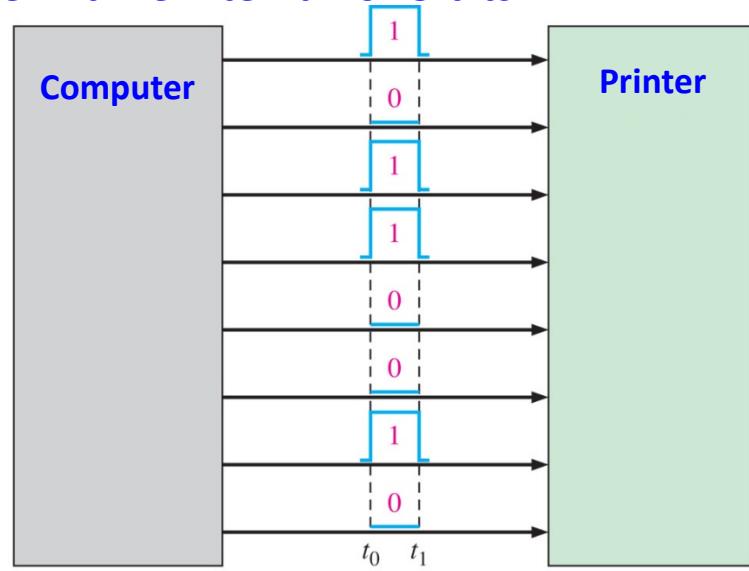
- In digital systems, all waveforms are synchronized with a basic timing **periodic** waveform called the clock.
- A timing diagram is used to show the relationship btw two or more digital waveforms



Data Transfer: Serial versus Parallel

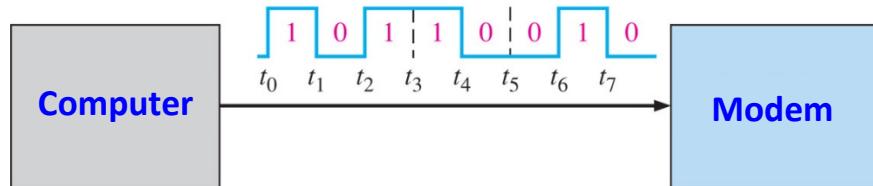
Parallel : multiple bits at the same time over separate lines

Example: 1 time interval for 8 bits



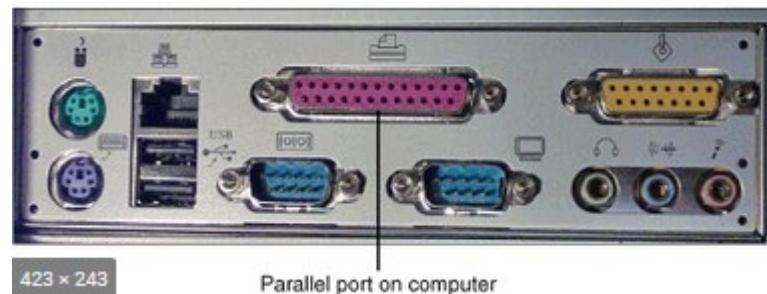
Serial: One bit at a time over a single line

Example: 8 time intervals for 8 bits



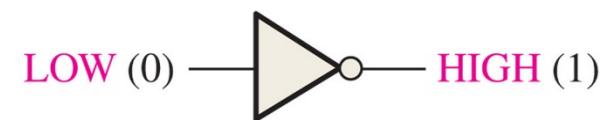
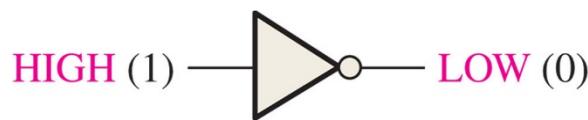
(a) Serial transfer of 8 bits of binary data. Interval t_0 to t_1 is first.

(b) Parallel transfer of 8 bits of binary data. The beginning time is t_0 .



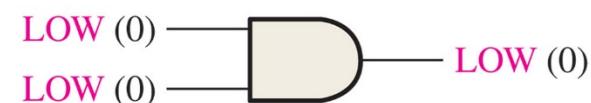
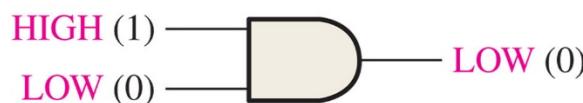
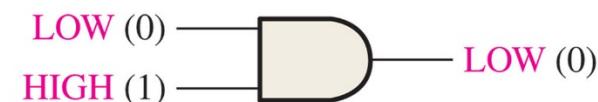
Basic Logic Functions: NOT, AND, and OR

NOT

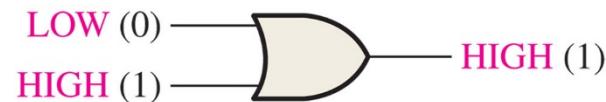
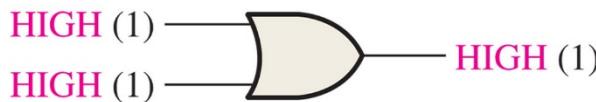


Opposite

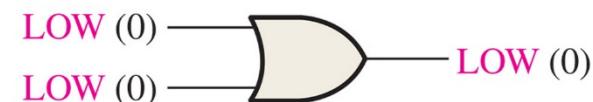
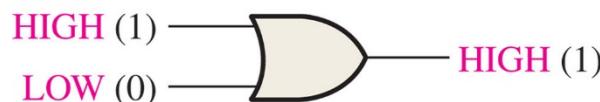
AND



OR



True if one of the inputs is true (can have more than two inputs)

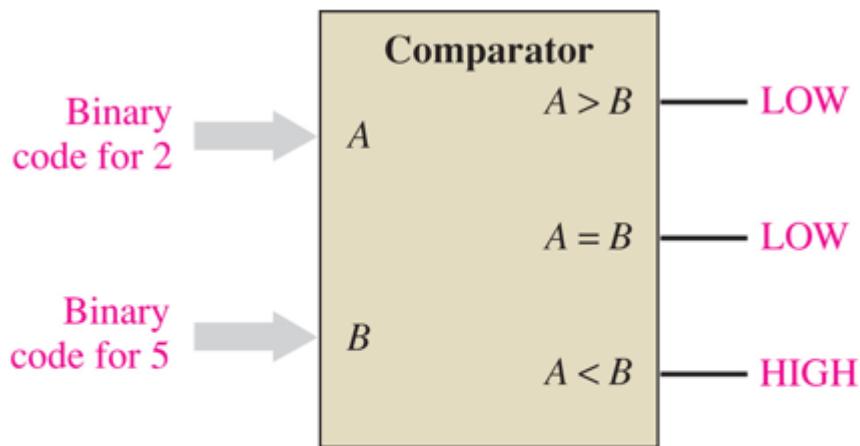


A **circuit** that performs a specified logic **function** is called a logic **gate**.



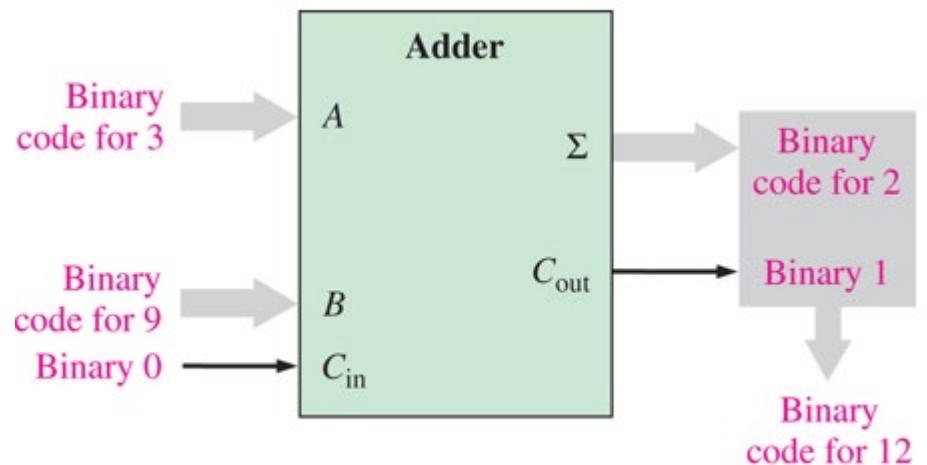
Logic Functions (I)

- AND, OR, and NOT can be combined to form various other types of more complex logic functions.



(b) Example: A is less than B ($2 < 5$) as indicated by the HIGH output ($A < B$)

Comparator



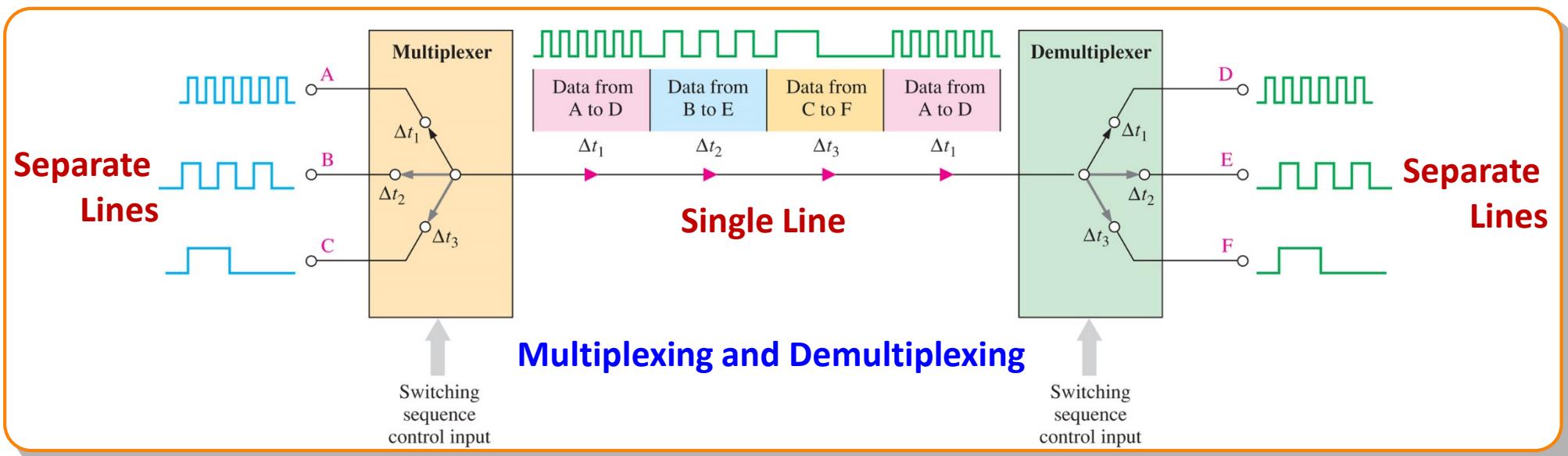
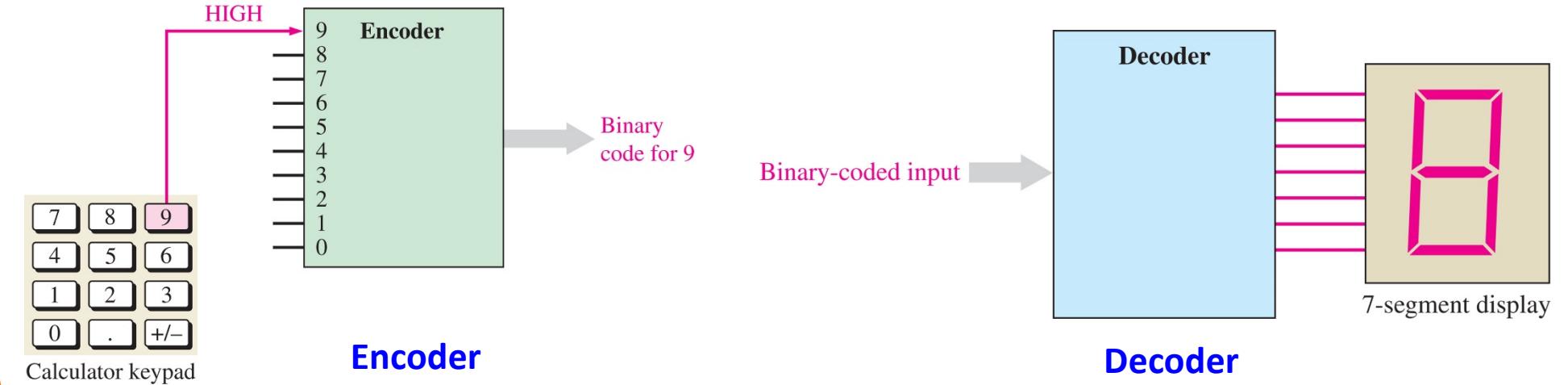
(b) Example: A plus B ($3 + 9 = 12$)

Adder

Subtraction/Multiplication/Division can be performed by an adder in conjunction with other circuits.



Logic Functions (II)



Logic Functions (IV): Storage

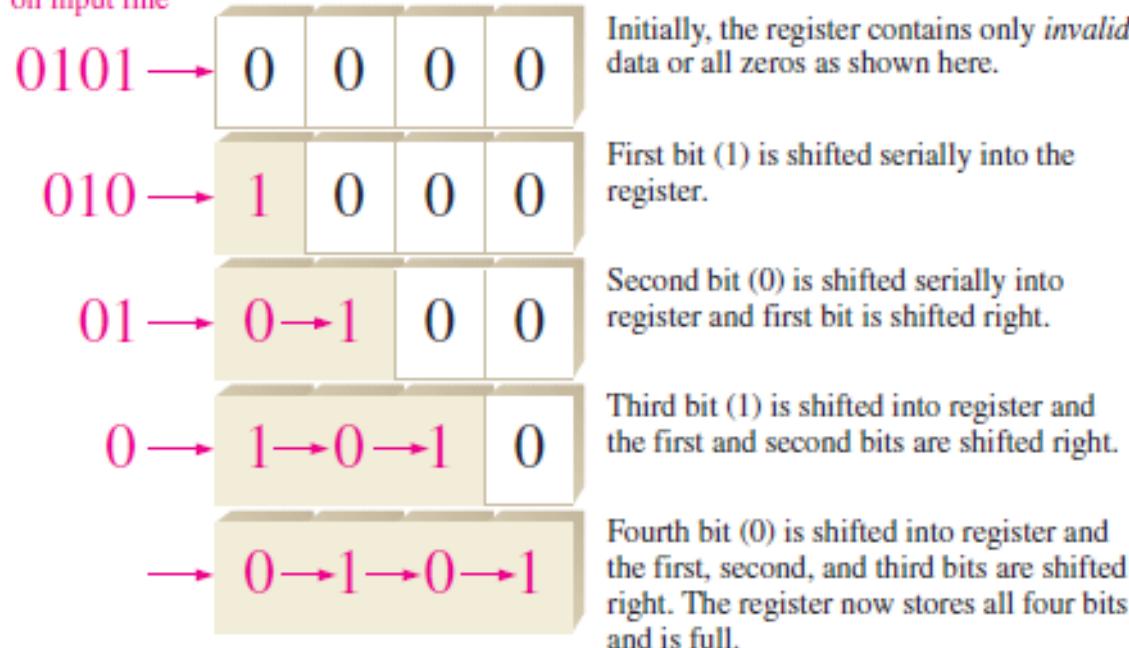


人字拖 (Flip-Flops)

- Storage: to retain binary data for a period of time.
- Flip-flops: a bistable (two stable states) logic circuit that can store only one bit at a time, either a 1 or a 0.

- Registers : several flip-flops

Serial bits
on input line



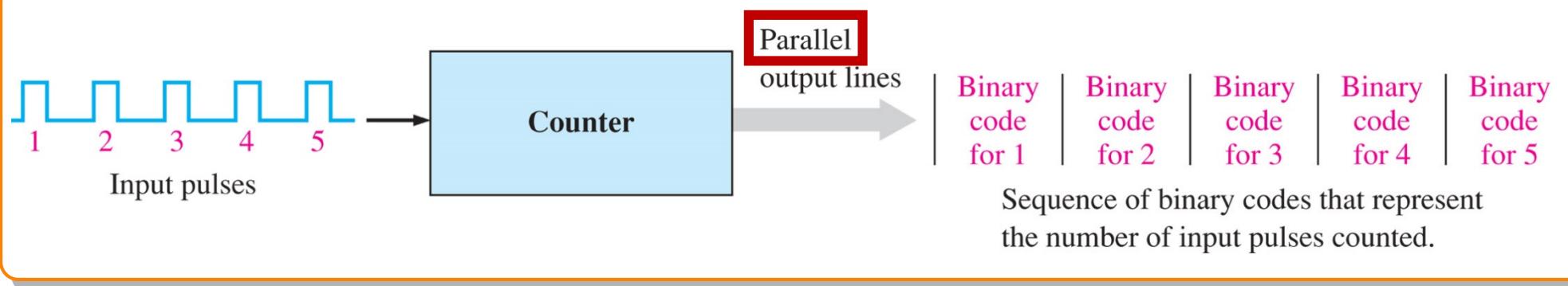
Jul 22, 2005 - A group of Northwestern University women's lacrosse players who wore flip-flops to the *White House* have fanned a flap over fashion sense ...



香港中文大學 (深圳)

The Chinese University of Hong Kong, Shenzhen

Logic Functions (V): Counting

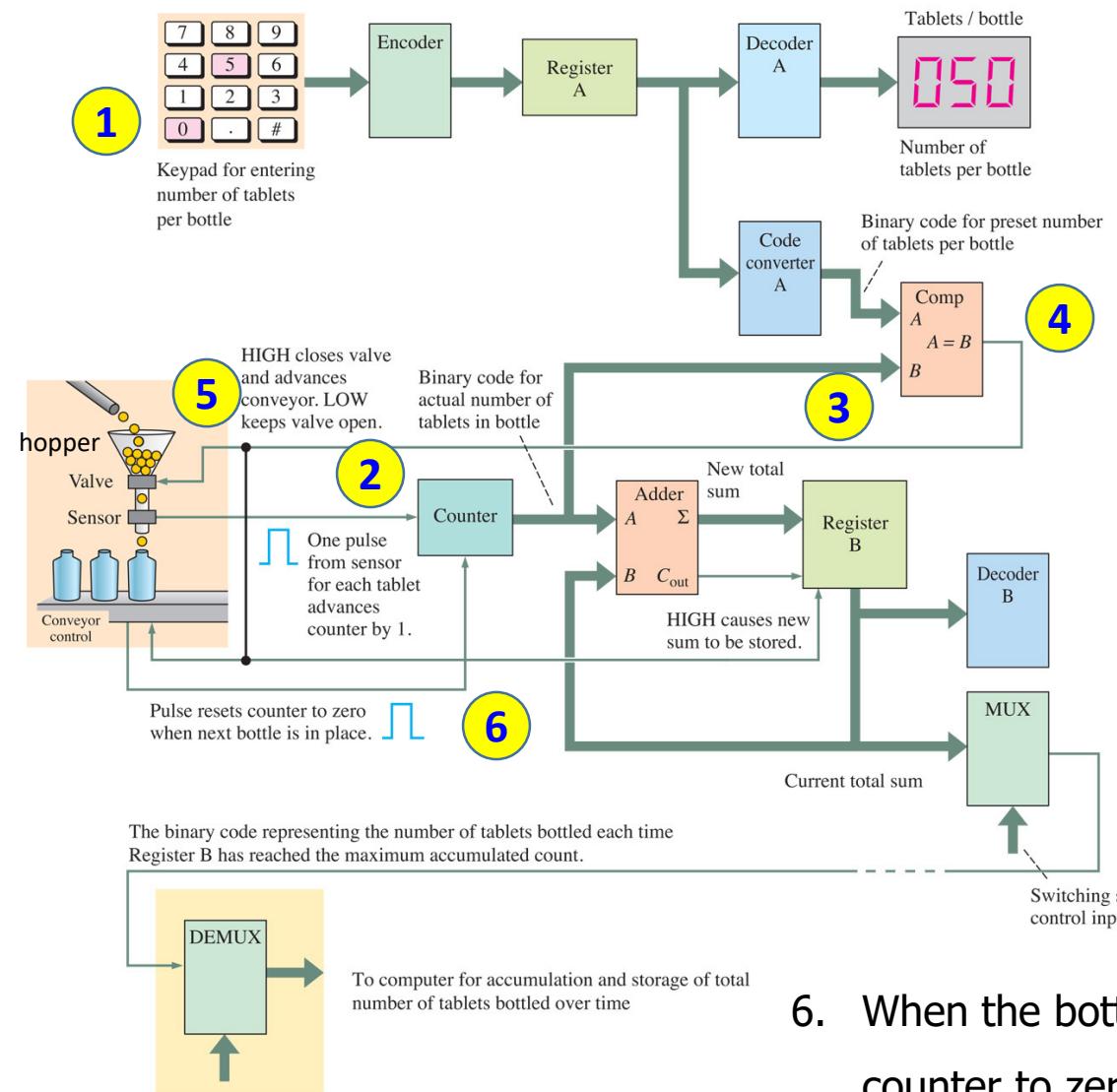


- To count, the counter must “**remember**” the present number so that it can go to the next proper number **in sequence**.
- **Storage** capability is an important characteristic of all counters, and **flip-flops** are generally used to implement them.

Will re-visit in Chapter 9



Example: A Process Control System

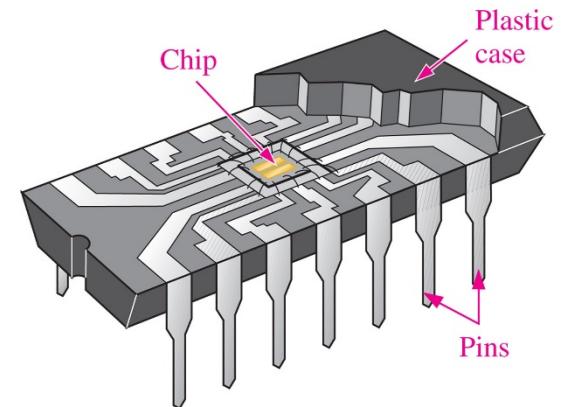


1. The maximum # of tablets per bottle is entered from the keypad;
2. An optical sensor detects each passing tablet & produces a pulse going to the **Counter** → Counter advanced by one;
3. The binary count is transferred from the counter to the B input of the **comparator**;
4. If $A=B$, **comparator** output goes HIGH, implying the bottle is full;
5. The HIGH comparator output closes the hopper valve & stop the flow of tablets while activating the conveyor to move the next empty bottle into place
6. When the bottle is in place, a pulse is issued to reset the counter to zero → the comparator output goes back LOW & the hopper valve restarts the flow of tablets.

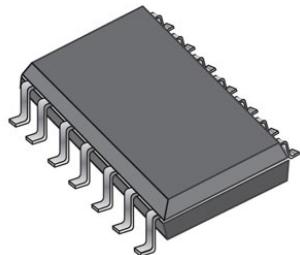


Integrated Circuits (IC)

- An electronic circuit entirely constructed on a single small chip of silicon
- Programmable and Fixed-function Logic
- IC packages : Surface-mounted and Through-hole



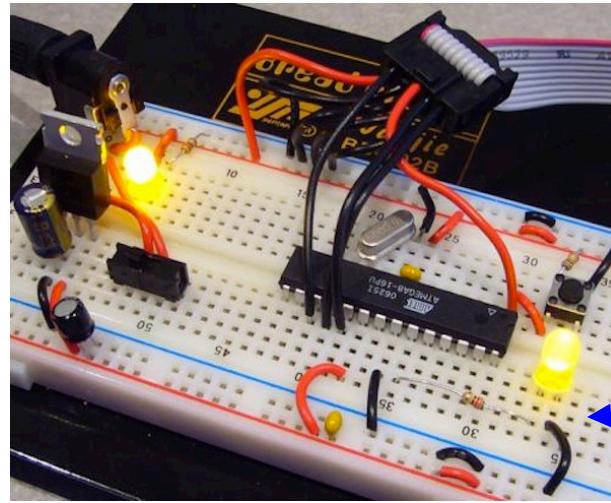
Dual in-line package (DIP)



Surface-mounted



Through-hole



面包板

or

免焊万用电路板

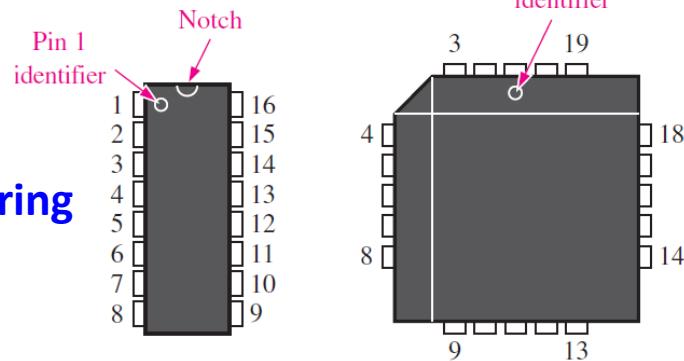
Solderless
breadboard



Complexity of Fixed-Function ICs

	# of gate circuits on a single chip	Typical Examples
Small-scale integration (SSI)	<10	Basic gates and flip-flop
Medium-scale integration (MSI)	10 to 100	Encoders, Decoders, Counters, Registers, Multiplexers, Arithmetic circuits, Small memories
Very large-scale integration (VLSI)	10,000 to 100,000	Memories
Ultra large-scale integration (ULSI)	>100,000	Very large memories, Larger micro-processors, Larger single-chip computers

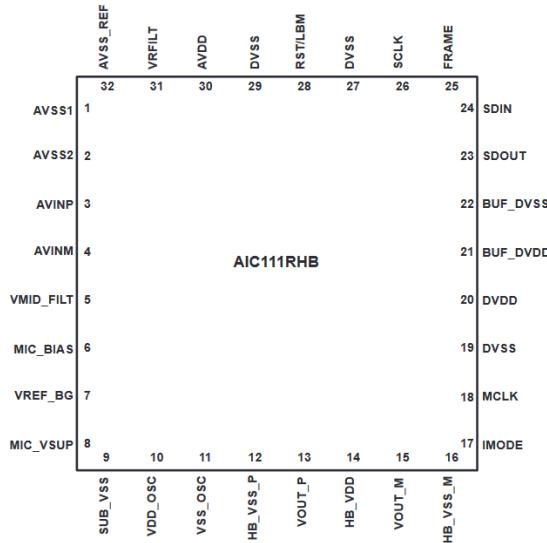
**Pin
Numbering**



- The dot is always next to pin 1.
- With the notch oriented upward, the pin numbers increase counterclockwise
- The highest pin number is always to the right of the notch or opposite the dot.



IC Specification/Data Sheet



Terminal Functions

TERMINAL NO.	Name	Type	Description
1	AVSS1	GND	Ground return for ADC analog circuits
2	AVSS2	GND	Ground return for PGAC and MIC power analog circuits
3	AVINP	AI	Noninverting differential analog input coupled through an external 1- μ F capacitor to external microphone output
4	AVINM	AI	Inverting differential analog signal input coupled through an external 1- μ F capacitor to ground
5	VMID_FILT	AO	Midsupply ac ground reference filter pin bypassed by a 1- μ F capacitor connected to ground
6	MIC_BIAS	AO	Source connection of external microphone source follower preamp. (Provides 29.1 k Ω to AVSS2)
7	VREF	AO	Bandgap reference output bypassed by external 1- μ F VREF filter capacitor
8	MIC_VSUP	AO	Supply voltage for external microphone source follower preamp bypassed with an external 0.1- μ F capacitor
9	SUB_VSS	GND	Isolated substrate VSS for analog circuits
10	VDD_OSC	VDD	Power pin for internal oscillator
11	VSS_OSC	GND	Ground return for internal oscillator
12	HB_VSS_P	GND	Ground return for noninverting stack of H-bridge amplifier
13	VOUT_P	AO	Noninverting H-bridge output voltage
14	HB_VDD	VDD	Power pin for H-bridge amplifier
15	VOUT_M	AO	Inverting H-bridge output voltage

AIC111 : Voice Band Audio Codec

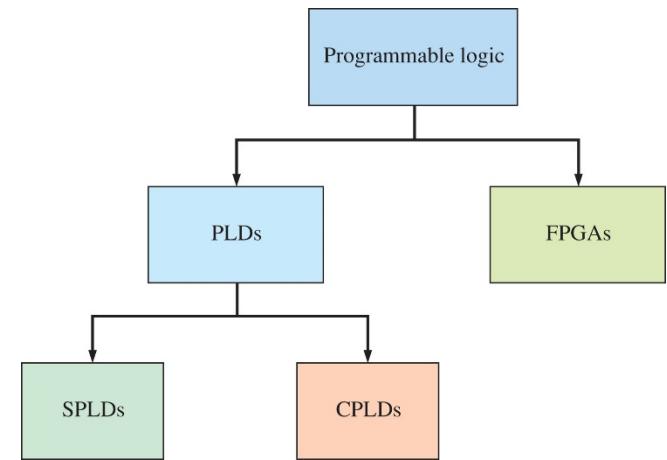


Programmable Logic

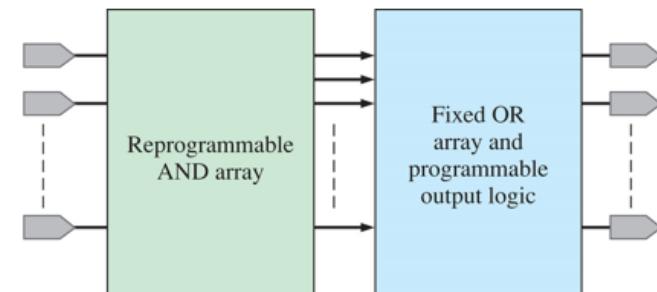
❑ Programmable Logic Devices (PLDs)

- ◆ SPLDs (simple PLDs)
- ◆ CPLDs (complex PLDs)

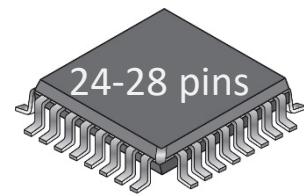
❑ Field-Programmable Gate Array (FPGA)



SPLD

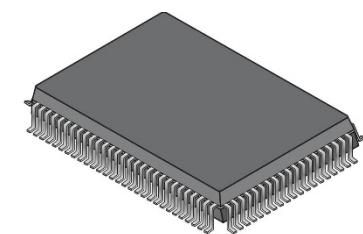
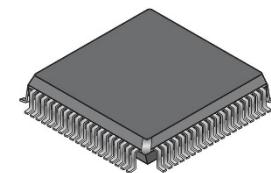
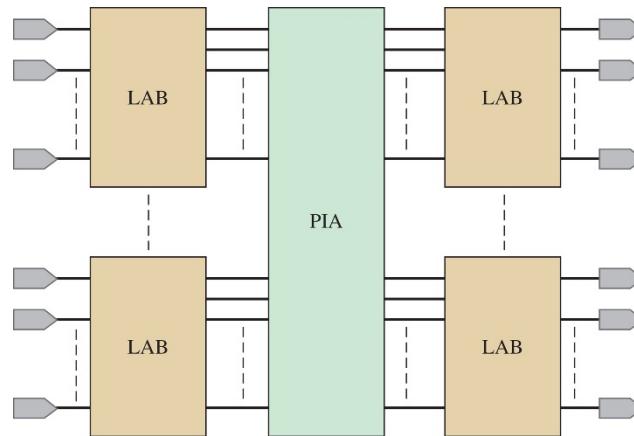


(b) GAL



A typical SPLD package

CPLD



LAB: Logic array block
PIA: Programmable
Interconnection array

Typical CPLD plastic quad flat packages (PQFP)



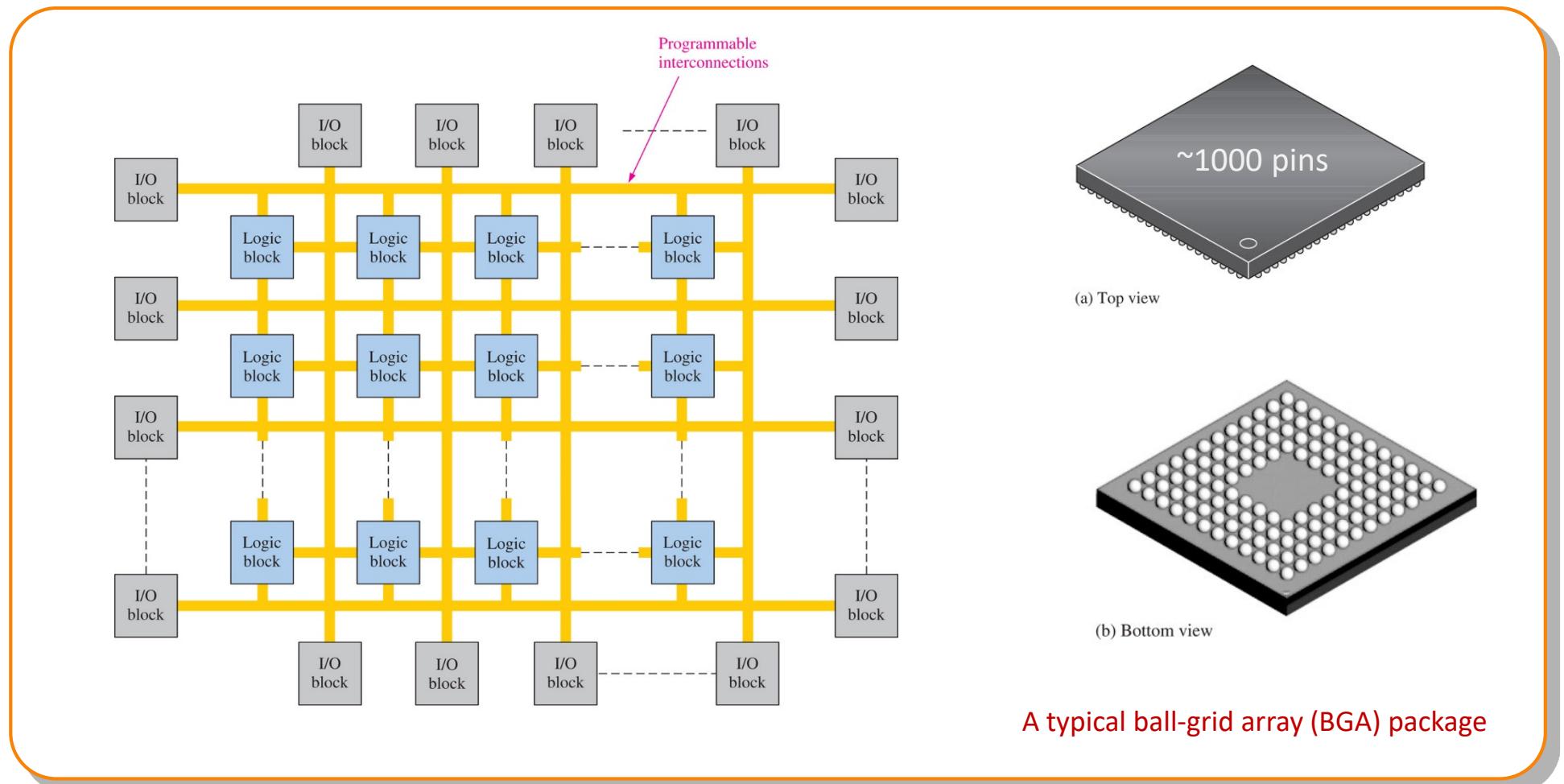
香港中文大學(深圳)

The Chinese University of Hong Kong, Shenzhen

Spring 2023 EIE2050 Digital Logic and Systems

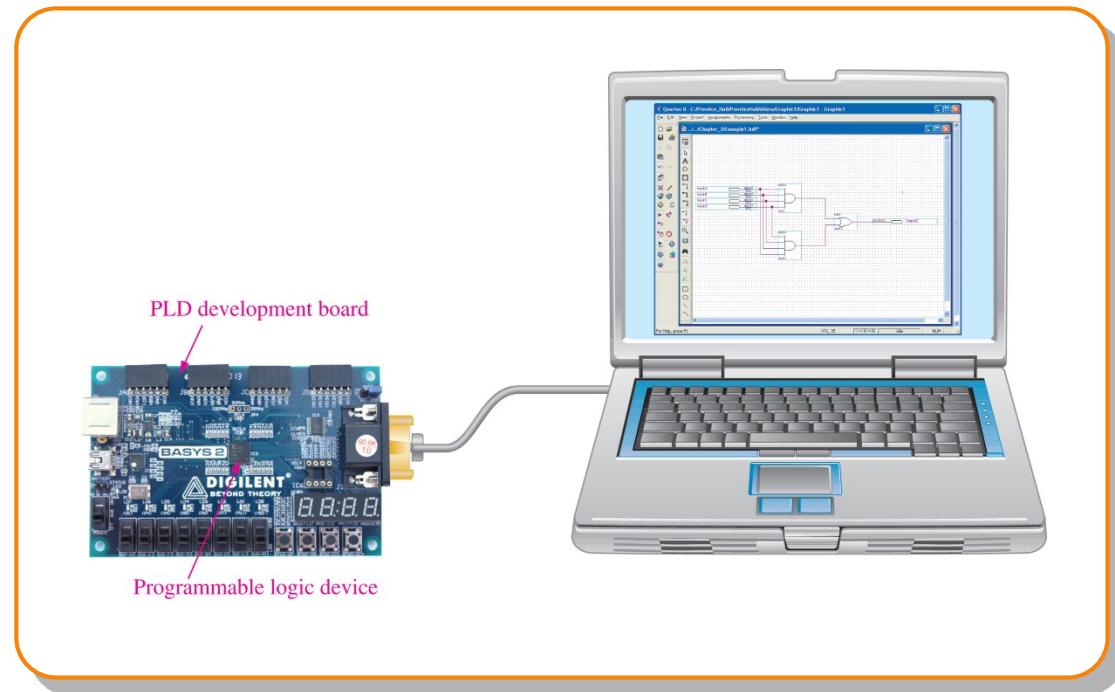
Field-Programmable Gate Array (FPGA)

- Three basic elements in an FPGA : logic block, the programmable interconnections, and the input/output (I/O)

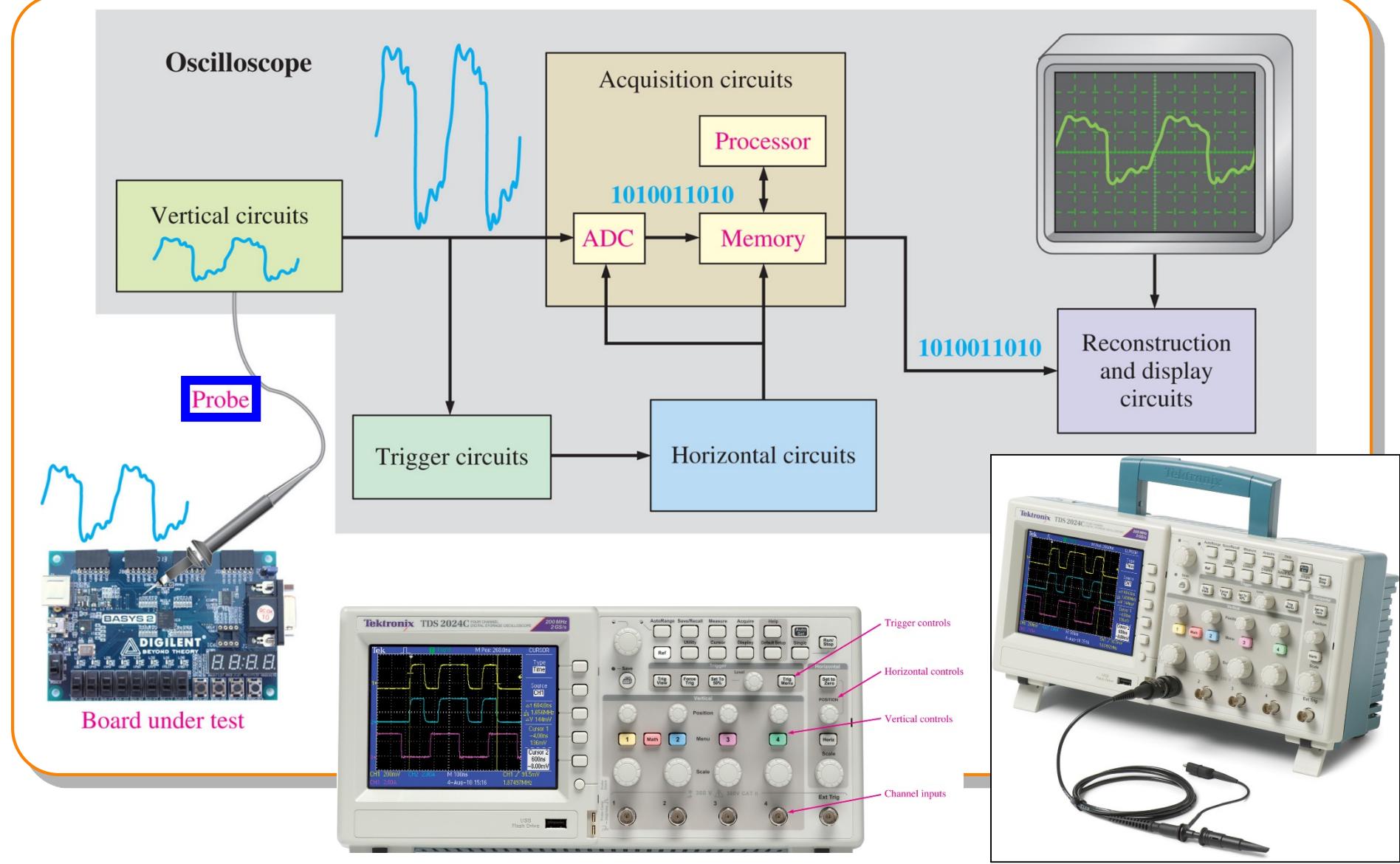


Programming Process

- ❑ Software development package installed on a computer
 - ◆ Graphic entry of a logic circuit
 - ◆ Text entry such as VHDL
- ❑ A development board
- ❑ A cable



Test and Measurement Instruments (I)

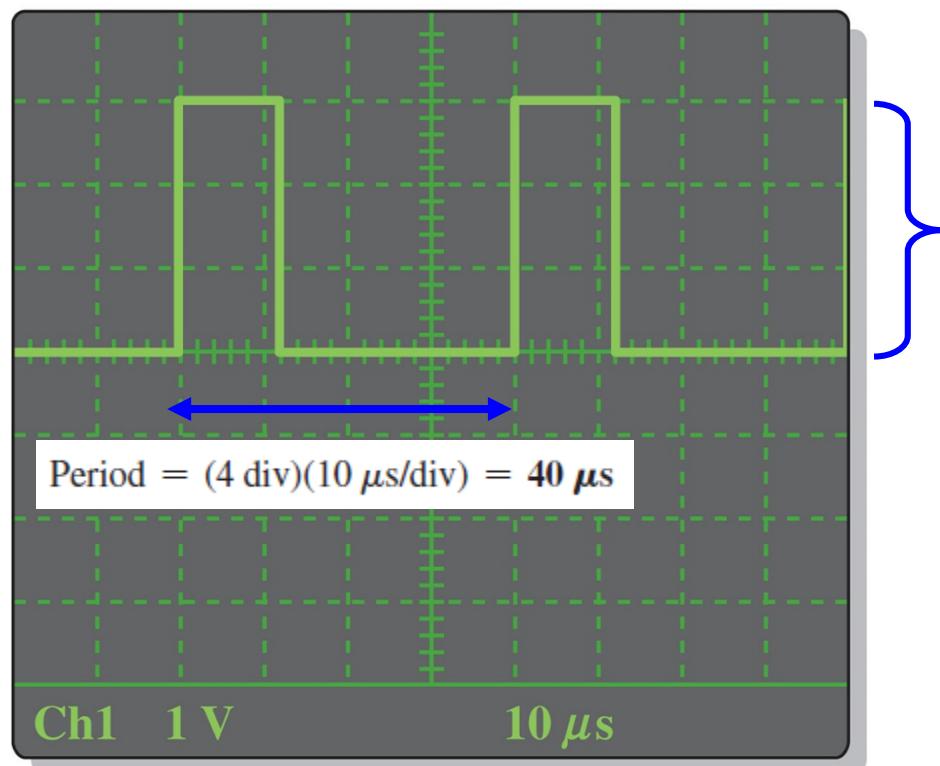


Oscilloscope Demo



Example 1–3

- Based on the readouts, determine the amplitude and the period of the pulse waveform on the screen of a digital oscilloscope as shown. Also, calculate the frequency.



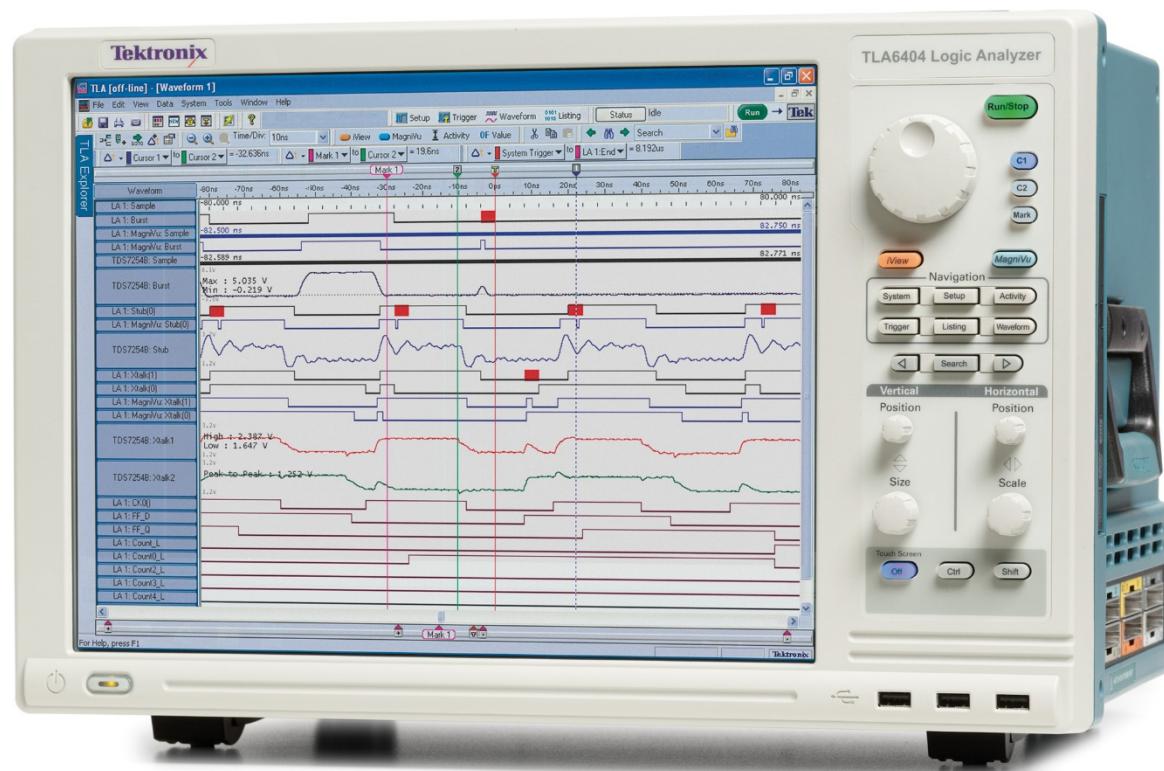
$$f = \frac{1}{T} = \frac{1}{40 \mu\text{s}} = 25 \text{ kHz}$$

μs : microsecond 10^{-6}
 ms : millisecond 10^{-3}

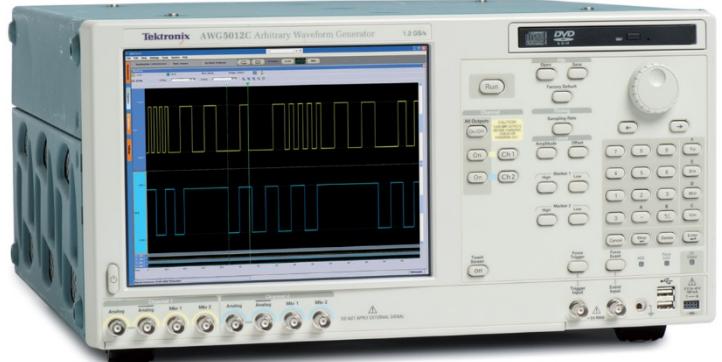


Test and Measurement Instruments (II)

	Oscilloscope	Logic Analyzer
Built-in Microprocessors	No	Yes
Input Channels	2-4	16-136
Measurement	Amplitude, Frequency and Timing	Amplitude, Frequency and Timing + correlation



Other Commonly Used Instruments



Waveform Generator



Function Generator



(a) Bench-type DMM



(b) Handheld DMM

DMM: Digital Multimeter



DC Power Supply



Typical Price for Different Instruments

Instrument	Model	Specification	Tag Price (RMB)
Logic analyzer	KEYSIGHT	MSOX4154A (16 Channels)	200,000
Oscilloscope	广州市中普电子有限公司	DS4012(4 Channels)	18,000
Signal generator	广州市中普电子有限公司	DG1022U	1,800
Waveform generator	优利德	UTG4162A (up to 160MHz Sampling freq.)	12,100
Digital multimeter	广州市中普电子有限公司	DM3068	5,500
DC power supply	广州市中普电子有限公司	DP821A	5,200



Chapter Review

- Analog versus Digital
- Bits (Binary digits), Logic Levels and Digital Waveforms
- Basic logic functions: NOT, AND and OR
- Combinational & sequential logic functions: comparator, adder, encoder/decoder, (de)multiplexer, flip-flops, registers, counter
- Integrated circuit (IC): Programmable versus Fixed-function
 - ◆ Package: Surface-mounted and Through-hole
 - ◆ Programmable: PLD (SPLD and CPLD) and FPGA
 - ◆ Fixed-function : SSI/MSI/VLSI/ULSI
- Instruments: Oscilloscope, logic analyzer, signal/waveform gen., digital multimeter, DC power supply.



True/False Quiz

- An analog quantity is one having continuous values.
- A digital quantity has no discrete values.
- There are two digits in the binary system.
- The term bit is short for binary digit.
- In positive logic, a LOW level represents a binary 1.
- A periodic wave repeats itself at a fixed interval.
- A timing diagram shows the timing relationship of two or more digital waveforms.
- An AND function is implemented by a logic circuit known as an inverter.
- A flip-flop is a bistable logic circuit that can store only two bits at a time.
- Two broad types of digital integrated circuits are fixed- function and programmable.



Answers

-  An analog quantity is one having continuous values.
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-  There are two digits in the binary system.
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-  In positive logic, a LOW level represents a binary 1.
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