



EIE 2050 Digital Logic and Systems

Chapter 5 : Combinational Logic Analysis

Simon Pun, Ph.D.



Last Week

- Boolean Operations and Expressions :
 - ◆ Addition → OR; Multiplication → AND
- Laws and Rules of Boolean Algebra :
 - ◆ Commutative, Associative and Distributive
 - ◆ 12 Rules
- DeMorgan's Theorems
- Standard Forms of Boolean Expressions
 - ◆ SOP and POS
- Boolean Expressions and Truth Tables
- The Karnaugh Map
 - ◆ Karnaugh Map SOP Minimization
 - ◆ Karnaugh Map POS Minimization
- The Quine-McCluskey Method

Basic rules of Boolean algebra.

- | | |
|----------------------|-------------------------------|
| 1. $A + 0 = A$ | 7. $A \cdot A = A$ |
| 2. $A + 1 = 1$ | 8. $A \cdot \bar{A} = 0$ |
| 3. $A \cdot 0 = 0$ | 9. $\bar{\bar{A}} = A$ |
| 4. $A \cdot 1 = A$ | 10. $A + AB = A$ |
| 5. $A + A = A$ | 11. $A + \bar{A}B = A + B$ |
| 6. $A + \bar{A} = 1$ | 12. $(A + B)(A + C) = A + BC$ |

DeMorgan's Theorems

$$\overline{XY} = \bar{X} + \bar{Y}$$

$$\overline{X + Y} = \bar{X}\bar{Y}$$



Basic Combinational Logic Circuits : AND-OR Logic

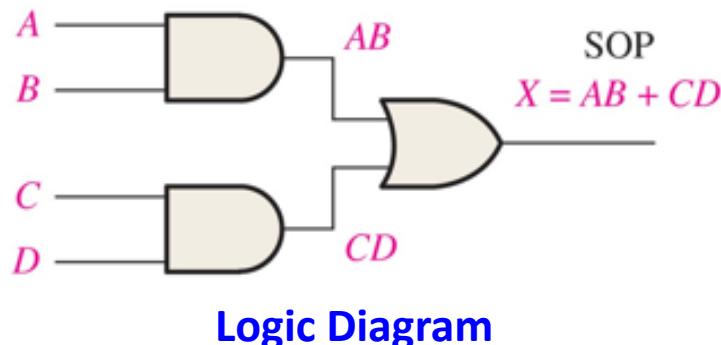


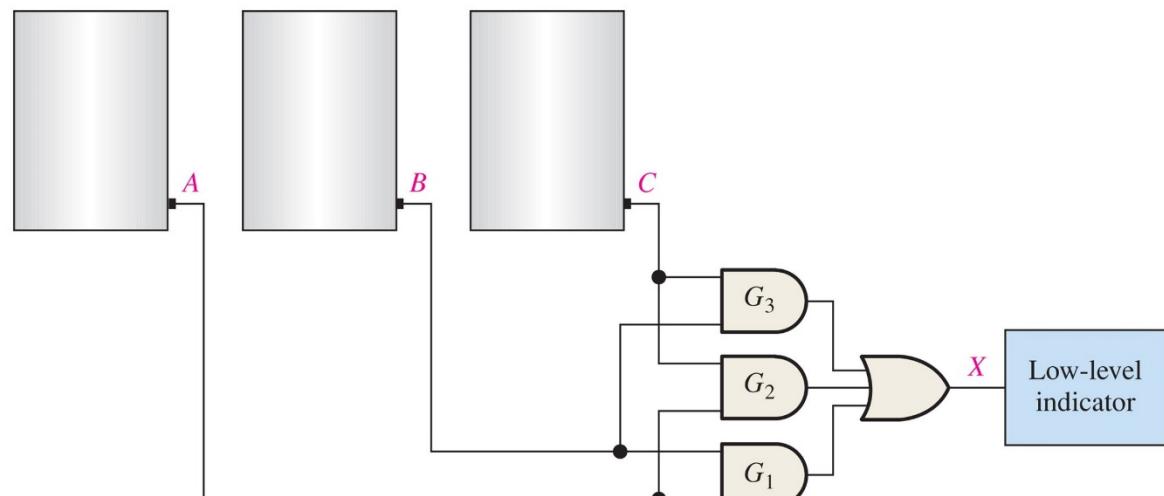
TABLE 5-1

Truth table for the AND-OR logic in Figure 5-1.

Inputs				AB	CD	Output X
A	B	C	D			
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	1	1
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	0	0
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	0	1	1
1	1	0	0	1	0	1
1	1	0	1	1	0	1
1	1	1	0	1	0	1
1	1	1	1	1	1	1

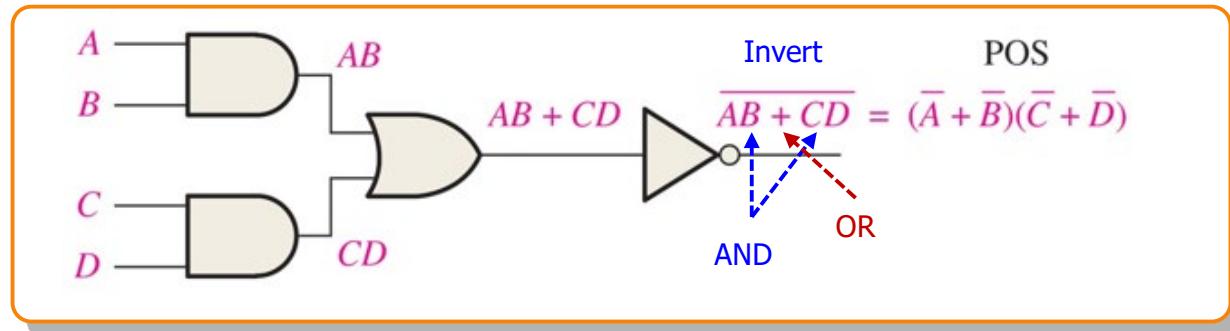
Example 5-1

A level sensor in each tank produces a HIGH voltage when the level of chemical in the tank drops below a specified point. Design a circuit that monitors the chemical level in each tank and indicates when the level in **any two of the tanks** drops below the specified point.



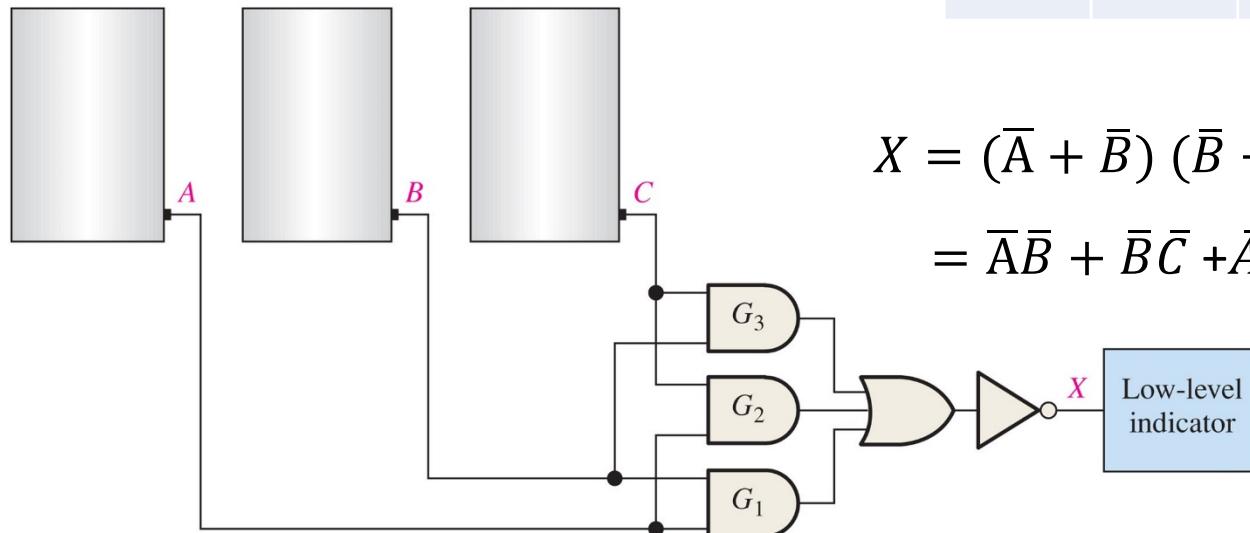
AND-OR-Invert Logic

$$X = (A + \bar{B} + \bar{C})(\bar{A} + \bar{B} + C)(\bar{A} + B + \bar{C})(\bar{A} + \bar{B} + \bar{C})$$

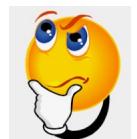


A level sensor in each tank produces a **LOW** voltage when the level of chemical in the tank drops below a specified point. Design a circuit that monitors the chemical level in each tank and indicates when the level in any two of the tanks drops below the specified point.

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



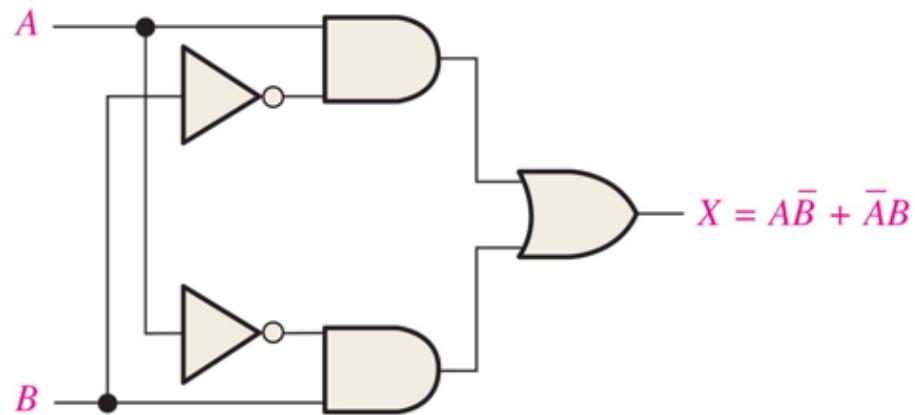
$$X = (\bar{A} + \bar{B})(\bar{B} + \bar{C})(\bar{A} + \bar{C}) \\ = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$$



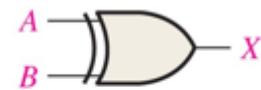
Why?



Exclusive-OR Logic



(a) Logic diagram



(b) ANSI distinctive
shape symbol

TABLE 5-2

Truth table for an exclusive-OR.

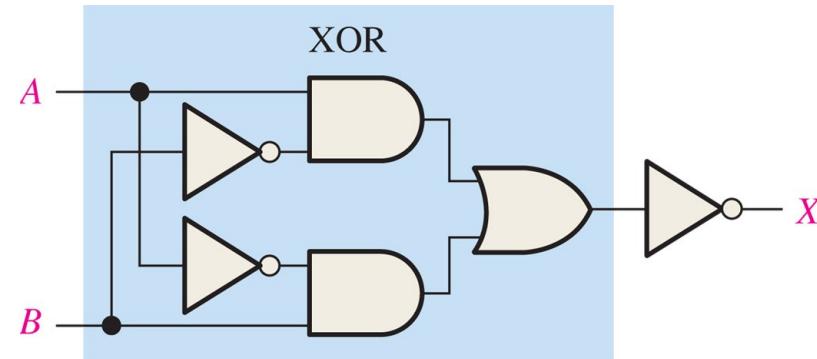
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

		B	0	1
		A	0	1
0	0	0	1	
	1	1	0	

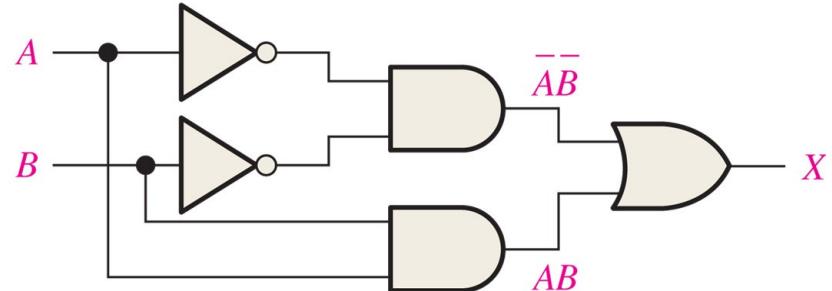
$$X = A\bar{B} + \bar{A}B = A \oplus B$$



Exclusive-NOR Logic



$$(a) X = \overline{A\bar{B}} + \overline{\bar{A}B}$$



$$(b) X = \overline{A\bar{B}} + AB$$

Truth Table for an Exclusive-NOR

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

		0	1
		0	1
0		1	0
1		0	1
A	B		

$$X = \overline{A\bar{B}} + \overline{\bar{A}B} = \overline{(A\bar{B})} \overline{(\bar{A}B)}$$

$$= (\bar{A} + B)(A + \bar{B}) = \overline{A\bar{B}} + AB$$



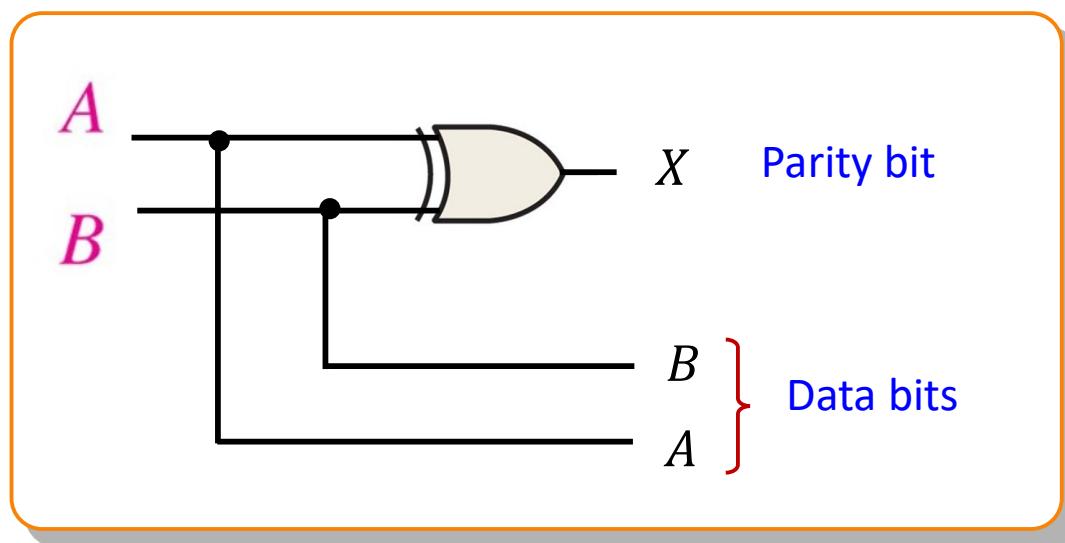
2-Bit Even-Parity Codes

Truth Table

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

B	0	1
A	0	1
1	1	0

$$X = A\bar{B} + \bar{A}B = A \oplus B$$



3-Bit Even-Parity Codes

Use exclusive-OR gates to implement an even-parity code generator for an original **3-bit** code.

		BC	00	01	11	10
		A	0	1	0	1
			0	1	0	1
A	0	0	1	0	1	0
	1	1	0	1	0	0

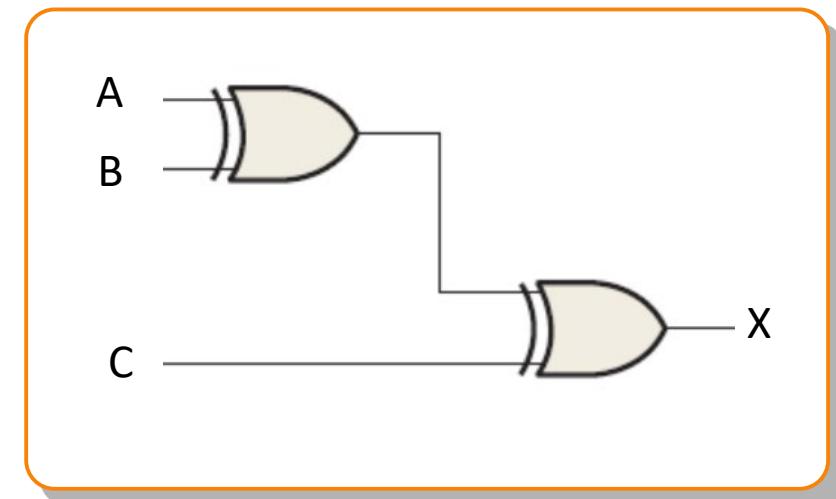
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$\begin{aligned}
 X &= \underbrace{\bar{A}\bar{B}C + \bar{A}B\bar{C}}_{=} + \underbrace{A\bar{B}\bar{C} + ABC}_{=} \\
 &= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)
 \end{aligned}$$

Recall $\bar{A}\bar{B} + AB = \overline{A \oplus B}$ XNOR

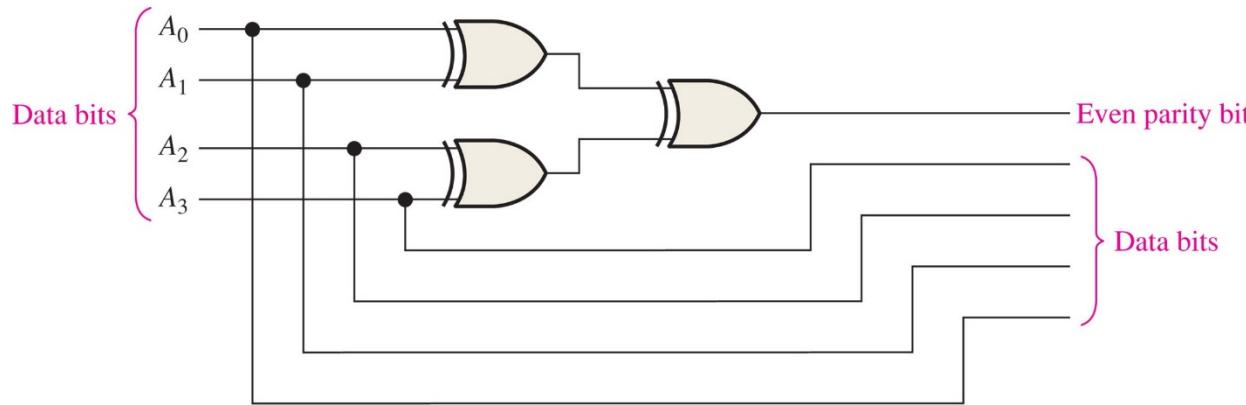
$$A\bar{B} + \bar{A}B = A \oplus B \quad \text{XOR}$$

$$\begin{aligned}
 &= \bar{A}(B \oplus C) + A(\overline{B \oplus C}) \\
 &= A \oplus B \oplus C
 \end{aligned}$$



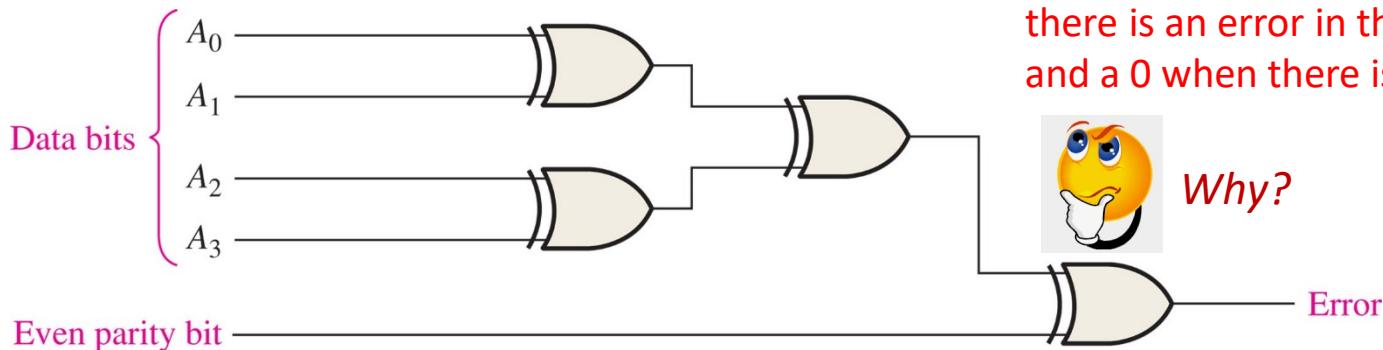
More on Even-Parity Code Generators

Use XOR gates to implement an even-parity code generator for an original 4-bit code.



Example 5-3

Use XOR gates to implement an even-parity checker for the 5-bit code generated by the circuit in Example 5–3.

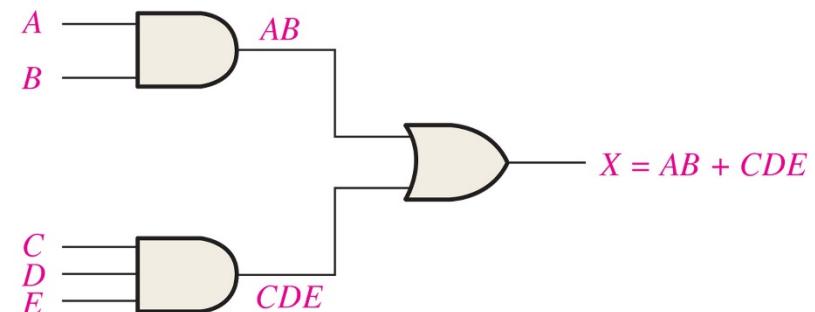
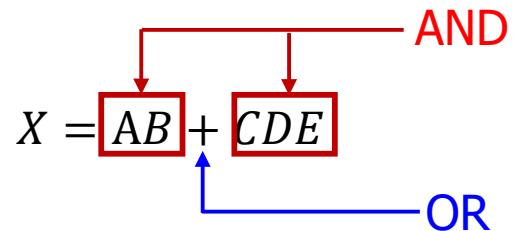


Example 5-4



Implementing Combinational Logic

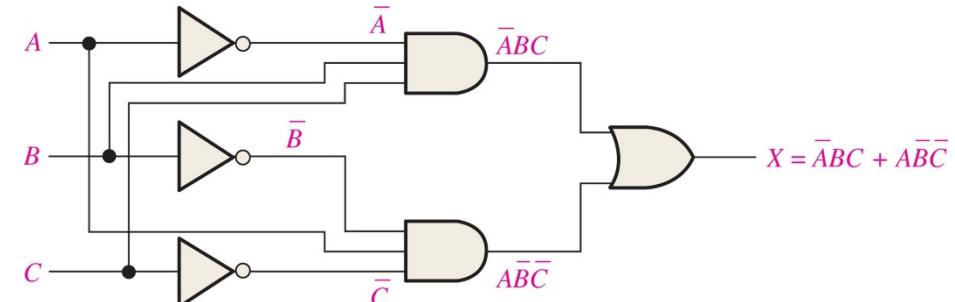
□ From a Boolean Expression to a Logic Circuit



□ From a Truth Table to a Logic Circuit

TABLE 5–3

Inputs			Output	Product Term
A	B	C	X	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\bar{A}BC$
1	0	0	1	$A\bar{B}\bar{C}$
1	0	1	0	
1	1	0	0	
1	1	1	0	



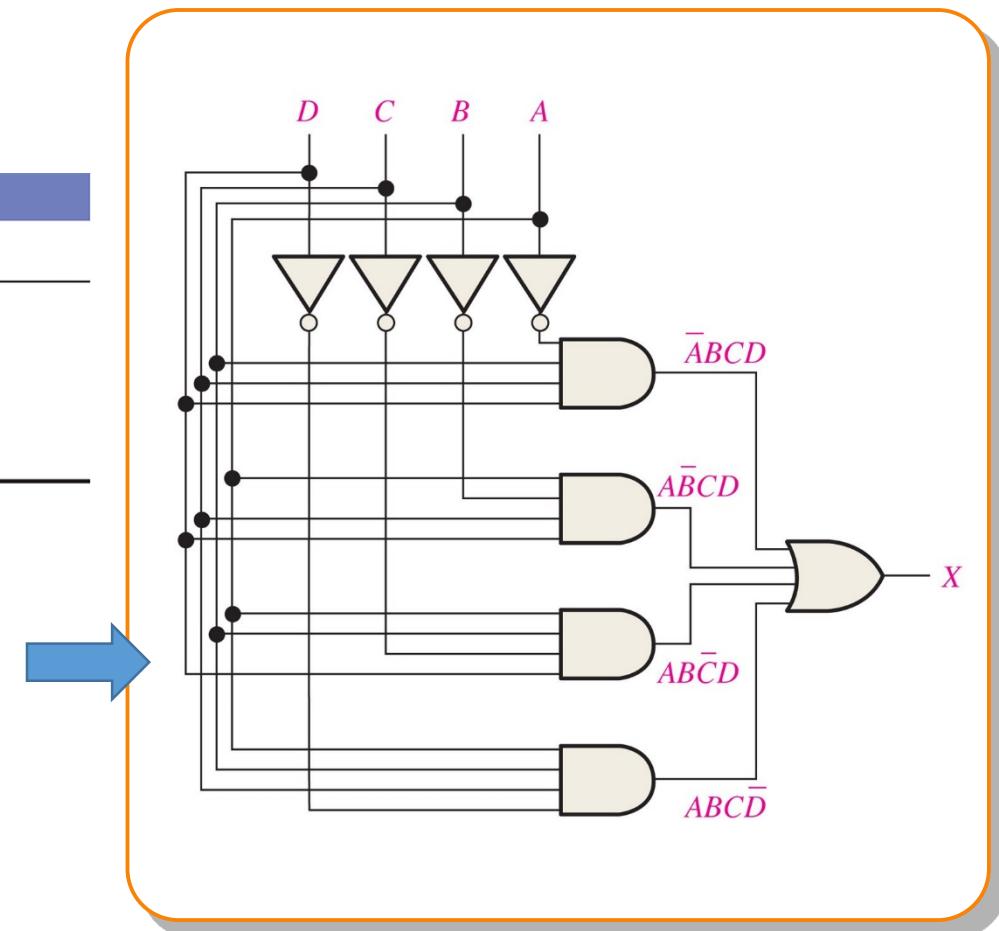
Example 5-6

Develop a logic circuit with four input variables that will only produce a 1 output when exactly three input variables are 1s.

TABLE 5-5

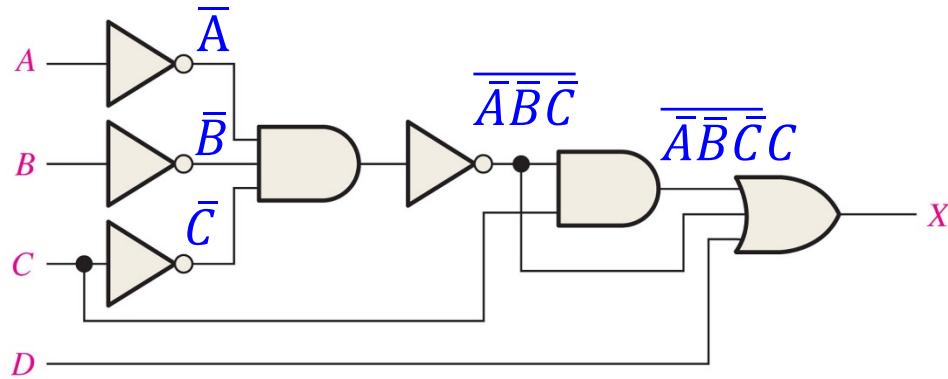
A	B	C	D	Product Term
0	1	1	1	$\bar{A}BCD$
1	0	1	1	$A\bar{B}CD$
1	1	0	1	$AB\bar{C}D$
1	1	1	0	$ABC\bar{D}$

$$X = \bar{A}BCD + A\bar{B}CD + AB\bar{C}D + ABC\bar{D}$$

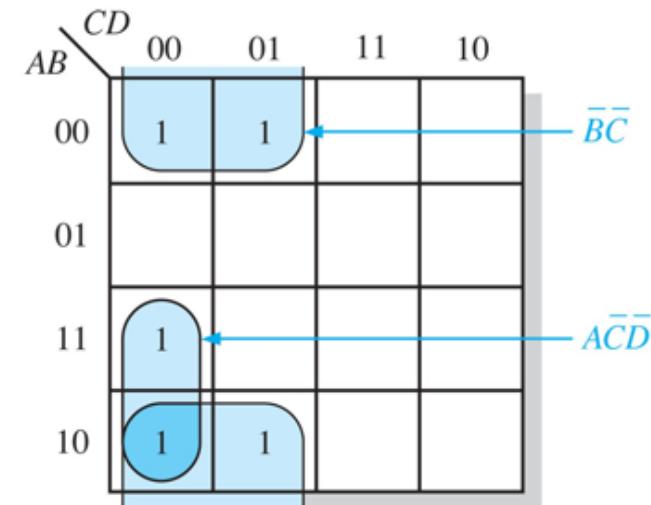
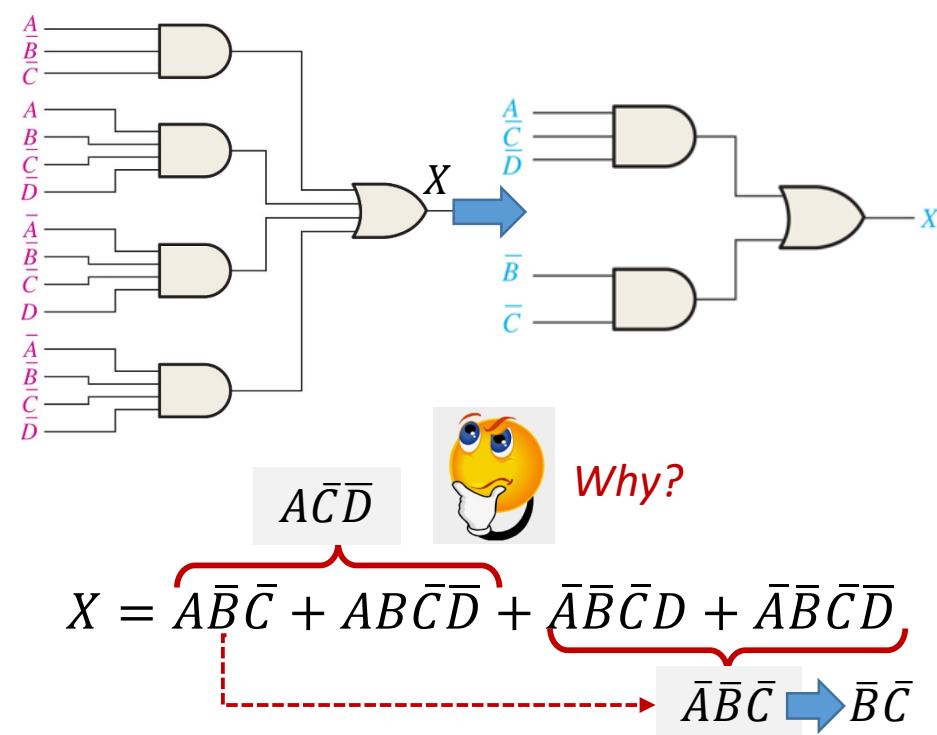
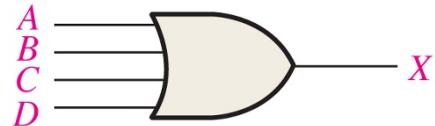


Example 5-7 & 5-8

Reduce the combinational logic circuit to a minimum form.

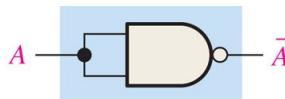


$$\begin{aligned}
 X &= \bar{A}\bar{B}\bar{C}C + \bar{A}\bar{B}\bar{C} + D \\
 &= (A + B + C)C + (A+B+C) + D \\
 &= (A+B+C) + D \\
 &= A+B+C + D
 \end{aligned}$$

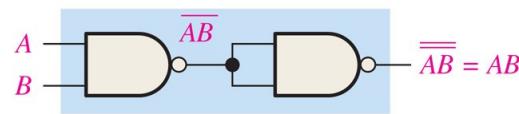
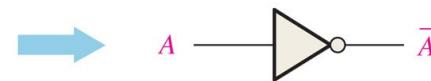


The Universal Property of NAND Gates

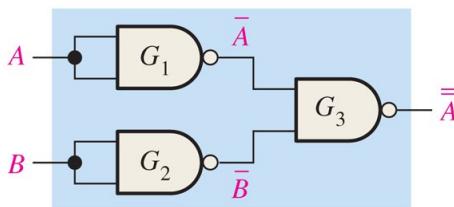
- Combinations of NAND gates can function as NOT, AND, OR, and NOR



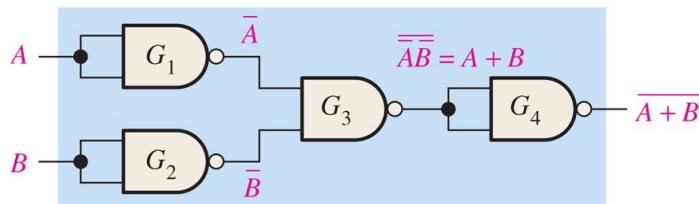
(a) One NAND gate used as an inverter



(b) Two NAND gates used as an AND gate



(c) Three NAND gates used as an OR gate

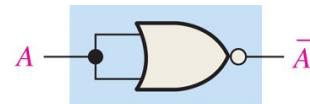


(d) Four NAND gates used as a NOR gate

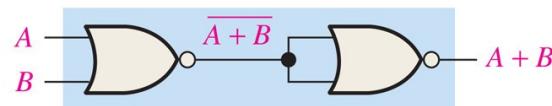


The Universal Property of NOR Gates

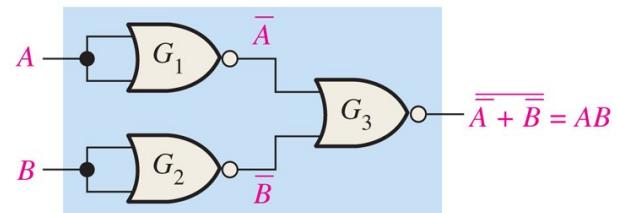
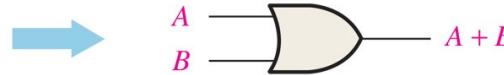
- Combinations of NOR gates can function as NOT, AND, OR, and NAND.



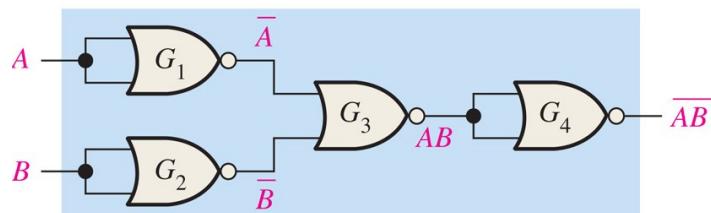
(a) One NOR gate used as an inverter



(b) Two NOR gates used as an OR gate



(c) Three NOR gates used as an AND gate



(d) Four NOR gates used as a NAND gate



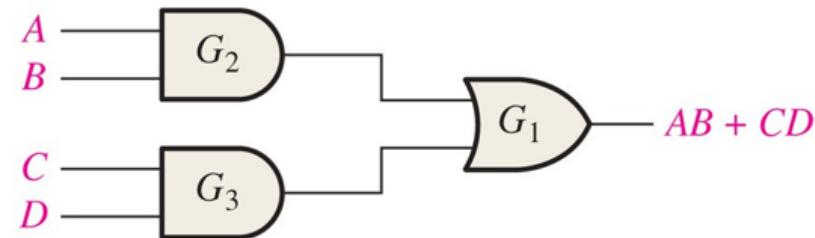
Combinational Logic Using Dual symbols

- Equivalent operations

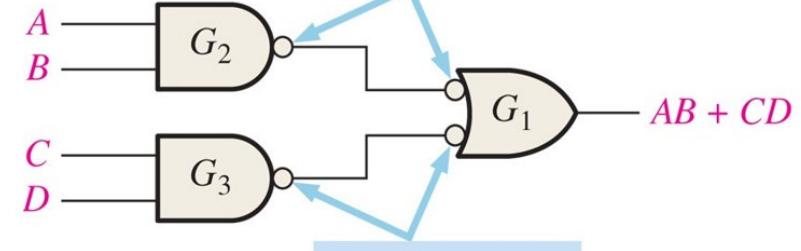
$$\overline{AB} = \bar{A} + \bar{B}$$

$$\overline{A + B} = \bar{A}\bar{B}$$

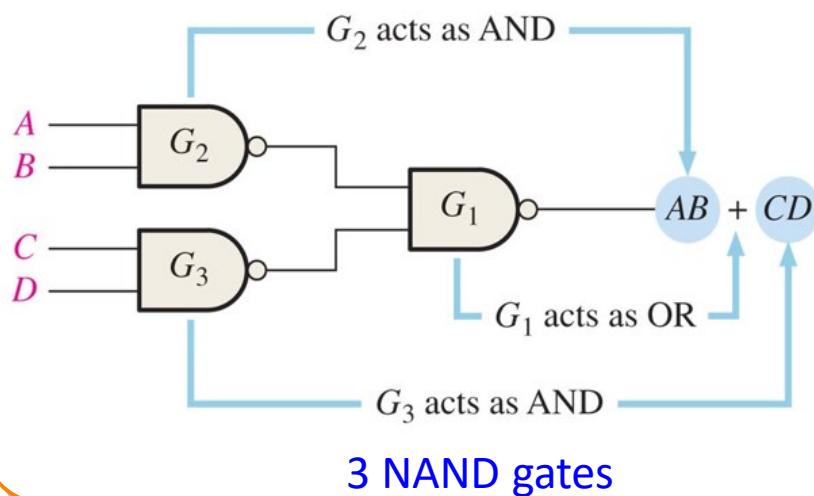
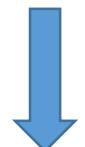
2 AND gates and 1 OR gate



Bubbles cancel



Bubbles cancel



3 NAND gates

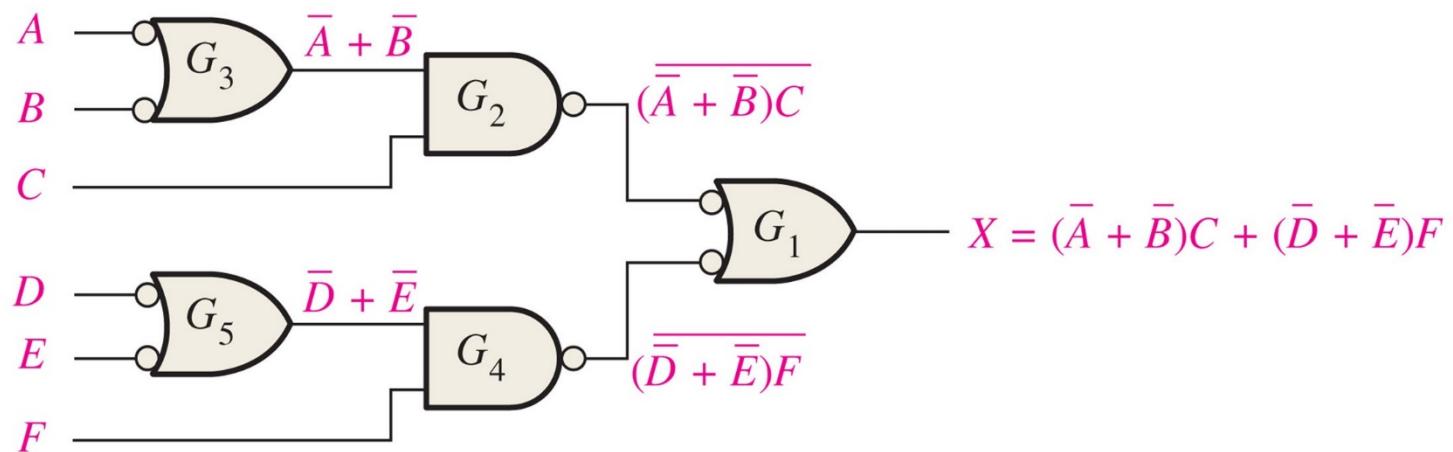
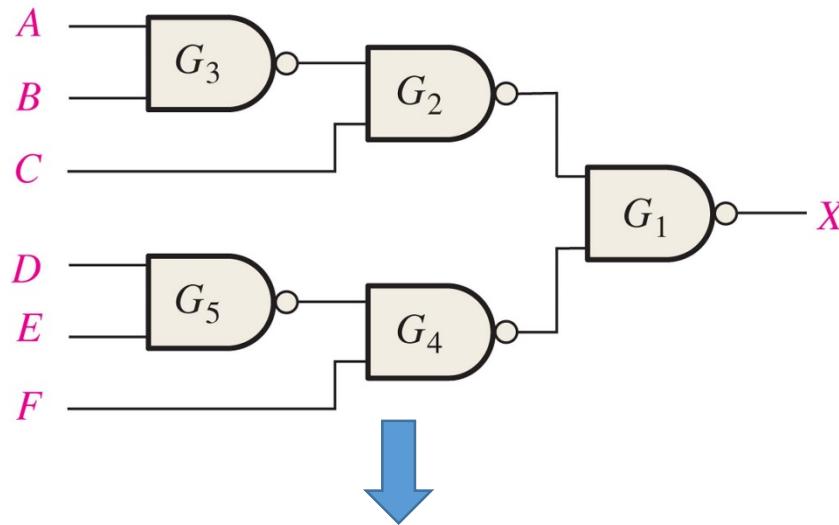
- ◆ Dual symbols : NAND and Negative-OR; NOR and Negative-AND
- ◆ Every connection btw a gate output and a gate input should be either bubble-to-bubble or nonbubble-to-nonbubble.
- ◆ In general, a bubble output should **NOT** be connected to a nonbubble input or vice versa in a logic diagram.



NAND Logic Diagrams Using Dual Symbols

Redraw the logic diagram and develop the output expression using the appropriate dual symbols.

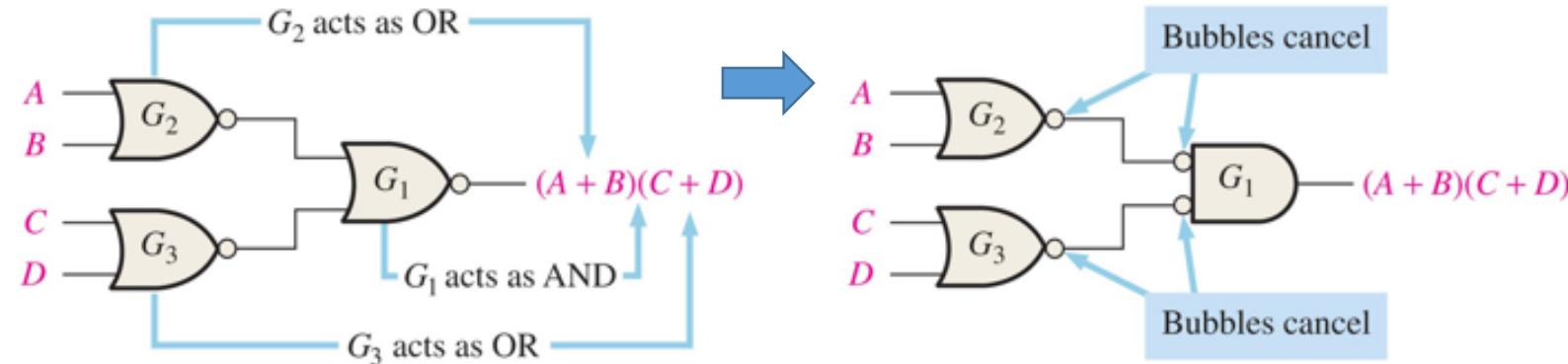
Example 5-9



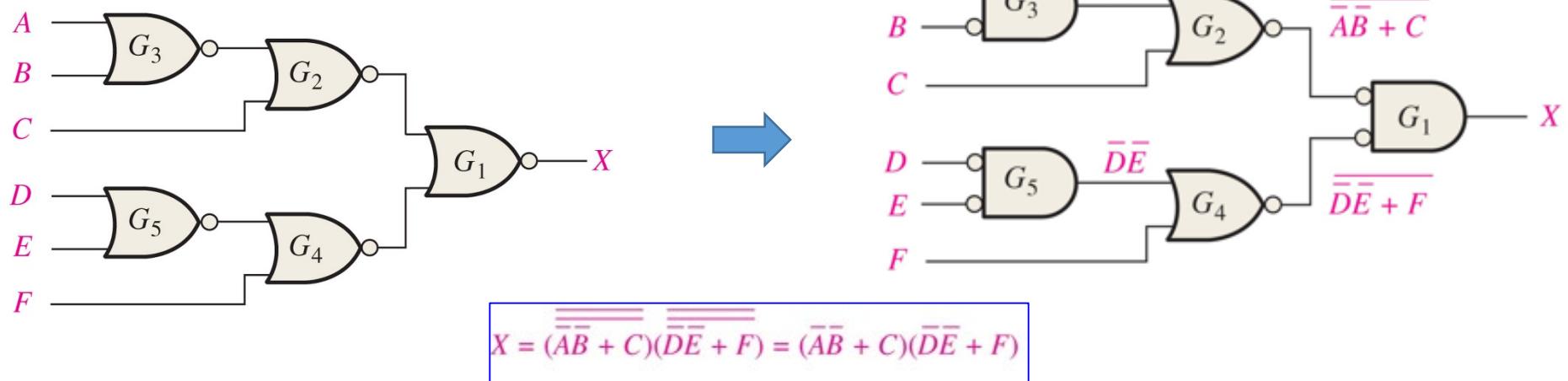
NOR Logic Diagrams Using Dual Symbols

□ Equivalent operations $\overline{AB} = \bar{A} + \bar{B}$

$$\overline{A + B} = \bar{A}\bar{B}$$



Example 5-11 Using appropriate dual symbols, redraw the logic diagram and develop the output expression for the circuit



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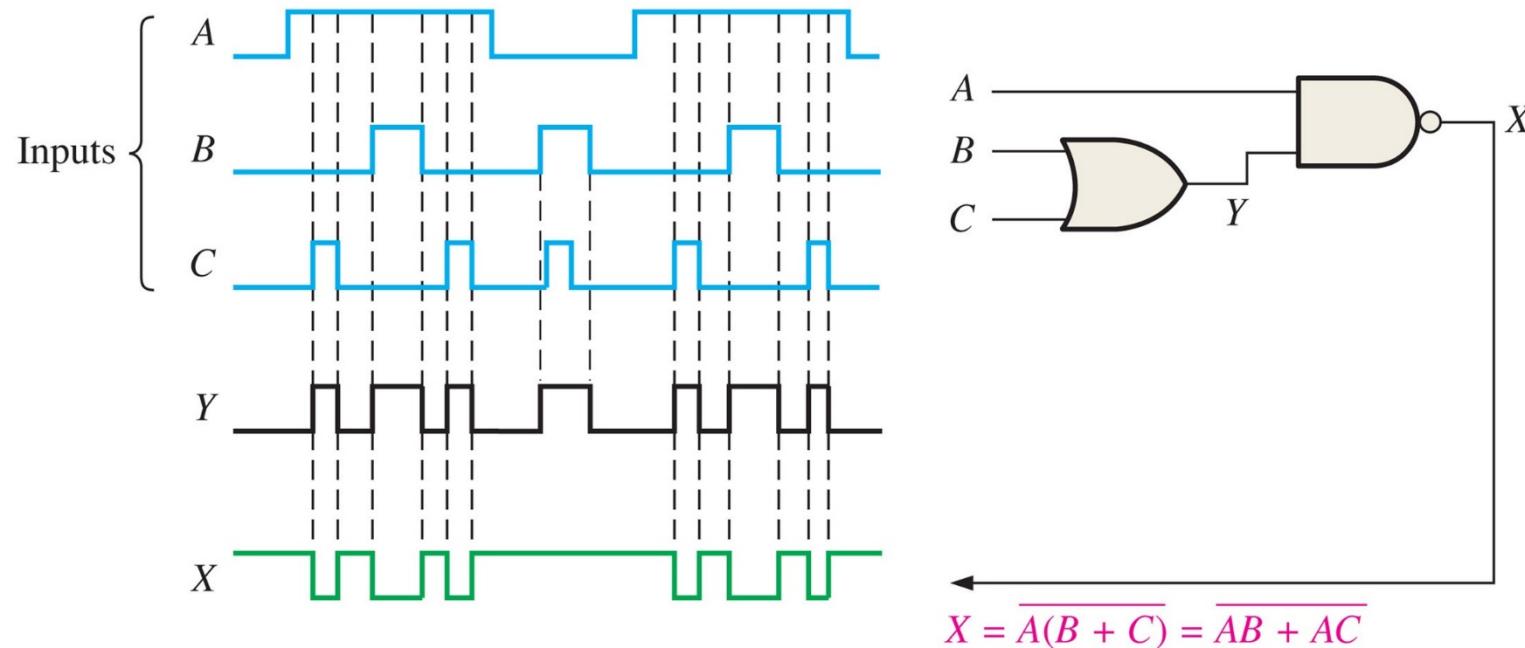
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Pulse Waveform Operation

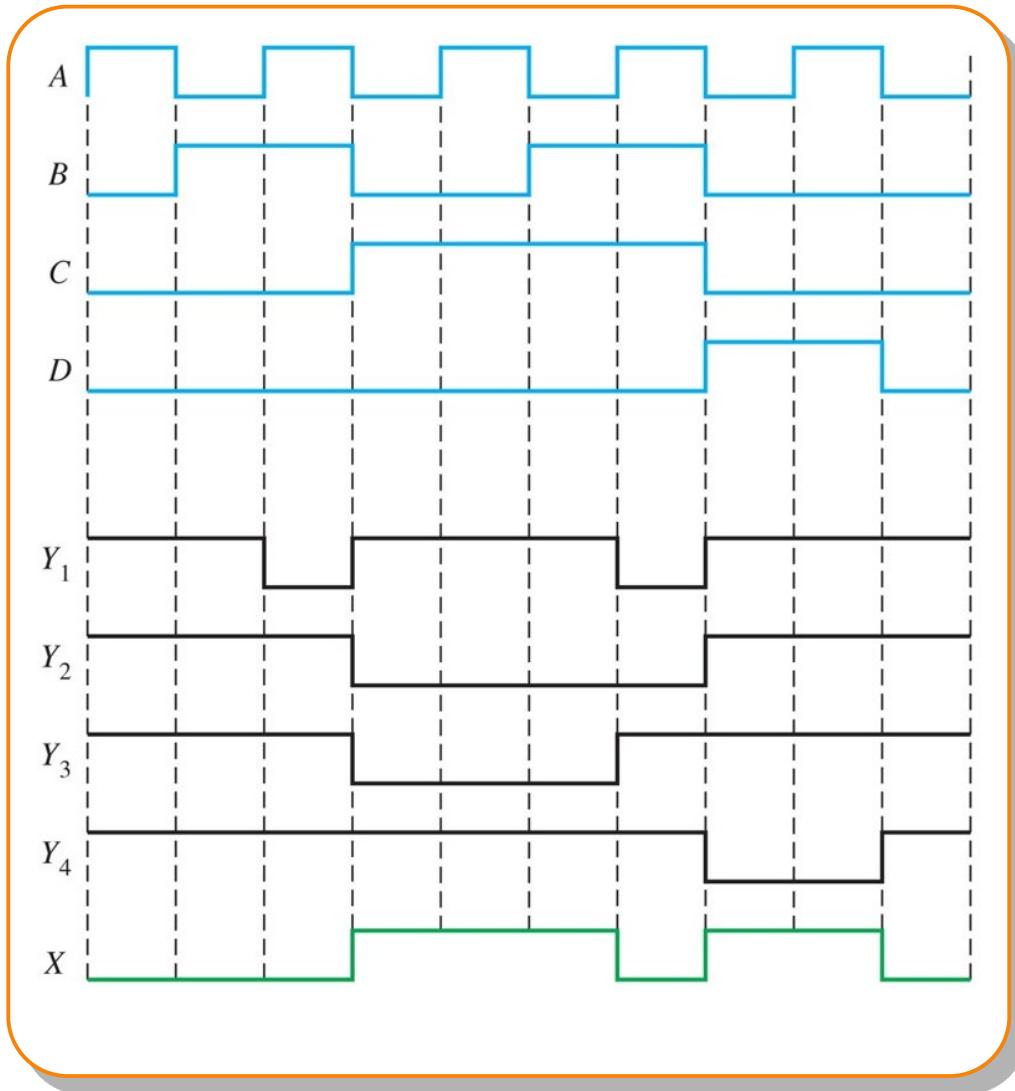
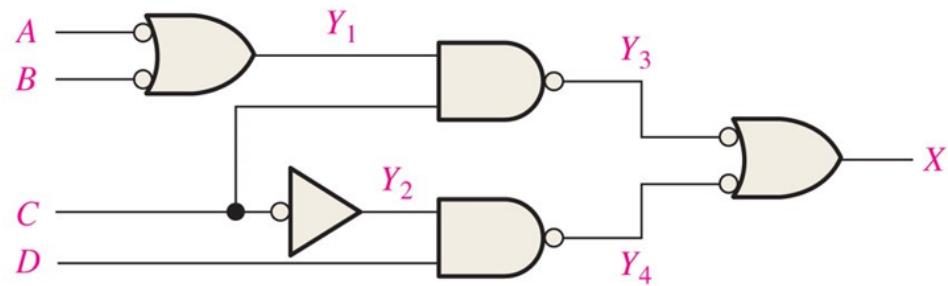
- Inputs: Pulse waveform inputs versus constant-level inputs
- Outputs: Depend on the inputs at that particular time → the relationship of the time-varying inputs is of primary importance.

Example 5-12 Determine the final output waveform X for the following circuit with input wave-forms A, B, and C as shown.



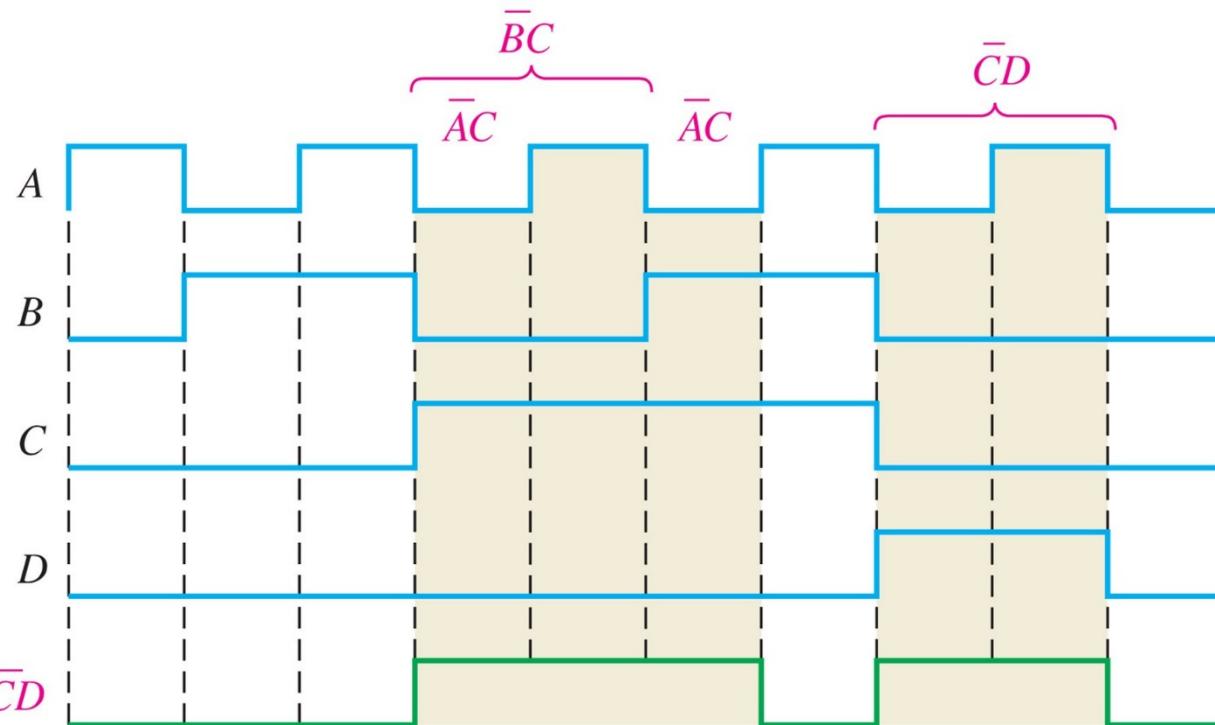
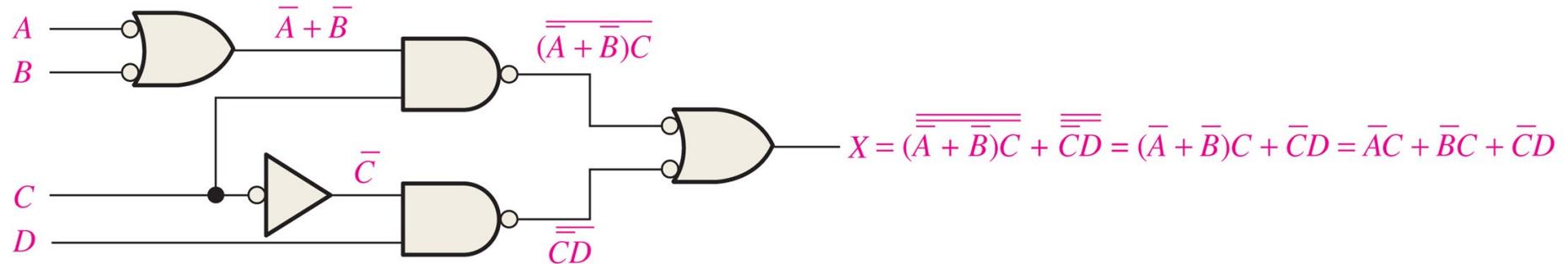
Example 5-14

Determine the output waveform X for the following logic circuit by first finding the intermediate waveform at each of points Y_1 , Y_2 , Y_3 , and Y_4 .



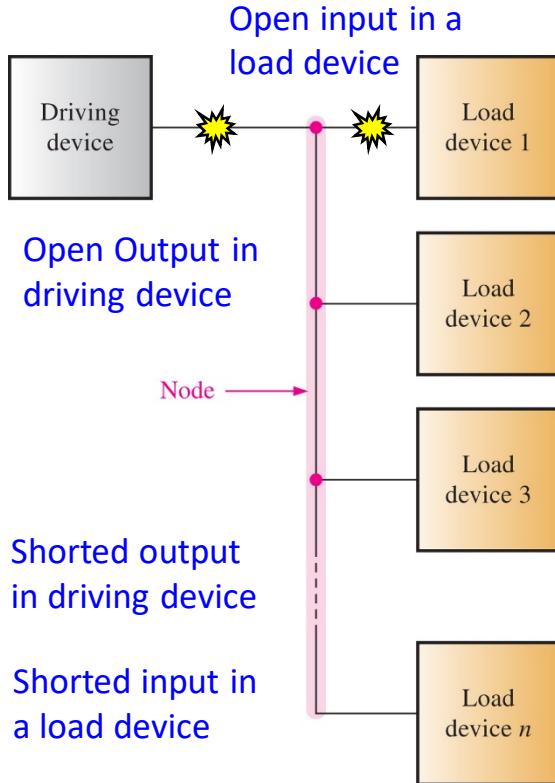
Example 5-15

Determine the output waveform X directly from the output expression.



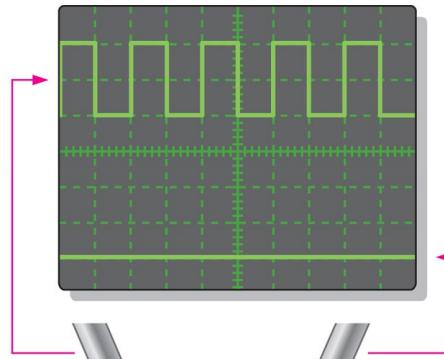
Troubleshooting: Open Output in driving device

Node: The interconnecting paths share a common electrical point known as a node

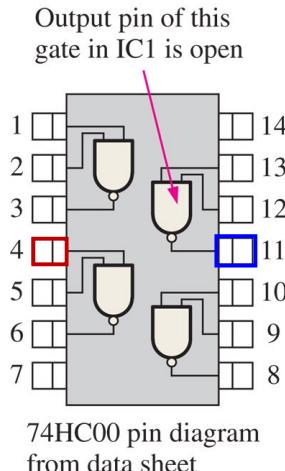


No pulse activity on the node → a loss of signal to all load devices.

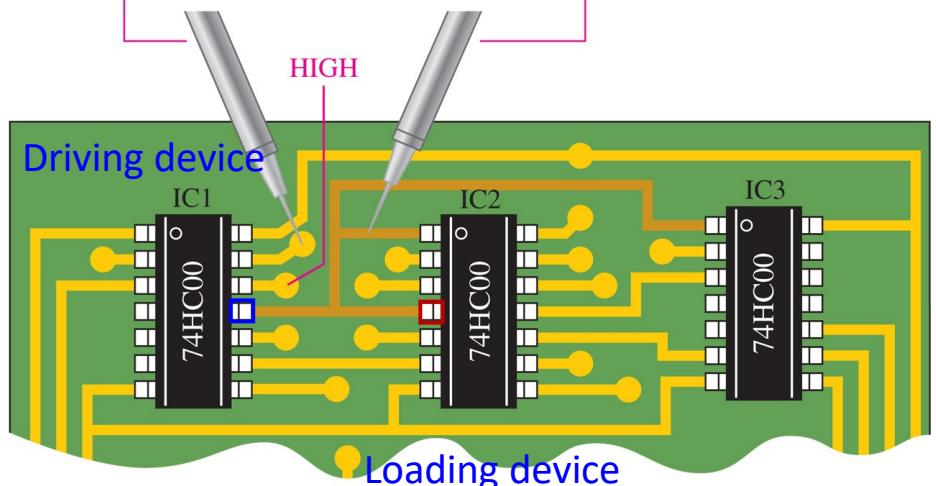
There are pulses on one input with the other input HIGH.



No pulse activity is indicated at any point on the node. Scope may indicate "floating" level.



74HC00 pin diagram from data sheet



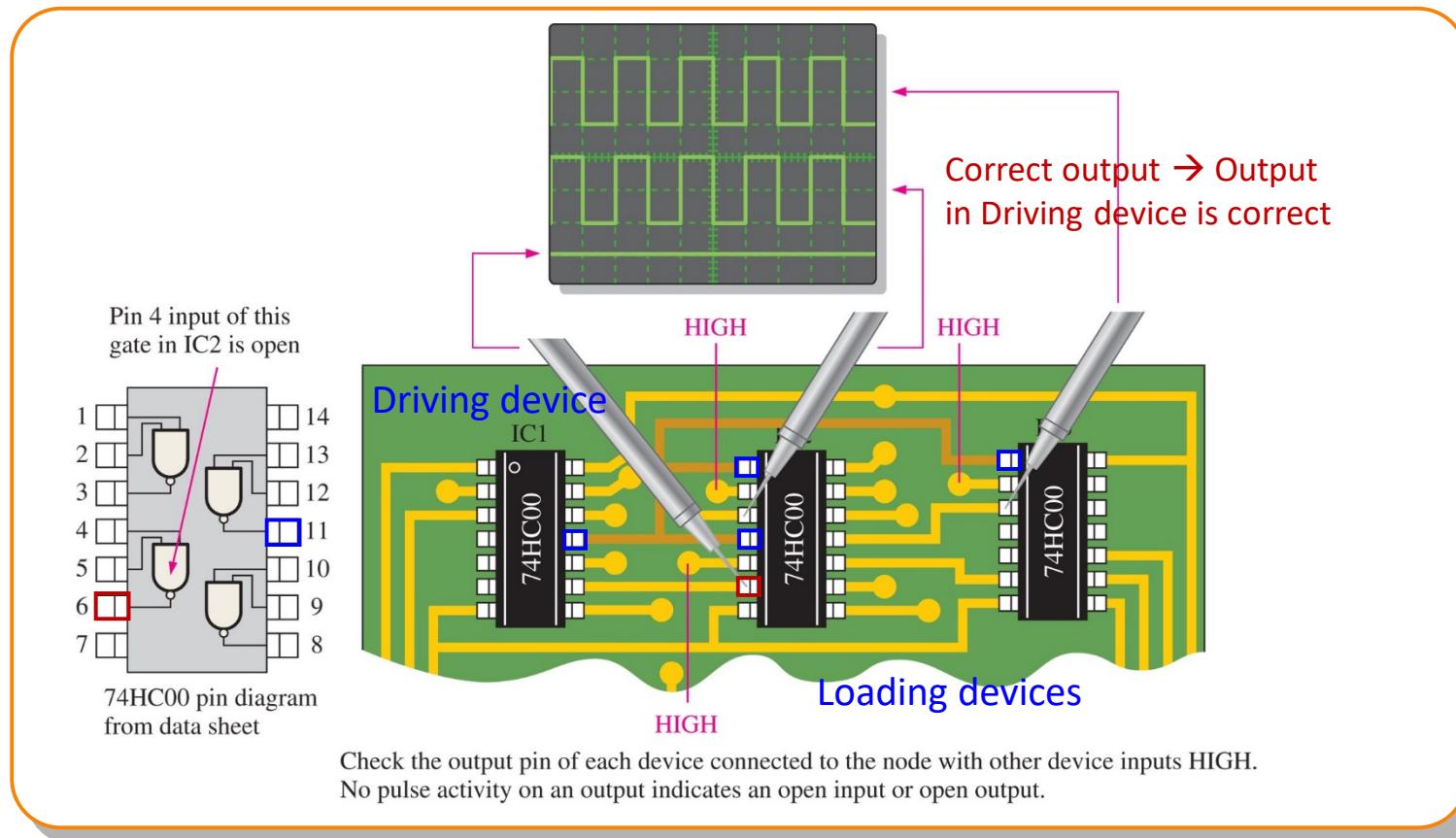
If there is no pulse activity at the output pin on IC1, there is an internal open. If there is pulse activity directly on the output pin but not on the node interconnections, the connection between the pin and the board is open.



Troubleshooting: Open input in a load device

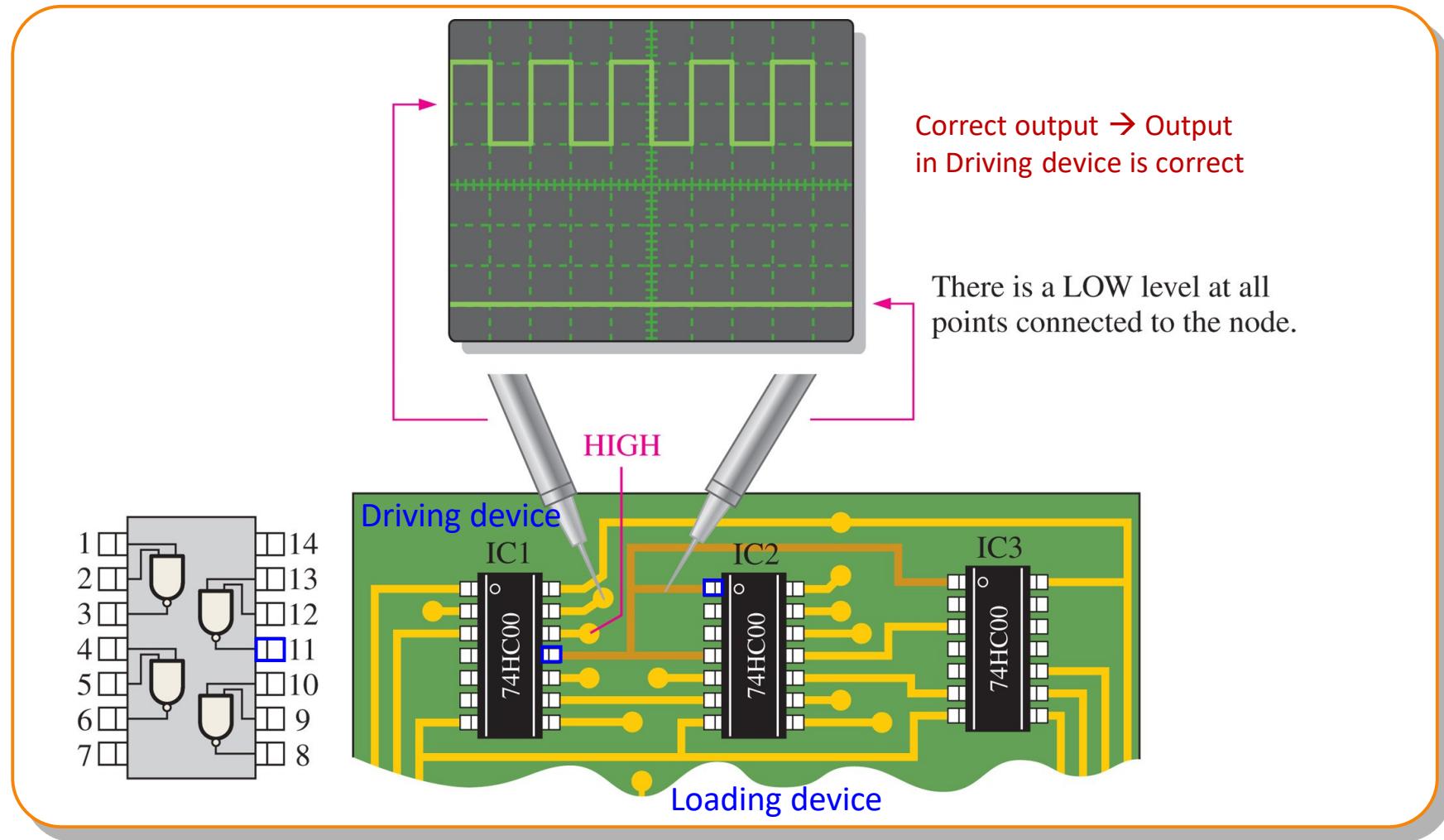
This failure will not affect the operation of any of the other devices connected to the node, but it will result in loss of signal output from the faulty device.

In the following example, the output of the driving device is connected to three inputs to three different gates two of which generate proper output waveforms.



Troubleshooting: Output or input shorted to Ground

The node is stuck LOW → Further checks are required.

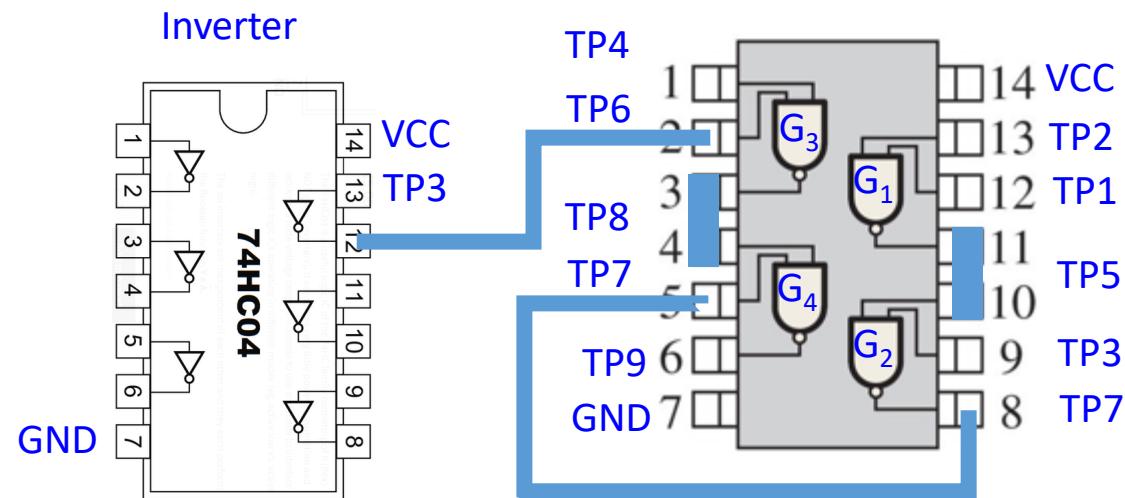
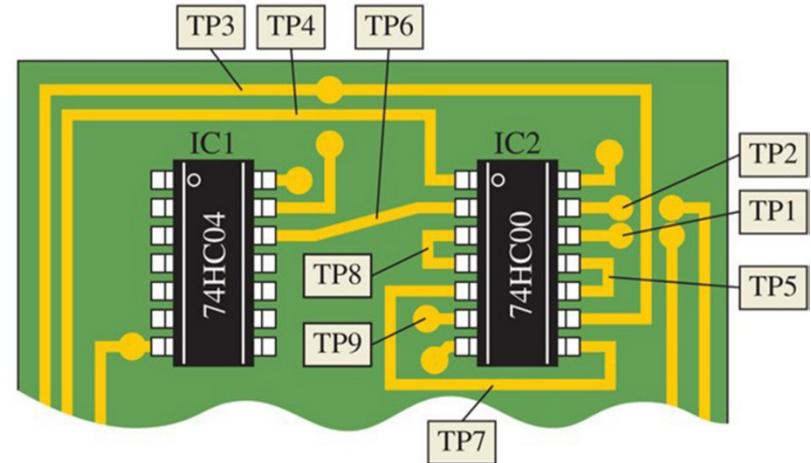
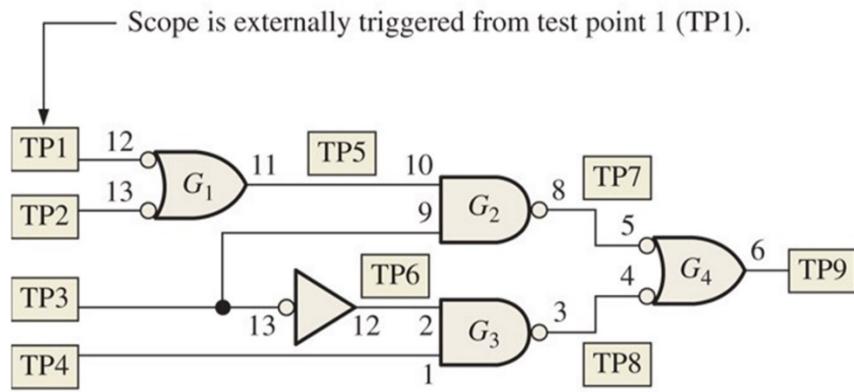


Signal Tracing and Waveform Analysis

- Observe the waveforms and their time relationships at all accessible points in the logic circuit;
- For each device, beginning at the input and working toward the output of the logic circuit, observe the output waveform of the device and compare it with the input waveforms by using the oscilloscope or the logic analyzer;
- If the output is incorrect, the device under test may be faulty;
- If the output is correct, go to the next device. Continue checking each device until an incorrect waveform is observed.



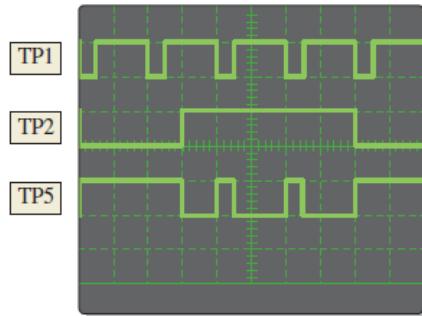
Building Circuits with Multiple Devices



Trouble-Shooting Example

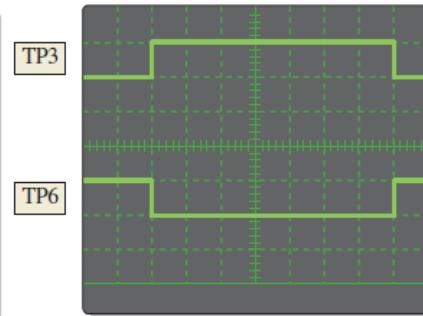
Step 1

- If correct, go to step 2.
- If incorrect, test IC2 and connections.



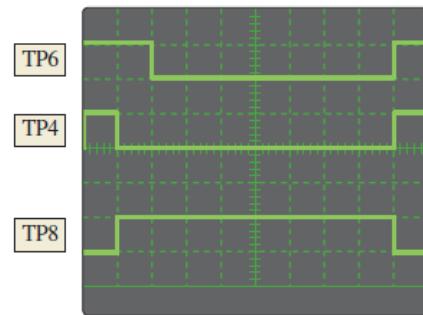
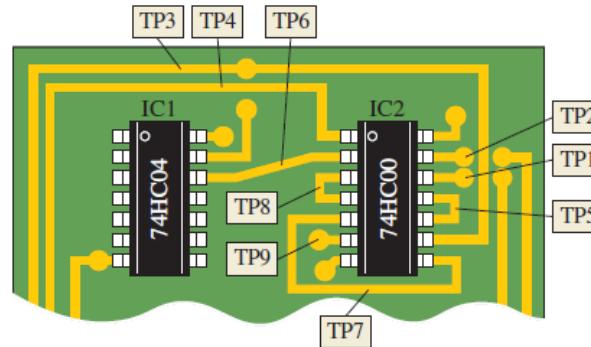
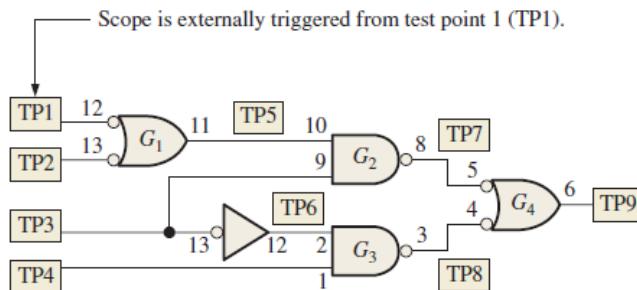
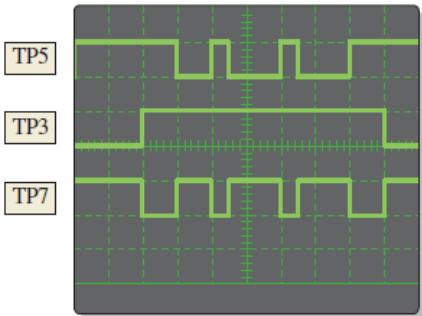
Step 2

- If correct, go to step 3.
- If incorrect, test IC1 and connections.



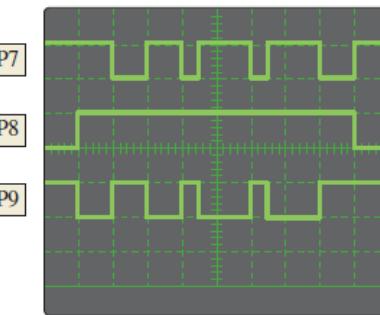
Step 3

- If correct, go to step 4.
- If incorrect, test IC2 and connections.



Step 4

- If correct, go to step 5.
- If incorrect, test IC2 and connections.



Step 5

- If correct, circuit is OK.
- If incorrect, test IC2 and connections.



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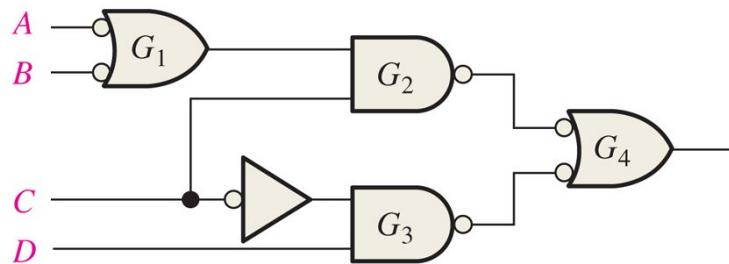
26

Example 5-17

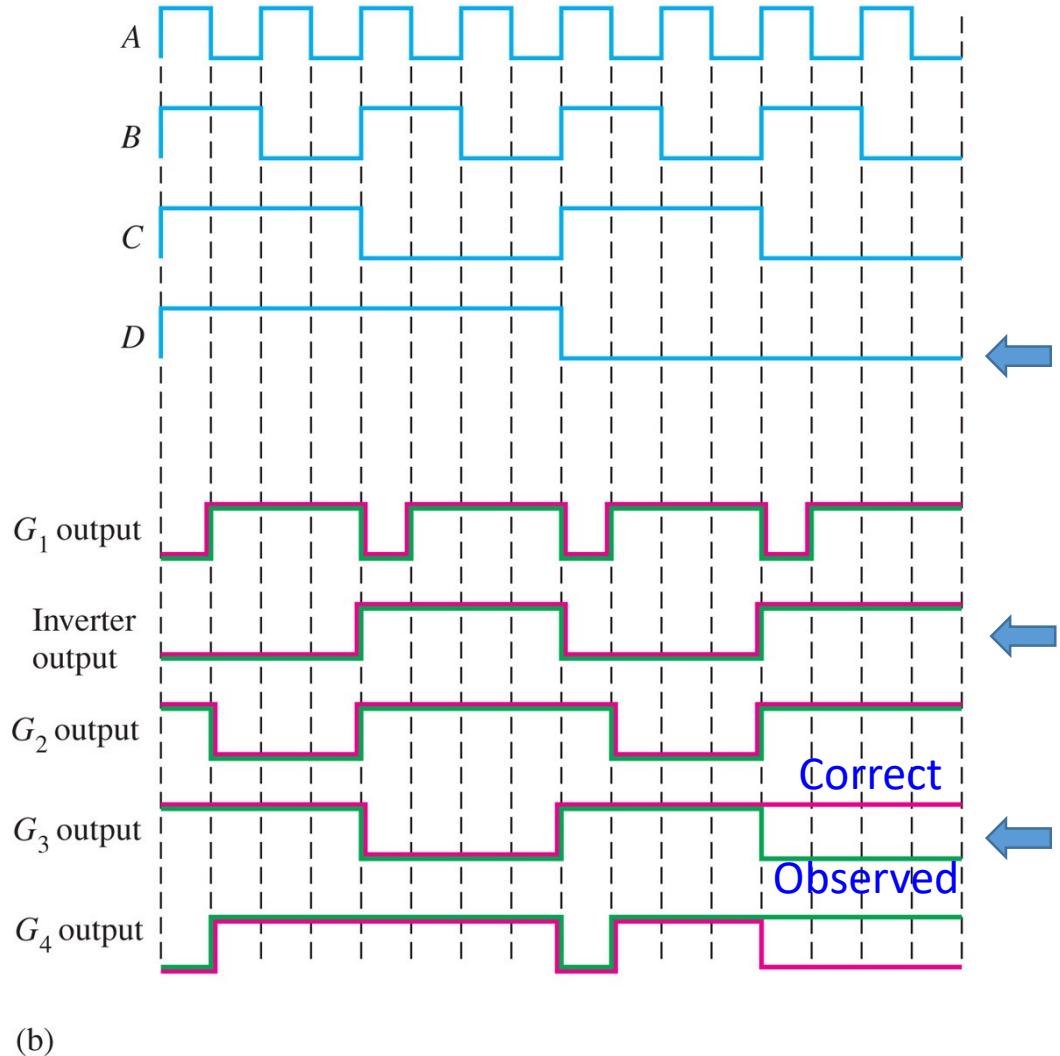
Determine the fault in the logic circuit by using waveform analysis. Waveforms in **green** are observed while those in **red** are correct.

Solution:

- ◆ Everything tested is correct until gate G3 is checked.
- ◆ If the D input to gate G3 is open and acting as a HIGH, you will get the output waveform measured.
- ◆ The output of G4 is also incorrect due to the incorrect input from G3.



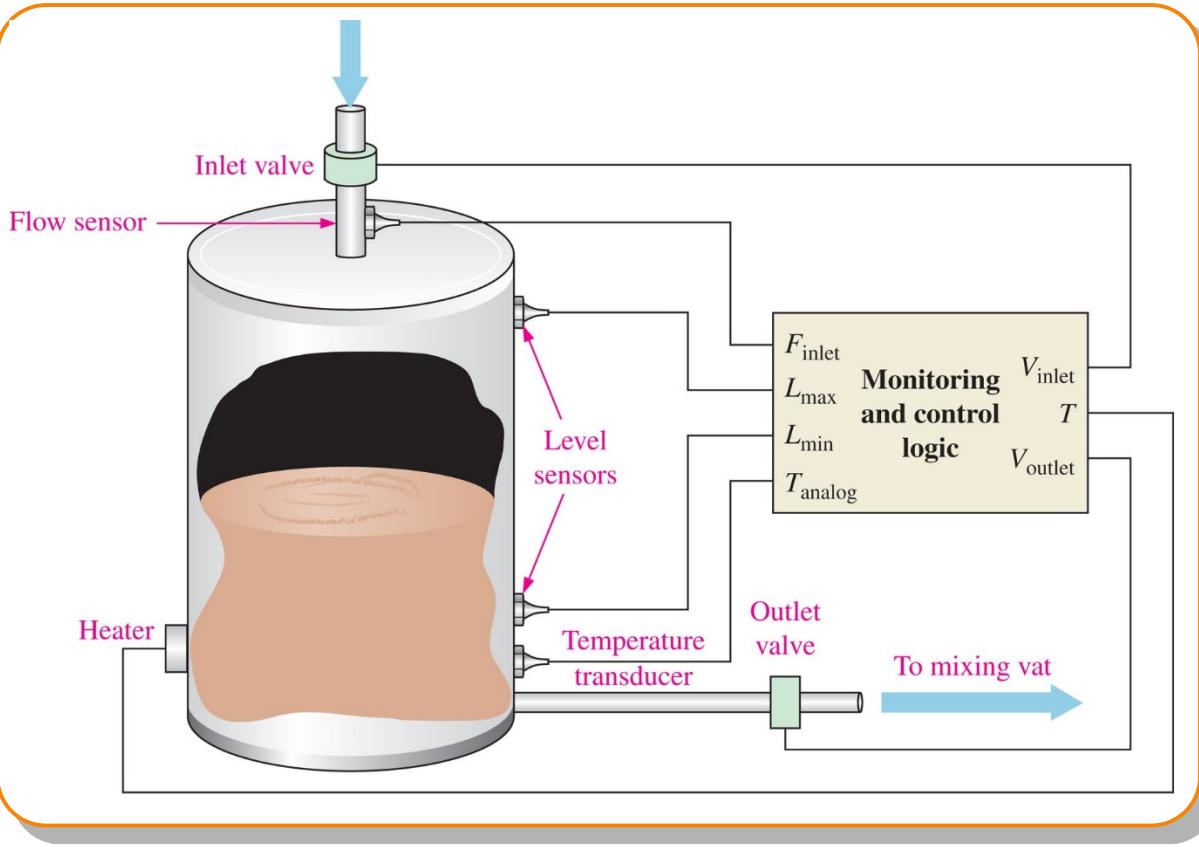
(a)



(b)



Applied Logic : Tank Control



□ Outlet Valve is open when

- ◆ The syrup level is above min. and the tank is not filling and
- ◆ The temp. of the syrup is at the specified value.

- Inlet Valve is open when
 - ◆ The solution level is at min. (L_{\min}) or
 - ◆ The tank is filling (F_{inlet}) but the max. level has not been reached (L_{\max})
- Temperature Control
 - ◆ The T output is HIGH if the measured temperature is below a specified temp.



Inlet Valve Control

- ◆ The solution level is at min. (L_{\min}) or
- ◆ The tank is filling (F_{inlet}) but the max. level has not been reached (L_{\max})

TABLE 5-6

Truth table for inlet valve control.

Inputs			Output	Description
L_{\max}	L_{\min}	F_{inlet}	V_{inlet}	
0	0	0	1	Level below minimum. No inlet flow.
0	0	1	1	Level below minimum. Inlet flow.
0	1	0	0	Level above min and below max. No inlet flow.
0	1	1	1	Level above min and below max. Inlet flow.
1	0	0	X	Invalid
1	0	1	X	Invalid
1	1	0	0	Level at maximum. No inlet flow.
1	1	1	0	Level at maximum. Inlet flow.

$$V_{\text{inlet}} = \overline{L}_{\max} \overline{L}_{\min} \overline{F}_{\text{inlet}} + \overline{L}_{\max} \overline{L}_{\min} F_{\text{inlet}} + \overline{L}_{\max} L_{\min} F_{\text{inlet}}$$



$$V_{\text{inlet}} = \overline{L}_{\min} + \overline{L}_{\max} F_{\text{inlet}}$$

L_{\max}	00	01	11	10
0	1	1	1	0
1	x	x	0	0



Outlet Valve Control

TABLE 5-7

Truth table for outlet valve control.

Inputs				Output	Description
L_{\max}	L_{\min}	F_{inlet}	T	V_{outlet}	
0	0	0	0	0	Level below minimum. No inlet flow. Temp low.
0	0	0	1	0	Level below minimum. No inlet flow. Temp correct.
0	0	1	0	0	Level below minimum. Inlet flow. Temp low.
0	0	1	1	0	Level below minimum. Inlet flow. Temp correct.
0	1	0	0	0	Level above min and below max. No inlet flow. Temp low.
0	1	0	1	1	Level above min and below max. No inlet flow. Temp correct.
0	1	1	0	0	Level above min and below max. Inlet flow. Temp low.
0	1	1	1	0	Level above min and below max. Inlet flow. Temp correct
1	0	0	0	X	Invalid
1	0	0	1	X	Invalid
1	0	1	0	X	Invalid
1	0	1	1	X	Invalid
1	1	0	0	0	Level at maximum. No inlet flow. Temp low.
1	1	0	1	1	Level at maximum. No inlet flow. Temp correct.
1	1	1	0	0	Level at maximum. Inlet flow. Temp low.
1	1	1	1	0	Level at maximum. Inlet flow. Temp correct.

- ◆ The syrup level is above min. and the tank is not filling and
- ◆ The temp. of the syrup is at the specified value.

$$V_{\text{outlet}} = \overline{L}_{\max} \overline{L}_{\min} \overline{F}_{\text{inlet}} T + L_{\max} \overline{L}_{\min} \overline{F}_{\text{inlet}} \overline{T}$$

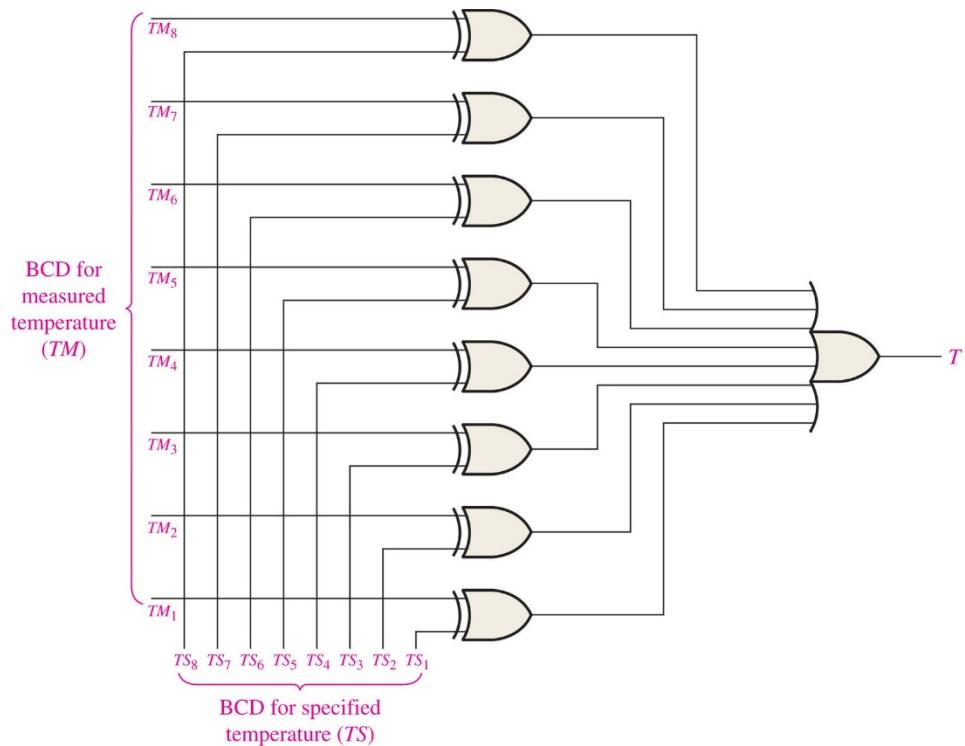


$$V_{\text{outlet}} = L_{\min} \overline{F}_{\text{inlet}} T$$

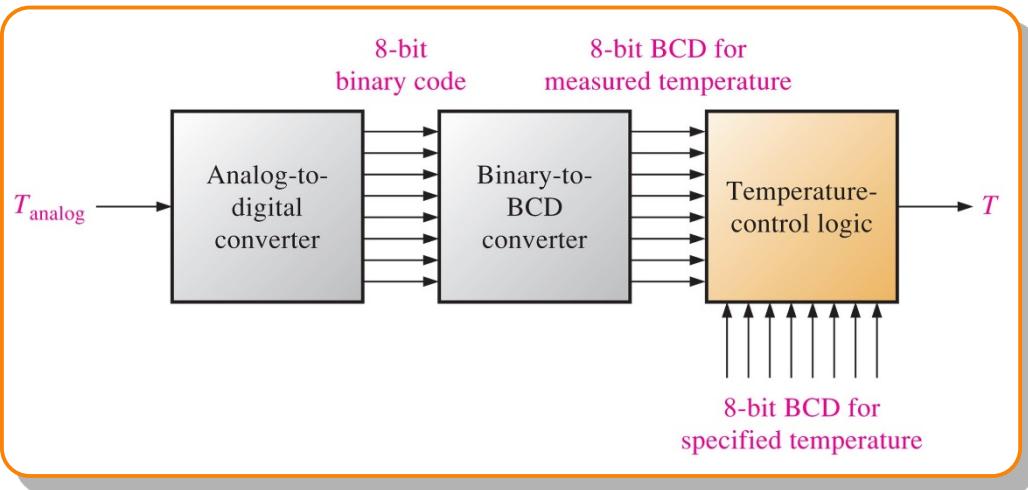


Temperature Control

- ◆ The T output is HIGH if the measured temperature is below a specified temp.



Any potential concerns with this design?



- ◆ If the bits are the same, XOR outputs 0;
- ◆ if they are different, XOR outputs 1.

When one or more XOR outputs equal 1, the T output of the OR gate equals 1, causing the heater to turn on.



Chapter Review

□ Basic Combinational Logic Circuits

- ◆ AND-OR Logic
- ◆ AND-OR-Invert Logic
- ◆ Exclusive-OR Logic $X = A\bar{B} + \bar{A}B = A \oplus B$
- ◆ Exclusive-NOR Logic $X = \bar{A}\bar{B} + AB$

□ The Universal Property of NAND Gates

- ◆ $\overline{AB} = \bar{A} + \bar{B}$ $\overline{A + B} = \bar{A}\bar{B}$
- ◆ Combinations of NAND gates can function as NOT, AND, OR, and NOR
- ◆ Combinations of NOR gates can function as NOT, AND, OR, and NAND.

□ Dual Symbols :

- ◆ NAND Logic Diagrams Using Dual Symbols : NAND and Negative-OR;
- ◆ NOR Logic Diagrams Using Dual Symbols : NOR and Negative-AND

□ Troubleshooting: Pulse Waveform Operation



True/False Quiz

- AND-OR logic can have only two 2-input AND gates.
- AOI is an acronym for AND-OR-Invert.
- If the inputs of an exclusive-OR gate are the same, the output is LOW (0).
- If the inputs of an exclusive-NOR gate are different, the output is HIGH (1).
- A parity generator cannot be implemented using exclusive-OR gates.
- NAND gates can be used to produce the AND functions.
- NOR gates cannot be used to produce the OR functions.
- Any SOP expression can be implemented using only NAND gates.
- The dual symbol for a NAND gate is a negative-AND symbol.
- Negative-OR is equivalent to NAND.



True/False Quiz

- AND-OR logic can have only two 2-input AND gates.
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