

EIE 2050 Digital Logic and Systems

Chapter 7 : Latches, Flip-Flops and Timers

Simon Pun, Ph.D.



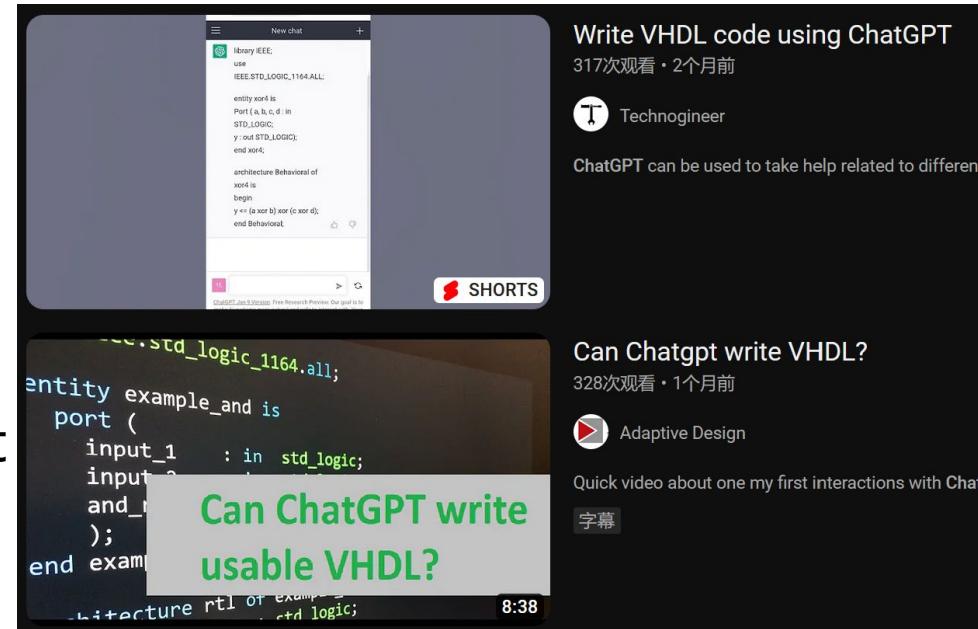
Announcements

□ Office Hour for THIS week (3/20-24)

- ◆ Changed to 3/23 (Thur.) 16:00-18:00

□ Project

- ◆ Will start after midterm
- ◆ To learn hardware programming language VHDL
- ◆ To implement a serial-in-parallel-out shift register



Company Visit in April

-  生益科技
SYTECH
- 总部位于东莞市松山湖，于1985年成立
- 电子电路基材供应商，主营业务是生产覆铜板以及PCB制造
- 全球覆铜板龙头，全球市场份额排名第二



全国大学生集成电路创新创业大赛 (CICIEC)

赛事介绍：集成电路，当今全球科技竞争的重中之重。全国最大规模的集成电路学科技竞赛——全国大学生集成电路创新创业大赛是由工信部举办，以服务产业发展需求为导向，以提升我国集成电路产业人才培养质量为目标，打造产学研用协同创新平台，将行业发展需求融入教学过程，提升在校大学生创新实践能力、工程素质以及团队协作精神，助力我国集成电路产业健康快速发展。集创赛全国共分7大赛区，划分8大赛道21个杯赛：射频与高速电路设计赛道、模拟与混合信号电路赛道、数字与SoC设计赛道、处理器设计与应用赛道、**FPGA设计与应用赛道（海云捷迅杯-基于FPGA机器视觉缺陷检测的实现）**、半导体产业链赛道、创业实践赛道、芯片设计与应用本科赛道。往年参赛中，理工学院有2支队伍获得全国总决赛三等奖，1支队伍获得全国总决赛优秀奖。

赛事日程：2023年5月31日前提交初赛作品，6月初赛，7月分赛区决赛，8月全国总决赛

赛事官网：univ.ciciec.com

赛事公众号：全国大学生集成电路创新创业大赛

报名截止时间：2023年3月31日23:59



2023集创赛大群



报名链接



DIGILENT
Nexys Video
(2020、2021)



海云捷迅
AI Edge Platform
(2022、2023)



往年参赛

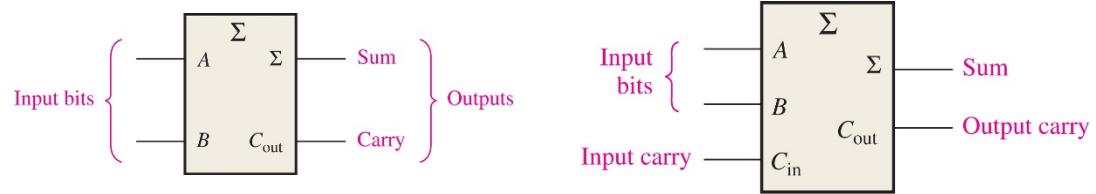


香港中文大學(深圳)

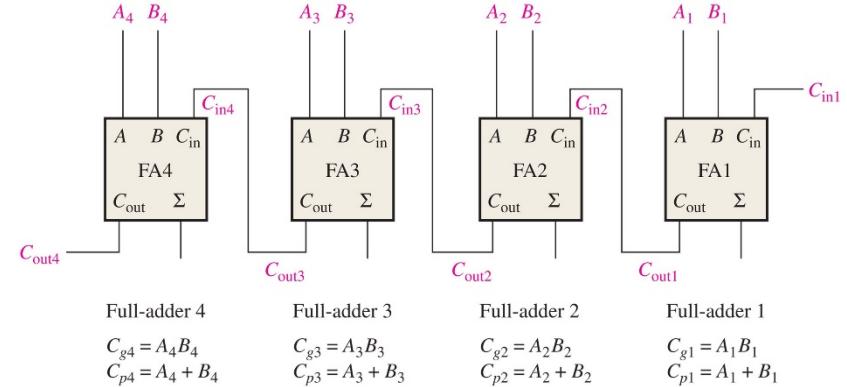
The Chinese University of Hong Kong, Shenzhen

Spring 2023 EIE2050 Digital Logic and Systems

Last Week

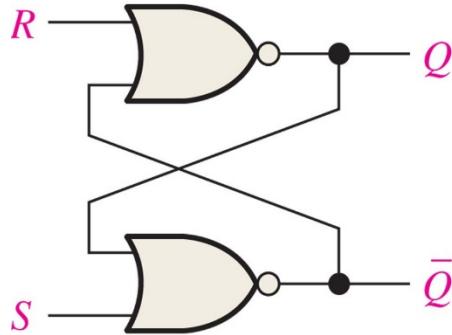


- Half and Full Adders
- Parallel Binary Adders
- Ripple Carry and Look-Ahead Carry Adders
- Comparators
- Decoders (n input lines \rightarrow max. 2^n output lines)
- Encoders (e.g. Decimal-to-BCD Priority Encoder)
- Code Converters (e.g. BCD-to-Binary Conversion)
- Multiplexers (To route several inputs onto a single output line)
- Demultiplexers
- Parity Generators/Checkers (Check for parity or generate a parity bit for a binary code)
- Troubleshooting (Glitches and Strobing)

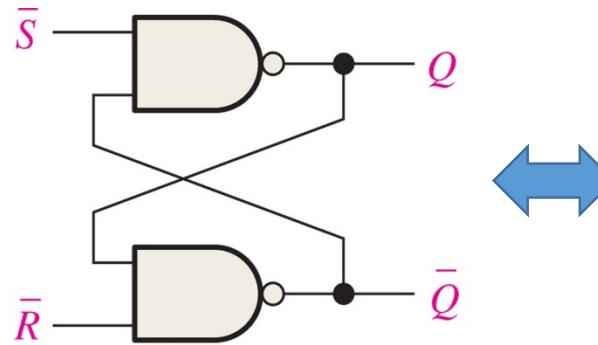


Latches

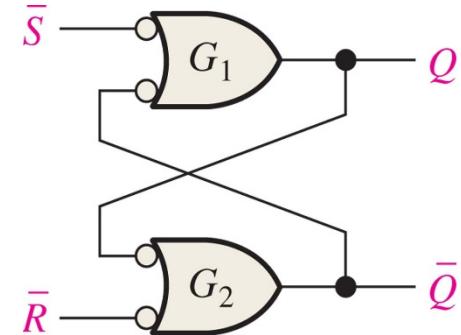
- A temporary storage device that has two stable states (bistable);



(a) Active-HIGH input S-R latch



(b) Active-LOW input \bar{S} - \bar{R} latch



- **Initial state:** both \bar{S} and \bar{R} inputs & the Q output are HIGH
- **RESET state:** \bar{R} is temporarily LOW, \bar{Q} @ $G_2 \rightarrow$ HIGH and $Q@G_1 \rightarrow$ LOW;
- This LOW on $Q@G_1$ is then coupled back to an input of G_2 , ensuring that the \bar{Q} output remains HIGH even when the LOW on the \bar{R} input is removed;
- **SET state:** $Q@G_1$ is LOW and the latch remains indefinitely in the RESET state until a momentary LOW is applied to the \bar{S} input, $Q@G_1 \rightarrow$ HIGH.



Latch operations

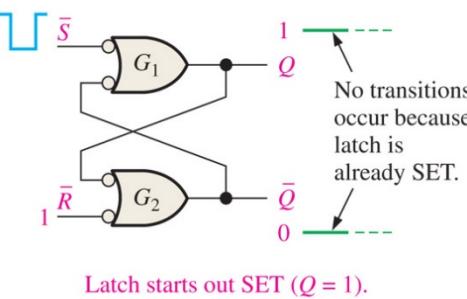
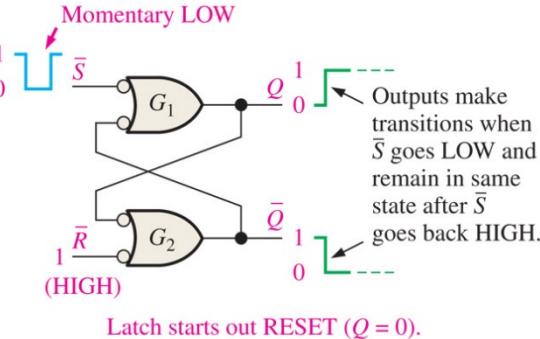


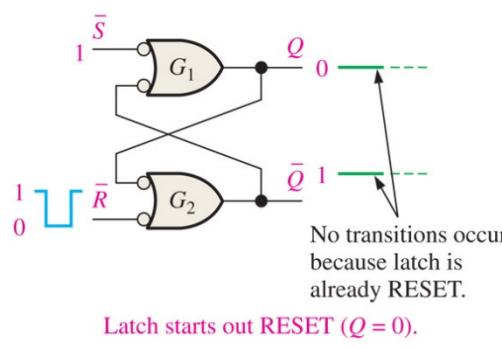
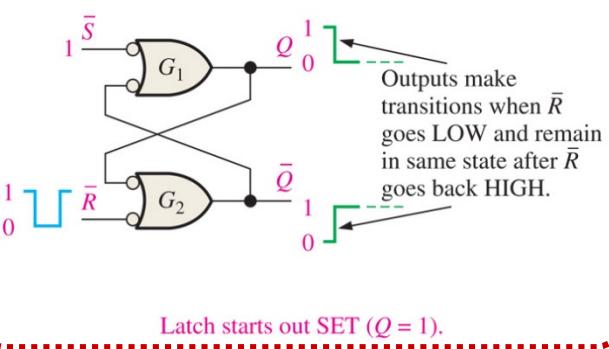
TABLE 7-1

Truth table for an active-LOW input \bar{S} - \bar{R} latch.

Inputs		Outputs		Comments
\bar{S}	\bar{R}	Q	\bar{Q}	
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

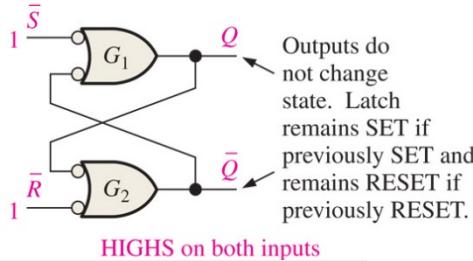
SET means that the Q output is HIGH.

Two possibilities for the SET operation

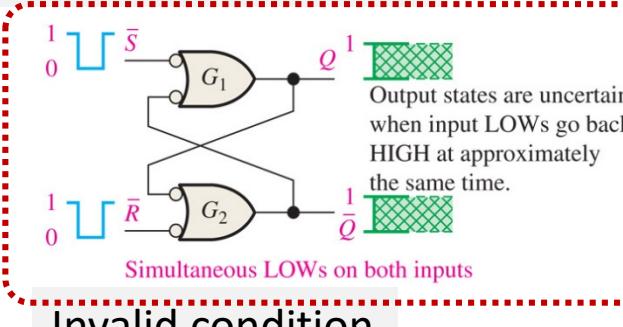


RESET means that the Q output is LOW.

Two possibilities for the RESET operation



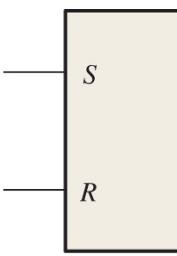
NO change condition



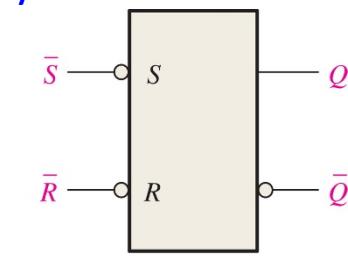
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Logic symbols



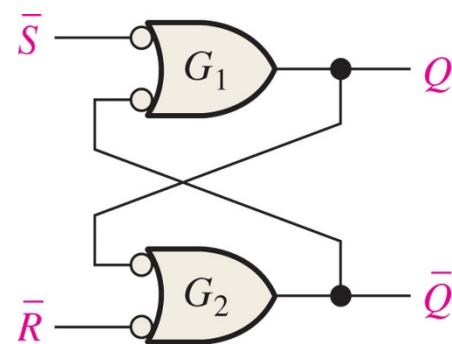
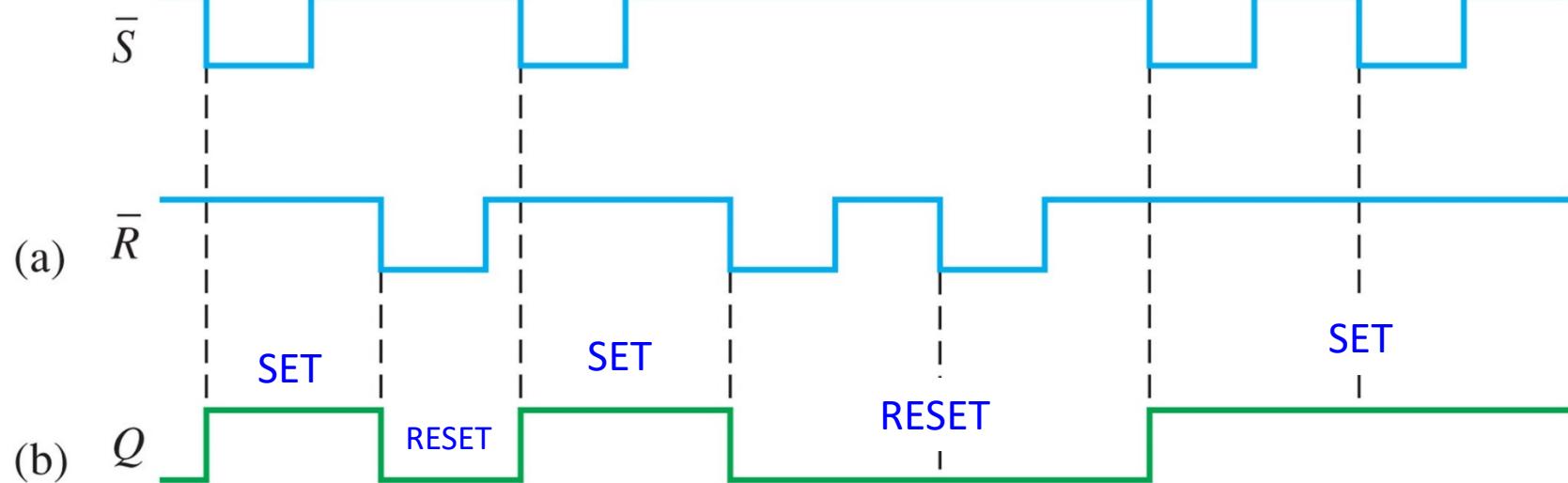
(a) Active-HIGH input S-R latch



(b) Active-LOW input S-R latch

Example 7-1

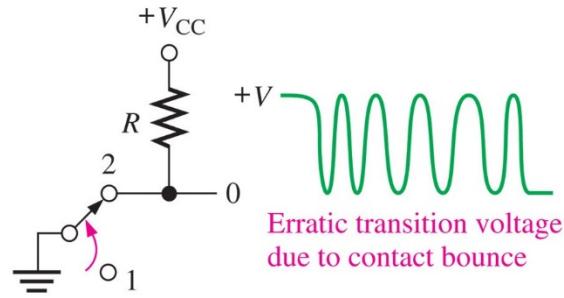
Both S and R are HIGH at the same time \rightarrow no change



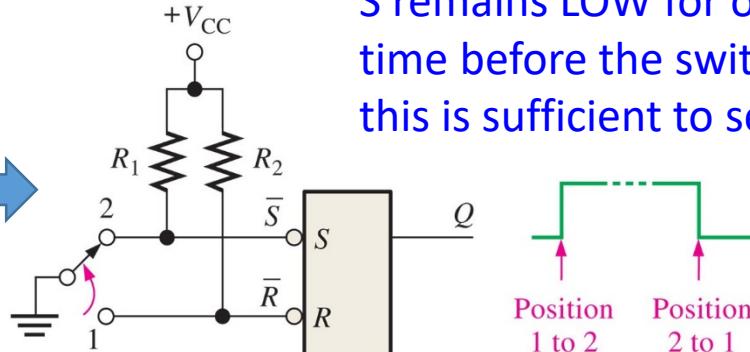
If both S and R are LOW at the same time, then the condition is invalid. Fortunately, it did not happen in this example.



Application: Latch as a Contact-Bounce Eliminator

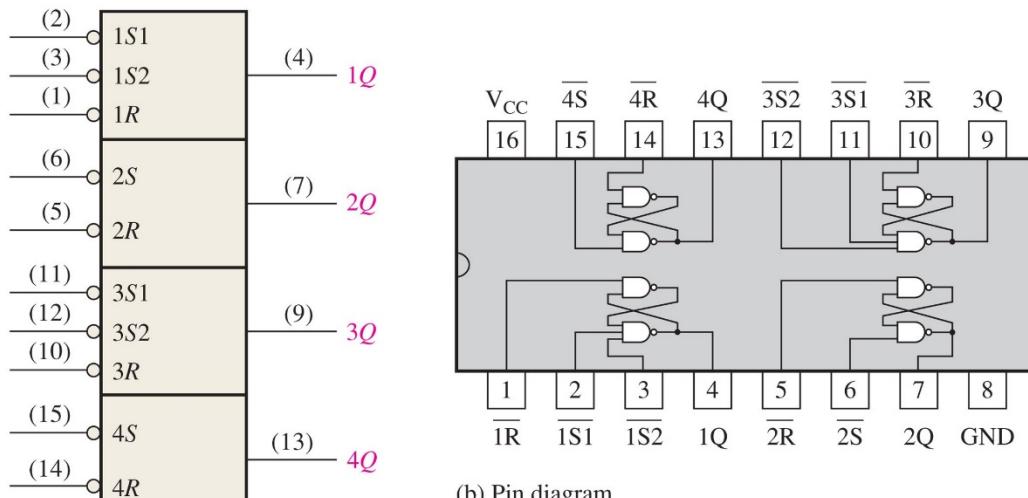


Physically bounces several times
before finally making a solid contact



(b) Contact-bounce eliminator circuit

\bar{S} remains LOW for only a very short time before the switch bounces, this is sufficient to set the latch

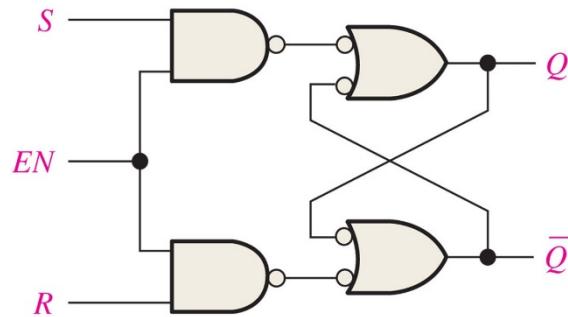


(a) Logic diagram

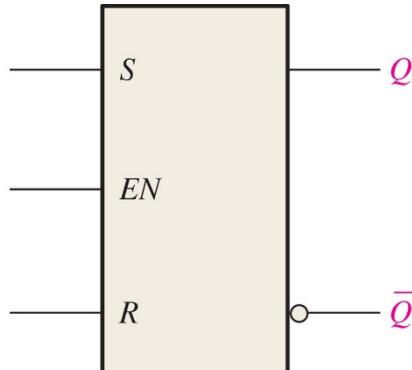
The 74HC279A is a quad $\bar{S}-\bar{R}$ latch



The Gated S-R Latch

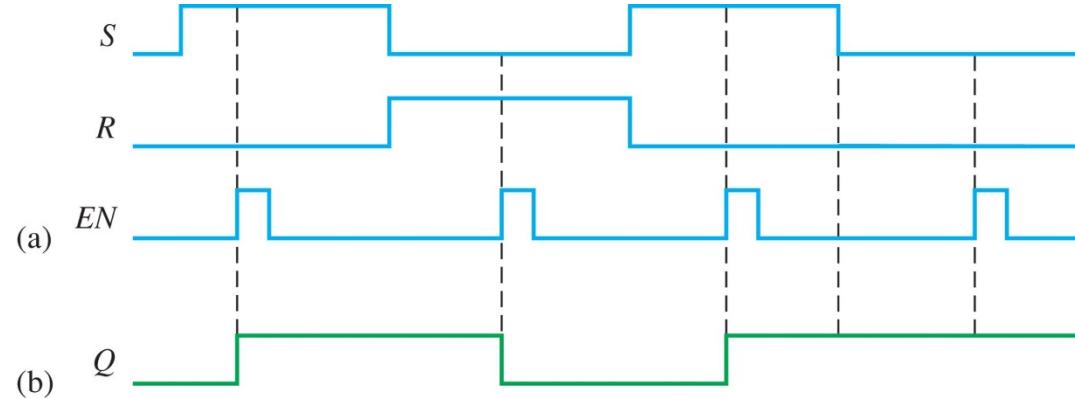


(a) Logic diagram

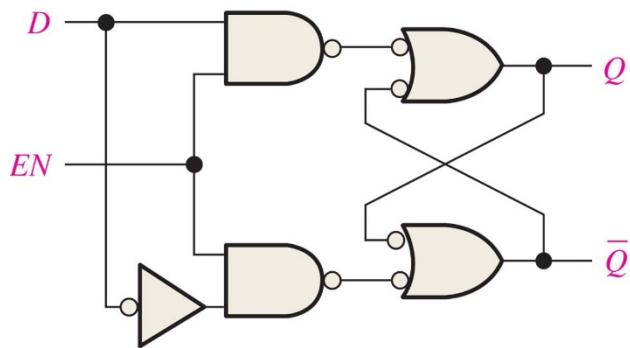


(b) Logic symbol

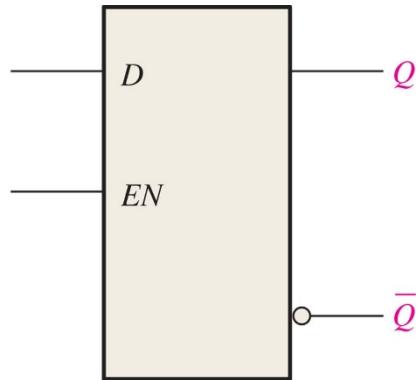
- The latch will not change its state until EN is HIGH
- When enabled, the NAND gates outputs are \bar{S} and \bar{R} , respectively.
- Invalid state occurs when both S and R are simultaneously HIGH and EN is also HIGH



The Gated D Latch

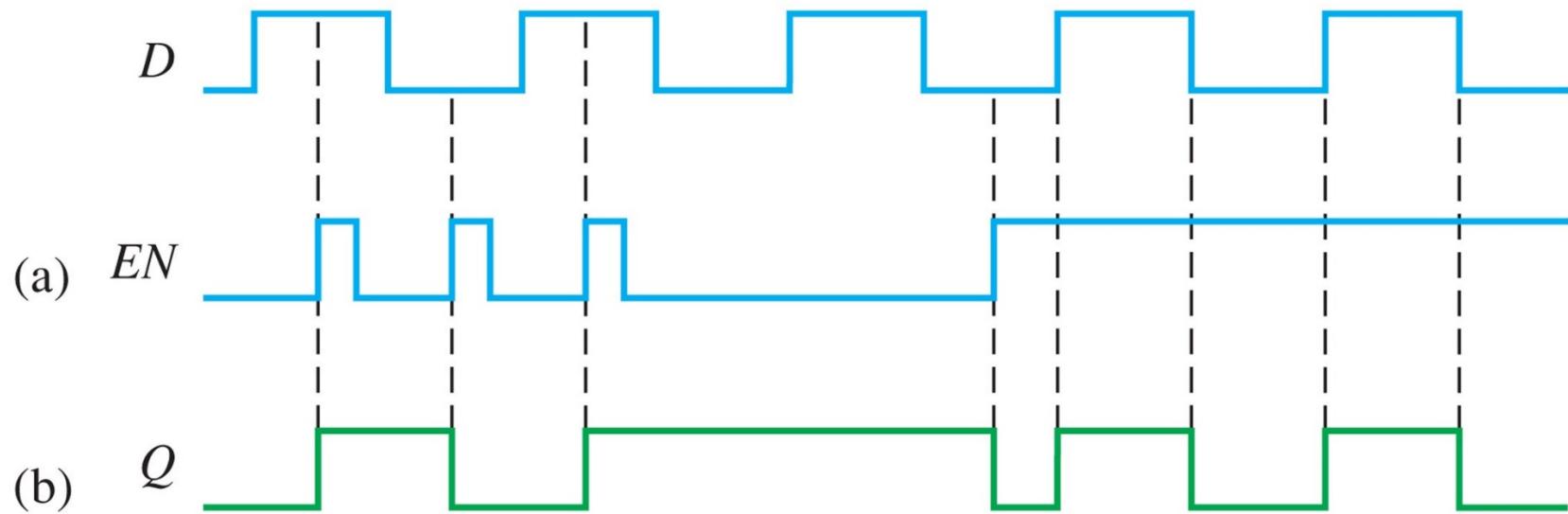


(a) Logic diagram



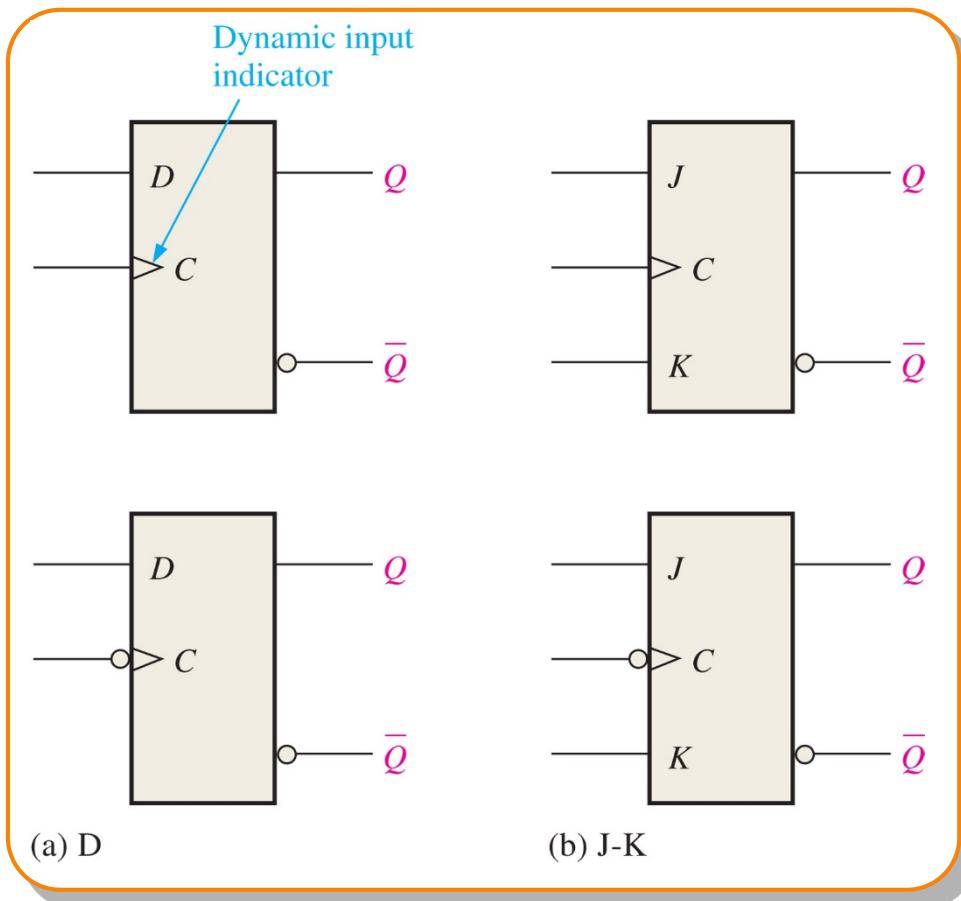
(b) Logic symbol

- Has only one input called the D (data) input & EN.
- **SET:** when D and EN are HIGH
- **RESET:** when D is LOW and EN is HIGH



Flip-Flops

- Flip-flops are synchronous bistable devices whose output **synchronously** changes state only at the **rising/positive** (no bubble at C input) or **falling/negative** edge (bubble at C input) of the clock (CLK)



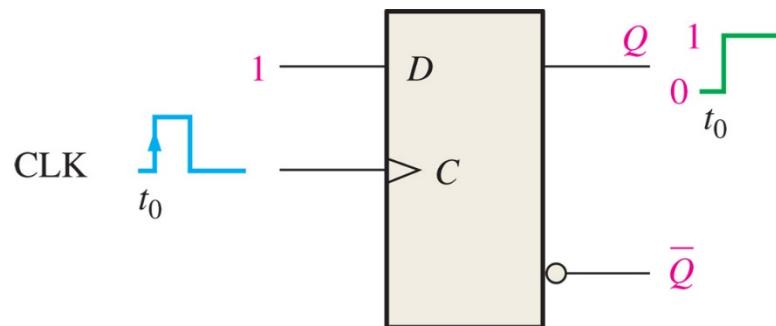
- An edge-triggered flip-flop is characterized by **the small triangle** inside the block at the clock (C) input. This triangle is called the **dynamic input indicator**.
- Note: the Gated S-R latch is enabled when EN is HIGH (NOT only the edge)
- Edge detection will be covered later.



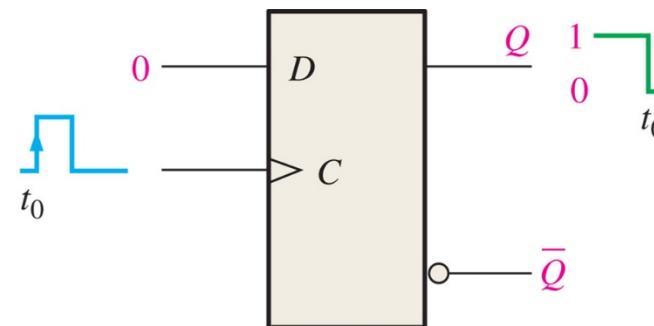
TABLE 7-2

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	CLK	Q	\bar{Q}	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

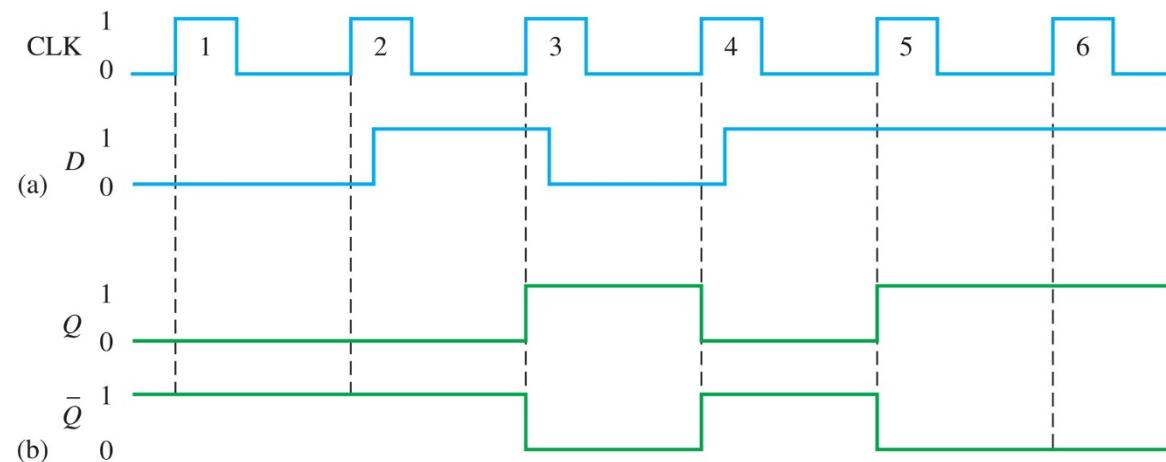
 \uparrow = clock transition LOW to HIGH

(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

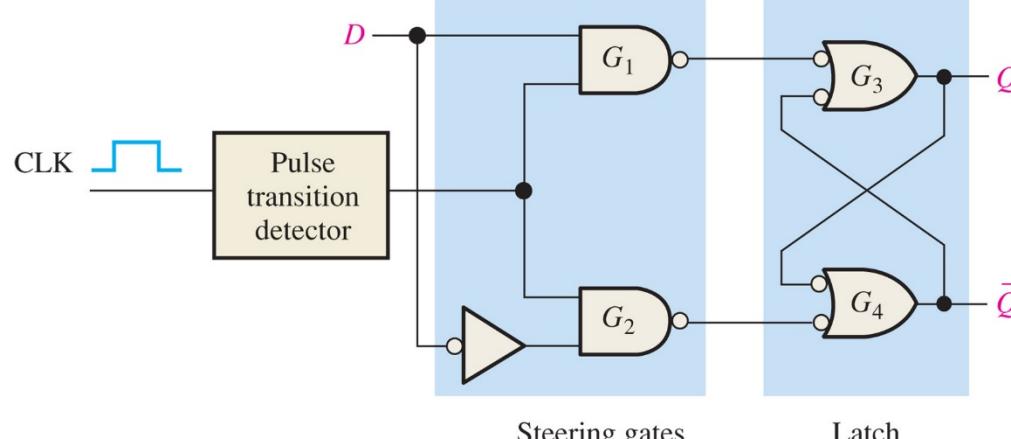


(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

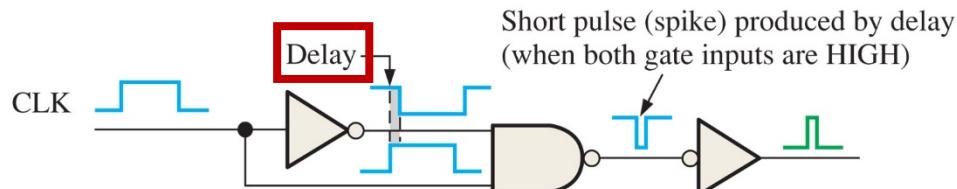
EXAMPLE 7-4 Assume that the positive edge-triggered flip-flop is initially RESET.



Edge-Triggered Operation (D Flip-Flop)



(a) A simplified logic diagram for a positive edge-triggered D flip-flop



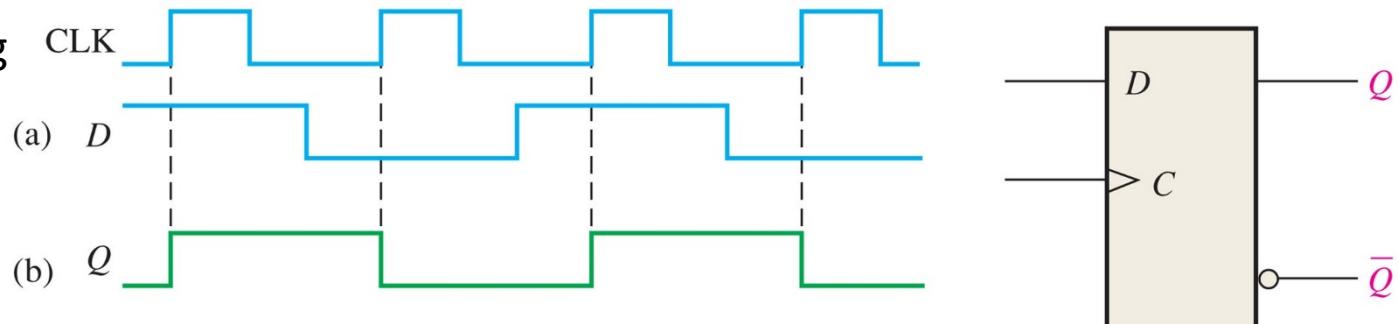
(b) A type of pulse transition detector

□ By exploiting a small delay through the inverter on one input to the NAND gate, generate a very short-duration spike on the positive-going transition of the clock pulse.



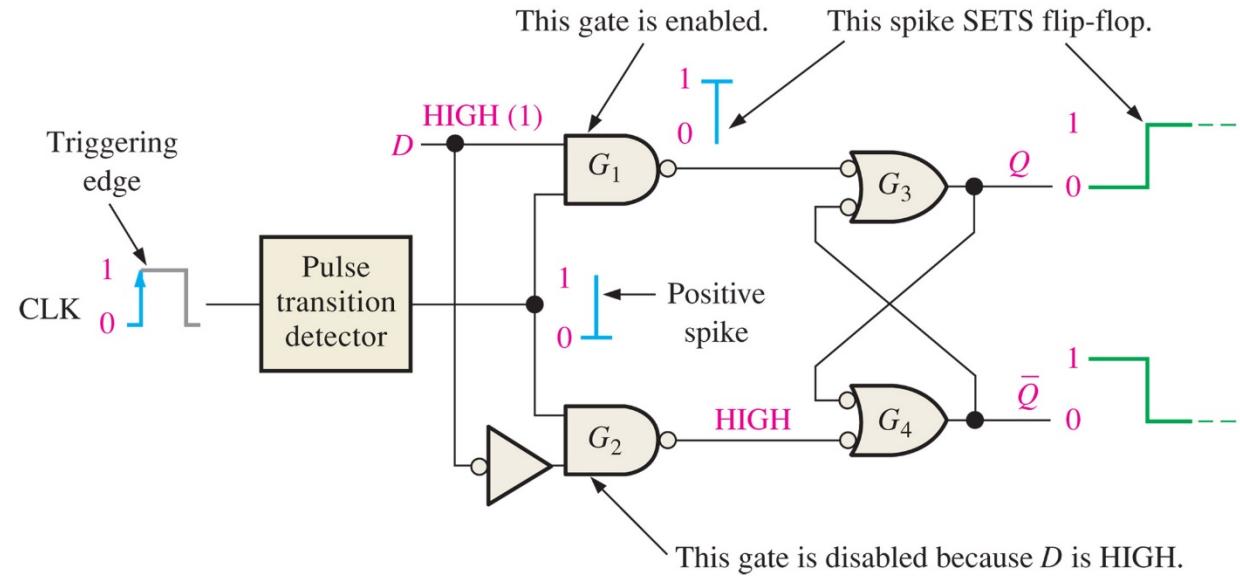
What about falling edge detection?

EXAMPLE 7–6 Assuming that the flip-flop is initially RESET

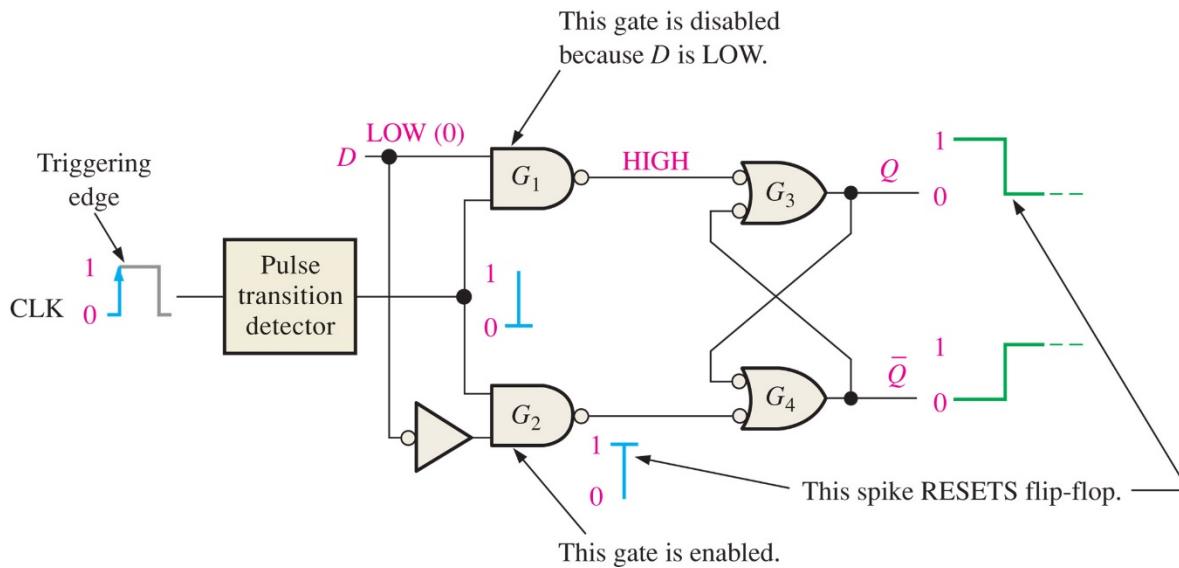


Examples: Transitions Between States

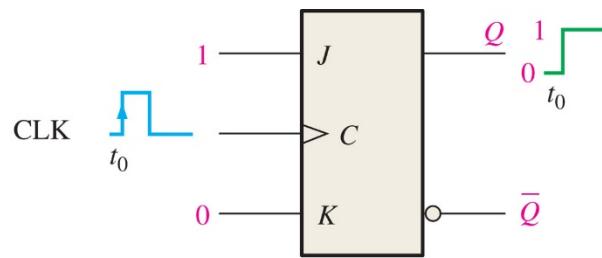
RESET \rightarrow SET



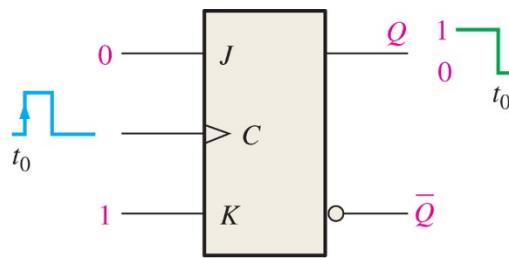
SET \rightarrow RESET



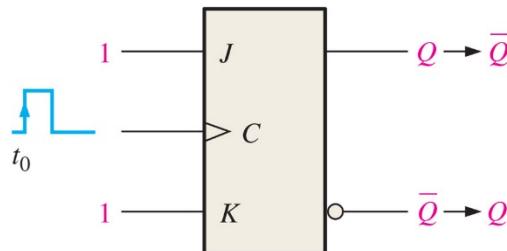
The J-K Flip-Flop



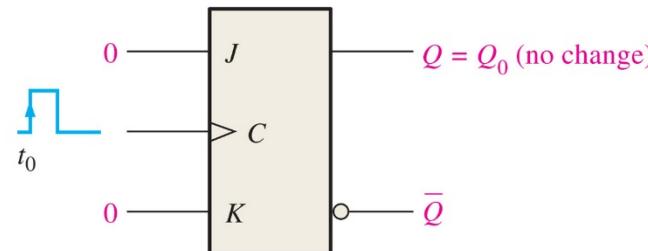
(a) $J = 1, K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $J = 0, K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $J = 1, K = 1$ flip-flop changes state (toggle).



(d) $J = 0, K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

TABLE 7-3

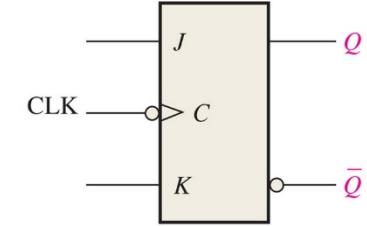
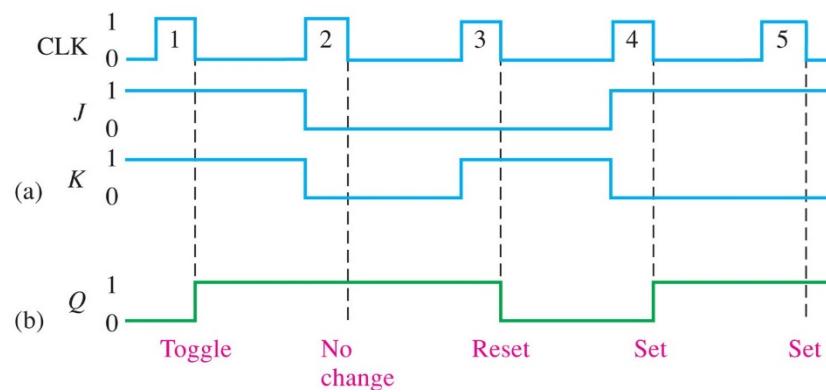
Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		Comments
J	K	CLK	Q	\bar{Q}	
0	0	↑	Q_0	\bar{Q}_0	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	\bar{Q}_0	Q_0	Toggle

↑ = clock transition LOW to HIGH
 Q_0 = output level prior to clock transition

□ The J and K inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse.

EXAMPLE 7-5 Assuming that the flip-flop is initially RESET



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A Closer Look at J-K Flip-Flop

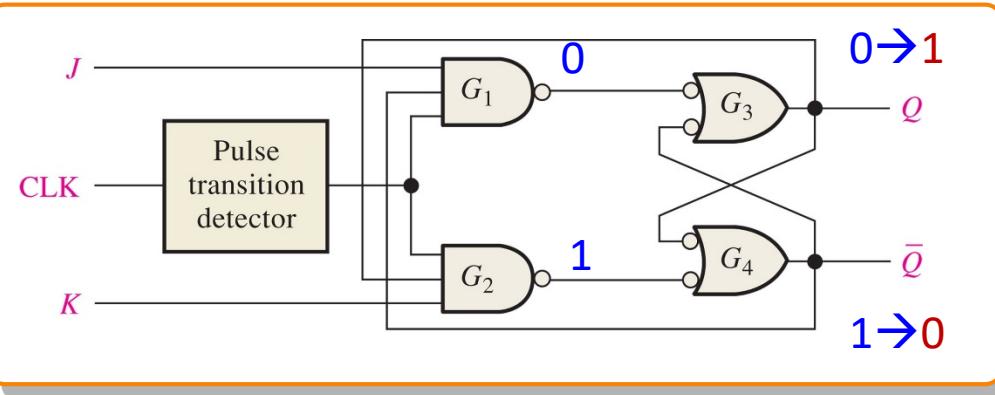


TABLE 7-3

Truth table for a positive edge-triggered J-K flip-flop.

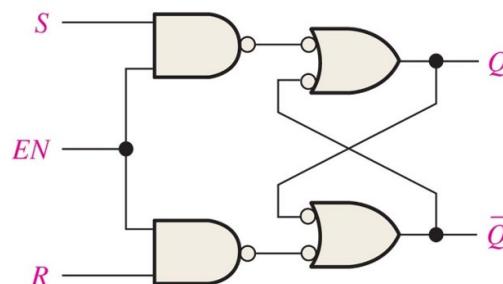
Inputs			Outputs		Comments
J	K	CLK	Q	\bar{Q}	
0	0	↑	Q_0	\bar{Q}_0	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	\bar{Q}_0	Q_0	Toggle

↑ = clock transition LOW to HIGH

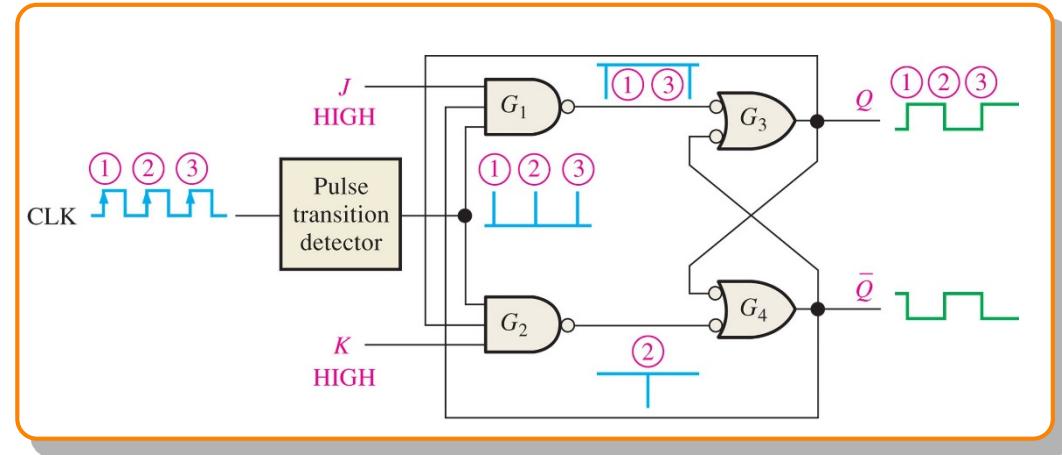
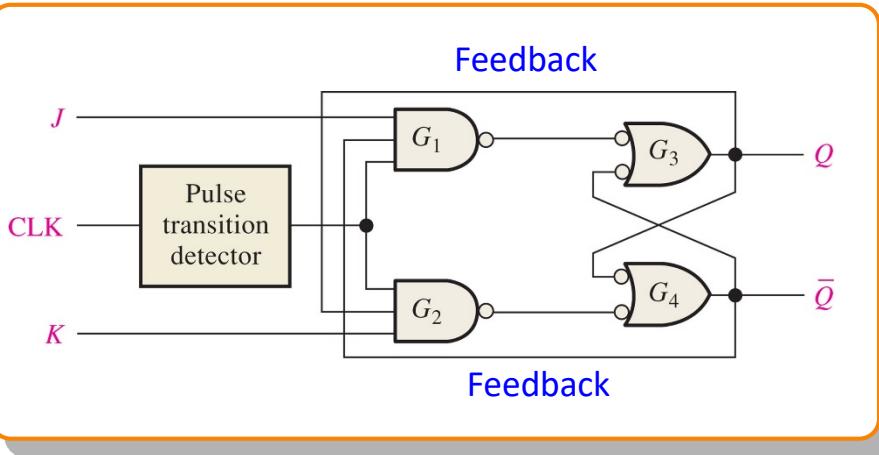
Q_0 = output level prior to clock transition

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Compare
with the
Gated S-R
Latch



Edge-Triggered Operation (J-K Flip-Flop)

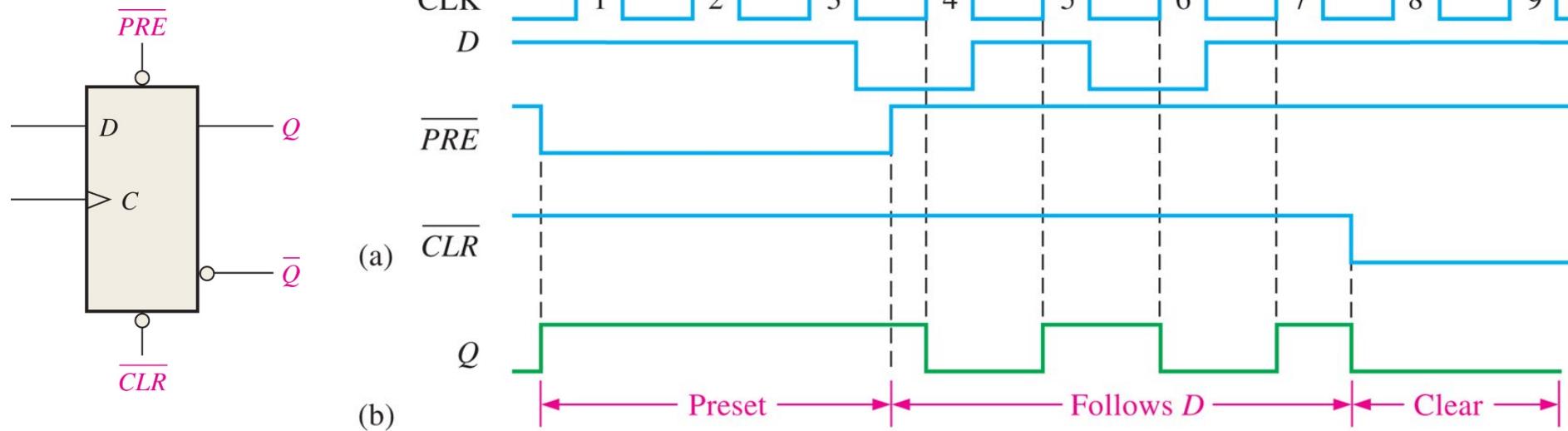
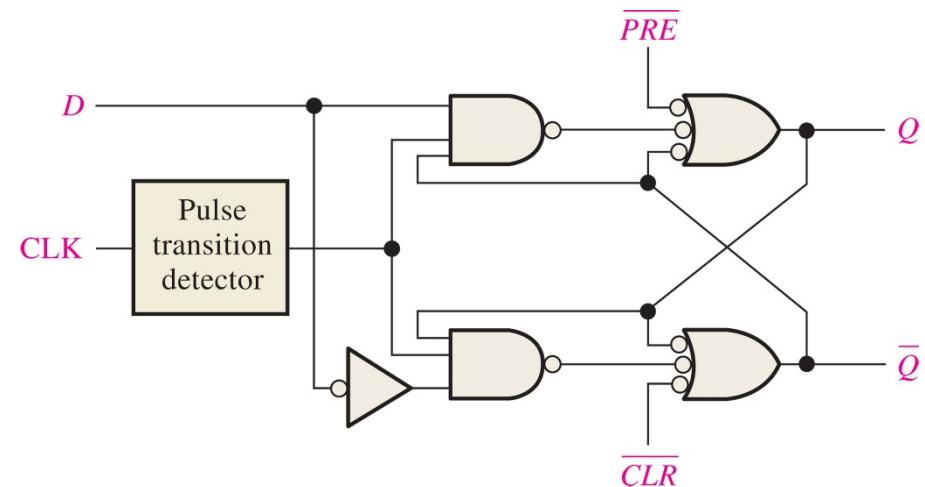


- Initial state RESET : \bar{Q} is HIGH. J and K are HIGH;
- When the clock pulse ① occurs, J and \bar{Q} are HIGH, which changes the flip-flop to the SET state, i.e. Q is HIGH;
- When the clock pulse ② passes through G_2 , (1) if J and K are HIGH, which changes the flip-flop to the RESET state, i.e. \bar{Q} is HIGH; (2) if J and K are LOW, the flip-flop will stay in its present state;
- When the clock pulse ③ occurs, if the flip-flop is in the RESET state with J and K being HIGH, then the flip-flop changes to its SET state.

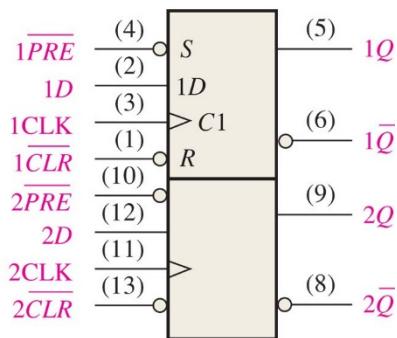
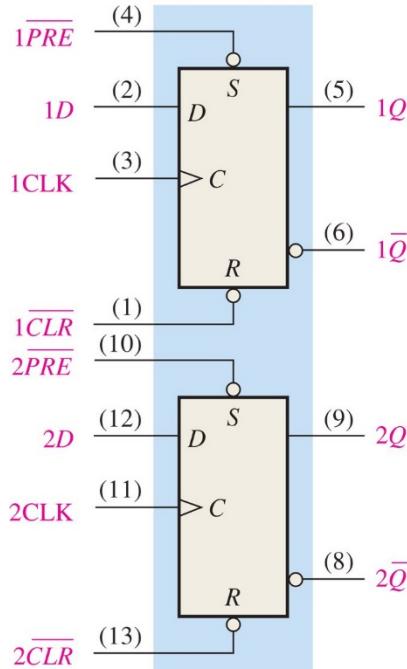


Asynchronous Preset and Clear Inputs

- Asynchronous inputs : preset (PRE) and clear (CLR)
- These inputs can override the effect of the synchronous input, D and the clock.

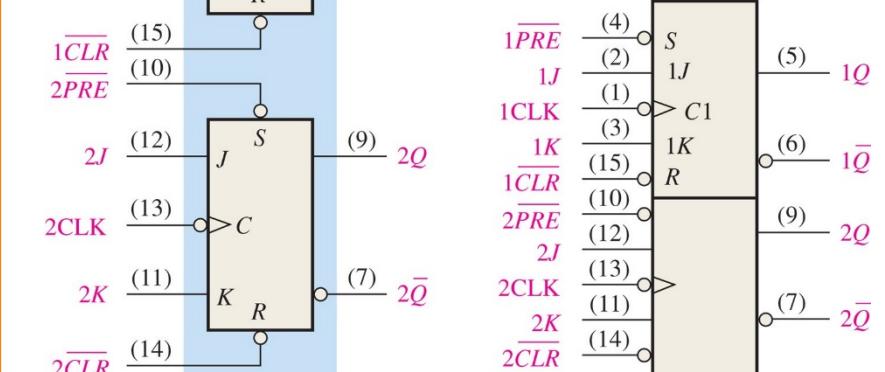
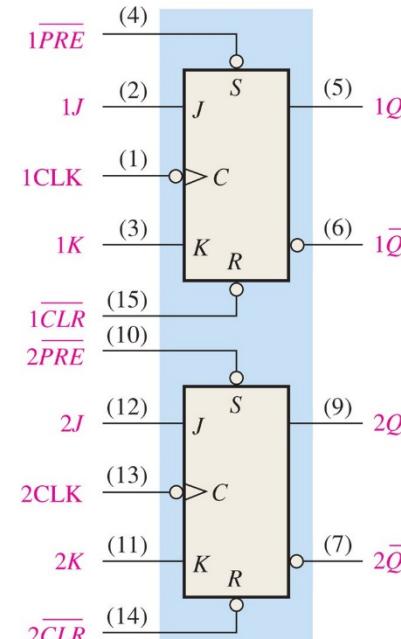


Implementation of Flip-Flops



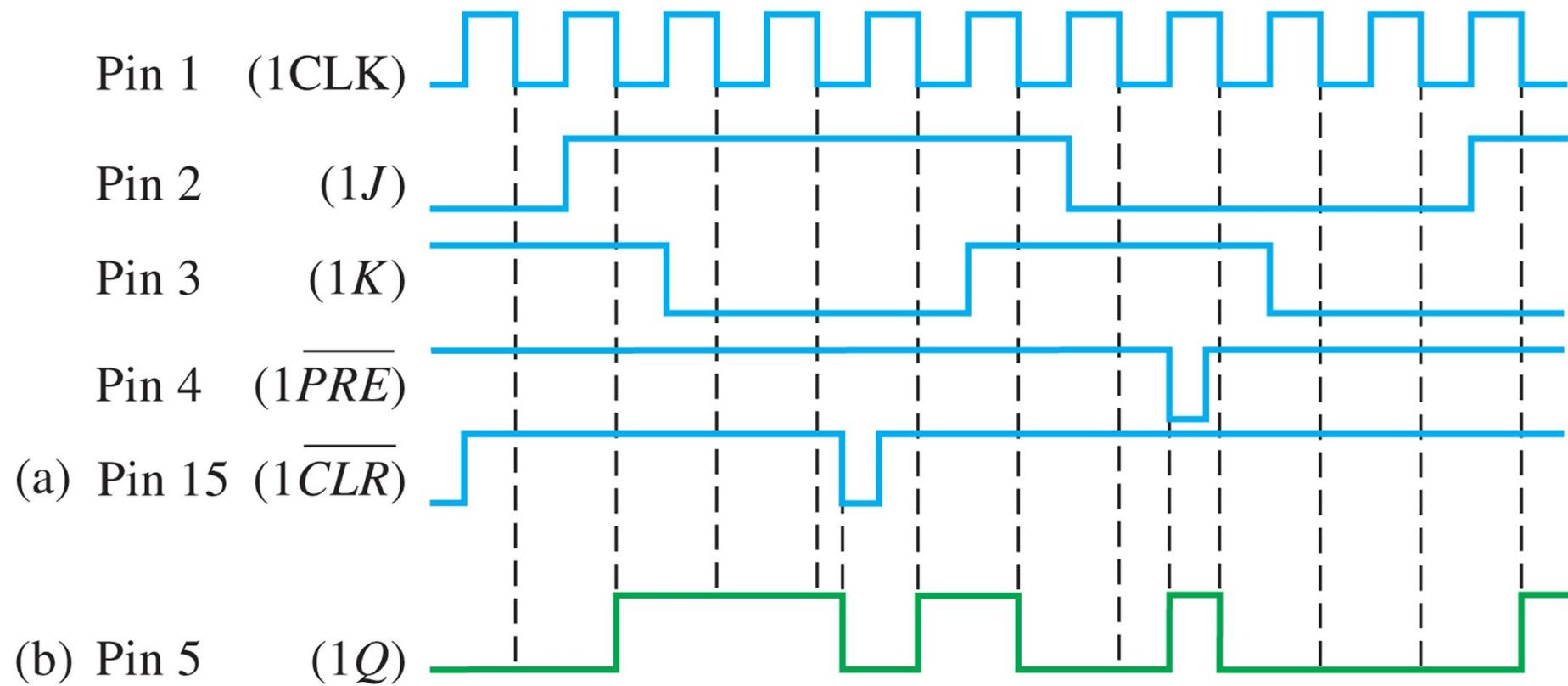
The 74HC112 dual J-K flip-flops

The 74HC74 dual D flip-flops



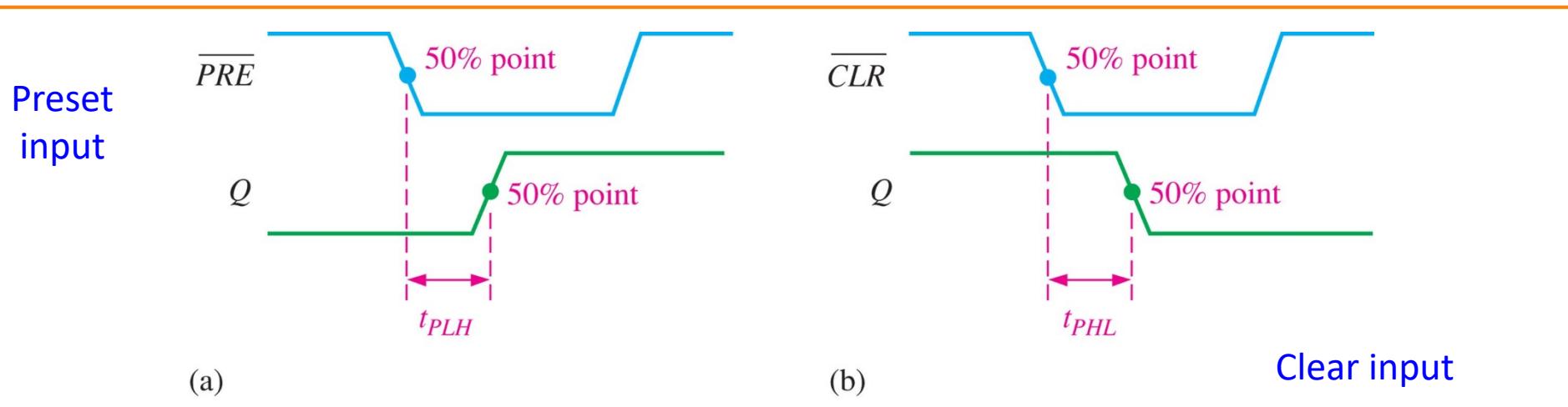
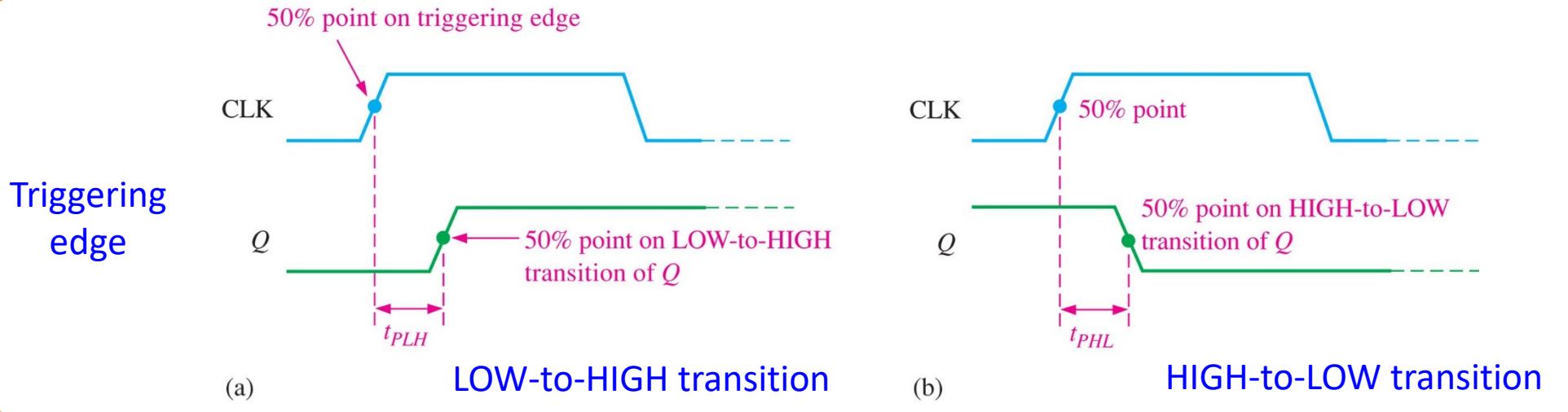
Example 7–8

- A negative edge-triggered flip-flops



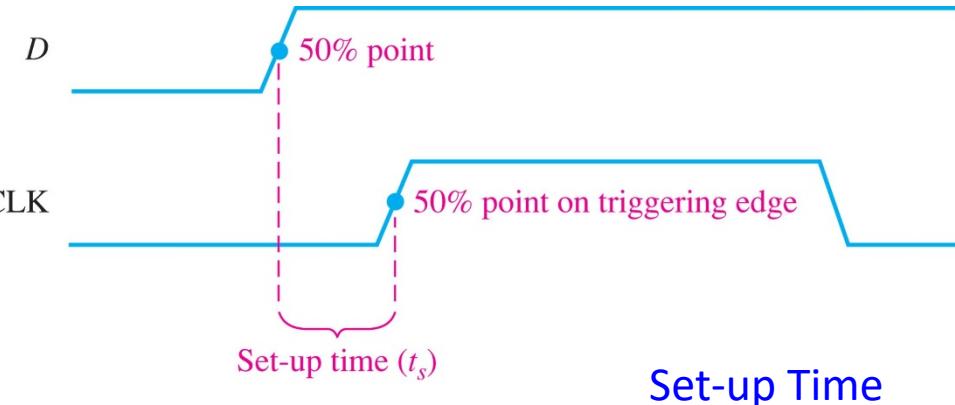
Characteristics : Propagation Delay Times

- The time interval required after an input signal has been applied for the resulting output change to occur.

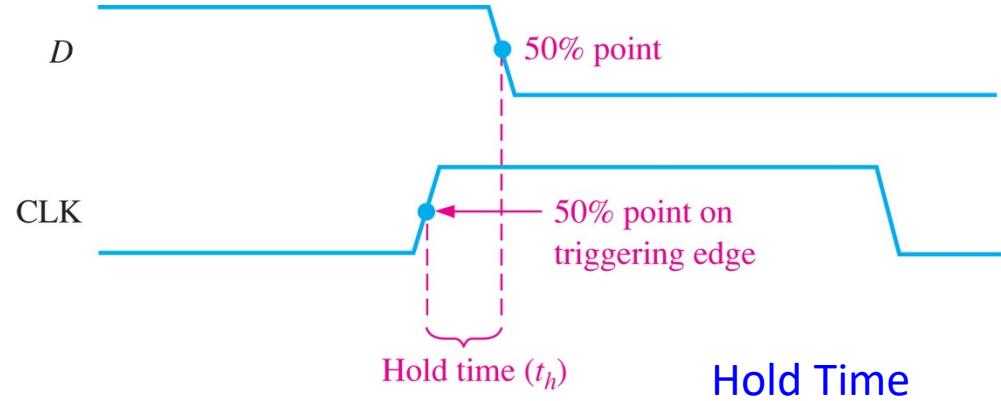


Characteristics : Set-up and Hold Time

- The min. interval required for the logic levels to be maintained constantly on the inputs (J and K, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop.



- The min. interval required for the logic levels to remain on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop.



More Characteristics

- **Maximum Clock Frequency** : the highest rate at which a flip-flop can be reliably triggered.
- **Pulse Widths** : the clock is specified by its minimum HIGH time and its minimum LOW time.

- **Power Dissipation**

$$P = V_{CC} * I_{CC}$$

TABLE 7-4

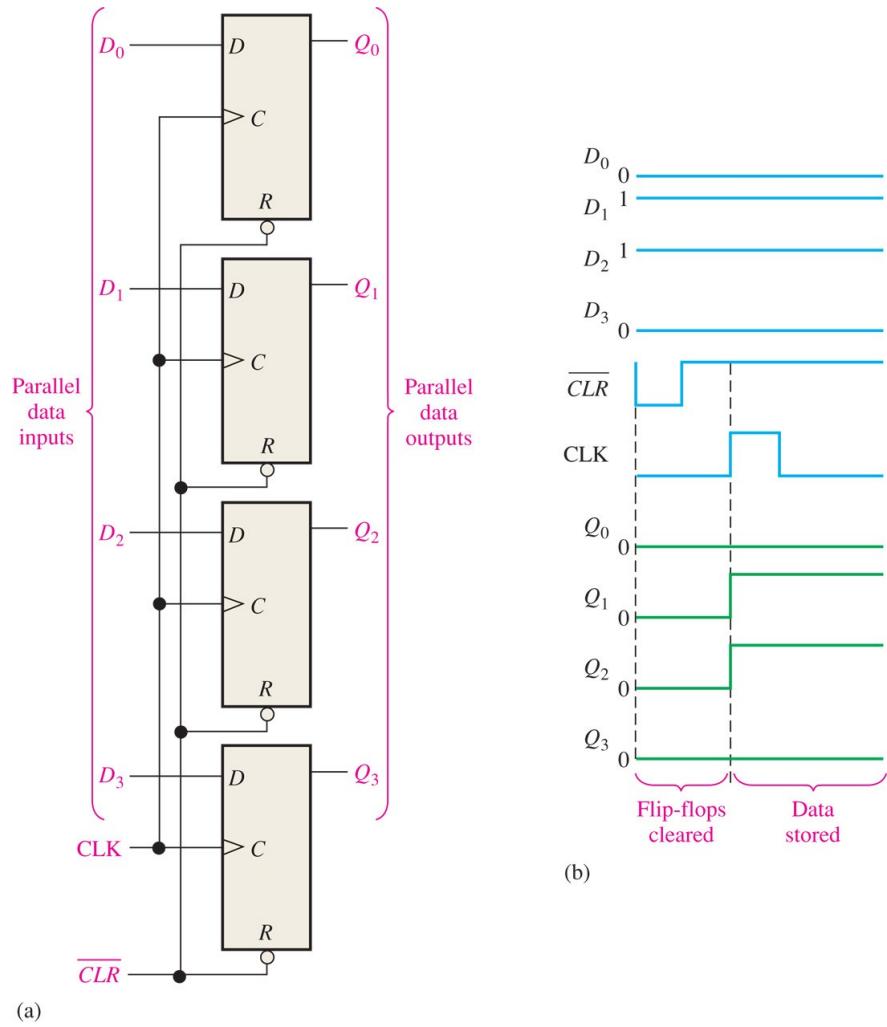
Comparison of operating parameters for four IC families of flip-flops of the same type at 25°C.

Parameter	CMOS 74HC74A	CMOS 74AHC74	Bipolar (TTL) 74LS74A	Bipolar (TTL) 74F74
t_{PHL} (CLK to Q)	17 ns	4.6 ns	40 ns	6.8 ns
t_{PLH} (CLK to Q)	17 ns	4.6 ns	25 ns	8.0 ns
$t_{PHL}(\overline{CLR}$ to Q)	18 ns	4.8 ns	40 ns	9.0 ns
$t_{PLH}(\overline{PRE}$ to Q)	18 ns	4.8 ns	25 ns	6.1 ns
t_s (set-up time)	14 ns	5.0 ns	20 ns	2.0 ns
t_h (hold time)	3.0 ns	0.5 ns	5 ns	1.0 ns
t_W (CLK HIGH)	10 ns	5.0 ns	25 ns	4.0 ns
t_W (CLK LOW)	10 ns	5.0 ns	25 ns	5.0 ns
$t_W(\overline{CLR}/\overline{PRE})$	10 ns	5.0 ns	25 ns	4.0 ns
f_{max}	35 MHz	170 MHz	25 MHz	100 MHz
Power, quiescent	0.012 mW	1.1 mW		
Power, 50% duty cycle			44 mW	88 mW

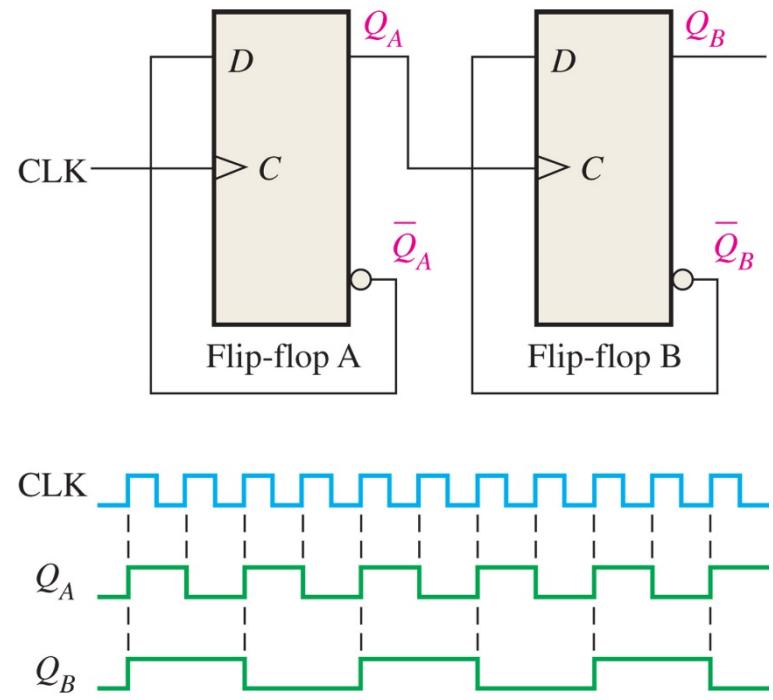


Flip-Flop Applications (I)

□ Parallel Data Storage



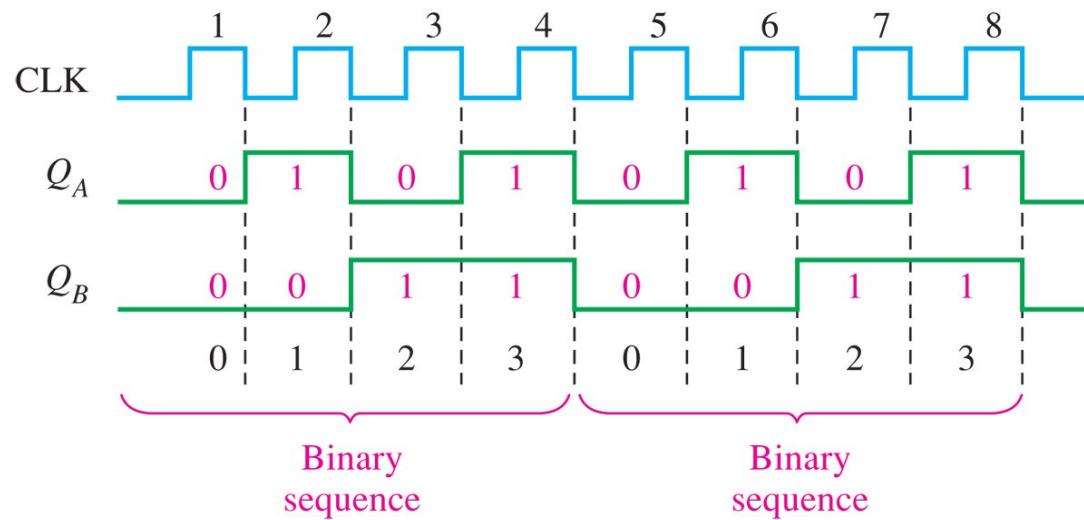
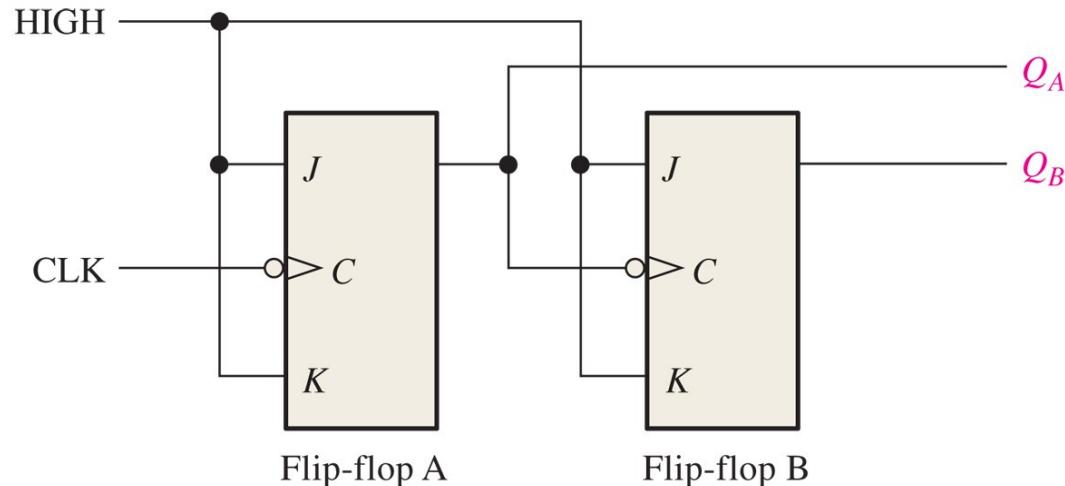
□ Frequency Division



By connecting flip-flops in this way, a frequency division of 2^n is achieved, where n is the number of flip-flops.



Flip-Flop Applications (II) : Counting

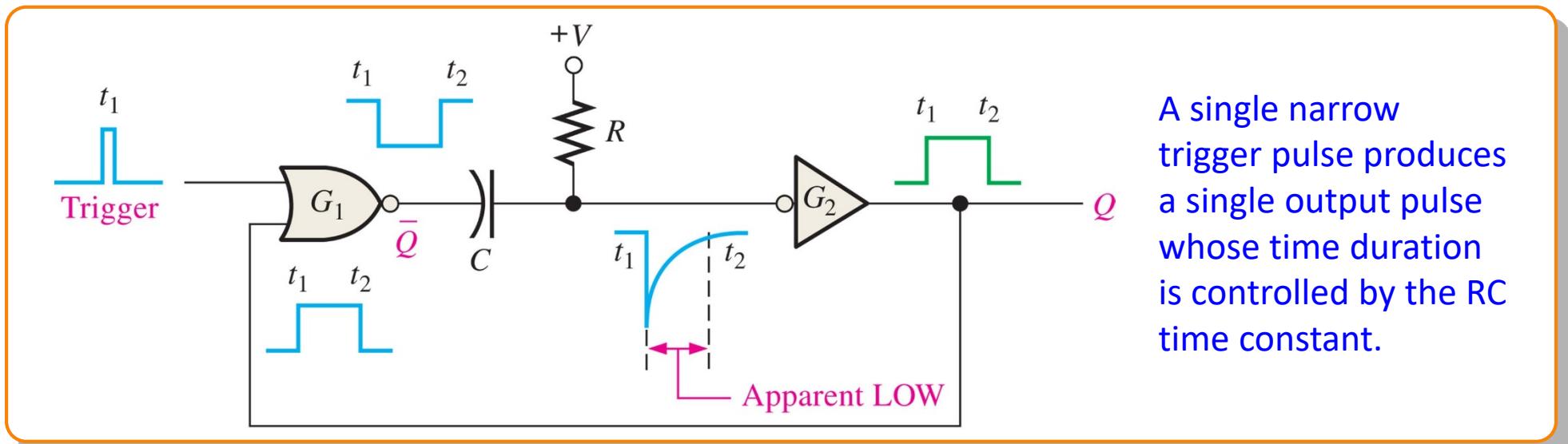


The flip-flops are counting in sequence from 0 to 3 (00, 01, 10, 11) and then recycling back to 0 to begin the sequence again.

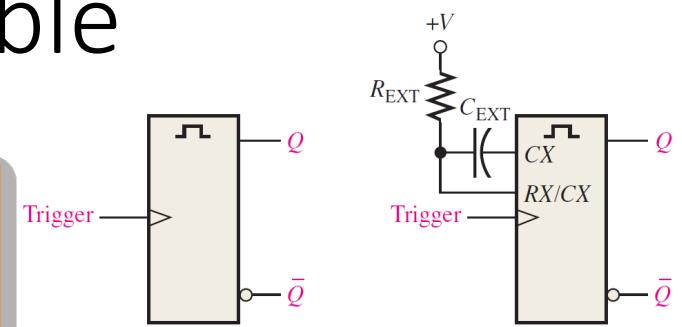
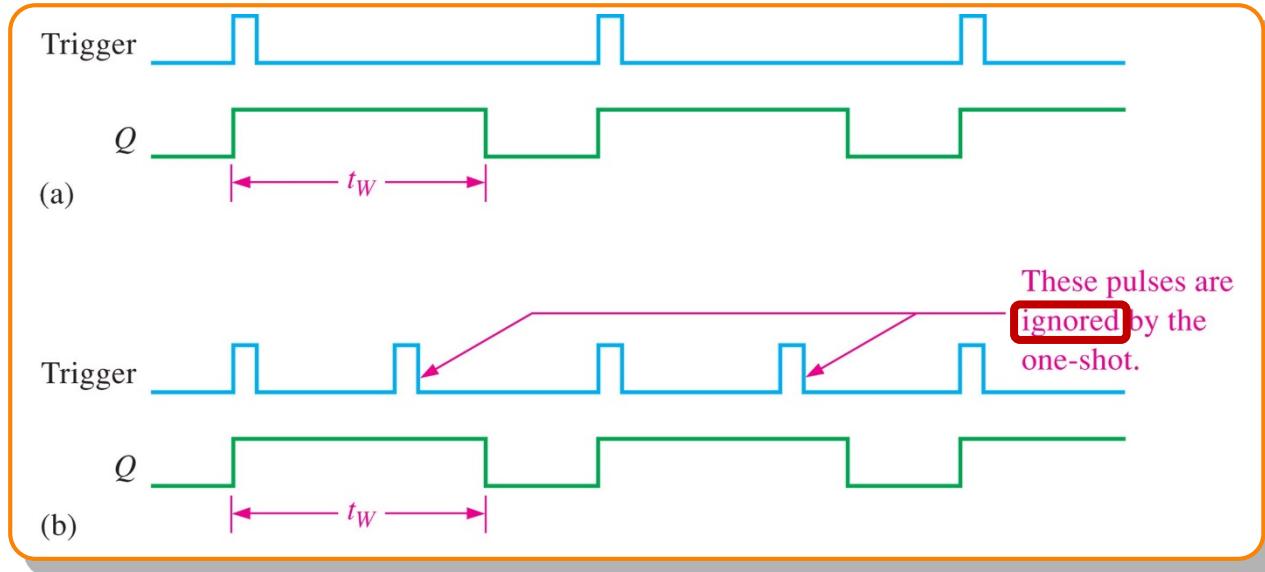


One-Shot Logics

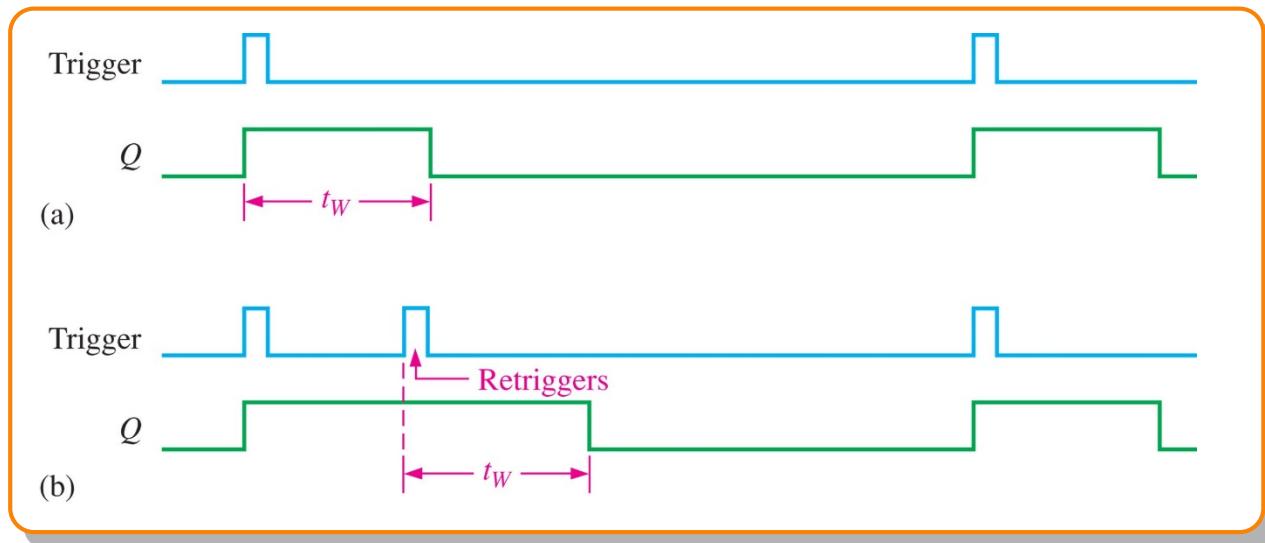
- When a pulse is applied, the output of gate G_1 goes LOW. This HIGH-to-LOW transition is coupled through the capacitor to the input of inverter G_2 . This G_2 HIGH output is connected back into G_1 , keeping its output LOW.
- The capacitor immediately begins to charge through R toward the high voltage level. The rate at which it charges is determined by the RC time constant. When the capacitor charges to a certain level, which appears as a HIGH to G_2 , the output goes back LOW.



Nonretriggerable & Retriggerable



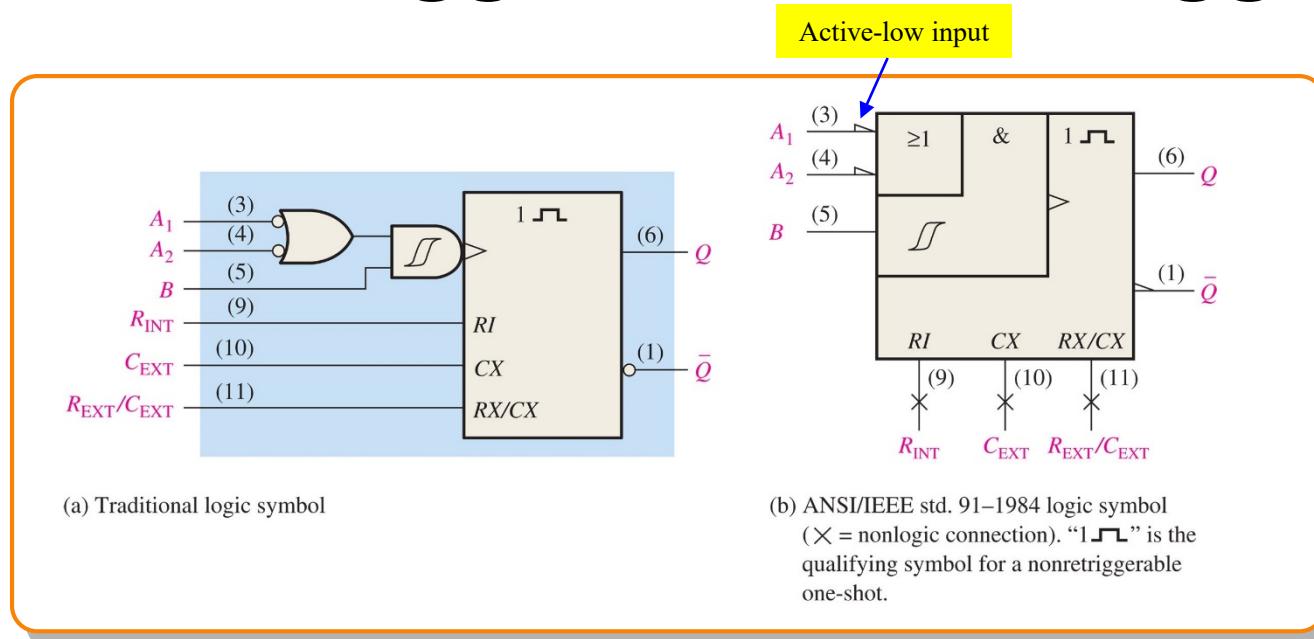
Nonretriggerable
one-shot action



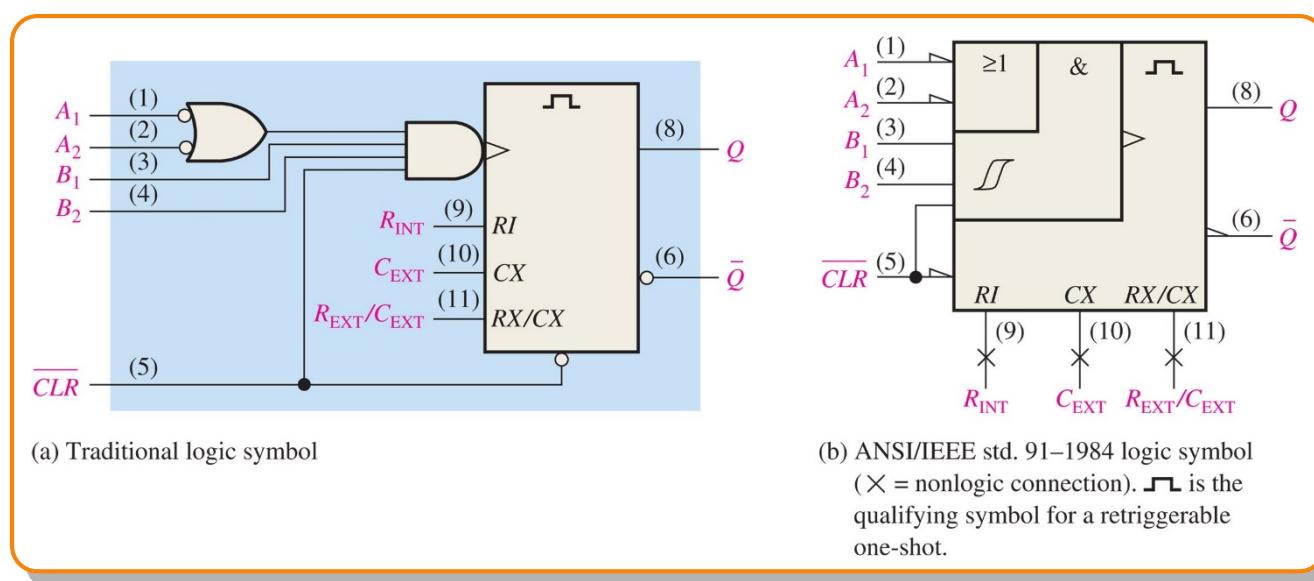
Retriggerable
one-shot action



Nonretriggerable & Retriggerable IC's



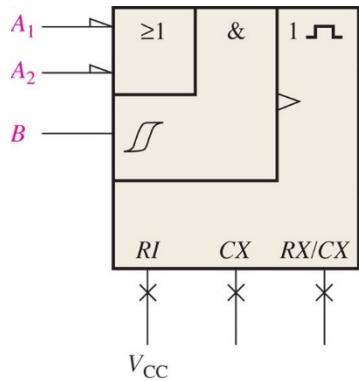
The 74121 is an example of a **nonretriggerable IC one-shot**.



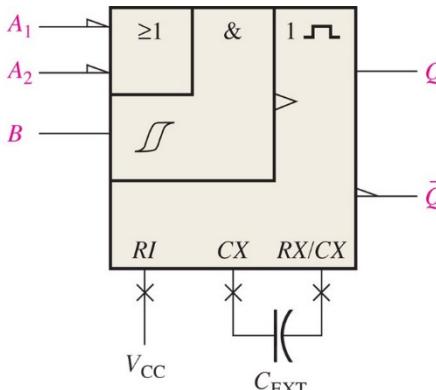
The 74LS122 is an example of a **retriggerable IC one-shot with a clear input**



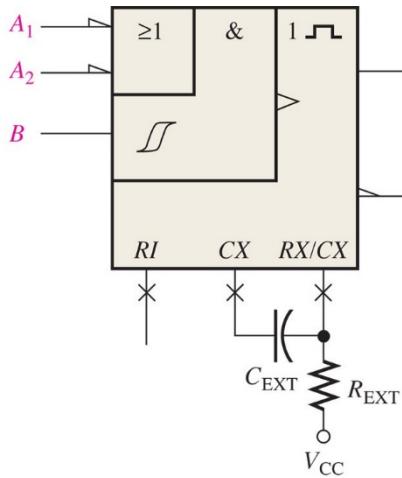
Setting the Pulse Width



(a) No external components
 R_{INT} to V_{CC}
 $t_W \approx 30 \text{ ns}$



(b) R_{INT} and C_{EXT}
 $t_W = 0.7(2 \text{ k}\Omega)C_{EXT}$



(c) R_{EXT} and C_{EXT}
 $t_W = 0.7R_{EXT}C_{EXT}$

Non-retriggerable

$$t_W = 0.7RC_{EXT}$$

Retriggerable $t_W = 0.32RC_{EXT} \left(1 + \frac{0.7}{R} \right)$

EXAMPLE 7–11 Using a 74121, $R_{EXT}=39\text{K}\Omega$, find the C_{EXT} to generate a one-shot with a pulse width of approximately 100 ms.

$$C_{EXT} = \frac{1 \times 10^8 \text{ ns}}{0.7(39\text{k}\Omega)} = 3.66 \times 10^{-6} \text{ pF} = 3.66 \mu\text{F}$$

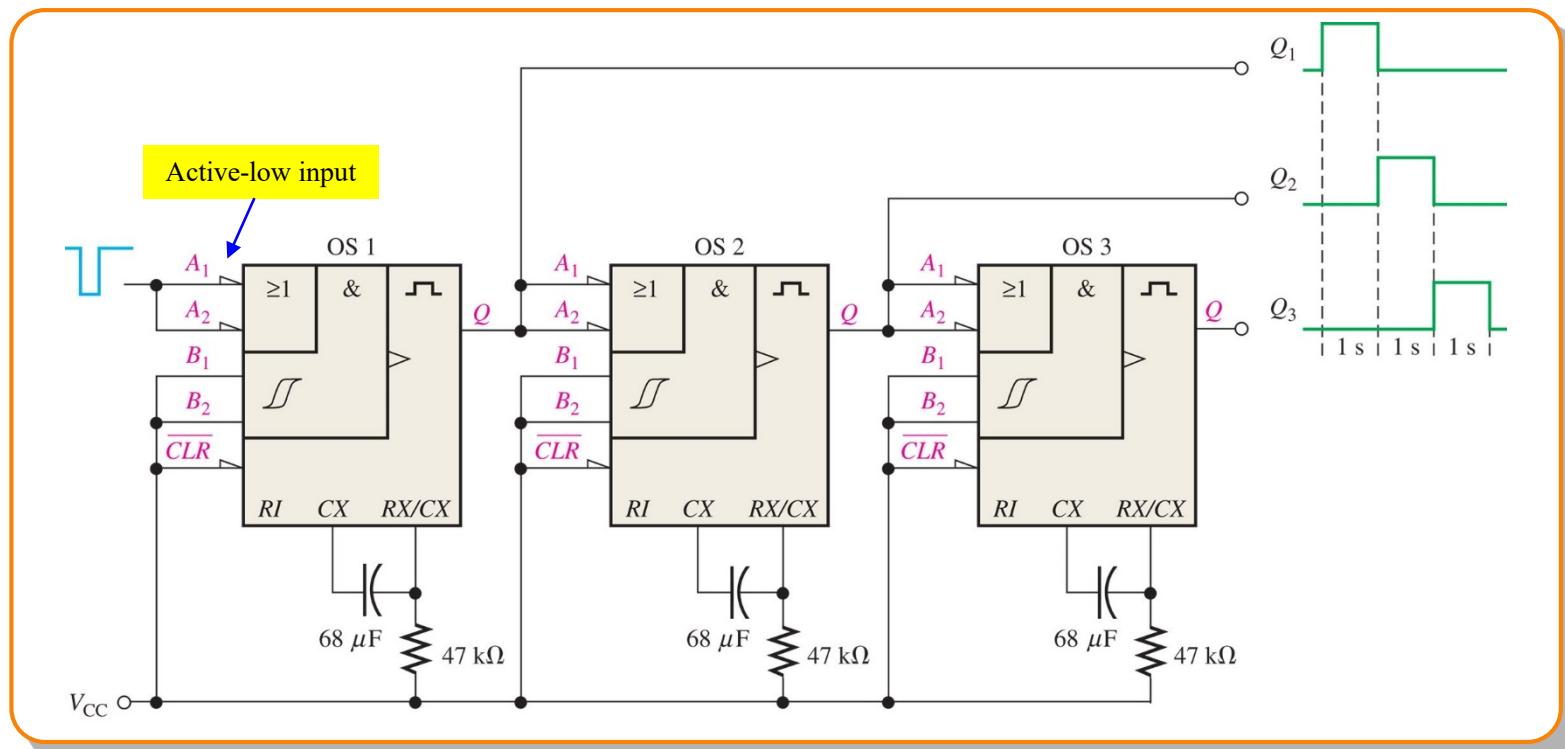
EXAMPLE 7–11 Using a 74LS122 and and $C_{EXT} = 560 \text{ pF}$, find R_{EXT} that will produce a pulse width of 1 ms

$$\begin{aligned} R_{EXT} &= \frac{t_W - (0.7)(0.32)C_{EXT}}{0.32C_{EXT}} = \frac{t_W}{0.32C_{EXT}} - 0.7 \\ &= \frac{1000\text{ns}}{(0.32)560\text{pF}} - 0.7 = 4.88\text{k}\Omega \end{aligned}$$



One-Shot Application: Sequential Timing

- The first one-shot is triggered by a switch closure, producing a 1 s output pulse.
- When the first one-shot (OS 1) times out and the 1 s pulse goes LOW, the second one-shot (OS 2) is triggered, also producing a 1 s output pulse.
- When this second pulse goes LOW, the third one-shot (OS 3) is triggered and the third 1 s pulse is produced.



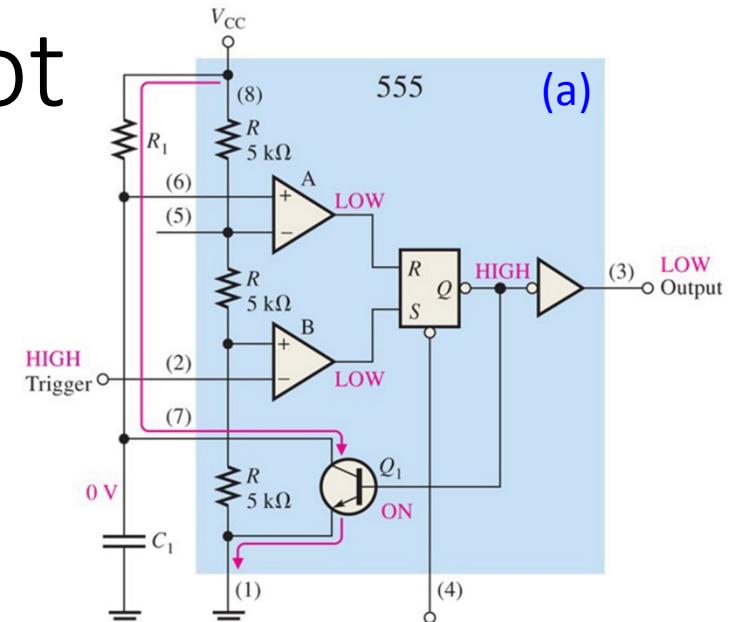
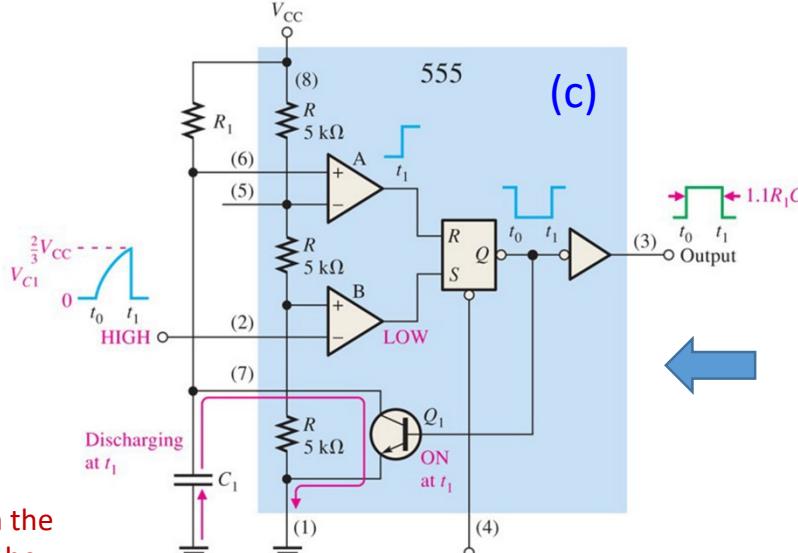
The 555 Timer as a One-Shot

- a. Before a trigger pulse is applied, the output is LOW and the discharge transistor Q_1 is on, keeping C_1 discharged;
- b. When a negative-going trigger pulse is applied at t_0 , the output goes HIGH and the discharge transistor turns off, allowing capacitor C_1 to begin charging through R_1 ;
- c. When C_1 charges to $\frac{2}{3} V_{CC}$, the output goes back LOW at t_1 and Q_1 turns on immediately, discharging C_1 ;

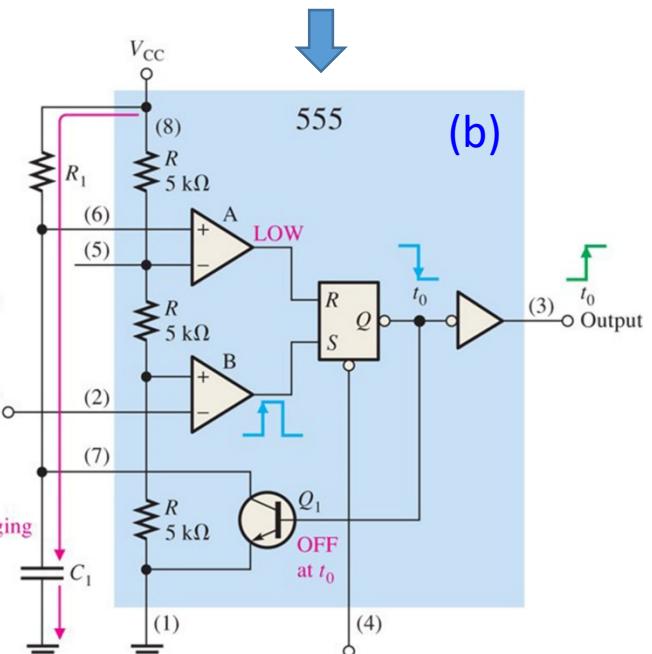
As you can see, the charging rate of C_1 determines how long the output is HIGH.

Comparators outputs HIGH when the positive (+) input is greater than the negative (-) input

(c) At end of charging interval



(a) Prior to triggering. (The current path is indicated by the red arrow.)



(b) When triggered



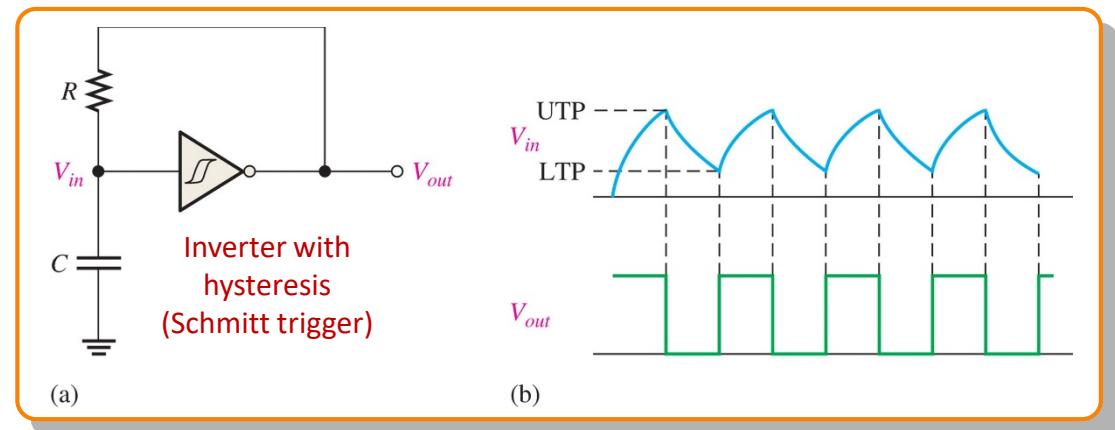
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The Chinese University of Hong Kong, Shenzhen

The Astable Multivibrator

- An astable multivibrator is a device that has no stable states; it changes back and forth (oscillates) between two unstable states without any external triggering.
- Its output is typically a square wave that is used as a clock signal in many types of sequential logic circuits. Astable multivibrators are also known as pulse oscillators.

- When power is first applied, the capacitor has no charge; so the input to the inverter is LOW and the output is HIGH;



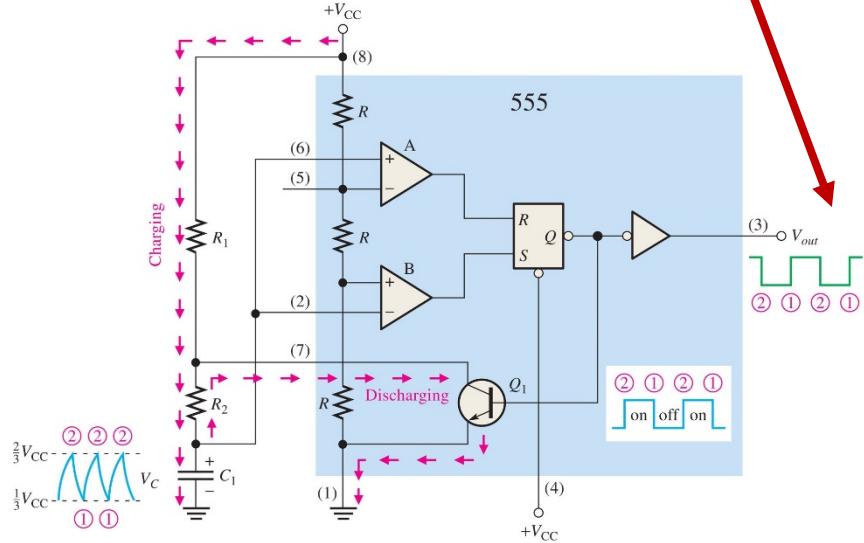
- The capacitor charges through R until the inverter input voltage reaches **the upper trigger point (UTP)**. At this point, the inverter output goes LOW, causing the capacitor to discharge back through R;
- When the inverter input voltage decreases to **the lower trigger point (LTP)**, its output goes HIGH and the capacitor charges again.



The 555 Timer as an Astable Multivibrator

- Initially, when the power is turned on, the capacitor (C_1) is uncharged and thus the trigger voltage is at 0 V. This causes the output of **comparator B** to be **HIGH** and the output of **comparator A** to be **LOW**, forcing the base of Q_1 , **LOW** and keeping the transistor off. Now, C_1 begins **charging** via R_1 and R_2 ;

Resulting a rectangular wave output whose duty cycle depends on the values of R_1 and R_2 .



- When the capacitor voltage reaches $1/3 V_{CC}$, **comparator B outputs LOW**; and when the capacitor voltage reaches $2/3 V_{CC}$, **comparator A outputs HIGH**; (**SET** \rightarrow **RESET**, output **HIGH** \rightarrow **LOW**)
- Resetting the latch turns on the transistor Q_1 , which creates a **discharge** path for the capacitor through R_2 and the transistor. The capacitor now begins to discharge, causing **comparator A to go LOW**. At the point where the capacitor discharges down to $1/3 V_{CC}$, **comparator B switches HIGH**; this sets the latch, making the base of Q_1 **LOW** and turning off the transistor. (**RESET** \rightarrow **SET**, output **LOW** \rightarrow **HIGH**)



Frequency of Oscillation

- The oscillation frequency of the output rectangular wave is given by

$$f = \frac{1.44}{(R_1 + 2R_2)C_1}$$

- The duty cycle can be adjusted using R_1 and R_2

$$\text{Duty cycle} = \frac{t_H}{T} = \frac{t_H}{t_H+t_L}$$

$$\text{Duty cycle} = \left(\frac{R_1+R_2}{R_1+2R_2} \right) 100\% \quad \text{\~{}50\% if } R_2 \gg R_1$$

with $t_L = 0.7R_2C_1$ and $t_H = 0.7(R_1 + R_2)C_1$

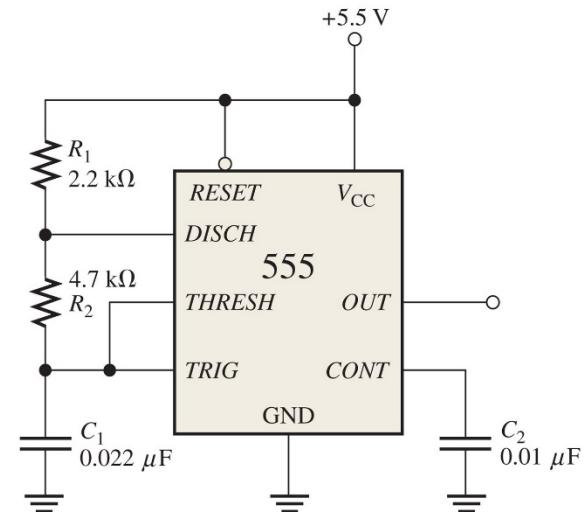
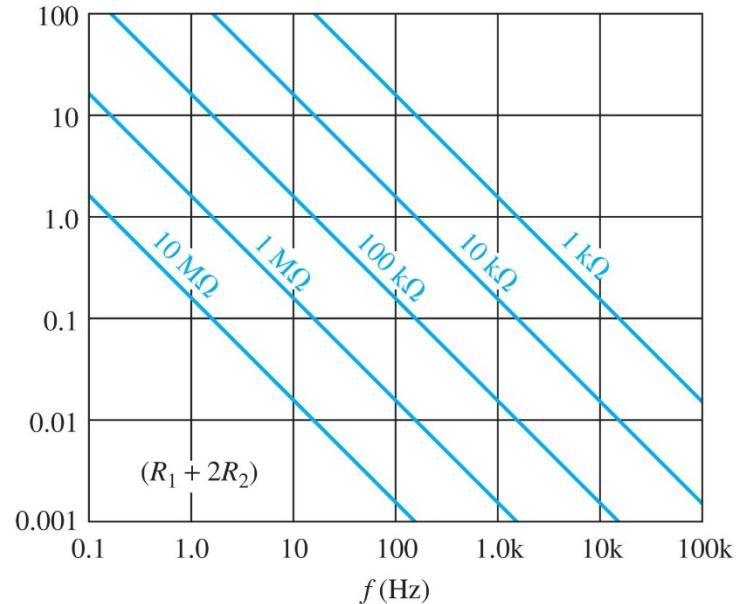
Output LOW
Time to **discharge** C_1 from $2/3 V_{CC}$ to $1/3 V_{CC}$

Output HIGH
Time to **charge** C_1 from $1/3 V_{CC}$ to $2/3 V_{CC}$

- Example 7-14

$$f = \frac{1.44}{(R_1 + 2R_2)C_1} = \frac{1.44}{(2.2k\Omega + 9.4k\Omega)0.022\mu F} = 5.64\text{kHz}$$

$$\text{Duty cycle} = \left(\frac{R_1 + R_2}{R_1 + 2R_2} \right) 100\% = \left(\frac{2.2k\Omega + 4.7k\Omega}{2.2k\Omega + 9.4k\Omega} \right) 100\% = 59.5\%$$

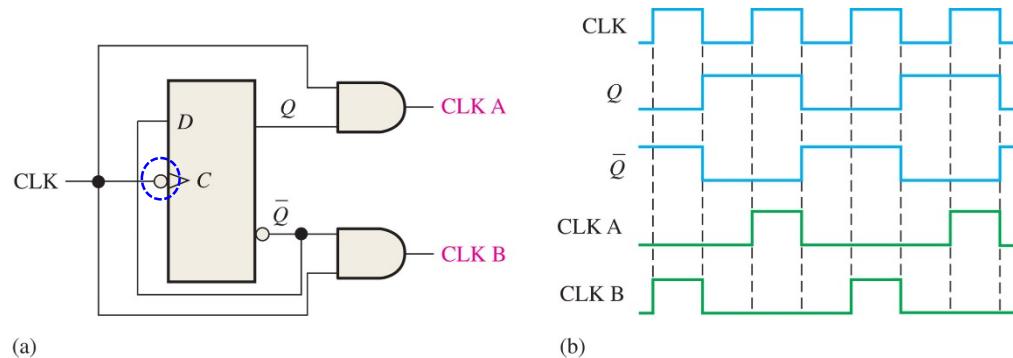
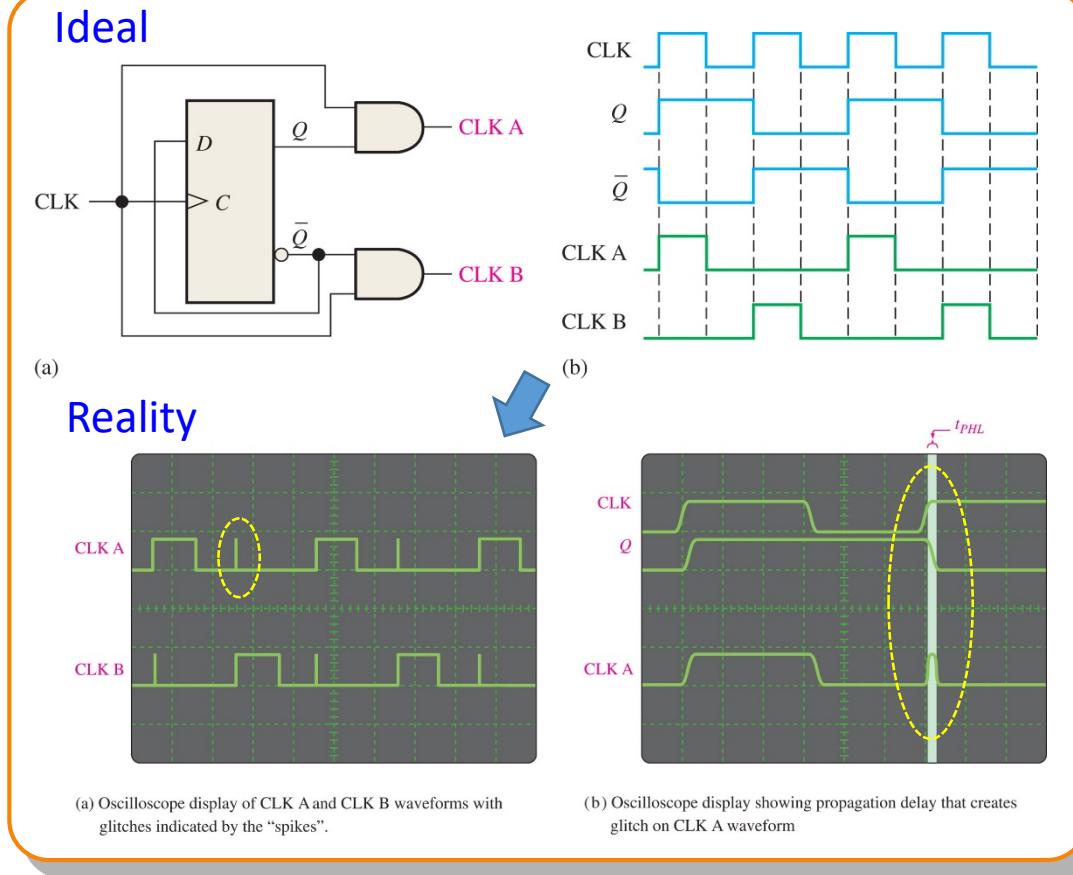


Troubleshooting

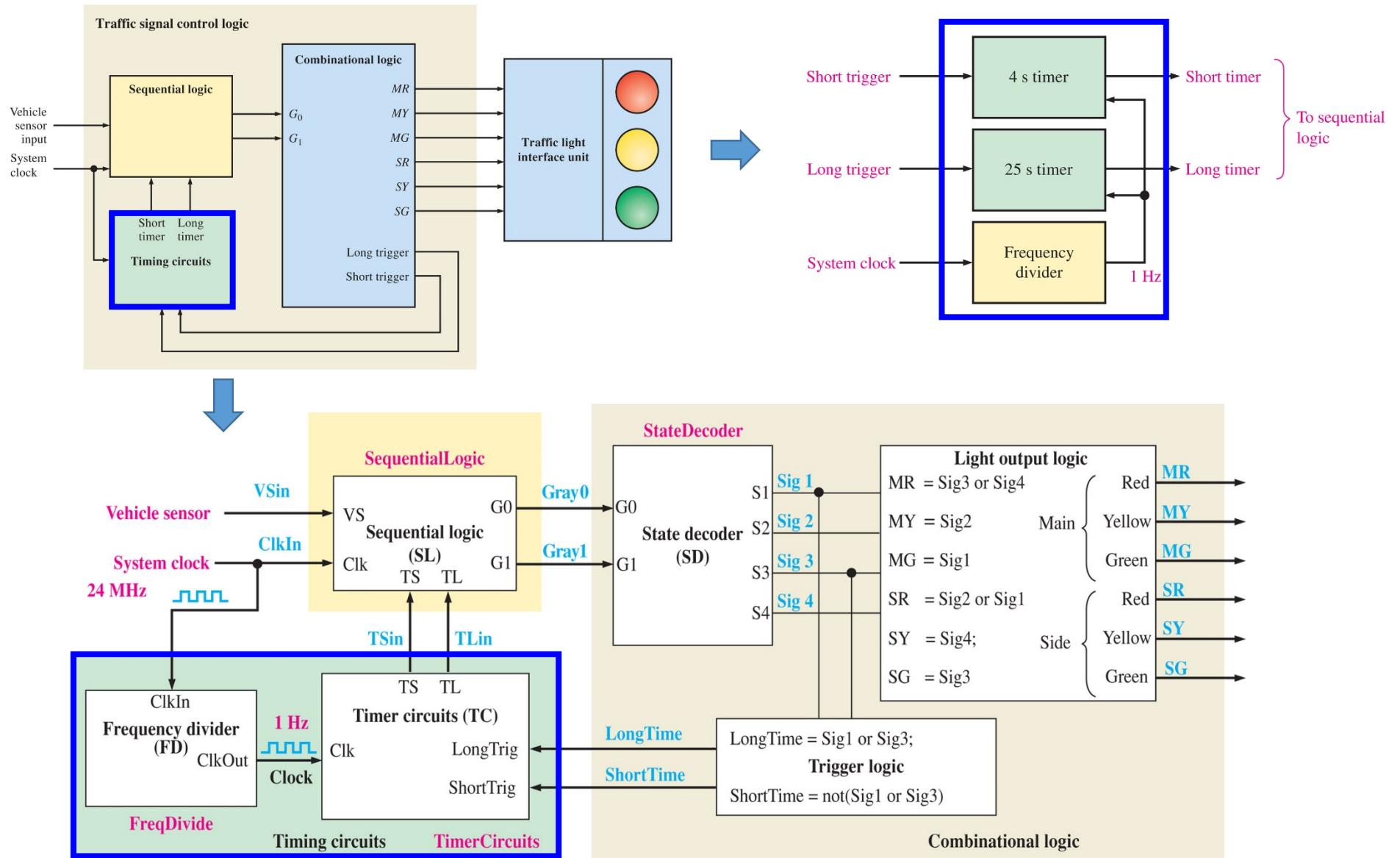
- When the circuit is tested, glitches occur on both CLK A and CLK B waveforms, which is caused by a race condition between the CLK signal and the Q and \bar{Q} signals at the inputs of the AND gates.

- The propagation delays between CLK and Q and \bar{Q} create a short-duration coincidence of HIGH levels at the leading edges of alternate clock pulses.

- THIS** problem can be corrected by using a **negative** edge-triggered flip-flop in place of the positive edge-triggered device **(CLK earlier than Q)**



Traffic Signal Controller: Part 2



The Sequential Logic

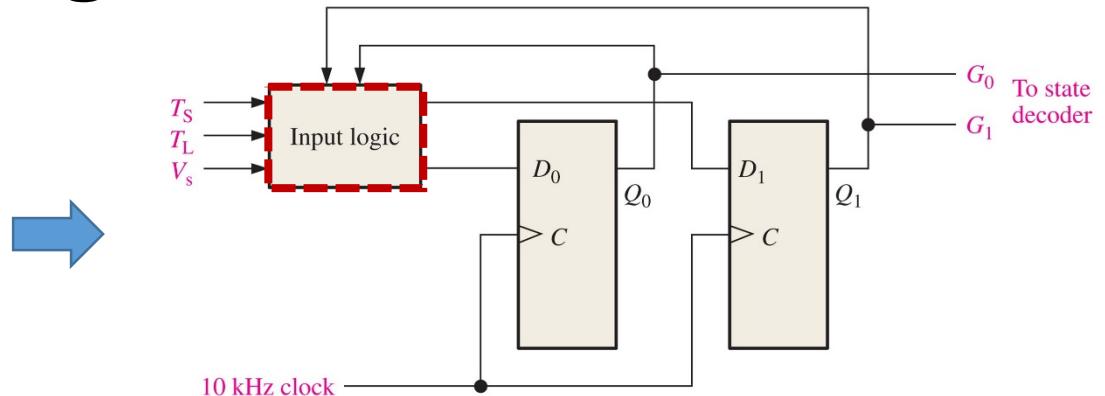
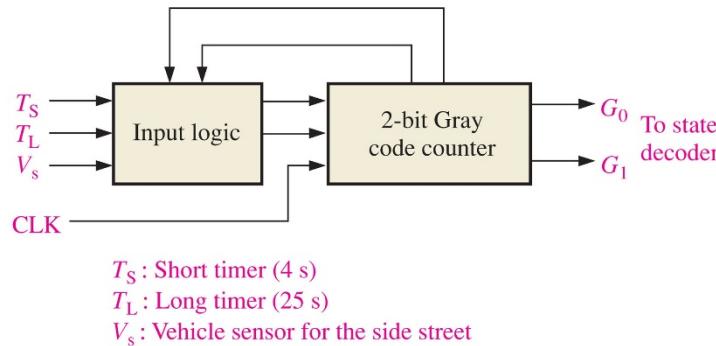


TABLE 7-5

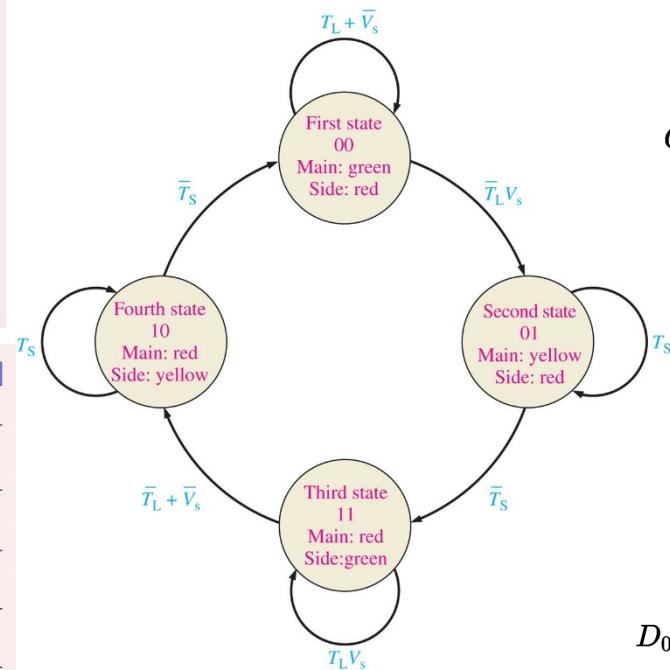
D flip-flop transition table. Q_N is the output before clock pulse. Q_{N+1} is output after clock pulse.

Output Transitions		Flip-Flop Input
Q_N	Q_{N+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

TABLE 7-6

Next-state table for the counter.

Present State Q_1 Q_0	Next State Q_1 Q_0	Input Conditions	FF Inputs D_1 D_0
0 0	0 0	$\bar{T}_S + \bar{V}_s$	0 0
0 0	0 1	$\bar{T}_L V_s$	0 1
0 1	0 1	T_S	0 1
0 1	1 1	\bar{T}_S	1 1
1 1	1 1	$T_L V_s$	1 1
1 1	1 0	$\bar{T}_L + \bar{V}_s$	1 0
1 0	1 0	T_S	1 0
1 0	0 0	\bar{T}_S	0 0



$T_L V_s$	00	01	11	10
$Q_1 Q_0$	00	1		
	1	1	1	1
			1	
				10

$$\begin{aligned}
 D_0 &= \bar{Q}_1 \bar{Q}_0 \bar{T}_L V_s + \bar{Q}_1 Q_0 T_S + \bar{Q}_1 Q_0 \bar{T}_S + Q_1 Q_0 T_L V_s \\
 &= \bar{Q}_1 Q_0 + \bar{T}_L V_s \bar{Q}_1 + T_L V_s Q_0
 \end{aligned}$$

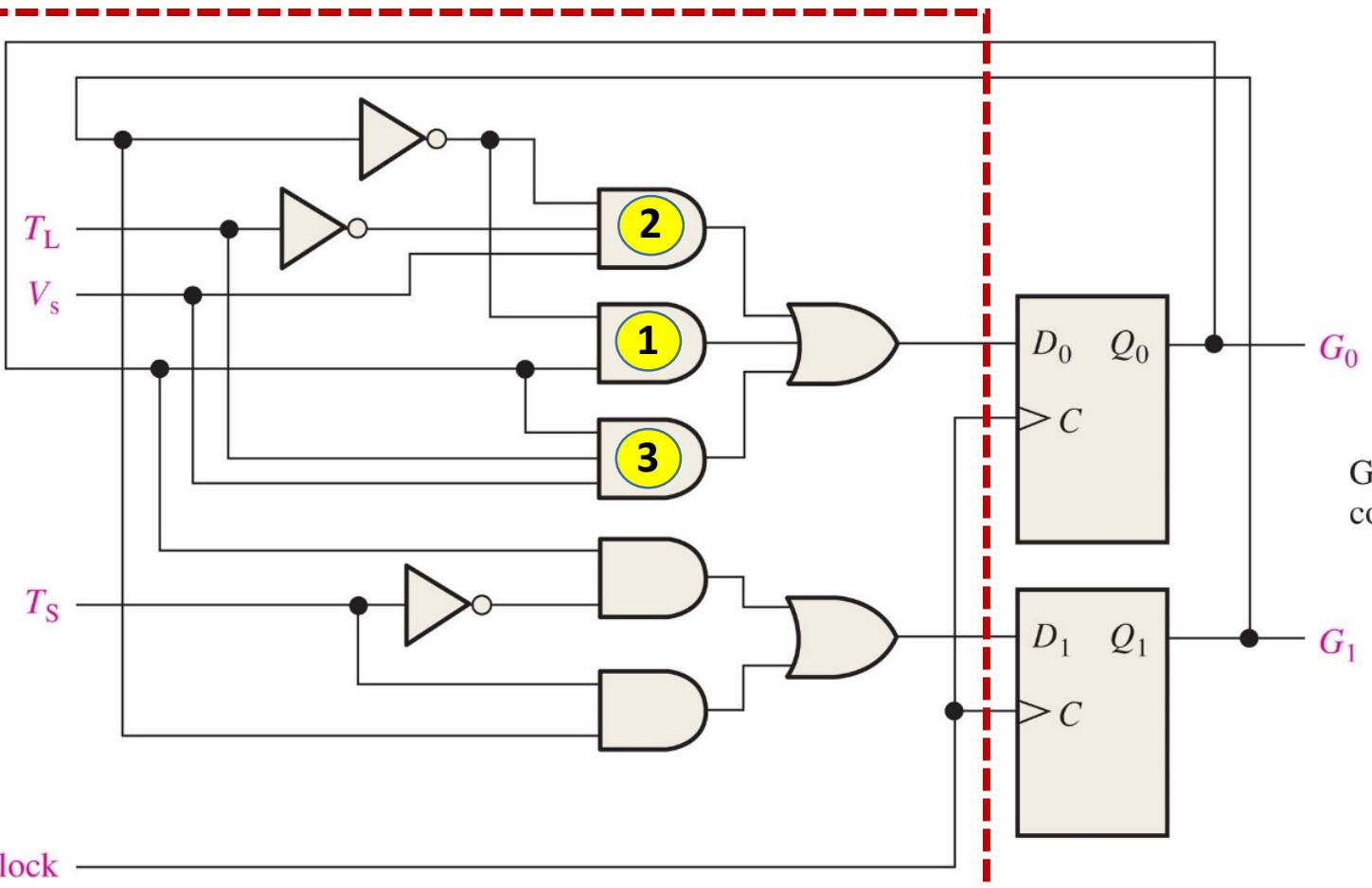


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Implementation

$$\overline{Q}_1 Q_0 + \overline{T}_L V_s \overline{Q}_1 + T_L V_s Q_0$$



Chapter Review

□ Latches

- ◆ Temp. storage devices with two stable states : SET (Q HIGH) & RESET : \bar{Q} HIGH
- ◆ Gated latches : Gated S-R latches, Gated D latches

□ Flip-Flops

- ◆ Bistable devices whose output synchronously changes at the rising/positive or falling/negative edge of the CLK : D Flip-Flop and J-K Flip-Flop
- ◆ Asynchronous Preset and Clear Inputs; Applications: Counting

□ Flip-Flop Operating Characteristics

- ◆ Prop. Delay/Set-up/Hold times, Max. clock freq., Pulse widths & Power dissipation

□ One-Shots (555 Timers)

- ◆ Devices with only one stable state : when triggered, remains in its unstable state for a predetermined length of time before automatically returning to its stable state.

□ The Astable Multivibrator

- ◆ Oscillates % two unstable states without any external triggering.



True/False Quiz

- A latch has one stable state.
- A latch is considered to be in the RESET state when the Q output is low.
- A gated D latch cannot be used to change state.
- Flip-flops and latches are both bistable devices.
- An edge-triggered D flip-flop changes state whenever the D input changes.
- A clock input is necessary for an edge-triggered flip-flop.
- When both the J and K inputs are HIGH, an edge-triggered J-K flip-flop changes state on each clock pulse.
- A one-shot is also known as an astable multivibrator.
- When triggered, a one-shot produces a single pulse.
- The 555 timer cannot be used as a pulse oscillator.



True/False Quiz

- A latch has one stable state.
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