

EIE 2050 Digital Logic and Systems

Chapter 9 : Counters

Simon Pun, Ph.D.



Last Week

□ Shift Registers

- ◆ Data storage
- ◆ Data movement
- ◆ Serial/Parallel In - Serial/Parallel Out

□ Counters

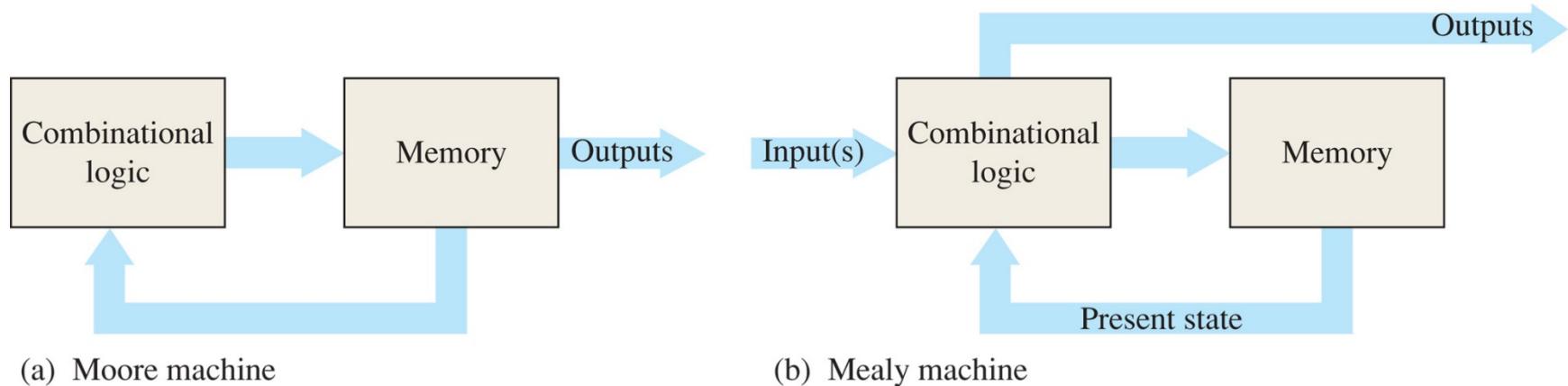
- ◆ Johnson counters
- ◆ Ring Counters

□ Shift Register Applications

- ◆ Time Delay
- ◆ Serial-to-Parallel Data Converter
- ◆ UART (Universal Asynchronous Receiver Transmitter)
- ◆ Keyboard Encoder



General Models of Finite State Machines

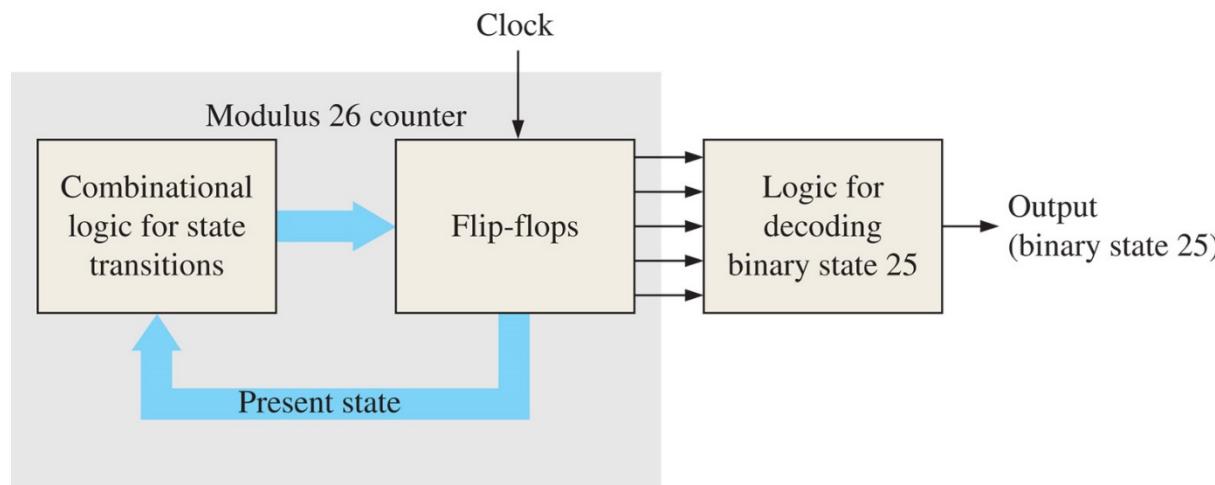


- Based on the input-output relationship
 - ◆ **Moore** machine : The outputs come directly from the memory. No external inputs!
 - ◆ **Mealy** machine : Both the present state and the external input affect the outputs
- Based on the existence of a common clock
 - ◆ **Asynchronous** versus **Synchronous**

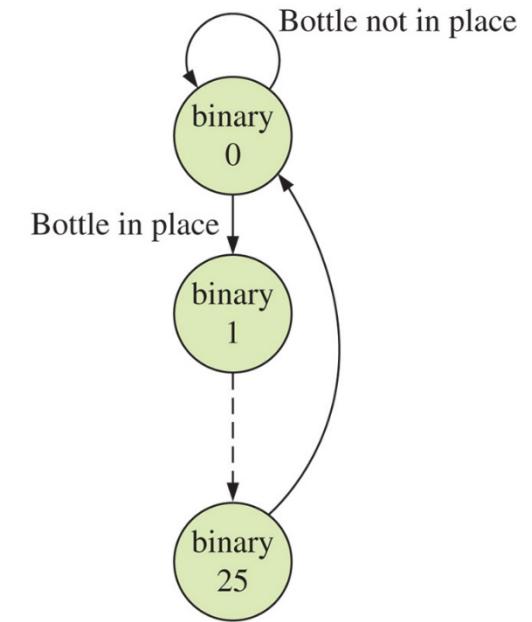


Example of a Moore Machine

- A Moore machine controls the number of tablets (25) that go into each bottle in an assembly line;
- A modulus-26 binary counter with states 0 through 25



(a) Moore machine



(b) State diagram



Example of a Mealy Machine

- A Mealy machine controls the number of tablets that go into each bottle with three different sizes of bottles: 25/50/100 tablets.
- A binary counter with 3 different terminal counts: 25, 50, and 100.

Modulus-select inputs
25 50 100

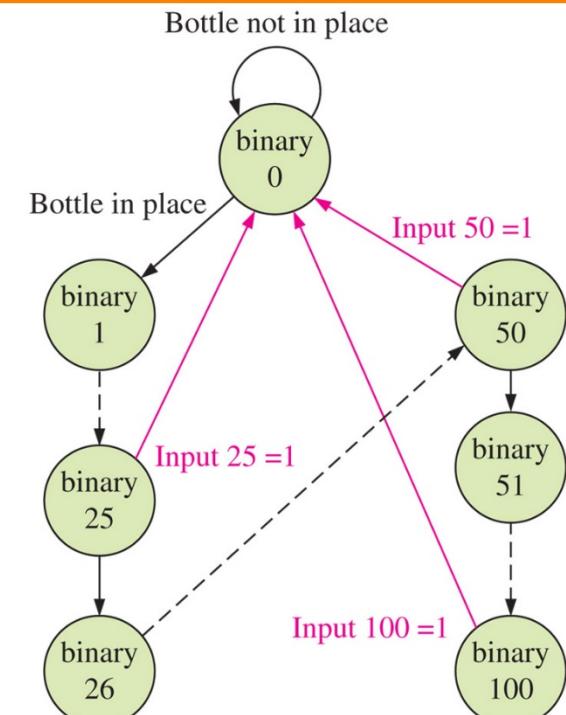
Combinational logic for the state transitions

Flip-flops

Combinational logic for decoding count
25 or 50 or 100

Output (final state)

(a) Mealy machine



(b) State diagram

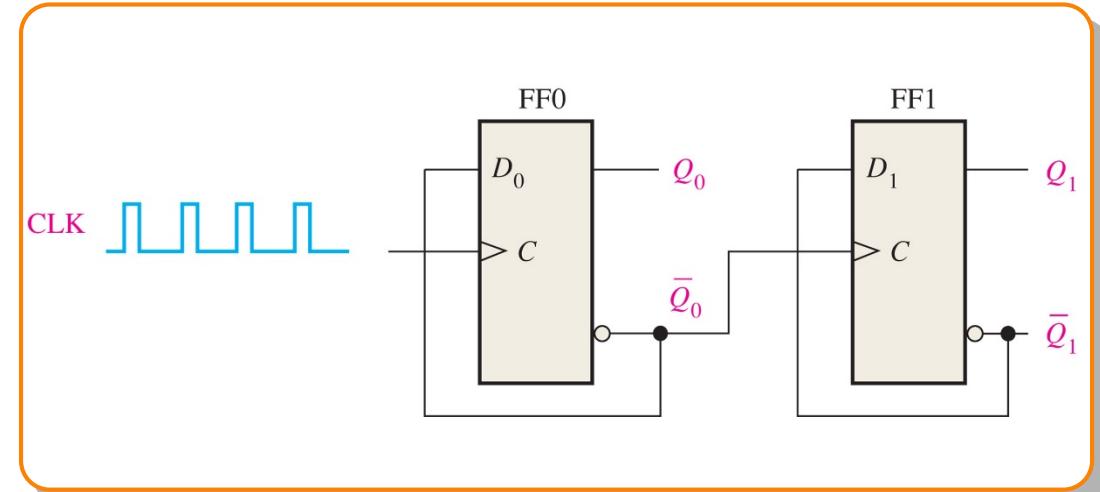


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Asynchronous Counters

- An asynchronous counter is one in which the flip-flops (FF) within the counter do not have a common clock;

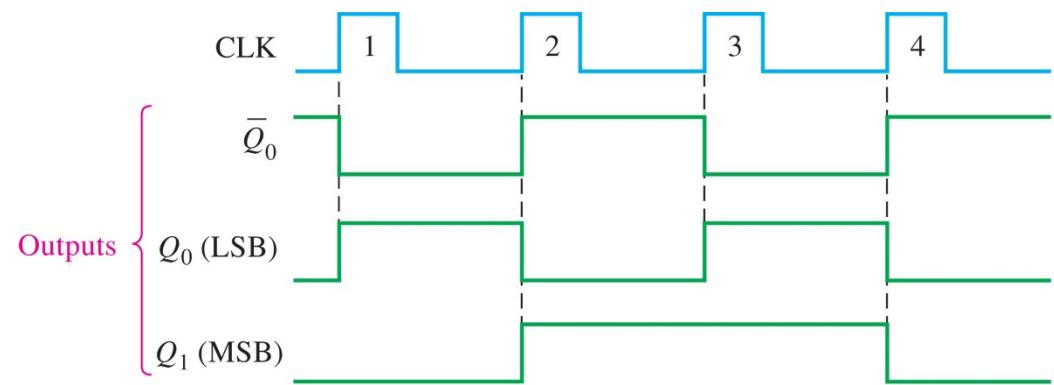


- The 2-bit asynchronous counter counts # of clock pulses up to 3, and on the 4th pulse, it recycles to its original state ($Q_0 = Q_1 = 0$).

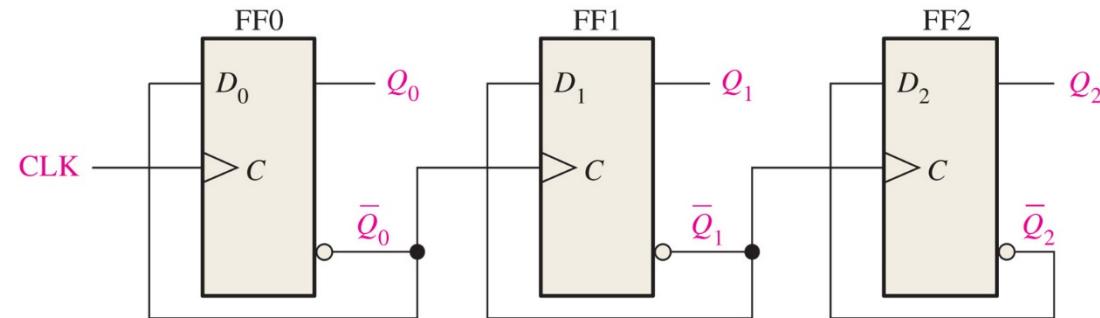
TABLE 9–1

Binary state sequence for the counter in Figure 9–4.

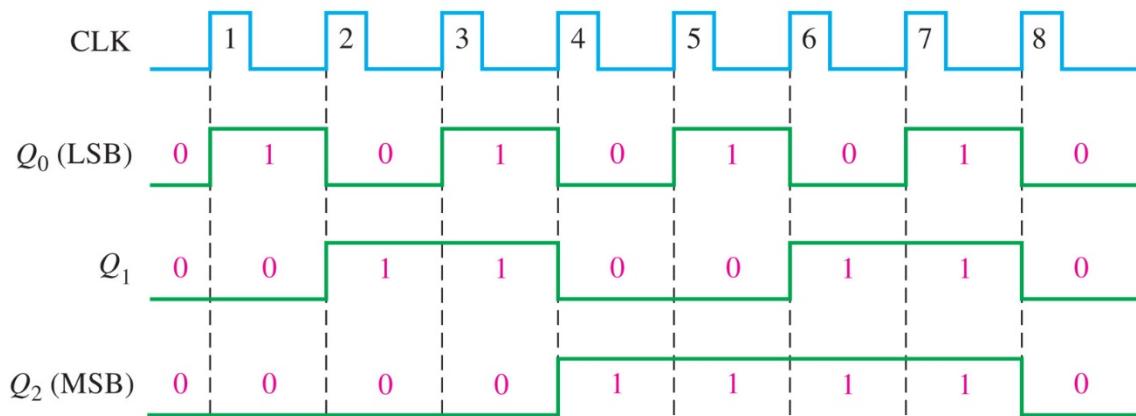
Clock Pulse	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0



A 3-Bit Asynchronous Binary Counter



(a)



(b)

TABLE 9-2

State sequence for a 3-bit binary counter.

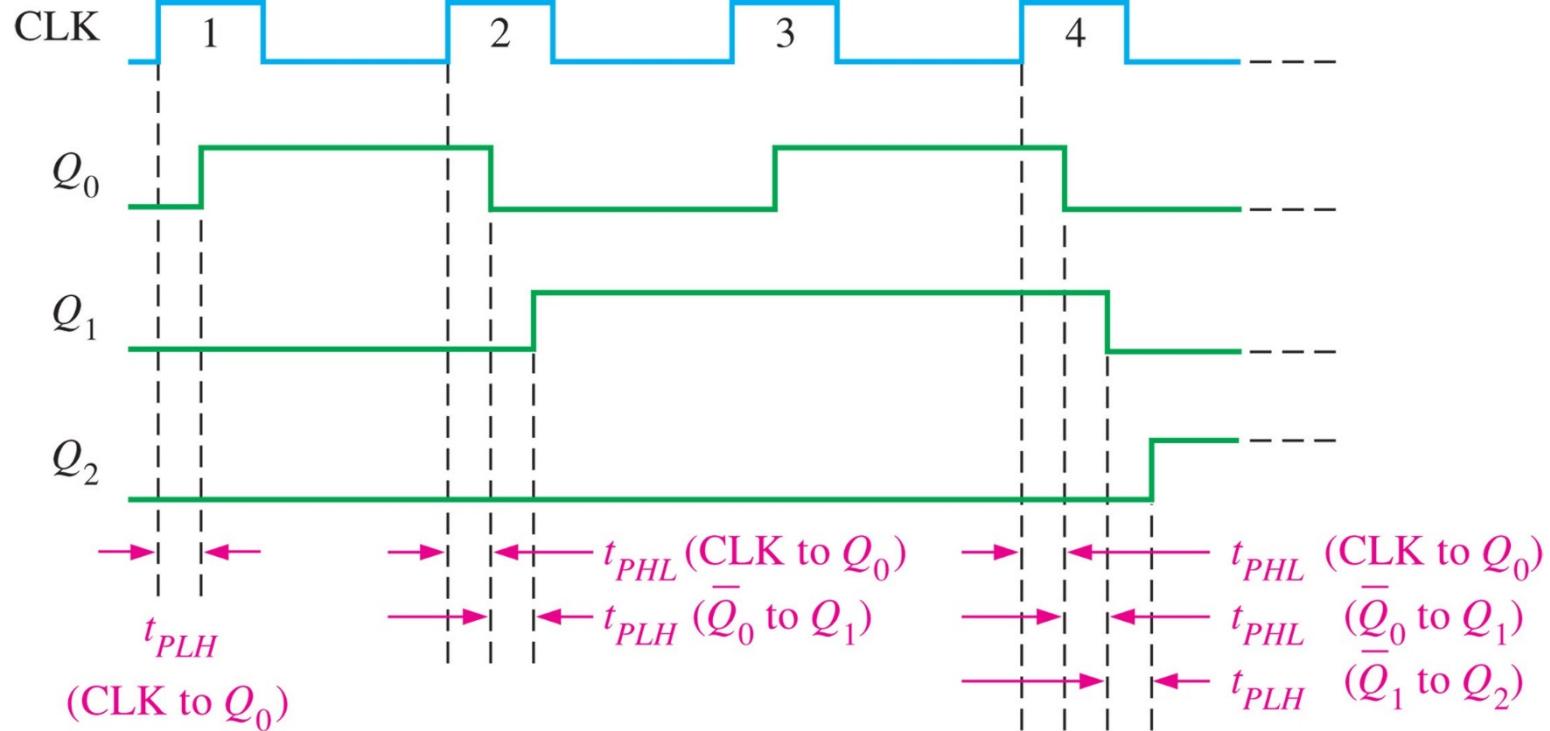
Clock Pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

□ Commonly referred to as **ripple** counters;

□ The cumulative delay of asynchronous counters is a major drawback.



Propagation Delay

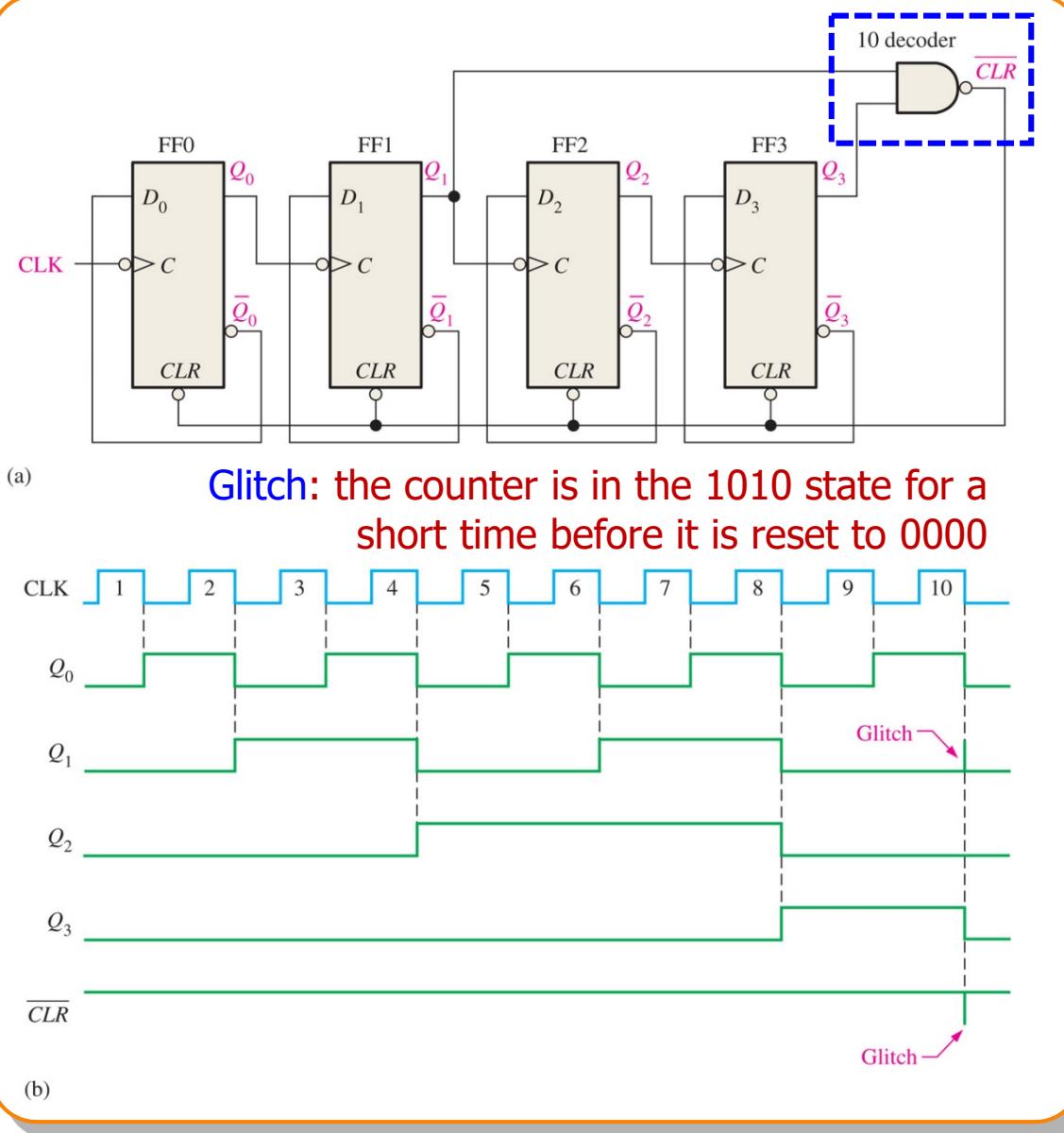


If each D flip-flop has a propagation delay for t second, then

- The total delay time: $t_{p(tot)} = t * \# \text{ of D flip-flops}$
- The maximum clock frequency: $f_{\max} = 1 / t_{p(tot)}$



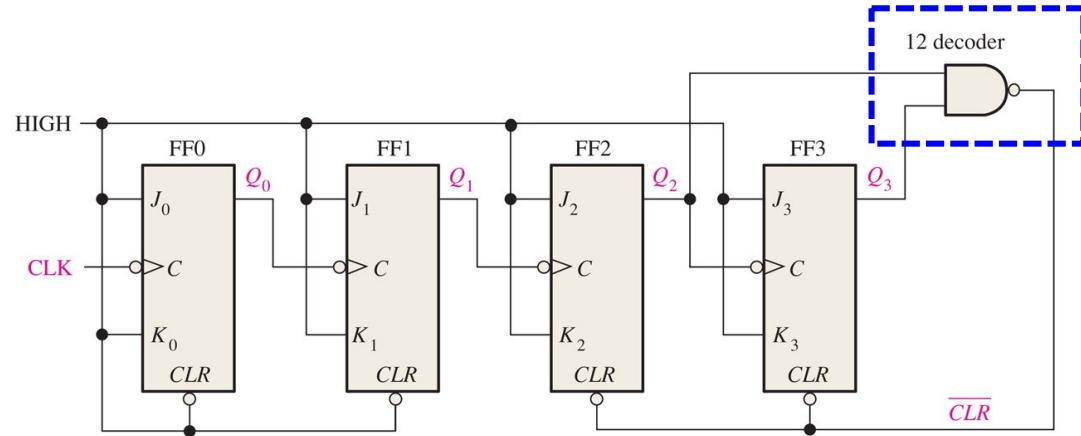
Asynchronous Decade Counters



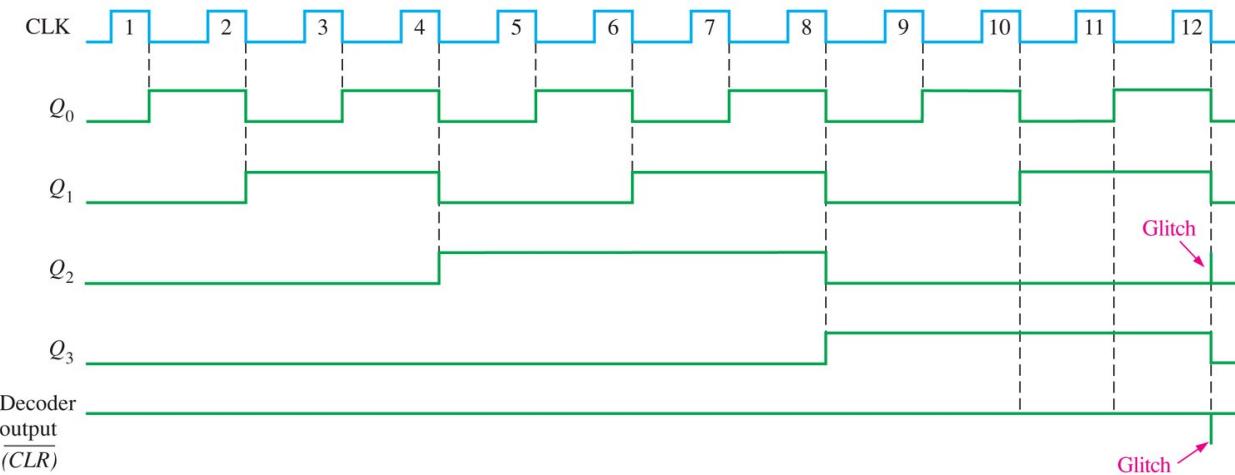
- Modulus: # of unique states through which the counter will sequence.
- Maximum modulus: 2^n for a counter of n flip-flops.
- Counters can have less than 2^n states, called a truncated sequence.
- Example: A **decade** counter with four flip-flops counts a truncated sequence from 0000 through 1001



Example 9–2 with J-K Flip-Flops



(a)

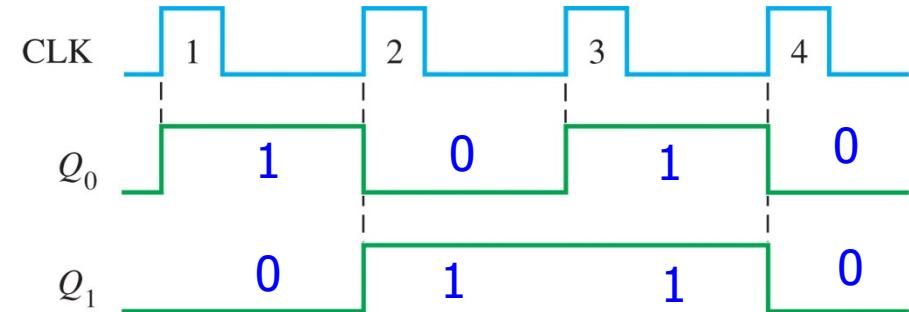
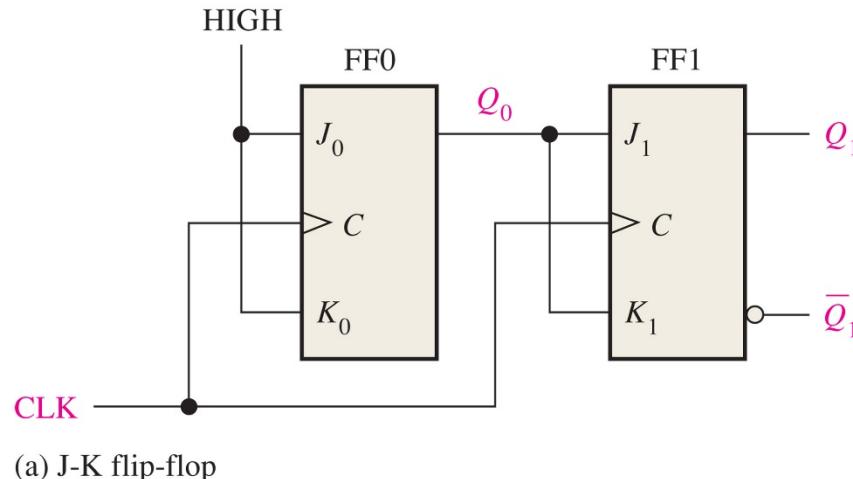


(b)

□ J and K inputs
are both HIGH →
Flip-flops toggle
between S/R
states



Synchronous Counters



- Synchronous: All flip-flops are controlled by the same clock
- Both J and K inputs are connected to HIGH
- Example: A **synchronous** counter with two flip-flops counts a sequence from 00 through 11 in four clock pulses

TABLE 7-3

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		Comments
J	K	CLK	Q	\bar{Q}	
0	0	↑	Q_0	\bar{Q}_0	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	\bar{Q}_0	Q_0	Toggle

↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition



A 3-Bit Synchronous Binary Counter

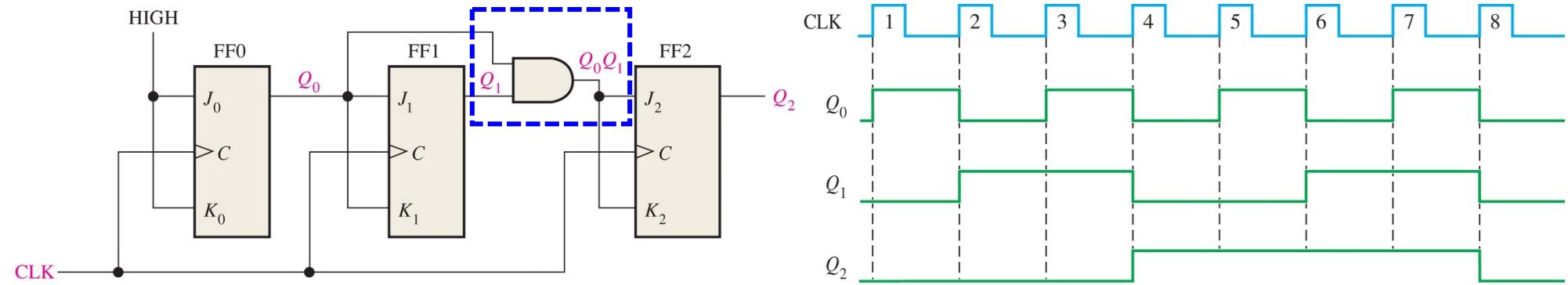


TABLE 9-4

Summary of the analysis of the counter in Figure 9–15.

Clock Pulse	Outputs			J-K Inputs					At the Next Clock Pulse			
	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	FF2	FF1	FF0
Initially	0	0	0	0	0	0	0	1	1	NC*	NC	Toggle
1	0	0	1	0	0	1	1	1	1	NC	Toggle	Toggle
2	0	1	0	0	0	0	0	1	1	NC	NC	Toggle
3	0	1	1	1	1	1	1	1	1	Toggle	Toggle	Toggle
4	1	0	0	0	0	0	0	1	1	NC	NC	Toggle
5	1	0	1	0	0	1	1	1	1	NC	Toggle	Toggle
6	1	1	0	0	0	0	0	1	1	NC	NC	Toggle
7	1	1	1	1	1	1	1	1	1	Toggle	Toggle	Toggle
										Counter recycles back to 000.		

*NC indicates No Change.



A 4-Bit Synchronous Decade Counter

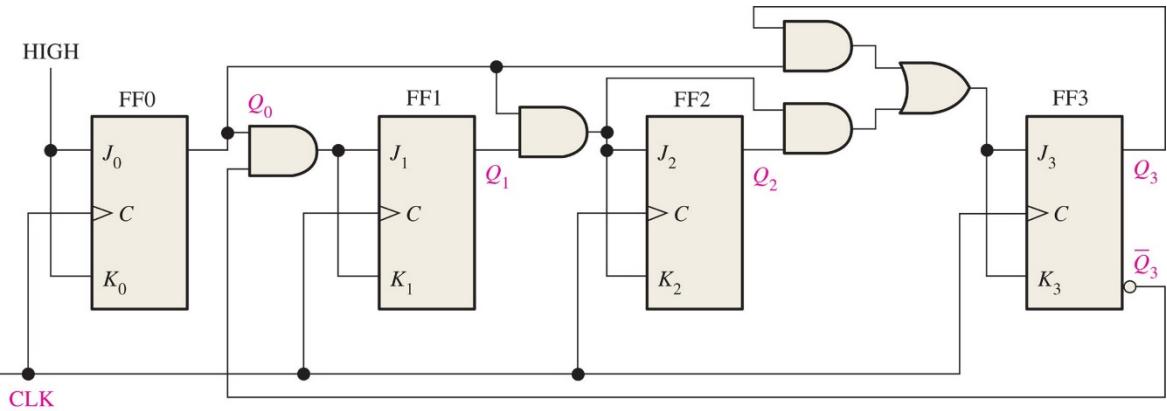
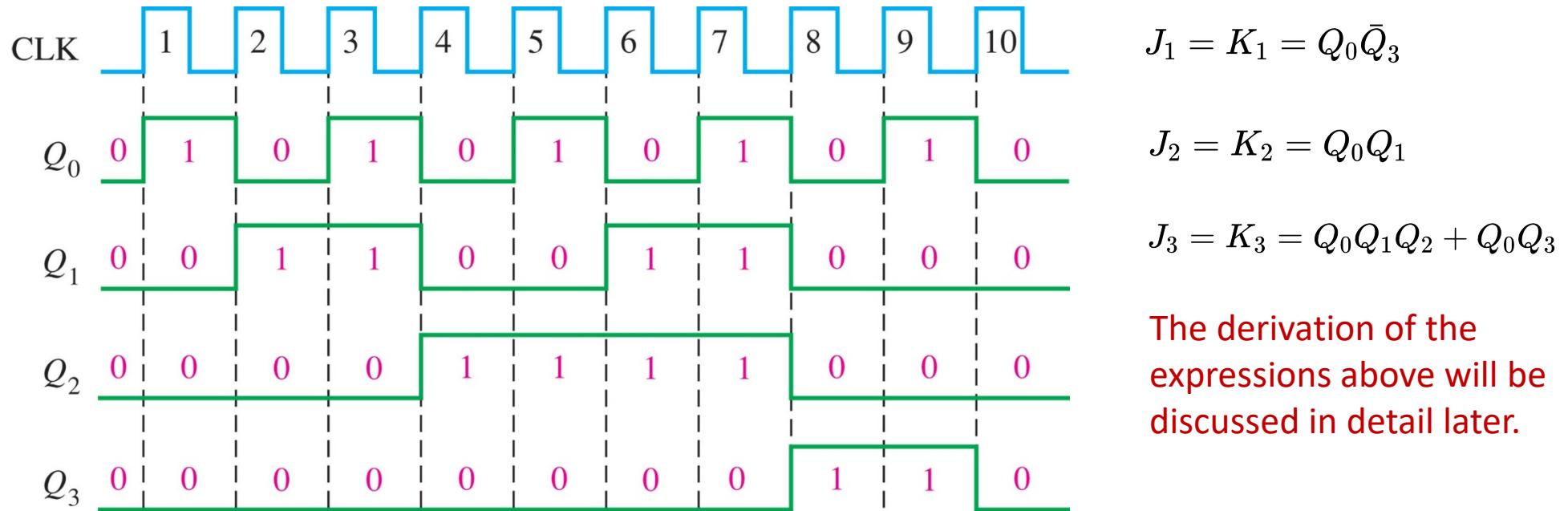


TABLE 9–5

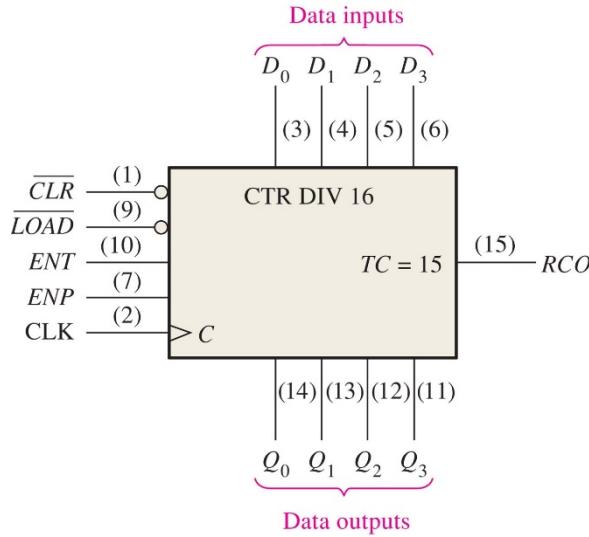
States of a BCD decade counter.

Clock Pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10 (recycles)	0	0	0	0

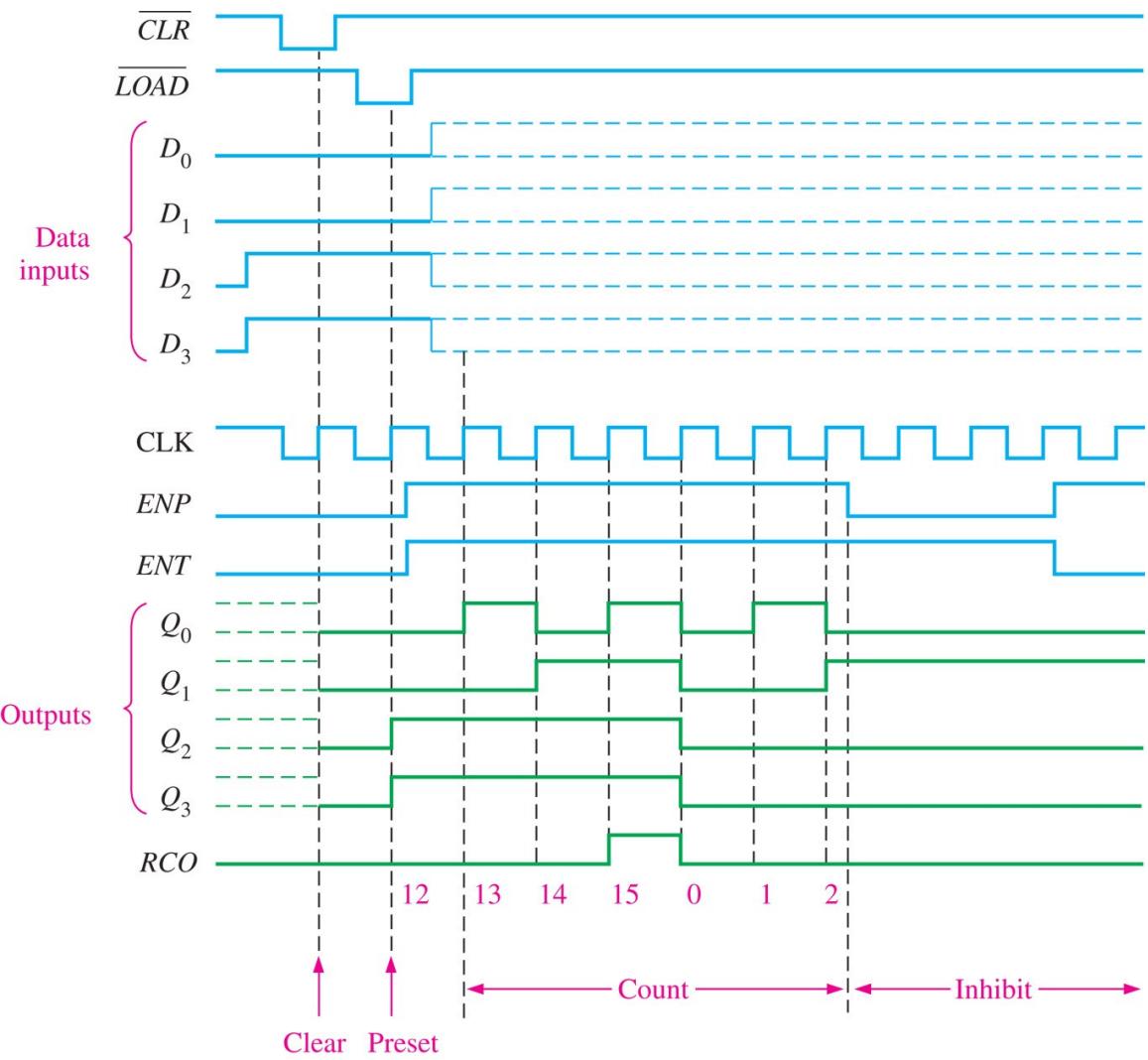


4-Bit Synchronous Binary Counter

74HC163 4-bit synchronous binary counter.



- When $LOAD$ is LOW, the counter will load $D_3D_2D_1D_0$ on the next clock pulse → the counter sequence can be started with any 4-bit binary number.
- The ripple clock output (RCO) goes HIGH when the counter reaches the last state in its sequence of fifteen, called the terminal count ($TC = 15$).



Up/Down Synchronous Counters

TABLE 9–6

Up/Down sequence for a 3-bit binary counter.

Clock Pulse	Up	Q_2	Q_1	Q_0	Down
0	↑	0	0	0	↓
1	↑	0	0	1	↓
2	↑	0	1	0	↓
3	↑	0	1	1	↓
4	↑	1	0	0	↓
5	↑	1	0	1	↓
6	↑	1	1	0	↓
7	↑	1	1	1	↓

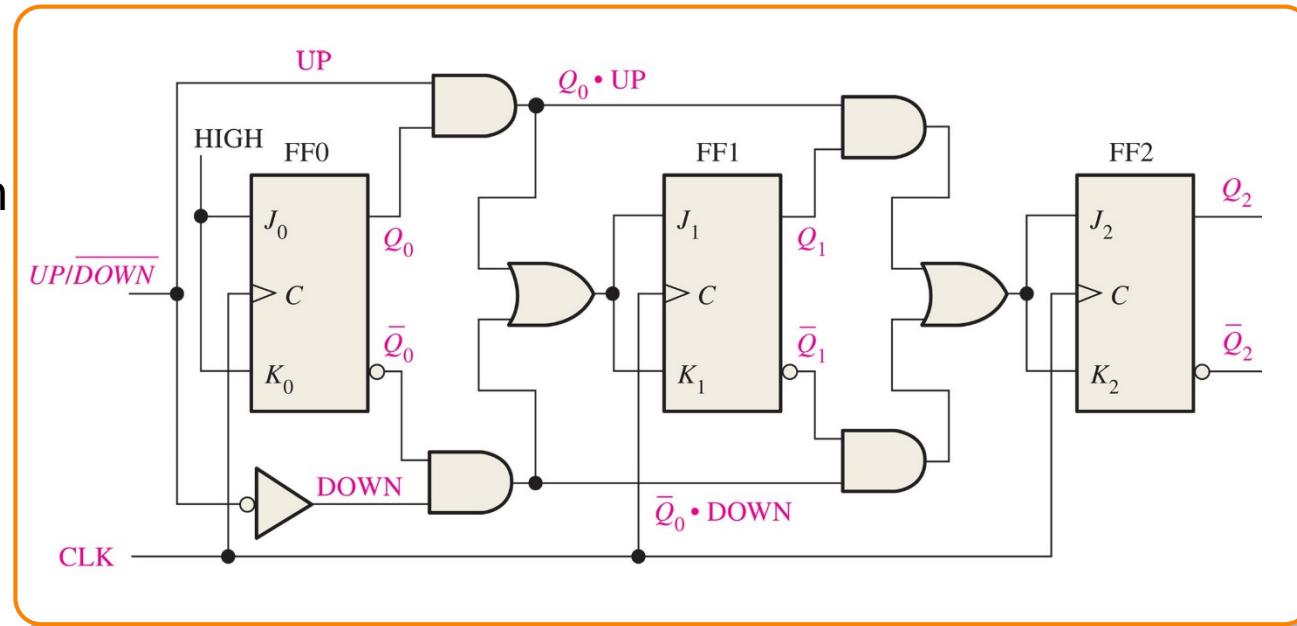
$$J_0 = K_0 = 1$$

$$J_1 = K_1 = (Q_0 \cdot \text{UP}) + (\bar{Q}_0 \cdot \text{DOWN})$$

$$J_2 = K_2 = (Q_0 \cdot Q_1 \cdot \text{UP}) + (\bar{Q}_0 \cdot \bar{Q}_1 \cdot \text{DOWN})$$

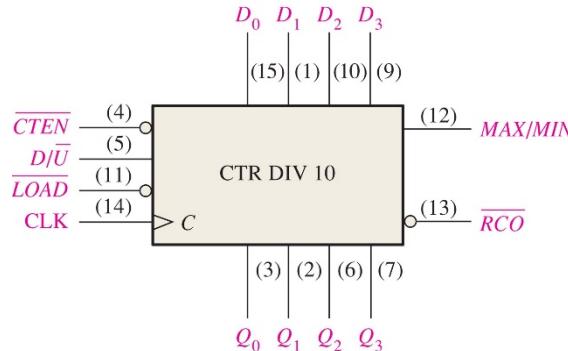
Again, the derivation of the expressions above will be discussed in detail later.

- Also known as the bidirectional counter that can progress in either direction
- In general, an UP/Down counter can be reversed at any point in its sequence

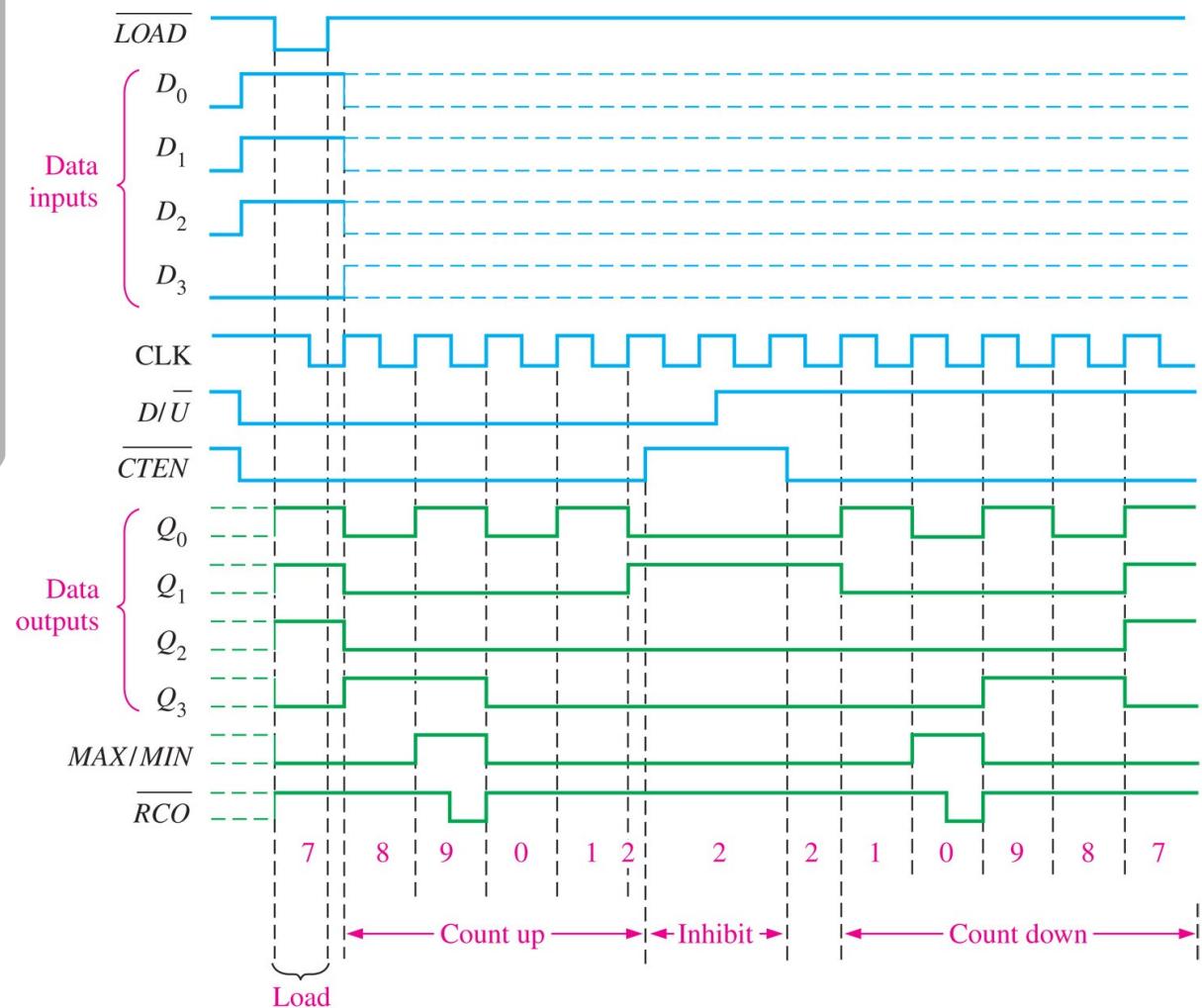


Implementation: Up/Down Decade Counters

74HC190 : a U/D synchronous decade counter



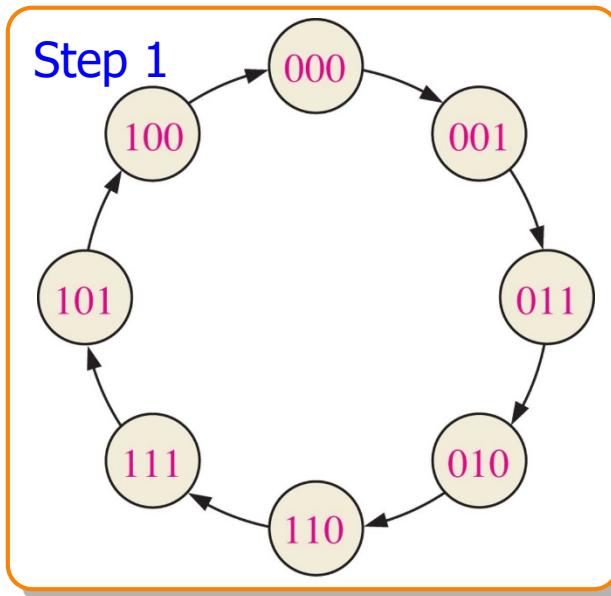
- The direction of the count is determined by the level of the up/down input (D/\bar{U}). When this input is HIGH, the counter counts down; when it is LOW, the counter counts up.



Design of Synchronous Counters (I)

Truth Table

- ❑ Step 1: State Diagram
- ❑ Step 2: Next-State Table
- ❑ Step 3: Flip-Flop Transition Table
- ❑ Step 4: Karnaugh Maps
- ❑ Step 5: Logic Expressions for Flip-Flop Inputs
- ❑ Step 6: Counter Implementation



Inputs		Outputs	
J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Step 2

TABLE 9-8

Next-state table for 3-bit Gray code counter.

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

TABLE 9-9

Transition table for a J-K flip-flop.

Step 3

Q_N	Output Transitions		Flip-Flop Inputs	
	Q_{N+1}	J	K	
0	→ 0	0	X	
0	→ 1	1	X	
1	→ 0	X	1	
1	→ 1	X	0	

Q_N : present state

Q_{N+1} : next state

X: “don’t care”



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Design of Synchronous Counters (II)

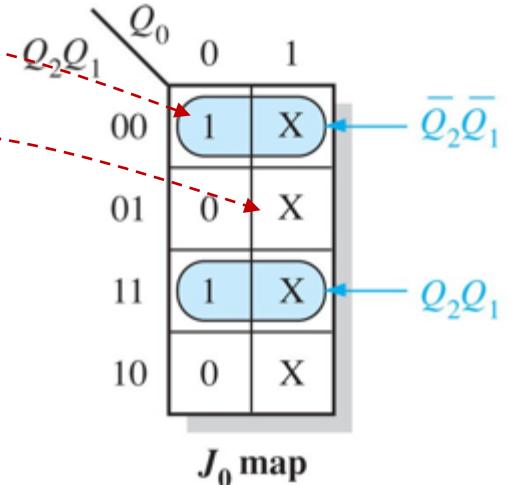
TABLE 9-8

Next-state table for 3-bit Gray code counter.

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

J_0	K_0
1	x
x	0
x	1
0	x
1	x
x	0
x	1
0	x

Step 4: Karnaugh Maps



Step 2

TABLE 9-9

Transition table for a J-K flip-flop.

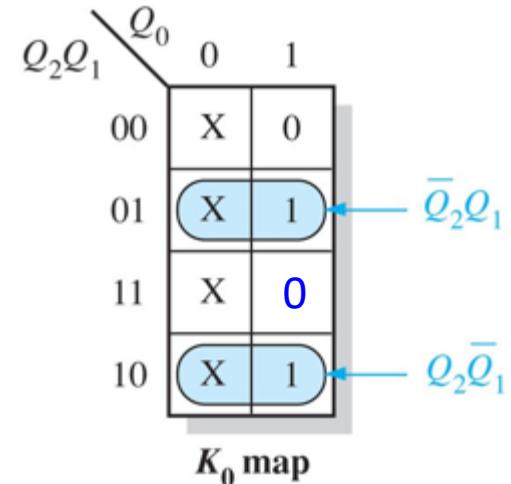
Output Transitions		Flip-Flop Inputs	
Q_N	Q_{N+1}	J	K
0	→ 0	0	X
0	→ 1	1	X
1	→ 0	X	1
1	→ 1	X	0

Q_N : present state

Q_{N+1} : next state

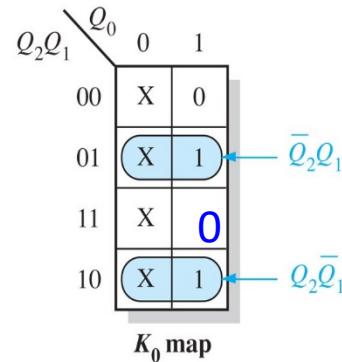
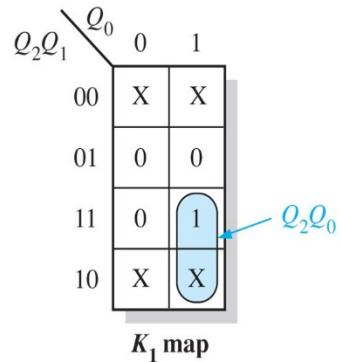
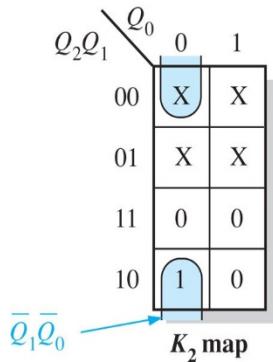
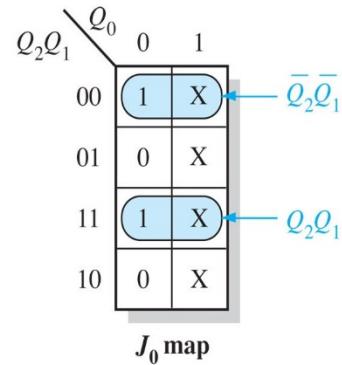
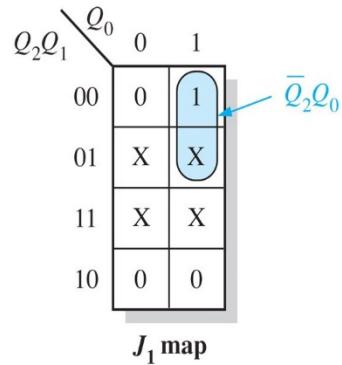
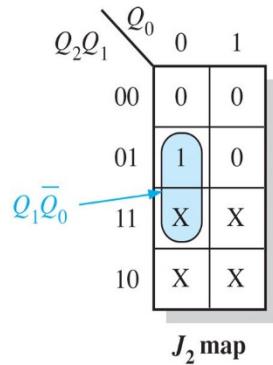
X: “don’t care”

Step 3



Design of Synchronous Counters (III)

Step 4: Karnaugh Maps



Step 5: Logic Expressions for Flip-Flop Inputs

$$J_0 = Q_2 Q_1 + \bar{Q}_2 \bar{Q}_1 = \overline{Q_2 \oplus Q_1}$$

$$K_0 = Q_2 \bar{Q}_1 + \bar{Q}_2 Q_1 = Q_2 \oplus Q_1$$

$$J_1 = \bar{Q}_2 Q_0$$

$$K_1 = Q_2 Q_0$$

$$J_2 = Q_1 \bar{Q}_0$$

$$K_2 = \bar{Q}_1 \bar{Q}_0$$



Design of Synchronous Counters (IV)

Step 5: Logic Expressions for Flip-Flop Inputs

$$J_0 = Q_2 Q_1 + \bar{Q}_2 \bar{Q}_1 = \overline{Q_2 \oplus Q_1}$$

$$K_0 = Q_2 \bar{Q}_1 + \bar{Q}_2 Q_1 = Q_2 \oplus Q_1$$

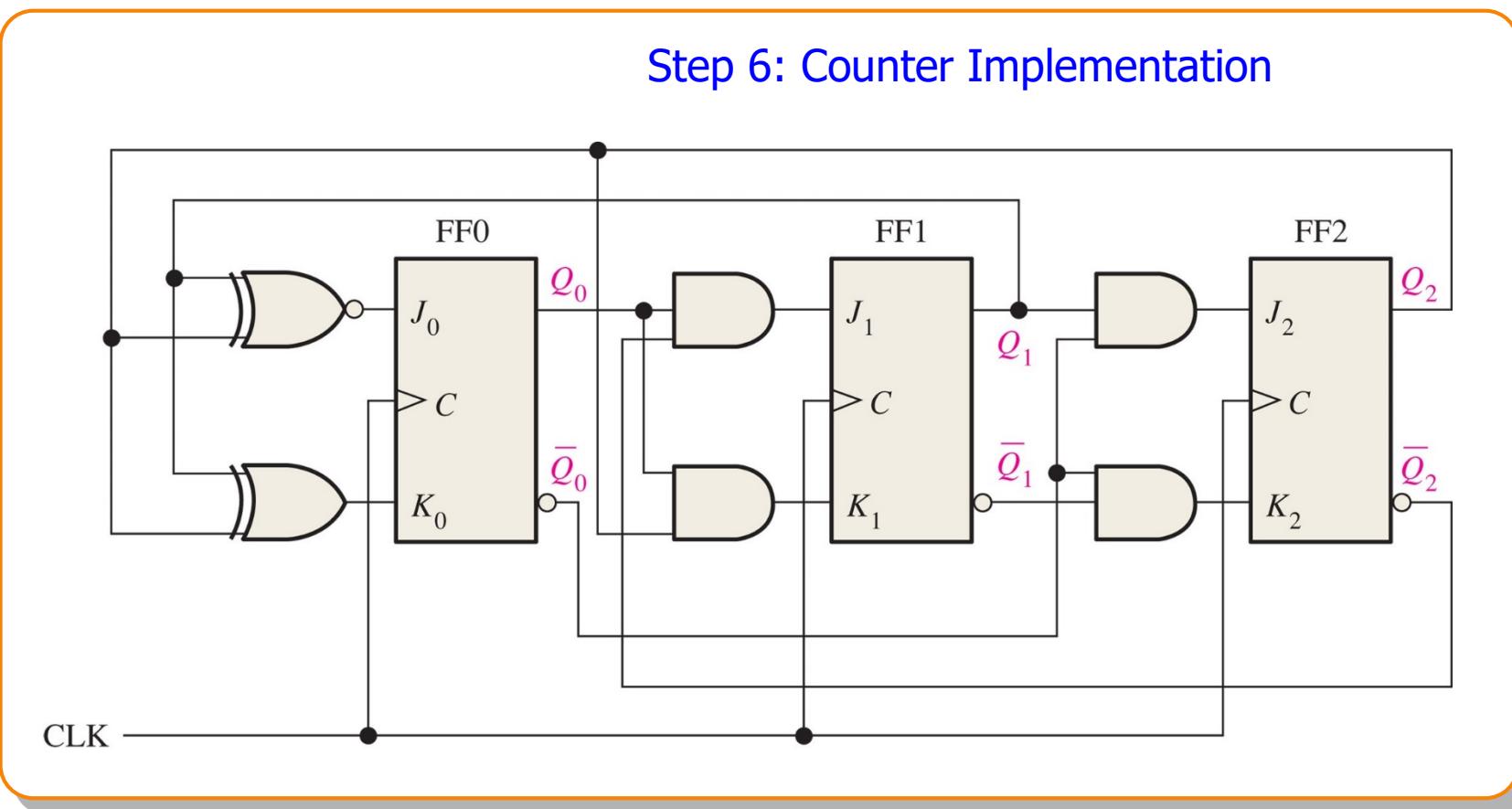
$$J_1 = \bar{Q}_2 Q_0$$

$$K_1 = Q_2 Q_0$$

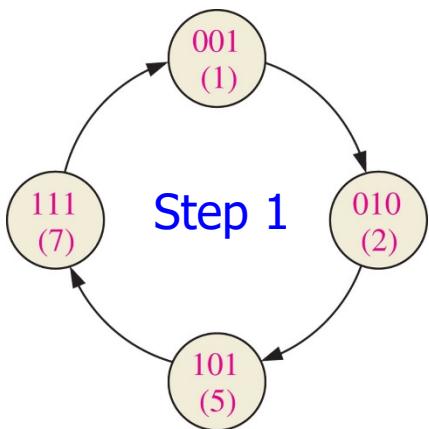
$$J_2 = Q_1 \bar{Q}_0$$

$$K_2 = \bar{Q}_1 \bar{Q}_0$$

Step 6: Counter Implementation



Example 9–4



Step 2

TABLE 9–10

Next-state table.

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0 0	0 1	1 0	0 1	0 1	0 1
1 0	0 0	1 1	1 1	1 0	1 1
1 1	1 1	1 1	0 0	0 0	1 1

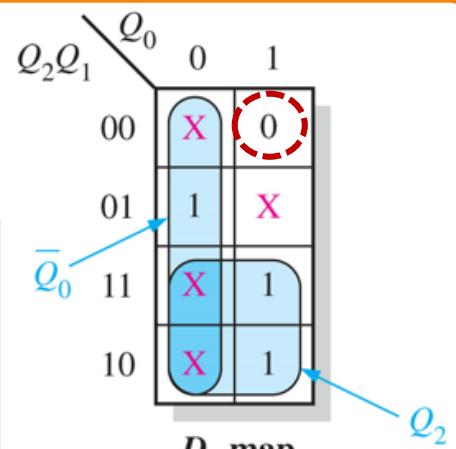
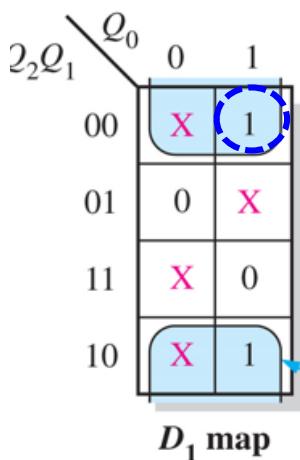
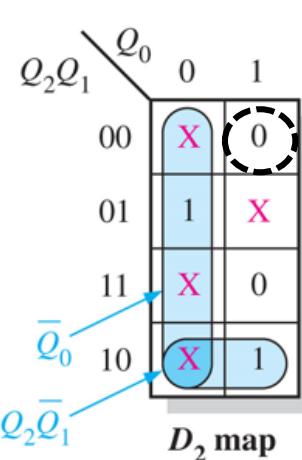
Step 3

TABLE 9–11

Transition table for a D flip-flop.

Output Transitions		Flip-Flop Input
Q_N	Q_{N+1}	D
0	→ 0	0
0	→ 1	1
1	→ 0	0
1	→ 1	1

Step 4



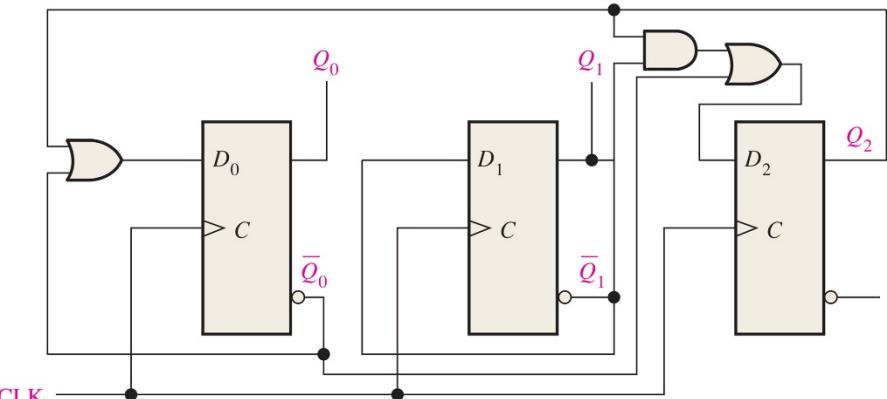
$$D_0 = \bar{Q}_0 + Q_2$$

$$D_1 = \bar{Q}_1$$

$$D_2 = \bar{Q}_0 + Q_2\bar{Q}_1$$

Step 5

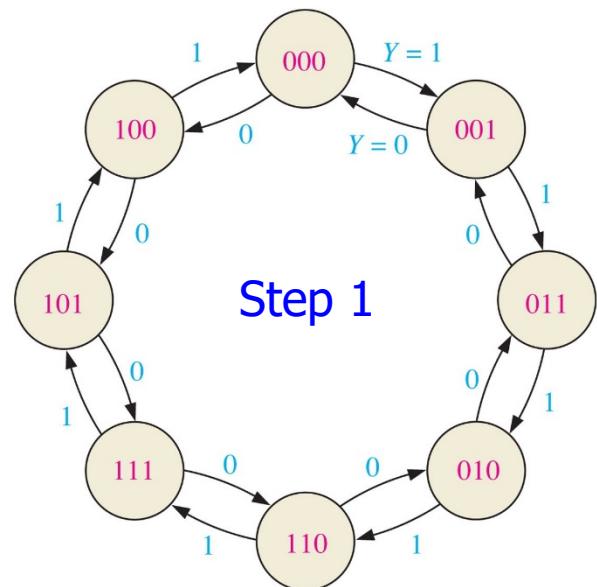
Step 6



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Example 9–5 : Synchronous 3-bit U/D Counters



	$Q_2 Q_1 Q_0 Y$	00	01	11	10
00	1	0	0	0	0
01	0	1	0	0	0
11	X	X	X	X	X
10	X	X	X	X	X

$\bar{Q}_1 \bar{Q}_0 Y$

	$Q_2 Q_1 Q_0 Y$	00	01	11	10
00	0	0	1	0	0
01	X	X	X	X	X
11	X	X	X	X	X
10	0	0	0	0	1

$Q_1 \bar{Q}_0 Y$

	$Q_2 Q_1 Q_0 Y$	00	01	11	10
00	0	0	X	X	X
01	1	0	X	X	X
11	0	1	X	X	X
10	1	0	X	X	X

$\bar{Q}_2 \bar{Q}_1 Y$

Step 4

	$Q_2 Q_1 Q_0 Y$	00	01	11	10
00	X	X	X	X	X
01	X	X	X	X	X
11	1	0	0	0	0
10	0	1	0	0	0

$\bar{Q}_1 \bar{Q}_0 Y$

	$Q_2 Q_1 Q_0 Y$	00	01	11	10
00	X	X	X	X	X
01	0	0	0	1	X
11	0	0	1	0	X
10	X	X	X	X	X

$Q_2 Q_0 Y$

	$Q_2 Q_1 Q_0 Y$	00	01	11	10
00	X	X	0	1	X
01	X	X	1	0	0
11	X	X	0	1	0
10	X	X	1	0	0

$\bar{Q}_2 \bar{Q}_1 Y$



TABLE 9-12

Next-state table for 3-bit up/down Gray code counter.

Step 2

Present State			Next State $Y = 0$ (DOWN)			Next State $Y = 1$ (UP)		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	1	0
0	1	0	0	1	1	1	1	0
1	1	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	1
1	0	1	1	1	1	1	0	0
1	0	0	1	0	1	0	0	0

$Y = \text{UP/DOWN}$ control input.

- The counter should count up when UP/DOWN is 1 and count down when 0.

$$J_0 = Q_2 Q_1 Y + Q_2 \bar{Q}_1 \bar{Y} + \bar{Q}_2 \bar{Q}_1 Y + \bar{Q}_2 Q_1 \bar{Y}$$

$$J_1 = \bar{Q}_2 Q_0 Y + Q_2 Q_0 \bar{Y}$$

$$J_2 = Q_1 \bar{Q}_0 Y + \bar{Q}_1 \bar{Q}_0 \bar{Y}$$

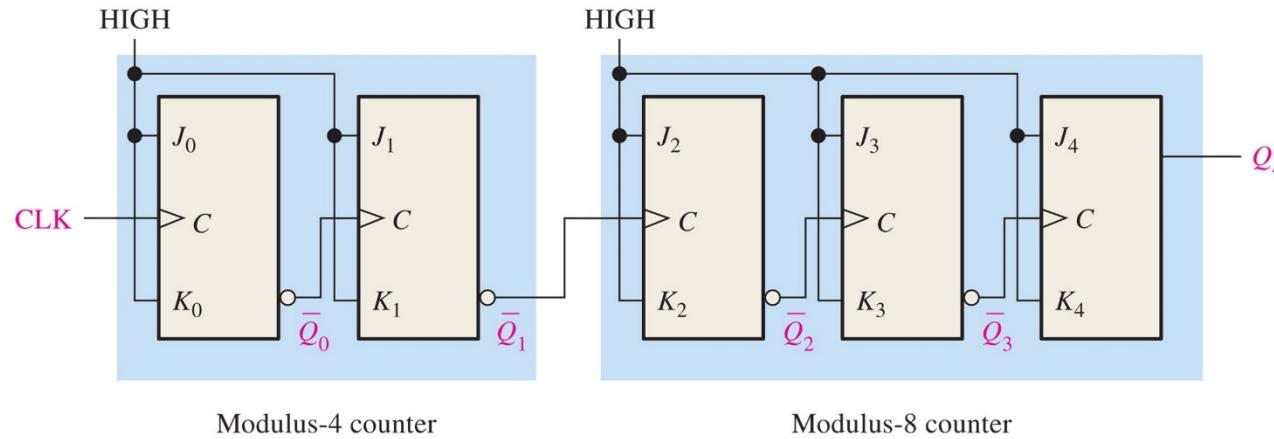
Step 5

$$K_0 = \bar{Q}_2 \bar{Q}_1 \bar{Y} + \bar{Q}_2 Q_1 Y + Q_2 \bar{Q}_1 Y + Q_2 Q_1 \bar{Y}$$

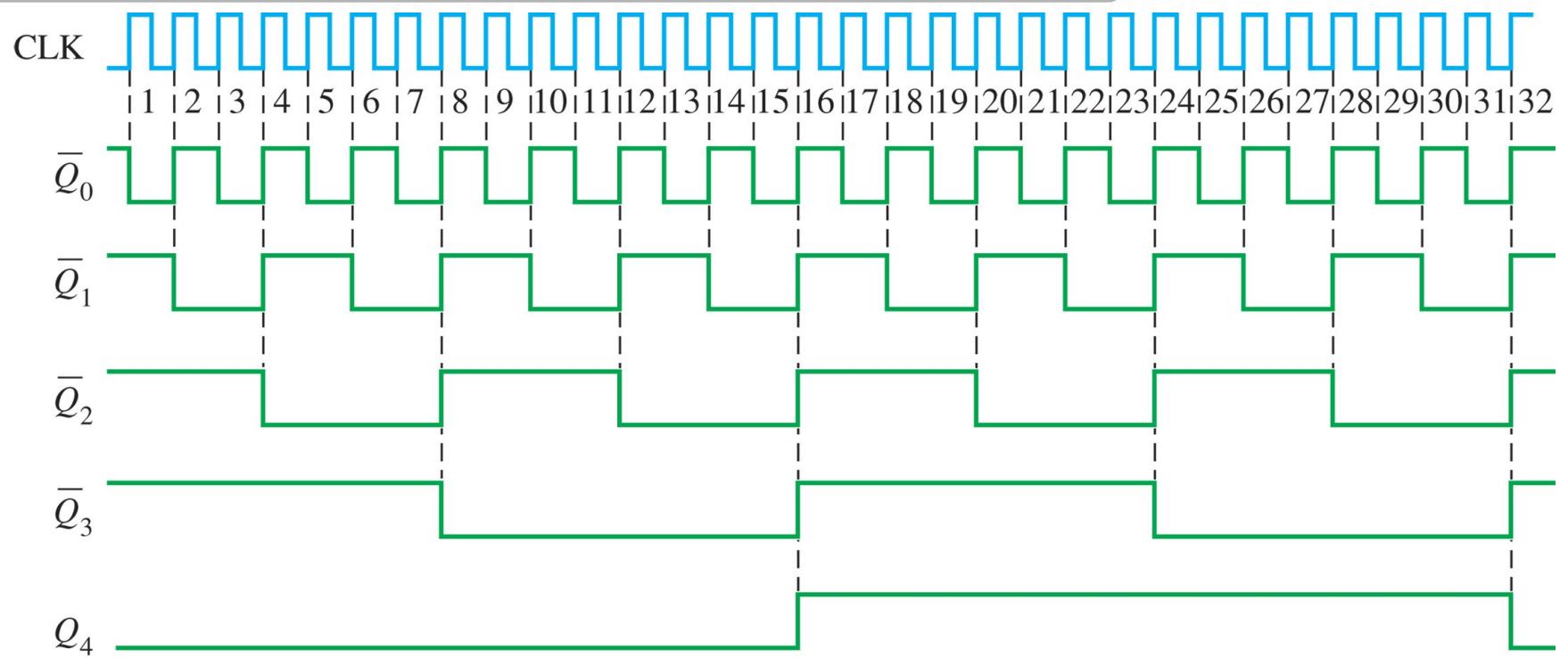
$$K_1 = \bar{Q}_2 Q_0 \bar{Y} + Q_2 Q_0 Y$$

$$K_2 = Q_1 \bar{Q}_0 \bar{Y} + \bar{Q}_1 \bar{Q}_0 Y$$

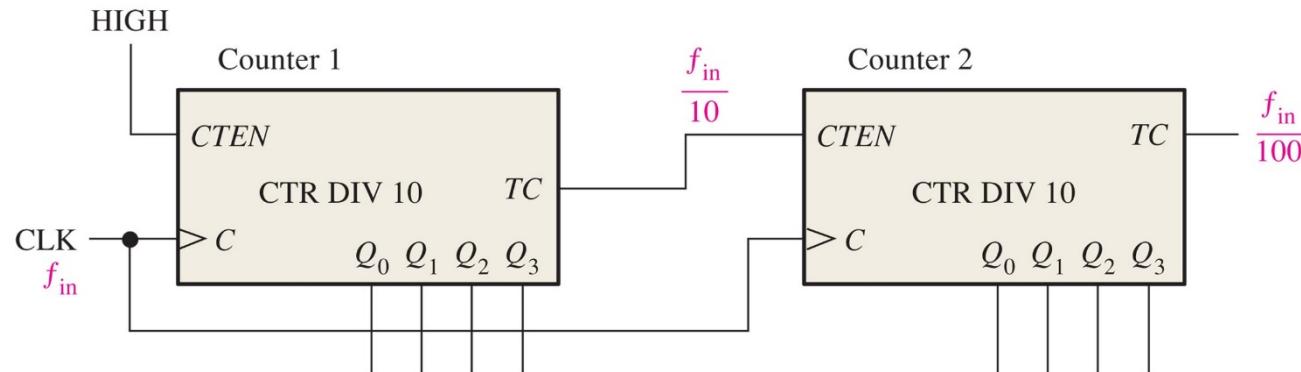
Cascaded Counters: Asynchronous



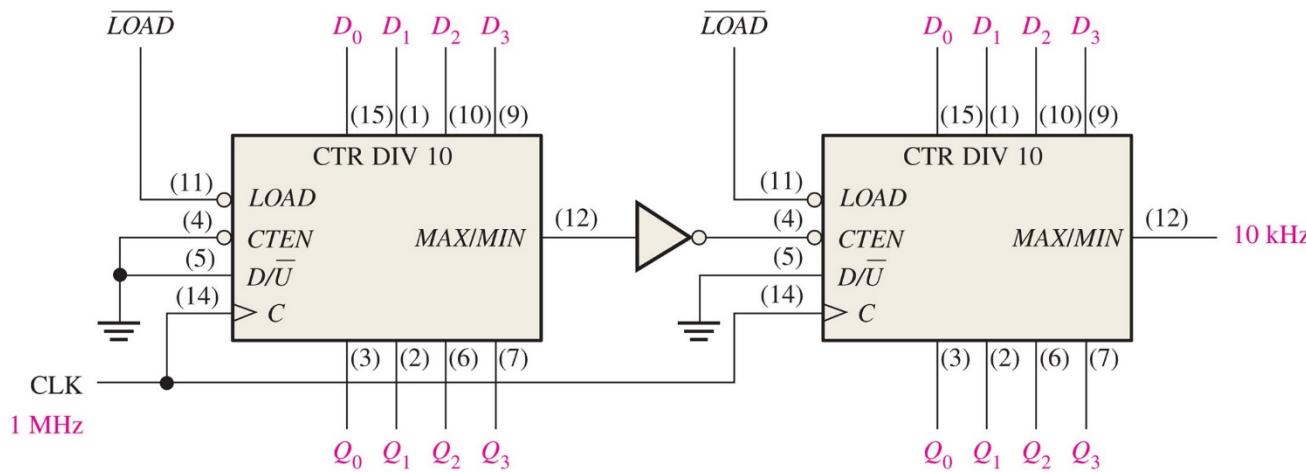
- The overall modulus of the two cascaded counters is $4 * 8 = 32$; that is, they act as a divide-by-32 counter.



Cascaded Counters: Synchronous



- The overall modulus of these two cascaded counters is $10 * 10 = 100$.

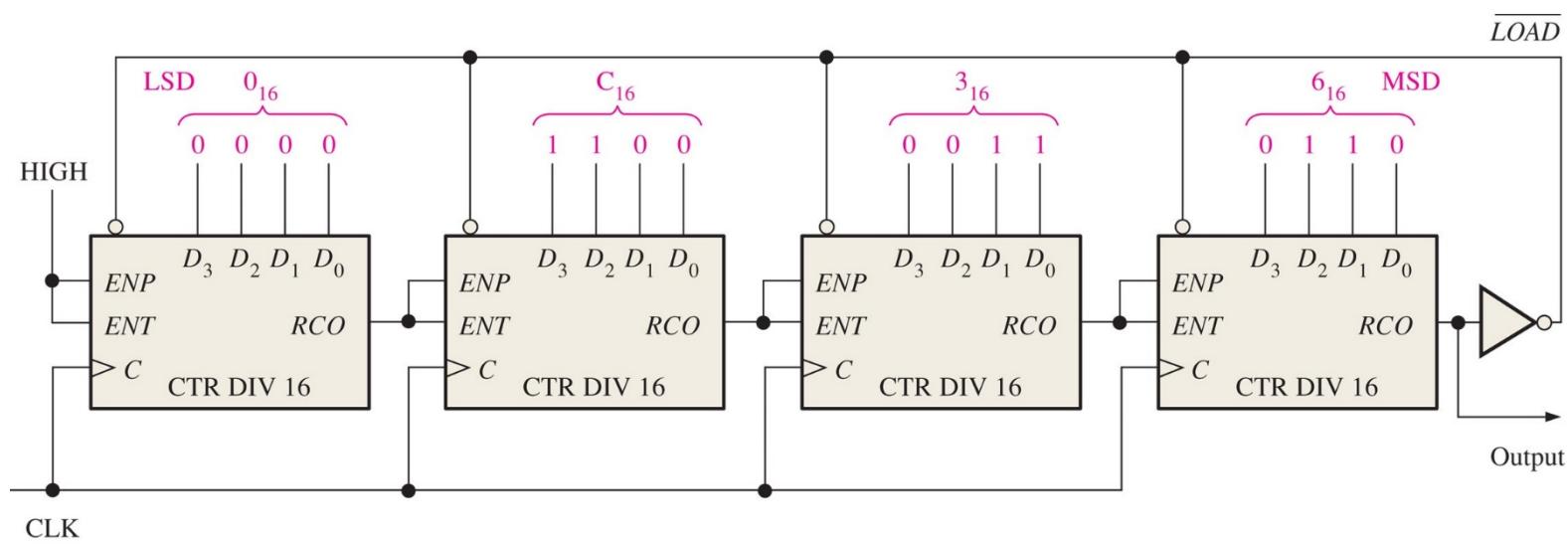


- A divide-by-100 counter using two 74HC190 up/down decade counters connected for the up sequence.



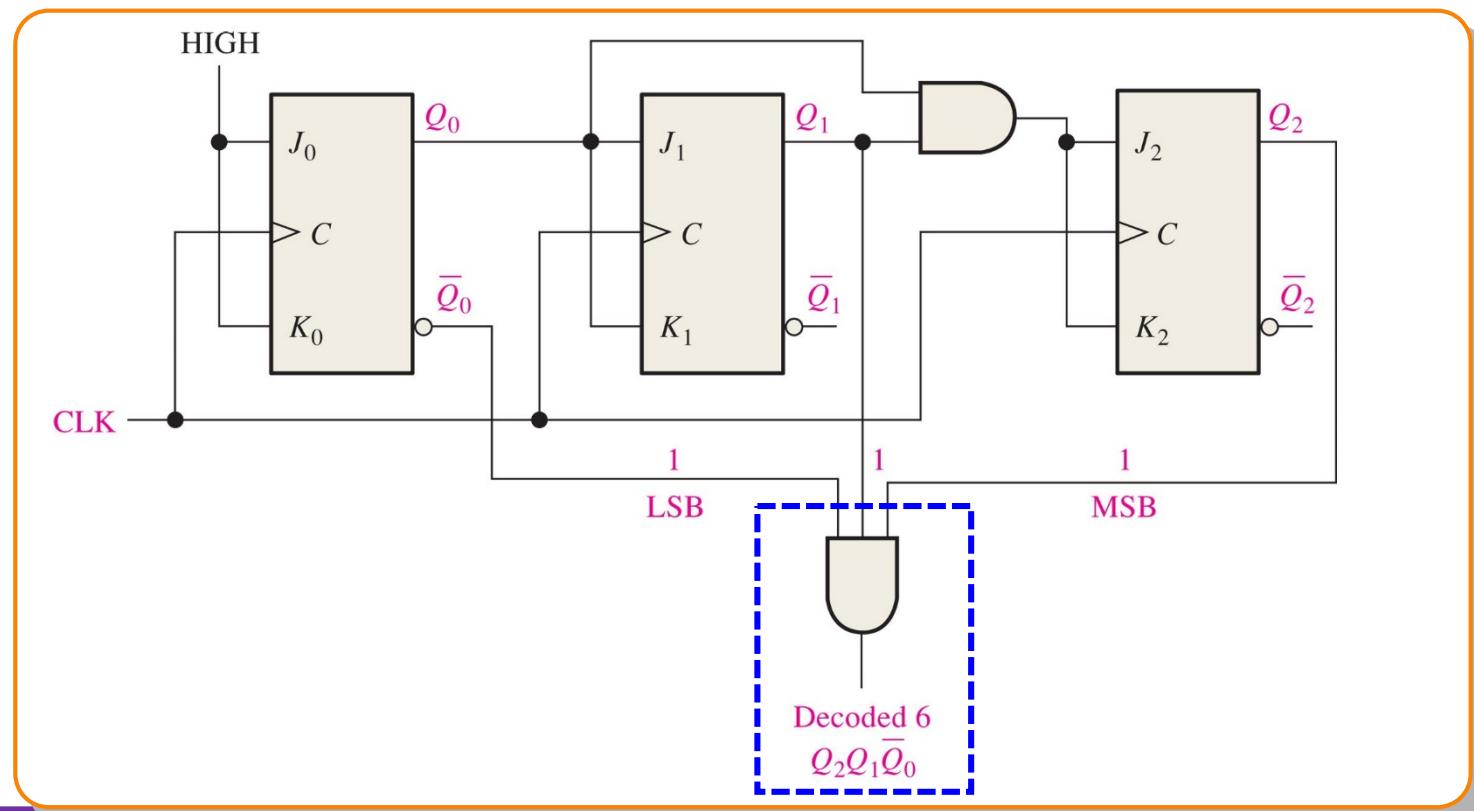
Cascaded Counters with Truncated Sequences

- Full-modulus cascading: the resulting overall modulus is the product of the individual moduli of all the cascaded counters.
- If the required modulus is less than that achieved by full modulus cascading, a truncated sequence must be implemented with cascaded counters.
- Example: to achieve a modulus-40,000 counter with four cascaded 74HC161s whose full modulus is $2^{16}=65,536$, we preset the cascaded counter to 25,536 (63C0 in hexadecimal) each time it recycles. $65,536 - 25536 = 40,000$

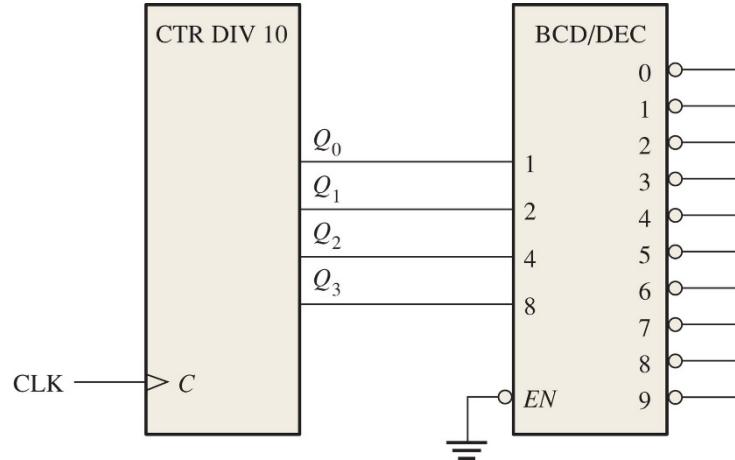


Counter Decoding

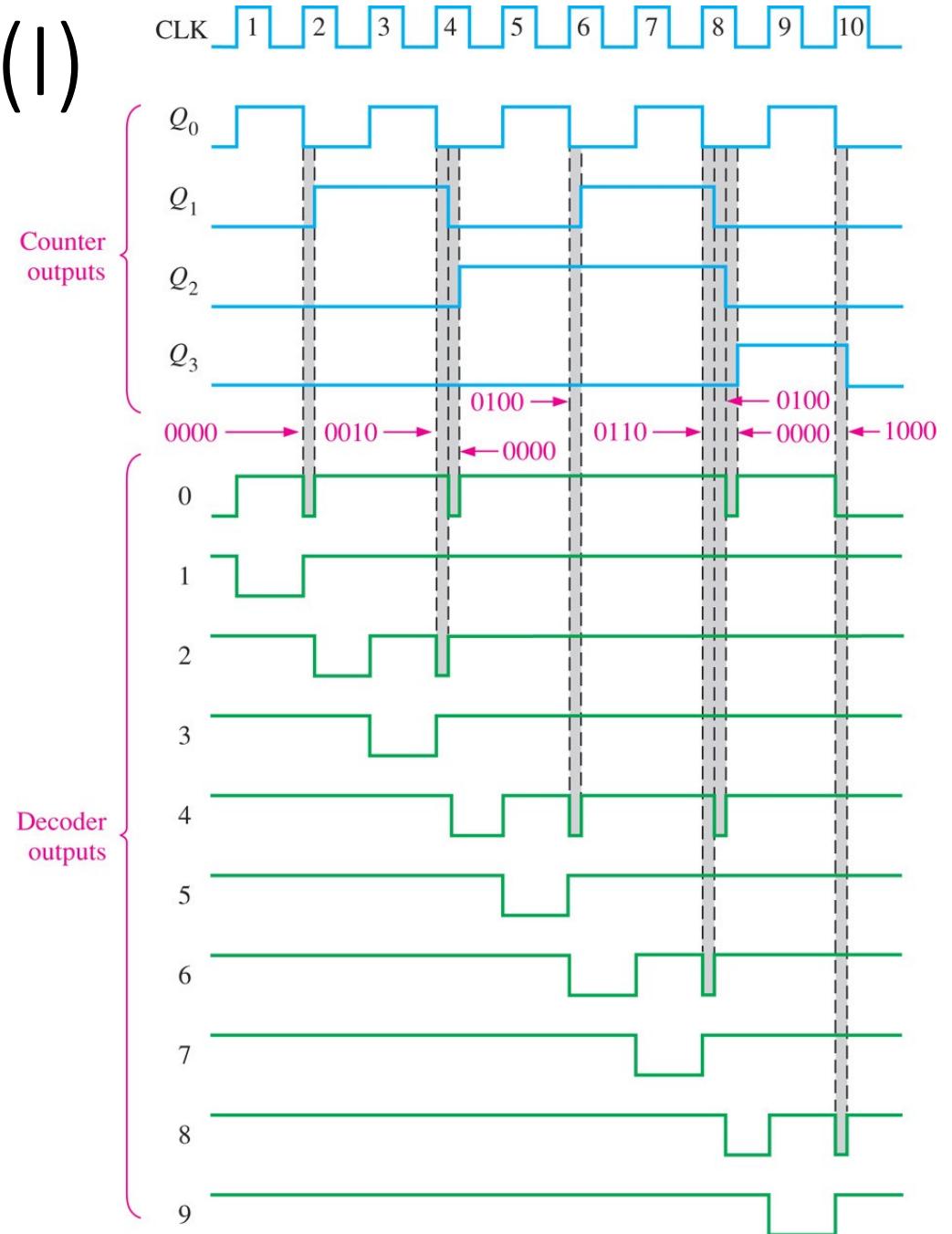
- The decoding of a counter involves using decoders or logic gates to determine when the counter is in a certain binary state in its sequence.
- For example, when $Q_2 = 1$, $Q_1 = 1$, and $Q_0 = 0$, a HIGH appears on the output of the following decoding gate, indicating that the counter is at state 6.



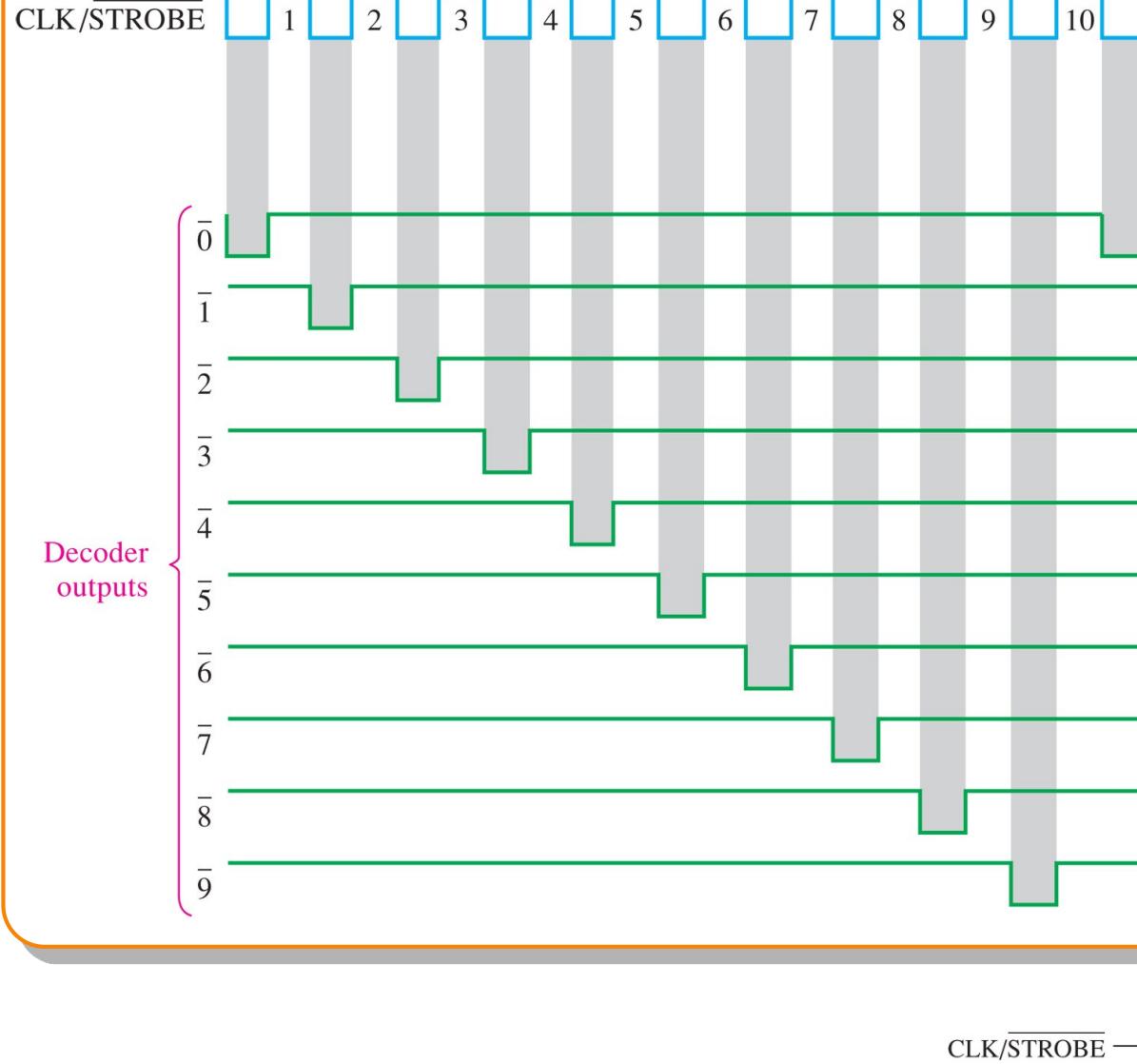
Decoding Glitches (I)



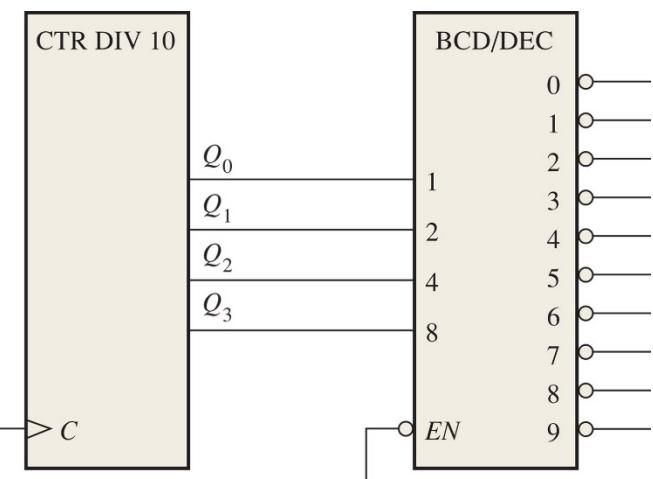
- The glitch problem can also occur to synchronous counters because the propagation delays from the clock to the Q outputs of each flip-flop in a counter can vary slightly.



Decoding Glitches (II)

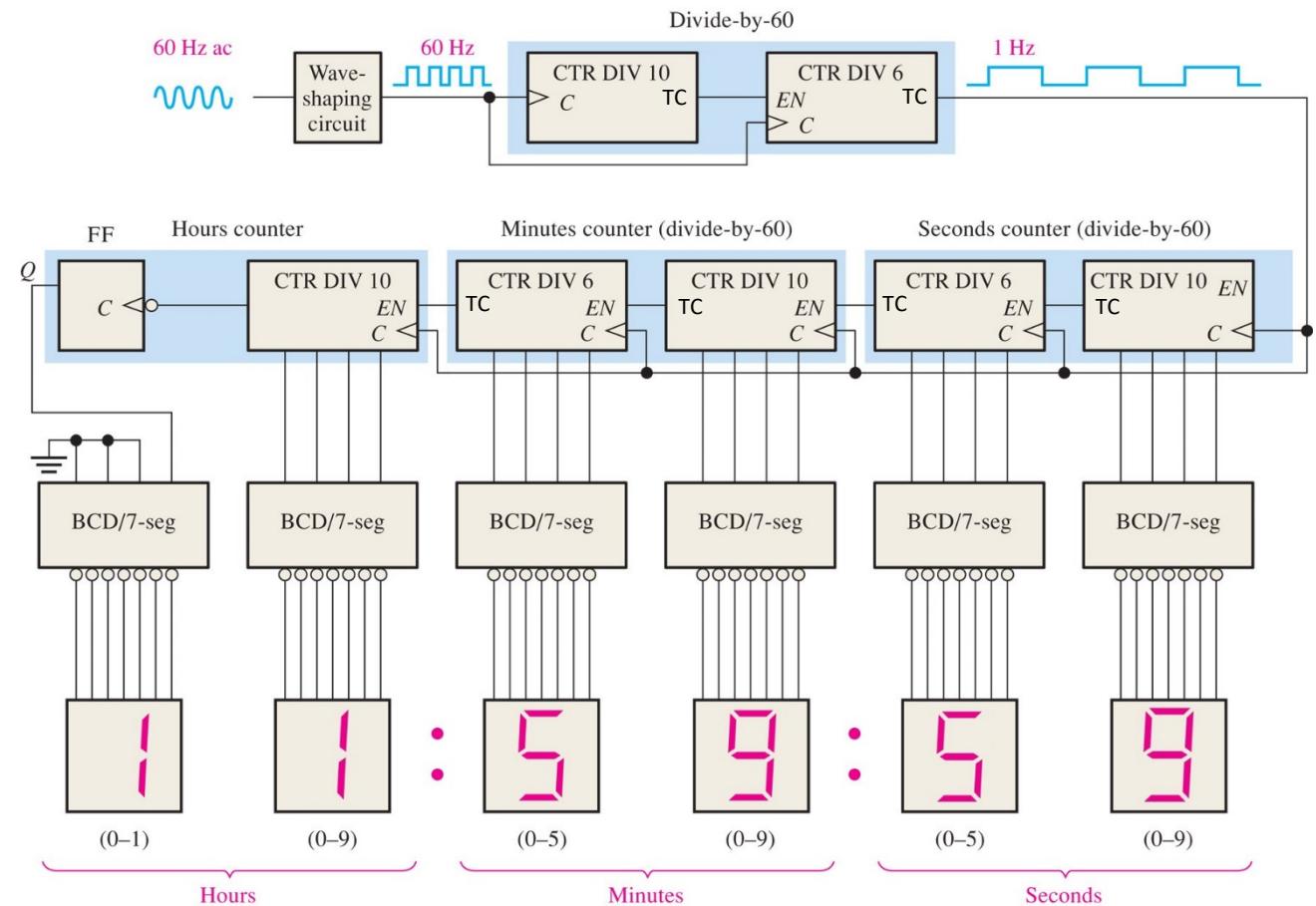


- For an active-HIGH clock, use the LOW level of the clock to enable the decoder.

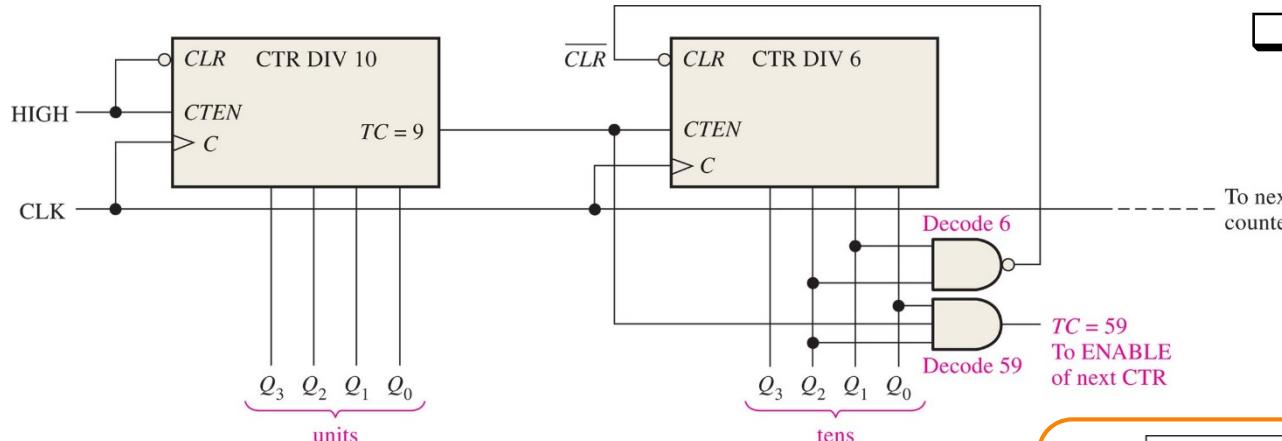


Counter Applications: A Digital Clock

- Input : a 60 Hz pulse waveform generated from a 60 Hz sinusoidal ac voltage;
- Counters for Seconds and Minutes : count from 0 to 59 and then recycle to 0;
- The hour counter : a decade counter and a flip-flop to illuminate a 1 on the tens-of-hours display.



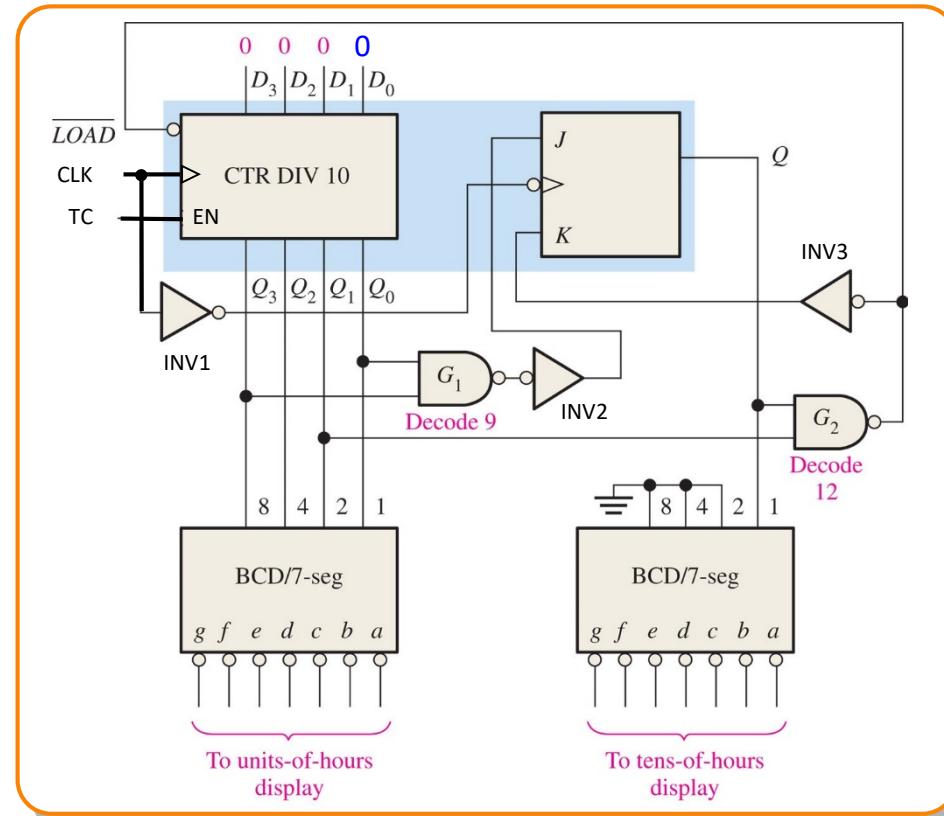
The Second/Minute/Hour Counter



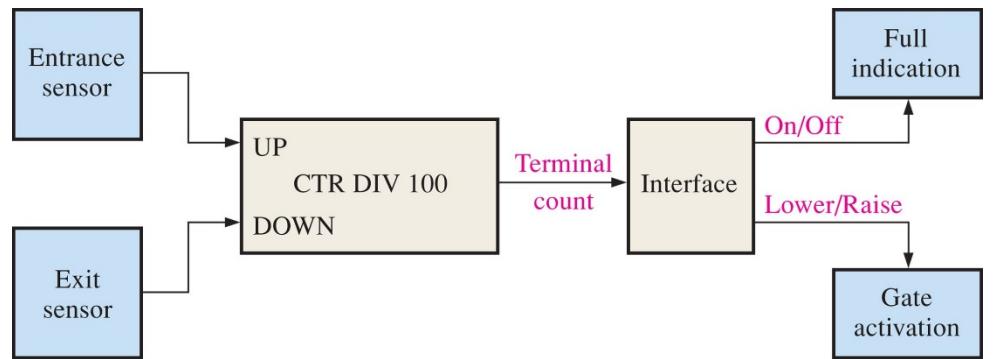
The right-most bit is the LSB

- In state 12, the G_2 output is LOW (i.e. Q and Q_1 are HIGH), which activates the LOAD input of the decade counter.
- On the next clock pulse, the decade counter is preset to 0000.

□ The terminal count, 59, is decoded to enable the next counter in the chain.

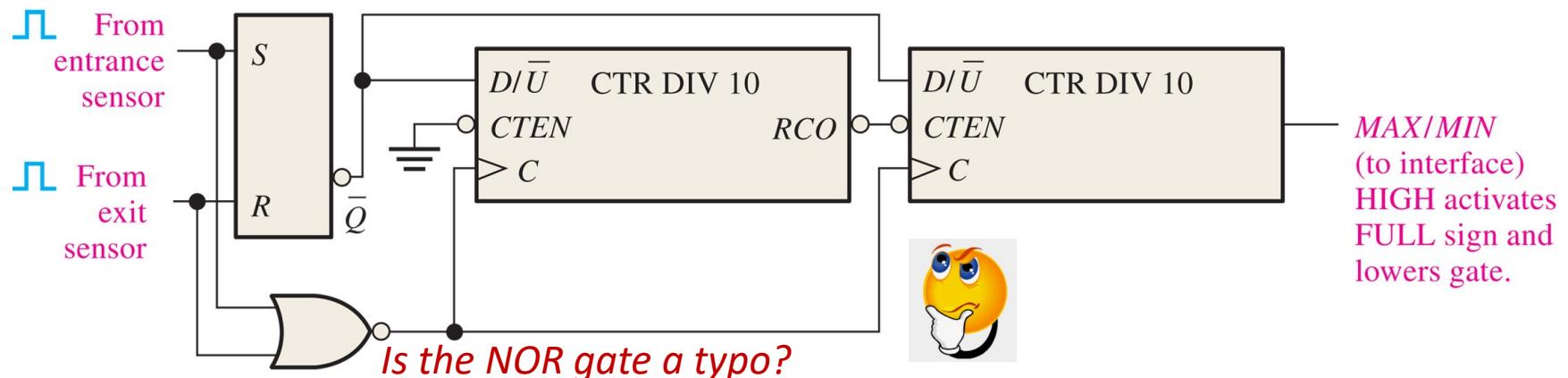


Automobile Parking Control



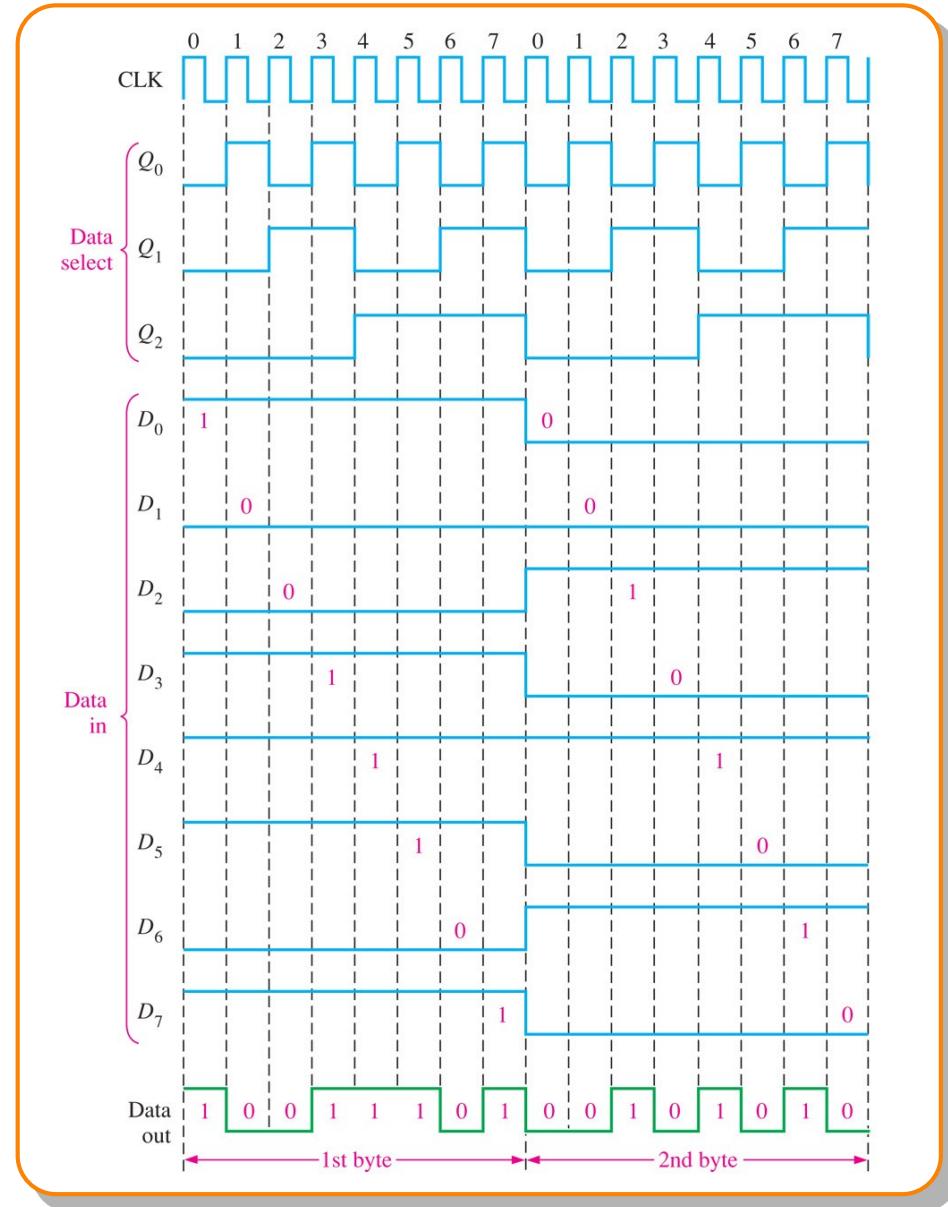
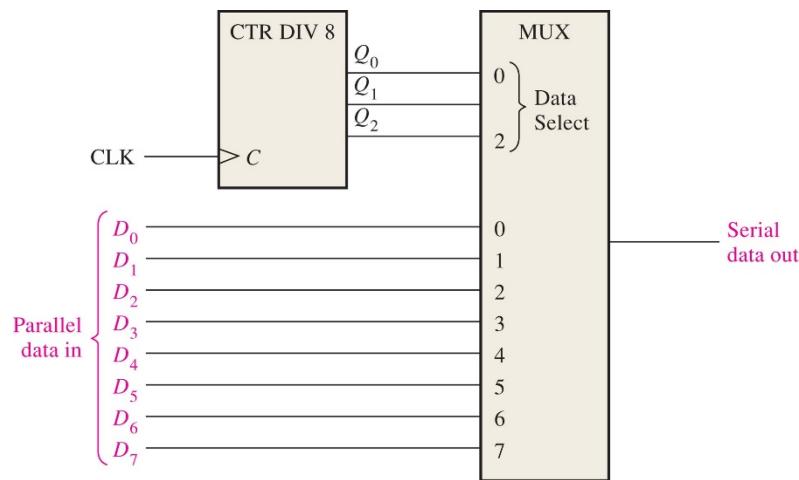
- Each time an automobile enters the garage, the counter is incremented by one
- When the 100th automobile enters, the counter goes to its last state (10010).

- The MAX/MIN output goes HIGH and activates the interface circuit, which lights the FULL sign and lowers the gate bar to prevent further entry.
- When an automobile exits, a sensor produces a positive pulse, which resets the S-R latch and puts the counter in the DOWN mode. The trailing edge of the clock decreases the count by one.



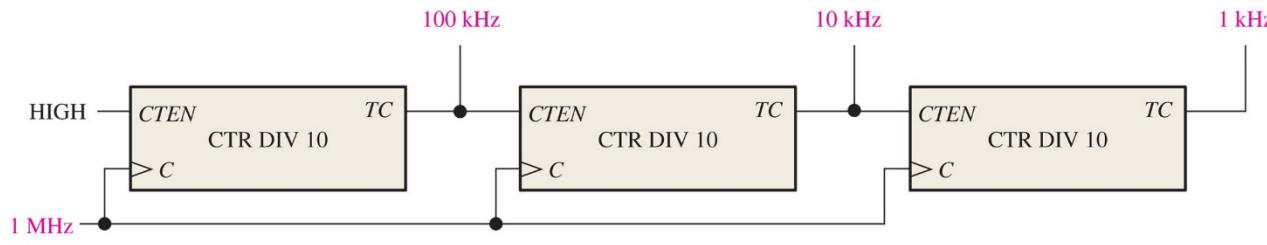
P/S Data Conversion (Multiplexing)

- The 1st byte of parallel data is applied to the multiplexer inputs. As the counter progresses from zero to seven, each bit, beginning with D₀, is sequentially selected and passed through the multiplexer to the output line.
- After eight clock pulses the data byte has been converted to a serial format and sent out on the transmission line.

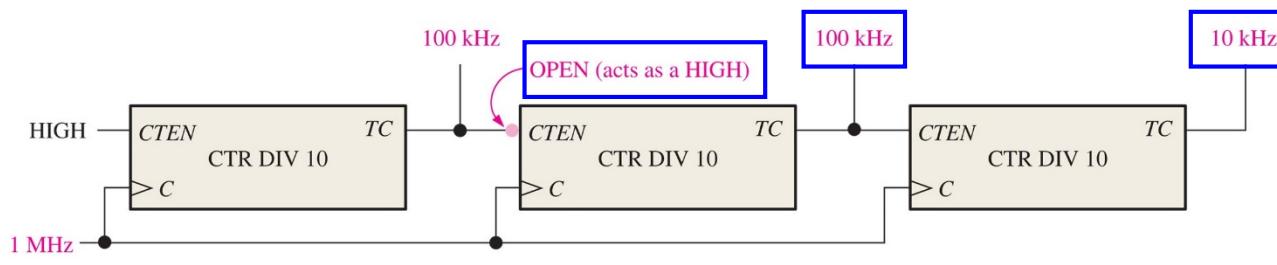


Troubleshooting

$$f_{\text{out}} = \frac{f_{\text{in}}}{\text{modulus}} = \frac{1\text{MHz}}{7232} \cong 138\text{Hz}$$

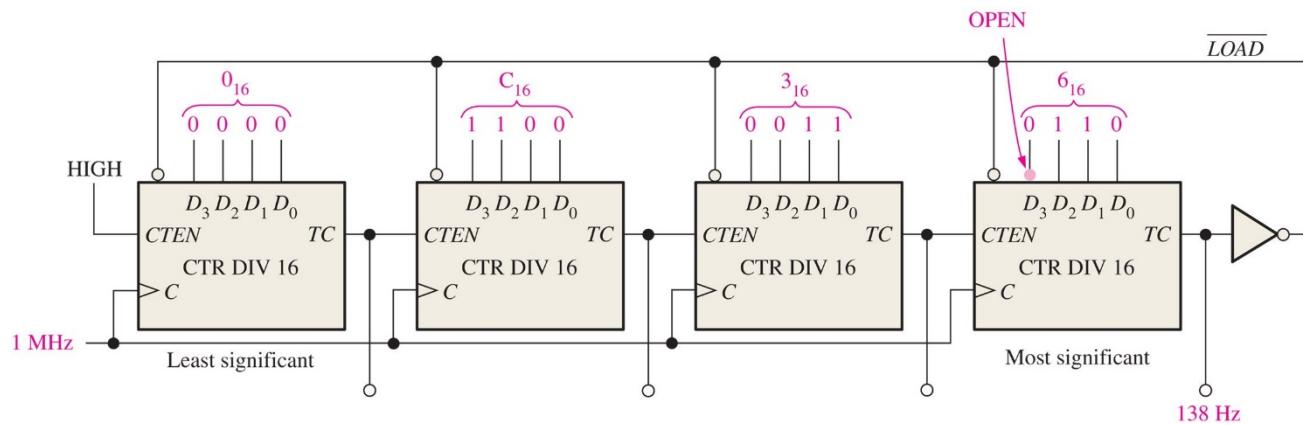


(a) Normal operation



(b) Count Enable (CTEN) input of second counter open

- The middle count enable input opens, it effectively acts as a HIGH → the counter is always enabled.

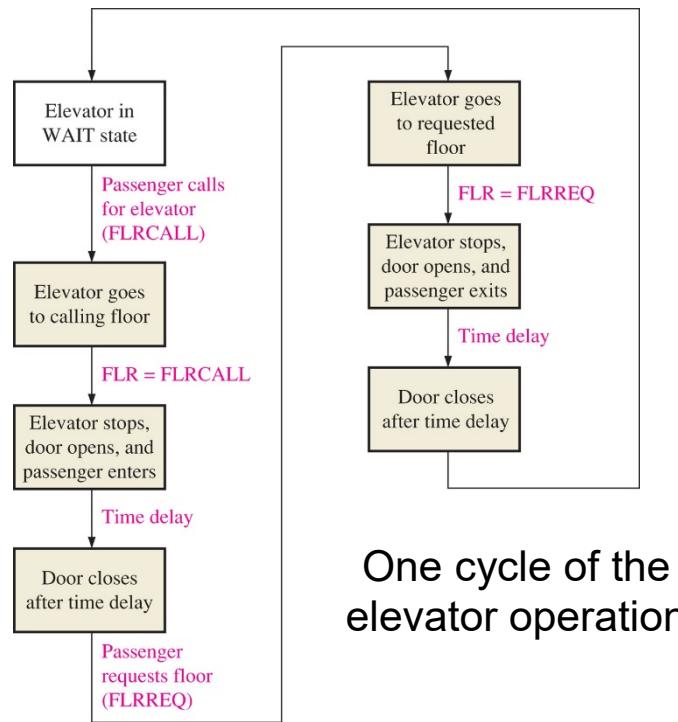


- Instead of 6_{16} (0110) being preset into the counter, E_{16} (1110) is preset in the most significant counter.

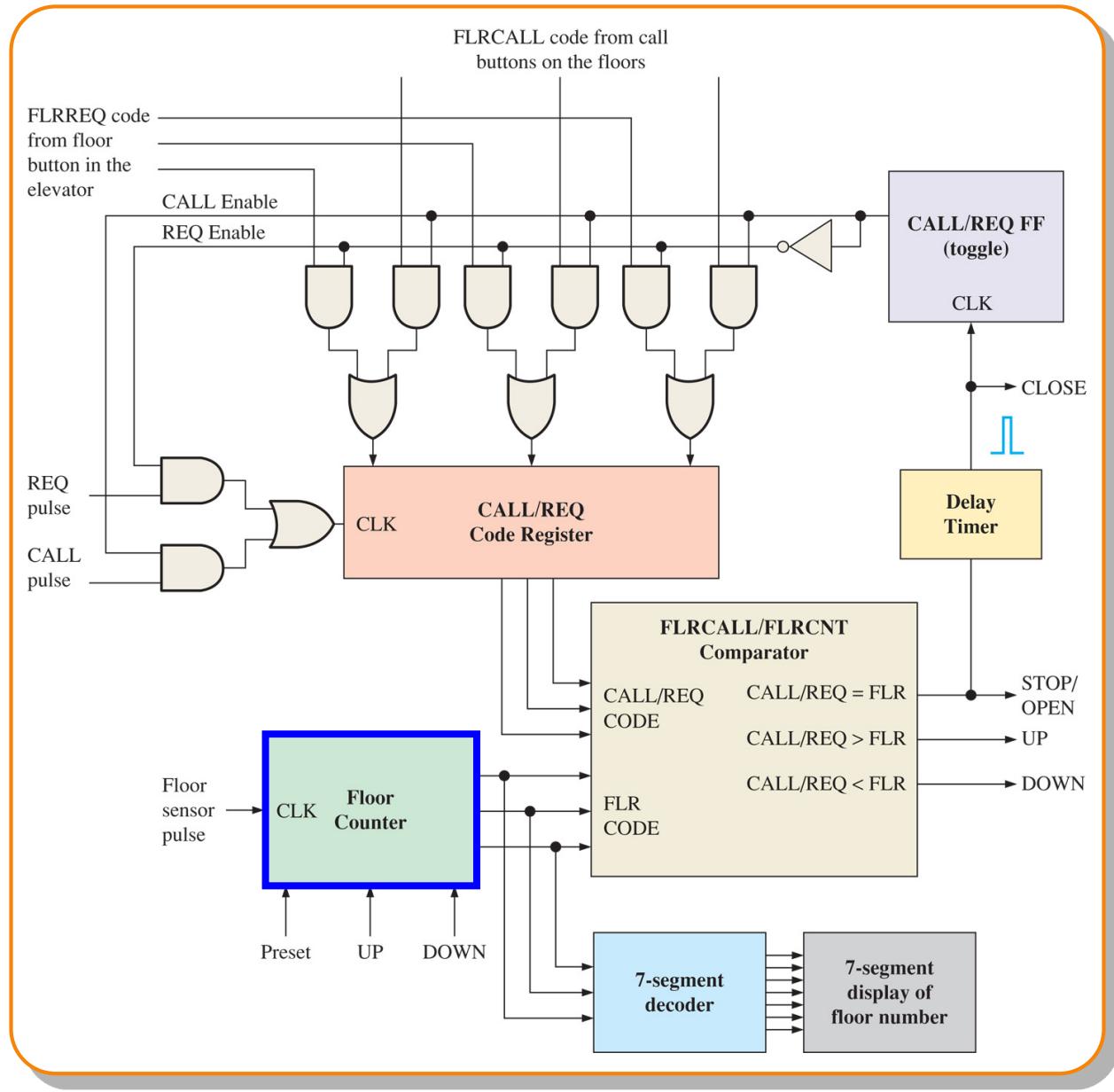
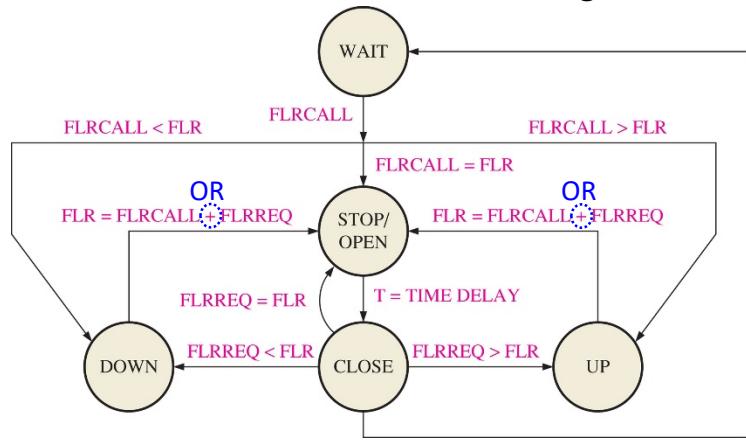
- Instead of beginning with $63C0_{16}$ ($25,536_{10}$) each time the counter recycles, the sequence will begin with $E3C0_{16}$ ($58,304_{10}$). The actual modulus becomes $65,536 - 58,304 = 7232$.



Applied Logic : Elevator Controller (Part 1)



Elevator controller state diagram



Chapter Review

□ Finite State Machines

- ◆ Moore machines
- ◆ Mealy machines

□ Counters

- ◆ Asynchronous
- ◆ Synchronous

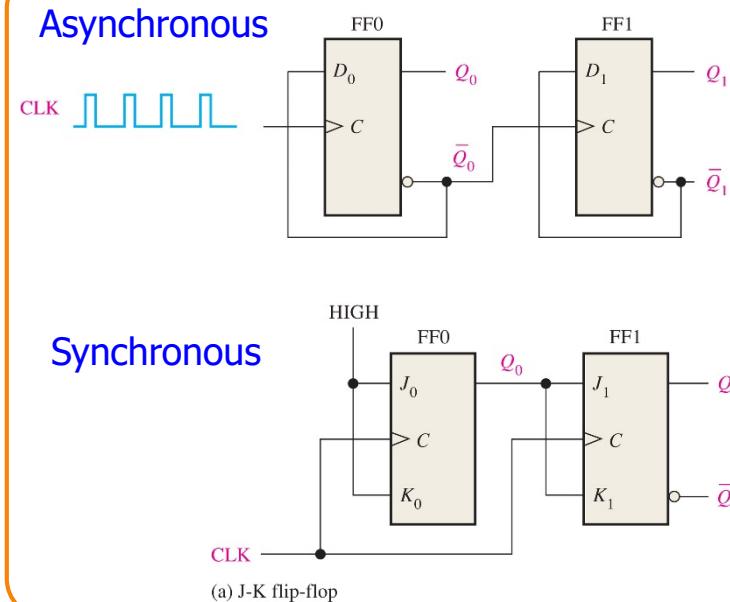
□ Up/Down Counters

□ Design of Synchronous Counters

□ Cascaded Counters

□ Counter Decoding

□ Troubleshooting



- Step 1: State Diagram
- Step 2: Next-State Table
- Step 3: Flip-Flop Transition Table
- Step 4: Karnaugh Maps
- Step 5: Logic Expressions for Flip-Flop Inputs
- Step 6: Counter Implementation



True/False Quiz

- A state machine is a sequential circuit having a limited number of states occurring in a prescribed order.
- Synchronous counters cannot be realized using J-K flip-flops.
- An asynchronous counter is also known as a ripple counter.
- A decade counter has twelve states.
- A counter with four stages has a maximum modulus of sixteen.
- To achieve a maximum modulus of 32, sixteen stages are required.
- If the present state is 1000, the next state of a 4-bit up/down counter in the DOWN mode is 0111.
- Two cascaded decade counters divide the clock frequency by 10.
- A counter with a truncated sequence has less than its maximum number of states.
- To achieve a modulus of 100, ten decade counters are required.



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