



EIE 2050 Digital Logic and Systems

Chapter 3 : Logic Gates

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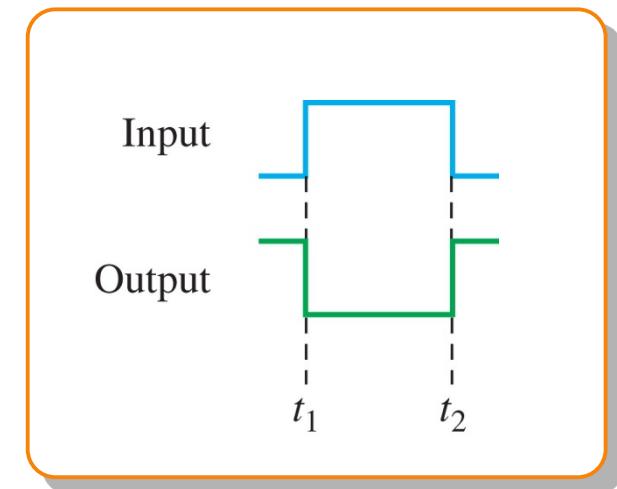
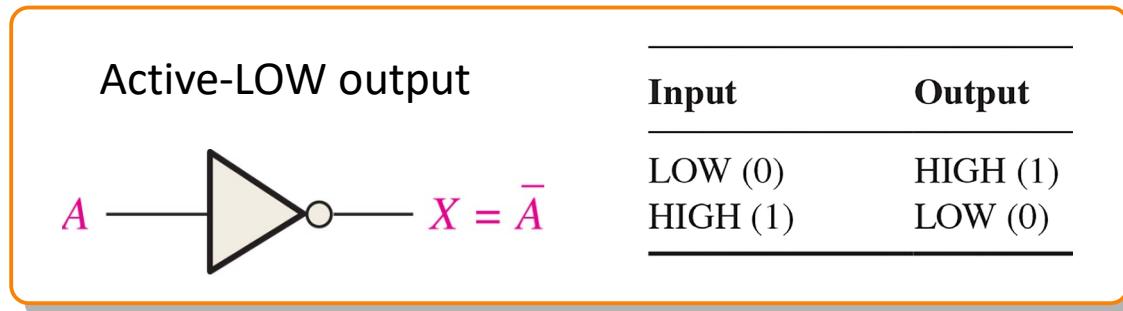
Last Week

- Binary, Decimal, Hexadecimal and Octal numbers
- Binary/Hexadecimal/Octal/Decimal Conversion
 - ◆ Binary/Hexadecimal/Octal-to-Decimal Conversion
 - ◆ Decimal-to-Binary/Hexadecimal/Octal Conversion: Repeated Division/Multiplication-by-2/16/8 (LSD → MSD)
- Most Significant Digit (MSD) and Least Significant Digit (LSD)
- Floating-Point numbers: Mantissa and (biased) Exponent
- Binary Arithmetic
 - ◆ Addition, Subtraction, Multiplication and Division
 - ◆ Unsigned versus Signed numbers
- Binary coded decimal (BCD)
- Digital codes: Gray/Alphanumeric/Error Codes



The Inverter

- Generally, inputs on the left and the output on the right.
- Truth Table shows the output for each possible input in terms of levels and corresponding bits.



- Timing diagrams : a graph that displays the relationship of two or more waveforms with respect to each other on a time basis
- Logic Expression: The complement of a variable designated by a bar over the letter $X = \bar{A}$



The AND Gate

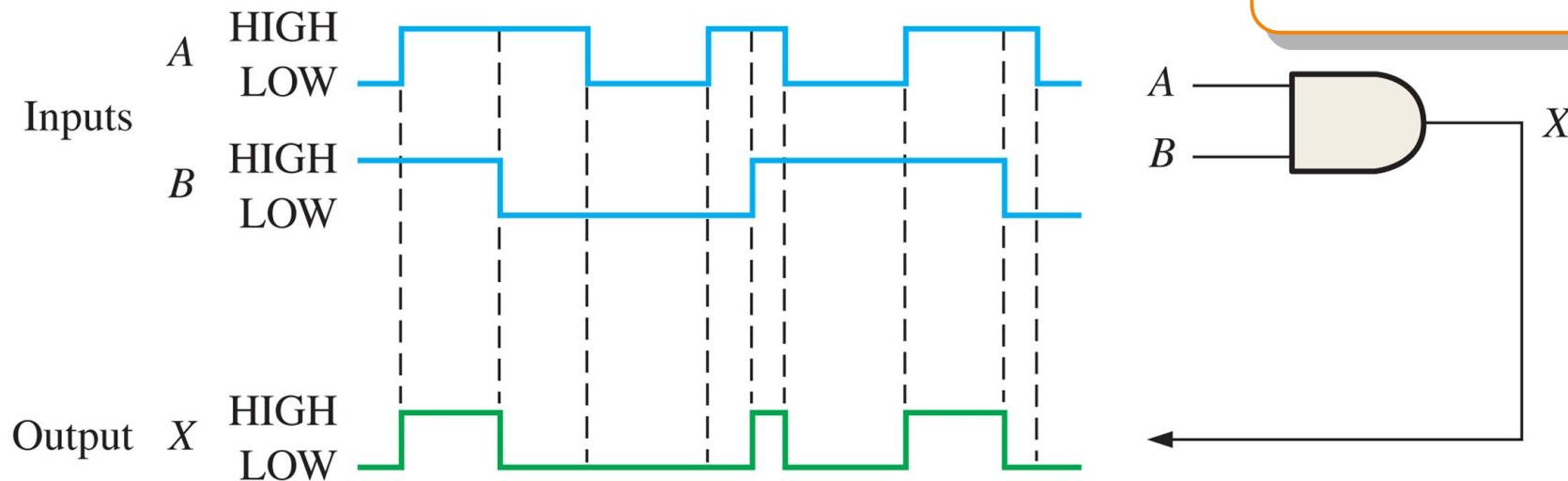
Distinctive Shape



- An AND gate can have any number of inputs greater than one
- Truth table: for n input variables, the total number of possible output is $N=2^n$
- Timing diagram
- Logic Expression $X = A B$

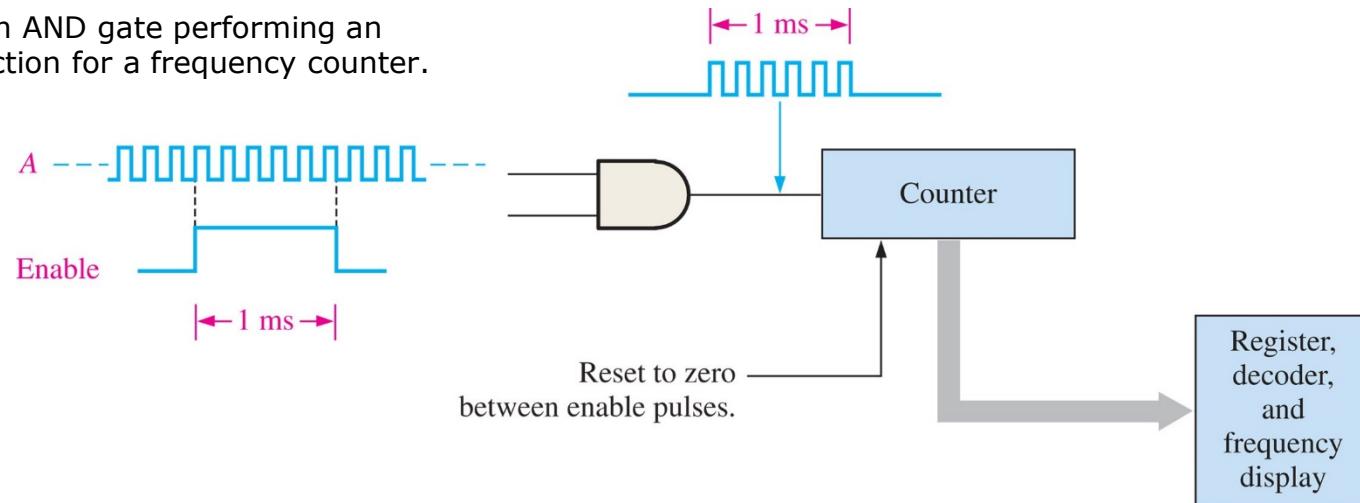
Truth Table for a 2-input AND gate

A	B	$AB = X$
0	0	$0 \cdot 0 = 0$
0	1	$0 \cdot 1 = 0$
1	0	$1 \cdot 0 = 0$
1	1	$1 \cdot 1 = 1$



The AND Gate : Applications

FIGURE 3-16 An AND gate performing an enable/inhibit function for a frequency counter.



HIGH = On
LOW = Off

HIGH = Unbuckled
LOW = Buckled

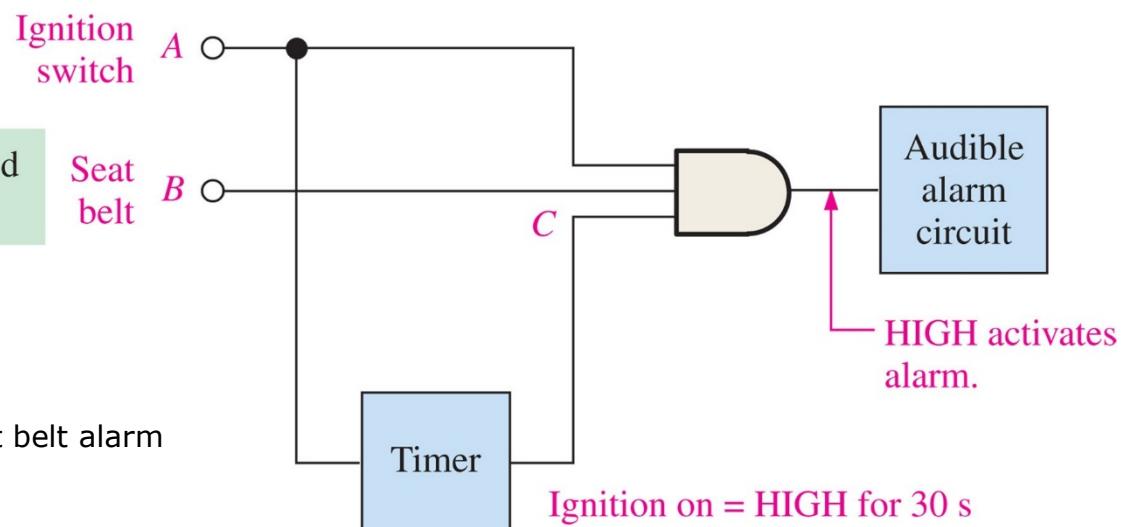
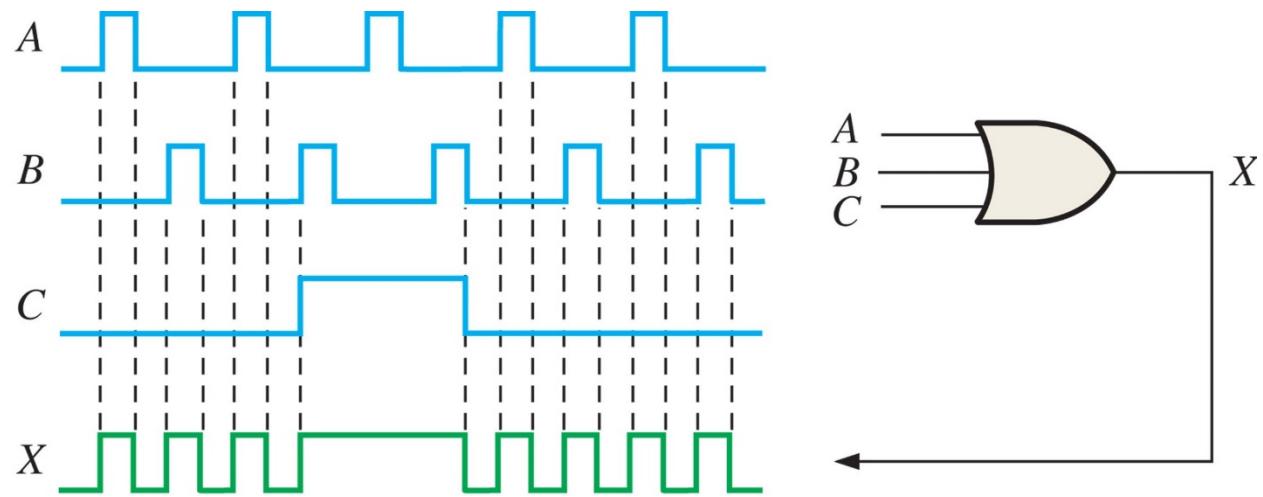


FIGURE 3-17 A simple seat belt alarm circuit using an AND gate.



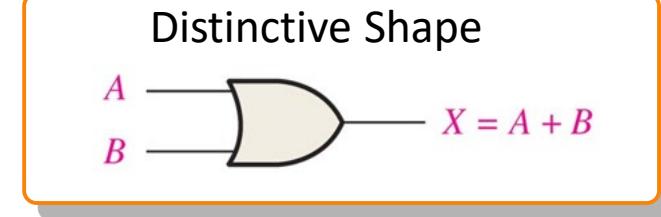
The OR Gate

- An OR gate can have any number of inputs greater than one
- Timing diagram



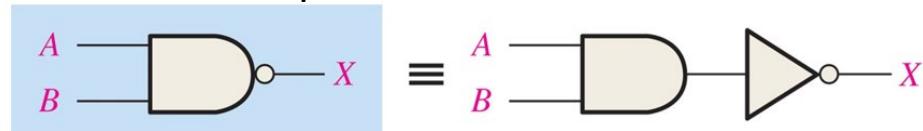
- Logic Expression $X = A + B$

A	B	$A + B = X$
0	0	$0 + 0 = 0$
0	1	$0 + 1 = 1$
1	0	$1 + 0 = 1$
1	1	$1 + 1 = 1$

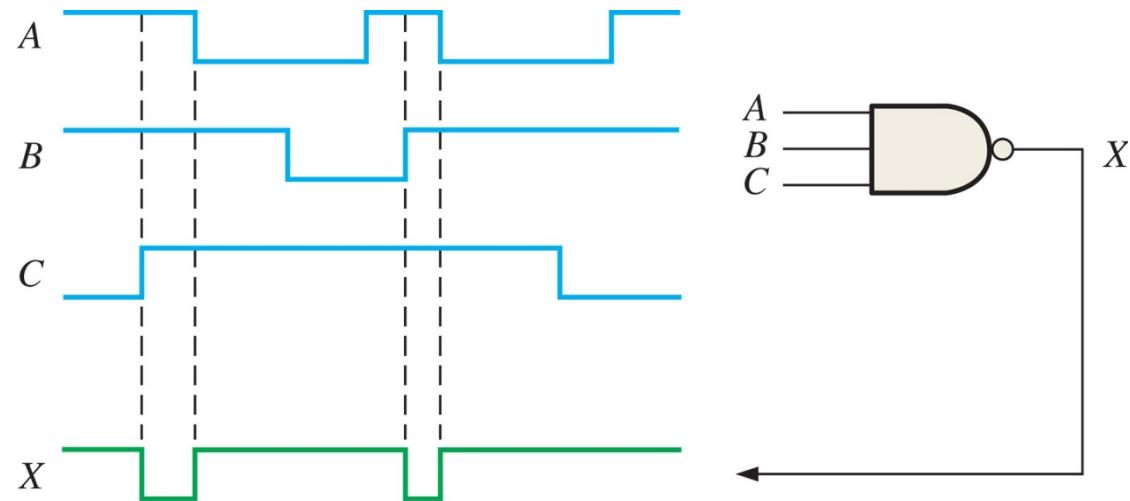


The NAND Gate

Distinctive Shape

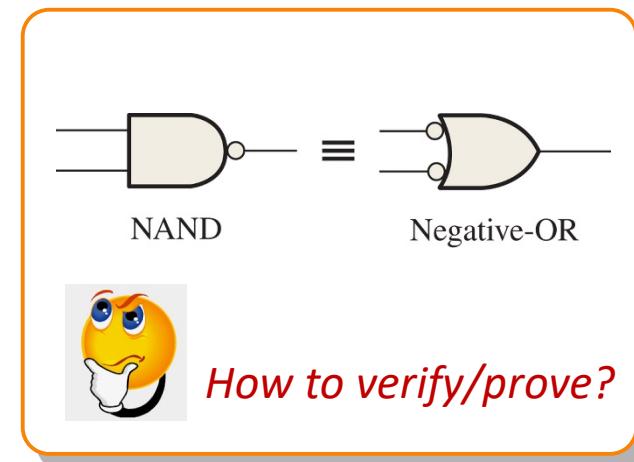


- An NAND gate can have any number of inputs greater than one
- Timing diagram



- Logic Expression $X = \overline{AB} = \overline{A} + \overline{B}$

A	B	$\overline{AB} = X$
0	0	$\overline{0 \cdot 0} = \overline{0} = 1$
0	1	$\overline{0 \cdot 1} = \overline{0} = 1$
1	0	$\overline{1 \cdot 0} = \overline{0} = 1$
1	1	$\overline{1 \cdot 1} = \overline{1} = 0$



The NAND Gate : Applications

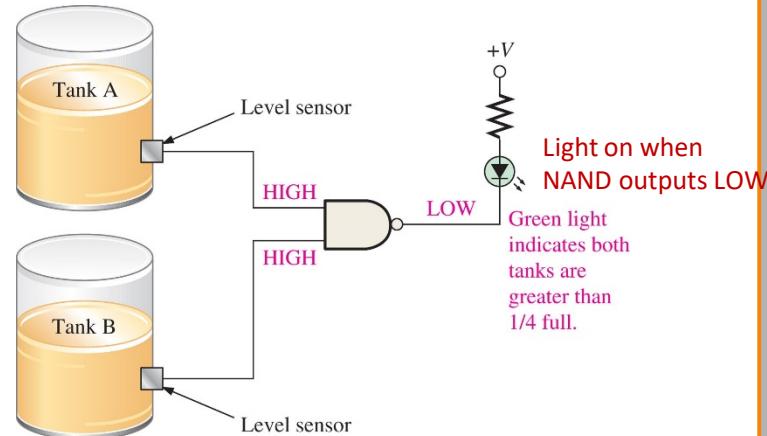


Can we switch the two lights?

- The sensors produce HIGH when the tanks are more than 1/4 full. Otherwise, the sensor outputs LOW.

EXAMPLE 3–12

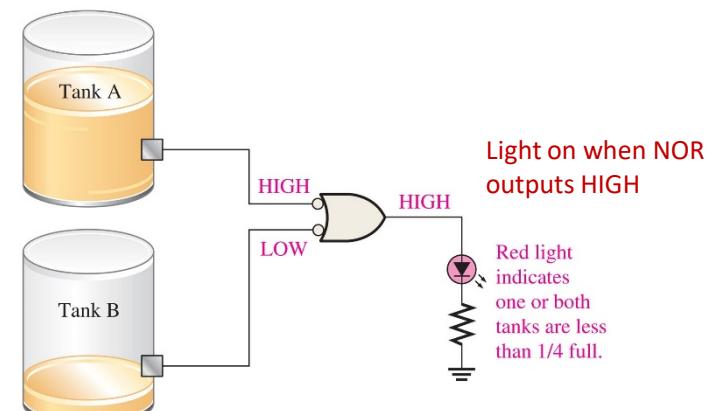
Goal: turn the **green** light when **both** tanks are **more** than 1/4 full



A	B	Output
1	1	0
1	0	1
0	1	1
0	0	1

EXAMPLE 3–13

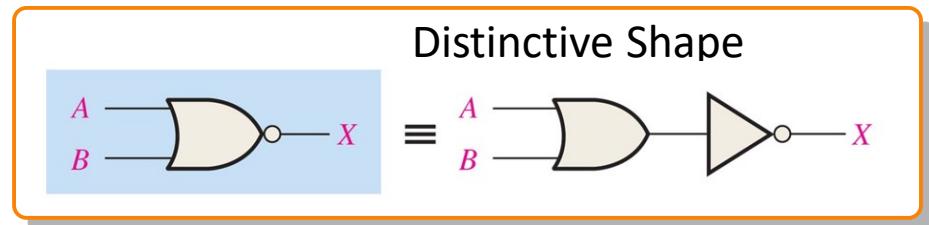
Goal: turn the **red** light on when **one** or **both** tanks are **less** than 1/4 full



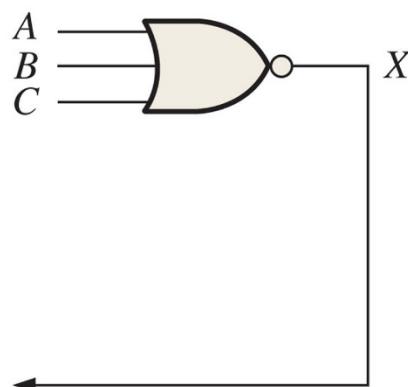
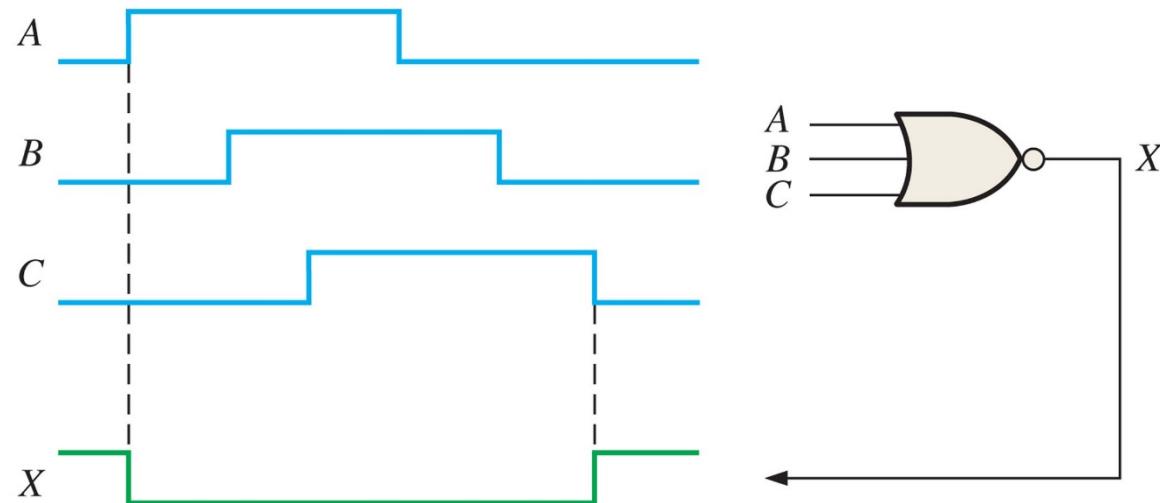
A	B	Output
1	1	0
1	0	1
0	1	1
0	0	1



The NOR Gate



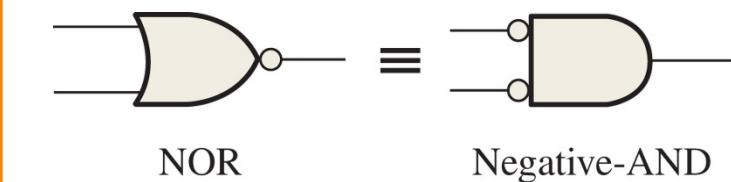
- An OR gate can have any number of inputs greater than one
- Timing diagram



Truth Table for a 2-input OR gate

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

- Logic Expression $X = \overline{A + B} = \overline{A}\overline{B}$



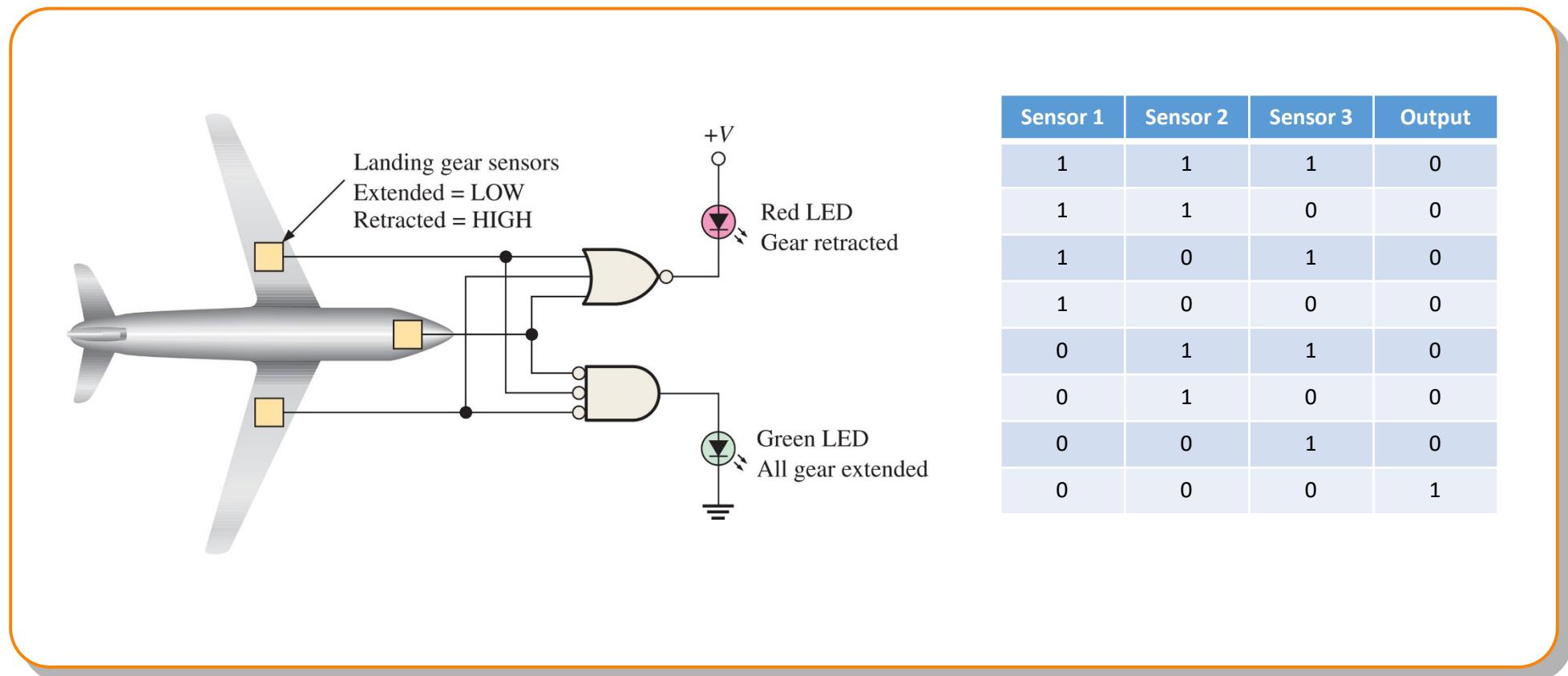
How to verify/prove?



The NOR Gate : Application

$$X = \overline{A + B} = \overline{A}\overline{B}$$

- When a landing gear is extended, its sensor produces LOW
- When a landing gear is retracted, its sensor produces HIGH
- Goal : To turn on a red LED on if any of the gear fails to extend



The Exclusive-OR and Exclusive-NOR Gates

□ XOR Gates

Distinctive Shape



Truth Table for a 2-input XOR gate

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

An XOR gate used to add two bits.

Input Bits Output (Sum)

A B Σ

0 0 0

0 1 1

1 0 1

1 1 0 (without the 1 carry bit)

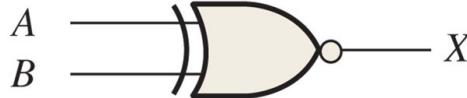


香港中文大學(深圳)

The Chinese University of Hong Kong, Shenzhen

□ XNOR Gates

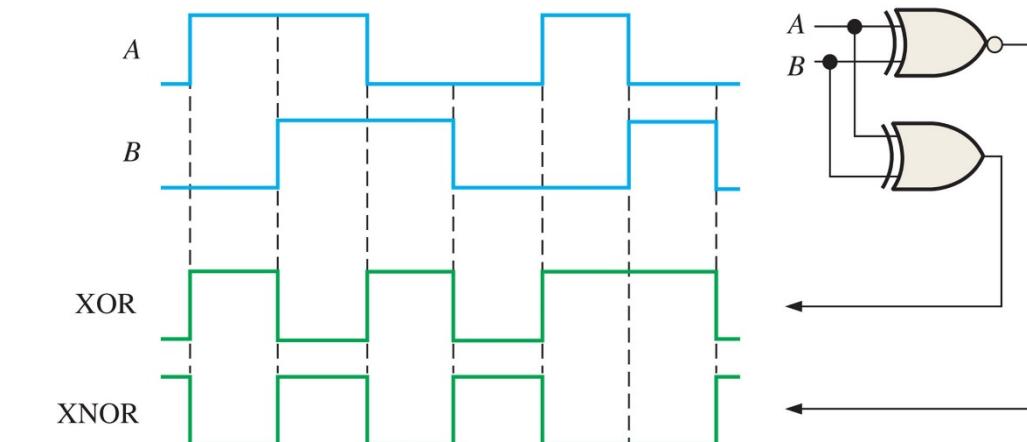
Distinctive Shape



Truth Table for a 2-input XNOR gate

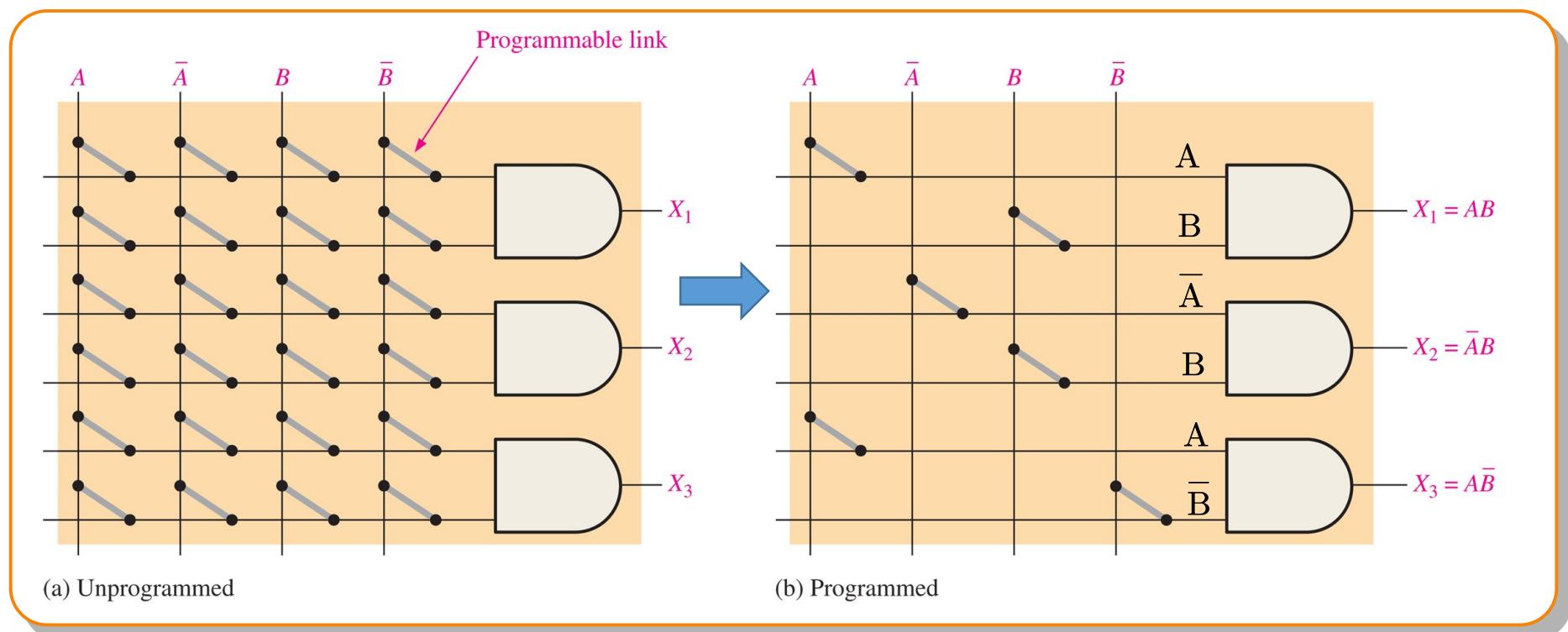
Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

EXAMPLE 3-21



Programmable Logic

- Most types of programmable logic devices (PLDs) use some form of AND array.
- An AND array consists of AND gates and a matrix of interconnections
- For each input to an AND gate, only one programmable link is left intact in order to connect the desired variable to the gate input



Programmable Link Process Technologies

FIGURE 3-51 The programmable **fuse** link.

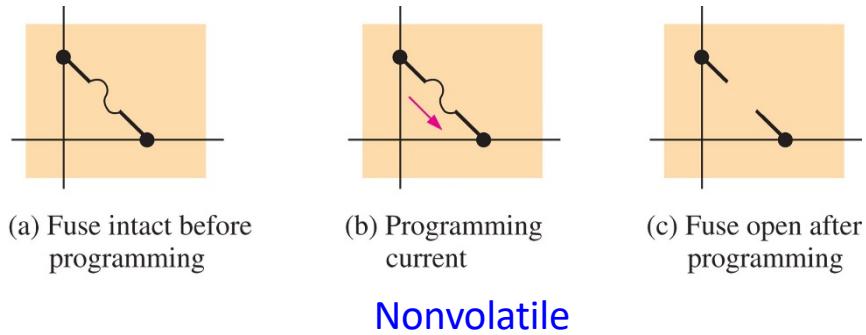


FIGURE 3-52 The programmable **antifuse** link.

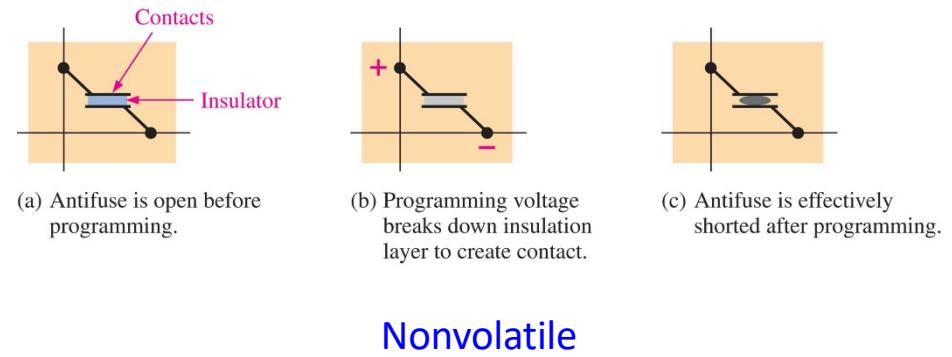


FIGURE 3-53 A simple AND array with **EPROM** technology. Only one gate in the array is shown for simplicity.

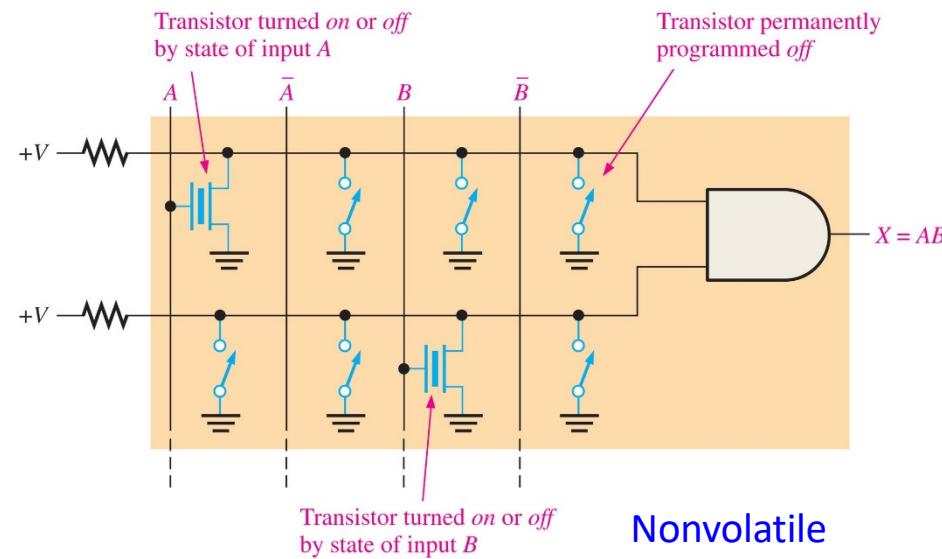
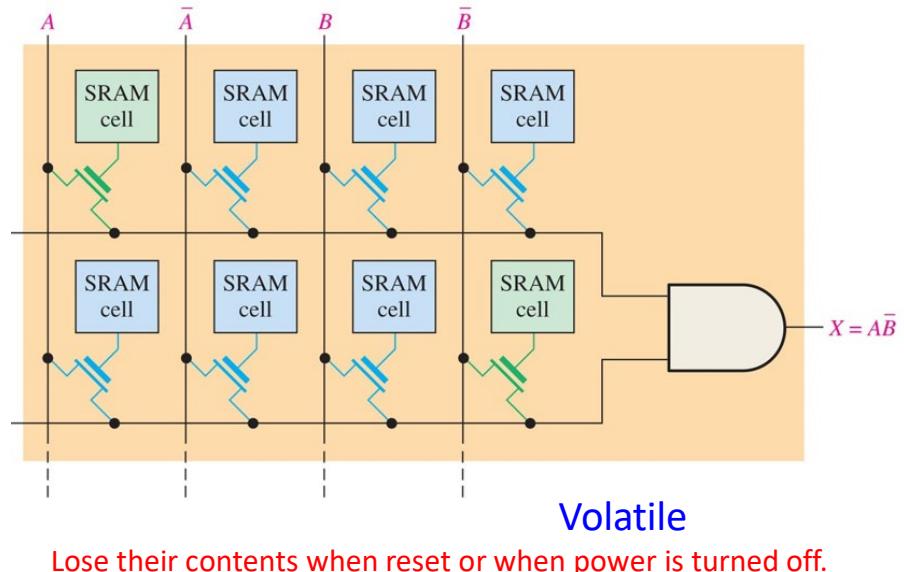


FIGURE 3-54 Concept of an AND array with **SRAM** technology.



Fixed-Function Logic Gates :74 Series

□ AND Gate

- ◆ The 74xx08/11/21 is a quad 2/3/4-input AND gate device

□ NAND Gate

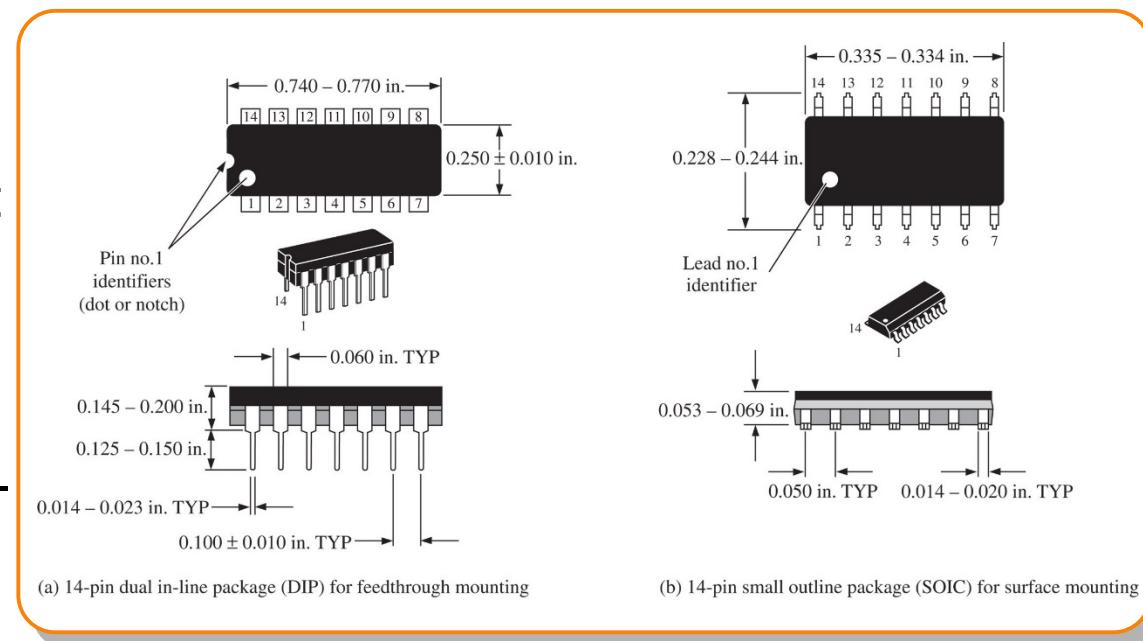
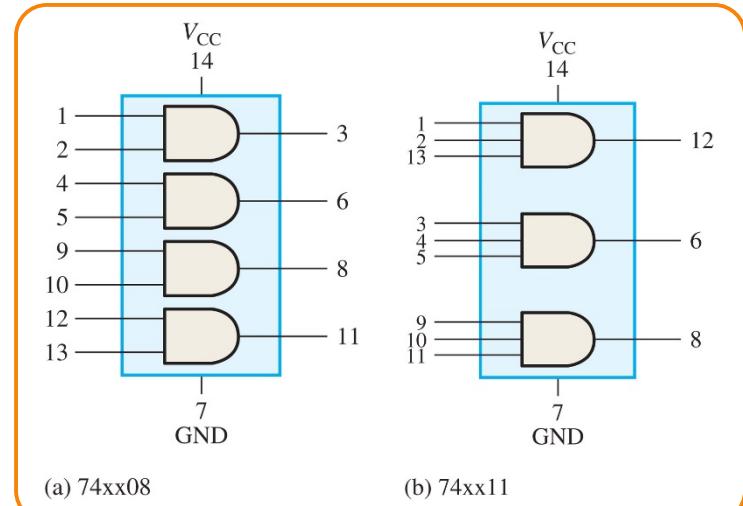
- ◆ The 74xx00/10/20/30 is a quad 2/3/4/8-input NAND gate device

□ OR Gate

- ◆ The 74xx32 is a quad 2-input OR gate device.

□ NOR Gate

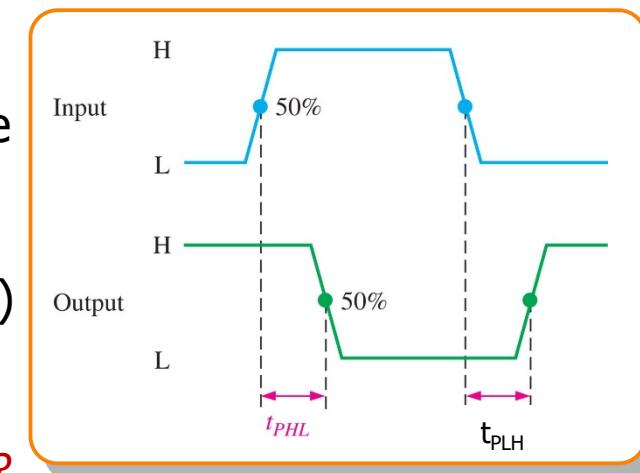
- ◆ The 74xx02/27 is a quad 2/3-input NOR gate device



Performance Characteristics & Parameters (I)

□ Propagation Delay Time

- ◆ Time interval btw the transition of an input pulse and the occurrence of the resulting output pulse
- ◆ t_{PHL} (t_{PLH}): Output changes: HIGH (LOW) \rightarrow LOW (HIGH)
- ◆ Typical Propagation Delay Time is on the order of ns (nano-second, i.e. 10^{-9} s) *How fast the circuit can operate?*



□ DC Supply Voltage (V_{CC})

- ◆ Typical DC supply voltage for CMOS logic is either 5 V, 3.3 V, 2.5 V, or 1.8 V,

□ Power Dissipation

- ◆ The supply current when the gate output is LOW is greater than when the gate output is HIGH.
- ◆ Assuming a 50% duty cycle (output LOW and HIGH half the time each), the average power dissipation

$$P_D = V_{CC} \left(\frac{I_{CCH} + I_{CCL}}{2} \right)$$

I_{CCH} : The supply current for the HIGH output state

I_{CCL} : The supply current for the LOW output state



Performance Characteristics & Parameters (II)

- Input and Output Logic Levels
- Speed-Power Product (SPP)
 - ◆ A measure of the performance of a logic circuit taking into account the propagation delay time and the power dissipation.
 - ◆ $SPP = t_p P_D$

EXAMPLE 3-24

A certain gate has a propagation delay of 5 ns and $I_{CCH} = 1 \text{ mA}$ and $I_{CCL} = 2.5 \text{ mA}$ with a dc supply voltage of 5 V. Determine the speed-power product.

Solution

$$P_D = V_{CC} \left(\frac{I_{CCH} + I_{CCL}}{2} \right) = 5 \text{ V} \left(\frac{1 \text{ mA} + 2.5 \text{ mA}}{2} \right) = 5 \text{ V}(1.75 \text{ mA}) = 8.75 \text{ mW}$$

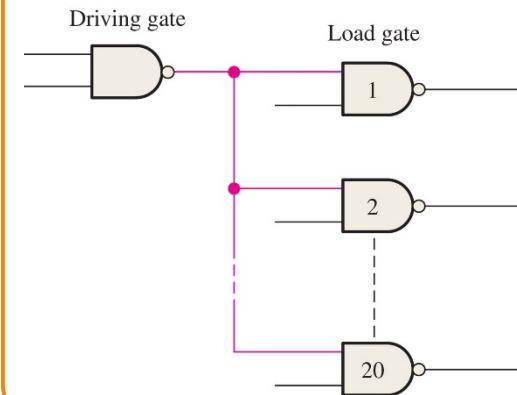
$$SPP = (5 \text{ ns})(8.75 \text{ mW}) = 43.75 \text{ pJ}$$

□ Fan-Out and Loading

- ◆ Fan-out : the maximum # of inputs can be connected to a gate's output and still maintain the output voltage levels within specified limits.
- ◆ Fan-out is specified in terms of **unit loads**

$$\text{Unit loads} = \frac{I_{OL}}{I_{IL}} = \frac{8.0 \text{ mA}}{0.4 \text{ mA}} = 20$$

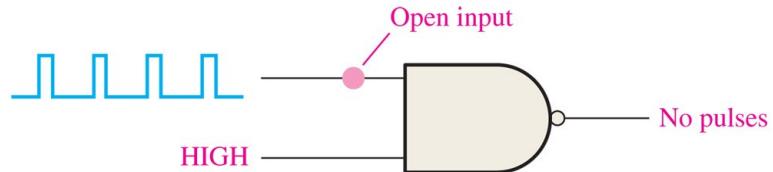
FIGURE 3-68 The LS family NAND gate output fans out to a max. of 20 LS family gate inputs.



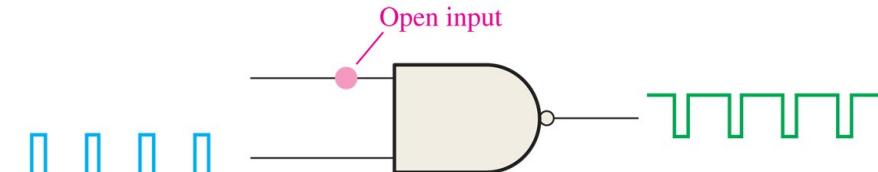
A	B	$\overline{AB} = X$
0	0	$\overline{0 \cdot 0} = \overline{0} = 1$
0	1	$\overline{0 \cdot 1} = \overline{0} = 1$
1	0	$\overline{1 \cdot 0} = \overline{0} = 1$
1	1	$\overline{1 \cdot 1} = \overline{1} = 0$

Troubleshooting: Internal Failures

Effects of an Internally Open Input



(a) Application of pulses to the open input will produce no pulses on the output.



(b) Application of pulses to the good input will produce output pulses for bipolar NAND and AND gates because an open input typically acts as a HIGH. It is uncertain for CMOS.

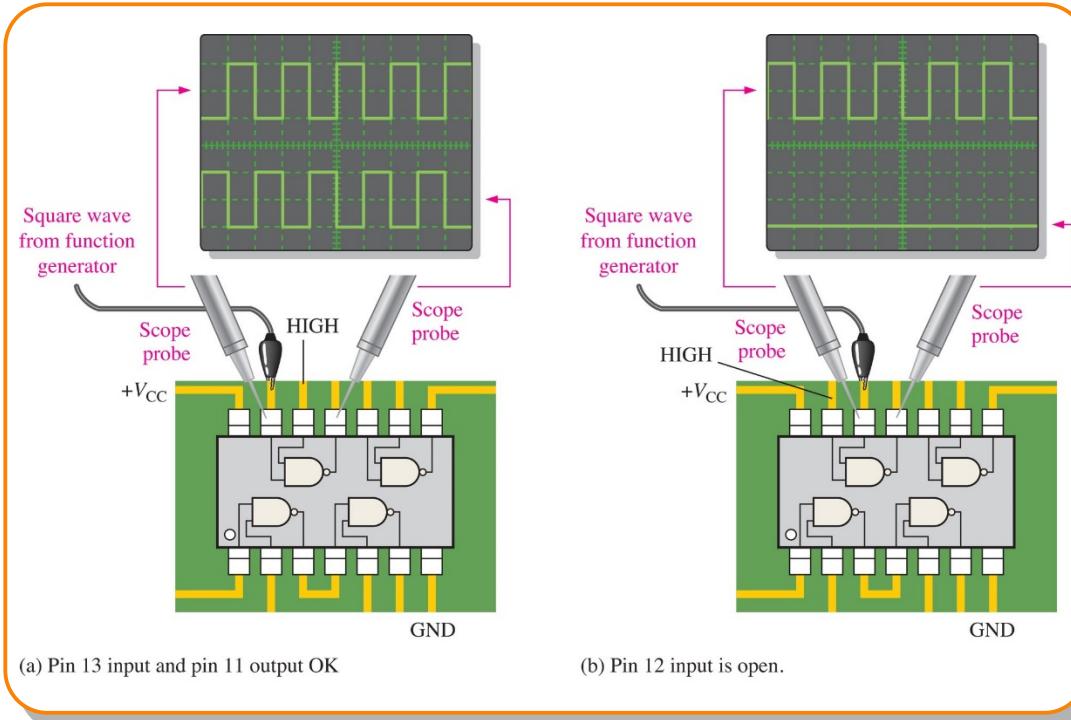
Conditions for Testing Gates

- When testing NAND or AND gates, the inputs that are not being pulsed should be HIGH *Why?*



Troubleshooting an Open Input

- Step (a): Pin 13 and 11 ✓
- Step (b): Pin 12 ✗



Troubleshooting: Internal Failures

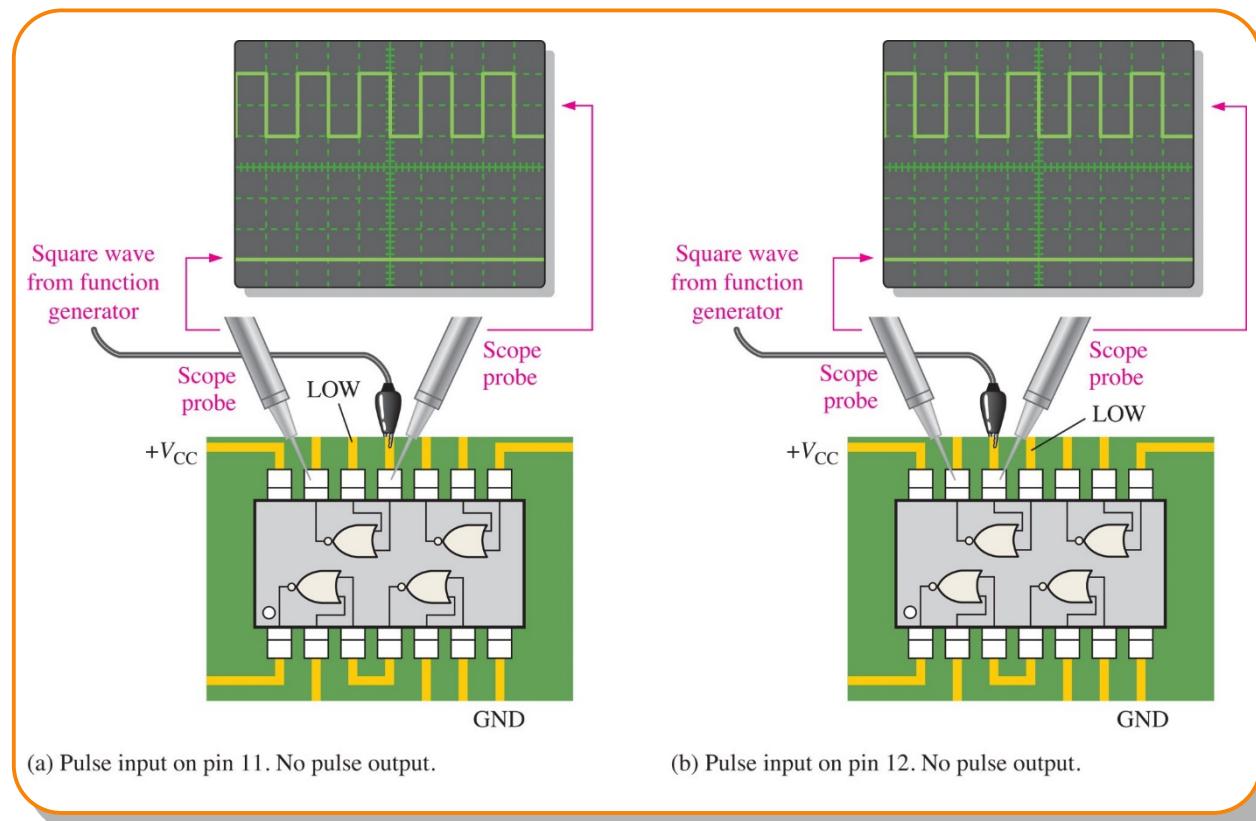
- Effects of an Internally Open Output
 - ◆ No signal getting to the output
- Troubleshooting an Open Output
 - ◆ No pulse waveform at the output regardless of the input
- Shorted Input or Output
 - ◆ Input (output) are shorted



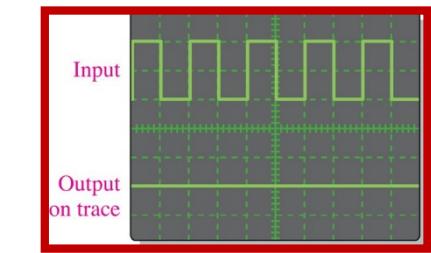
What will the truth table look like ?

Truth table for XOR

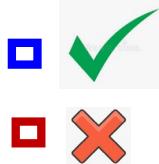
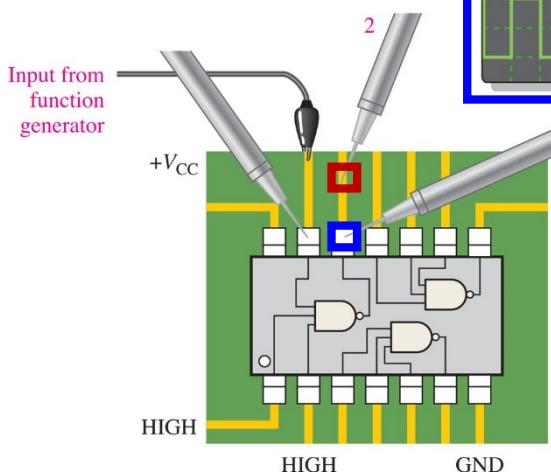
Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0



Troubleshooting: External Opens and Shorts



Example 3-25



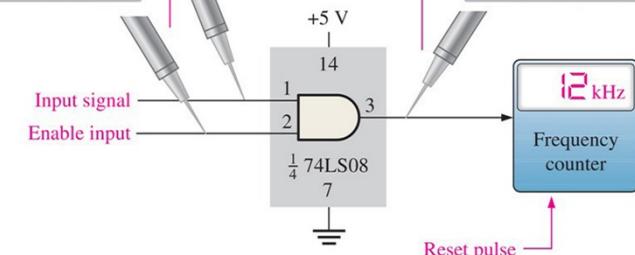
Bad contact
or solder
connection

Pin 13 input 1 → output 0; otherwise, output 1



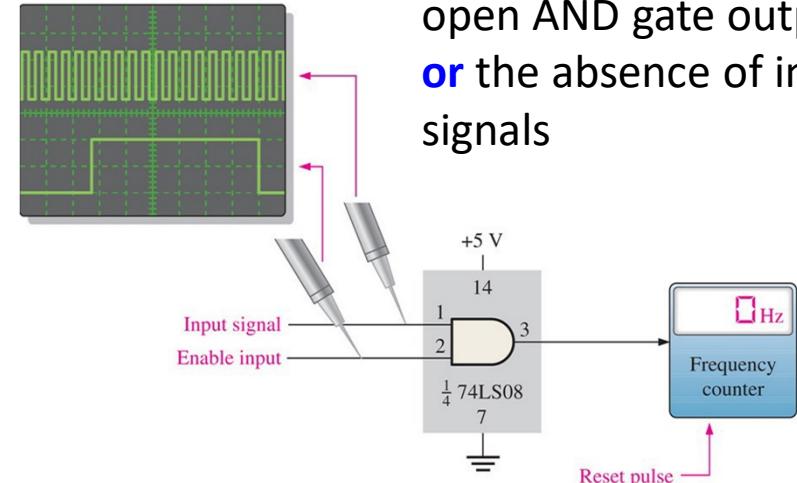
How can you perform further diagnosis?

Example 3-26



(a) The counter is working properly.

Possible problem: an open AND gate output
or the absence of input
signals

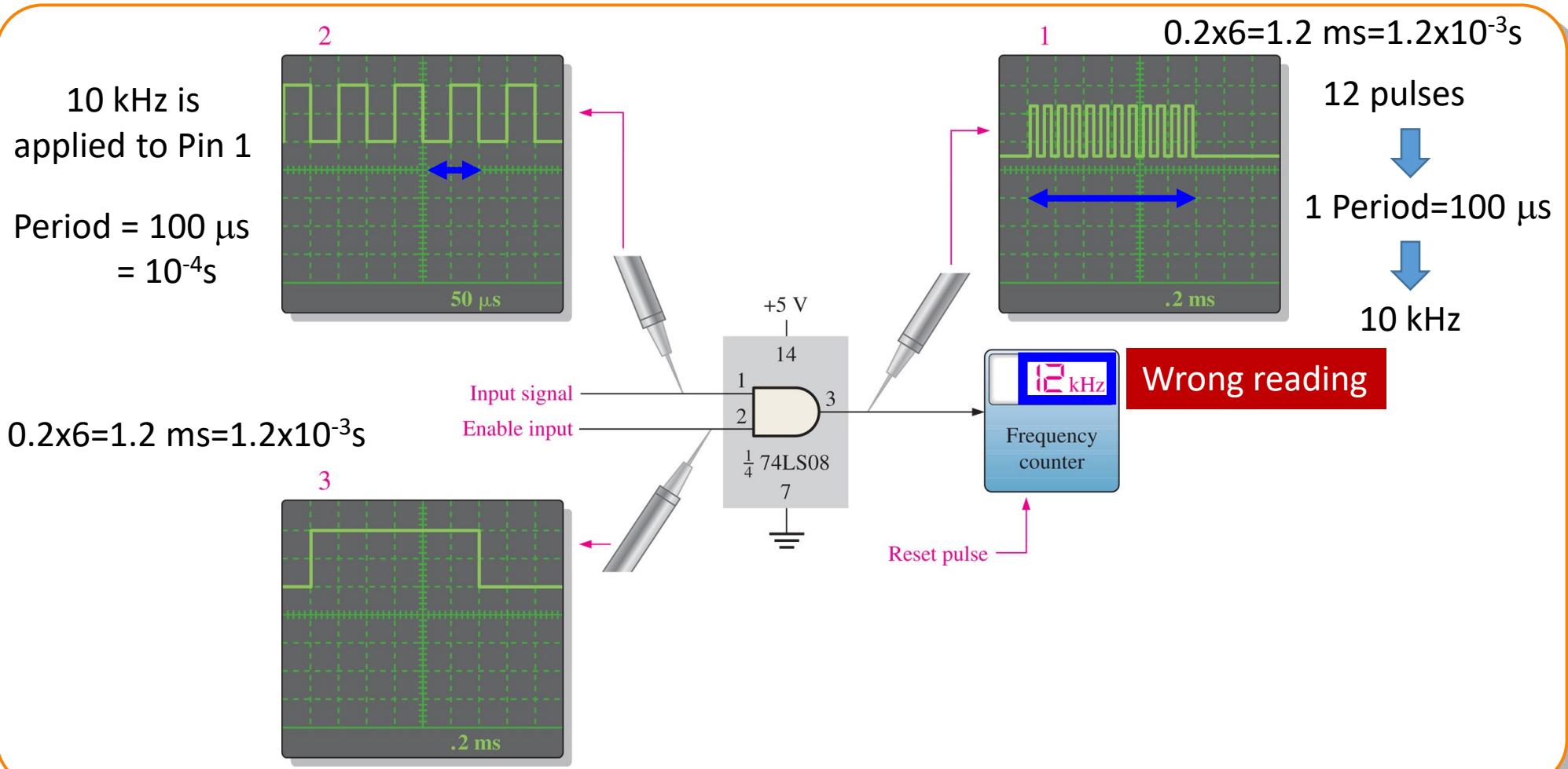


(b) The counter is not measuring a frequency.



Troubleshooting: External Opens and Shorts

Example 3-27 : The frequency counter shown in Figure 3–74 appears to measure the frequency of input signals incorrectly. It is found that when a signal with a precisely known frequency is applied to pin 1 of the AND gate, the oscilloscope display indicates a higher frequency. Determine what is wrong. The readings on the screen indicate time per division.



Chapter Review

□ Logic gates

- ◆ Inverter, AND, OR, NAND, NOR, XOR, XNOR
- ◆ Truth Tables, Distinctive Shape Symbols

□ Performance Characteristics and Parameters

- ◆ Propagation Delay Time
- ◆ DC Supply Voltage
- ◆ Power Dissipation
- ◆ Input and Output Logic Levels
- ◆ Speed-Power Product (SPP)
- ◆ Fan-Out and Loading

□ Troubleshooting

- ◆ Internal Failures of IC Logic Gates
- ◆ External Opens and Shorts



True/False Quiz

- An inverter performs a NOT operation.
- A NOT gate cannot have more than one input.
- If any input to an OR gate is zero, the output is zero.
- If all inputs to an AND gate are 1, the output is 0.
- A NAND gate can be considered as an AND gate followed by a NOT gate.
- A NOR gate can be considered as an OR gate followed by an inverter.
- The output of an exclusive-OR is 0 if the inputs are opposite.
- Two types of fixed-function logic integrated circuits are bipolar and NMOS.
- Once programmed, PLD logic can be changed.
- Fan-out is the number of similar gates that a given gate can drive.



True/False Quiz



An inverter performs a NOT operation.



A NOT gate cannot have more than one input.



If any input to an OR gate is zero, the output is zero.



If all inputs to an AND gate are 1, the output is 0.



A NAND gate can be considered as an AND gate followed by a NOT gate.



A NOR gate can be considered as an OR gate followed by an inverter.



The output of an exclusive-OR is 0 if the inputs are opposite.



Two types of fixed-function logic integrated circuits are bipolar and NMOS.



Once programmed, PLD logic can be changed.



Fan-out is the number of similar gates that a given gate can drive.

