Device Reliability Report

First Quarter 2007

UG116 (v4.0) June 4, 2007

XILINX®

Revision History

Device Reliability Report
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The following table shows the revision history for this document..

Date	Version	Revision
02/09/04	1.0	Initial release in new template.
05/10/04	2.0	First quarter 2004 revision.
05/24/04	2.1	Changed fit rate on page 7 for 0.5 µm from 89 to 8.
05/24/04	2.2	Changes to Tables 1-1, 2-1, 2-15, 3-44, 3-46, 3-48, 3-50, and 3-52; also a heading on page 75.
08/18/04	2.3	Added second quarter data.
01/04/05	2.4	Added third quarter data.
03/01/05	2.5	Changes in most tables to show the fourth-quarter test values. Removed packaging information from Chapter 1 and added a reference to the packaging website.
05/20/05	2.6	Data corrections in tables 2-61 and 3-32.

Date	Version	Revision
08/19/05	2.7	Changes in most tables to show the second-quarter test values.
11/17/05	2.8	Updates most tables to include the third-quarter test data.
02/24/06	2.9	Most tables updated to reflect the fourth-quarter test data.
05/05/06	3.0	Changes in most tables to show the first-quarter test data.
06/20/06	3.0.1	Corrected two transposed figures in Table 1-10.
08/11/06	3.1	Changes in most tables to show the second-quarter test data.
08/29/06	3.1.1	Changed typos in tables 2-91, 3-44, and 3-55.
10/06/06	3.1.2	Corrected values in tables 1-12, 2-87, 2-90, and 2-91.
12/01/06	3.2	Changes in most tables to show the third-quarter test data.
02/12/07	3.3	Changes in most tables to show the fourth-quarter test data.
02/20/07	3.3.1	Correct typos in three tables.
03/28/07	3.3.2	Correct typos in four tables.
06/04/07	4.0	Changes in most tables to show the first-quarter test data.

Table of Contents

Chapter 1: The Reliability Program

Chapter 2: Results by Product Family

Chapter 3: Results by Package Type

Chapter 1

The Reliability Program

Overview

This report is published by Xilinx to provide insight to our customers regarding the reliability of Xilinx products. Reliability is defined as product performance to specification over time in response to varied (specified) environmental stress conditions. The ultimate goal of our reliability program is to achieve continuous improvement in the robustness of the product being evaluated.

As part of this program, finished product reliability is measured periodically to ensure that the product performance meets or exceeds internal and external reliability specifications. Reliability programs are executed in response to internal programs as well as to individual customer requirements. All tests are performed or supervised by experienced Xilinx employees using facilities that are approved and audited by Xilinx for compliance to the requirements of DSCC and MIL-STD-883.

The Reliability Program: The reliability qualifications of new devices, wafer processes, and packages are designed to ensure that these Xilinx products satisfy the internal and external customer requirements before transfer into production. The reliability qualification and monitor requirements are outlined in the following tables. The reliability stress tests are conducted according to the conditions specified in JEDEC Solid State Technology Association' s reliability test methods for packaged devices, JESD22, except Group B and D tests in which it follows DSCC's test methods, MIL-STD-883.

Product Qualification

Wafer Process

The wafer process qualification is illustrated in Table 1-1.

Table 1-1: **Wafer Process Qualification**

Reliability Test	Condition	Duration	Lot Qty	SS/lot(1)	Acceptance
High Temperature Operating Life (HTOL)	$T_j \geq 125°C$, V_{DD} Max	1,000 hours	3	77	200FIT(2) 50 FIT
Temperature Humidity Bias (THB) or High Accelerated Stress Test (HAST)	85°C, 85% R.H., V_{DD}, 130°C, 85% R.H., V_{DD}, 110°C, 85% R.H., V_{DD}	1,000 hours, 100 hours, 264 hours	2	77	0 fail
Temperature Cycling (TC)(3)	-65°C/+150°C, -55°C/+125°C, -40°C/+125°C	500 cycles, 1,000 cycles, 1,000 cycles	1	77	0 fail
Data Retention Bake(4)	T_A = 150°C	1,000 hours	1	77	0 fail
High Temperature Storage Life (HTS)					
Program Erase(5)	T_A = 25°C	10,000 cycles	1	32	0 fail

Notes:

1. The sample size guideline listed is based on the die size 237 mm^2. For bigger die size, the sample size may be reduced to 36 or 22.
2. Phase I production is released as the qualification data demonstrates, meeting 200 FIT failure rate and other test requirements. Phase II production is released as the qualification data demonstrates, meeting 50 FIT failure rate and other test requirements.
3. For plastic QFP packages: -65°C/+150°C and 500 cycles or -55°C/+125°C and 1,000 cycles. For plastic BGA packages: -55°C/+125°C and 1000 cycles. For Flip Chip packages: -55°C/+125°C and 1,000 cycles or -40°C/+125°C and 1000 cycles.
4. For CPLD and EPROM products.
5. This is not a mandatory test and only for CPLD and EPROM products.
6. Package preconditioning is performed prior to THB, HAST & TC tests.

Nonhermetic and Hermetic Packages

Moisture sensitivity and reflow temperature information can be found in the "Device Package User Guide" linked here:
http://www.xilinx.com/bvdocs/userguides/ug112.pdf.

Package / Assembly

The nonhermetic package/assembly qualification is outlined in Nonhermetic Package/Assembly Qualification. However, for hermetic package qualification, a full group B & D test per MIL-STD-833, Test Methods, is required.

Table 1-2: **Nonhermetic Package/Assembly Qualification**

Reliability Test	Condition	Duration	Lot Qty	SS/lot(1)	Acceptance
Temperature Humidity Bias (THB) or High Accelerated Stress Test (HAST)	85°C, 85% R.H., V_{DD}, 130°C, 85% R.H., V_{DD}, 110°C, 85% R.H., V_{DD}	1,000 hours, 100 hours, 264 hours	1	77	0 fail
Temperature Cycling (TC)(2)	-65°C/+150°C, -55°C/+125°C, -40°C/+125°C	500 cycles, 1,000 cycles, 1,000 cycles	1	77	0 fail
Autoclave or Temperature Humidity (unbiased)	121°C, 100% R.H. or 85°C, 85% R.H.	96 hours or 1,000 hours	1	77	0 fail
Resistance to Solvent			1	3	0 fail
Solderability			1	3	0 fail
Lead Fatigue			1	3	0 fail
Ball Shear			1	5(40)(3)	0 fail
Bond Pull			1	4(22)(4)	0 fail

Notes:

1. The sample size listed above is based on the die size 237 mm^2. For bigger die size, the sample size may be reduced. to 36 or 22.
2. For plastic QFP packages: -65°C/+150°C and 500 cycles or -55°C/+125°C and 1,000 cycles.
   For plastic BGA packages: -55°C/+125°C and 1000 cycles.
   For Flip Chip packages: -55°C/+125°C and 1000 cycles or -40°C/+125°C and 1,000 cycles.
3. Minimum of 5 units with a total of 40 balls.
4. Minimum of 4 units with a total of 22 bonding wires.

Device

The qualification process for new devices is shown in Table 1-3.

Table 1-3: **Device Qualification**

Reliability Test	Condition	Lot Qty	SS/lot	Acceptance
ESD	HBM	1	3	2000V
Latch up	Current injection	1	6	200mA

Reliability Monitor Program

Wafer Process

The Wafer Process Monitor Program is based on the maturity of the process, device hours, and FIT Rate. All processes will be divided into the two classes that will determine the frequency of monitoring. Class 1 processes will be monitored every quarter, Class 2 processes will be monitored every other quarter. FIT Rate calculations for both classes will be based on approximately one million device hours (at T_J of 125ºC) per fab if the data is available. All processes that are four years old or less will be monitored every quarter regardless of the FIT rate. Mature processes older than four years will be monitored based on the FIT Rate. Table 1-4 illustrates the two Classes and the criteria for each.

Table 1-4: **Classes of Monitoring Processes**

Note:	Class 1	Class 2
Classification Criteria	Process Age < 4 years or FIT > 26 (FPGA); FIT > 55 (Flash PROM)	Process Age > 4 years and FIT < 26 (FPGA); FIT < 55 (Flash PROM)
Monitor Frequency	4 Times/year	2 Times/year

The reliability monitor for wafer process is shown in Table 1-5.

Table 1-5: **Wafer Process Monitor**

Reliability Test	Condition	Duration	Lot Qty	SS/Process/ Family/Quarter
High Temperature Operating Life (HTOL)	T_A=125°C, V_{DD} Max	1,000 hours	1	45
Data Retention Bake(1)	T_A = 150°C	1,000 hours	1	45

Note:

1. For CPLD and PROM products.

Package/Assembly

The reliability monitor for package/assembly is shown in Table 1-6.

Table 1-6: **Package/Assembly Monitor**

Reliability Test	Condition	Duration	Lot Qty	SS/Pkg Family/Quarter
Temperature Humidity Bias (THB) or High accelerated stress Test (HAST)	85°C, 85% R.H., V_{DD} 130°C, 85% R.H., V_{DD} 110°C, 85% R.H., V_{DD}	1,000 hours 100 hours 264 hours	1	45
Temperature Cycling (TC) (2)	-55°C/+125°C or -40°C/+125°C	1,000 cycles	1	45
Autoclave or Temperature Humidity (unbiased)	121°C, 100% R.H. or 85°C, 85% R.H	96 hours or 1,000 hours	1	45

Notes:

1. The sample size listed is based on the die size 237 mm^2. For bigger die size, the sample size may be reduced.
2. For plastic QFP and BGA packages: -55°C/+125°C and 1,000 cycles; for Flip chip packages: -55°C/+125°C and 1,000 cycles or -40°C/+125°C and 1,000 cycles.
3. Solderability, Mark Permanency, Lead Fatigue & Physical Dimension data are available upon special request.

Process Technology Family

Table 1-7: **Wafer Process Technology Family**

Process Technology	Device
0.09 µm	XC3Sxxx, XC3SxxxA, XC3SxxxE, XC4VxXxxx, XCE4VxXxxx
0.13 µm	XC2VPxxx, XCE2VPxxx
0.15 µm	XC2Vxxx, XCE2Vxxx
0.15 µm	XC18Vxxx, XCFxxxS/P
0.18 / 0.15 µm	XCVxxxE (shrink), XC2SxxxE
0.18 µm	XCVxxxE, XC2Cxxx
0.22 / 0.18 µm	XC2Sxxx, XCVxxx (shrink)
0.22 µm	XCVxxx
0.25 µm	XC4xxxXLA, XCSxxxXL, XC95xxxXV
0.35 µm / 0.25 µm	XC95xxxXL
0.35 µm	XC4xxxXL, XCSxxx, XCRxxxXL
0.35 µm	XC17Vxxx, XC17SxxxA
0.5 µm	XC4xxxE, XC95xxx
0.6 µm	XC4xxx/L/E
0.6 µm	XC17(S)xxx/(X)L/E

ESD and Latch-Up Summary

ESD results were obtained by using spec STM5.1-2001 or MIL-STD-883E.
Latch-Up results were obtained by using spec EIA/JESD78.

Table 1-8: **Product ESD and Latch-up Data**

Device	Latch-Up(24)	Human Body Model(24)	Charge Device Model
XC17xxxD/L	±200 mA	±2000V	±2000V(1)
XC17xxxE, XC17Sxxx	± 210 mA	±2000V	±1000V(8)
XC17Vxxx	± 200 mA	±2000V	±500V
XC18Vxxx	± 200 mA	±2000V	±500V(9)
XC31xxx/A	± 250 mA	±1750V to ±8000V	±1000V(3)
XC3xxx/A	± 220 mA	±4000V to ±7000V	±2000V(2)
XC4xxx/A	± 300 mA	±1000V to ±8000V	±2000V(4)
XC4xxxE	± 250 mA	±3000V to ±8000V	±2000V(5)
XC4xxxEX	± 250 mA	±3000V to ±7000V	±2000V(6)
XC4xxxXL	± 250 mA	±2000V to ±8000V	±1000V(7)
XC4xxxXLA	± 260 mA	±2000V to ±7000V	±500V(Core)/ ±1000V(corner)(10)
XCVxxx	± 200 mA	±1000V to ±2000V	±500V(11)
XCVxxxE	± 210 mA	±1000V to ±2500V(23)	±300V(12)
XCVxxxE/XC2SxxxE	± 210 mA	±2000V to ±3000V	±500V(13)
XCSxxx	± 310 mA	±6000V	±1000V(14)
XCSxxxXL	± 250 mA	±3000V	±500V(15)
XC2Sxxx	± 210 mA	±2000V	±500V(16)
XC5xxx	± 250 mA	±3000V to ±7000V	±2000V(17)
XC95xxx	± 200 mA	±2000V to ±3000V	±1000V(18)
XC95xxxXL	± 200 mA	±2000V to ±3000V	±1000V(19)
XC95xxxXV	± 200 mA	±2000V to ±3000V	±500V(20)
XCRxxxL	± 200 mA	±2000V to ±3000V	±500V(21)
XC2Vxxx	± 200 mA	±750V to ±2000V(22)(25)	±500V
XC2Cxxx	± 200 mA	±2000V	±500V
XC3Sxxx	± 200 mA	±2000V	±500V
XC3SxxxE	± 200 mA	±2000V	±500V
XC3SxxxA	± 200 mA	±2000V	±500V
XC18Vxxx(ST)	± 200 mA	±2000V	±500V

Table 1-8: **Product ESD and Latch-up Data *(Continued)***

XCFxxxS/P	± 200 mA	±2000V	±500V

Notes:

1. Measured on XC1765D
2. Measured on XC3090
3. Measured on XC3190/A
4. Measured on XC4005
5. Measured on XC4005E
6. Measured on XC4010E
7. Measured on XC4028XL
8. Measured on XC17256E
9. measured on XC18V04
10. Measured on XC4062XLA
11. Measured on XCV800
12. Measured on XCV50E
13. Measured on XCV2600(shrink), XCV3200(shrink)
14. Measured on XCS10 & XCS30
15. Measured on XCS30XL
16. Measured on XC2S200
17. Measured on XC5210
18. Measured on XC95108
19. Measured on XC9536XL
20. Measured on XC95288XV
21. Measured on XCR3064XL
22. Based on the data collected on XC2V40, XC2V80, XC2V250, XC2V500, XC2V1000, XC2V1500, XC2V2000, XC2V3000, XC2V4000, XC2V6000 and XC2V8000. For HBM, only XC2V40, XC2V500 and XC2V4000 (only from UMC 8D) device have ESD threshold below 2KV, XC2V40 pass at 1.75KV, XC2V4000 pass at 1.5KV and XC2V500 pass at 750V.
23. Only XCV100E and XCV812E have ESD threshold below 2KV, (XCV100E passed at 1.5KV and XCV812E passed at 1KV)
24. Both ESD & Latch-up tests performed @ Room temperature.
25. ESD results do not include Dxn and Dxp pins for all devices and Dxn & Dxp & Vbatt pins for XC2VxxxX devices.

Table 1-9: **ESD and Latch-up Data(1)**

Device	Latch-Up (± 200mA)	HBM Passing Voltage		CDM Passing Voltage	
		Regular IO & Power	MGT	Regular IO & Power	MGT
XC2VP2	Pass	± 1500V	± 2000V	± 500V	± 300V
XC2VP4	Pass	± 2000V	± 1500V	± 500V	± 300V
XC2VP7	Pass	± 2000V	± 1000V	± 500V	± 500V
XC2VP20	Pass	± 2000V	± 2000V	± 500V	± 300V
XC2VP30	Pass	± 2000V	± 2000V	± 500V	± 300V
XC2VP40	Pass	± 2000V	± 2000V	± 500V	±300V
XC2VP50	Pass	± 2000V	± 2000V	± 500V	± 300V
XC2VP70	Pass	± 2000V	± 2000V	± 500V	± 300V
XC2VP100	Pass	± 2000V	± 1000V	± 500V	± 300V
XC2VPX20	Pass	± 2000V	± 1500V	± 400V	± 200V

Notes:

1. The ESD results do not include DXN and DXP pins used for temperature sensing.

Table 1-10: **ESD and Latch-up Data for XC4VFXxxx**

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		STDIO	MGT	STDIO	MGT
XC4VFX12	pass	±2000V	N/A	±450V	N/A
XC4VFX60	pass	±2000V	±1000V	±500V	±300V
XC4VFX20	pass	±2000V	±1000V	±500V	±200V
XC4VFX100	pass	±2000V	±1000V	±500V	±100V

Table 1-11: **ESD and Latch-up Data for XC4VLXxxx and XC4VSXxxx**

Device	Latch-Up	HBM Passing Voltage	CDM Passing Voltage
XC4VLX15	pass	±2000V	±500V
XC4VLX25	pass	±2000V	±450V
XC4VLX40	pass	±2000V	±450V
XC4VLX60	pass	±2000V	±400V
XC4VLX80	pass	±2000V	±450V
XC4VLX100	pass	±2000V	±350V
XC4VLX160	pass	±2000V	±450V
XC4VLX200	pass	±2000V	±350V
XC4VSX25	pass	±2000V	±500V
XC4VSX35	pass	±2000V	±450V
XC4VSX55	pass	±2000V	±400V

Failure Rate Determination

The failure rate is typically defined in FIT (Failures In Time) units. One FIT means 1 failure per 1 billion device hours. For example, 5 fails expected out of 1 million components operating for 1000 hours will have failure rate of 5 FIT. The following is the failure rate calculation method:

$$\text{Failure Rate} = \frac{x^2\ 10^9}{2\ (\text{No. of dev.})\ (\text{No. of hrs.})\ (\text{Acc. Factor})}$$

Where x^2 = Chi-squared value at a desired confidence level and (2f + 2) degrees of freedom, where f is the number of failures.

The acceleration factor is calculated using the Arrhenius relationship

$A = \text{Exp}\ \{Ea/k\ (1/T_{J1} - 1/T_{J2})\}$

Ea = Thermal activation energy (0.7eV is assumed and used in failure rate calculation except EPROM in which 0.58 eV is used).

A = Acceleration factor

k = Boltzman's constant, 8.617164×10^{-5} eV/°K

T_{J1} = Use junction temperature in degrees Kelvin (°K =°C + 273.16)

T_{J2} = Stress junction temperature in degrees Kelvin (°K =°C + 273.16)

Failure Rate Summary

Table 1-12: **Summary of the Failure Rates**

Process Technology	Device Hours @ T_J = 125°C	FIT(1)
0.09 µm	6,600,120	2
0.13 µm	2,252,533	18
0.15 µm (FPGA)	3,221,660	17
0.15um (EPROM)	2,050,049	12
0.18/0.15 µm	2,609,391	10
0.18 µm	3,563,477	15
0.22/0.18 µm	2,241,533	12
0.22 µm	2,004,973	13
0.25 µm	3,001,551	4
0.35 µm/0.25 µm	2,261,805	6
0.35 µm	4,286,357	16
0.35 µm (EPROM)	1,662,661	15
0.5 µm	2,153,720	12
0.6 µm	718,785	16
0.6 µm (EPROM)	1,026,377	24

Note:

1. FIT is calculated based on 0.7 eV (0.58 eV for EPROM), 60% C.L. and T_J of 55°C.

Chapter 2

Results by Product Family

The FPGA Products

High-Temperature Operating Life (HTOL) Test

The HTOL test is conducted under the conditions of $T_j \geq 125°C$ temperature, maximum V_{DD} and either dynamic or static. The failure rate (FIT) calculation in the following tables is based on the assumption of 0.7 eV activation energy and 60% confidence level.

Summary

Table 2-1: **Summary of HTOL Test Results**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125^\circ C$	Failure Rate at 60% CL and $T_J=55^\circ C$ (FIT)
XC4xxx/E (0.6 µm)	12	0	547	270,742	718,785	16
XC4xxx/E (0.5 µm)	12	0	521	738,671	1,072,140	11
XC4xxxXL	22	3	931	1,084,452	2,033,310	26
XC4xxxXLA	11	0	472	771,630	1,078,772.	11
XCSxxx	11	0	479	660,098	1,179,091	10
XCSxxxXL	12	0	517	544,278	1,168,392	10
XC2Sxxx	13	0	808	917,044	1,165,354	10
XCVxxx	19	1	830	1,070,478	2,004,973	13
XCVxxx (shrink)	12	1	551	721,228	1,076,179	24
XCVxxxE	30	3	1,179	1,541,758	2,555,008	21
XCVxxxE (shrink)	18	1	639	976,814	1,502,774	17
XC2SxxxE	16	0	836	788,620	1,106,617	11
XC2Vxxx	18	1	735	1,199,076	2,176,790	12
XCE2Vxxx	14	2	441	625,388	1,044,870	38
XC2VPxxx	9	0	356	526,155	1,016,656	12
XCE2VPxxx	7	2	440	1,235,877	1,235,877	32
XC3Sxxx	9	0	627	726,158	1,011,056	12
XC3SxxxE	8	0	549	622,966	753,846	16
XC3SxxxA	7	0	376	544,902	740,483	16
XC4VxXxxx	14	0	684	1,248,043	2,116,769	6
XCE4VxVxxx	8	0	597	921,000	1,977,966	6

Note:

Each of the failures listed in the table above is also listed in each family device table with failure analysis results in the footnote.

Data

Table 2-2: **HTOL Test Results of 0.6 µm, Si Gate CMOS Device Type XC4xxx/E**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC4005E	2	0	94	24,064	63,878	
XC4010E	8	0	364	190,462	505,683	
XC4013E	1	0	42	44,184	117,286	
XC4025E	1	0	47	12,032	31,939	
XC4xxx/E	12	0	547	270,742	718,785	16 FIT

Table 2-3: **HTOL Test Results of 0.5 µm, Si Gate CMOS Device Type XC4xxx/E**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC4005E	1	0	42	42,084	111,711	
XC4008E	1	0	42	84,000	88,107	
XC4010E	2	0	93	117960.00	117,960.00	
XC4013E	6	0	261	369,000	557,906	
XC4020E	2	0	83	125,627	196,455	
XC4xxx/E	12	0	521	738,671	1,072,140	11 FIT

Table 2-4: **HTOL Test Results for 0.35 µm Si Gate CMOS Device Type XC4xxxXL**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC4005XL	1	0	44	43,340	115,045	
XC4010XL	7	1(1)	305	462,932	843,746	
XC4020XL	2	0	93	186,000	334,903	
XC4028XL	3	0	126	95,844	254,416	
XC4036XL	4	0	183	145,252	218,721	
XC4044XL	1	0	42	84,420	89,520	
XC4062XL	4	2(2)	138	66,664	176,959	
XC4xxxXL	22	3	931	1,084,452	2,033,310	26 FIT

Notes:

1. The device failed at post 1,033 hour but no failure analysis was performed.
2. No defect was found at post 48 hours

Table 2-5: **HTOL test Results for 0.25 µm Si Gate CMOS Device Type XC4xxxXLA**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125^\circ C$	Failure Rate at 60% CL and $T_J=55^\circ C$ (FIT)
XC4013XLA	1	0	45	45,000	119,452	
XC4020XLA	1	0	42	85,470	85,470	
XC4028XLA	3	0	127	213,450	365,492	
XC4036XLA	1	0	45	45,000	119,452	
XC4044XLA	1	0	44	88,797	92,134	
XC4052XLA	1	0	42	84,000	86,860	
XC4085XLA	3	0	127	209,913	209,913	
XC4xxxXLA	11	0	472	771,630	1,078,772.	11 FIT

Table 2-6: **HTOL Test Results for 0.35 µm Si Gate CMOS Device type XCSxxx**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125^\circ C$	Failure Rate at 60% CL and $T_J=55^\circ C$ (FIT)
XCS05	2	0	84	168,396	317,374	
XCS20	4	0	175	220,643	509,306	
XCS30	3	0	133	224,043	305,395	
XCS40	2	0	87	47,016	47,016	
XCSxxx	11	0	479	660,098	1,179,091	10 FIT

Table 2-7: **HTOL Test Results for 0.25 µm Si Gate CMOS Devices Type XCSxxxXL**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125^\circ C$	Failure Rate at 60% CL and $T_J=55^\circ C$ (FIT)
XCS05XL	2	0	90	137,565	365,164	
XCS20XL	3	0	129	129,594	272,427	
XCS30XL	6	0	253	269,514	523,195	
XCS40XL	1	0	45	7,605	7,605	
XCSxxxXL	12	0	517	544,278	1,168,392	10 FIT

Table 2-8: **HTOL Test Results for 0.22/0.18 µm Si Gate CMOS Device Type XC2Sxxx**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC2S50	3	0	166	171,041	245,567	
XC2S100	4	0	310	318,008	350,590	
XC2S150	3	0	135	180,675	195,004	
XC2S200	3	0	197	247,320	374,192	
XC2Sxxx	13	0	808	917,044	1,165,354	10 FIT

Table 2-9: **HTOL Test Results for 0.22 µm Si Gate CMOS Device Type XCVxxx**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XCV50	1	0	45	45,000	45,000	
XCV100	1	0	45	45,000	119,452	
XCV200	4	0	181	365,274	423,913	
XCV300	6	0	331	321,727	854,020	
XCV600	2	1(1)	94	144,220	382,830	
XCV800	2	0	44	28,402	38,484	
XCV1000	3	0	89	120,855	141,275	
XCVxxx	19	1	830	1,070,478	2,004,973	13 FIT

Notes:

1. No defect found at post 74 hours.

Table 2-10: **HTOL Test Results for 0.22/0.18 µm Si Gate CMOS Device Type XCVxxx (Shrink)**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XCV300	1	0	76	76,988	204,364	
XCV400	5	1(1)	188	286,565	286,565	
XCV600	3	0	163	188,055	314,425	
XCV800	3	0	123	169,620	270,826	
XCVxxx	12	1	551	721,228	1,076,179	24 FIT

Note:

1. The device failed at post 48 hours, no failure analysis was performed.

Table 2-11: **HTOL Test Results for 0.18 µm Si Gate CMOS Device Type XCVxxxE**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XCV50E	2	0	84	126,630	336,137	
XCV100E	2	0	80	115,765	115,765	
XCV200E	3	0	165	215,436	571,872	
XCV600E	5	0	192	193,043	512,430	
XCV405E	2	1(1)	119	108,304	108,304	
XCV812E	3	0	115	185,395	185,395	
XCV1000E	4	0	141	142,366	178,874	
XCV1600E	4	1(2)	150	298,739	350,233	
XCV2000E	5	1(3)	133	156,080	195,998	
XCVxxxE	30	3	1,179	1,541,758	2,555,008	21 FIT

Notes:

1. Functional fail at post 184 hours.
2. Marginal failure at post 501 hours.
3. No defect found at post 281 hrs.

Table 2-12: **HTOL Test Results for 0.18/0.15 µm Si Gate CMOS Device Type XCVxxxE (Shrink)**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XCV400E	2	0	121	166,653	293,400	
XCV600E	2	0	87	154,743	259,253	
XCV1000E	5	0	180	214,226	393,226	
XCV2000E	7	0	206	371,588	487,291	
XCV2600E	1	1(1)	22	23,604	23,604	
XCV3200E	1	0	23	46,000	46,000	
XCVxxxE(Shrink)	18	1	639	976,814	1,502,774	17 FIT

Note:

1. No defect found at post 189 Hours

Table 2-13: **HTOL Test Results for 0.18/0.15 µm Si Gate CMOS Device Type XC2SxxxE**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC2S50E	1	0	45	45,000	119,452	
XC2S100E	6	0	285	222,284	341,010	
XC2S150E	1	0	45	91,665	110,293	
XC2S200E	1	0	45	45,000	119,452	
XC2S300E	7	0	416	384,671	416,410	
XC2SxxxE	16	0	836	788,620	1,106,617	11 FIT

Table 2-14: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XC2Vxxx**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC2V40	1	0	44	90,248	141,951	
XC2V500	8	0	359	484,007	1,031,641	
XC2V1000	2	0	87	174,840	174,840	
XC2V3000	2	0	86	173,894	288,997	
XC2V4000	3	1(1)	117	192,087	433,202	
XC2V6000	2	0	42	84,000	106,158	
XC2Vxxx	18	1	735	1,199,076	2,176,790	12 FIT

Notes:

1. Failure due to UBM defect at post 1,051 hours.

Table 2-15: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XCE2Vxxx**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XCE2V2000	2	0	89	136,561	286,524	
XCE2V3000	4	2(1)	169	264,186	440,056	
XCE2V4000	8	0	183	22,464	318,289	
XCE2Vxxx	14	2	441	625,388	1,044,870	38 FIT

Note:

1. Due to metal particles at post 2,061 hours.

Table 2-16: **HTOL Test Results for 0.13 µm Si Gate CMOS Device Type XC2VPxxx**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC2VP7	1	0	45	67,725	118,517	
XC2VP30	1	0	43	43,344	64,794	
XC2VP50	5	0	221	318,577	648,438	
XC2VP70	2	0	47	96,509	184,907	
XC2VPxxx	9	0	356	526,155	1,016,656	12 FIT

Table 2-17: **HTOL Test Results for 0.13 µm Si Gate CMOS Device Type XCE2VPxxx**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XCE2VP7	7	2(1)	430	1,235,877	1,235,877	32 FIT

Note:

1. No defect found – at post 168 & 1,001 hrs.

Table 2-18: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3Sxxx**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC3S200	3	0	231	231,000	297,545	
XC3S400	3	0	231	232,540	305,211	
XC3S1500	2	0	89	135,025	180,458	
XC3S5000	1	0	76	127,593	227,843	
XC3Sxxx	9	0	627	726,158	1,011,056	12 FIT

Table 2-19: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3SxxxE**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC3S500E	3	0	228	231,631	320,936	
XC3S1200E	1	0	45	67,344	80,159	
XC3S1600E	4	0	276	323,991	352,751	
XC3SxxxE	8	0	549	622,966	753,846	16 FIT

Table 2-20: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3SxxxA**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC3S1400A	7	0	376	544,902	740,483	16 FIT

Table 2-21: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC4VxXxxx**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC4VLX60	5	0	353	763,046	1,184,974	
XC4VLX80	3	0	175	175,480	278,314	
XC4VLX100	4	0	69	134,990	349,581	
XC4VSX35	2	0	87	174,527	303,901	
XC4VxXxxx	14	0	684	1,248,043	2,116,769	6 FIT

Table 2-22: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XCE4VxXxxx**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XCE4VLX100	8	0	597	921,000	1,977,966	6 FIT

The Temperature Humidity Bias (THB) Test

The THB test is conducted under the conditions of 85°C and 85% R.H. and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the THB test.

Summary

Table 2-23: **THB Test Results for Si Gate CMOS Devices**

Device Family	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC4xxxE	1	0	38	38,000
XC4xxxXL	1	0	45	45,000
XCSxxx	1	0	40	40,000
XCSxxxXL	2	0	90	90,990
XCVxxxE	1	0	45	45,000
XCVxxxE (shrink)	3	0	134	134,630
XC2Vxxx	2	0	63	64,755
XC2Sxxx	3	0	231	237,391
XCE2Vxxx	2	0	63	64,773
XC2VPxxx	1	0	43	43,215
XCE2VPxxx	1	0	22	22,088
XC2SxxxE	19	0	1,070	1,086,254
XC3Sxxx	22	0	1,548	1,570,676
XC3SxxxE	4	1	220	224,265
XC3SxxxA	2	0	159	160,460
XC4VLXxxx	11	0	545	550,617

Note:

The failure listed in the table above is also listed in each family device table with failure analysis results in the footnote.

Data

Table 2-24: **THB Test Results for Si Gate CMOS Device Type XC4xxxE**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC4013E	1	0	38	38,000

Table 2-25: **THB Test Results for Si Gate CMOS Devices Type XC4xxxXL**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC4010XL	1	0	45	45,000

Table 2-26: **THB Test Results for Si Gate CMOS Device Type XCSxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCS10	1	0	40	40,000

Table 2-27: **THB Test Results for Si Gate CMOS Device Type XCSxxxXL**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCS10XL	1	0	45	45,540
XCS20XL	1	0	45	45,450
XCSxxxXL	2	0	90	90,990

Table 2-28: **THB Test Results for Si Gate CMOS Devices Type XCVxxxE**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCV1600E	1	0	45	45,000

Table 2-29: **THB Test Results for Si Gate CMOS Device Type XCVxxxE (shrink)**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCV600E	1	0	45	45,000
XCV1000E	2	0	89	89,630
XCVxxxE(shrink)	3	0	134	134,630

Table 2-30: **THB Test Results for Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2V3000	1	0	18	18,000
XC2V6000	1	0	45	46,755
XC2Vxxx	2	0	63	64,755

Table 2-31: **THB Test Results for Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2S100	3	0	231	237,391

Table 2-32: **THB Test Results for Si Gate CMOS Device Type XCE2Vxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCE2V2000	1	0	18	18,018
XCE2V4000	1	0	45	46,755
XCE2Vxxx	2	0	63	64,773

Table 2-33: **THB Test Results for Si Gate CMOS Device Type XCE2VPxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCE2VP4	1	0	22	22,088

Table 2-34: **THB Test Results for Si Gate CMOS Device Type XC2VPxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2VP4	1	0	43	43,215

Table 2-35: **THB Test Results for Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2S50E	1	0	44	45,232
XC2S100E	6	0	240	248,330
XC2S150E	1	0	42	43,508
XC2S300E	9	0	589	594,016
XC2S400E	2	0	155	155,000
XC2SxxxE	19	0	1,070	1,086,254

Table 2-36: **THB Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC3S200	3	0	199	199,379
XC3S400	5	0	381	386,473
XC3S1000	4	0	276	279,453
XC3S1500	6	0	462	473,088
XC3S2000	4	0	230	232,283
XC3Sxxx	22	0	1,548	1,570,676

Table 2-37: **THB Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC3S500E	4	1	220	224,265

Note:

Failure at post 1,075 hours – metal 2 defect. New PR coating recipe was implemented for M2 to M5

Table 2-38: **THB Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC3S1400A	2	0	159	160,460

Table 2-39: **THB Test Results for Si Gate CMOS Device Type XC4VLXxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC4VLX25	6	0	290	292,173
XC4VLX60	3	0	116	116,240
XC4VFX20	2	0	139	142,204
XC4VxXxxx	11	0	545	550,617

The Temperature Humidity (TH) Test

The TH test is conducted under the conditions of 85°C and 85% R.H. Package preconditioning is performed on the testing samples prior to the TH test.

Summary

Table 2-40: **Summary of TH Test Results**

Device Family	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC4xxxE	2	0	90	90,585
XC4xxxXLA	2	0	85	87,550
XCSxxx	1	0	60	60,480
XCSxxxXL	2	0	122	126,409
XC2Sxxx	2	0	85	85,405
XCVxxx (shrink)	1	0	45	45,000
XCVxxxE	2	0	67	67,443
XCVxxxE (shrink)	8	0	368	370,780
XC2SxxxE	6	0	323	325,147
XC2Vxxx	9	0	337	338,383
XCE2Vxxx	2	0	72	72,270
XC2VPxxx	9	0	536	543,814
XCE2VPxxx	1	0	22	22,154
XC3Sxxx	4	0	250	254,524
XC3SxxxE	8	0	453	457,370
XC3SxxxA	1	0	77	79,310
XC4VxXxxx	10	0	430	432,937

Data

Table 2-41: **TH Test Results for Si Gate CMOS Device Type XC4xxxE**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC4006E	1	0	45	45,135
XC4013E	1	0	45	45,450
XC4xxxE	2	0	90	90,585

Table 2-42: **TH Test Results for Si Gate CMOS Device Type XC4xxxXLA**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC4052XLA	1	0	40	42,280
XC4062XLA	1	0	45	45,270
XC4xxxXLA	2	0	85	87,550

Table 2-43: **TH Test Results for Si Gate CMOS Device Type XCSxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCS30	1	0	60	60,480

Table 2-44: **TH Test Results for Si Gate CMOS Device Type XCSxxxXL**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCS30XL	1	0	77	80,059
XCS40XL	1	0	45	46,350
XCSxxxXL	2	0	122	126,409

Table 2-45: **TH Test Results for Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2S100	1	0	40	40,360
XC2S200	1	0	45	45,045
XC2Sxxx	2	0	85	85,405

Table 2-46: **TH Test Results for Si Gate CMOS Device Type XCVxxxE**

Device Family	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCV1600E	2	0	67	67,443

Table 2-47: **TH Test Results for Si Gate CMOS Device Type XCVxxxE (shrink)**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCV600E	2	0	122	122,854
XCV1000E	3	0	134	134,986
XCV2000E	3	0	112	112,940
XCVxxxE	8	0	368	370,780

Table 2-48: **TH Test Results for Si Gate CMOS Devices Type XCVxxx (shrink)**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCV400	1	0	45	45,000

Table 2-49: **TH Test Results for Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2S100E	1	0	45	45,315
XC2S150E	1	0	40	40,120
XC2S300E	3	0	162	163,256
XC2S600E	1	0	76	76,456
XC2SxxxE	6	0	323	325,147

Table 2-50: **TH Test Results for Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2V250	1	0	30	30,120
XC2V1500	1	0	40	40,240
XC2V3000	2	0	90	90,405
XC2V4000	2	0	90	90,450
XC2V6000	3	0	87	87,168
XC2Vxxx	9	0	337	338,383

Table 2-51: **TH Test Results for Si Gate CMOS Devices Type XCE2Vxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCE2V2000	1	0	27	27,000
XCE2V4000	1	0	45	45,270
XCE2Vxxx	2	0	72	72,270

Table 2-52: **TH Test Results for Si Gate CMOS Devices Type XCE2VPxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCE2VP50	1	0	22	22,154

Table 2-53: **TH Test Results for Si Gate CMOS Devices Type XC2VPxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2VP4	1	0	43	43,043
XC2VP20	2	0	122	122,777
XC2VP30	2	0	150	150,592
XC2VP40	2	0	154	157,927
XC2VP50	1	0	45	47,475
X2VP70	1	0	22	22,000
XC2VPxxx	9	0	536	543,814

Table 2-54: **TH Test Results for Si Gate CMOS Devices Type XC3Sxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC3S1500	2	0	123	126,912
XC3S4000	1	0	50	50,150
XC3S5000	1	0	77	77,462
XC3Sxxx	4	0	250	254,524

Table 2-55: **TH Test Results for Si Gate CMOS Devices Type XC3SxxxE**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC3S250E	3	0	194	197,504
XC3S500E	3	0	170	170,555
XC3S1600E	2	0	89	89,311
XC3SxxxE	8	0	453	457,370

Table 2-56: **TH Test Results for Si Gate CMOS Devices Type XC3SxxxA**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC3S1400A	1	0	77	79,310

Table 2-57: **TH Test Results for Si Gate CMOS Devices Type XC4VxXxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC4VFX20	1	0	77	77,616
XC4VLX25	6	0	278	279,600
XC4VLX60	1	0	15	15,405
XC4VLX100	1	0	32	32,064
XC4VLX200	1	0	28	28,252
XC4VxXxxx	10	0	430	432,937

Autoclave Test

The autoclave test is conducted under the conditions of 121°C, 100% R.H. (unbiased) and 29.7 PSI. Package preconditioning is performed on the testing samples prior to the autoclave stress test.

Summary

Table 2-58: **Summary of Autoclave Test Results**

Device Family	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2Sxxx	2	0	122	11,712
XC3Sxxx	1	0	45	4,320

Data

Table 2-59: **Autoclave Test Results for Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2S50	1	0	45	4,320
XC2S100	1	0	77	7,392
XC2Sxxx	2	0	122	11,712

Table 2-60: **Autoclave Test Results for Si Gate CMOS Devices Type XC3Sxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC3S200	1	0	45	4,320

Temperature Cycling (TC) Test

The TC test is conducted under the conditions of predefined maximum and minimum temperatures and in air-to-air environment. Package precondition is performed on the testing samples prior to the TC test.

Summary

Table 2-61: **Summary of TC Test Results**

Device Family	Lot Qty	Failures	Device on Test	Total Device Cycles
XC4xxxE	3	0	134	143,956
XC4xxxXL	2	0	122	123,170
XC4xxxXLA	2	0	85	87,182
XCSxxx	2	0	100	101,880
XCSxxxXL	5	0	260	281,313
XC2Sxxx	4	0	207	210,061
XC2SxxxE	20	0	1,277	1,266,496
XCVxxx	2	0	122	131,737
XCVxxx (shrink)	2	0	67	67,336
XCVxxxE	2	0	67	69,015
XCVxxxE(shrink)	14	0	733	746,666
XC2Vxxx	11	2	478	489,771
XCE2Vxxx	1	0	45	45,945
XC2VPxxx	15	3	817	853,917
XCE2VPxxx	1	0	60	67,980
XC3Sxxx	27	0	1,955	2,052,589
XC3SxxxE	13	1	765	805,692
XC3SxxxA	5	0	389	487,841
XC4VxXxxx	35	2	1,566	1,614,124

Note:

Each of the failures listed in the table above is also listed in each family device table with failure analysis results in the footnote.

Data

Table 2-62: **TC Test Results for Si Gate CMOS Device Type XC4xxx/E**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC4006E	B: -55°C to +125°C	1	0	45	49,905
XC4013E	B: -55°C to +125°C	2	0	89	94,051
XC4xxx/E	B	3	0	134	143,956

Table 2-63: **TC Test Results for Si Gate CMOS Device Type XC4xxxXL**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC4010XL	B: -55°C to +125°C	1	0	45	46,170
XC4062XL	B: -55°C to +125°C	1	0	77	77,000
XC4xxxXL	B	2	0	122	123,170

Table 2-64: **TC Test Results for Si Gate CMOS Device Type XC4xxxXLA**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC4052XLA	B: -55°C to +125°C	1	0	41	43,050
XC4062XLA	B: -55°C to +125°C	1	0	44	44,132
XC4xxxXLA	B	2	0	85	87,182

Table 2-65: **TC Test Results of Si Gate CMOS Device Type XCSxxx**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XCS05	B: -55°C to +125°C	1	0	40	41,400
XCS30	B: -55°C to +125°C	1	0	60	60,480
XCSxxx	B	2	0	100	101,880

Table 2-66: **TC Test Results for Si Gate CMOS Device Type XCSxxxXL**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XCS10XL	B: -55°C to +125°C	1	0	45	45,000
XCS20XL	B: -55°C to +125°C	1	0	45	47,475
XCS30XL	B: -55°C to +125°C	1	0	82	97,722
XCS40XL	B: -55°C to +125°C	2	0	88	91,116
XCSxxxXL	B	5	0	260	281,313

Table 2-67: **TC Test Results for Si Gate CMOS Device Type XC2Sxxx**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC2S50	B: -55°C to +125°C	1	0	45	45,000
XC2S100	B: -55°C to +125°C	2	0	117	119,971
XC2S200	B: -55°C to +125°C	1	0	45	45,090
XC2Sxxx	B	4	0	207	210,061

Table 2-68: **TC Test Results for Si Gate CMOS Device Type XC2SxxxE**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC2S50E	B: -55°C to +125°C	1	0	45	45,000
XC2S100E	B: -55°C to +125°C	4	0	199	207,647
XC2S150E	B: -55°C to +125°C	2	0	89	89,530
XC2S300E	B: -55°C to +125°C	10	0	706	682,973
XC2S400E	B: -55°C to +125°C	2	0	161	163,268
XC2S600E	B: -55°C to +125°C	1	0	77	78,078
XC2SxxxE	B	20	0	1,277	1,266,496

Table 2-69: **TC Test Results for Si Gate CMOS Device Type XCVxxx**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XCV100	B: -55°C to +125°C	1	0	77	85,162
XCV200	B: -55°C to +125°C	1	0	45	46,575
XCVxxx	B	2	0	122	131,737

Table 2-70: **TC Test Results for Si Gate CMOS Device Type XCVxxx (shrink)**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XCV400	B: -55°C to +125°C	1	0	45	45,270
XCV800	B: -55°C to +125°C	1	0	22	22,066
XCVxxx (shrink)	B	2	0	67	67,336

Table 2-71: **TC Test Results for Si Gate CMOS Device Type XCVxxxE**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XCV1600E	B: -55°C to +125°C	2	0	67	69,015

Table 2-72: **TC Test Results for Si Gate CMOS Device Type XCVxxxE (shrink)**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XCV200E	B: -55°C to +125°C	1	0	76	76,760
XCV300E	B: -55°C to +125°C	1	0	77	77,539
XCV600E	B: -55°C to +125°C	5	0	287	292,979
XCV1000E	B: -55°C to +125°C	3	0	113	117,813
XCV2000E	B: -55°C to +125°C	4	0	180	181,575
XCVxxxE	B	14	0	733	746,666

Table 2-73: **TC Test Results for Si Gate CMOS Device Type XC2Vxxx**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC2V250	B: -55°C to +125°C	1	0	30	30,000
XC2V500	B: -55°C to +125°C	1	0	40	40,200
XC2V1500	B: -55°C to +125°C	1	0	41	41,615
XC2V3000	B: -55°C to +125°C	2	2(1)	90	90,900
XC2V4000	B: -55°C to +125°C	2	0	89	94,197
XC2V6000	B: -55°C to +125°C	3	0	135	135,990
XC2V8000	B: -55°C to +125°C	1	0	53	56,869
XC2Vxxx	B	11	2	478	489,771

Note:

1. Two failures at post 1,013 cycles were due to via misalignment at the package substrate. Tighter alignment limits have been implemented.

Table 2-74: **TC Test Results for Si Gate CMOS Device Type XCE2Vxxx**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XCE2V2000	B: -55°C to +125°C	1	0	45	45,945

Table 2-75: **TC Test Results for Si Gate CMOS Device Type XC2VPxxx**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC2VP4	B: -55°C to +125°C	2	0	90	95,130
XC2VP7	B: -55°C to +125°C	1	0	60	60,000
XC2VP20	B: -55°C to +125°C	3	0	162	173,657
XC2VP30	B: -55°C to +125°C	1	0	72	75,134
XC2VP40	B: -55°C to +125°C	2	0	157	163,975
XC2VP50	B: -55°C to +125°C	3	3(1)(2)	138	149,191
XC2VP70	B: -55°C to +125°C	1	0	21	21,000
XC2VP100	B: -55°C to +125°C	2	0	117	115,830
XC2VPxxx	B	15	3	817	853,917

Notes:

1. One failure at post 500 cycles due to substrate via defect. Process has been improved.
2. Two failure at post 1079 cycles due to substrate via defect. Process has been improved.

Table 2-76: **TC Test Results for Si Gate CMOS Device Type XCE2VPxxx**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XCE2VP50	B: -55°C to +125°C	1	0	60	67,980

Table 2-77: **TC Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC3S200	B: -55°C to +125°C	3	0	198	199,848
XC3S400	B: -55°C to +125°C	5	0	385	385,000
XC3S1000	B: -55°C to +125°C	6	0	430	460,311
XC3S1500	B: -55°C to +125°C	7	0	507	534,160
XC3S2000	B: -55°C to +125°C	3	0	231	243,012
XC3S4000	B: -55°C to +125°C	1	0	50	75,950
XC3S5000	B: -55°C to +125°C	2	0	154	154,308
XC3Sxxx	B	27	0	1,955	2,052,589

Table 2-78: **TC Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC3S100E	B: -55°C to +125°C	1	0	82	83,722
XC3S250E	B: -55°C to +125°C	3	0	198	216,751
XC3S500E	B: -55°C to +125°C	6	1(1)	350	365,989
XC3S1600E	B: -55°C to +125°C	3	0	135	139,230
XC3SxxxE	B	13	1	765	805,692

Note:

1. Failure at post 1,146 cycles due to random defect.

Table 2-79: **TC Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC3S200A	B: -55°C to +125°C	1	0	75	155,995
XC3S1400A	B: -55°C to +125°C	4	0	314	331,846
XC3SxxxA	B	5	0	389	487,841

Table 2-80: **TC Test Results for Si Gate CMOS Device Type XC4VxXxxx**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC4VLX25	B: -55°C to +125°C	8	0	483	495,048
XC4VLX60	B: -55°C to +125°C	3	0	123	125,126
XC4VFX60	B: -55°C to +125°C	2	0	157	164,754
XC4VLX100	B: -55°C to +125°C	5	2(1)	97	100,948
XC4VLX160	B: -55°C to +125°C	5	0	241	254,284
XC4VLX160	G: -40°C to +125°C	1	0	43	43,000
XC4VLX200	B: -55°C to +125°C	11	0	422	430,964
XC4VxXxxx	B&G	35	2	1,566	1,614,124

Note:

1. Two failures at post 500 cycles were due to defective via at package substrate. Via resistance measurement with tightened limits has been implemented for screening out the defect.

High Accelerated Stress Test (HAST)

The HAST test is conducted under the conditions of 130°C, 85% R.H. and V_{DD} bias or 110°C, 85% R.H. and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the HAST test.

Summary

Table 2-81: **Summary of HAST Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCVxxxE (shrink)	1	0	33	8,712
XC2SxxxE	2	0	82	8,032

Data

Table 2-82: **HAST Test Results of Si Gate CMOS Device Type XCVxxxE (shrink)**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCV400E	1	0	33	8,712

Table 2-83: **HAST Test Results of Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2S150E	1	0	40	4,000
XC2S400E	1	0	42	4,032
XC2SxxxE	2	0	82	8,032

High-Temperature Storage Life

The High-Temperature Storage Life test is conducted under the conditions of 150°C and unbiased.

Summary

Table 2-84: **Summary of High-Temperature Storage Life Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC4xxxE	1	0	30	30,240
XCSxxx	1	0	60	60,360
XCSxxxXL	1	0	77	124,255
XCVxxx	1	0	45	45,405
XCVxxxE(shrink)	1	0	74	74,370
XC2Sxxx	2	0	85	85,540
XC2SxxxE	7	0	431	433,658
XC2Vxxx	2	0	90	90,810
XC2VPxxx	4	0	194	194,840
XC3Sxxx	9	0	450	454,469
XC3SxxxE	6	0	355	357,248
XC3SxxxA	3	0	232	234,744
XC4VxXxxx	4	0	302	304,153

Data

Table 2-85: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC4xxxE**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC4013E	1	0	30	30,240

Table 2-86: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCSxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCS30	1	0	60	60,360

Table 2-87: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCSxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCS30XL	1	0	77	124,255

Table 2-88: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCVxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCV200	1	0	45	45,405

Table 2-89: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCVxxxE(shrink)**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCV600E	1	0	74	74,370

Table 2-90: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2S100	2	0	85	85,540

Table 2-91: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2S100E	1	0	2	2,010
XC2S300E	2	0	122	122,591
XC2S400E	2	0	156	156,936
XC2S600E	2	0	151	152,121
XC2SxxxE	7	0	431	433,658

Table 2-92: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2V250	1	0	45	45,360
XC2V500	1	0	45	45,450
XC2Vxxx	2	0	90	90,810

Table 2-93: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC2VPxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2VP20	3	0	165	165,840
XC2VP70	1	0	29	29,000
XC2VPxxx	4	0	194	194,840

Table 2-94: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC3S50	1	0	77	77,462
XC3S200	1	0	45	45,360
XC3S400	2	0	90	90,720
XC3S1000	1	0	26	26,286
XC3S1500	2	0	90	90,360
XC3S2000	1	0	45	46,665
XC3S5000	1	0	77	77,616
XC3Sxxx	9	0	450	454,469

Table 2-95: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC3S500E	4	0	233	234,632
XC3S1600E	2	0	122	122,616
XC3SxxxE	6	0	355	357,248

Table 2-96: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC4VxXxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC3S1400A	3	0	232	234,744

Table 2-97: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC4VxXxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC3FX20	1	0	75	76,075
XC4VLX25	3	0	227	228,078
XC4VxXxxx	4	0	302	304,153

The Flash PROM Products

High-Temperature Operating Life (HTOL) Tests

The HTOL test is conducted under the conditions of 125°C ambient temperature, maximum V_{DD} and either dynamic or static. The failure rate (FIT) calculation in the following tables is based on the assumption of 0.58 eV activation energy and 60% confidence level.

Summary

Table 2-98: **Summary of HTOL Test Results**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC17(S)xxx/(X)L	11	0	489	611,926	1,026,377	24
XC17Vxxx/17SxxxA	8	0	707	924,507	1,662,661	15
XC18Vxxx	12	0	540	540,000	1,011,896	25
XCFxxxS/P	10	0	392	1,000,000	1,038,153	24

Data

Table 2-99: **HTOL Test Results for 0.6 µm Si Gate CMOS Device Type XC17(S)xxx/(X)L**

Device	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC1701L	6	0	274	215,668	469,281	
XC1702	3	0	134	269,889	273,344	
XC17S40XL	1	0	36	36,144	81,159	
XC17S150XL	1	0	45	90,225	202,593	
XC17Sxx/XL	11	0	489	611,926	1,026,377	24 FIT

Table 2-100: **HTOL Test Results of 0.35 µm Si Gate CMOS Device Type XC17Vxx/XC17SxxxA**

Device	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC17V01	1	0	299	302,289	678,766	
XC17V04	3	0	166	289,208	538,012	
XC17V16	1	0	45	90,630	203,503	
XC17S50A	1	0	45	90,000	90,000	
XC17S200A	2	0	152	152,380	152,380	
XC17Vxx/ XC17SxxxA	8	0	707	924,507	1,662,661	15 FIT

Table 2-101: **HTOL Test Results for 0.15 µm Si Gate CMOS Devices Type 18Vxxx**

Device	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125^oC$	Failure Rate at 60% CL and $T_J=55^oC$ (FIT)
XC18V02	3	0	135	135,000	249,458	
XC18V04	9	0	405	405,000	762,439	
XC18Vxxx	12	0	540	540,000	1,011,896	25 FIT

Table 2-102: **HTOL Test Results for 0.15 µm Si Gate CMOS Devices Type XCFxxxS/P**

Device	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125^oC$	Failure Rate at 60% CL and $T_J=55^oC$ (FIT)
XCF04S	1	0	45	45,000	45,000	
XCF08P	2	0	90	90,000	90,000	
XCF16P	3	0	77	685,000	685,000	
XCF32P	4	0	180	180,000	218,153	
XCFxxxS/P	10	0	392	1,000,000	1,038,153	24 FIT

The Temperature Humidity Bias (THB) Test

The THB test is conducted under the conditions of 85°C and 85% R.H. and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the THB test.

Summary

Table 2-103: **Summary of THB Test Results**

Device Family	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC17(S)xxx/(X)L/E	6	0	322	322,585
XC17Vxxx/ XC17SxxxA	6	0	289	291,302
XCFxxxS/P	8	0	270	236,000

Data

Table 2-104: **THB Test Results for Si Gate CMOS Device Type XC17(S)xxx/(X)L/E**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC1701L	2	0	154	154,000
XC17128E	2	0	90	90,495
XC17S40XL	1	0	33	33,000
XC17S100XL	1	0	45	45,090
XC17(S)xxx/(X)L/E	6	0	322	322,585

Table 2-105: **THB Test Results for Si Gate CMOS Device Type XC17Vxxx/XC17SxxxA**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC17V01	3	0	134	135,030
XC17V02	1	0	45	45,315
XC17S50A	1	0	77	77,000
XC17S200A	1	0	33	33,957
XC17Vxxx/ XC17SxxxA	6	0	289	291,302

Table 2-106: **THB Test Results of Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCF08P	1	0	27	27,000
XCF16P	1	0	45	22,500
XCF32P	6	0	198	186,500
XCFxxxS/P	8	0	270	236,000

The Temperature Humidity (TH) Test

The TH test is conducted under the conditions of 85°C and 85% R.H. Package preconditioning is performed on the testing samples prior to the TH test.

Summary

Table 2-107: **Summary of TH Test Results**

Device Family	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC17(S)xxx/(X)L	3	0	187	187,231
XC17Vxxx	1	0	44	44,264

Data

Table 2-108: **TH Test Results of Si Gate CMOS Device Type XC17(S)xxx/(X)L**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC1701L	2	0	154	154,000
XC17S40XL	1	0	33	33,231
XC17(S)xxx/(X)L	3	0	187	187,231

Table 2-109: **TH Test Results of Si Gate CMOS Device Type XC17Vxxx/XC17SxxxA**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC17S200A	1	0	44	44,264

Autoclave Test

The autoclave test is conducted under the conditions of 121°C, 100% R.H. (unbiased) and 29.7 PSI. Package preconditioning is performed on the testing samples prior to the autoclave stress test.

Summary

Table 2-110: **Summary of Autoclave Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC17(S)xxx/(X)L/E	4	0	168	16,128
XC17Vxxx/XC17SxxxA	1	0	51	4,896

Data

Table 2-111: **Autoclave Test Results for Si Gate CMOS Device Type XC17(S)xxx/(X)L/E**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC17128E	2	0	90	8,640
XC17256E	1	0	33	3,168
XC17S100XL	1	0	45	4,320
XC17(S)xxx/(X)L/E	4	0	168	16,128

Table 2-112: **Autoclave Test Results for Si Gate CMOS Device Type XC17Vxxx/XC17SxxxA**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC17V16	1	0	51	4,896

Temperature Cycling Test (TC)

The TC test is conducted under the conditions of predefined maximum and minimum temperatures and in air-to- air environment. Package precondition is performed on the testing samples prior to the TC test.

Summary

Table 2-113: **Summary of TC Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC17(S)xxx/(X)L/E	5	0	245	265,529
XC17Vxxx/XC17SxxxA	6	0	289	304,257
XC18Vxxx	28	0	1,206	1,161,000
XCFxxxS/P	8	0	360	291,060

Data

Table 2-114: **TC Test Results for Si Gate CMOS Device XC17(S)xxx/(X)L/E**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC1701L	B: -55°C to +125°C	1	0	76	80,104
XC17128E	B: -55°C to +125°C	2	0	90	104,715
XC17S40XL	B: -55žC to +125žC	1	0	34	34,000
XC17S100XL	B: -55°C to +125°C	1	0	45	46,710
XC17(S)xxx/(X)L/E	B	5	0	245	265,529

Table 2-115: **TC Test Results for Si Gate CMOS Device Type XC17Vxxx/XC17SxxxA**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC17S50A	B: -55°C to +125°C	2	0	121	128,700
XC17S200A	B: -55°C to +125°C	3	0	124	131,557
XCS17S300A	B: -55°C to +125°C	1	0	44	44,000
XC17Vxxx/XC17SxxxA	B	6	0	289	304,257

Table 2-116: **TC Test Results for Si Gate CMOS Device Type XC18Vxxx**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC18V01	C: -65°C to +150°C	11	0	442	419,500
XC18V02	C: -65°C to +150°C	4	0	179	156,500
XC18V04	C: -65°C to +150°C	13	0	585	585,000
XC18V512	C: -65°C to +150°C	1	0	45	45,000
XC18Vxxx	C	28	0	1,206	1,161,000

Table 2-117: **TC Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XCF08P	C: -65°C to +150°C	2	0	90	88,560
XCF16P	C: -65°C to +150°C	1	0	45	45,000
XCF32P	C: -65°C to +150°C	5	0	225	157,500
XCFxxxS/P	C	8	0	360	291,060

High Accelerated Stress Test (HAST)

The HAST test is conducted under the conditions of 130°C, 85% R.H. and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the HAST test.

Summary

Table 2-118: **Summary of HAST Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC18Vxxx	28	0	1,111	106,656

Data

Table 2-119: **HAST Test Results of Si Gate CMOS Device Type XC18Vxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC18V01	9	0	342	32,832
XC18V02	5	0	225	21,600
XC18V04	13	0	499	47,904
XC18V512	1	0	45	4,320
XC18Vxxx	28	0	1,111	106,656

Data Retention Bake Test

The data retention bake test is conducted under the condition of 150ºC ambient temperature. The devices are programmed prior to the bake test.

Summary

Table 2-120: **Summary of Data Retention Bake Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC17(S)xxx/(X)L/E	5	1	292	296,571
XC17Vxxx/XC17SxxxA	3	1	116	116,019
XC18Vxxx	29	0	1,161	1,093,500
XCFxxxS/P	11	0	344	229,560

Data

Table 2-121: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC17(S)xxx/(X)L/E**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC1701L	2	0	153	157,232
XC1702L	2	0	89	89,445
XC1704L	1	1(1)	50	49,894
XC17(S)xxx/(X)L/E	5	1	292	296,571

Note:

1. Failure at post 502 hrs due to program disturb.

Table 2-122: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC17Vxxx/XC17SxxxA**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC17S200A	1	0	45	45,045
XC17V04	1	1(1)	45	44,766
XC17V16	1	0	26	26,208
XC17Vxxx/17SxxxA	3	1	116	116,019

Note:

1. Failure at post 501 hours due to single bit charge loss. Process improvement has been implemented.

Table 2-123: **Data Retention Bake Test Results for Si Gate CMOS Devices Type XC18Vxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC18V01	9	0	347	324,500
XC18V02	5	0	180	135,000
XC18V04	14	0	589	589,000
XC18V512	1	0	45	45,000
XC18Vxxx	29	0	1,161	1,093,500

Table 2-124: **Data Retention Bake Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCF08P	2	0	61	23,560
XCF16P	2	0	68	68,000
XCF32P	7	0	215	138,000
XCFxxxS/P	11	0	344	229,560

Program / Erase Endurance Test

The Program / Erase Endurance test is conducted under nominal voltage and room temperature.

Qualification Data

Table 2-125: **Program / Erase Endurance Test Results of Si Gate CMOS Device Type XC18Vxxx, XCFxxxS/P**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC18V04	1	0	32	640,000
XCF08P	1	0	16	320,000
XCF16P	2	0	93	1,860,000
XCF32P	2	0	93	1,860,000

The CPLD Products

High-Temperature Operating Life (HTOL) Tests

The HTOL test is conducted under the conditions of 125°C ambient temperature, maximum V_{DD} and either dynamic or static. The failure rate (FIT) calculation in the following tables is based on the assumption of 0.7 eV activation energy and 60% confidence level.

Summary

Table 2-126: **Summary of HTOL Test Results**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC95xxx	13	1	594	692,591	1,081,580	24
XC95xxxXL	23	0	1,566	1,733,398	2,261,805	5
XC95xxxXV	11	0	612	712,897	754,387	16
XCRxxxXL	10	1	511	712,643	1,073,956	24
XC2Cxxx/A	15	0	934	980,209	1,008,469	12

Note:

1. Each of the failures listed in the table above is also listed in each family device table with failure analysis results in the footnote.

Data

Table 2-127: **HTOL Test Results for 0.5 µm Si Gate CMOS Device Type XC95xxx**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC95108	2	1(1)	90	45,253	120,123	
XC95144	4	0	211	267,878	455,396	
XC95216	3	0	135	135,000	135,000	
XC95288	1	0	48	97,440	97,440	
XC9536	1	0	45	45,000	45,000	
XC9572	2	0	65	102,020	228,621	
XC95xxx	13	1	594	692,591	1,081,580	24 FIT

Note:

1. No defect found at post 500 hours

Table 2-128: **HTOL Test Results of 0.35 µm Si Gate CMOS Devices Type XC9xxxXL**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC9572XL	6	0	426	508,971	624,329	
XC95144XL	10	0	713	701,317	996,760	
XC95288XL	7	0	427	523,110	640,716	
XC95xxxXL	23	0	1,566	1,733,398	2,261,805	5 FIT

Table 2-129: **HTOL Test Results of 0.25 µm Si Gate CMOS Devices Type XC9xxxXV**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC9572XV	1	0	76	38,000	38,000	
XC95144XV	2	0	121	166,945	166,945	
XC95288XV	8	0	415	507,952	549,442	
XC95xxxXV	11	0	612	712,897	754,387	16 FIT

Table 2-130: **HTOL Test Results of 0.35 µm Si Gate CMOS Device Type XCRxxxXL**

Devices	Lot Qty	Failures	Device on Test	Actual Device Hours ($T_A \geq 125^oC$)	Equivalent Device Hours @ $T_J=°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XCR3032XL	2	0	121	197,076	271,528	
XCR3064XL	3	0	166	173,384	460,245	
XCR3256XL	2	1(1)	89	112,525	112,525	
XCR3384XL	1	0	42	85,302	85,302	
XCR3512XL	2	0	92	144,356	144,356	
XCRxxxXL	10	1	511	712,643	1,073,956	24 FIT

Note:

1. ILD defect at M2 to M1 at post 48 hours.

Table 2-131: **HTOL Test Results of 0.18 µm Si Gate CMOS Device Type XC2Cxxx/A**

Device Family	Lot Qty	Fail Qty	Device Qty	Actual Device Hours @ $T_A \geq 125^oC$	Equivalent Device Hours @ $T_J=125°C$	Failure Rate at 60% CL and $T_J=55°C$ (FIT)
XC2C64A	3	0	77	77,000	77,000	
XC2C256	4	0	308	308,462	309,051	
XC2C128	1	0	76	76,304	76,304	
XC2C384	4	0	307	307,000	331,703	
XC2C512	3	0	166	211,443	214,411	
XC2Cxxx/A	15	0	934	980,209	1,008,469	12 FIT

The Temperature Humidity Bias (THB) Test

The THB test is conducted under the conditions of 85C, 85% R.H. and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the THB test.

Summary

Table 2-132: **Summary of THB Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC95xxxXL	5	1	270	278,452
XCRxxxXL	1	0	45	46,800
XC2Cxxx/A	14	0	1,004	1,025,353

Note:

Each of the failures listed in the table above is also listed in each family device table with failure analysis results in the footnote.

Data

Table 2-133: **THB Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC9572XL	2	0	88	88,000
XC995144XL	2	0	152	161,272
XC95288XL	1	1(1)	30	29,180
XC95xxxXL	5	1	270	278,452

Note:

1. No defect found at post 180 hrs.

Table 2-134: **THB Test Results for Si Gate CMOS Device Type XCRxxxXL**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCR3064XL	1	0	45	46,800

Table 2-135: **THB Test Results for Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2C256	7	0	505	523,425
XC2C384	3	0	229	229,000
XC2C64A	4	0	270	272,928
XC2Cxxx/A	14	0	1,004	1,025,353

The Temperature Humidity (TH) Test

The TH test is conducted under the conditions of 85°C and 85% R.H. Package preconditioning is performed on the testing samples prior to the TH test.

Summary

Table 2-136: **Summary of TH Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC95xxx	2	0	75	75,330
XC95xxxXL	2	0	86	88,098
XCRxxxXL	8	0	401	405,777
XC2Cxxx/A	5	0	255	256,818

Table 2-137: **TH Test Results of Si Gate CMOS Devices Type XC95xxxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC95144	1	0	30	30,060
XC95216	1	0	45	45,270
XC95xxx	2	0	75	75,330

Table 2-138: **TH Test Results of Si Gate CMOS Devices Type XC95xxxXL(shrink)**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC9572XL	1	0	44	45,804
XC95288XL	1	0	42	42,294
XC95xxxXL	2	0	86	88,098

Table 2-139: **TH Test Results of 0.35 µm Si Gate CMOS Device Type XCRxxxXL**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCR3064XL	2	0	85	85,250
XCR3128XL	1	0	45	46,125
XCR3256XL	1	0	45	45,180
XCR3512XL	4	0	226	229,222
XCRxxxXL	8	0	401	405,777

Table 2-140: **TH Test Results of Si Gate CMOS Devices Type XC2Cxxx/A**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2C64A	2	0	89	89,315
XC2C256	3	0	166	167,503
XC2Cxxx/A	5	0	255	256,818

Autoclave Test

The autoclave test is conducted under the conditions of 121°C, 100% R.H. (unbiased) and 29.7 PSI. Package preconditioning is performed on the testing samples prior to the autoclave stress test.

Summary

Table 2-141: **Summary of Autoclave Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC95xxxXL	2	0	86	8,256

Data

Table 2-142: **Autoclave Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC9572XL	2	0	86	8,256

Temperature Cycling Test (TC)

The TC test is conducted under the conditions of predefined maximum and minimum temperatures and in air-to-air environment. Package precondition is performed on the testing samples prior to the TC test.

Summary

Table 2-143: **Summary of TC Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC95xxx	2	0	90	90,810
XC95xxxXL	12	0	708	821,582
XCRxxxXL	10	0	495	555,127
XC2Cxxx/A	22	0	1,427	1,471,249

Data

Table 2-144: **TC Test Results for Si Gate CMOS Device Type XC95xxx**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC95144	B: -55°C to +125°C	1	0	45	45,810
XC95216	B: -55°C to +125°C	1	0	45	45,000
XC95xxx	B	2	0	90	90,810

Table 2-145: **TC Test Results for Si Gate CMOS Device Type XC95xxxL**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC95144XL	B: -55°C to +125°C	4	0	308	406,714
XC95288XL	B: -55°C to +125°C	3	0	146	146,473
XC9572XL	B: -55°C to +125°C	5	0	254	268,395
XC95xxxXL	B	12	0	708	821,582

Table 2-146: **TC Test Results of Si Gate CMOS Device Type XCRxxxXL**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XCR3064XL	B: -55°C to +125°C	4	0	179	199,599
XCR3128XL	B: -55°C to +125°C	1	0	44	46,728
XCR3256XL	B: -55°C to +125°C	2	0	105	133,560
XCR3512XL	B: -55°C to +125°C	3	0	167	175,240
XCRxxxXL	B	10	0	495	555,127

Table 2-147: **TC Test Results of Si Gate CMOS Device Type XC2Cxxx/A**

Device	Stress Cond	Lot Qty	Fail Qty	Device Qty	Total Device Cycles
XC2C64A	B: -55°C to +125°C	5	0	317	331,407
XC2C256	B: -55°C to +125°C	10	0	673	679,784
XC2C384	B: -55°C to +125°C	5	0	320	330,854
XC2C512	B: -55°C to +125°C	2	0	117	129,204
XC2Cxxx/A	B	22	0	1,427	1,471,249

High Accelerated Stress Test (HAST)

The HAST test is conducted under the conditions of 130°C, 85% R.H. and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the HAST test.

Summary

Table 2-148: **Summary of HAST Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCR3064XL	1	0	45	4,500

Data Retention Bake Test

The Data Retention Bake Test is conducted under the condition of 150ºC. The devices are programmed prior to the bake test.

Summary

Table 2-149: **Summary of Data Retention Bake Test Results**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC95xxx	3	0	133	134,571
XC95xxxXL	12	0	559	722,157
XC95xxxXV	2	0	89	89,621
XCRxxxXL	3	0	167	167,931
XC2Cxxx/A	7	0	366	415,081

Data

Table 2-150: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC95xxx**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC95144	1	0	43	43,851
XC95216	1	0	45	45,270
XC95288	1	0	45	45,450
XC95xxx	3	0	133	134,571

Table 2-151: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC9572XL	3	0	135	135,720
XC95144XL	4	0	243	404,600
XC95288XL	5	0	181	181,837
XC95xxxXL	12	0	559	722,157

Table 2-152: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC95xxxXV**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC95288XV	2	0	89	89,621

Table 2-153: **Data Retention Bake Test Results of Si Gate CMOS Devices Type XCRxxxXL**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCR3384XL	1	0	45	45,315
XCR3512XL	2	0	122	122,616
XCRxxxXL	3	0	167	167,931

Table 2-154: **Data Retention Bake Test Results of Si Gate CMOS Devices Type XC2Cxxx/A**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC2C128	1	0	73	97,058
XC2C256	3	0	163	187,508
XC2C384	1	0	45	45,000
XC2C64A	2	0	85	85,515
XC2Cxxx/A	7	0	366	415,081

Program / Erase Endurance Test

The Program / Erase Endurance test is conducted under nominal voltage and predefined temperature.

Qualification Data

Table 2-155: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxx; Test Condition at 55°C**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC9536	1	0	29	290,000
XC95108	1	0	80	875,120
XC95xxx	2	0	109	1,165,120

Table 2-156: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxx; Test Condition at -40°C**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC9536	2	0	64	5,088,000

Table 2-157: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxxXL; Test Condition at -40°C**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC95144XL	1	0	21	420,000

Table 2-158: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxxXL; Test Condition at 70°C**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC95144XL	1	0	32	320,000

Table 2-159: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxxXV; Test Condition at 70°C**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XC95144XV	1	0	32	320,000

Table 2-160: **Erase Endurance Test Results of Si Gate CMOS Device Type XCRxxx**
Table 2-161: **/XL**

Device	Lot Qty	Fail Qty	Device Qty	Total Device Hours
XCR3128	1	0	10	10,000
XCR3032XL	2	0	57	684,000

Chapter 3

Results by Package Type

Reliability Data for Nonhermetic Packages

PD-8

Table 3-1: **Test Results for Devices Type XC17128E, XC17256E, XC17S200A, XC17S40XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	4	0	158	179,417
Pressure Pot	2	0	78	7,488
Temperature Humidity	1	0	33	33,231
85ºC /85% RH With Bias	3	0	111	112,452
High Temperature Storage Life	1	0	45	45,045

SO-20

Table 3-2: **Test Results for Devices Type, XC17S50A, XC17S100/XL, XC17V01, XC18V01, XC18V512**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-65ºC to +150ºC)	3	0	127	127,000
Temp Cycle (-55ºC to +125ºC)	3	0	166	175,410
Pressure Pot	1	0	45	4,320
85ºC /85% RH With Bias	3	0	167	167,090
HAST	4	0	172	16,512
High Temperature Storage Life	3	0	135	135,000

VO-20, 48

Table 3-3: **Test Results for Devices Type, XCF08P, XCF32P, XC18V01, XC18V02, XC18V04**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-65ºC to +150ºC)	20	0	854	807,560
85ºC /85% RH With Bias	7	0	270	270,000
HAST	12	0	480	46,080
High Temperature Storage Life	21	0	881	756,560

PC-44, 84

Table 3-4: **Test Results for Devices Type XC1704L, XC17V16, XC18V04, XC9572XL, XCR3064XL, XCS05, XCS10XL, XC4006E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-65ºC to +150ºC)	3	0	135	135,000
Temp Cycle (-55ºC to +125ºC)	6	0	263	279,260
Pressure Pot	2	0	92	8,832
85ºC /85% RH With Bias	3	0	130	132,340
Temperature Humidity	2	0	85	85,295
HAST	2	0	90	8,640
High Temperature Storage Life	7	1(1)	300	301,507

Note:

1. Failure at post 502 hrs due to program disturb.

PQ-100, 160, 208

Table 3-5: **Test Results for Devices Type XC2S50, XC3S200, XC3S400, XC4013E, XC4010XL, XC3S1500, XC95144, XC95216, XC95288XL, XC95288XV, XC2C384, XC2R3512XL, XCR3384XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	9	0	402	412,634
Pressure Pot	2	0	90	8,640
85ºC /85% RH With Bias	4	0	173	173,225
Temperature Humidity	2	0	75	75,330
High Temperature Storage Life	11	0	403	405,624

TQ-144

Table 3-6: **Test Results for Devices Type XC95144XL, XC2C256, XC2S50E, XC2S100/E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	8	0	406	417,933
Pressure Pot	1	0	77	7,392
85ºC /85% RH With Bias	9	0	470	485,626
Temperature Humidity	3	0	130	130,990
High Temperature Storage Life	5	0	240	401,835

VQ-44, 100

Table 3-7: **Test Results for Devices Type XC1702L, XC17S300A, XC17V02, XC17V04, 18V02 XC18V04, XCS30, XCS20XL, XC9572XL, XCF04S, XCR3064XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-65ºC to +150ºC)	11	0	495	472,500
Temp Cycle (-55ºC to +125ºC)	5	0	239	243,890
Pressure Pot	1	0	45	4,320
85ºC /85% RH With Bias	3	0	133	133,765
Temperature Humidity	2	0	105	105,930
HAST	12	0	459	44,244
High Temperature Storage Life	16	1(1)	647	626,071

Note:

1. Failure at post 501 hours due to single bit charge loss. Process improvement has been implemented.

HQ-208, 240

Table 3-8: **Test Results for Devices Type XCV400 (shrink), XCV600(shrink), XCV600E, XC95216, XC95288**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	3	0	135	139,995
Pressure Pot	1	0	45	4,320
Temperature Humidity	2	0	90	90,315
High Temperature Storage Life	3	0	119	119,807

BG-256

Table 3-9: **Test Results for Devices Type XCS40XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	2	0	45	47,385

BG-432, 560

Table 3-10: **Test Results for Devices Type XCV400E, XCV1000E, XC1600E, XC4062XLA**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	6	0	254	260,297
85ºC /85% RH With Bias	5	0	215	216,794
Temperature Humidity	5	0	194	199,387

CS-48

Table 3-11: **Test Results for Devices Type XC9572XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	2	0	89	100,475
85ºC /85% RH With Bias	1	0	45	45,000
Temperature Humidity	1	0	44	45,804

CS-280

Table 3-12: **Test Results for Devices Type XC95288XL, XC95288XV, XCR3256XL, XCR3512XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	3	0	164	179,420
85ºC /85% RH With Bias	2	1(1)	59	59,420
Temperature Humidity	1	0	59	59,295

Note:

1. No defect found at post 180 hours

CP- 56

Table 3-13: **Test Results for Devices Type XCR3064XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-65ºC to +150ºC)	1	0	44	56,364
Temperature Humidity	1	0	45	45,090

CP- 132

Table 3-14: **Test Results for Devices Type XC2C128, XC2C256, XC3S500E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	3	0	112	113,980
85ºC /85% RH With Bias	2	0	66	70,284
Temperature Humidity	1	0	45	45,045
High Temperature Storage Life	3	0	146	194,116

FS-48

Table 3-15: **Test Results for Devices Type XCF08P, XCF16P, XCF32P**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-65ºC to +150ºC)	5	0	225	180,000
85ºC /85% RH With Bias	4	0	135	101,000
High Temperature Storage Life	8	0	215	180,000

FG-256

Table 3-16: **Test Results for Devices Type XC2V250, XC2V500**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	1	0	40	40,200
Temperature Humidity	2	0	90	90,810

FG-320

Table 3-17: **Test Results for Devices Type XC2V250, XC2V500**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temperature Humidity	1	0	78	81,822

FG- 324, 456

Table 3-18: **Test Results of Devices Type XC2V250, XC2S200, XC3S1000, XC3S1500, XC2S300E, XCR3512XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	6	0	292	311,912
Temperature Humidity	6	0	287	288,411
High Temperature Storage Life	1	0	77	77,231

FG-676

Table 3-19: **Test Results for Devices Type XC2VP20, XC2VP30, XC3S1000, XC3S1400A, XCE2V2000, XCV600E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	5	0	244	251,298
85ºC /85% RH With Bias	1	0	18	18,018
Temperature Humidity	3	0	149	149,469
High Temperature Storage Life	3	0	168	168,549

FG-680

Table 3-20: **Test Results for Devices Type, XCV2000E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	3	0	135	135,495
Temperature Humidity	3	0	134	134,896
High Temperature Storage Life	1	0	33	8712

FG-1156

Table 3-21: **Test Results for Devices Type), XC3S5000, XCV2000E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	2	0	122	122,540
Temperature Humidity	1	0	77	77,462

FT-256

Table 3-22: **Test Results for Devices Type XCR3512XL, XC2S150E, XC2S300E, XC2C512, XC3S1000, XC3S200A**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	13	0	829	925,424
85ºC /85% RH With Bias	6	0	393	397,300
Temperature Humidity	3	0	125	125,670
HAST	1	0	40	4,000
High Temperature Storage Life	1	0	26	26,286

QF-32

Table 3-23: **Test Results for Devices Type XC2C64A**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	1	0	40	40,200
85ºC /85% RH With Bias	1	0	45	45,225
Temperature Humidity	1	0	45	45,315
High Temperature Storage Life	1	0	40	42,620

BF-957

Table 3-24: **Test Results for Devices Type XC2V3000, XC2V4000**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	3	2(1)	132	139,782
Temperature Humidity	3	0	135	135,585

Note:

1. Two failures at post 1,013 cycles were due to via misalignment at the package substrate. Tighter alignment limits have been implemented.

FF-672, 668

Table 3-25: **Test Results for Devices Type XC4VLX25, XC4VLX60, XC4VFX20, XC4VFX60**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	4	0	276	287,056
85ºC /85% RH With Bias	6	0	332	335,444
Temperature Humidity	2	0	111	111,616
High Temperature Storage Life	3	0	225	226,768

FF-1148, 1152

Table 3-26: **Test Results for Devices Type XC2V6000, XC4VLX60, XC4VLX100, XC4VLX160, XC4VFX60, XCE2V4000, XCE2VP40, XC2VP50**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	7	0	293	296,588
Temp Cycle (-40ºC to +125ºC	1	0	43	43,000
85ºC /85% RH With Bias	2	0	67	68,843
Temperature Humidity	5	0	141	141,656

FF-1513, 1517

Table 3-27: **Test Results for Devices Type XC4VLX100, XC4VLX200, XC4VLX160**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	18	2(1)	695	724,704
85ºC /85% RH With Bias	1	0	45	46,755
Temperature Humidity	2	0	73	73,252

Note:

1. Two failures at post 500 cycles were due to defective via at package substrate. Via resistance measurement with tightened limits has been implemented for screening out the defect.

FF-1704

Table 3-28: **Test Results for Devices Type XC2VP100, XC2VP70**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	2	0	79	78,420

SF-363

Table 3-29: **Test Results for Devices Type XC4VLX25**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55ºC to +125ºC)	2	0	152	157,624
85ºC /85% RH With Bias	1	0	40	40,000
Temperature Humidity	2	0	120	120,856
High Temperature Storage Life	1	0	77	77,385

Reliability Data for Hermetic Packages

Reliability Data for PGA Packages

Table 3-30: **Tests of Packages Type PG-84, -120, -132, -156, -175, -191, -223, -299, -475**

Code	Test	Sample Qty	Failures	Total Device Cycles
B2	Resistance to Solvents	54	0	
B3	Solderability	48	0	
B5	Bond Strength	60	0	
D1	Physical Dimension	15	0	
D2	Lead Integrity	3	0	
	Seal			
D3	Thermal Shock	15	0	225
	Temperature Cycle			1,500
	Seal			
	Visual Examination			
	End-Point Elect.			
	Parametrics			
D4	Mechanical Shock	15	0	
	Vibration, Var. Freq.			
	Constant Accel.			
	Seal			
	Visual Examination			
	End-Point Elec. Para.			
D5	Salt Atmosphere	15	0	
	Seal			
	Visual Examination			
D6	Internal Water-Vapor Content	3	0	
D7	Adhesion of lead finish	3	0	

Reliability Data for CB Packages

Table 3-31: **Tests of Packages Type CB-100, -164, -196, -228**

Code	Test	Sample Qty	Failures	Total Device Cycles
B2	Resistance to Solvents	126	0	
B3	Solderability	48	0	
B5	Bond Strength	56	0	
D1	Physical Dimension	30	0	
D2	Lead Integrity	6	0	
	Seal			
D3	Thermal Shock	15	0	225
	Temperature Cycle			1,500
	Seal			
	Visual Examination			
	End-Point Elect.			
	Parametrics			
D4	Mechanical Shock	15	0	
	Vibration, Var. Freq.			
	Constant Accel.			
	Seal			
	Visual Examination			
	End-Point Elec. Para.			
D5	Salt Atmosphere	15	0	
	Seal			
	Visual Examination			
D6	Internal Water-Vapor Content	3	0	
D7	Adhesion of lead finish	3	0	

Reliability Data for DD-8 Packages

Table 3-32: **Tests of Packages Type DD-8**

Code	Test	Sample Qty	Failures	Total Device Cycles
B2	Resistance to Solvents	9	0	
B3	Solderability	15	0	
B5	Bond Strength	12	0	
D1	Physical Dimension	30	0	
D2	Lead Integrity	6	0	
	Seal			
D3	Thermal Shock	15	0	225
	Temperature Cycle			1,500
	Seal			
	Visual Examination			
	End-Point Elect.			
	Parametrics			
D4	Mechanical Shock	15	0	
	Vibration, Var. Freq.			
	Constant Accel.			
	Seal			
	Visual Examination			
	End-Point Elec. Para.			
D5	Salt Atmosphere	15	0	
	Seal			
	Visual Examination			
D6	Internal Water-Vapor Content	3	0	
D7	Adhesion of lead finish	3	0	
D8	Lead Torque	5	0	

Reliability Data for Chip Scale CC-44 Packages

Table 3-33: **Tests of Packages Type Chip Scale CC-44**

Code	Test	Sample Qty	Failures	Total Device Cycles
B2	Resistance to Solvents	27	0	
B3	Solderability	30	0	
B5	Bond Strength	36	0	
D1	Physical Dimension	45	0	
D2	Lead Integrity	9	0	
	Seal			
D3	Thermal Shock	45	0	675
	Temperature Cycle			4,500
	Seal			
	Visual Examination			
	End-Point Elect.			
	Parametrics			
D4	Mechanical Shock	30	0	
	Vibration, Var. Freq.			
	Constant Accel.			
	Seal			
	Visual Examination			
	End-Point Elec. Para.			
D5	Salt Atmosphere	45	0	
	Seal			
	Visual Examination			
D6	Internal Water-Vapor Content	9	0	
D7	Adhesion of lead finish	9	0	
D8	Lead Torque	15	0	

Reliability Data for CF-1144 Packages

Table 3-34: **Tests of Packages Type CF-1144**

Code	Test	Sample Qty	Failures	Total Device Hrs/Cycles
B2	Resistance to Solvents	3	0	
D3	Thermal Shock	15	0	225
	Temperature Cycle			1,500
	Seal			
	Visual Examination			
	End-Point Elect.			
D3	Thermal Shock	15	0	225
	End-Point Elect.			
	Parametrics			
D4	Mechanical Shock	15	0	
	Vibration, Var. Freq.			
	Constant Accel.			
	Seal			
	Visual Examination			
	End-Point Elec. Para.			
	High Temperature Storage	10	0	10,340
	Temp Cycle (-65 to +155ºC)	20	0	10,000
	Temp Cycle (-55 to +125ºC)	22	0	22,814

Reliability Data for Pb-Free Packages

PDG– 8

Table 3-35: **Test Results for Devices Type XC1701L, XC17256E, XC17S200A**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	2	0	110	119,816
Pressure Pot	1	0	33	3,168
85ºC /85% RH With Bias	2	0	110	110,957
Temperature Humidity	1	0	77	77,000
High Temperature Storage Life	1	0	76	76,228

BGG-256

Table 3-36: **Test Results for Devices Type XCS40XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	2	0	88	91,116
Temperature Humidity	1	0	45	46,350

BGG-432, 560

Table 3-37: **Test Results for Devices Type XCV600E (shrink), XCV1000E (shrink), XC4062XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	3	0	204	209,629
85ºC /85% RH With Bias	1	0	45	45,630
Temperature Humidity	2	0	122	122,854
High Temperature Storage Life	1	0	74	74,370

CPG-56

Table 3-38: **Test Results for Devices Type XC2C64/A**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	1	0	41	41,861
85ºC /85% RH With Bias	1	0	44	44,000

CPG-132

Table 3-39: **Test Results for Devices Type XC2C256, XC2C128, XC3S50, XC3S300E, XC3S500E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	9	0	668	686,220
85ºC /85% RH With Bias	5	0	382	387,825
Temperature Humidity	3	0	202	202,901
High Temperature Storage Life	6	0	423	472,643

CSG-48

Table 3-40: **Test Results of Devices Type XC9572XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	1	0	45	45,045

CSG-144

Table 3-41: **Test Results of Devices Type XC95144XL, XCR3128XL, XCV200E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	5	0	351	452,894
85ºC /85% RH With Bias	2	0	152	161,272
Temperature Humidity	1	0	45	46,125
High Temperature Storage Life	1	0	45	45,135

CSG-280

Table 3-42: **Test Results of Devices Type XC95288XV, XCR3512XL, XCR3256XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	3	0	150	178,920
85ºC /85% RH With Bias	1	0	30	30,240
Temperature Humidity	2	0	104	104,475

FGG-256

Table 3-43: **Test Results of Devices Type XCV300E(shrink)**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	1	0	77	77,539

FGG-320

Table 3-44: **Test Results of Devices Type XC3S1500, XCV3S1600E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	1	0	45	45,315
Temperature Humidity	2	0	123	126,957
High Temperature Storage Life	1	0	77	77,616

FGG-400

Table 3-45: **Test Results of Devices Type XC3S1600E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	1	0	45	47,385
Temperature Humidity	1	0	44	44,176

FGG-324, 456, 484

Table 3-46: **Test Results of Devices Type XC2C512, XC2V250, XC2VP4, XC2S300E, XC3S1500, XC3S1600E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	9	0	555	568,536
85ºC /85% RH With Bias	3	0	231	236,544
Temperature Humidity	3	0	152	152,826
High Temperature Storage Life	3	0	167	167,591

FGG-676

Table 3-47: **Test Results of Devices Type XCV800, XCV600E, XC2V3000, XC2VP20, XC2VP30, XC2VP40, XC2S600E, XC3S1000, XC3S1500, XC3S2000, XC3S1400A**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	18	0	1,261	1,323,692
85ºC /85% RH With Bias	10	0	638	647,287
Temperature Humidity	9	0	624	632,017
High Temperature Storage Life	9	0	593	599,370

FGG-680

Table 3-48: **Test Results of Devices Type XCV1000E(shrink)**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	1	0	45	45,495

FGG-1156

Table 3-49: **Test Results of Devices Type XC3S4000, XC3S5000, XCV2000E(shrink)**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	4	0	217	244,383
Temperature Humidity	2	0	72	72,370
High Temperature Storage Life	1	0	77	77,616

FTG-256

Table 3-50: **Test Results for Devices Type, XC2C256, XC2C512, XC2S150E, XC2S300E, XC2S400E, XC3S1000, XC3S200A, XCR3512XL**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	16	0	1,135	1,250,786
85ºC /85% RH With Bias	9	0	594	598,126
Temperature Humidity	2	0	121	123,959
HAST	1	0	42	4,032
High Temperature Storage Life	5	0	304	306,198

PQG-160, 208

Table 3-51: **Test Results of Devices Type XC95144, XC95216, XC2S300E, XC3S400, XC3S500E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	7	1(2)	378	385,337
85ºC /85% RH With Bias	4	1(1)	274	279,815
Temperature Humidity	4	0	165	165,960
High Temperature Storage Life	3	0	166	167,913

Notes:

1. Failure at post 1,075 hours - metal 2 defect. New PR coating recipe was implemented for M2 to M5.
2. Failure at post 1,146 cycle due to random defect.

HQG- 240

Table 3-52: **Test Results of Devices Type XCV1000E (shrink), XC5215, XCV600**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125žC)	4	0	190	195,323
Pressure Pot	1	0	45	4,320
Temperature Humidity	1	0	45	45,855
High Temperature Storage Life	1	0	45	45,180

PCG-44, 84

Table 3-53: **Test Results for Devices Type XC9572XL, XCS05**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	2	0	83	86,120
Pressure Pot	1	0	41	3,936
85ºC /85% RH With Bias	1	0	40	40,000

SOG-20

Table 3-54: **Test Results for Devices Type XC1701, XC17S50A**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-65 to +150ºC)	1	0	77	79,464
85ºC /85% RH With Bias	2	0	154	154,000
Temperature Humidity	1	0	77	77,000
High Temperature Storage Life	1	0	77	81,004

VQG- 44, 64, 100

Table 3-55: **Test Results of Devices Type XCS30XL, XC18V04, XC2C64A, XC2C256, XC9572XL, XC3S200, XC3S250E, XC3S100E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	14	0	1,053	1,103,671
85ºC /85% RH With Bias	8	0	615	625,857
Temperature Humidity	3	0	197	201,965
HAST	1	0	45	4,320
High Temperature Storage Life	5	0	257	305,560

VOG - 20, 48

Table 3-56: **Test Results of Devices Type XCF08P, XC18V04**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-65 to +150ºC)	1	0	45	43,560
HAST	1	0	45	4,320
High Temperature Storage Life	3	0	135	135,000

TQG-100, 144

Table 3-57: **Test Results of Devices Type XC2S100E, XC2S100, XC95144XL, XC95288XL, XC2C384, XCV100, XC3S400, XC3S250E**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	10	0	698	713,687
85ºC /85% RH With Bias	7	0	501	505,890
Temperature Humidity	3	0	156	158,252
High Temperature Storage Life	4	0	175	175,900

FFG-672, 668

Table 3-58: **Test Results of Devices Type XC2VP4, XC2VP7, XC2VP20, XC4VLX25, XC4VFX60**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	5	0	304	319,955
85ºC /85% RH With Bias	1	0	43	43,215
Temperature Humidity	1	0	43	43,043

FFG-1148, 1152

Table 3-59: **Test Results of Devices Type XC2VP20, XC2VP50, XC4VLX60, XC4VLX160, XC4VFX60**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	5	0	236	245,937
Temp Cycle (-40 to +125ºC)	1	0	43	43,000
Temperature Humidity	1	0	15	15,405

FFG-1513, 1517

Table 3-60: **Test Results of Devices Type XCE2VP50, XC2VP50, XC4VLX100, XC4VLX160, XC4LX200**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	19	5(1) (12 (3)	739	784,554
Temperature Humidity	1	0	45	47,475

Notes:

1. Two failures at post 500 cycles were due to defective via at package substrate. Via resistance measurement with tightened limits has been implemented for screening out the defect.
2. One failure at post 500 cycles due to substrate via defect. Process improved.
3. Two failure at 1079 cycles due to substrate via defect. Process improved.

FFG-1704

Table 3-61: **Test Results of Devices Type XC2VP70, XC2VP100**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	1	0	59	58,410
Temperature Humidity	1	0	22	22,000
High Temperature Storage Life	1	0	29	29,000

SFG-363

Table 3-62: **Test Results of Devices Type XC4VLX25**

Reliability Test	Lot Qty	Failures	Device on Test	Total Device Hrs/Cycles
Temp Cycle (-55 to +125ºC)	5	0	255	262,148
85ºC /85% RH With Bias	4	0	173	175,173
Temperature Humidity	3	0	124	124,744

Board-Level Reliability Tests, SnPb Eutectic

Xilinx FG676, FG900, FG1156, BF957, FF672, FF896, FF1152, and FF1704

Table 3-63: **Package Details (all dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FG676	27 x 27	676	1.00	0.60	0.46	SMD	17.8x17.8x0.3	0.56 Thk, 4-layer
FG680	40 x 40	680	1.00	0.60	0.46	SMD	20.3x20.3x0.3	0.98 Thk, 3-layer
FG900	31 x 31	900	1.00	0.60	0.46	SMD	17.0x17.0x0.3	0.56 Thk, 4-layer
FG1156	35 x 35	1156	1.00	0.60	0.46	SMD	23x21x0.3	0.56 Thk, 4-layer
BF957	40 x 40	957	1.27	0.75	0.61	SMD	22x20x0.7	1.152 Thk, 6-layer
FF672	27 x 27	672	1.00	0.60	0.53	SMD	12x10x0.7	1.152 Thk, 6-layer
FF896	31 x 31	896	1.00	0.60	0.53	SMD	10x10x0.7	1.152 Thk, 6-layer
FF1152	35 x 35	1152	1.00	0.60	0.53	SMD	22x20x0.7	1.152 Thk, 6-layer
FF1704	42.5 x 42.5	1704	1.00	0.60	0.53	SMD	26x22x0.7	1.152 Thk, 6-layer
CF1144	35 x 35	1144	1.00	0.52	0.80	SMD	22x20x0.7	1.59 Thk, 10-layer

Mother Board Design and Assembly Details

- 8-Layer, FR-4, 220x140x2.3622 mm Size, HASL Finish
- 0.5mm Pad Diameter/0.65 mm Solder Mask Opening (NSMD Pads)
- Board Layer Structure: Signal/GND/Signal/Power/Signal/GND/Signal/Power
- Power, GND Layer has 70% Metal. Internal Signal Layer has 40% metal.
- 0.1524 mm Laser Cut Stencil, 0.50 mm Aperture, Alpha Metals WS609 Paste

Test Condition

- 0 < >100ºC, 10 minutes dwells, 5 minutes ramps, 2 cycles/hour

Failure Criteria

- Continuous Scanning of Daisy Chain Nets (Every 2 minutes)
- **OPEN**: Resistance of Net > Threshold Resistance (300 ohms)
- **FAIL**: At Least 2 OPENs Within One Cycle, Log 15 FAILURES for Each Net

Table 3-64: **Summary of Test Results**

Package	Cycles Completed	# Tested	# Failed	First Failure (Cycles)	Characteristic Life (Cycles)
FG676	7027	30	30	4686	6012
FG680	4000	30	0	NA	NA
FG900	7027	28	28	4405	5344
FG1156	5000	32	25	2786	4892
BF957	4145	35	35	1958	3662
FF672	5840	30	30	3764	4881
FF896	7027	12	10	5607	6783
FF1152	4158	30	30	2668	3822
FF1704	3247	30	29	2126	3085
CF1144	5000	21	0	NA	NA

Weibull Plots

FG676

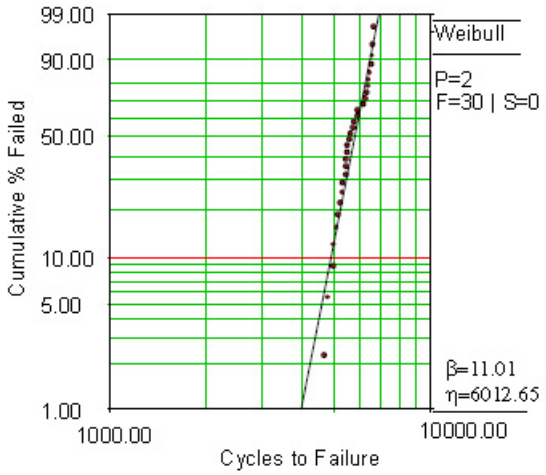

Figure 3-1: **Cycles to Failure in the Second-Level Reliability Tests for FG676**

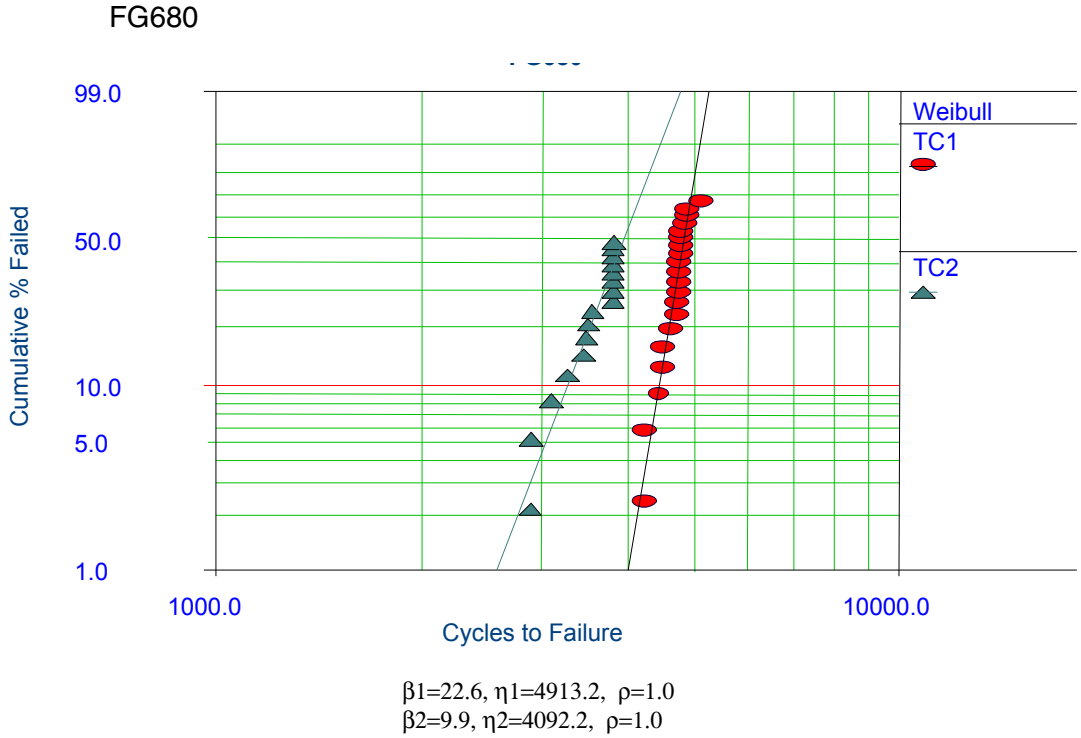

Figure 3-2: **Cycles to Failure in the Second-Level Reliability Tests for FG680**

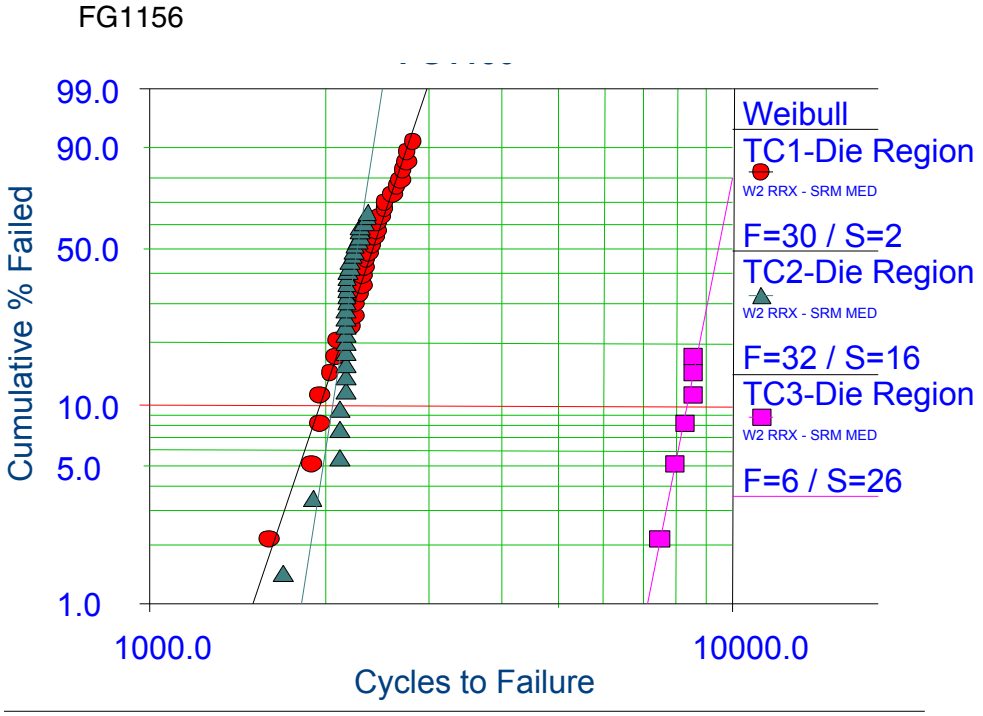

Figure 3-3: **Cycles to Failure in the Second-Level Reliability Tests for FG1156**

BF957

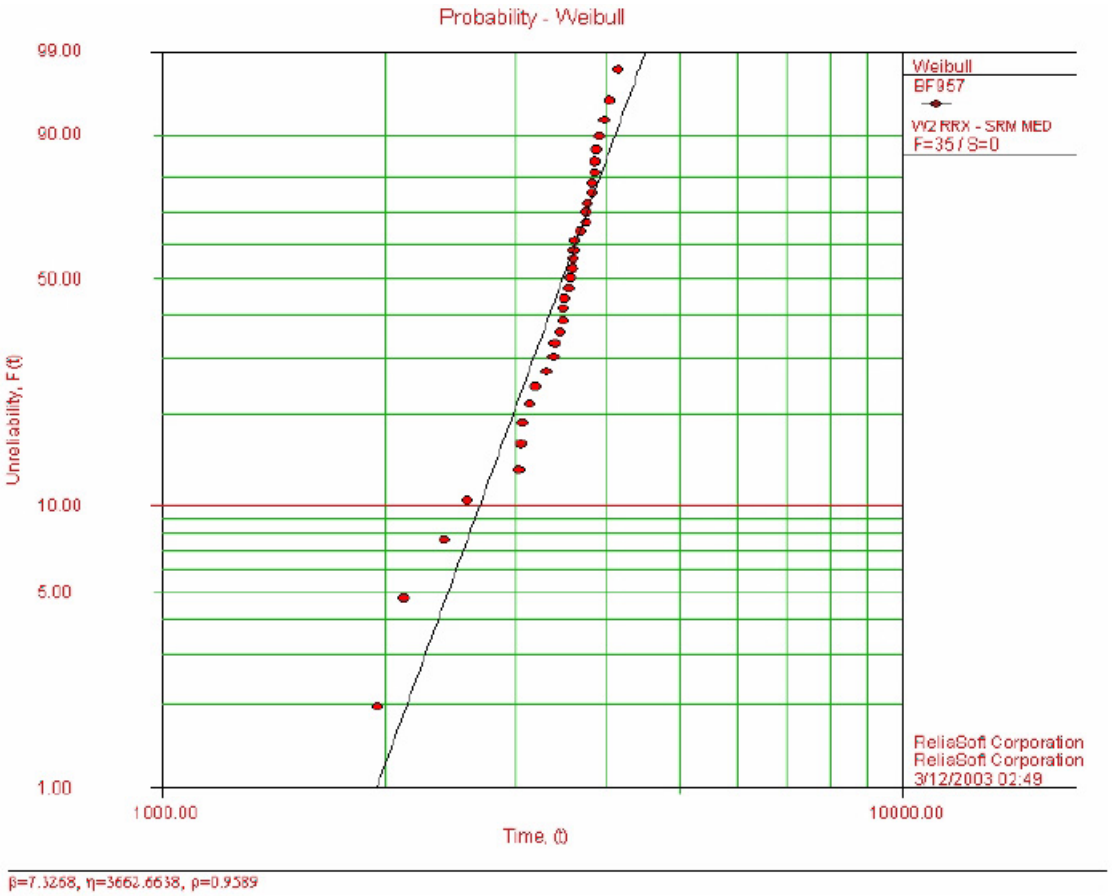

Figure 3-4: **Cycles to Failure in the Second-Level Reliability Tests for BF957**

FF672

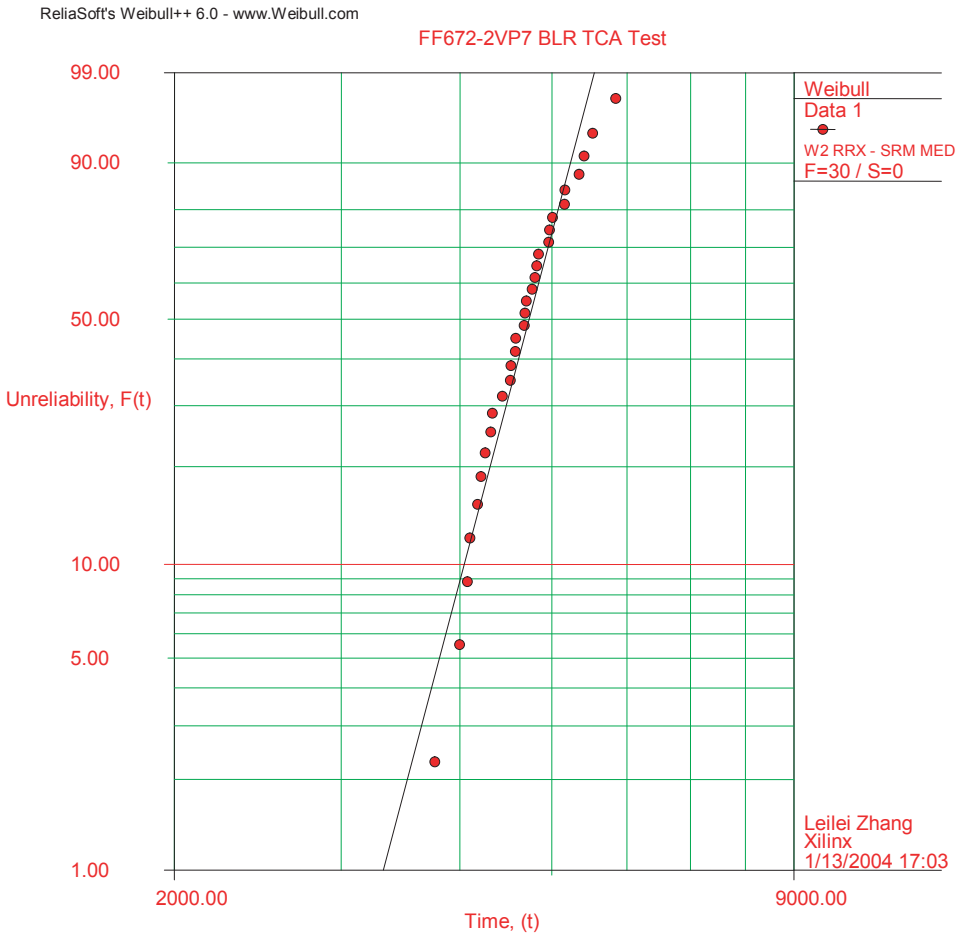

Figure 3-5: **Cycles to Failure in the Second-Level Reliability Tests for FF672**

FF896

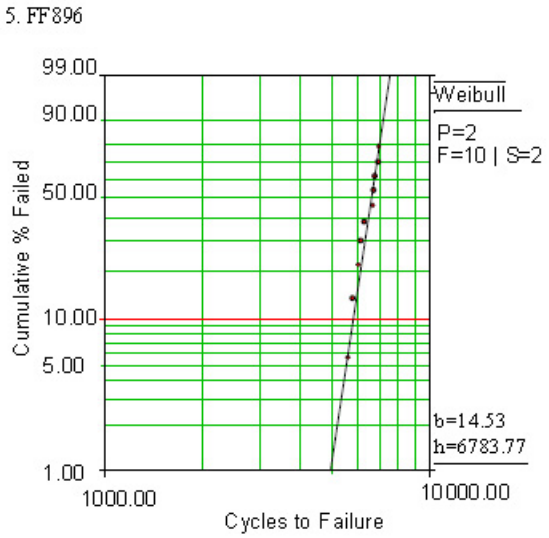

Figure 3-6: **Cycles to Failure in the Second-Level Reliability Tests for FF896**

FF1152

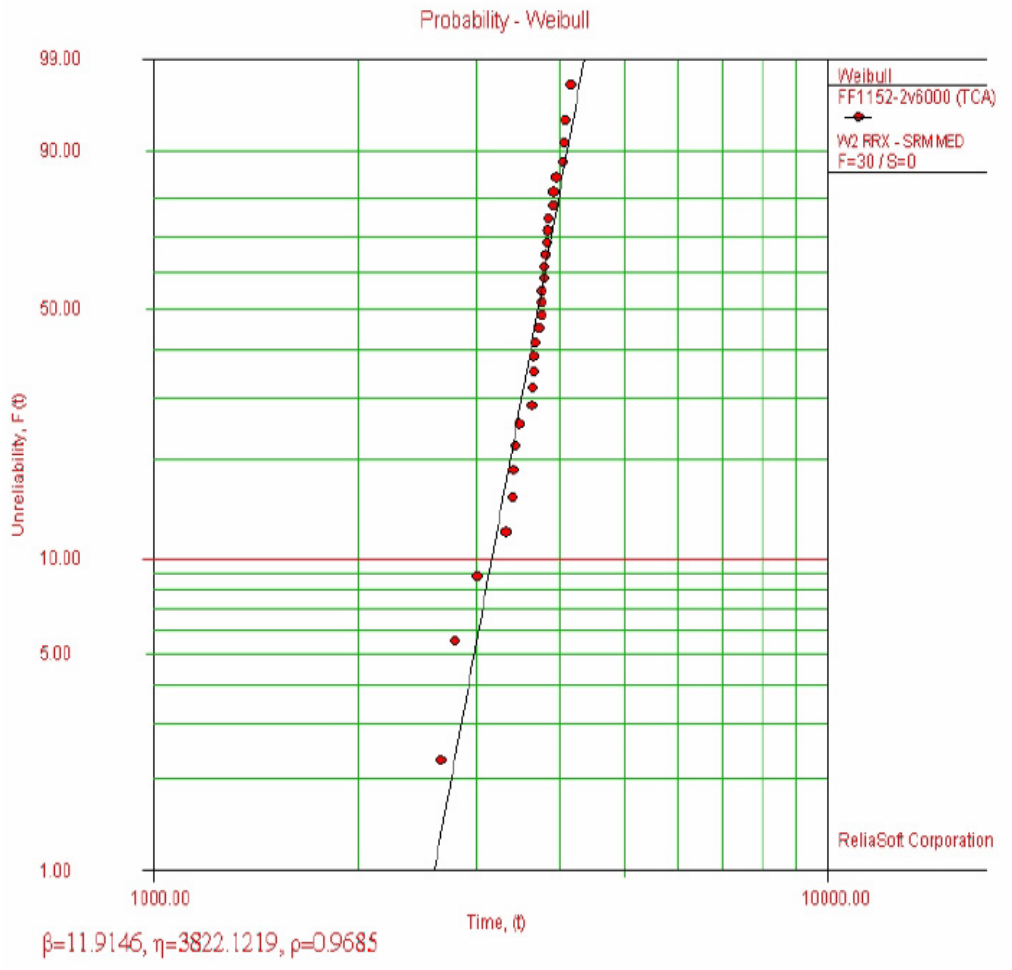

Figure 3-7: **Cycles to Failure in the Second-Level Reliability Tests for FF1152**

FF1704

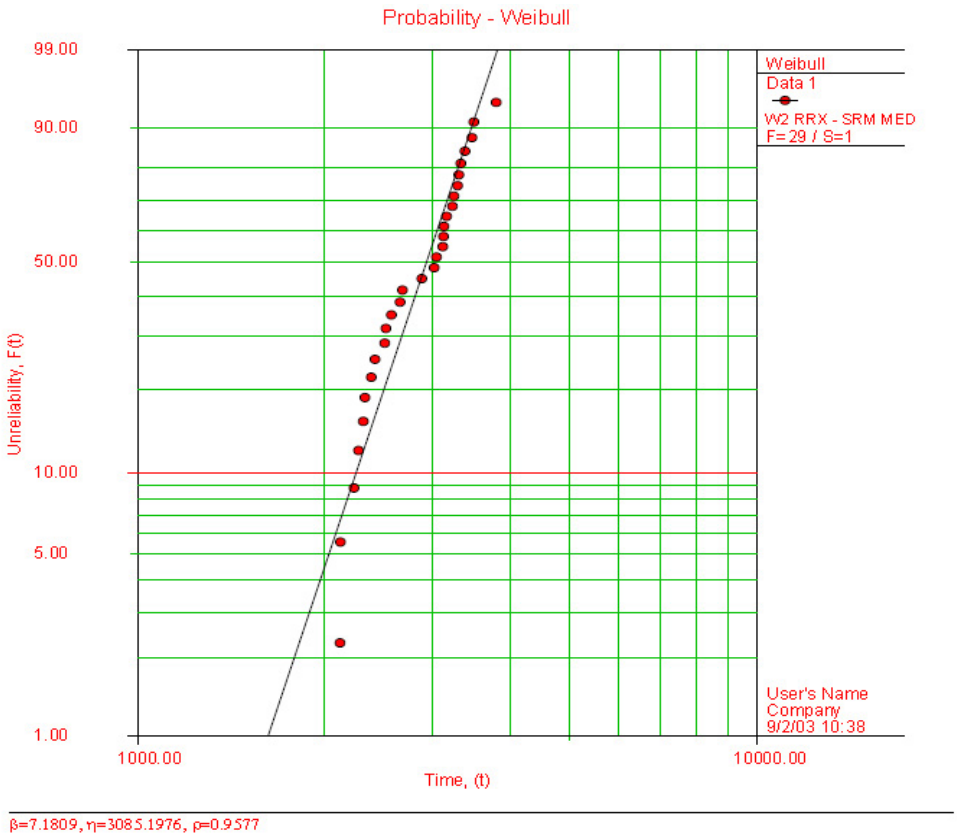

Figure 3-8: **Cycles to Failure in the Second-Level Reliability Tests for FF1704**

Board-Level Reliability Tests, Pb-Free

Xilinx FGG676, FFG1152

Table 3-65: **Package Details (all dimensions in mm)**

Package	Size	I/O	Pitch	Ball/Column Size	Pad Opening	Pad Type	Die Size	Substrate
FGG676	27 x 27	676	1.00	0.60	0.46	SMD	17.8x17.8x0.3	0.56 Thk, 4-layer
FFG1152	35 x 35	1152	1.00	0.60	0.53	SMD	22x20x0.7	1.152 Thk, 6- layer

Mother Board Design and Assembly Details

- 8-Layer, FR-4, 220x140x2.3622 mm Size, OSP Finish
- 0.5mm Pad Diameter/0.65 mm Solder Mask Opening (NSMD Pads)
- Board Layer Structure: Signal/GND/Signal/Power/Signal/GND/Signal/Power
- Power, GND Layer has 70% Metal. Internal Signal Layer has 40% metal.
- 0.1524 mm Laser Cut Stencil, 0.50 mm Aperture, Alpha Metals WS609 Paste

Test Condition

- FGG676: 0 < >100ºC, 40-minute thermal cycle, 10 minutes dwells, 10ºC/minute ramp rate
- FFG1152: 0 < >100ºC, 10 minutes dwells, 5 minutes ramps, 2 cycles/hour

Failure Criteria

- Continuous Scanning of Daisy Chain Nets (Every 2 minutes)
- **OPEN**: Resistance of Net > Threshold Resistance (300 ohms)
- **FAIL**: At Least 2 OPENs Within One Cycle, Log 15 FAILURES for Each Net

Table 3-66: **Summary of Test Results**

Package	Cycles Completed	# Tested	# Failed	First Failure (Cycles)	Characteristic Life (Cycles)
FGG676	7027	35	27	4390	5974
FFG1152	4640	28	26	3186	4121

Weibull Plots

FGG676

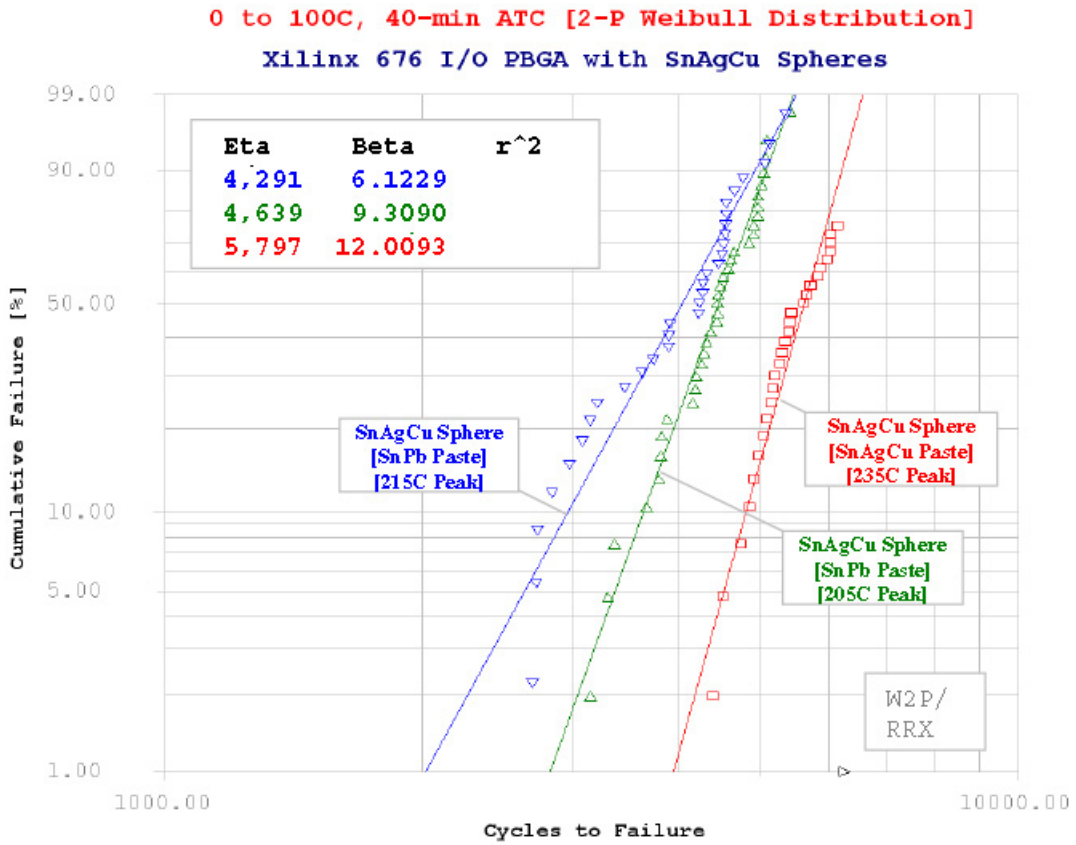

Figure 3-9: **Cycles to Failure in the Second-Level Reliability Tests for FGG676**

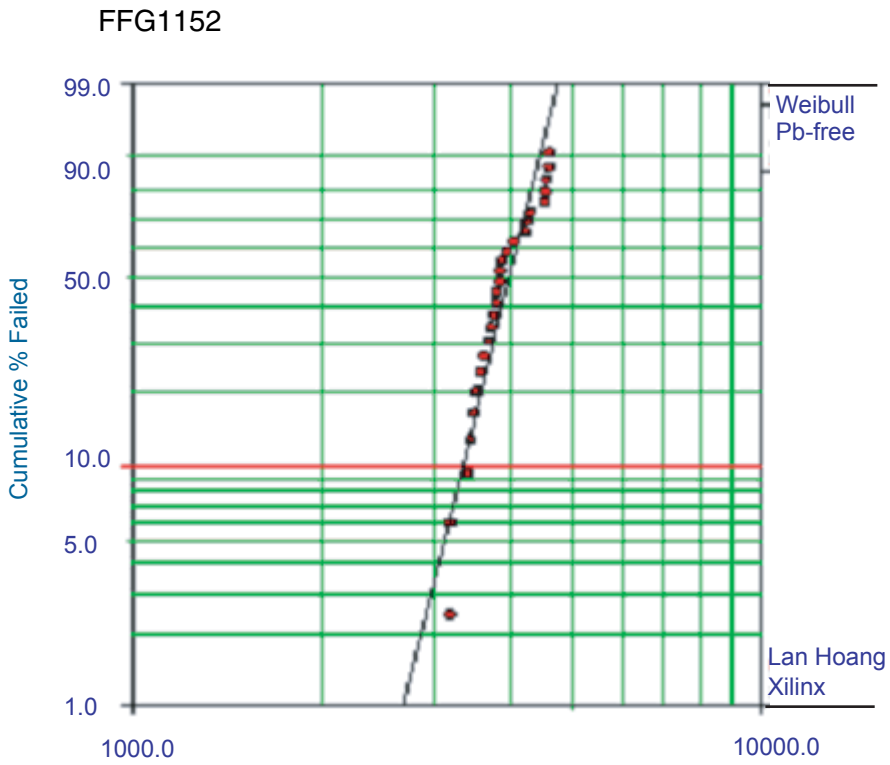

Figure 3-10: **Cycles to Failure in the Second-Level Reliability Tests for FFG1152**