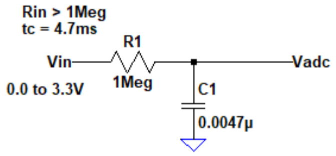
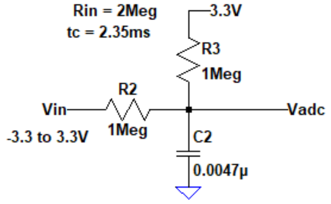
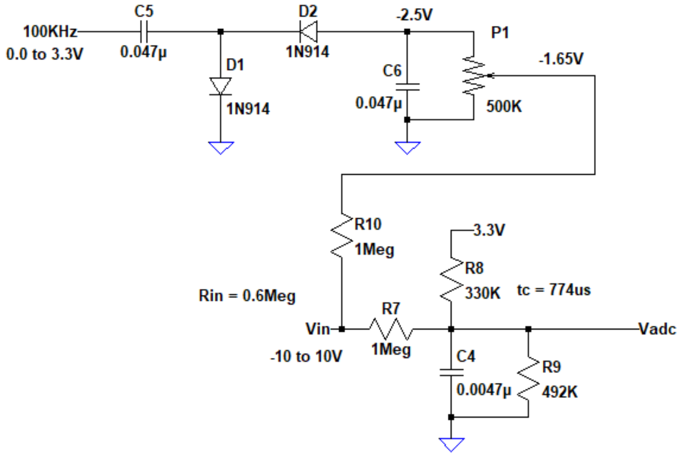
ADC Input Scaling

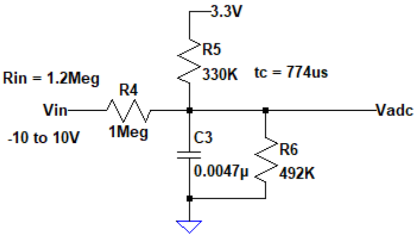
Our first goal is to scale the input for voltages greater than 3.3V and less than zero volts using only resistors and capacitors. A high resistance input network is desired as not to load circuits during measurement. The second goal is to characterize the input of the ADC and observe how it affects the input network. Finally, we will add a single supply op amp to buffer the network for better performance.

The ADC input sample and hold capacitance is specified at 1pF. Let's try to retain the input voltage within one bit for a 12-bit conversion. Adding an input capacitance 4096 times as large should work and 4.7nF is approximately this value.









The first example is for the standard 0 to 3.3V input range. Adding a series 1Meg resistor R1 to the capacitor bounds the minimum input resistance to 1Megohm. Currently, we haven't covered the ADC input impedance. Let's guess that it is much higher than 1Megohm. The time constant will be 4.7ms and the low pass cutoff frequency 33.9Hz. This is obviously a low bandwidth solution.

A voltage divider, R2 and R3, connected to the plus 3.3V reference is a simple way to extend the range from -3.3V to +3.3V. To obtain good performance without an input capacitor, low value resistances around 10K ohms are required. Adding a charge holding capacitor allows for higher value resistors. With 1Meg resistor values, the time constant is half at 2.35ms.

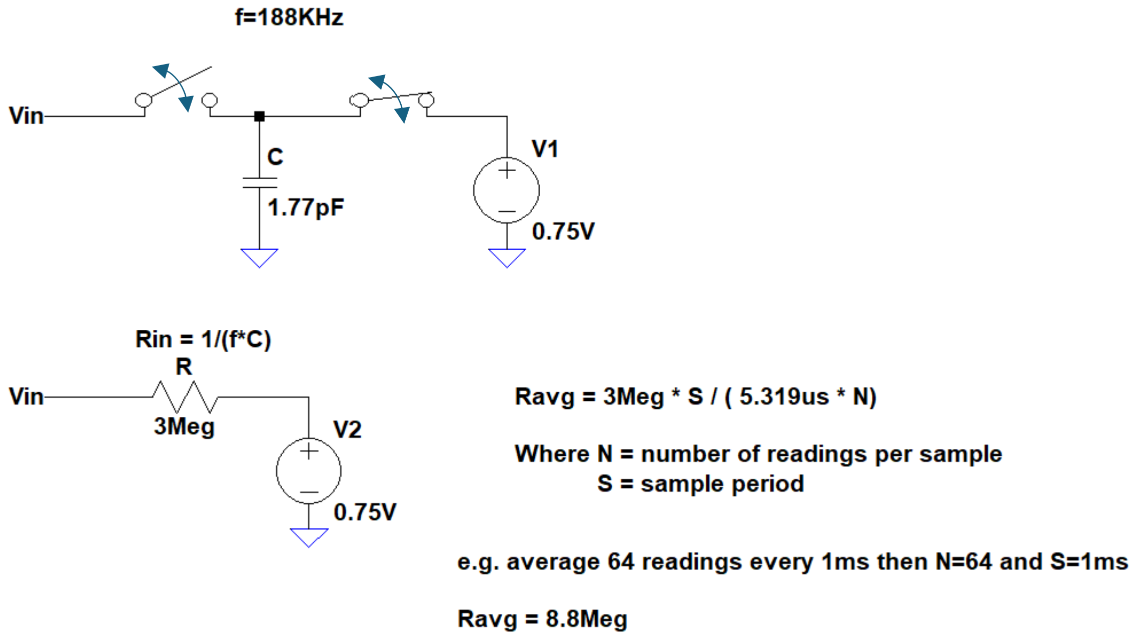
Simply adding a grounding resistor R6 increases the voltage input range.

Here is how to find the resistor values:

- For the maximum negative input value, we let the Vadc input be zero volts.
- With a 1Meg resistor R4 and -10V input, the current is 10uA.
    - The same current flows through the 3.3V pull up resistor R5 and no current flows in the ground resistor R6.
    - So, R5's value is 3.3V/10uA or 330K ohms.
- For the maximum positive input value of 10V, we let the Vadc input be 3.3V.
    - No current flows in the pull up resistor R5.
    - The current in the 1Meg resistor is (10V-3.3V)/1Meg or 6.7ua.
    - Resistor R6 is then 3.3V/6.7ua or 492.5K (470K+22K is close enough)

Looking into the ±10V R4 input we see a 1.2Meg resistance connected to a Thevenin voltage of 3.3V*492/(492+330)=1.975V. It takes -1.65uA to pull the input to zero. A simple charge pump circuit can use a square wave tone to make the needed negative voltage. C5 passes the AC signal where D1 clamps the positive level just above ground. The negative portion is passed by D2 where C6 filters it to DC.

A new resistor R10 is added to generate the needed current from the -1.65V set by potentiometer P1. The circuit is now balanced and the input floats at zero volts. The input resistance is lower at about 600K ohms.



Ravg = 3Meg * S / (5.319us * N)

Where N = number of readings per sample
S = sample period

e.g. average 64 readings every 1ms then N=64 and S=1ms

Ravg = 8.8Meg

Looking into the ADC input pin, we encounter a switched capacitor. There are obviously other internal circuit connections, but we will keep our model simple. The switched capacitor input will appear as a resistor connected to a voltage reference. Resistance is dependent on the switching frequency and the sampling capacitor value.

For this discussion, 10-bit ADC sampling was performed in an averaging loop with values of 8 and 64. The loop frequency measured was 188KHz. The averaging bursts were timed in a second loop set to 1ms or 8ms. No faster than 1ms was used to allow USB serial printing of the averaged value.

The input resistance of 3Megohms was measured and the sampling capacitor value calculated to be 1.77pF based on the 188KHz loop frequency. The ADC is only active over a portion of the outer timing loop. This has the effect of multiplying the resistance by the inverse ratio of the period to the averaging interval. Eight ADC samples take 8/188KHz or 42.55us. With an interval of 1ms, the average resistance increases to 3Meg times 1/0.04255 or 70.5Meg.

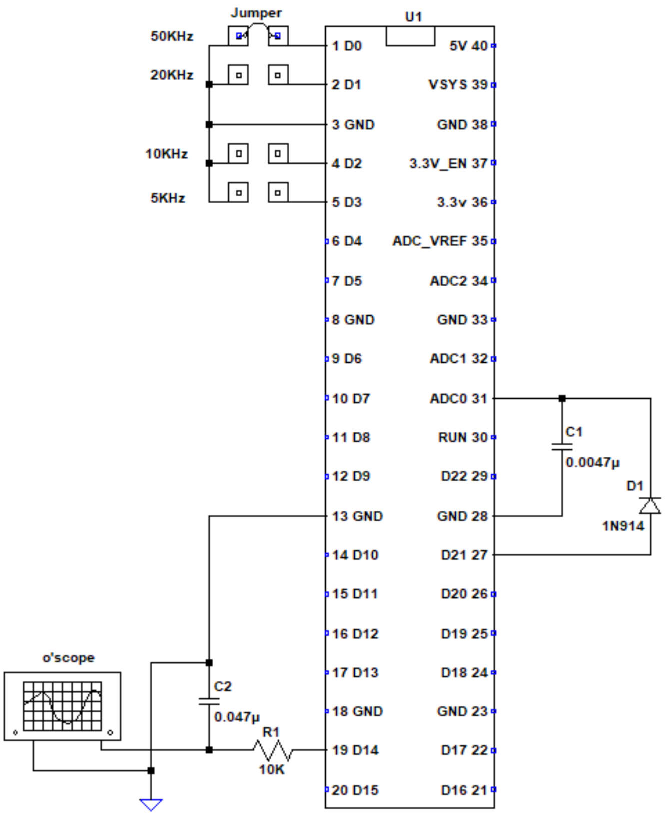
Let’s see what happens if we have a continuous ADC sampling period. Sixty-four samples over 1ms gives us a frequency of 64KHz. The input resistance is 1/(64KHz*1.77pF) = 8.8Megohms. The same result as the burst averaging.

The ADC input when attached to our scaling networks will increase the range and shift the offset. To minimize loading, we need to keep the sampling rate low. Also, the sampling rate and method need to be consistent as the load changes with frequency.

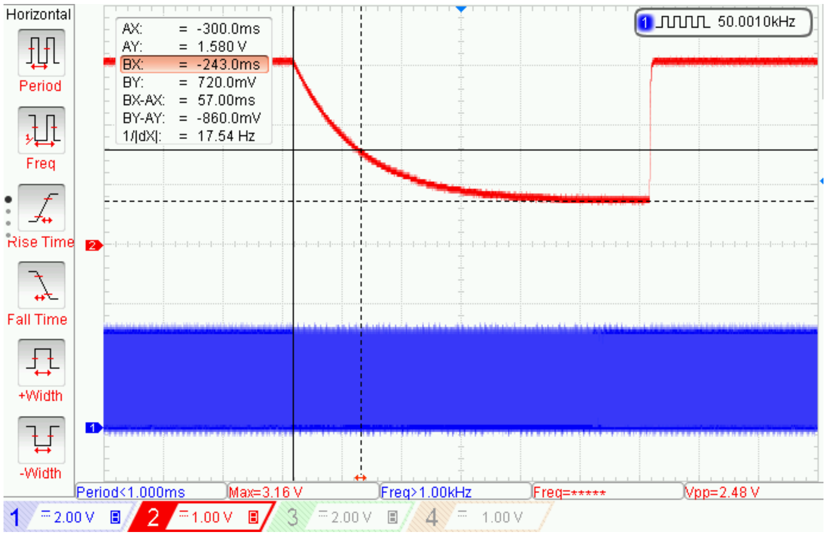
Our ±10V network has a Thevenin resistance of about 165K. As an example, we want to keep ADC input loading to less than 0.1% or 165Megohms. Single samples at a 3.4KHz rate keep us in this range.

Two methods were used to measure equivalent input resistance. The first, is an RC time constant method. A PWM output is used to create a DAC. The response of the ADC input can then be observed on an o'scope. A switched GP output is used to charge the input capacitor to around 3V then switch to a high impedance input state. A blocking diode was added for better isolation.

When the ADC is sampled at a continuous rate, the capacitor discharge to 0.75V can be observed. The time required, to change to 36.8% of the difference initial to final values, is measured. Dividing the time by the input capacitor yields the input resistance.


Ground One Pin to select sample frequency

Constant sample frequency setup. C1 used for this test measured 4.9nF.



```
AX:      =  -300.0ms
AY:      =  1.580 V
BX:      =  -243.0ms
BY:      =  720.0mV
BX-AX:   =  57.00ms
BY-AY:   =  -860.0mV
1/|dX|:  =  17.54 Hz
```

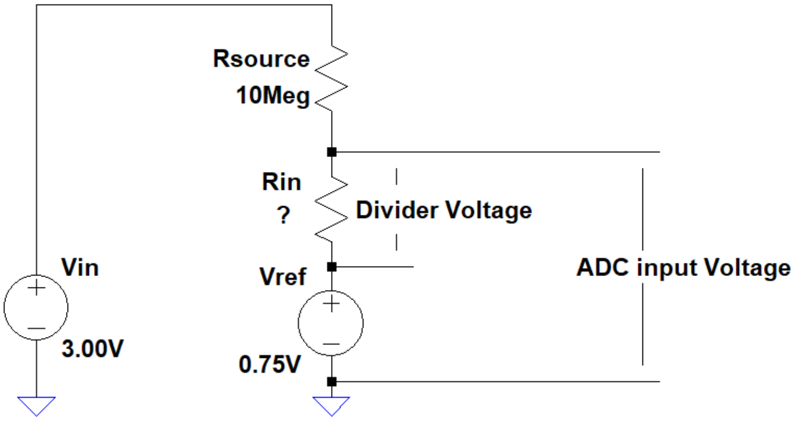
```
1 50.0010kHz
Period<1.000ms   Max=3.16 V   Freq>1.00kHz   Freq=*****   Vpp=2.48 V
1  2.00 V   2  1.00 V   3  2.00 V   4  1.00 V
```

Tc=57ms at fsampling = 50KHz
Rin = Tc/C1 = 0.057/4.9e-9 =11.6Megohms

Compared to the sampling method calculation, the value is as expected.

Rin = 1/(f*Cin) = (1/(50KHz*1.77e-12) = 11.3Megohms

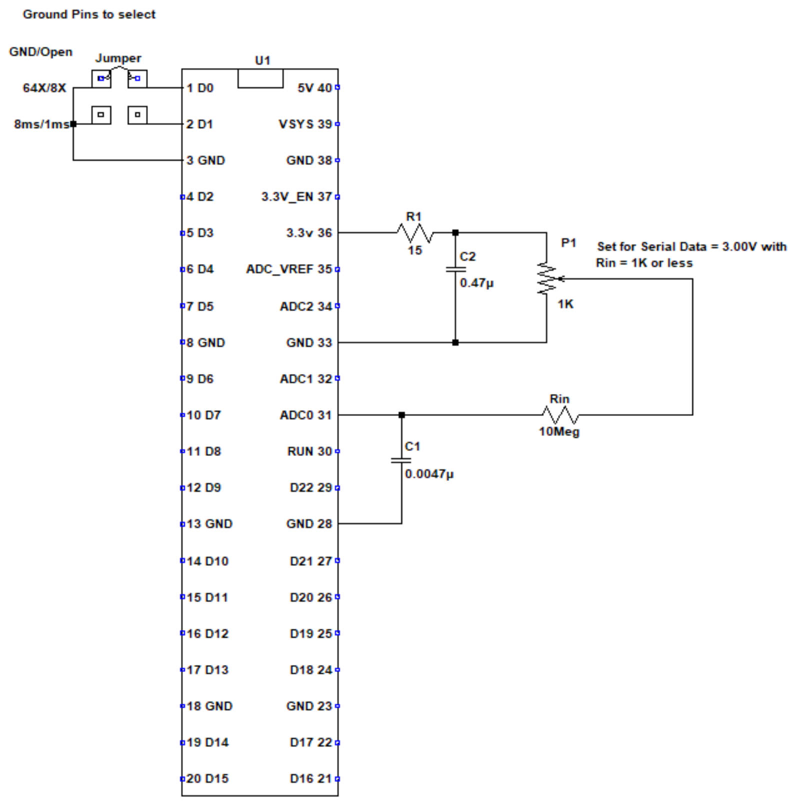
A second method of measuring ADC input resistance is to use a voltage divider. During calculations, the internal 0.75V reference needs to be subtracted from the input voltage. A high source resistance is best for testing as it gives the highest voltage drop.



When the ADC data is printed, we measure the voltage the ADC sees and not the divider formed between the internal reference and the external voltage. With a simple subtraction from the measured value, we can back calculate the input resistor Rin. Our 10Meg resistor was 10.12Megohms.

Vdivider_Ratio = (Vadc-0.75) / (Vin-0.75)

Rin = Rsource * Vdivider_Ratio / (1-Vdivider_Ratio)


Ground Pins to select

Set for Serial Data = 3.00V with Rin = 1K or less

ADC voltage is printed through the USB serial interface. Change Rin to less than 1K to adjust the input voltage to read 3.000V. Change Rin to 10Megohms to measure the voltage drop.

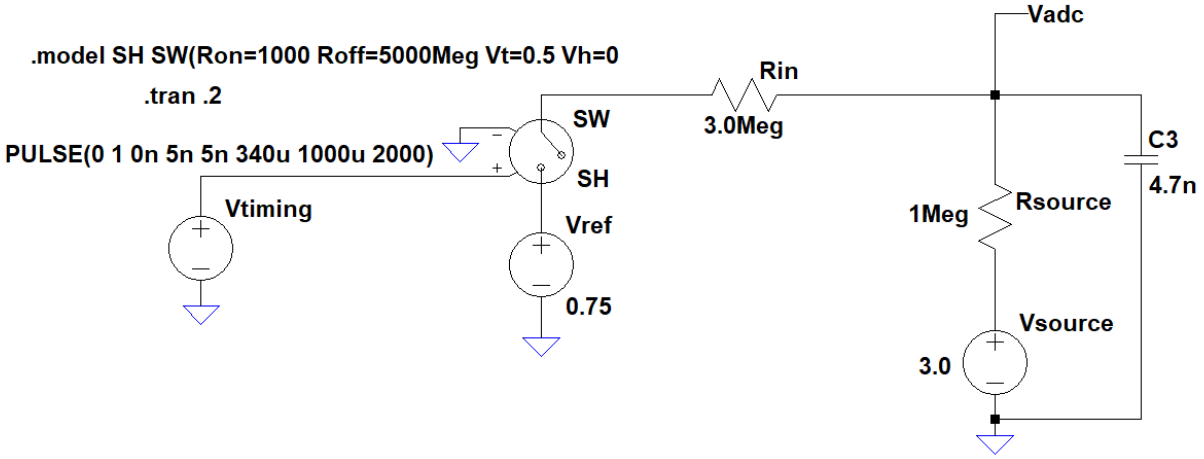
For 1ms and 64X averaging, we measured 1.793V. Rin calculated to 8.76Megohms
For 1ms and 8X averaging, we measured 2.717V. Rin calculated to 70.5Megohms
For 8ms and 64X averaging, we measured 2.717V. Rin calculated to 70.5Megohms
For 8ms and 8X averaging, we measured 2.958V. Rin calculated to 534Megohms

Using the base Rin value for the averaging clock of 1 / (188KHz * 1.77pF) = 3Megohms, the Rin values were calculated using the duty cycles.

3Meg*1ms/340us = 8.82Megohms
3Meg*1ms/42.5us = 70.6Megohms
3Meg*8ms/340us = 70.6Megohms
3Meg*8ms/42.5us = 565Megohms

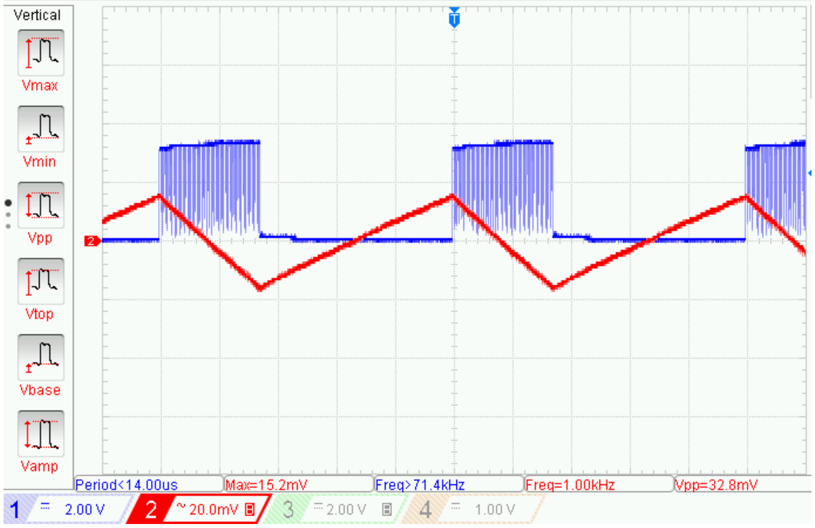
The voltage divider method is consistent with expected values.

So far, we have looked at the average signal. In the short term, the 3Megohm resistance for 188KHz sampling dominates. We can get fair estimates of the sampling signal induced ripple using simplified RC models. However, simulation of the switched system provides very good estimates. Below is the LTspice model for the 1Megohm input and a 4.7nF filter capacitor.


.model SH SW(Ron=1000 Roff=5000Meg Vt=0.5 Vh=0
.tran .2
PULSE(0 1 0n 5n 5n 340u 1000u 2000)
Vtiming
SW
SH
Vref
0.75
Rin
3.0Meg
Vadc
C3
4.7n
1Meg
Rsource
Vsource
3.0

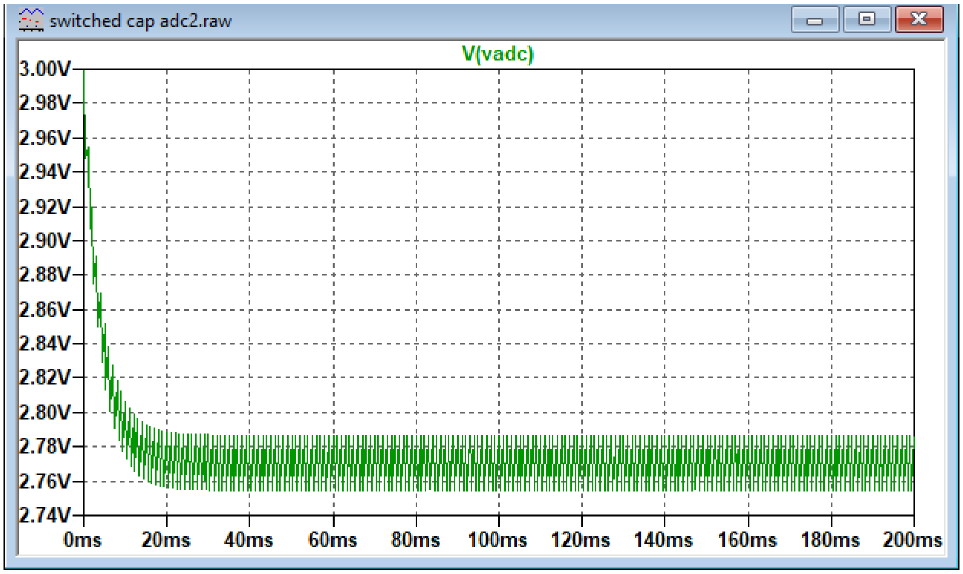
An op amp voltage follower buffer was added to measure the input at the ADC input pin. The following results were recorded:

3.000V in	32.8mVpp	Vavg 2.766V
1.875V in	15.6mVpp	Vavg 1.756V
1.325 in	7.96mVpp	Vavg 1.263V
0.75V in	0.25mVpp	Vavg 0.75V

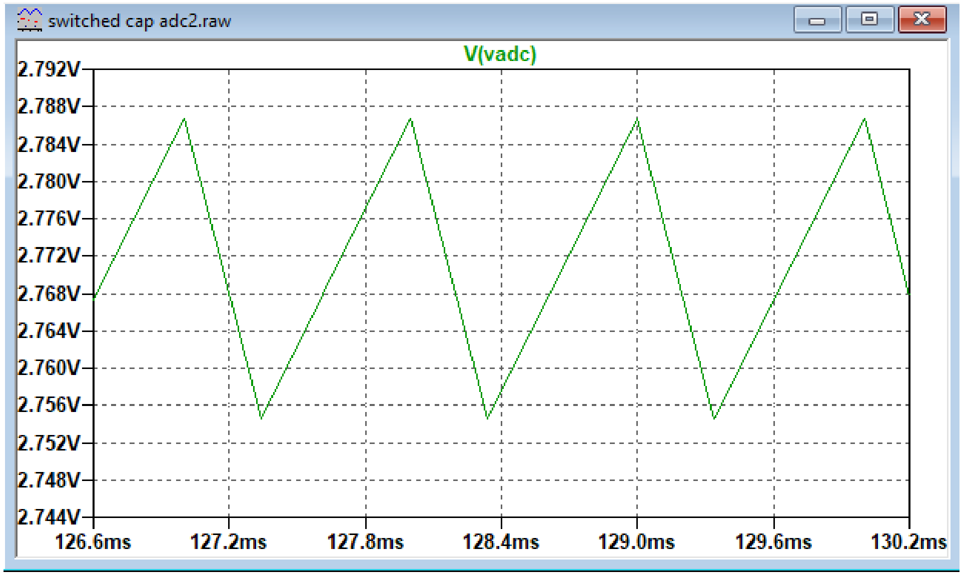


Period<14.00us Max=15.2mV Freq>71.4kHz Freq=1.00kHz Vpp=32.8mV

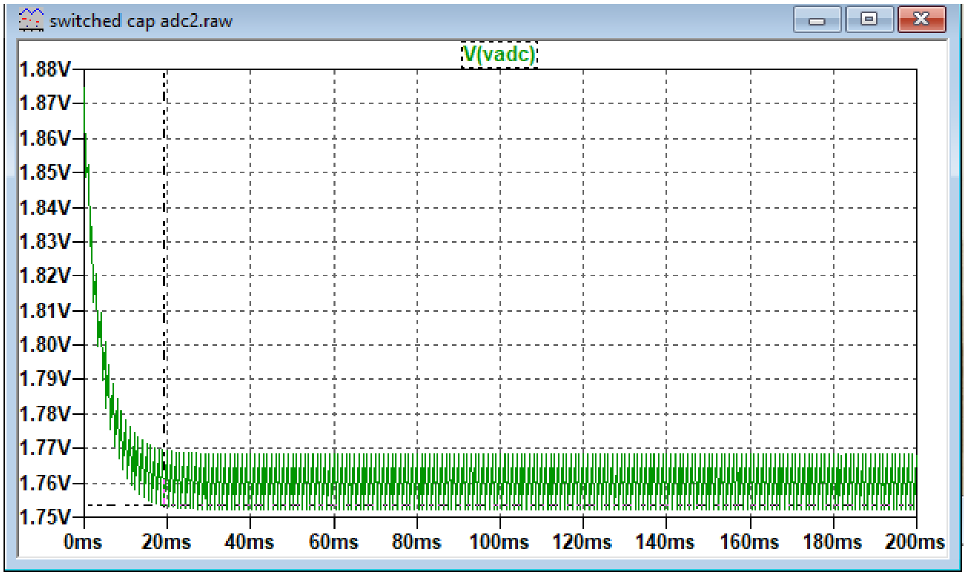
An oscilloscope trace of the sampling pulses in blue and the ADC input ripple in red.



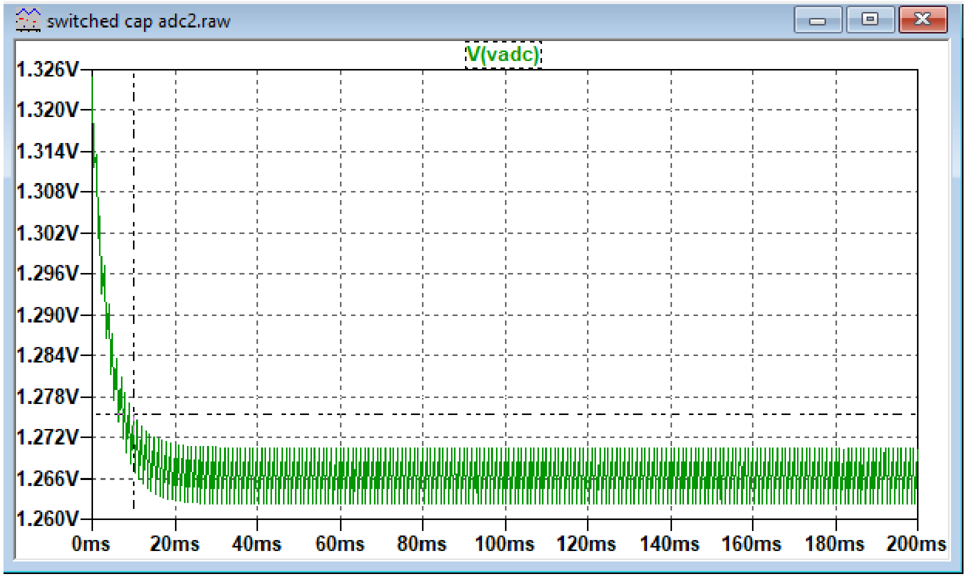
Simulation with 3V in. Vpp = 31.4mV and Vaverage = 2.770V



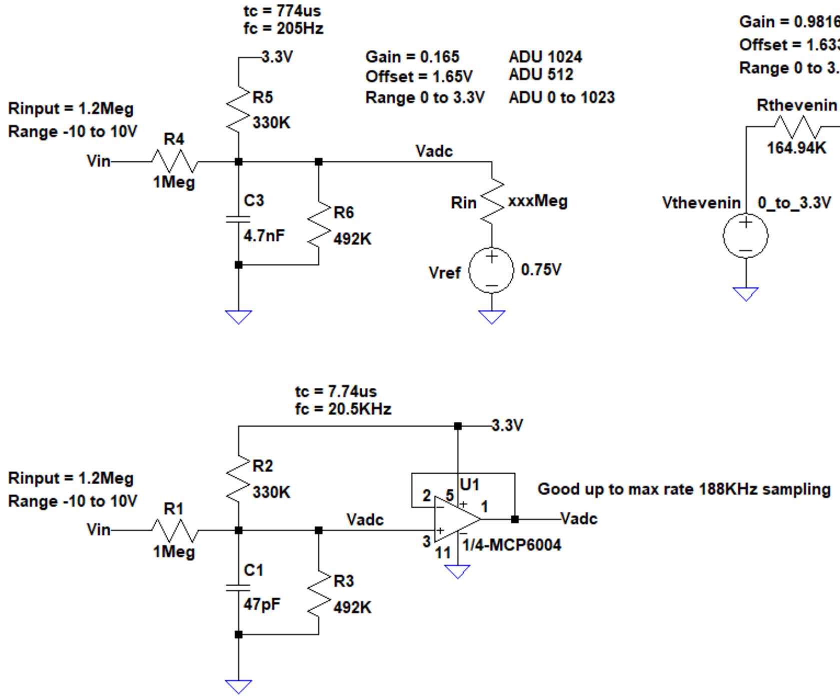
A magnified view of the simulated input ripple. The ripple in this case is linear and the 64 ADC readings will average the voltage to 2.77V. The ripple voltage is more dependent on the 0.0047uF filter capacitor. Lowering the input resistor reduces the average voltage drop. Increasing capacitance decreases the ripple voltage.



Simulation with 1.875V in. Vpp = 15.9mVpp, Vaverage = 1.760V



Simulation with 1.325V in. Vpp = 8.1mVpp and Vaverage = 1.264V



We can see that it is possible to make accurate measurements with high impedance networks. The example above shows an RC only network will have a slight change in gain and offset. Both changes can be corrected in scaling software.

One limitation is the requirement for consistent sampling methods. However, gain and offset tables can be created for different scenarios.

The major limitation of high impedance networks is bandwidth. The only way to improve this is to add a buffer amplifier. The same input network can be used. The filter capacitor can be significantly reduced or removed. Good bandwidth at maximum sampling can be achieved.

The test programs along with the UF2 compiled files can be found in the following folders. As with most projects on this site, the program is compiled using the Arduino IDE and Earle Philhower's arduino-pico core.

adc_rdiv_measure

adc_rc_measure