

Configuring the DMA Peripheral

Introduction

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The Direct Memory Access (DMA) peripheral is a byte-wide transfer system that can copy data from Program Flash Memory, Data EEPROM, General Purpose Registers (GPR) and Special Function Registers (SFR) to General Purpose or Special Function Registers. The transfer is transparent to the CPU and can be configured to interleave its transfers with the processor's operations or suspend processor operations until the DMA transfer is complete.

DMA transfers can be triggered by software and a variety of CIP trigger signals including clocks, timers outputs, comparators, communication peripherals, as well as CLCs. DMA transfers can operate as one-shot transfers or be configured to run continuously until stopped by either software intervention or a hardware CIP-based abort trigger.

Configuring the DMA peripheral involves several steps that can be a little confusing for someone who is new to the peripheral. This technical brief will cover the general configuration process and will highlight many of the available options.



Important: Several device families have multiple DMA peripherals. To access the registers associated with a specific DMA peripheral will require setting the DMASELECT register with the appropriate values. The DMA registers will then be available in the common memory address block.

To configure a DMA peripheral, the following sections need to be configured:

- · Source and destination memory address
- · Source and destination message sizes
- DMA trigger events
- DMA abort events (optional)
- DMA automation
- · DMA interrupts (optional)
- DMA priority and enabling of the overall DMA peripheral

There will also be a *closing section* that covers the variety of Status bits and registers available for monitoring the DMA progress.

The source and destination memory addresses include both the address and the type of memory; EEPROM, Flash Program Memory or SFR/GPR data memory.



Important: DMA can source data from EEPROM, Flash Program Memory and SFR/GPR data memory, but can only use GPR/SFR memory as a destination.

The source and destination sizes are the number of bytes in a message. Each byte is considered a transaction, a group of transactions that occur in response to a trigger are considered a message, and a group of messages are

considered a DMA operation. The size variables refer to the number of transactions that constitute a message. For example;

- Transferring data from a serial port Rx register to a data buffer would have a source size of one and a
 destination size equal to the buffer size.
- Transferring data from a data buffer to a serial Tx register would have a source size equal to the buffer size and a destination size of one.
- Transferring data from a data buffer to a 16-bit PWM duty cycle register would have a source size equal to the buffer size and a destination size of two.

The DMA trigger event can either be software or a CIP-based hardware trigger, such as timer roll over, comparator output or a group of signals combined in a CLC combinational logic function. The DMA abort is a similar function with both software and CIP-based hardware options.

Note: This is optional in that DMA can also be configured to operate continuously once enabled or shut down at the end of the DMA operation.

The DMA automation is what happens after the transfer; the source/destination addresses can be post incremented, post decremented or fixed. The automation also refers to which counter rollover, if any, will terminate the DMA operation.

The DMA peripheral is also capable of generating up to four specialized interrupts; one at the rollover of the source counter, one at the rollover of the destination counter, one in the event of an abort and one for an overrun error event.

Note: Individual devices may have options specific to that device. This document can be used as a general guide, but for specific settings and options, refer to the device data sheet.

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1. Setting the Source

The DMA peripheral can source data from three different memory systems in the microcontroller; Data EEPROM, Program Flash Memory and SFR/GPR memory.

1.1 Configuring the DMA Source

To configure the DMA source, the first step is to select the type of source memory. This is accomplished by setting the SMR bits in the DMAnCON1 register. Table 1-1 lists the possible options and the associated bit combination.

Table 1-1. Source Memory Selection

SMR[1:0]	Source Memory Region
11	Data EEPROM
10	Data EEPROM
01	Program Flash Memory
00	SFR/GPR data space

Once the type of source memory is selected, the next step is to load the DMAnSSAL, DMAnSSAH and DMAnSSAU registers. These registers specify the address of the source data. Together, the three registers can hold up to a 22-bit address.

Note: For Data EEPROM and SFR/GPR memory, only the DMAnSSAL and DMAnSSAH registers are used and the contents of the DMAnSSAU register is ignored. However, it is considered good programming practice to program DMAnSSAU with the value 0x38 for Data EEPROM access (program memory prefix address for the EEPROM area in Program Flash Memory address space).

1.2 Loading the Source Registers

Loading the source registers can be accomplished by using the set address routines supplied by MCC. They can be loaded individually by the system software, or all three registers can be loaded together by equating the DMAxSSA register with a 16- or 24-bit constant or variable containing the desired address.

```
DMAnSSa = 0x2C0070; // Access Device Information Area
```

Note: If the SMR bits are set for access to PFM, data EEPROM addresses can be accessed by loading the DMAnSSAU register with the value 0x38. In fact, loading the DMAnSSAU with other 8-bit MSb values will allow access to other upper flash memory areas including the Device Information Area (DIA) and User ID words. See Figure 1-1.

Figure 1-1. Program and Data Memory Map

	Device							
Address	PIC18Fx5Q43	PIC18Fx6Q43	PIC18Fx7Q43					
00 0000h								
to	D 51 1							
00 3FFFh	Program Flash							
00 4000h	Memory (16 KW) ⁽¹⁾	Program Flash						
to	(10 KVV).	Memory	Program Flash					
00 7FFFh		(32 KW) ⁽¹⁾						
00 8000h			Memory					
to			(64 KW) ⁽¹⁾					
00 FFFFh								
01 0000h								
to	Not							
01 FFFFh	Present ⁽²⁾	Not						
02 0000h		Present ⁽²⁾						
to			Not					
1F FFFFh			Present ⁽²⁾					
20 0000h								
to		User IDs (32 Words)(3)						
20 003Fh								
20 0040h								
to		Reserved						
2B FFFFh								
2C 0000h								
to								
2C 00FFh								
2C 0100h		Decembed						
to	Reserved							
2F FFFFh 30 0000h								
to		Configuration Bytes (3)						
30 0009h		Configuration Bytes						
30 000Ah								
to		Reserved						
37 FFFFh								
38 0000h								
to		Data EEPROM (1024 Bytes))					
38 03FFh								
38 0400h		D						
to 3B EEEEb		Reserved						
3B FFFFh								
3C 0000h	D-	vice Configuration Information	(3)(4)(5)					
to 3C 0009h	De	vice Configuration Information	•					
3C 000Ah								
to		Reserved						
3F FFFBh								
3F FFFCh								
to		Revision ID (1 Word) ⁽³⁾⁽⁴⁾⁽⁵⁾						
3F FFFDh								
3F FFFEh								
to Device ID (1 Word) ⁽³⁾⁽⁴⁾⁽⁵⁾								
3F FFFFh		/						

Note 1:

Storage Area Flash is implemented as the last 128 Words of User Flash, if enabled.

- 2: The addresses do not roll over. The region is read as '0'.
- 3: Not code-protected.
- 4: Hard-coded in silicon.
- 5: This region cannot be written by the user and it's not affected by a Bulk Erase.

In addition to the standard set of SFR memory locations, an additional copy of select SFRs is available to the DMA system exclusively. This section of SFR memory contains shadow copies of multiple SFRs. For programmer's convenience, the registers have been placed adjacent to each other to facilitate DMA access. See Figure 1-2.

Figure 1-2. Special Function Register MAP (DMA Access Only)

40FFh		40DFh		40BFh		409Fh		407Fh		405Fh		403Fh		401Fh	
40FFh 40FEh		40DFn 40DEh		40BFh		409Fh		407Fh	•	405Fh		403Fh		401Fh 401Eh	•
40FEN 40FDh		40DEN 40DDh		40BEN 40BDh		409En 409Dh		407En	ADDECH AM	405En		403En 403Dh		401En 401Dh	
	•								ADRESH_M1				-		
40FCh	· ·	40DCh		40BCh		409Ch		407Ch	ADRESL_M1	405Ch		403Ch		401Ch	-
40FBh	•	40DBh		40BBh	-	409Bh		407Bh	ADPCH_M1	405Bh	•	403Bh	•	401Bh	PWM3S1P2H_M1
40FAh		40DAh		40BAh	-	409Ah	•	407Ah	ADCLK_M1	405Ah	•	403Ah	•	401Ah	PWM3S1P2L_M1
40F9h		40D9h		40B9h	•	4099h		4079h	ADACT_M1	4059h		4039h	•	4019h	PWM3S1P1H_M2
40F8h	•	40D8h		40B8h	-	4098h	•	4078h	ADREF_M1	4058h	•	4038h	•	4018h	PWM3S1P1L_M2
40F7h		40D7h		40B7h	-	4097h		4077h	ADCON3_M1	4057h	<u> </u>	4037h	-	4017h	PWM2S1P2H_M1
40F6h	ADRESH_M2	40D6h		40B6h	-	4096h	•	4076h	ADCON2_M1	4056h		4036h	•	4016h	PWM2S1P2L_M1
40F5h	ADRESL_M2	40D5h		40B5h	-	4095h		4075h	ADCON1_M1	4055h	•	4035h	•	4015h	PWM2S1P1H_M2
40F4h	ADPCH_M2	40D4h		40B4h	-	4094h	•	4074h	ADCON0_M1	4054h	•	4034h	•	4014h	PWM2S1P1L_M2
40F3h	ADCAP_M2	40D3h		40B3h	-	4093h	•	4073h	ADCAP_M1	4053h	•	4033h	•	4013h	PWM1S1P2H_M1
40F2h	ADACQH_M2	40D2h		40B2h	•	4092h	•	4072h	ADACQH_M1	4052h		4032h	•	4012h	PWM1S1P2L_M1
40F1h	ADACQL_M2	40D1h		40B1h		4091h		4071h	ADACQL_M1	4051h		4031h	PWM3PRH_M1	4011h	PWM1S1P1H_M2
40F0h	ADPREVH_M2	40D0h		40B0h	•	4090h	•	4070h	ADPREVH_M1	4050h	•	4030h	PWM3PRL_M1	4010h	PWM1S1P1L_M2
40EFh	ADPREVL_M2	40CFh		40AFh		408Fh		406Fh	ADPREVL_M1	404Fh		402Fh	PWM3S1P2H_M2	400Fh	
40EEh	ADRPT_M2	40CEh		40AEh		408Eh		406Eh	ADRPT_M1	404Eh		402Eh	PWM3S1P2L_M2	400Eh	
40EDh	ADCNT_M2	40CDh		40ADh		408Dh		406Dh	ADCNT_M1	404Dh		402Dh	PWM3S1P1H_M3	400Dh	
40ECh	ADACCU_M2	40CCh		40ACh		408Ch		406Ch	ADACCU_M1	404Ch		402Ch	PWM3S1P1L_M3	400Ch	
40CBh	ADACCH_M2	40CBh		40ABh		408Bh		406Bh	ADACCH_M1	404Bh		402Bh	PWM2PRH_M1	400Bh	PWM3S1P1H_M1
40EAh	ADACCL_M2	40CAh		40AAh	-	408Ah		406Ah	ADACCL_M1	404Ah		402Ah	PWM2PRL_M1	400Ah	PWM3S1P1L_M1
40E9h	ADFLTRH_M2	40C9h		40A9h	-	4089h		4069h	ADFLTRH_M1	4049h		4029h	PWM2S1P2H_M2	4009h	PWM2S1P1H_M1
40E8h	ADFLTRL_M2	40C8h		40A8h	•	4088h		4068h	ADFLTRL_M1	4048h	T6PR_M1	4028h	PWM2S1P2L_M2	4008h	PWM2S1P1L_M1
40E7h	ADSTPTH_M2	40C7h		40A7h		4087h		4067h	ADSTPTH_M1	4047h	CCPR3H_M2	4027h	PWM2S1P1H_M3	4007h	PWM1S1P1H_M1
40E6h 40E5h	ADSTPTL_M2	40C6h 40C5h		40A6h		4086h		4066h	ADSTPTL_M1 ADERRH_M1	4046h 4045h	CCPR3L_M2	4026h 4025h	PWM2S1P1L_M3	4006h	PWM1S1P1L_M1
40E5h	ADERRH_M2 ADERRL M2	40C4h		40A5h 40A4h	•	4085h 4084h		4065h 4064h	ADERRI M1	4045h	T4PR_M1 CCPR2H M2	4025h 4024h	PWM1PRH_M1 PWM1PRL M1	4005h 4004h	CCPR3H_M1 CCPR3L M1
40E4II	ADUTHH M2	40C411		40A411		4083h		4064H	ADUTHH M1	4044II	CCPR2L M2	4024II	PWM1S1P2H M2	400411 4003h	CCPR2H M1
40E3H	ADUTHL M2	40C3h		40A311		4082h		406311 4062h	ADUTHL M1	404311 4042h	T2PR M1	402311 4022h	PWM1S1P2L M2	400311 4002h	CCPR2H_M1
40E2H	ADLTHH M2	40C2H		40A2II	- :	4082II	- :	406211 4061h	ADUTHL_M1 ADLTHH M1	4042II	CCPR1H M2	4022II	PWM1S1P1L_M2 PWM1S1P1H M3	4002h	CCPR2L_M1
40E0h	ADLTHL M2	40C0h		40A0h	-	4080h		4060h	ADLTHL M1	4040h	CCPR1L M2	4020h	PWM1S1P1L M3	4000h	CCPR1L M1
40LUII	ADEITIC_WZ	400011		HUMUII	-	400011	-	400011	ADLIIIL_WII	404011	CCFRIL_WIZ	402011	r www.ijjirit_iwij	400011	CCFRIL_WII
41FFh															
		41DEh		41DEh		410Eh		417Eh	DAMA COTOU DAMAG	4155h	DMANDETEL DMAS	412Eh	DMAnggau DMA2	111Eh	DMAnDSAH DMA2
		41DFh		41BFh	-	419Fh		417Fh	DMAnSPTRH_DMA6	415Fh	DMAnDPTRL_DMAS	413Fh	DMAnSSAH_DMA3	411Fh	DMAnDSAH_DMA2
41FEh	•	41DEh	-	41BEh		419Eh		417Eh	DMAnSPTRL_DMA6	415Eh	DMAnDCNTH_DMA5	413Eh	DMAnSSAL_DMA3	411Eh	DMAnDSAL_DMA2
41FEh 41FDh		41DEh 41DDh	-	41BEh 41BDh	-	419Eh 419Dh	-	417Eh 417Dh	DMAnSPTRL_DMA6 DMAnSCNTH_DMA6	415Eh 415Dh	DMAnDCNTH_DMA5 DMAnDCNTL_DMA5	413Eh 413Dh	DMAnSSAL_DMA3 DMAnSSZH_DMA3	411Eh 411Dh	DMAnDSAL_DMA2 DMAnDSZH_DMA2
41FEh 41FDh 41FCh		41DEh 41DDh 41DCh	-	41BEh 41BDh 41BCh		419Eh 419Dh 419Ch		417Eh 417Dh 417Ch	DMAnSPTRL_DMA6 DMAnSCNTH_DMA6 DMAnSCNTL_DMA6	415Eh 415Dh 415Ch	DMAnDCNTH_DMAS DMAnDCNTL_DMAS DMAnBUF_DMAS	413Eh 413Dh 413Ch	DMAnSSAL_DMA3 DMAnSSZH_DMA3 DMAnSSZL_DMA3	411Eh 411Dh 411Ch	DMAnDSAL_DMA2 DMAnDSZH_DMA2 DMAnDSZL_DMA2
41FEh 41FDh 41FCh 41FBh	- TMR5H_M1	41DEh 41DDh 41DCh 41DBh	•	41BEh 41BDh 41BCh 41BBh		419Eh 419Dh 419Ch 419Bh		417Eh 417Dh 417Ch 417Bh	DMAnSPTRL_DMA6 DMAnSCNTH_DMA6 DMAnSCNTL_DMA6 DMAnDSAH_DMA6	415Eh 415Dh 415Ch 415Bh	DMAnDCNTH_DMA5 DMAnDCNTL_DMA5 DMAnBUF_DMA5 DMAnSIRQ_DMA4	413Eh 413Dh 413Ch 413Bh	DMAnSSAL_DMA3 DMAnSSZH_DMA3 DMAnSSZL_DMA3 DMAnSPTRU_DMA3	411Eh 411Dh 411Ch 411Bh	DMAnDSAL_DMA2 DMAnDSZH_DMA2 DMAnDSZL_DMA2 DMAnDPTRH_DMA2
41FEh 41FDh 41FCh	TMR5H_M1 TMR5L_M1	41DEh 41DDh 41DCh 41DBh 41DAh	-	41BEh 41BDh 41BCh 41BBh 41BAh		419Eh 419Dh 419Ch 419Bh 419Ah		417Eh 417Dh 417Ch 417Bh 417Ah	DMAnSPTRL_DMA6 DMAnSCNTH_DMA6 DMAnSCNTL_DMA6 DMAnDSAH_DMA6 DMAnDSAH_DMA6 DMAnDSAL_DMA6	415Eh 415Dh 415Ch 415Bh 415Ah	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANBUF_DMAS DMANSIRQ_DMA4 DMANAIRQ_DMA4	413Eh 413Dh 413Ch 413Bh 413Ah	DMAnSSAL_DMA3 DMAnSSZH_DMA3 DMAnSSZL_DMA3 DMAnSSTRU_DMA3 DMAnSPTRU_DMA3	411Eh 411Dh 411Ch 411Bh 411Ah	DMANDSAL_DMA2 DMANDSZH_DMA2 DMANDSZL_DMA2 DMANDSZL_DMA2 DMANDPTRH_DMA2 DMANDPTRL_DMA2
41FEh 41FDh 41FCh 41FBh 41FAh	TMR5H_M1 TMR5L_M1 TMR3H_M1	41DEh 41DDh 41DCh 41DBh		41BEh 41BDh 41BCh 41BBh	-	419Eh 419Dh 419Ch 419Bh	-	417Eh 417Dh 417Ch 417Bh	DMANSPTRL_DMA6 DMANSCNTH_DMA6 DMANSCNTL_DMA6 DMANDSAH_DMA6 DMANDSAH_DMA6 DMANDSAL_DMA6 DMANDSZH_DMA6	415Eh 415Dh 415Ch 415Bh	DMANDCNTH_DMA5 DMANDCNTL_DMA5 DMANBUF_DMA5 DMANSIRQ_DMA4 DMANAIRQ_DMA4 DMANCON1_DMA4	413Eh 413Dh 413Ch 413Bh	DMANSSAL_DMA3 DMANSSZH_DMA3 DMANSSZL_DMA3 DMANSPTRU_DMA3 DMANSPTRH_DMA3 DMANSPTRL_DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h	DMAnDSAL_DMA2 DMAnDSZH_DMA2 DMAnDSZL_DMA2 DMAnDFTRH_DMA2 DMAnDFTRL_DMA2 DMAnDCNTH_DMA2
41FEh 41FDh 41FCh 41FBh 41FAh 41F9h 41F8h	TMR5H_M1 TMR5L_M1 TMR3H_M1 TMR3L_M1	41DEh 41DDh 41DCh 41DBh 41DAh 41D9h 41D8h		41BEh 41BDh 41BCh 41BBh 41BAh 41B9h 41B8h	•	419Eh 419Dh 419Ch 419Bh 419Ah 4199h 4198h	•	417Eh 417Dh 417Ch 417Bh 417Ah 4179h 4178h	DMANSPTRL_DMA6 DMANSCNTH_DMA6 DMANSCNTL_DMA6 DMANDSAH_DMA6 DMANDSAL_DMA6 DMANDSZH_DMA6 DMANDSZL_DMA6 DMANDSZL_DMA6	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANBUF_DMA5 DMANSIRQ_DMA4 DMANAIRQ_DMA4 DMANCON1_DMA4 DMANCON0_DMA4	413Eh 413Dh 413Ch 413Bh 413Ah 4139h 4138h	DMANSSAL_DMA3 DMANSSZH_DMA3 DMANSSZL_DMA3 DMANSPTRU_DMA3 DMANSPTRH_DMA3 DMANSPTRL_DMA3 DMANSPTRL_DMA3 DMANSCNTH_DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h 4118h	DMAnDSAL_DMA2 DMAnDSZH_DMA2 DMAnDSZL_DMA2 DMAnDPTRH_DMA2 DMAnDPTRL_DMA2 DMAnDCNTH_DMA2 DMAnDCNTH_DMA2
41FEh 41FDh 41FCh 41FBh 41FAh 41F9h 41F8h 41F7h	TMR5H_M1 TMR5L_M1 TMR3H_M1 TMR3L_M1 TMR3L_M1 TMR1H_M1	41DEh 41DCh 41DCh 41DBh 41DAh 41D9h 41D8h 41D8h 41D7h	-	41BEh 41BDh 41BCh 41BBh 41BAh 41B9h 41B8h 41B8h 41B7h	- - - -	419Eh 419Dh 419Ch 419Bh 419Ah 4199h 4198h 4197h	- - - -	417Eh 417Dh 417Ch 417Bh 417Ah 4179h 4178h 4177h	DMAnSPTRL_DMA6 DMAnSCNTH_DMA6 DMAnSCNTL_DMA6 DMAnDSAH_DMA6 DMAnDSAH_DMA6 DMAnDSZH_DMA6 DMANDSZH_DMA6 DMANDSZL_DMA6 DMANDSZL_DMA6 DMANDFRH_DMA6	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h 4157h	DMANDCNTH_DMA5 DMANDCNTL_DMA5 DMANBUF_DMA5 DMANSIRQ_DMA4 DMANAIRQ_DMA4 DMANCON1_DMA4 DMANCON0_DMA4 DMANCSNU_DMA4 DMANCSNU_DMA4	413Eh 413Ch 413Ch 413Bh 413Ah 4139h 4138h 4137h	DMAnSSAL_DMA3 DMAnSSZH_DMA3 DMAnSSZL_DMA3 DMAnSSTRU_DMA3 DMAnSPTRU_DMA3 DMAnSPTRL_DMA3 DMAnSPTRL_DMA3 DMAnSCNTH_DMA3 DMAnSCNTH_DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h 4118h 4117h	DMAnDSAL_DMA2 DMAnDSZH_DMA2 DMAnDSZL_DMA2 DMAnDSZL_DMA2 DMAnDPTRH_DMA2 DMAnDPTRL_DMA2 DMAnDCNTH_DMA2 DMAnDCNTL_DMA2 DMANDCNTL_DMA2 DMANDLT_DMA2
41FEh 41FDh 41FCh 41FBh 41FAh 41F9h 41F8h	TMR5H_M1 TMR5L_M1 TMR3H_M1 TMR3L_M1	41DEh 41DDh 41DCh 41DBh 41DAh 41D9h 41D8h		41BEh 41BDh 41BCh 41BBh 41BAh 41B9h 41B8h	- - - -	419Eh 419Dh 419Ch 419Bh 419Ah 4199h 4198h	- - - -	417Eh 417Dh 417Ch 417Bh 417Ah 4179h 4178h 4177h 4176h	DMANSPTRL_DMA6 DMANSCNTH_DMA6 DMANSCNTL_DMA6 DMANDSAH_DMA6 DMANDSAL_DMA6 DMANDSZH_DMA6 DMANDSZH_DMA6 DMANDSZH_DMA6 DMANDSTRL_DMA6 DMANDPTRH_DMA6 DMANDPTRL_DMA6	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h	DMANDCNTH_DMA5 DMANDCNTL_DMA5 DMANBUF_DMA5 DMANSIRQ_DMA4 DMANAIRQ_DMA4 DMANCON1_DMA4 DMANCON0_DMA4 DMANSSAU_DMA4 DMANSSAU_DMA4	413Eh 413Dh 413Ch 413Bh 413Ah 4139h 4138h	DMAnSSAL_DMA3 DMAnSSZH_DMA3 DMANSSZH_DMA3 DMASPTRU_DMA3 DMANSPTRU_DMA3 DMANSPTRL_DMA3 DMANSPTRL_DMA3 DMANSCNTH_DMA3 DMANSCNTH_DMA3 DMANSCNTL_DMA3 DMANDSAH_DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h 4118h	DMAnDSAL_DMA2 DMAnDSZH_DMA2 DMAnDSZL_DMA2 DMAnDPTRH_DMA2 DMAnDPTRH_DMA2 DMAnDPTRH_DMA2 DMANDCNTL_DMA2 DMANDCNTL_DMA2 DMANDCNTL_DMA2 DMANDLYDMA2 DMANDLYDMA2 DMANDLYDMA2
41FEh 41FDh 41FCh 41FBh 41FAh 41F9h 41F8h 41F7h 41F6h	TMRSH_M1 TMRSL_M1 TMR3H_M1 TMR3L_M1 TMR1L_M1 TMR1H_M1	41DEh 41DCh 41DCh 41DBh 41DAh 41D9h 41D8h 41D7h 41D6h		41BEh 41BDh 41BCh 41BBh 41BAh 41B9h 41B8h 41B7h 41B6h		419Eh 419Dh 419Ch 419Bh 419Ah 4199h 4198h 4197h 4196h		417Eh 417Dh 417Ch 417Bh 417Ah 4179h 4178h 4177h	DMAnSPTRL_DMA6 DMAnSCNTH_DMA6 DMAnSCNTL_DMA6 DMAnDSAH_DMA6 DMAnDSAH_DMA6 DMAnDSZH_DMA6 DMANDSZH_DMA6 DMANDSZL_DMA6 DMANDSZL_DMA6 DMANDFRH_DMA6	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h 4157h 4156h	DMANDCNTH_DMA5 DMANDCNTL_DMA5 DMANBUF_DMA5 DMANSIRQ_DMA4 DMANAIRQ_DMA4 DMANCON1_DMA4 DMANCON0_DMA4 DMANCSNU_DMA4 DMANCSNU_DMA4	413Eh 413Ch 413Ch 413Bh 413Ah 4139h 4138h 4137h 4136h	DMAnSSAL_DMA3 DMAnSSZH_DMA3 DMAnSSZL_DMA3 DMAnSSTRU_DMA3 DMAnSPTRU_DMA3 DMAnSPTRL_DMA3 DMAnSPTRL_DMA3 DMAnSCNTH_DMA3 DMAnSCNTH_DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h 4118h 4117h 4116h	DMAnDSAL_DMA2 DMAnDSZH_DMA2 DMAnDSZL_DMA2 DMAnDSZL_DMA2 DMAnDPTRH_DMA2 DMAnDPTRL_DMA2 DMAnDCNTH_DMA2 DMAnDCNTL_DMA2 DMANDCNTL_DMA2 DMANDLT_DMA2
41FEh 41FDh 41FCh 41FBh 41FAh 41F9h 41F8h 41F7h 41F6h 41F5h	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1	41DEh 41DDh 41DCh 41DBh 41DAh 41D9h 41D8h 41D7h 41D6h 41D5h		41BEh 41BDh 41BCh 41BBh 41BAh 41B9h 41B8h 41B7h 41B6h 41B5h		419Eh 419Dh 419Ch 419Bh 419Ah 4199h 4198h 4197h 4196h 4195h		417Eh 417Dh 417Ch 417Bh 417Ah 417Ah 4179h 4178h 4177h 4176h 4175h	DMAnSPTRL_DMA6 DMAnSCNTH_DMA6 DMANSCNTL_DMA6 DMANDSAH_DMA6 DMANDSAH_DMA6 DMANDSAL_DMA6 DMANDSZL_DMA6 DMANDSZL_DMA6 DMANDSZL_DMA6 DMANDPTRH_DMA6 DMANDPTRL_DMA6 DMANDPTRL_DMA6	415Eh 415Dh 415Ch 415Bh 415Ah 415Ah 4159h 4158h 4157h 4156h 4155h	DMANDCNTH_DMA5 DMANDLTD DMA5 DMANBUF_DMA5 DMANBUF_DMA4 DMANSIRQ_DMA4 DMANCON1_DMA4 DMANCON1_DMA4 DMANCON1_DMA4 DMANSSAU_DMA4 DMANSSAU_DMA4 DMANSSAL_DMA4 DMANSSAL_DMA4 DMANSSAL_DMA4	413Eh 413Dh 413Ch 413Bh 413Ah 4139h 4138h 4137h 4136h 4135h	DMAnSSAL_DMA3 DMAnSSZH_DMA3 DMAnSSZL_DMA3 DMAnSSZL_DMA3 DMAnSPTRU_DMA3 DMANSPTRL_DMA3 DMANSPTRL_DMA3 DMANSCNTH_DMA3 DMANSCNTH_DMA3 DMANSCNTL_DMA3 DMANDSAH_DMA3 DMANDSAL_DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h 4118h 4117h 4116h 4115h	DMANDSAL DMA2 DMANDSZH DMA2 DMANDSZH DMA2 DMANDSZL DMA2 DMANDPTRH DMA2 DMANDPTRL DMA2 DMANDENTH DMA2 DMANDENTH DMA2 DMANDENTH DMA2 DMANDUT DMA2 DMANBUF DMA2 DMANBUF DMA2 DMANBUR DMA1 DMANBUR DMA1
41FEh 41FDh 41FCh 41FBh 41FAh 41F9h 41F8h 41F7h 41F6h 41F5h 41F4h	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1	41DEh 41DDh 41DCh 41DBh 41DAh 41D9h 41D8h 41D7h 41D6h 41D5h 41D4h		41BEh 41BDh 41BCh 41BBh 41BAh 41B9h 41B8h 41B7h 41B6h 41B5h 41B4h		419Eh 419Dh 419Ch 419Bh 419Ah 4199h 4198h 4197h 4196h 4195h 4194h		417Eh 417Dh 417Ch 417Bh 417Ah 4179h 4178h 4177h 4176h 4175h 4174h	DMANSPTRL_DMA6 DMANSCNTH_DMA6 DMANSCNTL_DMA6 DMANDSAH_DMA6 DMANDSAL_DMA6 DMANDSAL_DMA6 DMANDSZL_DMA6 DMANDSZL_DMA6 DMANDSZL_DMA6 DMANDPTRL_DMA6 DMANDPTRL_DMA6 DMANDPTRL_DMA6 DMANDPTRL_DMA6 DMANDPTRL_DMA6 DMANDCNTL_DMA6	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h 4157h 4156h 4155h 4154h	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANBUF_DMAS DMANSIRQ_DMA4 DMANSIRQ_DMA4 DMANCON1_DMA4 DMANCON0_DMA4 DMANCSAU_DMA4 DMANSSAU_DMA4 DMANSSAU_DMA4 DMANSSAU_DMA4 DMANSSAL_DMA4 DMANSSAL_DMA4 DMANSSAL_DMA4 DMANSSAL_DMA4	413Eh 413Ch 413Ch 413Bh 413Ah 4139h 4138h 4137h 4136h 4135h 4134h	DMANSSAL_DMA3 DMANSSZH_DMA3 DMANSSZH_DMA3 DMANSSTRU_DMA3 DMANSPTRU_DMA3 DMANSPTRU_DMA3 DMANSPTRU_DMA3 DMANSCNTH_DMA3 DMANSCNTH_DMA3 DMANSCNTL_DMA3 DMANDSAH_DMA3 DMANDSAH_DMA3 DMANDSAL_DMA3 DMANDSZH_DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h 4118h 4117h 4116h 4115h 4114h	DMANDSAL DMA2 DMANDSZH DMA2 DMANDSZL DMA2 DMANDPTRL DMA2 DMANDPTRL DMA2 DMANDPTRL DMA2 DMANDCNTL DMA2 DMANDCNTL DMA2 DMANDCNTL DMA2 DMANDIC DMA1 DMANSIRQ DMA1 DMANIRQ DMA1 DMANIRQ DMA1 DMANIRQ DMA1
41FEh 41FDh 41FCh 41FBh 41FAh 41F9h 41F8h 41F7h 41F6h 41F5h 41F3h	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1	41DEh 41DDh 41DCh 41DBh 41DAh 41D9h 41D8h 41D7h 41D6h 41D5h 41D5h 41D4h 41D3h		41BEh 41BDh 41BCh 41BBh 41BAh 41B9h 41B8h 41B7h 41B6h 41B5h 41B4h 41B3h		419Eh 419Dh 419Ch 419Bh 419Ah 4199h 4197h 4196h 4195h 4194h 4193h		417Eh 417Ch 417Ch 417Bh 417Ah 4179h 4178h 4177h 4176h 4175h 4174h 4173h	DMAnSPTRL DMA6 DMAnSCNTH_DMA6 DMAnSCNTH_DMA6 DMAnSCNTL_DMA6 DMANDSAL_DMA6 DMANDSAL_DMA6 DMANDSAL_DMA6 DMANDSZL_DMA6 DMANDSZL_DMA6 DMANDSTRL_DMA6 DMANDTRL_DMA6 DMANDCNTL_DMA6 DMANDCNTL_DMA6 DMANDCNTL_DMA6 DMANDCNTL_DMA6	415Eh 415Dh 415Ch 4158h 415Ah 4159h 4158h 4157h 4156h 4155h 4155h 4154h	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANDLP_DMAS DMANSIRQ_DMAS DMANSIRQ_DMAA DMANAIRQ_DMAA DMANACONI_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANCSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAL_DMAA DMANSSZH_DMAA DMANSSZH_DMAA	413Eh 413Ch 413Ch 413Bh 413Ah 4139h 4138h 4137h 4136h 4135h 4134h 4133h	DMANSSAL DMA3 DMANSZE, DMA3 DMANSSZE, DMA3 DMANSPTRU_DMA3 DMANSPTRU_DMA3 DMANSPTRL_DMA3 DMANSPTRL_DMA3 DMANSCNTL_DMA3 DMANSCNTL_DMA3 DMANSCNTL_DMA3 DMANDSAL_DMA3 DMANDSAL_DMA3 DMANDSAL_DMA3 DMANDSAL_DMA3 DMANDSZE_DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 411Ah 4119h 4118h 4117h 4116h 4115h 4114h 4113h	DMANDSAL DMA2 DMANDSZH DMA2 DMANDSZH DMA2 DMANDSZH DMA2 DMANDFIRH DMA2 DMANDFIRH DMA2 DMANDCNTL DMA2 DMANDCNTL DMA2 DMANDCNTL DMA2 DMANBUF DMA2 DMANBUF DMA2 DMANBUF DMA2 DMANDRO DMA1 DMANCONI DMA1 DMANCONI DMA1
41FEh 41FDh 41FCh 41FBh 41FAh 41F9h 41F8h 41F7h 41F6h 41F5h 41F5h 41F3h 41F3h	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1	41DEh 41DDh 41DCh 41DBh 41DAh 41D9h 41D8h 41D7h 41D6h 41D5h 41D4h 41D3h 41D3h 41D3h 41D3h		41BEh 41BDh 41BCh 41BBh 41BAh 41B9h 41B8h 41B7h 41B6h 41B5h 41B4h 41B3h 41B3h 41B3h		419Eh 419Ch 419Ch 419Bh 419Ah 4199h 4198h 4197h 4196h 4195h 4194h 4193h 4192h	-	417Eh 417Ch 417Ch 417Bh 417Ah 4179h 4178h 4177h 4176h 4175h 4174h 4173h 4172h	DMAnSPTRL_DMA6 DMAnSCNTH_DMA6 DMAnSCNTH_DMA6 DMANDSAH_DMA6 DMANDSAH_DMA6 DMANDSZH_DMA6 DMANDSZH_DMA6 DMANDSZH_DMA6 DMANDSZH_DMA6 DMANDPTRL_DMA6 DMANDPTRL_DMA6 DMANDPTRL_DMA6 DMANDPTRL_DMA6 DMANDPTRL_DMA6 DMANDCNTL_DMA6 DMANDLAND_DMANDLAND_DMANDLAND_DMA6 DMANDLAND_DMA6 DMANDLAND_DMA6	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h 4157h 4156h 4155h 4154h 4153h 4152h	DMANDCNTH DMAS DMANDCNTL DMAS DMANBUF, DMAS DMANSIRO, DMAA DMANGIRO, DMAA DMANGOND, DMAA DMANGOND, DMAA DMANGOND, DMAA DMANGSAL, DMAA DMANSSAL, DMAA DMANSSAL, DMAA DMANSSZL, DMAA DMANSSZL, DMAA DMANSSZL, DMAA	413Eh 413Dh 413Ch 413Bh 413Ah 4139h 4138h 4137h 4136h 4135h 4134h 4133h 4132h	DMAnSSAL DMA3 DMAnSZZI, DMA3 DMAnSSZI, DMA3 DMAnSFIRU, DMA3 DMAnSFIRU, DMA3 DMANSFIRI, DMA3 DMANSFIRI, DMA3 DMANSCNTH, DMA3 DMANSCNTH, DMA3 DMANDSAL DMA3 DMANDSAL DMA3 DMANDSAL DMA3 DMANDSAL DMA3 DMANDSZI, DMA3 DMANDSZI, DMA3 DMANDSZI, DMA3 DMANDSZI, DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h 4118h 4117h 4116h 4115h 4114h 4113h 4112h	DMANDSAL_DMA2 DMANDSTH_DMA2 DMANDSTH_DMA2 DMANDSTH_DMA2 DMANDFTRH_DMA2 DMANDFTRH_DMA2 DMANDFTRH_DMA2 DMANDFTRH_DMA2 DMANDFTRH_DMA2 DMANSIRQ_DMA1 DMANSIRQ_DMA1 DMANGCON1_DMA1 DMANGCON1_DMA1 DMANGCON1_DMA1
41FEh 41FDh 41FCh 41FBh 41FAh 41F9h 41F8h 41F7h 41F6h 41F5h 41F4h 41F3h 41F2h 41F1h	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1	41DEh 41DDh 41DCh 41DBh 41DAh 41D9h 41D8h 41D7h 41D6h 41D5h 41D5h 41D4h 41D3h 41D2h 41D1h		418Eh 41BDh 41BCh 41BBh 41BAh 41B9h 41B7h 41B6h 41B5h 41B5h 41B4h 41B3h 41B2h 41B1h		419Eh 419Dh 419Ch 419Bh 419Ah 4199h 4198h 4197h 4196h 4195h 4194h 4193h 4192h 4191h		417Eh 417Dh 417Ch 417Bh 417Ah 4179h 4178h 4177h 4176h 4175h 4174h 4173h 4172h 4171h	DMANSPTRL DMA6 DMANSCNTH DMA6 DMANSCNTH DMA6 DMANDSAH DMA6 DMANDSAH DMA6 DMANDSAL DMA6 DMANDSZH DMA6 DMANDSZH DMA6 DMANDSZH DMA6 DMANDTRL DMA6 DMANDTRL DMA6 DMANDTRL DMA6 DMANDTRL DMA6 DMANDTRL DMA6 DMANDL DMA6 DMANDL DMA6 DMANBLF DMA6 DMANSIRQ DMA5 DMANSIRQ DMA5	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h 4157h 4156h 4155h 4154h 4153h 4152h 4151h	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANDUT_DMAS DMANSIRQ_DMAS DMANSIRQ_DMAA DMANCON1_DMAA DMANCON1_DMAA DMANCON1_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSEY_DMAA DMANSSEY_DMAA DMANSSTEY_DMAA DMANSPTRU_DMAA	413Eh 413Dh 413Ch 413Bh 413Ah 4139h 4138h 4137h 4136h 4135h 4134h 4133h 4132h 4131h	DMANSSAL DMA3 DMANSZH, DMA3 DMANSSZH, DMA3 DMANSFTRL, DMA3 DMANSFTRL, DMA3 DMANSFTRL, DMA3 DMANSFTRL, DMA3 DMANSCNTH, DMA3 DMANSCNTH, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDSZL, DMA3 DMANDSZL, DMA3 DMANDFTRL, DMA3 DMANDFTRL, DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h 4118h 4117h 4116h 4115h 4114h 4113h 4112h 4111h	DMANDSAL DMA2 DMANDSAL DMA2 DMANDSL DMA2 DMANDSL DMA2 DMANDPIRH DMA2 DMANDPIRH DMA2 DMANDCNTH, DMA2 DMANDCNTH, DMA2 DMANGUN DMA2 DMANGUN DMA1
41FEh 41FDh 41FCh 41FBh 41FAh 41FAh 41F7h 41F6h 41F5h 41F5h 41F4h 41F3h 41F2h 41F1h 41F1h	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1	41DEh 41DDh 41DCh 41DBh 41DAh 41D9h 41D8h 41D7h 41D6h 41D5h 41D4h 41D3h 41D2h 41D1h 41D1h		41BEh 41BCh 41BCh 41BBh 41BAh 41B9h 41B7h 41B6h 41B5h 41B4h 41B3h 41B3h 41B1h 41B1h 41B1h		419Eh 419Dh 419Ch 419Bh 419Ah 4199h 4198h 4197h 4196h 4195h 4194h 4193h 4192h 4191h 4190h		417Eh 417Dh 417Ch 417Rh 4178h 4179h 4177h 4177h 4176h 4175h 4173h 4172h 4171h 4171h 4171h	DMANSTRIL, DMAG DMANSCNTH, DMAG DMANSCNTL, DMAG DMANDSAH, DMAG DMANDSAH, DMAG DMANDSZH, DMAG DMANDSZH, DMAG DMANDSZH, DMAG DMANDSZH, DMAG DMANDFIRI, DMAG DMANDFIRI, DMAG DMANDCNTL, DMAG DMANDCNTL, DMAG DMANDCNTL, DMAG DMANDCNTL, DMAG DMANDCNTL, DMAG DMANDCNTL, DMAG DMANDLY, DMAG DMAG DMANDLY, DMAG DMAG DMARDLY, DMAG DMAG DMAG DMAG DMAG DMAG DMAG DMAG	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h 4157h 4156h 4155h 4154h 4153h 4152h 4151h 4150h	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANDNT_DMAS DMANSIRO_DMAS DMANSIRO_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANSSAH_DMAA DMANSSAH_DMAA DMANSSAH_DMAA DMANSSZH_DMAA DMANSSZH_DMAA DMANSSTRU_DMAA DMANSPTRU_DMAA DMANSPTRU_DMAA	413Eh 413Dh 413Ch 413Bh 413Ah 4139h 4138h 4137h 4136h 4135h 4134h 4133h 4132h 4131h 4130h	DMAnSSAL DMA3 DMAnSSZH DMA3 DMANSSZH DMA3 DMANSFIRU DMA3 DMANSFIRU DMA3 DMANSFIRU DMA3 DMANSFIRU DMA3 DMANSFIRU DMA3 DMANSFIRU DMA3 DMANDSAH DMA3 DMANDSAH DMA3 DMANDSAH DMA3 DMANDSZH DMA3 DMANDSZH DMA3 DMANDSZH DMA3 DMANDSZH DMA3 DMANDFIRU DMA3 DMANDFIRU DMA3 DMANDFIRU DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h 4118h 4117h 4116h 4115h 4114h 4113h 4114h 4111h 4111h 4110h	DMANDSAL_DMA2 DMANDSH_DMA2 DMANDSH_DMA2 DMANDSH_DMA2 DMANDFIRH_DMA2 DMANDFIRH_DMA2 DMANDCNTH_DMA2 DMANDCNTH_DMA2 DMANGSIRQ_DMA1 DMA3SIRQ_DMA1 DMANGCONI_DMA1 DMANGCONI_DMA1 DMANGSAL_DMA1 DMANSSAL_DMA1 DMANSSAL_DMA1 DMANSSAL_DMA1
41FEh 41FDh 41FCh 41FBh 41FBh 41F9h 41F7h 41F6h 41F5h 41F4h 41F3h 41F2h 41F1h 41F0h 41F2h 41F1h	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1	41DEh 41DDh 41DCh 41DBh 41DAh 41D9h 41D8h 41D7h 41D6h 41D5h 41D4h 41D3h 41D4h 41D2h 41D1h 41D1h 41D0h 41D1h 41D0h 41D6h		41BEh 41BCh 41BCh 41BBh 41BAh 41B9h 41B7h 41B6h 41B5h 41B4h 41B3h 41B3h 41B1h 41B1h 41B1h 41B1h 41B1h 41B1h		419Eh 419Dh 419Ch 419Bh 4199h 4199h 4197h 4196h 4195h 4194h 4193h 4192h 4191h 4190h 418Fh		417Eh 417Dh 417Ch 417Rh 417Ah 4179h 4178h 4177h 4176h 4175h 4174h 4173h 4172h 4171h 4170h 416Fh	DMANSPTRL DMA6 DMANSPTRL DMA6 DMANDSAH DMA6 DMANDSAH DMA6 DMANDSAH DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDPTRH, DMA6 DMANDPTRH, DMA6 DMANDCNTH,	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h 4157h 4156h 4155h 4154h 4153h 4152h 4151h 4150h 414Fh	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANDST_DMAS DMANSIRQ_DMAA DMANSIRQ_DMAA DMANCON1_DMAA DMANCON1_DMAA DMANCON1_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSTEN_DMAA DMANSSTEN_DMAA DMANSSTEN_DMAA DMANSFIRU_DMAA DMANSFIRU_DMAA DMANSFIRU_DMAA DMANSFIRU_DMAA	413Eh 413Dh 413Ch 413Bh 413Ah 4139h 4138h 4137h 4136h 4135h 4134h 4133h 4132h 4131h 4130h 412Fh	DMANSSAL DMA3 DMANSSZH DMA3 DMANSSZH DMA3 DMANSSTR DMA3 DMANSFTRU DMA3 DMANSFTRU DMA3 DMANSFTRI DMA3 DMANSFTRI DMA3 DMANSCATL DMA3 DMANSCATL DMA3 DMANDSAL DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h 4118h 4117h 4116h 4115h 4114h 4113h 4114h 4111h 4110h 4110h 4110h	DMANDSAL DMA2 DMANDSAL DMA2 DMANDSCH DMA2 DMANDSCH DMA2 DMANDTRH DMA2 DMANDFRH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNT DMA1 DMANDCND DMA1 DMANDCND DMA1 DMANDSAL DMA1
41FEh 41FDh 41FCh 41FEh 41FAh 41F9h 41F8h 41F7h 41F5h 41F5h 41F4h 41F3h 41F2h 41F1h 41F0h 41EFh	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1	41DEh 41DDh 41DCh 41DBh 41DAh 41D9h 41D8h 41D7h 41D6h 41D5h 41D4h 41D3h 41D2h 41D1h 41D1h 41D0h 41CFh 41CEh		418Eh 418Dh 418Ch 418Bh 418Ah 4189h 4187h 4186h 4185h 4185h 4184h 4183h 4182h 4181h 4181h 4181h 4181h 4181h		419Eh 419Dh 419Ch 419Bh 4199h 4198h 4197h 4196h 4195h 4194h 4193h 4192h 4191h 4190h 418Fh 418Eh		417Eh 417Dh 417Ch 417Rh 417Ah 4179h 4178h 4177h 4176h 4175h 4174h 4173h 4171h 4171h 416Fh 416Eh	DMANSPTRL DMAS DMANSTRTH DMAS DMANSCNTH DMAS DMANDSAH DMAS DMANDSAH DMAS DMANDSAH DMAS DMANDSZH DMAS DMANDSZH DMAS DMANDSZH DMAS DMANDSZH DMAS DMANDSZH DMAS DMANDFTRL DMAS DMANDFTRL DMAS DMANDCNTL DMAS DMANDCNTL DMAS DMANGCNTL DMAS	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h 4157h 4156h 4155h 4155h 4154h 4152h 4151h 4151h 4150h 414Fh	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANDKT_DMAS DMANSIRO_DMAS DMANSIRO_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANCSAN_DMAA DMANSSAN_DMAA DMANSSAN_DMAA DMANSSAN_DMAA DMANSSTRI_DMAA DMANSTRIL_DMAA DMANSFIRI_DMAA DMANSFIRI_DMAA DMANSFIRI_DMAA DMANSFIRI_DMAA DMANSFIRI_DMAA	413Eh 413Dh 413Ch 413Bh 413Ah 4138h 4137h 4136h 4135h 4135h 4135h 4131h 4131h 4130h 412Fh 412Eh	DMANSSAL DMA3 DMANSSZH DMA3 DMANSSZH DMA3 DMANSFIRU DMA3 DMANSFIRU DMA3 DMANSFIRI DMA3 DMANSFIRI DMA3 DMANSFIRI DMA3 DMANSCATL DMA3 DMANDSAH DMA3 DMANDSAH DMA3 DMANDSAH DMA3 DMANDSZH DMA3 DMANDSZH DMA3 DMANDSZH DMA3 DMANDFIRI DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 4119h 4119h 4116h 4115h 4111h 4113h 4112h 4111h 4110h 410Fh 410Eh	DMANDSAL DMA2 DMANDSAL DMA2 DMANDSTH DMA2 DMANDSTH DMA2 DMANDSTH DMA2 DMANDFIRH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTD DMA2 DMANSIRQ DMA1 DMANSIRQ DMA1 DMANSIRQ DMA1 DMANSSAL DMA1 DMANSSAL DMA1 DMANSSAL DMA1 DMANSSAL DMA1 DMANSSAL DMA1
41FEh 41FDh 41FCh 41FBh 41F8h 41F8h 41F7h 41F6h 41F5h 41F4h 41F3h 41F1h 41F0h 41EFh 41EEh	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1	41DEh 41DDh 41DCh 41DBh 41DBh 41D9h 41D8h 41D7h 41D6h 41D5h 41D4h 41D3h 41D2h 41D1h 41D0h 41CPh 41CCh 41CCh		418Eh 418Dh 418Ch 418Bh 418Ah 4189h 4188h 4187h 4186h 4185h 4184h 4183h 4182h 4181h 4181h 4180h 41AFh 41AEh 41ADh		419Eh 419Dh 419Ch 419Bh 4199h 4198h 4197h 4196h 4195h 4194h 4193h 4192h 4191h 4190h 418Fh 418Eh 418Dh		417Eh 417Dh 417Ch 417Bh 417Ah 4179h 4177h 4176h 4175h 4175h 4174h 4173h 4172h 4171h 4171h 416Fh 416Eh 416Dh	DMANSPTRL DMA6 DMANSPTRL DMA6 DMANSCNTL DMA6 DMANDSAH DMA6 DMANDSAH DMA6 DMANDSAH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDPTRH, DMA6 DMANDPTRH, DMA6 DMANDPTRH, DMA6 DMANDCNTH, DMA6 DMANGCNT, DMA6 DMANGCNT, DMA6 DMANGCNT, DMA6 DMANGCNT, DMA6 DMANGCND, DMA5 DMANGCND, DMA5 DMANGCND, DMA5 DMANGCND, DMA5 DMANGSAU, DMA5	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h 4157h 4156h 4155h 4153h 4153h 4152h 4151h 4150h 414Fh 414Eh 414Dh	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANDST_DMAS DMANSRQ_DMAS DMANSRQ_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSTRU_DMAA DMANSSTRU_DMAA DMANSSTRU_DMAA DMANSSTRU_DMAA DMANSSTRU_DMAA DMANSSTRU_DMAA DMANSSTRU_DMAA	413Eh 413Dh 413Ch 413Bh 413Ah 4138h 4137h 4136h 4135h 4134h 4133h 4131h 4131h 4130h 412Fh 412Eh 412Dh	DMANSSAL, DMA3 DMANSSZP, DMA3 DMANSSZP, DMA3 DMANSSTR, DMA3 DMANSFTRU, DMA3 DMANSFTRI, DMA3 DMANSFTRI, DMA3 DMANSCOTI, DMA3 DMANSCOTI, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDSZI, DMA3	411Eh 411Dh 411Ch 411Bh 411Ah 411Ah 4119h 4118h 4117h 4116h 4115h 4114h 4111h 4112h 4111h 4110h 410Ph 410Ph 410Dh	DMANDSAL DMA2 DMANDSAL DMA2 DMANDSZH DMA2 DMANDSZL DMA2 DMANDPTRH DMA2 DMANDPTRH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANBUF DMA2 DMANBUF DMA2 DMANBUF DMA2 DMANBUF DMA2 DMANBUF DMA1 DMANGCOND DMA1 DMANGCOND DMA1 DMANSSAL DMA1
41FEh 41FDh 41FCh 41FBh 41FAh 41FSh 41FSh 41FSh 41FSh 41F3h 41F3h 41F2h 41F1h 41FCh 41EFh 41EFh 41ECh 41ECh 41ECh 41ECh 41ECh 41ECh 41ECh 41ECh 41ECh 41ECh	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1	41DEh 41DCh 41DCh 41DCh 41DBh 41D8h 41D7h 41D8h 41D7h 41D6h 41D5h 41D4h 41D2h 41D1h 41D1h 41CEh 41CCh 41CCh 41CCh 41CCh 41CCh 41CCh 41CCh 41CCh 41CAh		418Eh 418Dh 418Ch 418Bh 4188h 4188h 4188h 4187h 4186h 4185h 4184h 4181h 4180h 4184h 414Eh 41ACh 41ACh 41ACh 41AAh		419Eh 419Dh 419Ch 419Bh 419Ah 4199h 4199h 4197h 4196h 4195h 4194h 4191h 4190h 418Fh 418Eh 418Bh 418Ch 418Bh		417Eh 417Dh 417Ch 417Bh 4178h 4179h 4178h 4177h 4176h 4175h 4173h 4173h 4171h 4170h 416Fh 416Eh 416Eh 416Bh 416Bh	DMANSPTRL DMA6 DMANSPTRL DMA6 DMANSCNTI, DMA6 DMANDSAH, DMA6 DMANDSAH, DMA6 DMANDSAH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDPTRH, DMA6 DMANDCNTH, DMA6 DMANSSAH, DMA5 DMANSSAH, DMA5 DMANSSAH, DMA5 DMANSSAH, DMAS DMANSSAH, DMAS DMANSSAH, DMAS DMANSSAH, DMAS DMANSSAH, DMAS	415Eh 415Dh 415Ch 415Sh 415Sh 415Sh 415Sh 415Sh 415Sh 415Sh 415Sh 415Sh 415Sh 415Sh 415Sh 415Ch 414Ch 414Eh 414Ch 414Ch 414Ch 414Rh 414Ah	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANDUT_DMAS DMANSINO_DMAS DMANSINO_DMAS DMANSINO_DMAS DMANCONI_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANSAN_DMAM DMANSSAN_DMAA DMANSSAN_DMAA DMANSSAN_DMAA DMANSSTRU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSCNTL_DMAA DMANSCNTL_DMAA DMANDSAN_DMAA DMAADSAN_DMAA DMAADSAN_DMAA DMAADSAN_DMAA DMAADSAN_DMAA DMAA DMAADSAN_DMAA	413Eh 413Dh 413Ch 413Bh 413Ah 413Ah 4137h 4136h 4135h 4135h 4131h 4130h 412Fh 412Eh 412Eh 412Eh 412Bh 412Ah	DMANSSAL DMA3 DMANSSZI, DMA3 DMANSSZI, DMA3 DMANSSTZ, DMA3 DMANSFTRU, DMA3 DMANSFTRU, DMA3 DMANSFTRI, DMA3 DMANSFTRI, DMA3 DMANSCATI, DMA3 DMANSCATI, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDSZI, DMA3 DMANDSZI, DMA3 DMANDSZI, DMA3 DMANDSZI, DMA3 DMANDSZI, DMA3 DMANDFTRI, DMA3 DMA3 DMANDF	411Eh 411Dh 411Ch 411Bh 411Ah 411Ah 411Ah 411Ah 411Ah 411Ah 411Ah 411Ah 411Ah 411Ah 411Ch 410Ch 410Ch 410Ch 410Ch 410Ch 410Ch 410Ch 410Ch 410Ch	DMANDSAL DMA2 DMANDSAL DMA2 DMANDSAL DMA2 DMANDSAL DMA2 DMANDFIRH DMA2 DMANDFIRH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANGCNTH DMA2 DMANGCNTH DMA2 DMANGCNT DMA2 DMANGCNT DMA2 DMANGSAL DMA1 DMA1 DMA1 DMA1 DMA1 DMA1 DMA1 DMA1
41FEh 41FDh 41FCh 41FBh 41FBh 41FBh 41F7h 41F7h 41F6h 41F3h 41F3h 41F3h 41F1h 41F0h 41EEh 41EEh 41EEh 41EEh 41EEh	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1	41DEh 41DDh 41DCh 41DBh 41DBh 41D9h 41D8h 41D7h 41D6h 41D5h 41D4h 41D4h 41D2h 41D1h 41CH 41CCh 41CCh 41CCh 41CCh		418Eh 418Dh 418Ch 418Bh 418Ah 4189h 4187h 4185h 4185h 4182h 4181h 4181h 4181h 4181h 4184h		419Eh 419Dh 419Ch 419Bh 419Ah 4199h 4198h 4197h 4195h 4195h 4193h 4192h 4193h 418Ph 418Bh 418Ch 418Ch 418Bh		417Eh 417Dh 417Ch 417Bh 417Ah 4178h 4178h 4176h 4176h 4175h 4174h 4172h 4171h 4171h 4166h 4166h 4166h 416Ch 416Ch	DMANSPTRL DMAS DMANSCATH DMAS DMANSCATH DMAS DMANSCATH DMAS DMANDSAH DMAS DMANDSAH DMAS DMANDSAH DMAS DMANDSAH DMAS DMANDSAH DMAS DMANDSTRL DMAS DMANDFRL DMAS DMANDFRL DMAS DMANDFRL DMAS DMANDFRL DMAS DMANDFRL DMAS DMANDFRL DMAS DMANSSAL DMAS	415Eh 415Dh 415Ch 415Bh 415Ah 4159h 4158h 4155h 4155h 4155h 4154h 4152h 4151h 4150h 414Eh 414Eh 414Eh 414Ch 414Ch	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANBUF_DMAS DMANSRO_DMAA DMANSRO_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSTRI_DMAA DMANSPTRIL_DMAA DMANSPTRIL_DMAA DMANSPTRIL_DMAA DMANSCNTIL_DMAA DMANSCNTIL_DMAA DMANSCNTIL_DMAA DMANSCNTIL_DMAA DMANSCNTIL_DMAA DMANSCNTIL_DMAA DMANSCNTIL_DMAA DMANDSAL_DMAA DMANDSAL_DMAA DMANDSAL_DMAA	413Eh 413Dh 413Ch 4138h 4133h 4138h 4137h 4136h 4137h 4132h 4131h 4130h 412Eh 412Eh 412Ch 412Ch 412Ch 412Bh	DMANSAL DMA3 DMANSSZL DMA3 DMANSSZL DMA3 DMANSFYRU, DMA3 DMANSFYRU, DMA3 DMANSFYRI, DMA3 DMANSFYRI, DMA3 DMANSFYRI, DMA3 DMANSCATI, DMA3 DMANSCATI, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDSAL, DMA3 DMANDFYRI, DMA3 DMA3 DMANDFYRI, DMA3 DMA3 DMA3 DMA3 DMA3 DMA3 DMA3 DMA3	411Eh 411Dh 411Ch 411Bh 4118h 4118h 4117h 4117h 4116h 4117h 4116h 4111h 4110h 410Ch	DMANDSAL DMA2 DMANDSZL DMA2 DMANDSZL DMA2 DMANDSZL DMA2 DMANDSZL DMA2 DMANDFIL DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDSCNTD DMA2 DMANDSCNTD DMA1 DMANDSCNTD DMA1 DMANDSCNTD DMA1 DMANDSSZL DMA1 DMANDSZL DMA1 DMANDSSZL DMA1 DMANDSSZL DMA1 DMANDSZL DMA1 DMA1 DMA1 DMA1 DMA1 DMA1 DMA1 DMA1
41FEh 41FDh 41FCh 41FBh 41FAh 41F9h 41F8h 41F5h 41F5h 41F5h 41F2h 41F2h 41F2h 41F1h 41FCh 41EFh 41EFh 41ECh	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1	41DEh 41DCh 41DCh 41DCh 41DBh 41D8h 41D8h 41D7h 41D6h 41D5h 41D4h 41D3h 41D4h 41D1h 41CCh 41CCh 41CCh 41CBh 41CCh 41CBh 41CCh 41CCh 41CBh 41CSh		418Eh 418Dh 418Ch 4188h 4188h 4188h 4188h 4188h 4188h 4182h 4182h 4182h 4182h 4182h 4182h 4182h 4182h 4184h		419Eh 419Dh 419Ch 4198h 4199h 4199h 4199h 4198h 4195h 4195h 4191h 4191h 4191h 4181h 4181h 4181h 4188h 4188h 4188h 4188h	DMAnSRQ_DMA6	417Eh 417Dh 417Ch 417Ah 4178h 4179h 4179h 4176h 4177h 4177h 4177h 4177h 4170h 416Ch 416Ch 416Ch 416Ch 416Bh 416Bh 4168h 4168h	DMANSPTRU, DMA6 DMANSPTRU, DMA6 DMANDSAH, DMA6 DMANDSAH, DMA6 DMANDSAH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDPTRH, DMA6 DMANSRO, DMA5 DMANSRO, DMA5 DMANSRO, DMA5 DMANSSAL, DMA5 DMANSSAL, DMA5 DMANSSAL, DMA5 DMANSSAL, DMA5 DMANSSAL, DMA5 DMANSSAL, DMA5 DMANSSPTRU, DMA5 DMANSSPTRU, DMA5 DMANSSPTRU, DMA5 DMANSSPTRU, DMA5 DMANSSPTRU, DMA5	415Eh 415Dh 415Ch 4158h 4158h 4158h 4158h 4157h 4156h 4153h 4154h 4151h 414Eh 414Ch 414Ch 414Ah 414Ah 4148h	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANDLTL_DMAS DMANSIRQ_DMAS DMANSIRQ_DMAA DMANCON1_DMAA DMANCON1_DMAA DMANCON1_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANSCONTL_DMAA DMANSCONTL_DMAA DMANDSAU_DMAA	413Eh 413Ch 413Ch 413Ah 413Ah 4139h 4138h 4137h 4136h 4134h 4134h 4134h 4134h 412Ch	DMANSSAL DMA3 DMANSSZI, DMA3 DMANSSZI, DMA3 DMANSSTRU, DMA3 DMANSPTRU, DMA3 DMANSPTRU, DMA3 DMANSPTRU, DMA3 DMANSPTRU, DMA3 DMANSCATI, DMA3 DMANDSAL, DMA3 DMANDSTL, DMA3 DMANDFRI, DMA3 DMANDFRID, DMA3 DMA3 DMANDFRID, DMA3 DMA3 DMA3 DMA3 DMA3 DMA3 DMA3 DMA3	411Eh 411Dh 411Ch 411Bh 4111Bh 4111Bh 4111Bh 4117h 4116h 4115h 4111Ah 4111Ah 4111Ah 4111Ch 411Ch 410Ch 410Ch 410Ch 410Bh 410Ah 410Ah 410Ah 410Bh 410Ah 410Ah 410Ah 410Bh 410Ah 410Ah 410Bh 410Ah 410Bh 410Ah 410Bh	DMANDSAL DMA2 DMANDSAL DMA2 DMANDSAL DMA2 DMANDTRH DMA2 DMANDTRH DMA2 DMANDTRH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANGCNT DMA2 DMANGCNT DMA2 DMANGCNT DMA1 DMANGCNT DMA1 DMANGCNT DMA1 DMANGCNT DMA1 DMANGSAL DMA1 DMANGSTRL DMA1 DMANGSCNTL DMA1
41FEh 41FDh 41FCh 41FBh 41FAh 41F9h 41F8h 41F7h 41F6h 41F3h 41F2h 41F1h 41F2h 41F1h 41ECh	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1	41DEh 41DDh 41DCh 41DBh 41DBh 41DSh 41DSh 41DSh 41DSh 41DSh 41DSh 41DLh 41DLh 41DLh 41DLh 41CEh 41CCh		418Eh 418Dh 418Ch 418Bh 4188h 4189h 4188h 4184h 4184h 4184h 4184h 4184h 4184h 4184h 4184h 414Ah		419Eh 419Ch 419Ch 419Ah 419Ah 4199h 4199h 4199h 4195h 4194h 4194h 4193h 4191h 418Ch 418Eh 418Ch 418Bh 418Ah	DMAnSRQ_DMA6 DMAnAIRQ_DMA6 DMAnAIRQ_DMA6	417Eh 417Dh 417Ch 417Ah 4179h 4179h 4179h 4179h 4177h 4177h 4177h 4177h 4177h 4170h 416Eh 416Ch 416Ch 416Ch 416Bh 416Ah	DMANSPTRL DMAS DMANSCATH DMAS DMANSCATH DMAS DMANSCATH DMAS DMANDSAH DMAS DMANSSAL DMAS	415Eh 415Dh 415Ch 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 416Ah 414Ah 414Ah 414Ah 414Ah 414Ah 414Ah 414Ah 414Ah 414Ah	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANBUF_DMAS DMANBUF_DMAS DMANSIRO_DMAM DMANCONI_DMAM DMANCONI_DMAM DMANCONI_DMAM DMANSSAL_DMAM DMANSSAL_DMAM DMANSSAL_DMAM DMANSSAL_DMAM DMANSSTRI_DMAM DMANSSTRI_DMAM DMANSSTRI_DMAM DMANSSTRI_DMAM DMANSSTRI_DMAM DMANSCNTL_DMAM DMANDSAL_DMAM DMANDSAL_D	413Eh 413Ch 413Sh 413Ah 413Ah 413Ah 413Ah 413Ch 413Ch 413Ch 413Ch 413Ch 413Ch 412Ch	DMANSAL DMA3 DMANSSZH DMA3 DMANSSZH DMA3 DMANSPTRU DMA3 DMANSPTRU DMA3 DMANSPTRU DMA3 DMANSPTRU DMA3 DMANSPTRU DMA3 DMANSCATL DMA3 DMANSCATL DMA3 DMANSCATL DMA3 DMANDSAL DMA3 DMANDSAL DMA3 DMANDSAL DMA3 DMANDSAL DMA3 DMANDSTRU DMA3 DMANDFRU	411Eh 411Dh 411Ch 411Bh 411Bh 411Bh 411Ah 4119h 4116h 4115h 4116h 4111h 4110h 4110h 410Ch	DMANDSAL, DMA2 DMANDSZL, DMA2 DMANDSZL, DMA2 DMANDSZL, DMA2 DMANDSZL, DMA2 DMANDFIL, DMA2 DMANDCNTH, DMA2 DMANDCNTH, DMA2 DMANDCNTH, DMA2 DMANDCNTH, DMA2 DMANDSQL, DMA1 DMANDSQL, DMA1 DMANDSQL, DMA1 DMANDSQL, DMA1 DMANDSQL, DMA1 DMANDSQL, DMA1 DMANDSZL, DMA1 DMANDZL, DMA1 DMANDZL, DMA1 DMA1 DMA1 DMA1 DMA1 DMA1 DMA1 DMA1
41FEh 41FDh 41FCh 41FBh 41FBh 41F8h 41F8h 41F7h 41F6h 41F5h 41F3h 41F2h 41F1h 41F0h 41FCh 41EDh 41EDh 41EDh 41EBh	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1	41DEh 41DCh 41DCh 41DBh 41DBh 41DBh 41DBh 41D7h 41D6h 41D7h 41D3h 41D2h 41D1h 41D2h 41D1h 41CCh		418Eh 418Dh 418Ch 418Bh 4188h 4189h 4189h 4189h 4185h 4185h 4185h 4181h 4181h 4181h 4181h 4184h		419Eh 419Ch 419Sh 4199Ah 4199Ah 4199Ah 4199Ah 4199Ah 4195Ah 4191Ah 4193Ah 4191Ah 4191Ah 418Eh 418Eh 418Eh 418BA 418BA 41	DMANSIRQ DMA6 DMANCON1 DMA6 DMANCON1 DMA6	417Eh 417Dh 417Ch 417Ah 417Ah 4173h 4177h 4176h 4176h 4176h 4175h 4171h 4171h 416Ch 416Eh 416Ch 416Bh 416Ah 4169h 4168h 4168h 4168h 4168h 4168h 4168h	DMANSPTRL, DMA6 DMANSPTRL, DMA6 DMANDSAH, DMA6 DMANDSAH, DMA6 DMANDSAH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDSZH, DMA6 DMANDTRH, DMA6 DMANDTRH, DMA6 DMANDTRH, DMA6 DMANDTRH, DMA6 DMANSINQ, DMAS DMANSSAU, DMA5 DMANSSAU, DMA5 DMANSSAU, DMA5 DMANSSAU, DMA5 DMANSSAU, DMA5 DMANSSAU, DMA5 DMANSSZH, DMA5 DMANSSZH, DMA5 DMANSSTRL, DMA5	415Eh 415Dh 415Ch 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 414Eh 414Ch 414Ch 414Ah 414Ah 414Ah 414Ah 414Ah 414Ah 414Ah 414Ah	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANDST_DMAS DMANSIRQ_DMAS DMANSIRQ_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSTEN_DMAA DMANSSTEN_DMAA DMANSSTEN_DMAA DMANSPIRU_DMAA DMANSPIRU_DMAA DMANDST_DMAA	413Eh 413Ch 413Ch 413Ah 413Ah 413Ah 4137h 4136h 4135h 4135h 4135h 4132h 413Ch 412Ch	DMANSSAL DMA3 DMANSSZH DMA3 DMANSSZH DMA3 DMANSSTR DMA3 DMANSFTRU DMA3 DMANSFTRU DMA3 DMANSFTRI DMA3 DMANSFTRI DMA3 DMANSFTRI DMA3 DMANSCATI DMA3 DMANDSAL DMA3 DMANDSAL DMA3 DMANDSAL DMA3 DMANDSZH DMA3 DMANDCATI DMA3 DMA3 DMA3 DMA3 DMA3 DMA3 DMA3 DMA3	411Eh 411Dh 411Ch 411Bh 411Bh 411Ah 411Bh 4117h 4116h 4115h 4111h 4111h 4110h 410Ch	DMANDSAL DMA2 DMANDSAL DMA2 DMANDSAL DMA2 DMANDSAL DMA2 DMANDTRH DMA2 DMANDTRH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDSAL DMA1
41FEh 41FDh 41FCh 41FBh 41FBh 41FBh 41FBh 41FBh 41FBh 41FBh 41FBh 41FBh 41FBh 41FBh 41FBh 41FCh	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1	410Eh 410DH 410CH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410CH 41CCH 41CCH 41CCH 41CCH 41CCH 41CCH 41CSH		418Eh 418Dh 418Bh 4188h 4188h 4188h 4186h 4186h 4186h 4184h 4184h 4184h 4180h 41AEh 41AEh 41ACh 41ACh 41AAh 41A8h 41A3h		419Eh 419Ch 419Sh 419Sh 4199h 4198h 4197h 4195h 4195h 4195h 4195h 4195h 4195h 418Eh 418Ch 418Ch 418Ch 418Bh 418Ch 418Bh 418Ch 418Bh	DMAnSIRQ_DMA6 DMAnAIRQ_DMA6 DMAnCONQ_DMA6 DMANCONQ_DMA6	417Eh 417Dh 417Ch 417Bh 4178h 4178h 4178h 4177h 4177h 4176h 4175h 4171h 4171h 4170h 416Eh 416Dh 416Eh 416Bh 416Sh 416Sh 416Sh 416Sh 416Sh 416Sh 416Sh	DMANSPTRL DMAS DMANSCATH DMAS DMANSCATH DMAS DMANSCATH DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSTRL DMAS DMANDSTRL DMAS DMANDSTRL DMAS DMANDSTRL DMAS DMANDSTRL DMAS DMANDSTRL DMAS DMANSSAL DMAS DMANSSALL DMAS DMANSSALL DMAS	415Eh 415Bh 415Ah 415Bh 415Ah 4159h 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 415Ah 414Ah	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANBUF_DMAS DMANBUF_DMAS DMANBUF_DMAS DMANBUF_DMAS DMANBUF_DMAS DMANGON_DMAS DMANGON_DMAS DMANGSAL_DMAS DMANGSAL_DMAS DMANSSAL_DMAS DMANSSAL_DMAS DMANSSTRL_DMAS DMANSSTRL_DMAS DMANSFIRL_DMAS DMANSFIRL_DMAS DMANSFIRL_DMAS DMANSFIRL_DMAS DMANSFIRL_DMAS DMANSFIRL_DMAS DMANSFIRL_DMAS DMANDSAL_DMAS DMAS DMAS DMAS DMAS DMAS DMAS DMAS	413Eh 413Ch 413Ch 413Bh 413Bh 413Bh 413Bh 413Ch 413Ch 413Ch 413Ch 413Ch 413Ch 413Ch 412Ch	DMANSAL DMAS DMANSSZH DMAS DMANSSZH DMAS DMANSSZH DMAS DMANSFIRL DMAS DMANSFIRL DMAS DMANSFIRL DMAS DMANSFIRL DMAS DMANSFIRL DMAS DMANSCONT, DMAS DMANDAL DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSZH DMAS DMANDSZH DMAS DMANDSZH DMAS DMANDFIRL DMAS DMAN	4116h 4110h 4110h 41113h 4113h 4113h 4113h 4113h 4113h 4113h 4113h 4113h 4110h 4106h 4106h 4108h 4106h 4108h 4106h	DMANDSAL DMA2 DMANDSAL DMA1
41FEh 41FDh 41FCh 41FBh 41FBh 41FBh 41FBh 41FBh 41FSh 41FSh 41FSh 41F3h 41F3h 41F3h 41F2h 41EDh 41EDh 41EDh 41EDh 41EBh	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1 TMRSH_M1	41DEh 41DEh 41DEh 41DEh 41DBH 41DBH 41DBH 41DBH 41DBH 41DBH 41DBH 41DBH 41DBH 41DBH 41DBH 41DBH 41DBH 41CBH		418Eh 418Dh 418Bh 418Lh 418Lh 418Lh 41ABh 41AEh		419Eh 419Dh 419Ch 419Sh 4198h 4198h 4198h 4198h 4195h 4195h 4195h 4191h 4192h 4191h 418Eh 418Eh 418Eh 418Bh	DMAnSIRQ_DMA6 DMAnCON1_DMA6 DMAnCON1_DMA6 DMAnCON0_DMA6 DMANCSON_DMA6	417Eh 417Dh 417Ch 417Ah 4178h 4178h 4178h 4178h 4176h 4176h 4176h 4176h 4171h 4170h 416Ch 416Ch 416Bh 416Ch 416Bh 416Sh 4168h 4168h 4168h 4167h 4168h 4168h 4168h 4166h 4166h 4166h 4166h 4166h 4166h 4166h	DMANSPTRL DMA6 DMANSPTRL DMA6 DMANDSAH DMA6 DMANDSAH DMA6 DMANDSAH DMA6 DMANDSAH DMA6 DMANDSZH DMA6 DMANDSZH DMA6 DMANDSZH DMA6 DMANDSZH DMA6 DMANDSZH DMA6 DMANDFRH DMA6 DMANDFRH DMA6 DMANDFRH DMA6 DMANDFRH DMA6 DMANDFRH DMA6 DMANSRQ DMAS DMANGNA DMAS DMANSRQ DMAS DMANSSAL DMAS	415Eh 415Ch 415Ch 415Ch 415Bh 415Ah 415Ah 415Ah 415Ch 415Ch 415Ch 415Ch 415Ch 415Ch 414Ch	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANDSTD, DMAS DMANSRQ_DMAA DMANSRQ_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSAU_DMAA DMANSSTRU_DMAA DMANSSTRU_DMAA DMANSSTRU_DMAA DMANSSTRU_DMAA DMANSTRU_DMAA DMANDSTRU_DMAA DMANDSTRU_DMAA DMANDSTRU_DMAA DMANDSTRU_DMAA DMANDSTRU_DMAA DMANDSAU_DMAA	413Eh 413Ch 413Ch 413Ah 413Ah 413Ah 413Ah 413Ah 413Ah 413Ah 413Ch 413Ch 413Ch 412Ch	DMANSSEL DMA3 DMANSSEL DMA3 DMANSSEL DMA3 DMANSFEL DMA3 DMANSFEL DMA3 DMANSFEL DMA3 DMANSFEL DMA3 DMANSFEL DMA3 DMANSFEL DMA3 DMANSCOTTL DMA3 DMANSCOTTL DMA3 DMANDSEL DMA3	411Eh 411Dh 411Ch 411Bh 410Ch 410Bh 410Ch 410Bh	DMANDSAL DMA2 DMANDSAL DMA2 DMANDSAL DMA2 DMANDSAL DMA2 DMANDTRH DMA2 DMANDFRH DMA2 DMANDCNTH DMA2 DMANDSAL DMA1
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41FEH 41FDH 41FCH 41FBH 41 41 41 41 41 41 41 41 41 41 41 41 41	TMRSH_M1 TMRSL_M1 TMRSH_M1 TMR	410Eh 410DH 410BH		418Eh 418Dh 418Ch 418Bh 418Ch 418Ah 41ACh		419Eh 419Ch 419Ch 419Sh 4198h 4198h 4199h 4197h 4196h 4195h 4193h 4192h 4193h 4192h 418Eh	DMANSIRQ DMA6 DMANAIRQ, DMA6 DMANCON1, DMA6 DMANCON1, DMA6 DMANSSAU, DMA6 DMANSSAU, DMA6 DMANSSAU, DMA6 DMANSSAU, DMA6	417Eh 417Oh 417Ch 417Ah 4178h 4178h 4177h 4177h 4177h 4177h 4177h 4171h 4170h 416Ch	DMANSPTRL, DMA6 DMANSSTRL, DMA6 DMANSCNTL, DMA6 DMANDSAH, DMA6 DMANDSAH, DMA6 DMANDSAH, DMA6 DMANDSZH, DMA6 DMANSSAU, DMA5 DMANSSTRL, DMA5 DMANSSTRL, DMA5 DMANSPTRL, DMA5 DMANSSTRL, DMA5 DMANSSTRL, DMA5 DMANSPTRL, DMA5 DMANSSTRL, DMA5 DMANSSAU, DMA5 DMANSSAU, DMA5 DMANSSAU, DMA5 DMANDSAL, DMA5 DMANDSAL, DMA5 DMANDSAL, DMA5 DMANDSAL, DMA5 DMANDSAL, DMA5	415Eh 415Dh 415Bh 415Ah 414Ah	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANDSNTL_DMAS DMANSIRQ_DMAA DMANSIRQ_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANCONI_DMAA DMANSSAL_DMAA DMANSSAL_DMAA DMANSSAL_DMAA DMANSSAL_DMAA DMANSSTRL_DMAA DMANSSTRL_DMAA DMANSSTRL_DMAA DMANSSTRL_DMAA DMANSPTRL_DMAA DMANSPTRL_DMAA DMANSPTRL_DMAA DMANDSAL_DMAA DMANDS	413Eh 413Ch 413Eh 413Ah 413Ch 412Ch 412Eh	DMANSSEL DMA3 DMANSSEL DMA3 DMANSSEL DMA3 DMANSFEL DMA3 DMANSFEL DMA3 DMANSFEL DMA3 DMANSFEL DMA3 DMANSFEL DMA3 DMANSFEL DMA3 DMANSCOTTL DMA3 DMANSCOTTL DMA3 DMANDSCOTTL DMA3 DMANDSCOTTL DMA3 DMANDSEL DMA3	411Eh 411Dh 411Bh 411Ah 411Bh	DMANDSAL DMA2 DMANDSAL DMA2 DMANDSZH DMA2 DMANDSZH DMA2 DMANDSZH DMA2 DMANDFRH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANDCNTH DMA2 DMANBUF DMA2 DMANBUF DMA2 DMANBUF DMA2 DMANBUF DMA2 DMANSAL DMA1 DMANCOND DMA1 DMANCOND DMA1 DMANSSAL DMA1 DMANSSTRH DMA1 DMANDSZH DMA1
41FEh 41FDh 41FCh 41FBh 41 41FBh 41 41FBh 41 41FBh 41 41FBh 41 41 41 41 41 41 41 41 41 41 41 41 41	TMRSH MI TMRSL MI TMRSL MI TMRSH MI	410Eh 410DH 410CH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410BH 410CH 41CCH 41CCH 41CCH 41CCH 41CCH 41CCH 41CSH		418Eh 418Dh 418Ch 418Ch 418Bh 418Ah 418Ah 4186h 4186h 4185h 418Ah 418Ch 418Ah 418Ah 41ACh		419Eh 419Ch 419Sh 419Sh 419Sh 419Sh 419Sh 419Sh 419Sh 419Sh 419Sh 419Sh 419Sh 419Sh 418Sh 418Ch 418Bh 418Ch 418Sh	DMAnSIRQ_DMA6 DMAnAIRQ_DMA6 DMAnCOND_DMA6 DMAnCOND_DMA6 DMAnSAH_DMA6 DMAnSSAH_DMA6	417Eh 417Oh 417Ch 417Bh 417Bh 4178h 4177h 4177h 4177h 4177h 4173h 4173h 4173h 4171h 416Eh 416Eh 416Eh 416Bh 416Ah 416Bh 416Ah 416Bh 416Bh 416Ah 416Bh	DMANSTRL DMAS DMANSCATH DMAS DMANSCATH DMAS DMANSCATH DMAS DMANSCATH DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSAL DMAS DMANDSTRL DMAS DMANDPTRL DMAS DMANDPTRL DMAS DMANDPTRL DMAS DMANDCATH DMAS DMANDCATH DMAS DMANGCATH DMAS DMANSCAL DMAS DMANSSAL DMAS	415Eh 415Dh 415Bh 416Bh	DMANDCNTH_DMAS DMANDCNTL_DMAS DMANBLET_DMAS DMANBLET_DMAS DMANBLET_DMAS DMANBLET_DMAS DMANBLET_DMAS DMANBLET_DMAS DMANCONI_DMAS DMANCONI_DMAS DMANCSAL_DMAS DMANSSAL_DMAS DMANSSAL_DMAS DMANSSAL_DMAS DMANSSTRL_DMAS DMANSFIRL_DMAS DMANSFIRL_DMAS DMANSFIRL_DMAS DMANSFIRL_DMAS DMANSFIRL_DMAS DMANDSAL_DMAS	413Eh 413Ch 413Bh 413Ah 4138h 4137h 4136h 4137h 4133h 4132h 4133h 4132h 412Eh 412Eh 412Ch	DMANSAL DMAS DMANSSZH DMAS DMANSSZH DMAS DMANSSZH DMAS DMANSFTRU DMAS DMANSFTRU DMAS DMANSFTRU DMAS DMANSFTRU DMAS DMANSFTRU DMAS DMANSCNTL DMAS DMANDSAL DMAS DMANDFTRU DMAS	4116h 4110h 4110h 41118h 4108h 4108	DMANDSAL DMA2 DMANDSZH DMA2 DMANDSZH DMA2 DMANDSZH DMA2 DMANDSZH DMA2 DMANDDTHL DMA2 DMANDDTHL DMA2 DMANDDTHL DMA2 DMANDDTHL DMA2 DMANDDTHL DMA2 DMANDSH DMA2 DMANSH DMA1 DMANSH DMA1 DMANSSH DMA1 DMANSSTR DMA1 DMANSSTR DMA1 DMANSTR DMA1 DMANDSH DMA1 DMANDPTR DMA1 DMANDPTR DMA1

2. Setting the Destination

The DMA peripheral can store data into only one memory system in the microcontroller; SFR/GPR memory. As a result, there is not a corresponding set of destination memory select bits.

2.1 Configuring Destination Registers

To configure the DMA destination, the only step is to load the DMAnDSAL and DMAnDSAH registers. These registers specify the address of the data destination. Together, the two registers can hold up to a 16-bit address.

2.2 Loading Destination Registers

Loading the destination registers can be accomplished by using the set address routines supplied by MCC. They can be loaded individually by the system software, or both registers can be loaded together by equating the DMAnDSA register with a 16 constant or a variable containing the desired address.

DMAnSSA = &U4TXB; // destination USART 4 TX reg.

Note: The & prefix is used with the UxTXB label to specify the address of the SFR, rather than the SFR's contents.

3. Setting the Size of Transfer

A DMA transaction is the transfer of a single byte. A DMA message consists of one or more transactions. A complete DMA process consists of one or more messages. The source and destination size registers determine the size of the DMA message and the number of DMA messages in the DMA process. The smaller of the source/destination sizes determines the size of the DMA message and the larger value, divided by the smaller size, determines the number of messages in the DMA process.

The source size is loaded into the DMAnSSZ registers. The destination is loaded into the DMAnDSZ registers. Both registers are 16-bit and located such that a 16-bit assignment will load both registers correctly, allowing either individual loading or equating the variable to a 16-bit value of variable.

Note: The size of the source and destination are typically different. For examples, see Table 3-1.

Once a transfer has been completed;

- 1. The counter registers are decremented
- 2. The address registers are updated (post increment, post decrement, fixed)
- And the data transfers will continue until either or both of the DMA counters (DMAnSCNTL/H or DMAnDCNTL/H) roll over. When the counters roll over, they are reloaded with the value from the DMAnSSZL/H or DMAnDSZL/H registers and the event ends the current DMA message.

Note: If one of the size registers is programmed with 1, then only one transfer will occur for each trigger event. If the smallest size register is N, then N transactions will occur for each DMA trigger.

Table 3-1. Example Message Size

Operation	Example	SCNT	DCNT	Comments
Read from single SFR location to RAM	UART Receive Buffer	1	N	N equals the number of bytes desired in the destination buffer. N ≥ 1.
Write to single SFR location from RAM	UART Transmit Buffer	N	1	N equals the number of bytes desired in the source buffer. N ≥ 1.
Read from multiple SFR location	ADC Result registers	2	2*N	N equals the number of ADC results to be stored in memory. N ≥ 1.
Write to Multiple SFR registers	PWM Duty Cycle registers	2*N	2	N equals the number of PWM duty cycle values to be loaded from a memory table. N ≥ 1.

4. Selecting the Transfer Trigger

The next step in configuring the DMA peripheral is to select the transfer trigger event. The value loaded into the DMAnSIRQ register selects the hardware event that will trigger the DMA. Potential triggers can include CLCs, ADC conversions, communications peripherals, timers and even other DMA channels. Table 4-1 lists an example of all the possible DMA triggers for the PIC18F-Q43.

Once the DMAnSIRQ register is configured, the SIRQEN bit in the DMAnCON0 register must be set to enable the selected hardware trigger.

If a 0x00 is loaded into the DMAnSIRQ register, or the SIRQEN bit is cleared, then the only method for triggering a DMA transfer is to manually trigger a transfer by setting the DGO bit in the DMAnCON0 register.

Table 4-1. DMAnSIRQ Interrupt Sources

Table 1 in 2 in a month of month of the course		
DMAnSIRQ	DMA Start/Abort Trigger source	
0x0	-	
0x1	HLVD (High/Low-Voltage Detect)	
0x2	OSF (Oscillator Fail)	
0x3	CSW (Clock Switching)	
0x4	-	
0x5	CLC1 (Configurable Logic Cell)	
0x6	-	
0x7	IOC (Interrupt-on-Change)	
0x8	INT0	
0x9	ZCD (Zero-Cross Detection)	
0xA	AD (ADC Conversion Complete)	
0xB	ACT (ADC Auto-Conversion Trigger)	
0xC	CM1 (Comparator)	
0xD	SMT1 (Signal Measurement Timer)	
0xE	SMT1PRA	
0xF	SMT1PWA	
0x10	ADT	
0x11 - 0x13	-	
0x14	DMA1SCNT (Direct Memory Access)	
0x15	DMA1DCNT	
0x16	DMA1OR	
0x17	DMA1A	
0x18	SPI1RX (Serial Peripheral Interface)	
0x19	SPI1TX	
0x1A	SPI1	
0x1B	TMR2	
0x1C	TMR1	

Selecting the Transfer Trigger

continued	
DMAnSIRQ	DMA Start/Abort Trigger source
0x1D	TMR1G
0x1E	CCP1 (Capture/Compare/PWM)
0x1F	TMR0
0x20	U1RX
0x21	U1TX
0x22	U1E
0x23	U1
0x24 - 0x25	-
0x26	PWM1RINT
0x27	PWM1GINT
0x28	SPI2RX
0x29	SPI2TX
0x2A	SPI2
0x2B	-
0x2C	TMR3
0x2D	TMR3G
0x2E	PWM2RINT
0x2F	PWM2GINT
0x30	INT1
0x31	CLC2
0x32	CWG1 (Complementary Waveform Generator)
0x33	NCO1 (Numerically Controlled Oscillator)
0x34	DMA2SCNT
0x35	DMA2DCNT
0x36	DMA2OR
0x37	DMA2A
0x38	I2C1RX
0x39	I2C1TX
0x3A	I2C1
0x3B	I2C1E
0x3C	-
0x3D	CLC3
0x3E	PWM3RINT
0x3F	PWM3GINT
0x40	U2RX

Selecting the Transfer Trigger

continued	
DMAnSIRQ	DMA Start/Abort Trigger source
0x41	U2TX
0x42	U2E
0x43	U2
0x44	TMR5
0x45	TMR5G
0x46	CCP2
0x47	SCAN
0x48	U3RX
0x49	U3TX
0x4A	U3E
0x4B	U3
0x4C	-
0x4D	CLC4
0x4E - 0x4F	-
0x50	INT2
0x51	CLC5
0x52	CWG2
0x53	NCO2
0x54	DMA3SCNT
0x55	DMA3DCNT
0x56	DMA3OR
0x57	DMA3A
0x58	CCP3
0x59	CLC6
0x5A	CWG3
0x5B	TMR4
0x5C	DMA4SCNT
0x5D	DMA4DCNT
0x5E	DMA4OR
0x5F	DMA4A
0x60	U4RX
0x61	U4TX
0x62	U4E
0x63	U4
0x64	DMA5SCNT

continued	
DMAnSIRQ	DMA Start/Abort Trigger source
0x65	DMA5DCNT
0x66	DMA5OR
0x67	DMA5A
0x68	U5RX
0x69	U5TX
0x6A	U5E
0x6B	U5
0x6C	DMA6SCNT
0x6D	DMA6DCNT
0x6E	DMA6OR
0x6F	DMA6A
0x70	-
0x71	CLC7
0x72	CM2
0x73	NCO3
0x74 - 0x77	-
0x78	NVM
0x79	CLC8
0x7A	CRC
0x7B	TMR6
0x7C - 0x8F	-
0x90	PWM1 S1P1 (PWM1 Parameter 1 of Slice 1)
0x91	PWM1 S1P2 (PWM1 Parameter 2 of Slice 1)
0x92	PWM2 S1P1 (PWM2 Parameter 1 of Slice 1)
0x93	PWM2 S1P2 (PWM2 Parameter 2 of Slice 1)
0x94	PWM3 S1P1 (PWM3 Parameter 1 of Slice 1)
0x95	PWM3 S1P2 (PWM3 Parameter 2 of Slice 1)

5. Selecting an Abort Trigger

In addition to the trigger select, there is an abort select that can immediately terminate a DMA in response to a hardware trigger. DMAnAIRQ is configured with a selected hardware abort trigger and when the abort is detected, the DGO bit and the SIRQEN bits are both cleared. This happens immediately and any byte in transit is not stored to the designation. The options for an abort select signal is typically the same as the selections for a trigger signal. See Table 4-1 for abort event options.



Important: In addition to selecting an abort event, the AIRQEN bit must also be set to enable the abort event. If cleared, no trigger will abort a DMA message.

6. Configuring DMA Automation

Now that the DMA is mostly configured, options for the automation of the DMA must be selected. These include Post Increment/Decrement/Fixed and the termination event for the DMA transfers.

The next step in the configuration process is to set the Automation mode for both the source and destination. Both can be individually configured for post increment, post decrement or fixed operation. The source is configured using the SMODE bits and the destination is configured using the DMODE bits. Both sets of bits are in the DMAnCON1 register. See Tables 6-1 and 6-2 for selecting the mode.

Table 6-1. Source Operating Mode

SMODE1	SMODE0	Mode
1	1	Reserved
1	0	Post Decrement
0	1	Post Increment
0	0	Fixed (no Change)

Table 6-2. Destination Operating Mode

DMODE1	DMODE0	Mode
1	1	Reserved
1	0	Post Decrement
0	1	Post Increment
0	0	Fixed (no Change)

To select the source counter roll over to terminate the DMA process, the SSTP bit in the DMAnCON1 register is set. To select the destination counter roll over, the DSTP bit in the DMAnCON1 register must be set. If neither bit is set, then the DMA process can only be terminated by clearing the DGO bit in the DMAnCON0 register.

Note:

- 1. If a post decrement operating mode is chosen, then the associated Source/Destination Address register must be loaded with the last address of the variable space/peripheral registers, rather than the first.
- 2. If a fixed operating mode is chosen and the associated size register is set to 0x01, then a single transfer will terminate the DMA message. If a fixed operating mode is chosen and the associated size register is set to N (N > 0x01), then a N transfers will terminate the DMA message.

The second automation selection concerns which of the transaction counter roll over events will terminate the DMA operation. Both the source and destination have been configured for size. This selection determines which, if either, roll over will end the DMA process.

For example, if a USART is configured to receive and the DMA is configured to capture the received data and store it into a buffer, then the terminating roll over is typically the buffer's counter. When that happens the DGO bit, the SIRQEN bit and the AIRWEN bit are all cleared. The hardware trigger enable SIRQEN is also cleared, preventing additional triggers by a hardware source.

7. Enabling Interrupts

The DMA peripheral can generate four interrupts; Source Count, Destination Count, Abort and Overrun. The source counter interrupt generates a system interrupt when the source counter reloads. The destination counter interrupt does the same thing when the destination counter reloads. Together, these two interrupts convey the completion of a DMA message and the full DMA process. The determination of which interrupt signifies which event is dependent upon which counter is reloaded from the larger size value.

The abort interrupt is generated whenever a hardware abort signal is received by the DMA peripheral. The overrun interrupt is generated whenever the DMA peripheral receives a second trigger event while still processing the first DMA.

These interrupts not only provide feedback to the controlling software, they also provide CIP signals that can be routed to other peripherals. An example would be using the DMA to reconfigure the ADC and then using the destination counter reload interrupt to trigger an ADC conversion.

8. Setting Transfer Priority and Enabling Transfers

PIC18F microcontrollers, which contain the DMA peripheral, also contain a System Arbiter function. The System Arbiter controls the relative priority of the DMA peripherals, the interrupts and normal code execution. It determines which function can suspend the other operations to take control of the address and data buses.

For example, the interrupts typically have the highest priority, followed by main code operation and then the DMA peripherals. This means that main code has control of the buses until an interrupt occurs. Then the interrupt has control, until the interrupt completes. Because the DMA has such a low priority, it can only take control of the buses when the main code is executing a branch or jump and the buses are idle. However, using the arbiter, it is possible to increase the priority of the DMA, allowing it to interrupt both the main code and the interrupt functions and take over control of the buses, until it completes its message.

In fact, using the arbiter, it is even possible to put the interrupt at a lower priority than the main code. However, as this would effectively disable the interrupt system, there are provisions within the arbiter that prevent this specific scenario.

Note: Because each device has a different number of DMA peripherals and different modes of interrupt operation, it is impractical to specify all the possible priority combinations using the System Arbiter in this document. Therefore, the reader is referred to the **System Arbiter** chapter in the desired device data sheet for the recommended configuration and operation of the System Arbiter.

To begin operation for a given DMA peripheral, the programmer will need to lock the peripheral using the PRLOCK sequence and set the EN bit in the appropriate DMAnCON0 register to enable DMA operation. If the transfer is to be initiated by hardware, the DMA peripheral will sit dormant until the hardware trigger is detected. If the DMA peripheral is configured for a software trigger, then set the DGO bit in the DMAnCON0 register to initiate the first DMA transfer. See Examples 8-1 and 8-2 for locking and unlocking sequences.

Example 8-1. Priority Lock Sequence

```
; Disable interrupts
BCF INTCONO, GIE
; Bank to PRLOCK register
BANKSEL PRLOCK
MOVIW
; Required sequence, next 4 instructions
MOVWF PRIOCK
      AAh
W.TVOM
MOVWF
       PRLOCK
; Set PRLOCKED bit to grant memory access to peripherals
BSF
    PRLOCK, 0
; Enable Interrupts
    INTCON0, GIE
```

Example 8-2. Priority Unlock Sequence

```
; Disable interrupts
BCF INTCONO,GIE

; Bank to PRLOCK register
BANKSEL PRLOCK
MOVLW 55h

; Required sequence, next 4 instructions
MOVWF PRLOCK
MOVLW AAh
MOVWF PRLOCK
; Clear PRLOCKED bit to allow changing priority settings
BCF PRLOCK, 0
```

; Enable Interrupts
BSF INTCONO,GIE

Note:

- 1. The PRLOCK sequence is a requirement to start the DMA peripheral. This is an added layer of security to avoid priority mismatch errors.
- 2. Both hardware and software triggers can be used in the same DMA operation. This allows the trigger of DMA from hardware, while also initiating the first DMA message from software.

9. Monitor Transfer Status

The DMA peripheral has two Status bits, the DGO and XIP bits in the DMAnCON0 register. The DGO bit indicates that the DMA peripheral has been triggered and is currently in the process of transferring data. The XIP bit indicates that a transfer is occurring and the data being transferred is currently stored in the DMAxBUF register. This indicates that the memory read has occurred, but the memory write is pending.

In addition, the counter registers, DMAnSCNT and DMAnDCNT can be monitored to gauge the progress of the DMA operation. Each time the smaller counter register is reloaded, it will indicate the completion of a DMA message, and the reload the larger counter will indicate the completion of the DMA process. To gauge the overall progress of the DMA, the DMA address registers (DMAnSPTR and DMAnDPTR) can also be read to determine the last address read from and written to.

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ISBN: 978-1-5224-5602-5

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