Non-Linear Analog Circuit Test and Diagnosis under Process Variation using V-Transform Coefficients

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***Abstract*—Parametric fault testing of non-linear analog circuits based on a new mathematical transform is presented. The V-Transform acts on the polynomial expansion of the circuit's function. Its main properties are: 1) to make the polynomial coefficients monotonic, 2) to reduce masking of parametric faults due to process variation, and 3) to increase the sensitivity of polynomial coefficients to the circuit parameter variation, thus enhancing diagnostic resolution. We show that the sensitivity of V-Transform Coefficients (VTC) with respect to circuit parameter variation is up to 3 to 5 times greater than the sensitivity of polynomial coefficients. Fault diagnosis of parametric faults under process variation using VTC is then presented. We also propose a scheme to distinguish between circuit specifications failures due to process variation versus manufacturing defects which manifest as parametric faults. To validate our approach, we apply the test and diagnosis procedures to a benchmark fifth order elliptic filter. We use SPICE program for fault injection, with about 50,000 Monte Carlo simulation runs to demonstrate fault detection-diagnosis under process variation. The test scheme uncovers 95% of all injected single parametric faults whose sizes deviate 5% from the nominal values of circuit components corrected for process variation, while the procedure successfully diagnosed all component faults under $\pm 3\sigma$ process variation with 88% confidence level.**

I. Introduction

Non-linear circuit testing has been well studied and different methods have been proposed for finding parametric faults [1], [2], [3], [4], [5], [6], [7], [8]. Prominent among them in the industry is the I_{DDQ} based testing where current from the supply rail is monitored and sizable deviation from its quiescent value is reported. However this requires augmentation of the CUT. For example, in the simplest case a regulator supplying power to any sizable circuit has to be augmented with a current sensing resistor and an ADC (for digital output) and then there is subsequent analysis to be performed on sensed current. Further I_{DDQ} is suitable only for catastrophic faults as the current drawn from the supply is distinguishable only when there is some "big enough" fault so as to change the current drawn from the supply from its quiescent value to a region where it is distinguishable. For example with resistor R_2 being open in Figure 1, the current drawn from supply can change by 50% of its quiescent value. Such faults can typically be found by monitoring I_{DDQ} using a current sensor. However parametric deviations say lesser than 10% from its nominal value cannot be observed using this scheme, specially so in the deep submicron era where the leakage currents can be comparable with defect induced current [9]. The other approach for testing parametric faults that can be found in literature [10], [11], [12], [13], [14] is based on the use of neural networks. Neural network based approaches propose the use of circuit observer blocks to track the output for a set of input signals which is used for training the neurons. The trained set of neurons is then used to estimate variations in the output for a standard input stimulus. This method, however, suffers from large amounts of training required and the consequent increase in test application time that the scheme is prohibitive for even medium sized analog circuits at production. More recently, the use of Volterra series coefficients was proposed to estimate non-linear characteristics of the system. These coefficients are then used for testing the circuit with a pseudo random input stimulus [15], [16]. This method however suffers from the high computational requirement of estimation of Volterra series coeffcients for every circuit at production which can increase the test cost significantly. It is therefore interesting to develop a method to detect parametric faults with little circuit augmentation while keeping the test access mechanism simple and the test application time to a minimum.

To address the issue of parametric deviation, we would typically need more observables to have an idea about the parametric drift in circuit parameters. This would mean an increase in complexity of the sensing circuit. However, we would also want only little augmentation to tap any of the internal circuit nodes or currents. To overcome these seemingly contrasting requirements the method intended should have some way of "seeing through" the circuit with only the outputs and inputs at its disposal. References [17], [18] have accomplished this sort of a strategy for linear circuits in a different context as described next.

Savir and Guo describe a method [17] based on transfer function of a circuit under test (CUT). The transfer function,

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$H(s)$, of the CUT is expressed as:

$$H(s) = \frac{\sum_{i=0}^{M} a_i s^i}{\sum_{i=0}^{N} b_i s^i} \qquad (M < N) \tag{1}$$

Here, a_i and b_i are referred to as transfer function coefficients (TFCs). The CUT is subjected to frequency rich input signals and the output at these frequencies is observed. With these input-output pairs they estimate the TFCs of CUT. These coefficients are now compared with the ideal circuit TFCs, which are known a priori. The CUT is classified faulty if any of the estimated coefficients are beyond the tolerable range. This method necessarily needs the CUT to be linear, as transfer functions are possible only for LTI systems.

To extend the above idea to more general non-linear circuits we adopted a strategy in [19] where we expand the function of the circuit as a polynomial by the Taylor's series expansion about the input voltage mangitude v_{in} at a given frequency, as follows:

$$v_{out} = f(v_{in}) = f(0) + \frac{f'(0)}{1!}v_{in} + \frac{f''(0)}{2!}v_{in}^2 + \frac{f'''(0)}{3!}v_{in}^3 + \cdots + \frac{f^{(n)}(0)}{n!}v_{in}^n + \cdots \tag{2}$$

where $f(v_{in})$ is a real function of v_{in}. Ignoring the higher order terms in (2), we can expand v_{out} up to the n^{th} power of v_{in}, which gives us the approximation in (3):

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + \cdots + a_n v_{in}^n \tag{3}$$

where $a_0, a_1, a_2, \ldots, a_n$ are all real-valued functions of circuit parameters $p_k,\ \forall k$. Further assume that normal parameter variations (normal drift) in a good circuit are within a fraction α of their nominal value, where $\alpha << 1$. This means that every parameter p_i is allowed to vary within the range $p_{k,nom}(1-\alpha) < p_k < p_{k,nom}(1+\alpha)$, $\forall k$, where $p_{k,nom}$ is the nominal value of parameter p_k. Whenever one or more of the coefficient values slip outside its individual hypercube we get a different set of coefficients that reflects a detectable fault. Therefore, equation (4) describes a hypercube for all parameters that correspond to either good machine values or undetectable parameter faults [2], [8], [17]:

$$a_{i,\min} < a_i < a_{i,\max} \quad \forall a_i,\ 0 \le i \le n \tag{4}$$

In the latter portion of this paper we address an important problem that has kept analog circuit test cost high [20], namely, distinguishing between faults induced due to process variation. For example, we would like to distinguish random drifts in t_{ox}, W, L, and doping densities of devices in an integrated circuits from those resulting from manufacturing defect induced (parametric) faults (e.g., Lithographic errors, etching errors, etc.) that lead to a substantial deviation of a circuit from its nominal behavior but are not large enough to render the circuit dysfunctional. We quantify an error distance measure between faults induced due to process variation with those induced due to manufacturing defects. We can then estimate the probabilities of a detected fault being caused by process variation or by a manufacturing defect. We make this estimation based on maximizing *a posteriori* probabilities of the two kinds of errors conditioned on the event that a fault is detected.

This paper is organized as follows. Section II we state previously published results [21] on the polynomial expansion of function $f(v_{in})$ and notions of detectable fault sizes. Section III outlines V-Transform and the resulting sensitivity improvement. In Section IV we describe the problem at hand and discuss the proposed solution with an example. In Section V we generalize the test solution to an arbitrarily large circuit. Section VI establishes, 1) a method to distinguish between process variation induced faults and those induced due to manufacturing defects and 2) identify the fault site if it is of the latter kind. Section VII presents the simulation results for a standard elliptic filter. We conclude in Section VIII.

II. Background

The coefficients a_i, $\forall 0 \le i \le n$, are in general non-linear functions of circuit parameters $p_k,\ \forall k$. The rationale in using these coefficients as metrics in classifying CUT as faulty or fault free is based on the premise of dependence of coefficients on circuit parameters.

Theorem 1. If coefficient a_i is a monotonic function of all parameters, then a_i takes its limit (maximum and minimum) values when at least one or more of the parameters are at the boundaries of their individual hypercube.

Lemma 1. If coefficient a_i is a non-monotonic function of one or more circuit parameters p_i, then a_i can take its limit values anywhere inside the hypercube enclosing the parameters.

By Theorem 1 and Lemma 1 it is clear that by exhaustively searching the space in the hypercube of each parameter we can get the maximum and minimum values of the polynomial coefficient. Typically this can be formulated as a non-linear optimization problem to find the maximum and minimum values of coefficient with constraints on parameters allowing only a normal drift.

Theorem 2. In polynomial expansion of Non-Linear Analog circuit there exists at least one coefficient that is a monotonic function of all the circuit parameters.

In conclusion, from Lemma 1 and Theorem 2, circuit parameter deviations have a bearing on coefficients and the monotonically varying coefficients can be used to detect parametric faults of the circuit parameters [19].

Definition: A minimum size detectable fault (MSDF), ρ, for a parameter is defined as the minimum fractional deviation of the circuit parameter from its nominal value for it to be detectable with all other parameters held at their nominal values. The fractional deviation can be positive or negative and is named upside-MSDF (UMSDF) or downside-MSDF (DMSDF) accordingly.

If ψ is the set of all coefficient values spanned by the parameters while varying within their normal drifts, i.e.,

$$\psi = \{v_0, v_1, \cdots, v_n \,|\, v_0 \in A_0, v_1 \in A_1, \cdots, v_n \in A_n\}$$
$$\forall_k \quad p_{k,nom}(1-\alpha) < p_k < p_{k,nom}(1+\alpha)$$

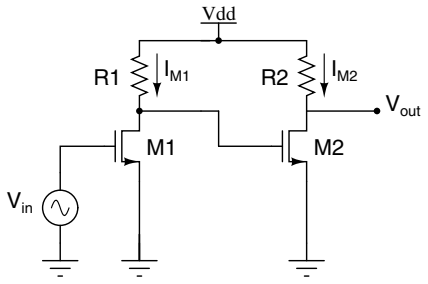

Fig. 1. Cascaded amplifier.

then by definitions of MSDF, ψ includes all possible values of coefficients that are not detectable. Any parametric fault inducing coefficient value outside the set ψ will result in a detectable fault.

III. The V-Transform

We define V-Transform coefficients as follows: if $C_1, C_2 \cdots C_n$ are polynomial coefficients of CUT then their V-Transform coefficients, $V_{C_1}, V_{C_2} \cdots V_{C_n}$, are

$$V_{C_i} = e^{\gamma C_i^{'}} \ \forall \ 0 \leq i \leq n \tag{5}$$

where C_i' are the modified polynomial coefficients defined indirectly as follows

$$\frac{dC_i'}{dp_j} = \left| \frac{dC_i}{dp_j} \right| \ \forall \ 0 \leq i \leq n \tag{6}$$

The modification C_i' according to (6) ensures that the modified polynomial coefficients are monotonic with the polynomial coefficients. Further, the V-Transform coefficients (VTC) are exponential functions of the modified polynomial coefficients and γ is a sensitivity parameter chosen according to the desired sensitivity. The gain in sensitivity of V-Transform coefficients to circuit parameters over the sensitivity of ordinary polynomial coefficients is given by

$$\frac{S_{p_i}^{V_{C_i}}}{S_{p_i}^{C_i}} = \frac{\left|\frac{dC_i}{dp_i}\right| \gamma e^{\gamma C_i'} \bullet \frac{p_i}{e^{\gamma C_i'}}}{\frac{dC_i}{dp_i} \bullet \frac{p_i}{C_i}} = \gamma C_i \tag{7}$$

Choices of $\gamma = 3$, for instance, results in a 3 times more sensitive coefficient to circuit parameters.

IV. Problem and Approach

We shall first illustrate with an example the calculation of limits of the polynomial coefficients for a simple circuit using MOS transistors. We shall follow this up with MSDF values for the circuit parameters.

Example 1. Two stage amplifier: Consider the cascaded amplifier shown in Figure 1. The output voltage V_{out} in terms of input voltage results in a fourth degree polynomial:

$$V_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + a_4 v_{in}^4 \tag{8}$$

where constants a_0, a_1, a_2, a_3 are defined symbolically in (9) for transistors M1 and M2 operating in the saturation region. Nominal values of $V_{DD} = 1.2V$, $V_T = 400mV$, $\left(\frac{W}{L}\right)_1 = \frac{1}{2}\left(\frac{W}{L}\right)_2 = 20$, and $K = 100\mu A/V^2$ are used for this example.

$$\begin{aligned}
a_0 &= V_{DD} - R_2 K \left(\tfrac{W}{L}\right)_2 \left\{ \begin{array}{l} (V_{DD}-V_T)^2 + \\ R_1^2 K^2 \left(\tfrac{W}{L}\right)_1^2 V_T^4 - \\ 2(V_{DD}-V_T) R_1 \left(\tfrac{W}{L}\right)_1 V_T^2 \end{array} \right\} \\
a_1 &= R_2 K \left(\tfrac{W}{L}\right)_2 \left\{ \begin{array}{l} 4R_1^2 K^2 \left(\tfrac{W}{L}\right)_1^2 V_T^3 \\ +2(V_{DD}-V_T) R_1 K \left(\tfrac{W}{L}\right)_1 V_T \end{array} \right\} \\
a_2 &= R_2 K \left(\tfrac{W}{L}\right)_2 \left\{ \begin{array}{l} 2(V_{DD}-V_T) R_1 K \left(\tfrac{W}{L}\right)_1 \\ -6R_1^2 K^2 \left(\tfrac{W}{L}\right)_1^2 V_T^2 \end{array} \right\} \\
a_3 &= 4V_T K^3 \left(\tfrac{W}{L}\right)_1^2 \left(\tfrac{W}{L}\right)_2^2 R_1^2 R_2 \\
a_4 &= -K^3 \left(\tfrac{W}{L}\right)_1^2 \left(\tfrac{W}{L}\right)_2^2 R_1^2 R_2
\end{aligned} \tag{9}$$

To find the limit values of the coefficient a_0 we assume that parameters R_1 and R_2 deviate by fractions x and y from their nominal values, respectively. To maximize a_0 we have the objective function (10) subject to constraints (11) through (15). Note that here we have set out to find MSDF of R_1. Similar approach can be used to find the MSDF of R_2.

$$1.2 - R_{2,nom}(1+y) \left\{ \begin{array}{l} 2.56 \times 10^{-3} + \\ 1.024 \ \times \ 10^{-7} R_{1,nom}^2 (1+x)^2 \\ -5.12 \ \times \ 10^{-4} R_{1,nom}(1+x) \end{array} \right\} \tag{10}$$

$$\begin{aligned}
&4.096 \ \times \ 10^{-9} R_{1,nom}^2 (1+x)^2 R_{2,nom} \ (1+y) \\
&+5.12 \ \times \ 10^{-6} R_{1,nom}(1+x) R_{2,nom}(1+y) \\
&\quad = 4.096 \ \times \ 10^{-9} R_{1,nom}^2 (1+\rho)^2 R_{2,nom} \\
&\quad + 5.12 \quad \times \quad 10^{-6} R_{1,nom}(1+\rho) R_{2,nom}
\end{aligned} \tag{11}$$

$$\begin{aligned}
&1.28 \quad \times \quad 10^{-5} R_{1,nom}(1+x) R_{2,nom}(1+y) \\
&-1.536 \times 10^{-8} R_{1,nom}^2 (1+x)^2 R_{2,nom} \ (1+y) \\
&\quad = 1.28 \ \times \ 10^{-5} R_{1,nom}(1+\rho) R_{2,nom} \\
&\quad - 1.536 \ \times \ 10^{-8} R_{1,nom}^2 (1+\rho)^2 R_{2,nom}
\end{aligned} \tag{12}$$

$$\begin{aligned}
&2.56 \times 10^{-8} R_{1,nom}^2 (1+x)^2 R_{2,nom}(1+y) \\
&\quad = 2.56 \times 10^{-8} R_{1,nom}^2 (1+\rho)^2 R_{2,nom}
\end{aligned} \tag{13}$$

$$\begin{aligned}
&1.6 \times 10^{-8} R_{1,nom}^2 (1+x)^2 R_{2,nom}(1+y) \\
&\quad = 1.6 \times 10^{-8} R_{1,nom}^2 (1+\rho)^2 R_{2,nom}
\end{aligned} \tag{14}$$

$$-\alpha \leq x, y \leq \alpha \tag{15}$$

The extreme values for x and y are obained by solving the set of equations (10-15). We get $x = -\alpha$ and $y = -\alpha$ and this gives the MSDF for R_1, as

$$\rho = (1-\alpha)^{1.5} - 1 \approx 1.5\alpha - 0.375\alpha^2 \tag{16}$$

Table I gives the MSDF for R_1 and R_2 based on the above calculation.

TABLE I
MSDF FOR CASCADED AMPLIFIER OF FIGURE 1 WITH $\alpha = 0.05$.

Circuit parameter	%upside MSDF	%downside MSDF
Resistor R_1	10.3	7.4
Resistor R_2	12.3	8.5

V. GENERALIZATION

The computation of the previous section is too complex for arbitrarily large circuits. Such circuits are handled by first obtaining a nominal numeric polynomial expansion for them. This is done by sweeping the input voltage across all possible values and noting the corresponding output voltages. The output voltage is plotted against the input voltage. A polynomial is fitted to this curve and the coefficients of this polynomial are taken to be the nominal coefficients for the desired polynomial. A V-Transform curve is now obtained based on the polynomial curve using the transformation in equation (5). The circuit is simulated for different drifts in the parameter values at equally spaced points from inside the hypercube enclosing each circuit parameter, spaced ϵ apart. Polynomial coefficients and hence V-Transform coefficients are obtained for each of these simulations. The maximum and minimum values of coefficient in this search are taken as the limiting values for that coefficient. Once the limiting values for all coefficients have been determined the CUT is subjected to a DC sweep at the input and the output response is curve-fitted using a polynomial of the same order as that used for the fault free circuit. The V-Transform coefficients for CUT are now obtained. If there are any coefficients that lay outside the limiting values of the corresponding coefficients of the fault free circuit, we conclude that CUT is faulty. The converse need not be true as there could be other specifications, the circuit needs to meet, which are not captured by polynomial based test. Flowchart I in Figure 2 summarizes the process of numerically finding the V-transform coefficients and their bounds. Flowchart II in Figure 2 outlines a procedure to test CUT using the V-Transform coefficients. The bounds on coefficients of fault free circuit are found a priori as shown in Flowchart I of Figure 2.

VI. FAULT DIAGNOSIS

Fault diagnosis involves the location of likely fault sites in a CUT given that the CUT has failed an applied test giving a particular response. We use V-transform coefficients (VTC) to characterize the response of the circuit at different frequencies (about 4 or 5 frequencies are sufficient for most circuits with less than 100 circuit elements), by obtaining its input-output response over the entire input range. Process variation induces a fault-free variation of say σ, about the mean value of every VTC. Any value beyond σ from the mean μ of VTC indicates a circuit failure. Assuming a normal distribution for circuit parameter variation, we can find the probability distribution of the coefficients by Monte-Carlo simulation for process variation of all circuit parameters. Once the Monte-Carlo distributions for the coefficients of fault free circuit are

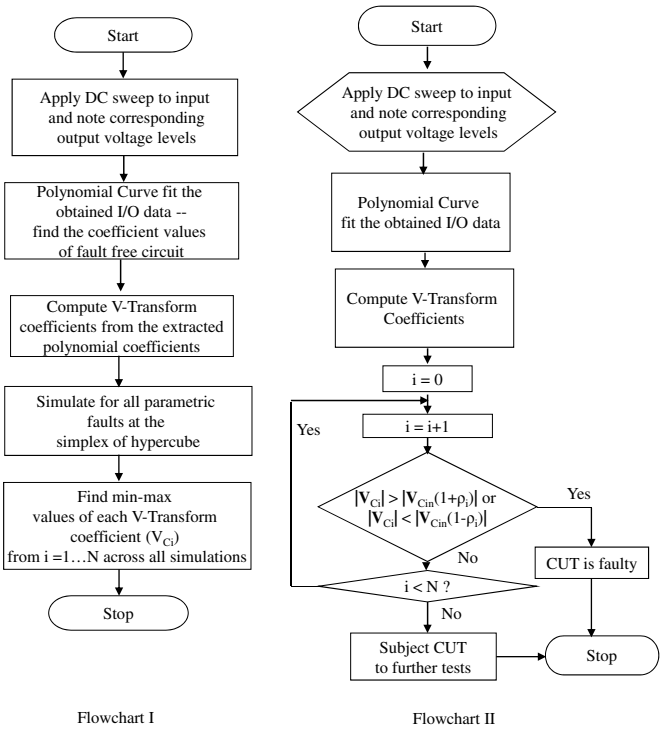

Fig. 2. Fault simulation process and bounding of coefficients (Flowchart I), and complete test procedure (Flowchart II).

obtained we can inject desired sizes of parametric faults (those that are induced due to manufacturing defects) and obtain the new probability distribution of faulty circuit under process variation.

As an illustration, Figure 3 shows the probability density distributions obtained with (broken line) and without (solid line) parametric fault. There are three distinct regions in the probability space of any coefficient C_k. Region R is the fault-free space because coefficients at all frequencies are within the desired limits. Region 1 where dominant mechanism of faults are due to PV of circuit parameters and Region 2 where dominant mechanism of faults is due to manufacturing defects (also called parametric fault). The cross-over point of these two distributions gives the equiprobable region of faults, where we can have faults due to either of the mechanism with the same likelihood. We denote this point on the coefficient axis as $\mathrm{C_{th}}$. Measuring the value of coefficient C of CUT, we can now determine the likelihood of the nature of fault mechanism. That is, $\mathrm{C} \in [\mu, \mathrm{C_{th}}] \implies$ failures due to PV are more in number and $\mathrm{C} \in [\mathrm{C_{th}}, \mu'] \implies$ failures due to parametric faults are more in number. The confidence of this distinction is given by the relative magnitudes of the two probability density function G_1 and G_2 at the point C on coefficient axis. Once we know, that the fault mechanism is due to a manufacturing defect, we can predict the fault site based on knowledge of the sensitivity of the coefficient to various circuit parameters at different frequencies [22], [23]. A fault dictionary is maintained for faults against circuit parameters at different frequencies. On measuring a parametric fault, the most likely fault site is deduced by intersection of fault sites that can contribute to

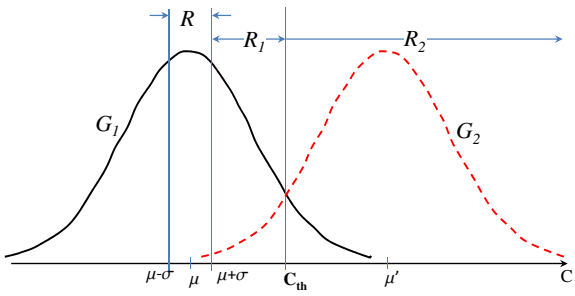

Fig. 3. Probability distribution of polynomial coefficient C under a parametric fault (broken line) as opposed to that with only process variation (solid line).

this fault at most of frequencies. The confidence level (P) this deduction is given by:

$$P = 1 - \prod_{i=1}^{i=N} (1 - P_i) \quad (1$$

where N is the number of frequencies (including DC) which the circuit is diagnosed and P_i is the confidence fault diagnosis at i^{th} frequency.

VII. Simulation Results

We simulated an elliptic filter shown in Figure 4 for Transform coefficient based test. The circuit parameter values are as in the benchmark circuit maintained by Stroud et al. [24]. Our Monte-Carlo simulation included 50,000 circuit instances, with process variations sampled as zero mean and standard deviation = ±10% of nominal circuit component value. This was repeated for different injected parametric faults to obtain distribution of the coefficients under both parametric faults and process variation (PV) of circuit components. We used parametric faults of sizes α = 5% from their nominal value to find min-max values of coefficients. Figure 5 shows the computed response and the estimated polynomial obtained by curve fitting:

$$\begin{aligned} v_{out} = {} & 4.5341 - 3.498 v_{in} - 2.5487 v_{in}^2 \\ & + 2.1309 v_{in}^3 - 0.50514 v_{in}^4 + 0.039463 v_{in}^5 \end{aligned} \quad (18)$$

The combinations of parameter values leading to limits on the coefficients are as shown in Tables II and III. Some of the circuit parameters are not shown in the table because they do not appear in any of the coefficients and are kept at their

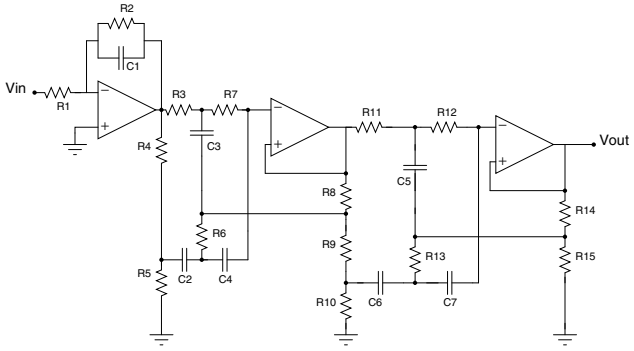

Fig. 4. Elliptic filter.

TABLE II
Parameter combinations leading to maximum values of V-Transform coefficients with α = 0.05.

Circuit Parameter (Ω)	V_{c_0}	V_{c_1}	V_{c_2}	V_{c_3}	V_{c_4}	V_{c_5}
R_1 = 19.6k	18.6k	20.5k	20.5k	20.5k	18.6k	18.6k
R_2 = 196k	186k	205k	186k	186k	186k	205k
R_3 = 147k	139k	154k	154k	154k	139k	154k
R_4 = 1k	950	1010	1010	1010	1010	1010
R_5 = 71.5	70	80	80	70	80	70
R_6 = 37.4k	37.4k	37.4k	37.4k	37.4k	37.4k	37.4k
R_7 = 154k	161k	161k	146k	161k	146k	146k
R_{11} = 110k	115k	115k	104k	115k	104k	104k
R_{12} = 110k	104k	115k	104k	104k	104k	104k

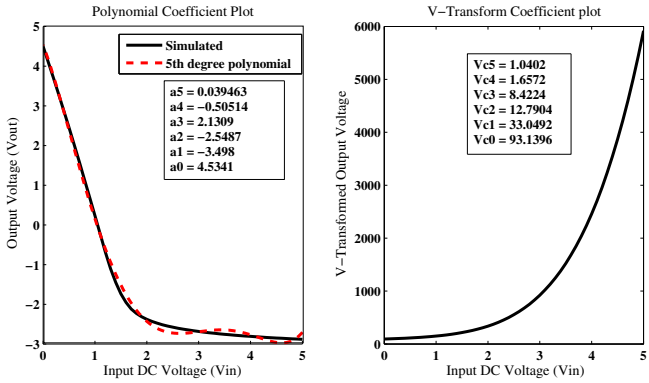

Fig. 5. DC response of elliptic filter with curve fitting polynomial and V-Transform plot.

nominal values. Further, results on pass/fail detectability of few injected faults are tabulated in Table IV. In the cases where coefficient deviation lies in the region R_1 for a coefficient C_k, the fault is attributed to PV as opposed to parametric fault. The same procedure is repeated for VTC and the number of cases in which the fault is diagnosed to be in the region R_1 and incorrectly attributed to PV is reduced. This is due to he enhanced sensitivity of V-transform coefficients to circuit parameters. Table V shows the diagnosed results of a few injected faults using sensitivity of V-transform coefficients to circuit parameters as described in Section VI.

VIII. Conclusion

A new approach for test and diagnosis of non-linear circuits based on a transformation of polynomial expansion of the circuit is demonstrated. The V-Transform renders the polynomial coefficients monotonicity and enhances their sensitivity. The

TABLE III
Parameter combinations leading to minimum values of V-Transform coefficients with α = 0.05.

Circuit Parameter (Ω)	V_{c_0}	V_{c_1}	V_{c_2}	V_{c_3}	V_{c_4}	V_{c_5}
R_1 = 19.6k	20.5k	18.6k	18.6k	20.5k	20.5k	20.5k
R_2 = 196k	205k	186k	205k	205k	205k	186k
R_3 = 147k	150k	139k	139k	146k	154k	139k
R_4 = 1k	1010	950	950	950	950	950
R_5 = 71.5	80	70	70	80	70	80
R_6 = 37.4k	39.2k	39.2k	39.2k	39.2k	35.5k	39.2k
R_7 = 154k	146k	146k	161k	146k	161k	161k
R_{11} = 110k	104k	104k	115k	104k	115k	115k
R_{12} = 110k	115k	104k	115k	115k	115k	115k

TABLE IV
RESULTS FOR SOME INJECTED FAULTS.

Circuit Parameter	Out of bound polynomial coefficient	Fault detected?	Out of bound V-Transform coefficient	Fault detected?
R_1 down 5%	$a_3,\ a_4$	Yes	$V_{c_0} - V_{c_4}$	Yes
R_2 down 10%	a_2	Yes	$V_{c_2},\ V_{c_5}$	Yes
R_3 up 5%	a_3	Yes	$V_{c_1},\ V_{c_2},\ V_{c_3}$	Yes
R_4 down 10%	a_0	Yes	$V_{c_0} - V_{c_4}$	Yes
R_5 up 10%	a_4	Yes	$V_{c_0},\ V_{c_4}$	Yes
R_7 up 5%	None	PV	$V_{c_1},\ V_{c_2}$	Yes
R_{11} up 5%	None	PV	$V_{c_4},\ V_{c_5}$	Yes
R_{12} down 5%	None	PV	$V_{c_4},\ V_{c_5}$	Yes

TABLE V
PARAMETRIC FAULT DIAGNOSIS WITH CONFIDENCE LEVELS OF $\approx 88\%$

Injected fault	Diagnosed fault sites					Deduced fault
	DC	100Hz	900Hz	1000Hz	1100Hz	
R_1 dn 15%	R_1 R_4	R_1	R_1, R_2	R_1, R_2 C_1	R_1 C_1	R_1
R_2 dn 10%	R_2	R_2 C_1	R_2, R_3 C_1	R_2, R_3	R_2 C_1	R_2
R_3 up 5%	R_1 R_3	R_3 C_3	R_3, R_4 C_3	R_3	R_3, C_3 C_3	R_3
R_4 dn 20%	R_1 R_4	R_1 R_4	R_2, R_4 C_1	R_1, R_2 R_4	R_1, R_2 R_4	R_4
R_5 up 15%	R_5	R_5 C_2	R_4, R_5	R_4, R_5 C_2	R_5, R_6 C_3	R_5
R_7 dn 10%	R_3 R_7	R_7 C_3	R_3, R_7	R_3, R_6 R_7	R_3, R_7 C_3	R_7

minimum sizes of detectable faults in some of the circuit parameters are as low as 5% which implies that impressive fault coverage can be achieved with VTC. The use of VTC shows a reduction in masking of parametric faults due to process variation. The method is then extended to sensitivity based fault diagnosis by evaluating VTC at different frequencies. Our future work will attempt to reduce the "false alarms" in fault detection when there is no manufacturing defect but just process variation.

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