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Four-quadrant analogue multiplier using operational amplifier

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A method to realise a four-quadrant analogue multiplier using general-purpose operational amplifiers (opamps) as only the active elements is described in this article. The realisation method is based on the quarter-square technique, which utilises the inherent square-law characteristic of class AB output stage of the opamp. The multiplier can be achieved from the proposed structure with using either bipolar or complementary metal-oxide-semiconductor (CMOS) opamps. The operation principle of the proposed multiplier has been confirmed by PSPICE analogue simulation program. Simulation results reveal that the principle of proposed scheme provides an adequate performance for a four-quadrant analogue multiplier. Experimental implementations of the proposed multiplier using bipolar and CMOS opamps are performed to verify the circuit performances. Measured results of the experimental proposed schemes based on the use of bipolar and CMOS opamps with supply voltage ± 2.4 V show the worst-case relative errors of 0.32% and 0.47%, and the total harmonic distortions of 0.47% and 0.98%, respectively.

Keywords: four-quadrant analogue multiplier; operational amplifier; squaring circuit; quarter-square technique; class AB

1. Introduction

An analogue multiplier is a basic circuit building block for analogue signal processing in instrumentation and communication systems such as a variable gain amplifier, automatic gain control amplifier, waveform generator, modulator, frequency doubler, phase-locked loop, amplitude-locked loop, small signal rectifier, etc. The most received attention techniques to realise analogue multiplier are based on the use of quarter-square technique (Pena-Finol and Connelly 1987; Kimura 1994) and translinear characteristics of bipolar or MOS transistors operating in a saturation region (Huijsing, Lucas and Bruin 1982; Bratt, King and Lysejko 1991; Oliaei and Loumeau 1996; Abuelmaatti and Abed 1999; Ravindran, Ramarao, Vidal and Ismail 2001; De La Cruz-Blas, Lopez-Martin and Carlosena 2003). However, these approaches are realised for the specific purpose and are unavailable in commercial integrated circuit form. The economical attraction in the design of electronic circuits is one of the most important roles to take into consideration. Consequently, a general-purpose operational amplifier (opamp), which is a commercially available,

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low-cost and high performance device, is usually employed as a basic circuit building block in analogue circuits and system applications. The output stage of almost opamp provides a class AB configuration, where its characteristic can be explained by translinear principle (Gilbert 1975; Seevinck and Wiegerink 1991). The characteristic of class AB output stage of opamp can be exploited to realise a high performance squaring scheme (Surakampontorn 1988), which is well suited for implementing the analogue multiplier based on quarter-square technique. The use of opamp in the realisation of the analogue multiplier will provide the structure of high performance at low cost and simple construction. In this article, a four-quadrant analogue multiplier is described. The proposed circuit requires only general-purpose opamps as active element. Either bipolar or CMOS opamps can be used to realise the analogue multiplier using the proposed scheme. The technique is based on translinear characteristic of class AB output stage of opamp, which is already existed within its supply current. The opamp supply current sensing technique (Toumazou and Lidgey 1987; Surakampontorn 1988; Riewruja and Kamsri 2009) is employed to obtain the square of sum and difference of two input signals, and the multiplication is preformed by the quarter-square algebraic identity. In addition, low-supply voltage operation of the proposed analogue multiplier is also achieved for low-voltage opamp used in the scheme.

2. Circuit description

2.1. *Principle*

The proposed four-quadrant analogue multiplier is realised based on the quarter-square technique. The squaring circuit and summing amplifiers formed by general-purpose opamps are used to set up the mathematical relationship as

$$v_o = \frac{1}{4}[(v_1 + v_2)^2 - (v_1 - v_2)^2] = v_1 v_2. \tag{1}$$

The square operation can be achieved from the characteristic of the class AB output stage of the opamp. Simple scheme to extract the existed square signal from the supply current is shown in Figure 1 (Surakampontorn 1988). Opamps A_1 and A_2 and resistor R_1 form a voltage-to-current converter to convert the input signal voltage v_{in} into the signal current $i_{in} = v_{in}/R_1$. For bipolar opamp, the supply currents I_1 and I_2

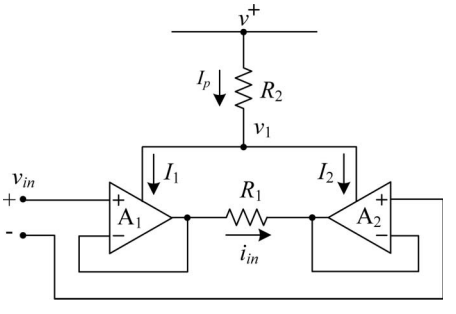


Figure 1. Squaring scheme.

can be expressed as (Toumazou and Lidgey 1987; Surakampontorn 1988; Riewruja and Kamsri 2009)

$$I_1 = I_{B1} + \left[\frac{(4I_{S1}^2 + i_{in}^2)^{1/2} + i_{in}}{2}\right] \text{ for } |i_{in}| \leq 2I_{S1} \tag{2a}$$

$$I_2 = I_{B2} + \left[\frac{(4I_{S2}^2 + i_{in}^2)^{1/2} - i_{in}}{2}\right] \text{ for } |i_{in}| \leq 2I_{S2} \tag{2b}$$

where I_{Bi} and I_{Si} denote the quiescent supply current and the class AB bias current, respectively, of opamp A_i. Assuming that opamps A_1 and A_2 are closely matched such as $I_{B1} = I_{B2} = I_B$ and $I_{S1} = I_{S2} = I_S$. The current I_p, which is the sum of the currents I_1 and I_2, is sensed and converted to voltage v_1 by resistor R_2. Therefore, the voltage v_1 can be written as

$$v_1 = v^+ - 2R_2I_B - 2R_2I_S\left(1 + \frac{i_{in}^2}{4I_S^2}\right)^{1/2}. \tag{3}$$

The square-root term in Equation (3) can be expanded using the power series and then becomes

$$v_1 = v^+ - 2R_2(I_B + I_S) - 2R_2I_S\left[\frac{1}{2}\left(\frac{i_{in}}{2I_S}\right)^2 - \frac{1}{8}\left(\frac{i_{in}}{2I_S}\right)^4 + \cdots\right]. \tag{4}$$

If the magnitude of signal current i_{in} is chosen such that $i_{in} \leq 1.26I_S$, then the higher-order terms in the expansion can be neglected, and Equation (4) is given as

$$v_1 = [v^+ - 2R_2(I_B + I_S)] - \frac{R_2}{4I_S}i_{in}^2 \tag{5a}$$

or

$$v_1 = [v^+ - 2R_2(I_B + I_S)] - \frac{R_2}{4I_SR_1^2}v_{in}^2. \tag{5b}$$

It should be noted that the first term in the right side of Equation (5b) is DC component and the second term is the square of the input signal voltage v_{in} with the scale factor $R_2/(4I_SR_1^2)$. If CMOS opamp is used in Figure 1, then the currents I_1 and I_2 can be given by (Surakampontorn and Riewruja 1992)

$$I_1 = I_{B1} + \frac{(4I_{S1} + i_{in})^2}{16I_{S1}} = I_{B1} + I_{S1}\left(1 + \frac{i_{in}}{4I_{S1}}\right)^2 \tag{6a}$$

$$I_2 = I_{B2} + \frac{(4I_{S2} - i_{in})^2}{16I_{S2}} = I_B + I_{S2}\left(1 - \frac{i_{in}}{4I_{S2}}\right)^2. \tag{6b}$$

Similar to bipolar opamp case, the voltage v_1 of the circuit in Figure 1, can be stated as

$$v_1 = [v^+ - 2R_2(I_B + I_S)] - \frac{R_2 i_{in}^2}{8I_S} \tag{7a}$$

or

$$v_1 = [v^+ - 2R_2(I_B + I_S)] - \frac{R_2 v_{in}^2}{8I_S R_1^2}. \tag{7b}$$

It should be noted that the second term of the right side of Equation (7b) is the square of the input signal voltage v_{in} with scale factor $R_2/(8I_S R_1^2)$.

2.2. *Multiplier realisation*

The proposed four-quadrant analogue multiplier using opamps is shown in Figure 2. The circuit consists of five general-purpose opamps such that the opamps A_{i1} and A_{i2} are available in same package. Opamps A_{11} and A_{12}, A_{21} and A_{22} and resistors $R_{11} = R_{12} = R_1$ are connected as voltage-to-current converters. Resistors R_{21} and R_{22}, where $R_{21} = R_{22} = R_2$, are used to sense the supply currents I_{p1} and I_{p2}. The input signal voltage v_y is inverted by the unity-gain inverting amplifier formed by opamp A_{22} and resistors $R_{51} = R_{52}$. Therefore, the current $i_y = (v_x + v_y)/R_1$ is achieved. If bipolar opamp is used in Figure 2, then the sensing voltages v_{21} and v_{22} can be expressed as

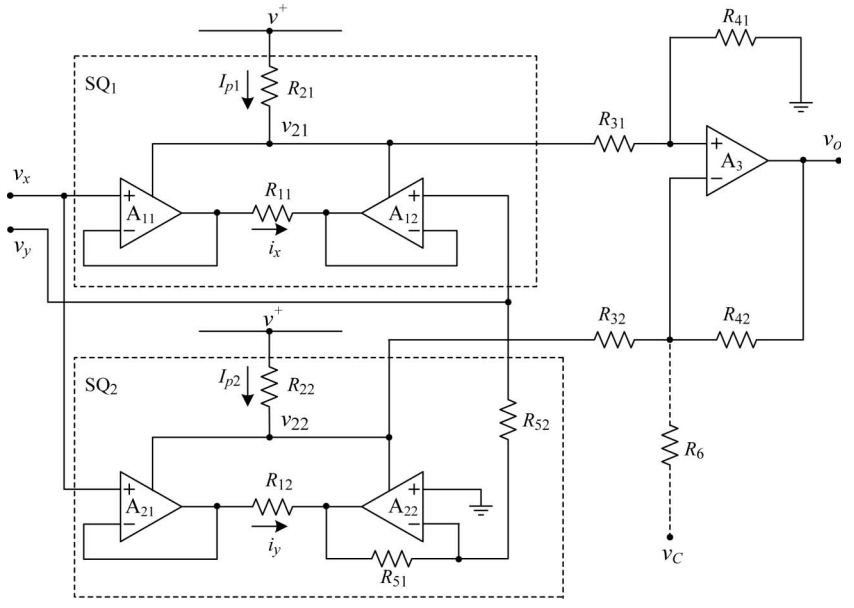


Figure 2. Proposed four-quadrant analogue multiplier.

$$v_{21} = v^{+} - 2R_2(I_B + I_S) - \frac{R_2}{4I_S R_1^2}(v_x - v_y)^2 \tag{8a}$$

$$v_{22} = v^{+} - 2R_2(I_B + I_S) - \frac{R_2}{4I_S R_1^2}(v_x + v_y)^2 \tag{8b}$$

where v_x and v_y are input signal voltages. The voltages v_{21} and v_{22} are transferred to difference amplifier formed by opamp A_3 and resistors $R_{31} = R_{32} = R_3$ and $R_{41} = R_{42} = R_4$, where resistance R_3 is chosen such that $R_3 \gg R_2$. As a result, output voltage v_o is given by

$$v_o = K_b v_x v_y \tag{9a}$$

$$K_b = \frac{R_4 R_2}{I_S R_3 R_1^2} \tag{9b}$$

where K_b is the scale factor of the proposed multiplier using bipolar opamps. If CMOS opamp is used in the proposed multiplier, then the voltages v_{21} and v_{22} are obtained as follows:

$$v_{21} = v^{+} - 2R_2(I_B + I_S) - \frac{R_2}{8I_S R_1^2}(v_x - v_y)^2 \tag{10a}$$

$$v_{22} = v^{+} - 2R_2(I_B + I_S) - \frac{R_2}{8I_S R_1^2}(v_x + v_y)^2. \tag{10b}$$

Consequently, output voltage v_o is given by

$$v_o = K_c v_x v_y \tag{11a}$$

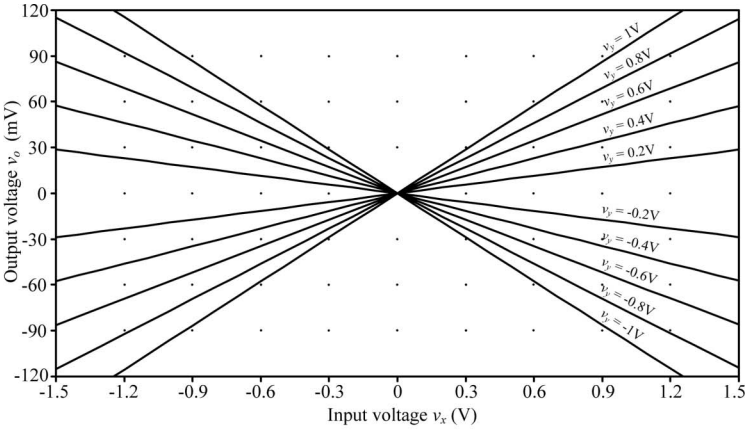
$$K_c = \frac{R_4 R_2}{2I_S R_3 R_1^2} \tag{11b}$$

where K_c denotes the scale factor of the proposed circuit using CMOS opamps. It can be seen that the four-quadrant analogue multiplier can be realised using bipolar or CMOS opamps without a specific device.

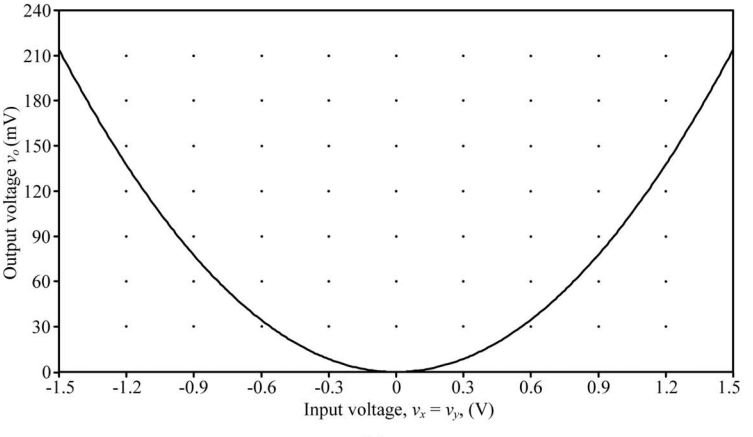
3. Performance analysis

3.1. Errors in the multiplier

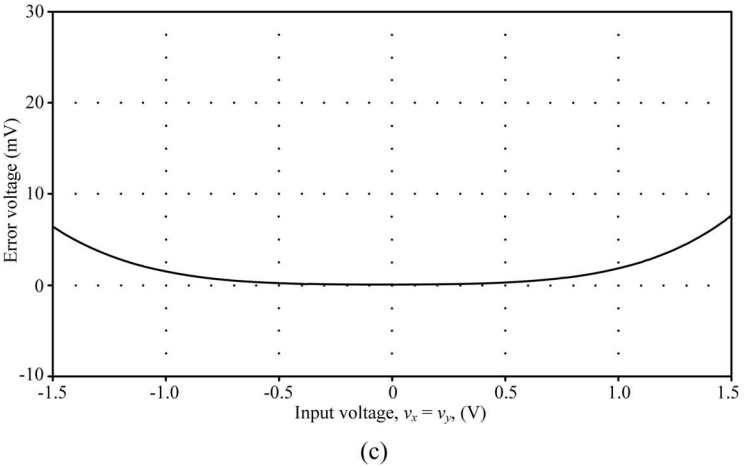
The multiplication function in previous description results from the assumptions that all devices are perfectly matched. However, in a practical realisation, the mismatches of devices used in the circuit are the major factor contributing to the distortion and error in the output response. The mismatch between opamps in



(a)



(b)



(c)

Figure 3. Simulation results. (a) DC transfer characteristic. (b) Transfer characteristic of proposed multiplier as squarer. (c) Error of transfer characteristic for proposed multiplier as squarer.

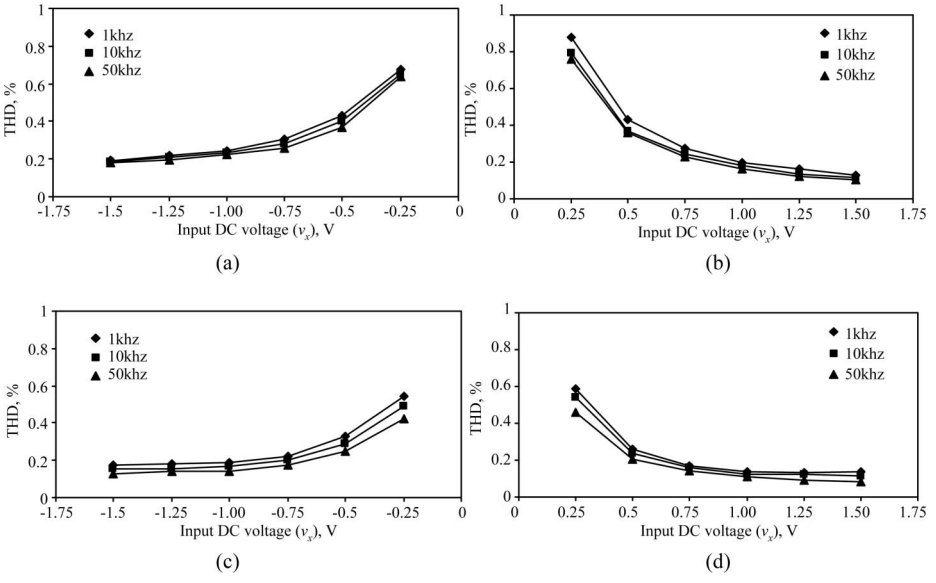


Figure 4. Simulated THDs. (a) For the first case with $v_x < 0$. (b) For the first case with $v_x > 0$. (c) For the second case with $v_y < 0$. (d) For the second case with $v_y > 0$.

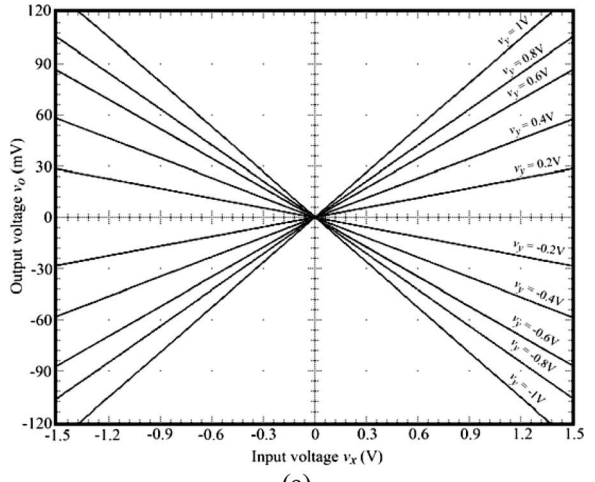
dotted line frames SQ_1 and SQ_2 and also the mismatch between resistors R_{i1} and R_{i2}, where $i = 1, 2, 3, 4$ and 5, in Figure 2 are considered. Hence output signal voltage v_o can be written as

$$v_o = \frac{R_2 R_4}{a R_1^2 R_3 I_S}\left[(1-\varepsilon_1)v_x v_y + \frac{\Delta_R}{2}\left(v_x^2 + v_y^2\right) - \Delta_R v_y^2\right] - v_{offset} \tag{12a}$$

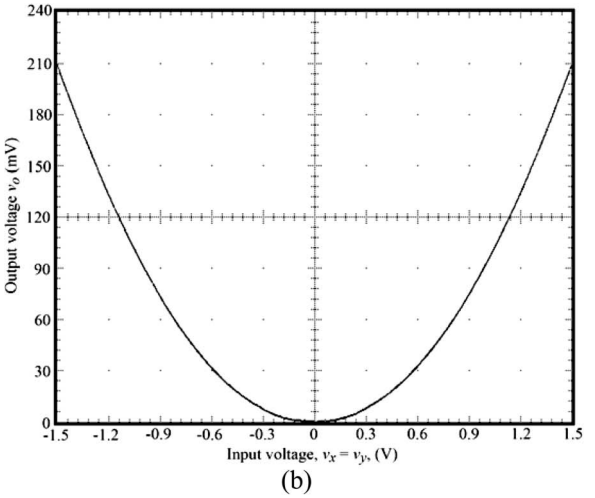
$$\varepsilon_1 = \frac{\Delta_R}{2} + \frac{\Delta_S}{2I_S} \tag{12b}$$

$$v_{offset} = \frac{2R_2 R_4}{R_3}(I_B + I_S)\left[\Delta_R + \frac{(\Delta_B + \Delta_S)}{(I_B + I_S)}\right] \tag{12c}$$

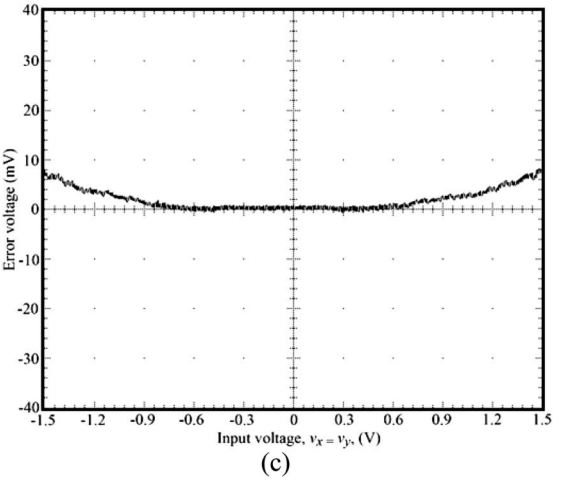
where Δ_B and Δ_S are the mismatch current of the quiescent current I_B and the class AB bias current I_S, respectively, of opamps in SQ_1 and SQ_2, $\Delta_R = (R_{i1} - R_{i2})/R_i$ is the mismatch factor between resistors R_{i1} and R_{i2}, a is constant that set to 1 and 2 for bipolar and CMOS opamps, respectively, used in the circuit, ε_1 is the error factor and v_{offset} denotes DC voltage offset. The currents I_B and I_S are, respectively, assigned to $I_{B1} = (1 + 0.5\Delta_B)I_B$ and $I_{S1} = (1 + 0.5\Delta_S)I_S$ for opamps in SQ_1 and $I_{B2} = (1 - 0.5\Delta_B)I_B$ and $I_{S2} = (1 - 0.5\Delta_S)I_S$ for opamps in SQ_2. Also resistors R_{i1} and R_{i2} are assigned to $R_{i1} = (1 + 0.5\Delta_R)R_i$ for resistor in SQ_1 and $R_{i2} = (1 - 0.5\Delta_R)R_i$ for resistor in SQ_2. From Equations (12a) and (12c), DC offset voltage v_{offset} can be eliminated by the appropriated value of the voltage v_C in the Figure 2. Practically, the general-purpose dual opamp MC33172, which is designed using bipolar



(a)



(b)



(c)

Figure 5. Experimental results of proposed multiplier using bipolar opamp. (a) DC transfer characteristic. (b) Transfer characteristic of proposed multiplier as squarer. (c) Error of transfer characteristic.

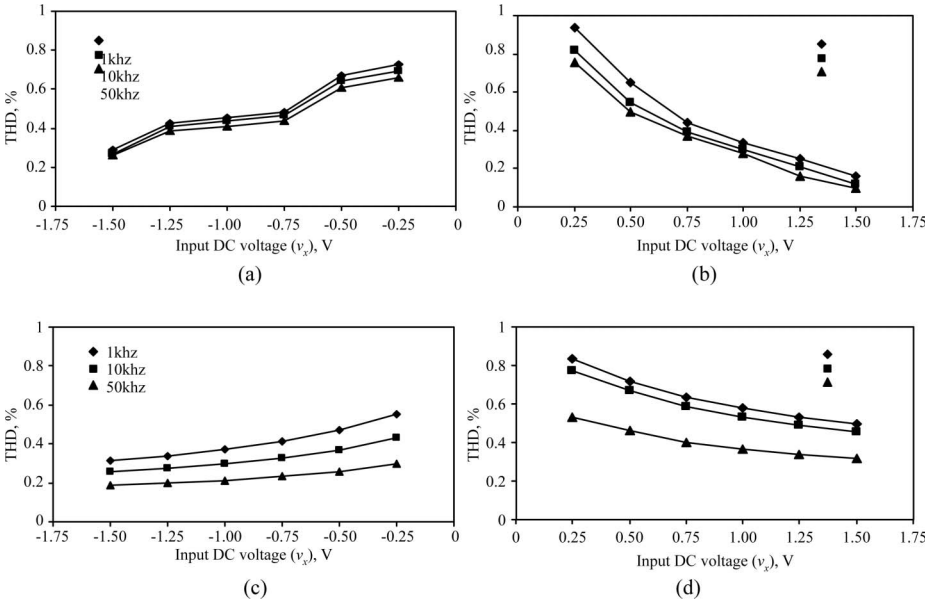


Figure 6. Measured THDs of proposed multiplier using bipolar opamp. (a) For the first case with $v_x < 0$. (b) For the first case with $v_x > 0$. (c) For the second case with $v_y < 0$. (d) For the second case with $v_y > 0$.

technology, is chosen for opamps used in the schemes of SQ_1 and SQ_2. The measured values of parameters I_B, I_S, Δ_{BS} and Δ_S are 94.4 μA, 75 μA, 1.9 μA and 0.36 μA, respectively. The resistance mismatch Δ_R is selected to the worst-case value of 2×10^{-3} or 0.2%. Resistors R_1 to R_4 are $R_1 = 10$ kΩ, $R_2 = 1$ kΩ, $R_3 = R_5 =$ 250 kΩ and $R_4 = 500$ kΩ. Supply voltage $v^+ = -v^-$ is set to 2.4 V. Thus, DC offset voltage v_{offset} and error ε_1 are calculated as $v_{offset} = 10.4$ mV and $\varepsilon_1 = 3.4 \times 10^{-3}$. For CMOS opamps used in Figure 2, output signal voltage v_o is similar to the bipolar opamp case. If the general-purpose CMOS opamp OPA2703 is chosen for the circuit implementation, where the parameters I_B, I_S, Δ_B and Δ_S are 100.2 μA, 29.76 μA, 1.4 μA and 0.2 μA, respectively, then $v_{offset} = 7.44$ mV and $\varepsilon_{1=} 4.3 \times 10^{-3}$ are achieved.

3.2. *High frequency response*

High frequency response of proposed multiplier is limited by opamps used in the circuit. From circuit in Figure 2, opamps A_{1i} and A_{2i} are connected as unity-gain voltage amplifier, which provide high frequency response equal to the gain bandwidth product. Therefore, the high frequency limitation is dependent on the voltage gain of difference amplifier formed by opamp A_3 and resistors R_{31}, R_{32}, R_{41} and R_{42}, where $R_{31} = R_{32} = R_3$ and $R_{41} = R_{42} = R_4$. The single dominant pole P_n of the proposed multiplier can be approximately given by

$$P_n = \frac{1}{\left(1 + \dfrac{R_4 s}{R_3 GBW}\right)} \tag{13}$$

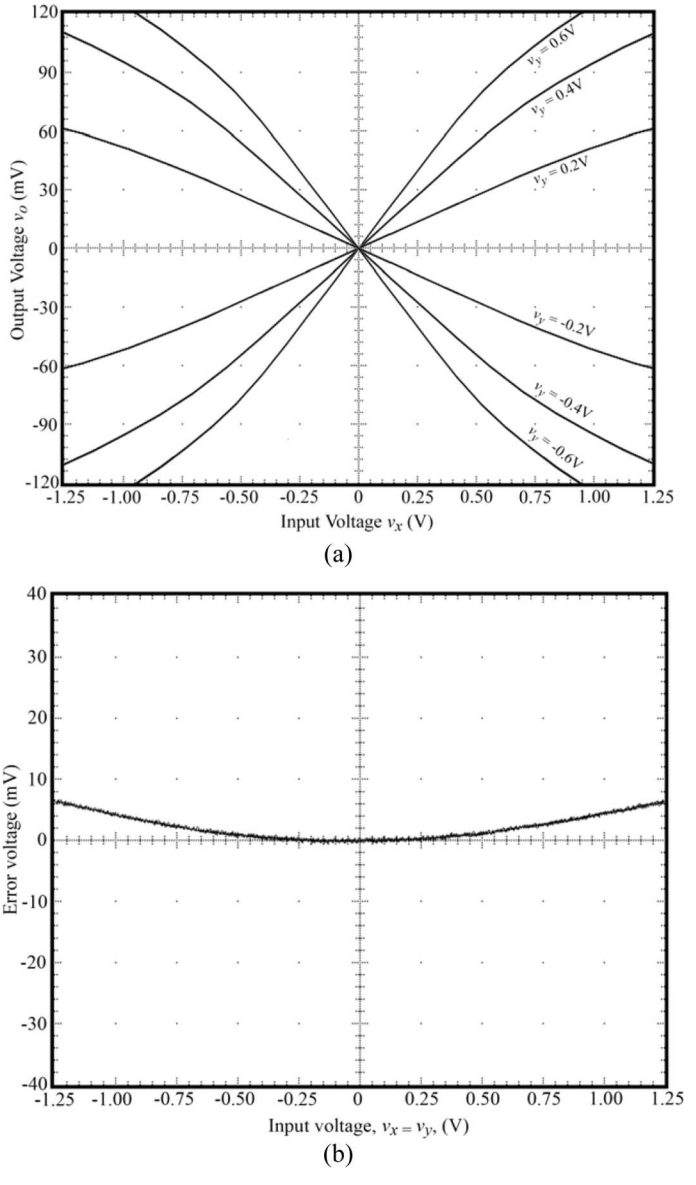


Figure 7. Experimental results of proposed multiplier using low power bipolar opamp. (a) DC transfer characteristic. (b) Error of transfer characteristic for proposed multiplier as squarer.

where GBW is gain bandwidth product of opamp. If $GBW = 1.8$ MHz for opamp MC33172 and $R_4/R_3 = 2$ then dominate pole P_n will be located at 900 kHz.

3.3. *Input operating range*

The range of input signal voltage is determined in term of $(|v_x| + |v_y|)$. For the proposed circuit in Figure 2 using bipolar opamps, the voltages v_{21} and v_{22} are

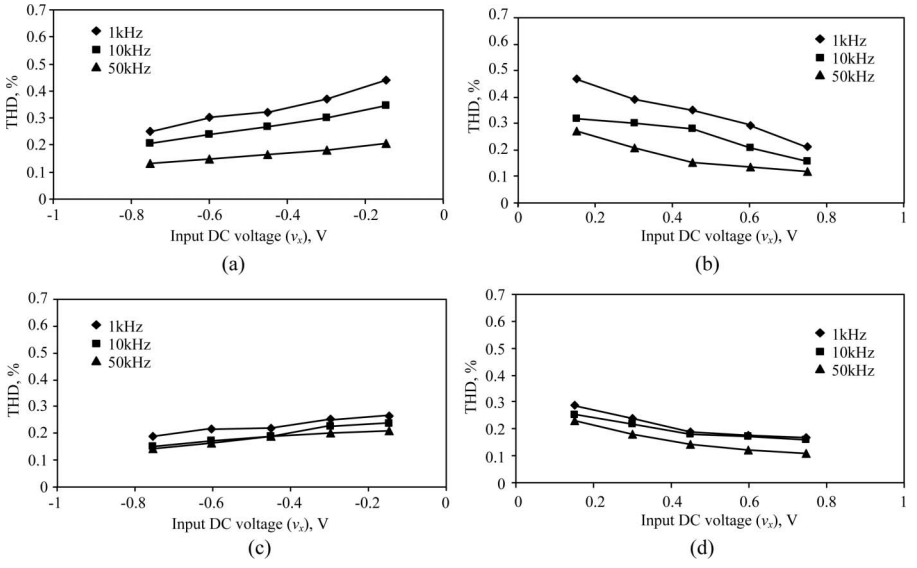


Figure 8. Measured THDs of proposed multiplier using low power bipolar opamp. (a) For the first case with $v_x < 0$. (b) For the first case with $v_x > 0$. (c) For the second case with $v_y < 0$. (d) For the second case with $v_y > 0$.

fulfilled as expressed in Equations (8a) and (8b) with the condition of i_x and i_y smaller than $1.26I_S$. Therefore, the input operating ranges of v_x and v_y are conformed the condition such that $(|v_x| + |v_y|) = 1.26I_S R_1$. In the case of CMOS opamp, the input operating range can be deduced as $(|v_x| + |v_y|) = 4I_S R_1$. It should be noted that the input operating range can be increased using large value of resistance R_1. However, this will decrease the scale factor of proposed multiplier as expressed in Equations (9) and (11).

4. Simulation and experimental results

4.1. Simulation results

The proposed multiplier performance was observed through the use of PSPICE analogue simulation program with using bipolar opamp UA741, where the simplified schematic diagram of UA741 was proposed in the literature (Gray, Hurst, Lewis and Meyer 2001). The opamp bias current I_B and I_S are set to the same value with experimental implementation as 870 μA and 208 μA, respectively. The transistor model of AT&T ALA400 transistor array (Frey 1993) was used for bipolar transistors in the simplified schematic diagram of UA741. Resistors were set to $R_1 = 10$ kΩ, $R_2 = 1$ kΩ, $R_3 = R_5 = 250$ kΩ, $R_4 = 500$ kΩ. Power supply voltage was $v^+ = -v^- = 8$ V. The input operating range and the scale factor K_b can be calculated as 2.62 V and 0.096, respectively. Figure 3(a) shows DC transfer characteristic of the proposed circuit for v_y stepped from -1 V to 1 V by 0.2 V and v_x varied from -1.5 V to 1.5 V. Figure 3(b) and 3(c) show the DC transfer characteristic of the proposed multiplier connected as squarer, $v_x = v_y$, and the error of transfer characteristic, respectively. From Figure 3(c), the worst-case error of about 4.8 mV or 0.37% is obtained for the input operating range

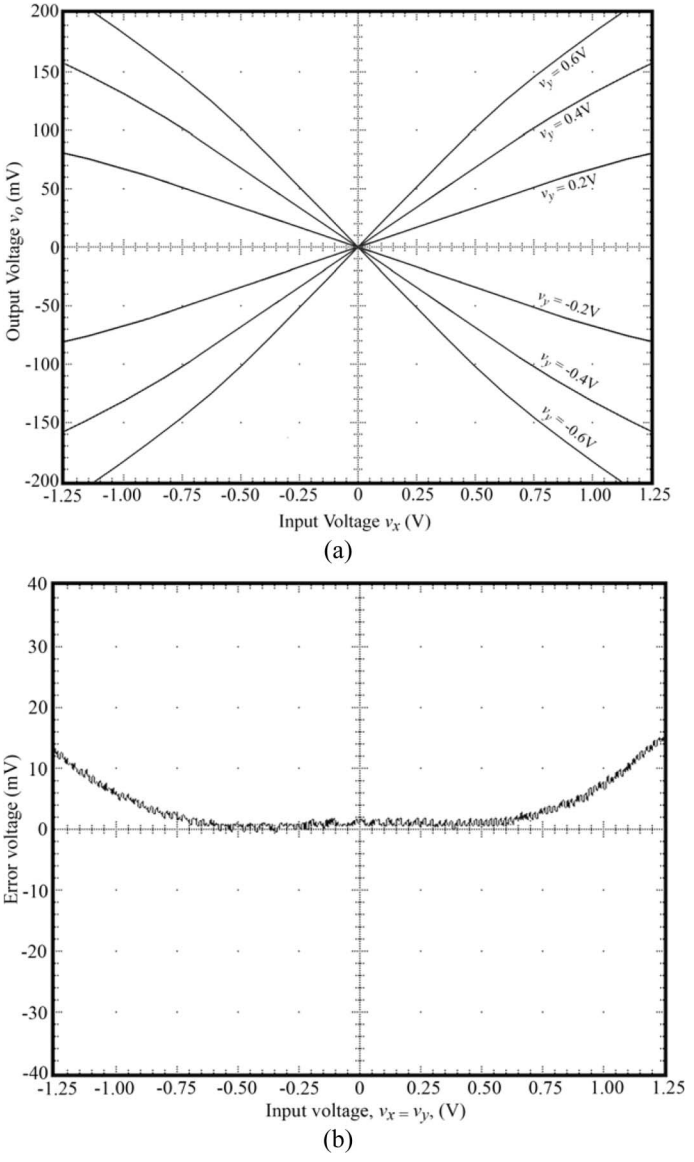


Figure 9. Experimental results of proposed multiplier using low power CMOS opamp. (a) DC transfer characteristic. (b) Error of transfer characteristic for proposed multiplier as squarer.

$|v_x| = |v_y|$ of about 1.3 V. The total harmonic distortion (THD) of the proposed multiplier is determined in two cases. For the first case, the signal voltage is applied to input v_y, while input v_x is set to DC voltage. The second case is that inputs v_x and v_y in the first case are interchanged. The plots of THDs against input signals at 1 kHz, 10 kHz and 50 kHz sinusoidal wave of amplitude 0.5 V_{PP} are shown in Figure 4(a) to 4(d). It can be seen that the maximum THD of about 0.88% is observed.

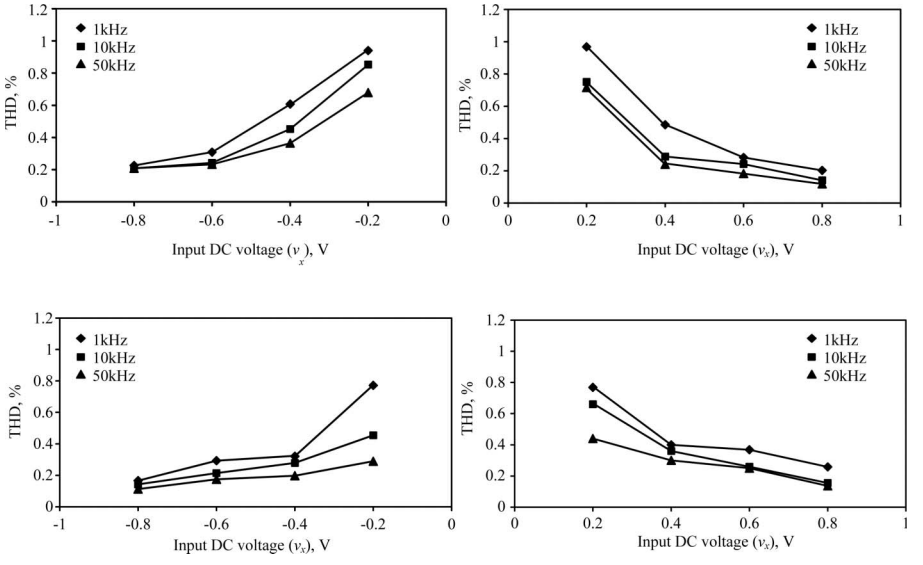


Figure 10. Measured THDs of proposed multiplier using low power CMOS opamp. (a) For the first case with $v_x < 0$. (b) For the first case with $v_x > 0$. (c) For the second case with $v_y < 0$. (d) For the second case with $v_y > 0$.

4.2. Experimental results

To confirm the performances of the proposed circuit, the commercial dual opamp UA1458, which comprised two UA741 in the same package, was used for experimental implementation of circuit in Figure 2. The measured average values of currents I_B, I_S, Δ_B and Δ_S are 870 μA, 208 μA, 11 μA and 7.5 μA, respectively, using the method proposed in the literature (Toumazou and Lidgey 1987). The matched resistors used in the circuit were selectively matched better than 0.2%. The resistors and supply voltages were set to the same values used for the simulation. Figure 5(a) shows the measured DC transfer characteristic, where input voltage v_x varied from -1.5 V to 1.5 V and input voltage v_y stepped from -1 V to 1 V by 0.2 V. The performance of the proposed multiplier connected as squarer is shown in Figure 5(b). Figure 5(c) shows the error of the output voltage v_o. From Figure 5(c), the worst-case error of about 5.2 mV or 0.4% for input operating range $|v_x| = |v_y| = 1.3$ V is achieved. THDs of the proposed multiplier are measured for the same condition with the simulation as shown in Figure 6(a) to 6(d). The maximum THD of about 0.94% is achieved from the result of the first case. It should be noted that the mismatches of devices used in the proposed multiplier cause the THD of experimental results larger than simulation results. For a low power supply voltage, UA1458 opamps used in the circuit are replaced to the commercial low-power and low-voltage opamps. The general-purpose dual opamps MC33172 and OPA2703, which are bipolar opamp and CMOS opamp, respectively, were chosen for demonstrating the performance of the proposed multiplier. Power supply voltage $v^+ = -v^-$ was set to 2.4 V. For the proposed multiplier using bipolar opamps, the measured opamp parameters I_B, I_S, Δ_B and Δ_S are 94.4 μA, 75 μA, 1.9 μA and 0.36 μA, respectively. The maximum operating range ($|v_x| + |v_y|$) of the

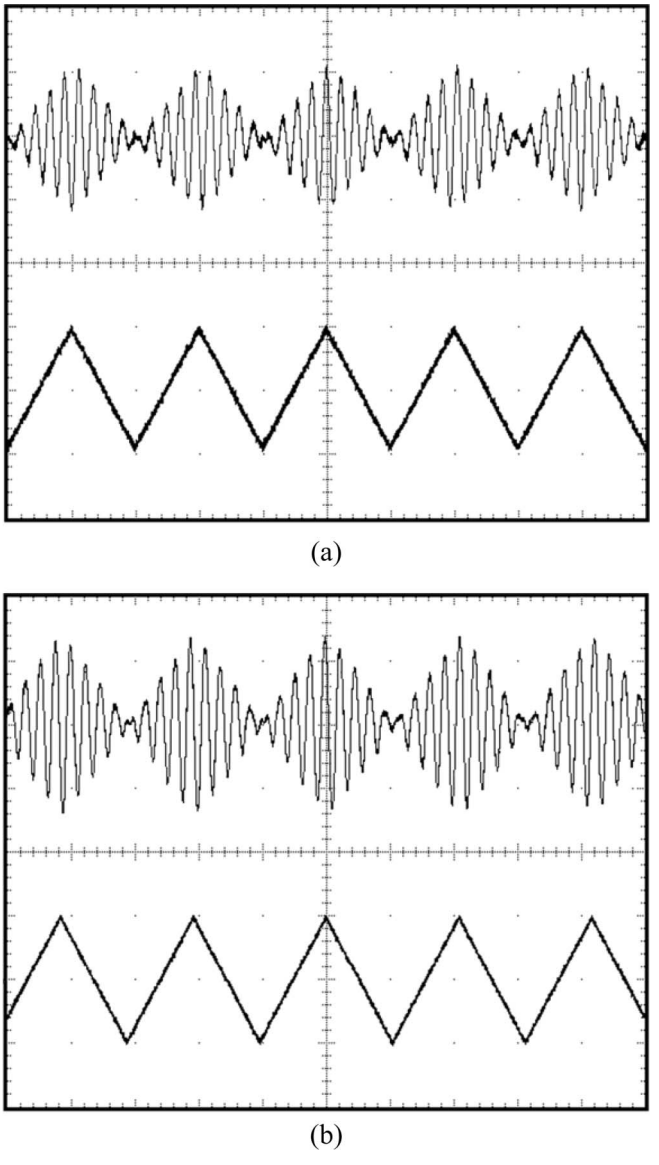


Figure 11. Multiplying result of sinusoidal 100 kHz amplitude 0.4 V_{pp} with triangle 1 kHz amplitude 0.4 V_{pp}. (a) Using low-voltage bipolar opamp, vertical scale, upper trace (output voltage v_o): 20 mV/div; lower trace (input voltage v_y): 0.2 V/div, horizontal scale: 0.5 ms/div. (b) Using low-voltage CMOS opamp, vertical scale, upper trace (output voltage v_o): 20 mV/div; lower trace (input voltage v_y): 0.2 V/div, horizontal scale: 0.5 ms/div.

input voltage of about 0.945 V is calculated. Figure 7(a) shows the DC transfer characteristic. Figure 7(b) shows the measured output error voltage for the proposed multiplier operated as squarer. The worst-case error is about 1.5 mV or 0.32% for the maximum operating range $|v_x| = |v_y| = 0.47$ V. The measured THDs are determined with the same case of the simulation for the amplitude of sinusoidal

Table 1. Comparison between proposed multiplier and previous works.

	Lopez-Martin and Carlosena (2001)	Gravati, Valle, Ferri, Guerrini and Reyes (2005)	Kumngern and Dejhan (2006)	Proposed circuit using bipolar opamps	Proposed circuit using CMOS opamp
THD (%)	1.5	0.9	1.9	0.47	0.98
Measured relative error (%)	1.9	5	1.2	0.32	0.3

frequency of 0.2 V_{pp} as shown in Figure 8(a) to 8(d). The maximum THDs for the first case and second case of about 0.47% and 0.28%, respectively, are observed. The measured bandwidth of about 840 kHz is achieved. For the proposed multiplier using CMOS opamps, the measured opamp parameters I_B, I_S, Δ_B and Δ_S are 100.2 μA, 29.76 μA, 1.4 μA and 0.2 μA, respectively. The maximum input operating range ($|v_x| + |v_y|$) of about 1.2 V is obtained. DC performance is shown in Figure 9(a). Figure 9(b) shows the measured output error voltage for the proposed multiplier operated as squarer. The measured worst-case error is about 1.8 mV or 0.3% for the maximum operating range $|v_x| = |v_y| = 0.6$ V. Also, the measured THDs are obtained to the same case with the simulation for the amplitude of sinusoidal frequency of 0.2 V_{pp} as shown in Figure 10(a) to 10(d). The maximum THDs are about 0.95% and 0.98% for the first case and second case, respectively. The measured bandwidth is about 495 kHz. It should be noted that the THD in the first case is greater than that of the second case for both proposed multiplier using bipolar and CMOS opamps. This is due to the mismatch between resistances R_{51} and R_{52} of the inverting amplifier formed by opamp A_{22}. The proposed multiplier operating as amplitude modulator was used for application example. Figure 11(a) and 11(b) show the results for proposed multiplier using bipolar and CMOS opamps of a 100 kHz sinusoidal of amplitude 0.4 V_{pp} and a 1 kHz triangular wave of amplitude 0.4 V_{pp} applied to inputs v_x and v_y, respectively. It should be noted that the scale factors of proposed multiplier using bipolar and CMOS opamps are about 0.27 and 0.34, respectively. The recent multipliers proposed in Lopez-Martin and Carlosena (2001), Gravati, Valle, Ferri, Guerrini and Reyes (2005) and Kumngern and Dejhan (2006) are referenced for comparison with the proposed circuit in terms of THD and maximum relative error of transfer characteristic. It should be noted that the recent multipliers mentioned above are required for specific design of custom integrated circuit fabrication. Table 1 shows the comparisons of THDs and relative errors of this proposed circuit for ± 2.4 V supply voltage and those of previous works. It is clearly seen that the proposed multiplier exhibits an adequate basic performance for analogue signal processing.

5. Conclusion

A four-quadrant analogue multiplier based on quarter-square technique using general-purpose opamp has been presented. The supply current sensing of the opamp was used to provide a sum-square and difference-square function. The multiplication function was obtained by the result of the difference of sum-square and difference-square function of input signals. Either bipolar or CMOS opamp can

be used in the proposed multiplier. The performances of the proposed multiplier have been demonstrated by simulation and experimental results. The results indicate that the proposed multiplier provides a good performance and offers the advantage of low cost and simple circuit configuration.

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