Analog multiplier using operational amplifier

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Abstract: In this article, presents an analog multiplier using a general-purpose operational amplifier (opamp). The realization method is based on the quarter-square technique, which utilize the square-law characteristic of the class AB output stage of the opamp. The experimental results verifying the proposed multiplier performances are also included. The linearity error and the total harmonic distortion is about 0.8% and 1.6%, respectively.

Keywords: analog multiplier, operational amplifier, quarter-square technique

1. INTRODUCTION

Analog multiplier are basic circuit building blocks for analog signal processing in instrumentation and communication systems such as a variable gain amplifier, automatic gain control amplifier, frequency doubler, phase locked loop, amplitude locked loop, small signal rectifier, etc. In the present, the most received attention analog multipliers are implemented in the form of integrated circuit [1]-[2]. The realization method of these approaches is based on the use of the translinear characteristic of transistors operating in saturation region. However, a specific circuit is required to perform a multiplication function. It is well know that an output stage of a general-purpose opamp is usually a class AB configuration. The operation of a class AB output stage is based on the translinear principle. Therefore, the opamp with a class AB output stage can be employed as a basic active element in the realization of an analog multiplier. The translinear characteristic of an opamp with class AB output stage is existed within the supply current of the opamp. The opamp supply current sensing technique [3]-[4] is employed to obtain the square of the sum and difference of two input signals. The multiplication is achieved by the quarter-square algebraic identity. The purpose of this article is to propose analog multiplier using operational amplifier. The realization method is based on the use of a translinear principle and quarter-square technique. The proposed circuit is required three general-purpose opamps together with resistors, which provides high performance, simple construction and low cost attraction.

2. CIRCUIT DESCRIPTION

2.1 Quarter-square technique

The proposed analog multiplier is based on the quarter-square technique as shown in Fig. 1. The sum and difference of the input v_1 and v_2 are provided for the squares. The difference of squares at the output v_0 is obtained to get the multiplication function and can be written as

$$v_0 = [(v_1 + v_2)^2 - (v_1 - v_2)^2] = 4v_1v_2 \quad (1)$$

From Fig. 1, a square circuit is an important element in the quarter-square technique. Previously, many schemes to realize a square circuit can be found in the literature [5] – [10]. It is known that the class AB characteristic at the output stage of the opamp can be exploited to realize a squaring scheme [5].

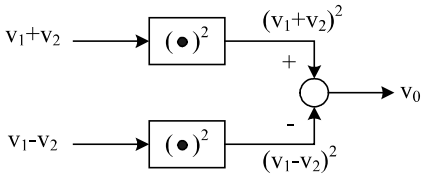


Fig.1 A quarter-square technique

2.2 Characteristic of the class AB output stage

Fig. 2(a) shows a unity gain voltage controlled voltage source using an opamp. The class AB output stage of an opamp is shown in Fig 2(b) transistors in saturation region. From Fig. 2, the relation of the supply currents I_1 and I_2 depicted in Fig 2(a) are comprised of the quiescent bias current drawn by the opamp and the currents I_{01} and I_{02} or

$$I_1 = I_B^+ + I_{01} \quad (2a)$$
$$I_2 = I_B^- + I_{02} \quad (2b)$$

Where I_B^+ and I_B^- are the bias currents drawn by the opamp. In general, the magnitude of the bias current I_B^+ and I_B^- are quite variable from opamp to opamp.

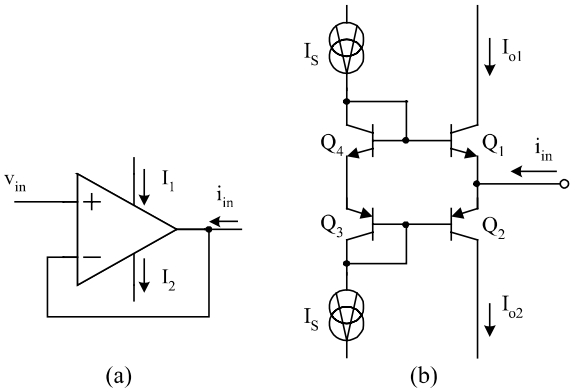


Fig. 2 Principle of the Class AB output stage

Assuming that all transistors in Fig. 2(b) is well matched, the current I_{01} and I_{02} in the Fig. 2(b) can be approximately given by [5]

$$I_{01} = \frac{\{(4I_S^2 + i_{in}^2)^{1/2} - i_{in}\}}{2} \quad \text{for } |i_{in}| \le 2I_S \quad (3a)$$

$$I_{02} = \frac{\{(4I_S^2 + i_{in}^2)^{1/2} + i_{in}\}}{2} \qquad \text{for } |i_{in}| \le 2I_S \qquad (3b)$$

where I_S is the class AB bias current. It should be noted that a square signal is existed in the supply currents I_1 and I_2.

2.3 Squaring scheme

A simple squaring scheme is shown in Fig. 3 [5].

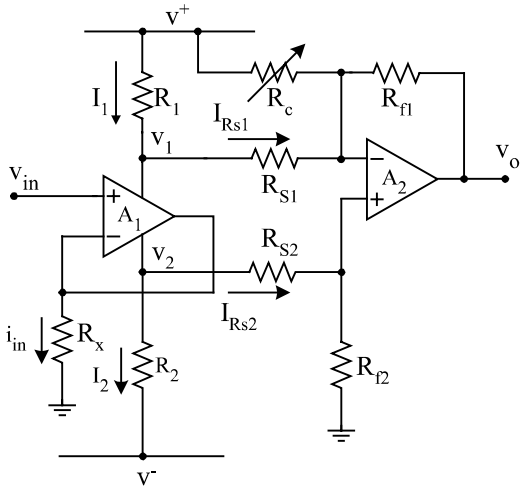


Fig. 3 A simple squaring scheme

The opamp A_1 and converting resistor R_x convert an input signal voltage v_{in} into a signal current $i_{in} = v_{in} / R_x$. For the opamps A_1 and A_2 implemented in bipolar technology, the currents I_1 and I_2 can be given by the use of Eq. (2) and (3) as

$$I_1 = I_B^+ + \frac{\{(4I_S^2 + i_{in}^2)^{1/2} - i_{in}\}}{2} \qquad \text{for } |i_{in}| \le 2I_S \qquad (4a)$$

$$I_2 = I_B^- + \frac{\{(4I_S^2 + i_{in}^2)^{1/2} + i_{in}\}}{2} \qquad \text{for } |i_{in}| \le 2I_S \qquad (4b)$$

The currents I_1 and I_2 are, respectively, converted by the sensing resistors R_1 and R_2 to the voltage v_1 and v_2. The voltages v_1 and v_2 are transferred to the summing amplifier, formed by the opamp A_2 and resistors R_{f1}, R_{f2}, R_{S1} and R_{S2}. Assuming that $I_1 >> I_{RS1}$ and $I_2 >> I_{RS2}$, where I_{RS1} and I_{RS2} are the currents through the resistors R_{S1} and R_{S2}, respectively. If $R_1 = R_2 = R$, $R_{S1} = R_{S2} = R_S$, $R_{f1} = R_{f2} = R_f$ and $v^+ = -v^- = v$ then the output voltage v_0 can be expressed as

$$v_0 = 2\frac{RR_f}{R_S} I_B - \frac{R_f}{R_C} v + 2\frac{RR_f}{R_S} I_S \left(1 + \frac{i_{in}^2}{4I_S^2}\right)^{1/2} \qquad (5)$$

The square-root term in the Eq. (5) can be expanded using the power series and then the Eq. (5) becomes

$$v_0 = \left(\frac{2RR_f}{R_S}(I_B + I_S) - \frac{R_f}{R_C} v\right) + \frac{2RR_f I_S}{R_S}\left[\frac{1}{2}\left(\frac{i_{in}}{2I_S}\right)^2 - \frac{1}{8}\left(\frac{i_{in}}{2I_S}\right)^4 + \ldots\ldots\right] \qquad (6)$$

It should be noted that the first term in the right side of the Eq. (6) is the DC component and can be eliminated by setting $(R_f / R_C)v = (2RR_f / R_S)(I_B + I_S)$. If the magnitude of the signal current i_{in} is chosen such that $i_{in} << 2I_S$, then the output voltage v_0 can be given as

$$v_0 = \frac{2RR_f}{8R_S I_S}(i_{in})^2 = \frac{RR_f}{4R_S I_S}\left(\frac{v_{in}}{R_X}\right)^2 = K_1 (v_{in})^2 \qquad (7a)$$

$$K_1 = \frac{RR_f}{4R_S R_X^2 I_S} \qquad (7b)$$

It is evident that the output voltage v_0 is the square of the input voltage v_{in} with the scale factor K_1.

2.4 Multiplier realization

The proposed analog multiplier using opamp is shown in Fig. 4. The circuit consists of three general-purpose opamps A_1, A_2, A_3 and resistors. The opamps A_1, A_2 and resistors $R_{31} = R_{32} = R_3$ are connected as a voltage-to-current converter.

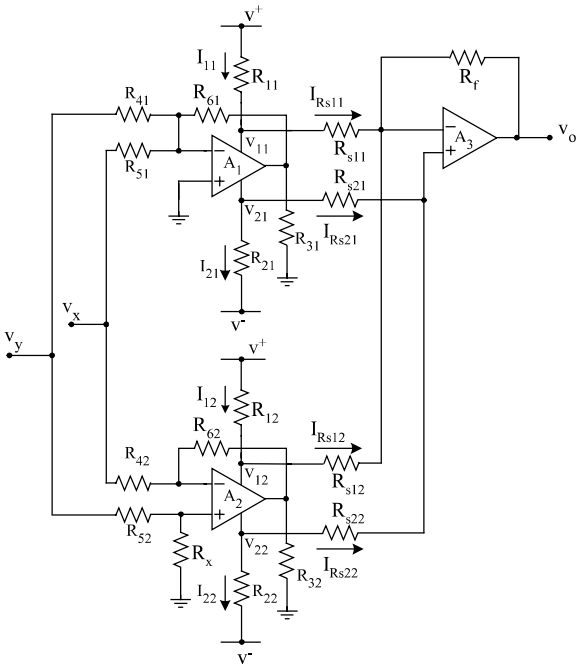


Fig. 4 Proposed analog multiplier

The resistors R_{11}, R_{21}, R_{12} and R_{22} are used to sense the supply current and set $R_{11} = R_{12} = R_1$, $R_{21} = R_{22} = R_2$, $R_1 = R_2$. In Fig. 4, the output voltage v_{01} and v_{02} from opamp A_1 and A_3, A_2 and A_3, respectively, can be expressed as

$$v_{01} = \frac{2RR_f}{8R_S I_S}(i_{31})^2 = \frac{RR_f}{4R_S I_S}\left(\frac{v_x + v_y}{R_X}\right)^2 = K_1 (v_x + v_y)^2 \qquad (8a)$$

$$v_{02} = \frac{2RR_f}{8R_S I_S}(i_{32})^2 = \frac{RR_f}{4R_S I_S}\left(\frac{v_x - v_y}{R_X}\right)^2 = K_1 (v_x - v_y)^2 \qquad (8b)$$

where v_x and v_y are the input signal voltages. The voltage v_{01} and v_{02} are transferred to the difference amplifier formed by the opamp A_3 and resistors $R_{S11} = R_{S21} = R_{S12} = R_{S22} = R_S$ and

$R_{f1} = R_{f2} = R_f$. As a result, the output voltage v_0 is given by

$$v_0 = v_{01} - v_{02} \tag{9}$$

Substituting Eq. (8a) and (8b) into Eq. (9), then the output voltage v_0 is given by

$$v_0 = K_2 v_X v_y \tag{10}$$

$$K_2 = \frac{RR_f}{I_S R_S R_X^2} \tag{11}$$

It can be seen that the general-purpose operational amplifier can be realized an analog multiplier using the proposed structure.

3. EXPERIMENTAL RESULT

The performance of the proposed multiplier depicted in Fig. 4 was shown experimentally. The opamp LM741 was chosen for demonstrating the performance of the proposed multiplier. The resistors used were in the form of 1% tolerance, where $R_1 = R_2 = 2k\Omega$, $R_3 = 10k\Omega$, $R_4 = R_5 = R_6 = R_S = R_x = 100k\Omega$ and $R_f = 200k\Omega$. The power supply voltages $v^+ = -v^-$ were set to 6V.

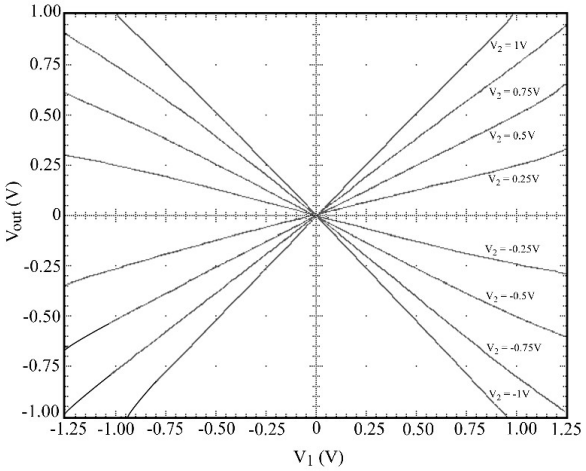


Fig. 5 DC transfer characteristic

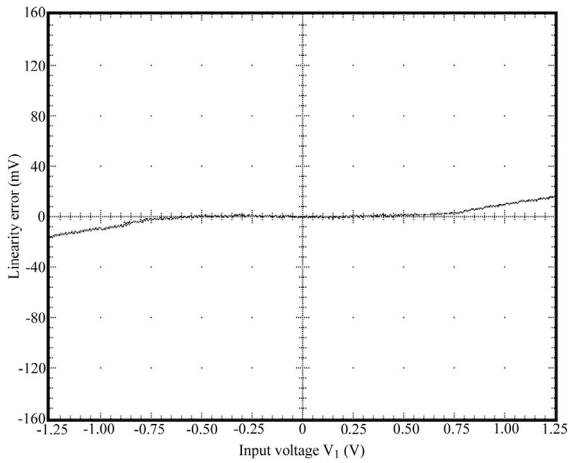
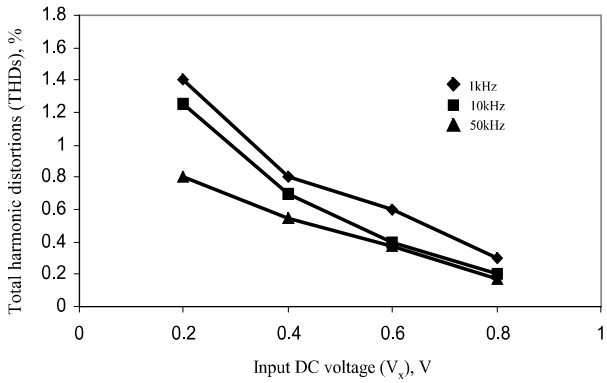


Fig. 6 Linearity error

The DC transfer characteristic is shown in Fig. 5. The dynamic range of the input voltage v_x and v_y of about ±1V is observed. Fig 6 shows the measured linearity error for the input voltage varied from –1.25V to 1.25V. The worse-case linearity error is about 7.9mV or relative error of 0.8% in ±1V input dynamic range. The output response of the proposed multiplier is determined in two cases. For the first case, the signal voltage is applied to the input v_x, while the input v_y is set to dc voltage. The second case is that the input v_x and v_y in the first case are interchanged.



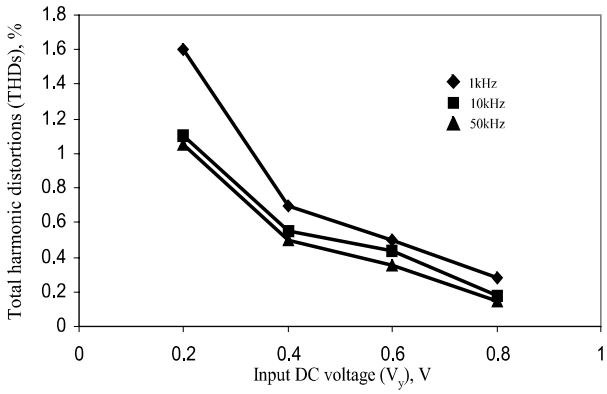


Fig. 7 Total harmonic distortion

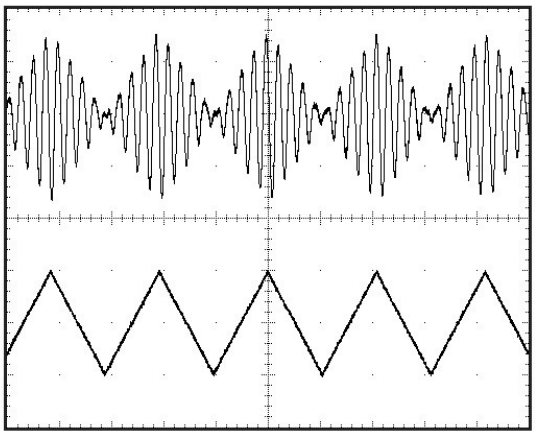


Fig. 8 Multiplying result of sinusoidal 100kHz amplitude 1Vp-p with triangle 1kHz amplitude 1Vp-p

The total harmonic distortions (THDs) versus the input voltage at 1kHz, 10kHz and 50kHz of the amplitude $1V_{p-p}$ are shown in Fig. 7 for the both case. The maximum THD of about 1.6%, are observed. Fig. 8 shows the multiplying result of a 100kHz sinusoidal of amplitude $1V_{p-p}$ and a 1kHz triangular wave of the amplitude $1V_{p-p}$ applied to the input v_x and v_y, respectively. It should be noted that the scale factors of the proposed multiplier using opamp is about 0.75. From the experimental results, it is clearly seen that the proposed multiplier exhibits an adequate basic performance for analog signal processing.

4.CONCLUSION

The analog multiplier based on a quarter-square technique using general-purpose opamp has been presented. The opamp supply-current sensing was used to provide a sum-square and difference-square function. The multiplication function was obtained by the result of the difference of sum-square and difference-square of the input signals. The performance of the proposed multiplier has been demonstrated by experimental implementation. The results indicate that the proposed multiplier provides high performance and offers the advantage of the simple circuit configuration and low cost required.

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