FAULT DETECTION IN MULTI-INPUT ANALOG CIRCUITS USING POLYNOMIAL REGRESSION MODELLING

Presented by

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OBJECTIVE

To detect faults in multi-input analog circuits using polynomial regression models.

- Polynomial modelling for both **linear and nonlinear circuits**.
- Fault detection under **DC sweep and sine wave inputs**
- Analysis of **single and multiple faults**, **noise robustness.**

Literature Survey

Citation	Literature	Purpose	Method Used	Research Gap
S. Sindia, V. D. Agrawal, and V. Singh [1]	29th VLSI Test Symposium, 2011	Non-linear analog circuit test using V-transform	Polynomial coefficients made monotonic using V-transform	Fails to handle multiple faults or noise-influenced variation
S. Sindia and V. D. Agrawal [2]	ITC Conference, 2013	High-sensitivity test signatures for analog circuits	Needs little circuit augmentation	Considers only one fault at a time
Piotr Bilski [3]	*Measurement*, vol. 160, 2020	Ensemble regression for parametric identification	Uses regression ensembles to analyze faults	Not tested on heterogeneous architectures
Zhao & Yuzhu He [4]	*J. of Electronic Testing*, 2015	Test point selection method	Fault ambiguity minimized using optimization	Ignores circuits with undefined inputs
Alkis A. Hatzopoulos [5]	IMSTW 2017	Current spectrum-based analog test	Uses wavelet transforms and supply current	Intermittent faults remain undetected
H. Kobayashi et al. [6]	ICSICT 2020	Op-amp and ADC testing techniques	Combines DC-AC, null, and input generators	Not versatile for all circuit types
Riewruja & Rerkratn [7]	*Int. J. of Electronics*, 2011	Design of low-cost analog multiplier using op-amps	Uses quarter-square technique with class AB op-amps	No regression-based testing or noise/fault sensitivity analysis provided

WHY THIS METHOD?

For Testing Analog Circuits

Specification based test methodology

Suffers from high test cost

To alleviate testing cost problem

Fault Model based test

Alternate test

Limited industry acceptance

Signature based testing using polynomial expansion

Taylor Coefficients as Test Signatures

Advantage of new approach[1] :

- Enhances coefficient sensitivity.
- Improved fault diagnosis without circuit augmentation.
- Increased fault coverage.
- Low defect level & yield loss.

Using :

- OrCAD (for fault injection)
- MATLAB (o/p function is expanded & modified for testing)

Due to :

- Lack of confidence in defect level & yield loss.
- Unavailability of output that are sufficiently sensitive to circuit components.

POLYNOMIAL REGRESSION MODELLING

- **Polynomial regression is a form of linear regression where the relationship between input variables and output is modeled as an nth-degree polynomial.**

- **It approximates the output Vout of an Analog circuit as a Taylor series expansion around nominal input values Vin1=V1 and Vin2=V2.**

$$V_{out} = f(V_{in1}, V_{in2}) = f(V_1, V_2) + (V_{in1} - V_1).f_1(V_1, V_2) + (V_{in1} - V_2).f_2(V_1, V_2) + \frac{1}{2!}\{(V_{in1} - V_1)^2.f_{11}(V_1, V_2) + 2.(V_{in1} - V_1).(V_{in2} - V_2).f_{12}(V_1, V_2) + (V_{in2} - V_2)^2.f_{22}(V_1, V_2)\} + \frac{1}{3!}\{(V_{in1} - V_1)^3.f_{111}(V_1, V_2) + 3.(V_{in1} - V_1)^2.(V_{in2} - V_2).f_{112}(V_1, V_2) + 3.(V_{in1} - V_1).(V_{in2} - V_2)^2.f_{122}(V_1, V_2) + (V_{in2} - V_2)^3.f_{222}(V_1, V_2)\} + \ldots\ldots \quad (1)$$

where $f(V_{in1}, V_{in2})$ and all its partial derivatives $f_1 \equiv \frac{\partial f}{\partial V_{in1}}$, $f_2 \equiv \frac{\partial f}{\partial V_{in2}}$, $f_{11} \equiv \frac{\partial^2 f}{\partial {V_{in1}}^2}$, $f_{22} \equiv \frac{\partial^2 f}{\partial {V_{in2}}^2}$, $f_{12} \equiv \frac{\partial^2 f}{\partial V_{in1}.\partial V_{in2}}$ and so on are continuous and exist at nominal values $V_{in1} = V_1$ and $V_{in2} = V_2$.

- Coefficients ai are estimated using **least squares fitting** (e.g., MATLAB's Polyfitn).

Eqn. (1) can be further approximated as

- $$\boldsymbol{V_{out} = f(V_{in1}, V_{in2}) = a_0 {V_{in1}}^{m} + a_1 {V_{in1}}^{m-1} V_{in2} + a_2 {V_{in1}}^{m-1} + a_3 {V_{in1}}^{m-2} {V_{in2}}^{2} + \ldots\ldots\ldots + \varepsilon} \quad \textbf{(3)}$$

The number of coefficients for an m^{th} degree polynomial regression model which can estimate the output of a two-input CUT can be given as

- $$\mathbf{N_{coeff}} = \frac{(m+1)(m+2)}{2}$$

OPTIMAL ORDER

- **Selecting the right polynomial degree (order) is crucial to avoid underfitting or overfitting in regression-based fault modeling.**

- AIC/BIC provides an automated, principled, and efficient method for selecting the best polynomial order in regression-based fault modeling — without overfitting, thresholds, or guesswork.

$AIC = n \cdot \ln(MSE) + 2 \cdot k$

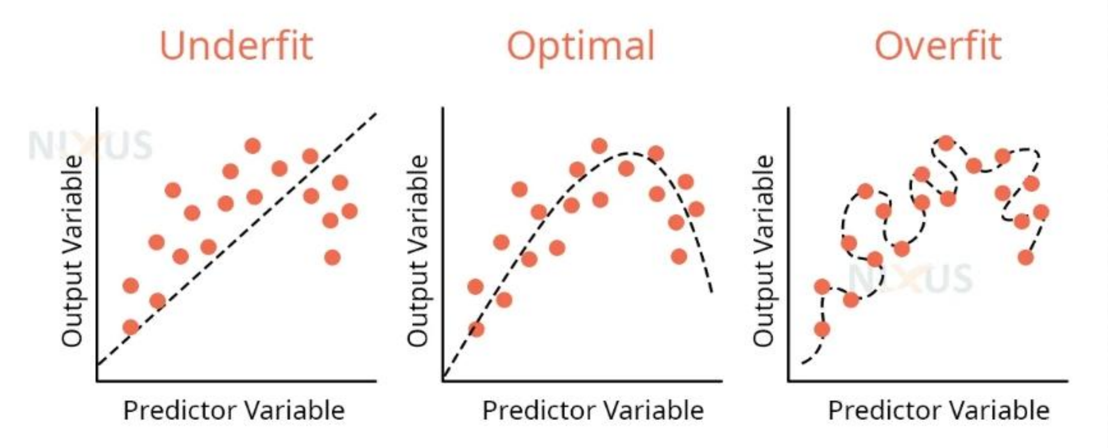
$BIC = n \cdot \ln(MSE) + k \cdot \ln(n)$

Where:

n = Number of data points.

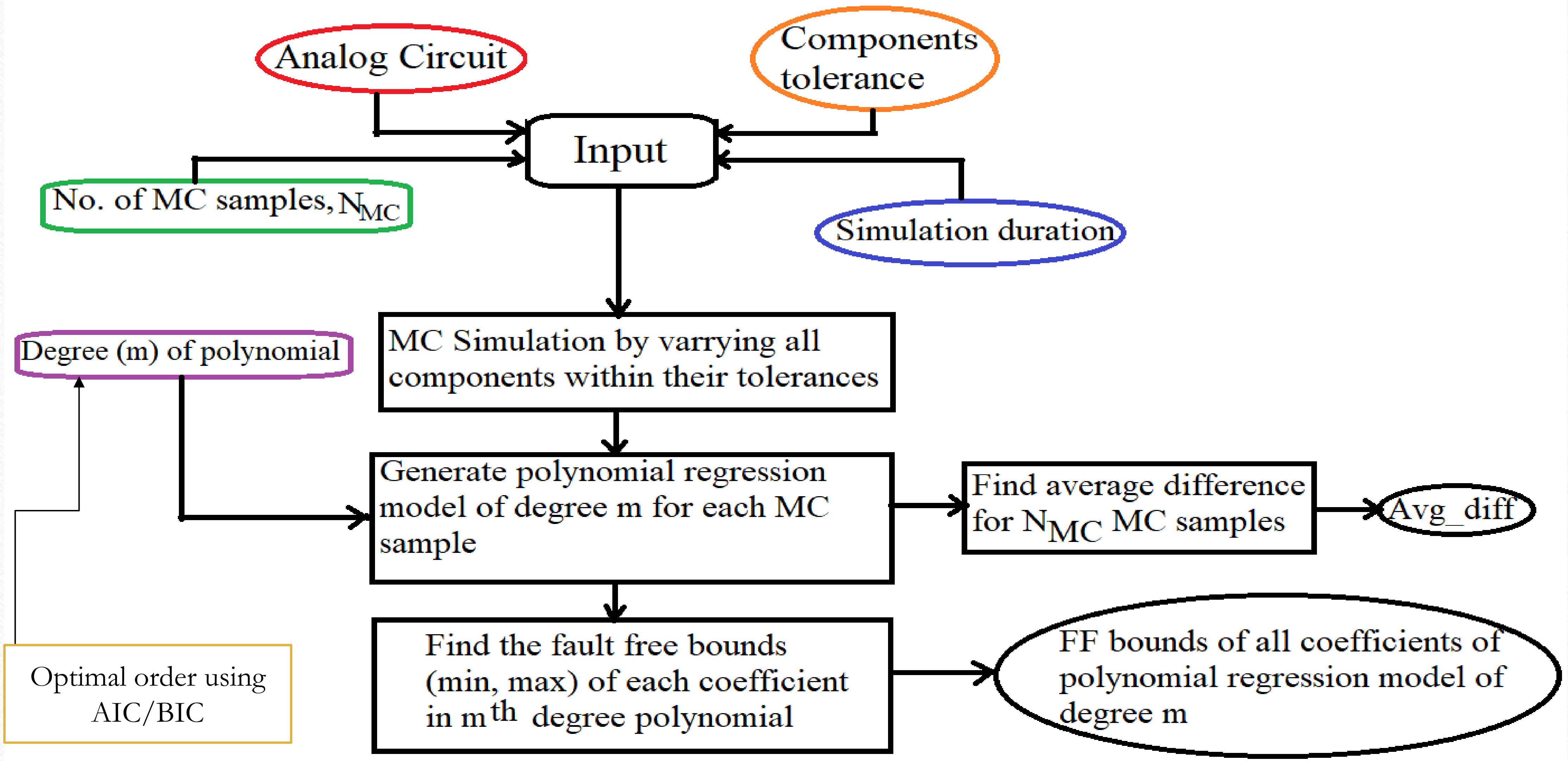
k = Number of parameters (Polynomial order).

MSE = Mean Squared Error.

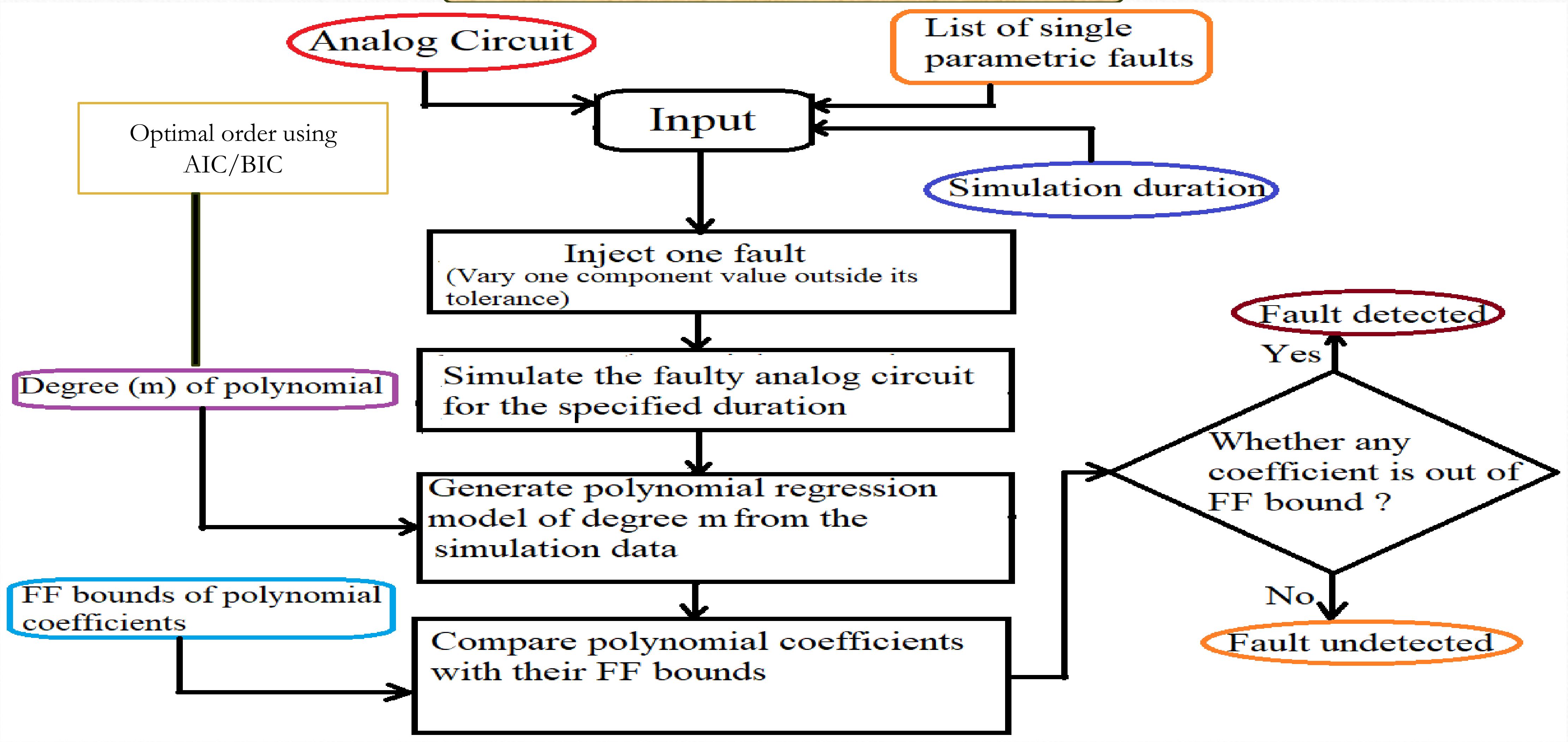


- **AIC/BIC minimizes overfitting by balancing model complexity and error.**
- **This ensures optimal polynomial order for reliable fault detection in analog circuits.**

Flow chart for computation of fault free coefficient bounds



Flowchart for finding faulty component



CIRCUITS UNDER STUDY

LINEAR CIRCUIT

- Lead-lag Circuit with sine input
- Lead-lag circuit with DC sweep input varied at rate of 50 Hz & 100Hz frequency
- PI Compensator of a Buck Converter

NON-LINEAR CIRCUIT

- Analog multiplier with sine input
- Analog Multiplier with DC sweep input varied at the rate of 50 Hz and 100Hz frequency

Case Study-1: Lead-lag Circuit

- A 100 Hz sinusoidal signal at 200 mV amplitude is applied at the inverting input, while a 10 Hz sinusoidal signal at 400 mV amplitude is applied at the non-inverting input.

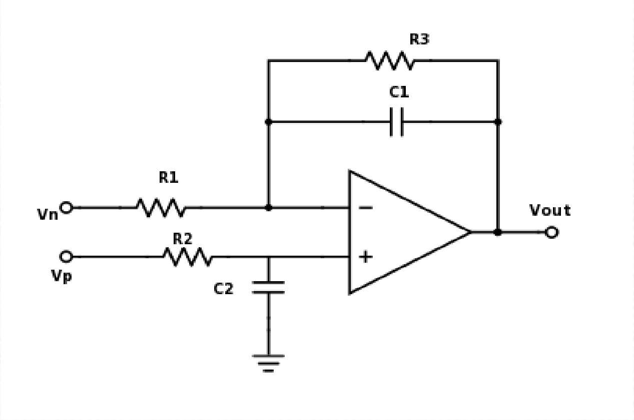
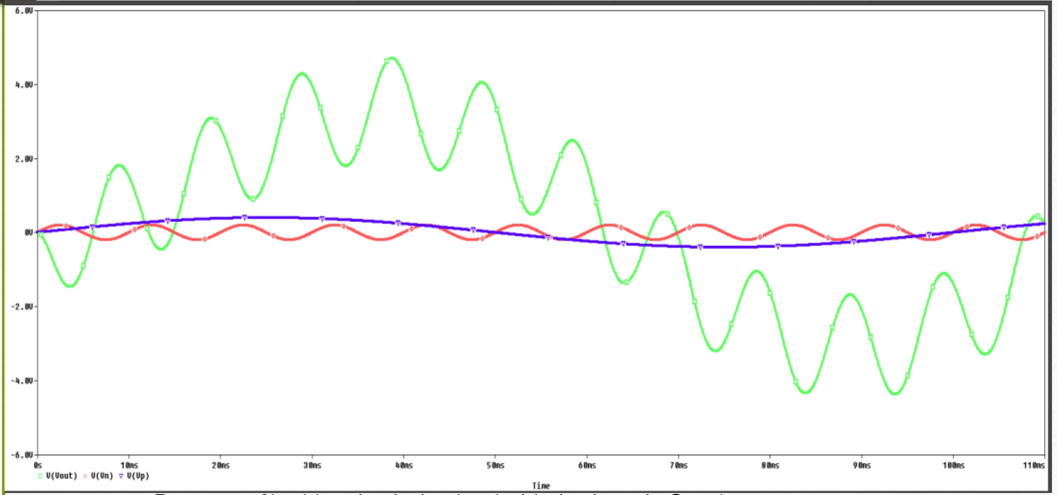


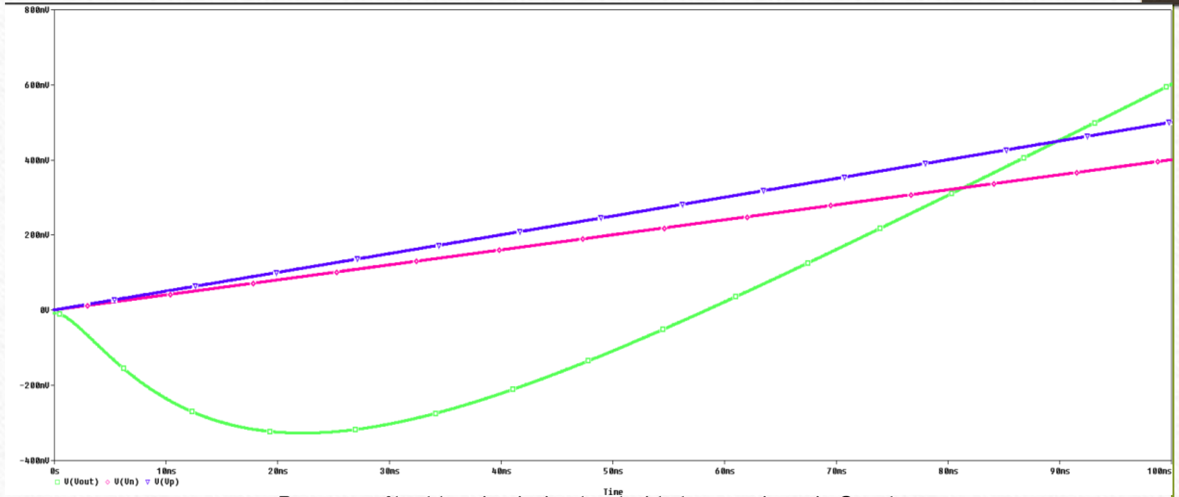
Fig. - Lead-lag circuit with two low-pass filters

- A DC sweep input at the rate of 100 Hz from 0V to 0.4V is applied at the inverting input, while a DC sweep input at the rate of 50 Hz from 0V to 0.5V is applied at the non-inverting input.

The nominal values of the circuit components of the lead-lag circuit shown in Fig. 3 are- R1=1kΩ, R2= 10kΩ, R3=10kΩ, C1=0.1595µF, C2=1.595µF



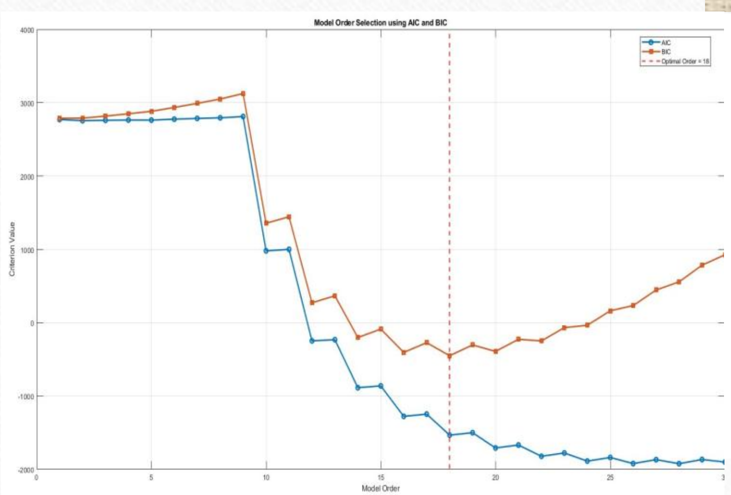
Response of lead-lag circuit simulated with sine input in Orcade



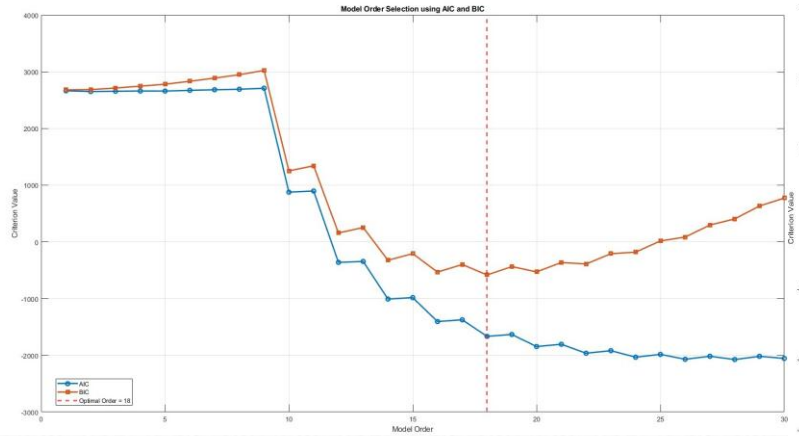
Response of lead-lag circuit simulated with dc sweep input in Orcade

Illustration-1 : Lead-lag Circuit with sine input

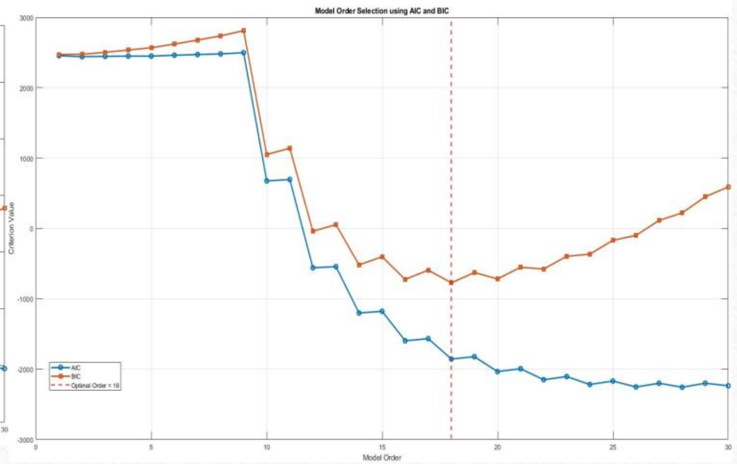
Determination of optimal Order



Optimal order plot at Nmc=500

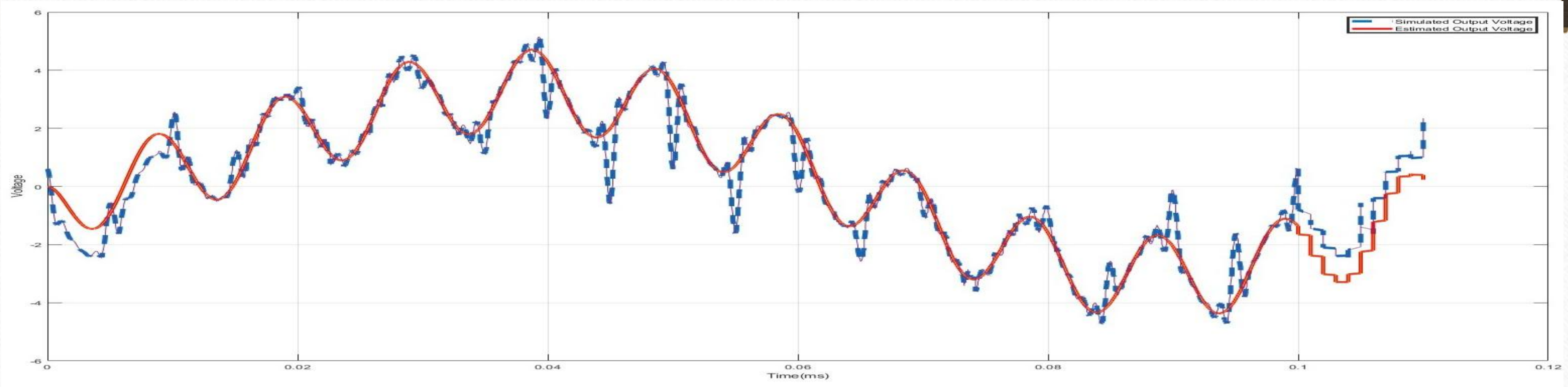


Optimal order plot at Nmc=1000



Optimal order plot at Nmc=2000

Simulated Output VS regression model Output



RESULT

LEADLAG - in case of AC INPUT(SINE WAVE)

Various Detected Faults in LEADLAG in the presence of faults with deviations (5% – 15%) & (20%-47%)

Injected Faults	N_{MC}=500, **Avg_dif** = 0.0420 Optimal Order – 18th		N_{MC}=1000, **Avg_dif** = 0.0420 Optimal Order – 18th		N_{MC}=2000, **Avg_dif** = 0.0420 Optimal Order – 18th	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R1 12%↑	113	√	73	√	64	√
R1 8% ↓	1	√	0	X	0	X
R2 9% ↑	0	X	0	X	0	X
R2 6%↓	0	X	0	X	0	X
R3 10% ↑	71	√	57	√	38	√
R3 7%↓	0	X	0	X	0	X
C1 13%↑	0	X	0	X	0	X
C1 15%↓	3	√	3	√	3	√
C2 11% ↑	0	X	0	X	0	X
C2 14%↓	10	√	7	√	6	√
R1 20%↑	163	√	156	√	153	√
R1 30% ↓	183	√	183	√	183	√
R2 32% ↑	34	√	33	√	32	√
R2 40% ↓	104	√	93	√	89	√
R3 25% ↑	174	√	173	√	172	√
R3 45%↓	185	√	184	√	183	√
C1 42%↑	17	√	14	√	13	√
C1 25% ↓	15	√	14	√	12	√
C2 35% ↑	38	√	33	√	31	√
C2 47% ↓	140	√	135	√	132	√

LEADLAG - in case of AC INPUT(SINE WAVE)

Various Detected Faults in LEADLAG in the presence of faults with deviations (>5%)

Injected Faults	N_{MC}=500, **Avg_dif** = 0.0420 Optimal Order – 18th		N_{MC}=1000, **Avg_dif** = 0.0420 Optimal Order – 18th		N_{MC}=2000, **Avg_dif** = 0.0420 Optimal Order – 18th	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R1 3%↑	0	X	0	X	0	X
R2 2% ↓	0	X	0	X	0	X
R3 4% ↑	0	X	0	X	0	X
C1 2% ↓	0	X	0	X	0	X
C2 4% ↑	0	X	0	X	0	X
R1 1%↓	0	X	0	X	0	X
R2 1%↑	0	X	0	X	0	X
R3 4% ↓	0	X	0	X	0	X
C1 3% ↑	0	X	0	X	0	X
C2 4% ↓	0	X	0	X	0	X

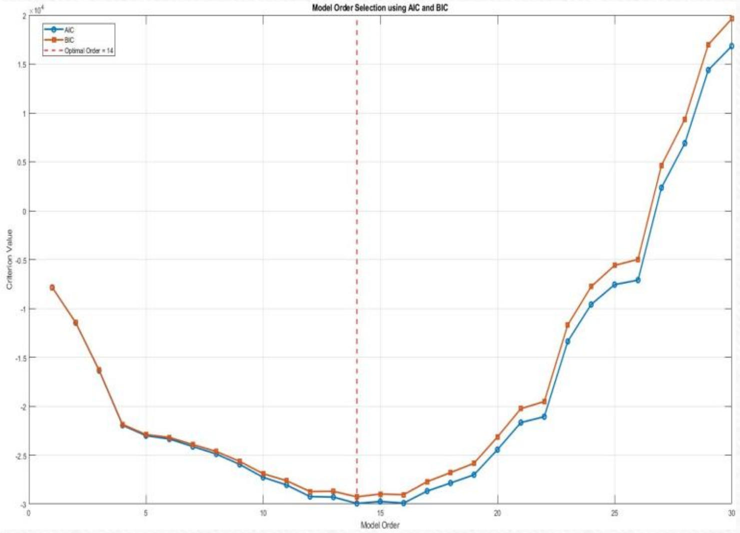
LEADLAG - in case of AC INPUT(SINE WAVE)

Various Detected Faults in LEADLAG in the presence of MULTIPLE faults with deviations

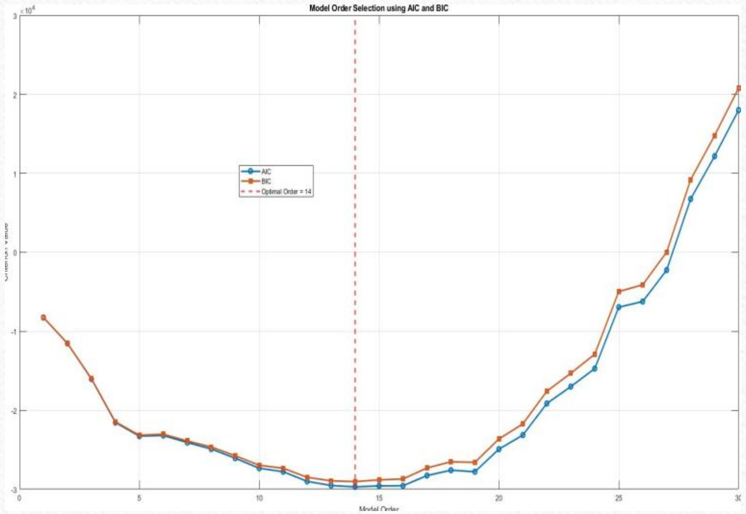
Injected Faults	N_{MC}=500, Avg_dif = 0.0420 Optimal Order – 18th		N_{MC}=1000, Avg_dif = 0.0420 Optimal Order – 18th		N_{MC}=2000, Avg_dif = 0.0420 Optimal Order – 18th	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R1 15%↑ R2 20% ↓	162	√	155	√	151	√
R2 8% ↓ R3 12% ↑	100	√	96	√	90	√
R3 20% ↑ C1 10% ↑ C2 10% ↓	158	√	152	√	151	√
R1 18% ↓ C1 10% ↑ C2 10% ↓	166	√	162	√	160	√
R2 9% ↑ R3 15% ↓ C1 12% ↑ C2 8% ↓	153	√	142	√	137	√

Illustration-2 : Lead-lag Circuit with DC sweep input

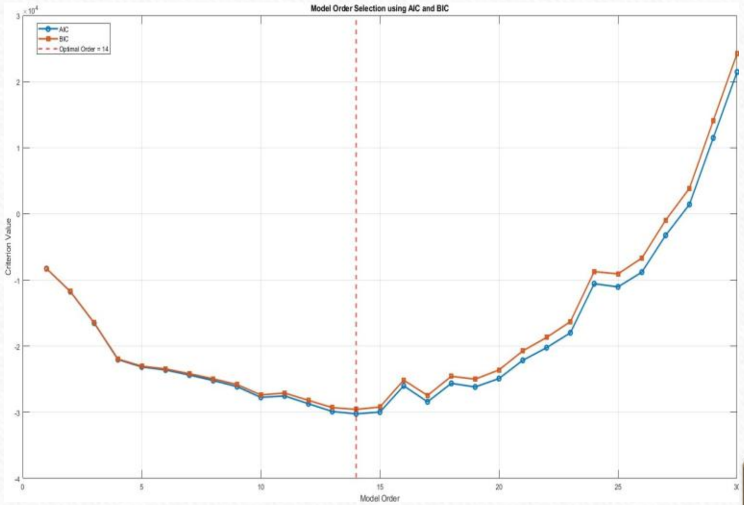
Determination of optimal Order



Optimal order plot at Nmc=500

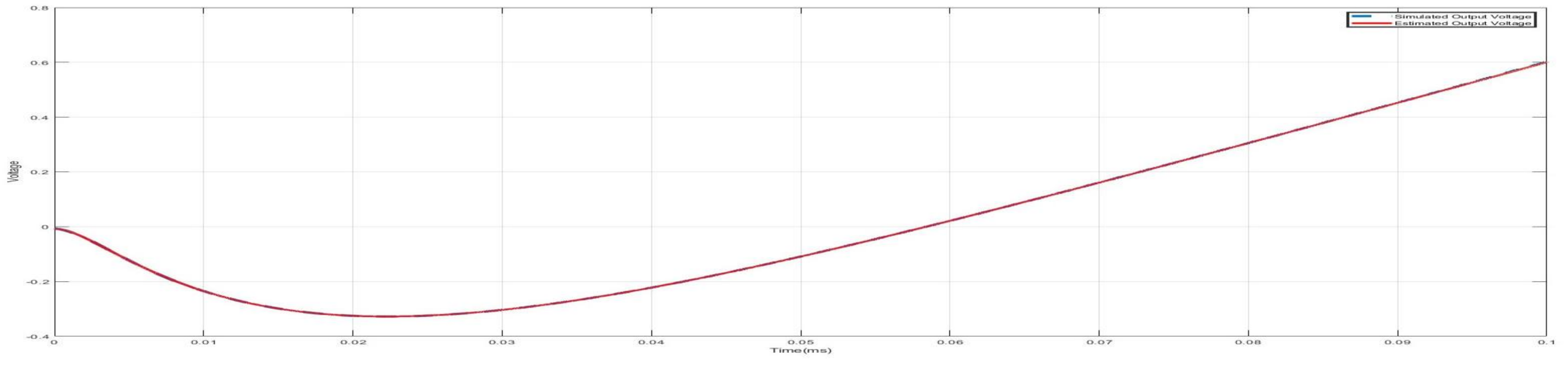


Optimal order plot at Nmc=1000



Optimal order plot at Nmc=2000

Simulated Output VS regression model Output



RESULT

LEADLAG- in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)						
Various Detected Faults in LEADLAG in the presence of faults with deviations (5% – 15%) & (20%-47%)						
Injected Faults	N_{MC}=500, **Avg_dif** = 5.1931e-04 Optimal Order – 14th		N_{MC}=1000,**Avg_dif** = 5.1978e-04 Optimal Order – 14th		N_{MC}=2000,**Avg_dif** = 5.2020e-04 Optimal Order – 14th	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R1 12%↑	0	X	0	X	0	X
R1 8% ↓	0	X	0	X	0	X
R2 9% ↑	0	X	0	X	0	X
R2 6%↓	0	X	0	X	0	X
R3 10% ↑	0	X	0	X	0	X
R3 7%↓	0	X	0	X	0	X
C1 13%↑	0	X	0	X	0	X
C1 15%↓	3	√	2	√	2	√
C2 11% ↑	0	X	0	X	0	X
C2 14%↓	1	√	1	√	1	√
R1 20%↑	1	√	0	X	0	X
R1 30% ↓	3	√	3	√	3	√
R2 32% ↑	1	√	1	√	1	√
R2 40% ↓	1	√	1	√	1	√
R3 25% ↑	10	√	8	√	8	√
R3 45%↓	4	√	4	√	4	√
C1 42%↑	4	√	4	√	3	√
C1 25% ↓	2	√	2	√	2	√
C2 35% ↑	0	X	0	X	0	X
C2 47% ↓	35	√	30	√	26	√

LEADLAG- in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)						
Various Detected Faults in LEADLAG in the presence of faults with deviations (>5%)						
Injected Faults	N_{MC}=500, **Avg_dif** =5.1931e-04 Optimal Order – 14th		N_{MC}=1000, **Avg_dif** = 5.1978e-04 Optimal Order – 14th		N_{MC}=2000, **Avg_dif** = 5.2020e-04 Optimal Order – 14th	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detectio n Status
R1 3%↑	1	√	1	√	1	√
R2 2% ↓	1	√	1	√	0	X
R3 4% ↑	0	X	0	X	0	X
C1 2% ↓	0	X	0	X	0	X
C2 4% ↑	0	X	0	X	0	X
R1 1%↓	0	X	0	X	0	X
R2 1%↑	0	X	0	X	0	X
R3 4% ↓	1	√	0	X	0	X
C1 3% ↑	0	X	0	X	0	X
C2 4% ↓	0	X	0	X	0	X

LEADLAG- in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)						
Various Detected Faults in LEADLAG in the presence of MULTIPLE faults with deviations						
Injected Faults	N_{MC}=500, **Avg_dif** = 5.1931e-04 Optimal Order – 14th		N_{MC}=1000, **Avg_dif** = 5.1978e-04 Optimal Order – 14th		N_{MC}=2000, **Avg_dif** = 5.2020e-04 Optimal Order – 14th	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R1 15%↑ R2 20% ↓	32	√	32	√	29	√
R2 8% ↓ R3 12% ↑	30	√	30	√	29	√
R3 20% ↑ C1 10% ↑ C2 10% ↓	28	√	27	√	25	√
R1 18% ↓ C1 10% ↑ C2 10% ↓	34	√	34	√	32	√
R2 9% ↑ R3 15% ↓ C1 12% ↑ C2 8% ↓	32	√	32	√	29	√

Case Study-2: Analog Multiplier Circuit

Key Features of the Proposed Analog Multiplier:

• Utilizes translinear characteristic of the class-AB output stage of op-amps.
• Employs op-amp supply current sensing technique to obtain:

- Square of sum and Square of difference of two input signals.
- **$v_o = (1/4) \times [\,(v_1 + v_2)^2 - (v_1 - v_2)^2\,] = v_1 \times v_2$**

• Multiplication performed using quarter-square algebraic identity.
• Achieves low-voltage operation with general-purpose op-amps.
• Implements a four-quadrant analog multiplier using only op-amps (no extra active devices).

The nominal component values used in the simulation are:
R11=R12 = 10 kΩ,R21=R22=1 kΩ,R31 =R32= 250 kΩ,R41 =R42= 500 kΩ, R51 = R52=250 kΩ

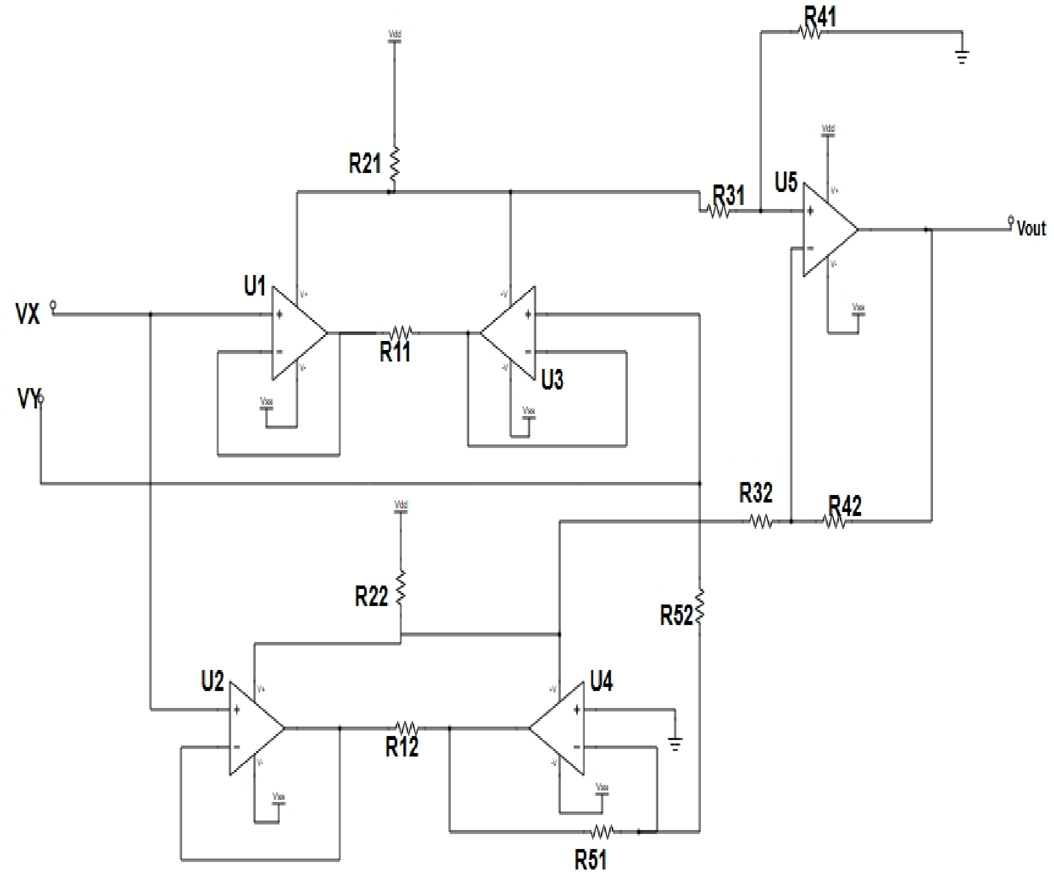


Fig:- Four Quadrant Analog Multiplier using op-amp

Case Study-2: Analog Multiplier Circuit

Fig:-Response of multiplier with sine input

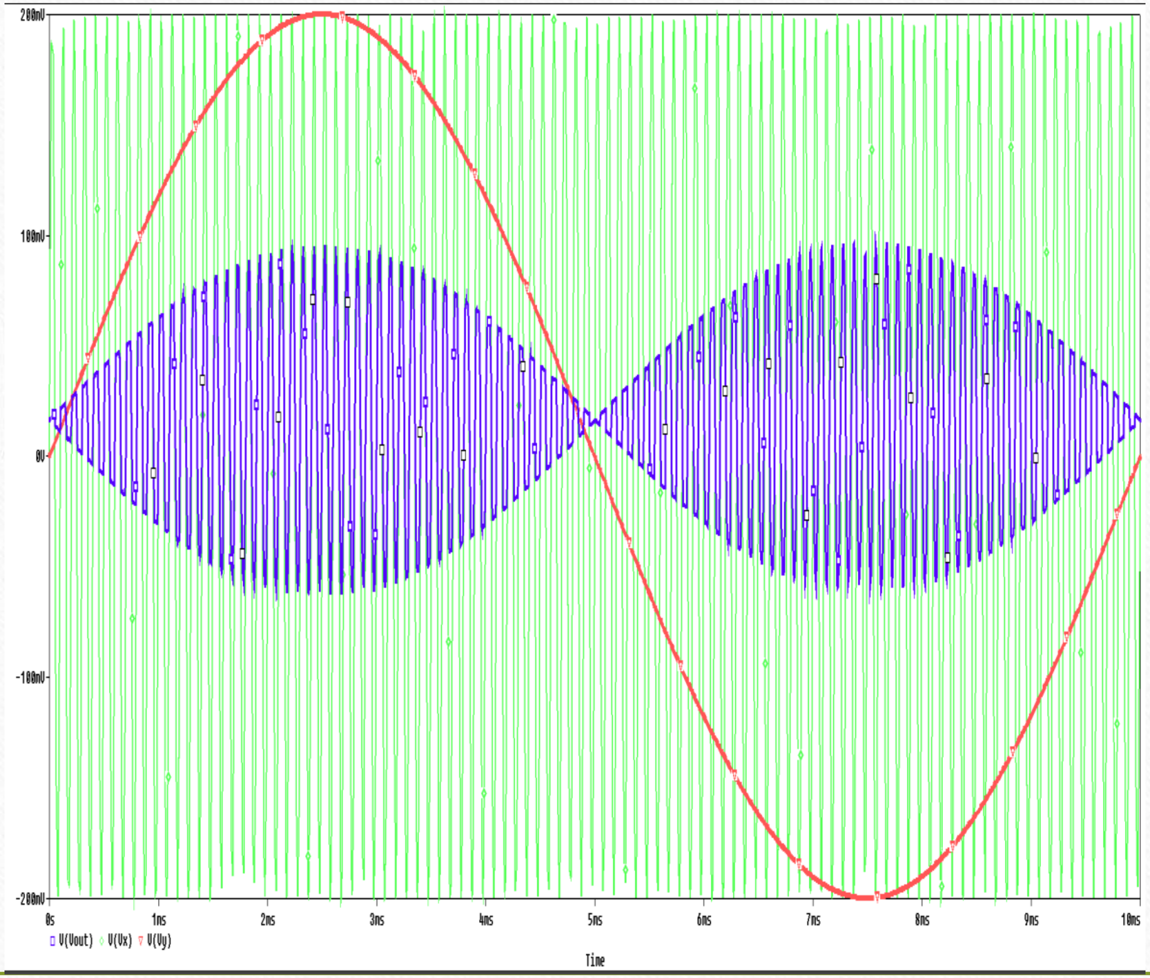


Fig:-Response of multiplier with slowDC input

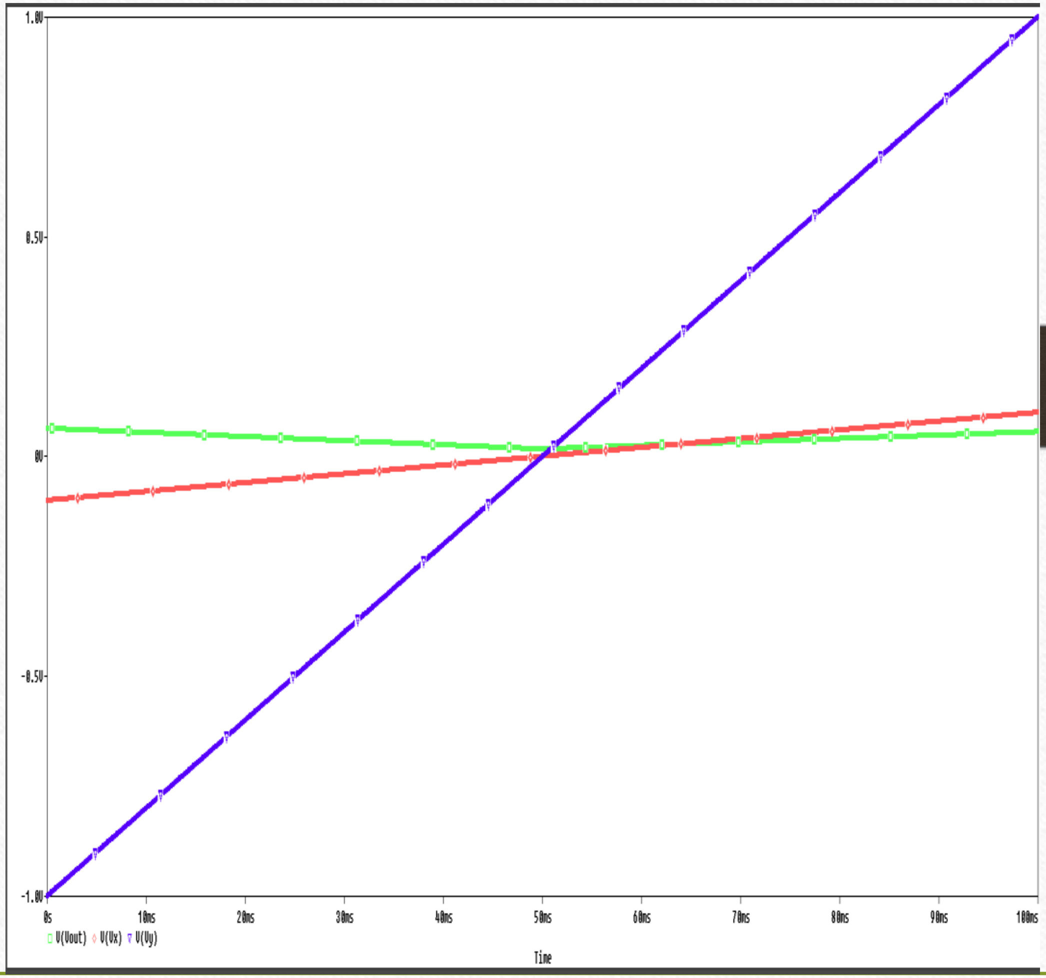
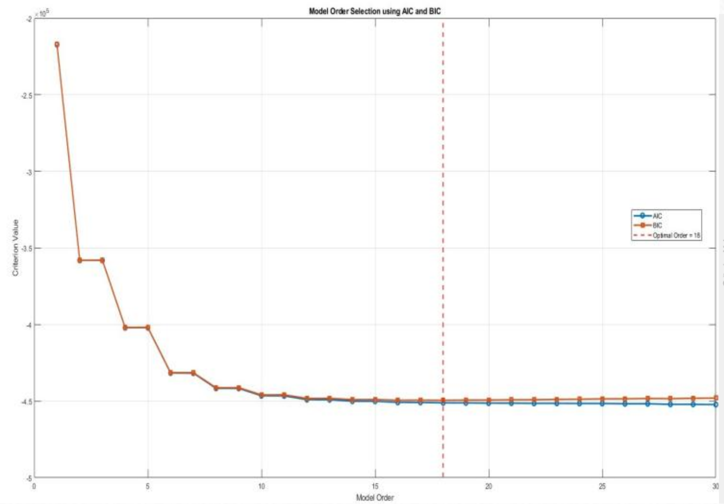
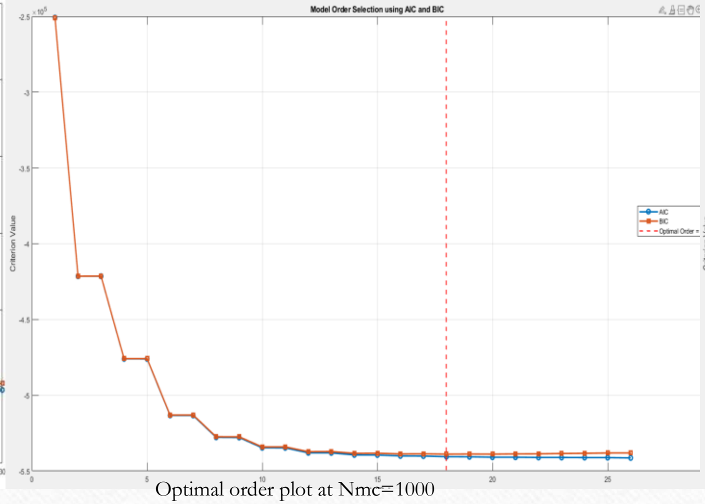


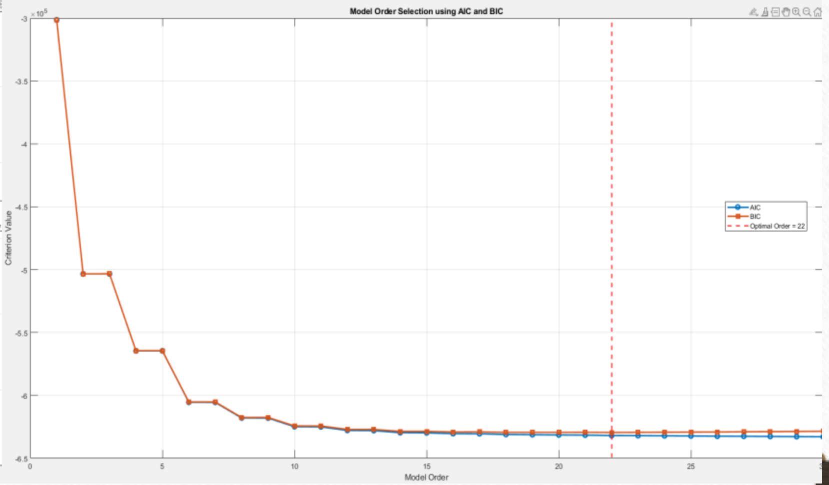
Illustration-3 : Analog Multiplier with sine input

Determination of optimal Order





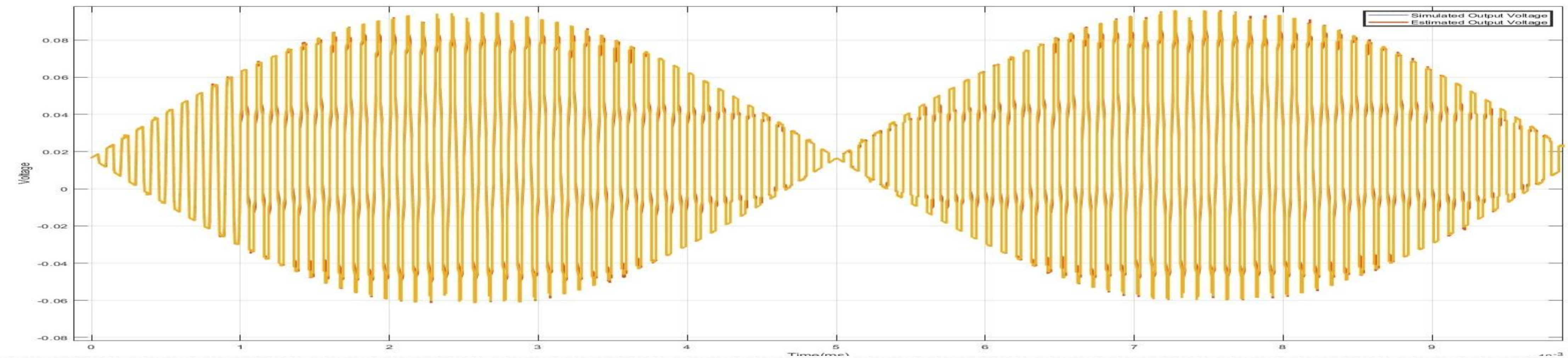
Optimal order plot at Nmc=1000



Optimal order plot at Nmc=2000

Optimal order plot at Nmc=500

Simulated Output VS regression model Output



RESULT

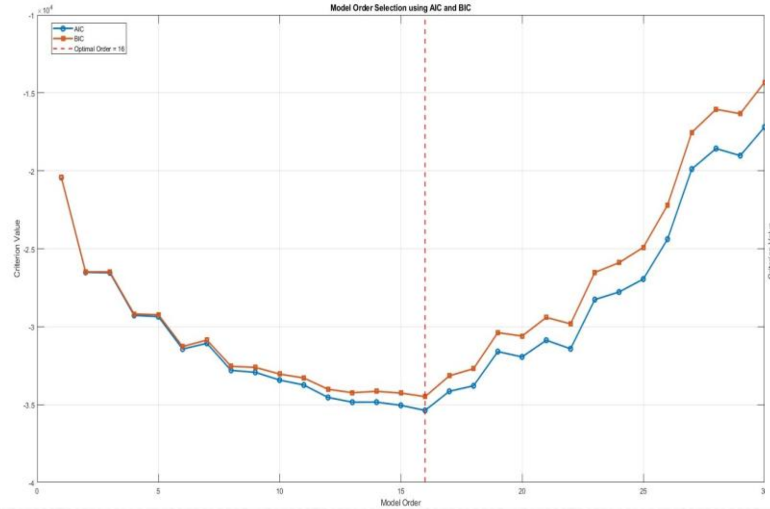
ANALOG MULTIPLIER- in case of AC INPUT(SINE WAVE)						
Various Detected Faults in Analog Multiplier in the presence of faults with deviations (5% – 15%) & (20%-46%)						
Injected Faults	N_{MC}=500, **Avg_dif** = 0.0098 Optimal Order – 18th		N_{MC}=1000, **Avg_dif** = 0.0097 Optimal Order – 18th		N_{MC}=2000, **Avg_dif** = 0.0097 Optimal Order – 22nd	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R11 6%↑	19	√	16	√	23	√
R11 6% ↓	12	√	7	√	12	√
R12 7% ↑	10	√	4	√	23	√
R12 7% ↓	27	√	20	√	64	√
R21 8% ↑	25	√	16	√	12	√
R21 8%↓	15	√	8	√	12	√
R22 9%↑	20	√	15	√	32	√
R22 9% ↓	21	√	17	√	30	√
R31 10% ↑	15	√	12	√	11	√
R31 10% ↓	30	√	30	√	27	√
R32 11% ↑	22	√	15	√	30	√
R32 11% ↓	36	√	30	√	32	√
R41 12% ↑	38	√	35	√	13	√
R41 12% ↓	17	√	15	√	17	√
R42 13% ↑	29	√	18	√	32	√
R42 13% ↓	21	√	8	√	18	√
R51 14% ↑	3	√	5	√	12	√
R51 14% ↓	16	√	16	√	35	√
R52 15% ↑	41	√	38	√	18	√
R52 15% ↓	26	√	24	√	13	√
R11 20% ↑	17	v	9	√	25	√
R11 20% ↓	58	√	37	√	39	√
R12 25% ↑	17	√	14	√	27	√
R12 25% ↓	40	√	20	√	15	√
R21 30% ↑	33	√	28	√	39	√
R21 30% ↓	4	√	3	√	9	√
R22 35% ↑	40	√	27	√	22	√
R22 35% ↓	20	√	20	√	14	√
R31 36% ↑	28	√	27	√	8	√
R31 36% ↓	38	√	26	√	18	√
R32 38% ↑	7	√	7	√	2	√
R32 38% ↓	75	√	57	√	96	√
R41 40% ↑	32	√	23	√	26	√
R41 40% ↓	18	√	10	√	30	√
R42 42% ↑	46	√	44	√	34	√
R42 42% ↓	3	√	4	√	4	√
R51 44% ↑	30	√	26	√	19	√
R51 44% ↓	68	√	58	√	53	√
R52 46% ↑	66	√	65	√	71	√
R52 46% ↓	28	√	24	√	36	√

ANALOG MULTIPLIER- in case of AC INPUT(SINE WAVE)						
Various Detected Faults in Analog Multiplier in the presence of faults with deviations (>5%)						
Injected Faults	N_{MC}=500, **Avg_dif** = 0.0098 Optimal Order – 18th		N_{MC}=1000, **Avg_dif** = 0.0097 Optimal Order – 18th		N_{MC}=2000, **Avg_dif** = 0.0097 Optimal Order – 22nd	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detecti on Status
R11 1%↓	0	X	0	X	1	√
R11 3% ↑	5	√	5	√	0	X
R12 2% ↑	1	√	0	X	0	X
R12 1% ↓	5	√	5	√	5	√
R21 3% ↑	0	X	1	√	0	X
R21 2.5%↓	0	X	0	X	0	X
R22 2%↑	1	√	0	X	0	X
R22 3% ↓	3	√	1	√	0	X
R31 4% ↑	0	X	0	X	0	X
R31 3.5% ↓	3	√	0	X	0	X
R32 1% ↑	1	√	0	X	0	X
R32 3% ↓	7	√	5	√	3	√
R41 2%↑	0	X	0	X	0	X
R41 1%↓	0	X	0	X	0	X
R42 3%↑	3	√	1	√	0	X
R42 1%↓	1	√	1	√	0	X
R51 1.5% ↑	0	X	2	√	1	√
R51 1.8% ↓	2	√	0	X	0	X
R52 2.3% ↑	0	X	0	X	0	X
R52 2.9%↓	0	X	0	X	0	X

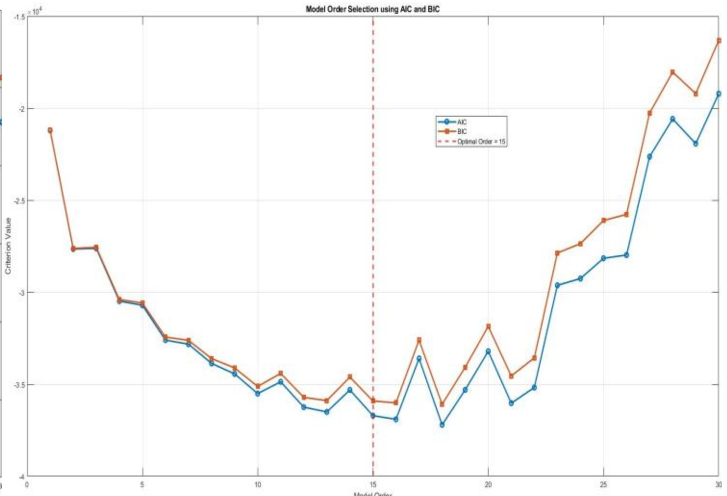
ANALOG MULTIPLIER- in case of AC INPUT(SINE WAVE)						
Various Detected Faults in MULTIPLIER in the presence of MULTIPLE faults with deviations						
Injected Faults	N_{MC}=500, **Avg_dif** = 0.0098 Optimal Order – 18th		N_{MC}=1000, **Avg_dif** = 0.0097 Optimal Order – 18th		N_{MC}=2000, **Avg_dif** = 0.0097 Optimal Order – 22nd	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R11 8%↑ **R12 10% ↑**	15	√	13	√	17	√
R21 20% ↑ **R22 15% ↓**	25	√	21	√	38	√
R31 20% ↓ **R32 20% ↑** **R41 10% ↑**	18	√	17	√	16	√
R52 30%↓ **R51 20% ↑**	21	√	16	√	23	√
R11 15% ↑ **R12 20% ↓** **R42 18 % ↑**	34	√	31	√	55	√

Illustration-4 : Analog Multiplier with DC sweep input

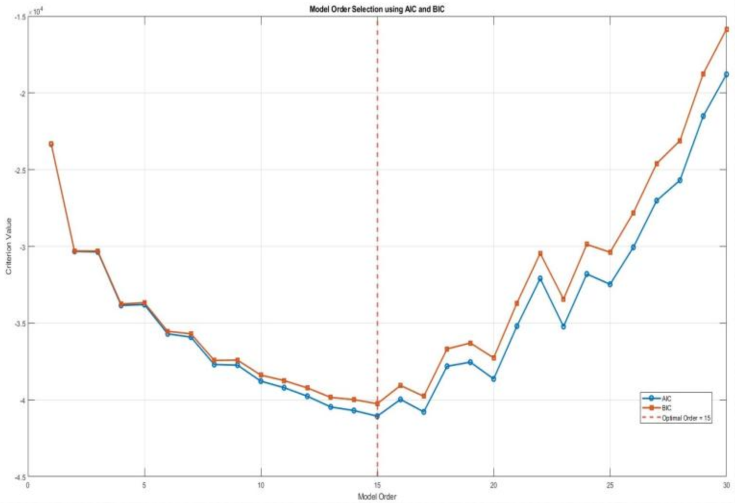
Determination of optimal Order



Optimal order plot at Nmc=500

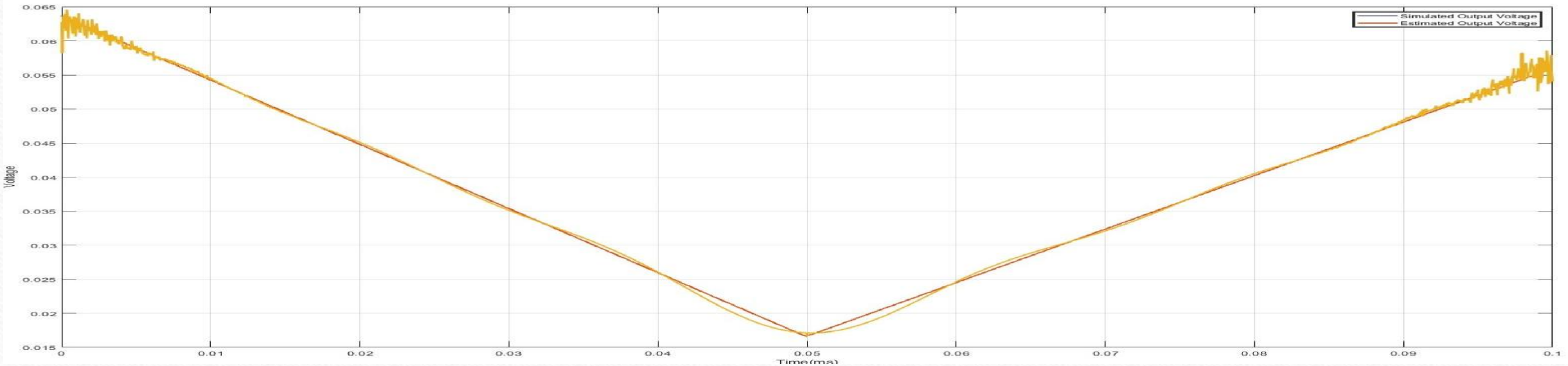


Optimal order plot at Nmc=1000



Optimal order plot at Nmc=2000

Simulated Output VS regression model Output



RESULT

ANALOG MULTIPLIER - in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)						
Various Detected Faults in Analog Multiplier in the presence of faults with deviations (5% – 15%) & (20%-46%)						
Injected Faults	N_{MC}=500, **Avg_dif** = 0.0103 Optimal Order - 16th		N_{MC}=1000, **Avg_dif** = 0.0108 Optimal Order - 15th		N_{MC}=2000, **Avg_dif** = 0.0110 Optimal Order - 15th	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R11 6%↑	10	√	12	√	3	√
R11 6% ↓	2	√	8	√	2	√
R12 7% ↑	4	√	3	√	2	√
R12 7% ↓	6	√	9	v	5	√
R21 8% ↑	2	√	4	√	2	√
R21 8%↓	12	√	13	√	2	√
R22 9%↑	12	√	8	√	2	√
R22 9% ↓	1	√	3	√	0	X
R31 10% ↑	8	√	7	√	2	√
R31 10% ↓	6	√	8	√	2	√
R32 11% ↑	2	√	7	√	3	√
R32 11% ↓	10	√	6	√	3	√
R41 12% ↑	5	√	7	√	2	√
R41 12% ↓	5	√	13	√	2	√
R42 13% ↑	10	√	8	√	4	√
R42 13% ↓	1	√	4	√	3	√
R51 14% ↑	1	√	2	√	0	X
R51 14% ↓	13	√	12	√	4	√
R52 15% ↑	12	√	14	√	7	√
R52 15% ↓	1	√	3	√	0	X
R11 20% ↑	13	√	16	√	9	√
R11 20% ↓	1	√	2	√	0	X
R12 25% ↑	1	√	2	√	0	X
R12 25% ↓	28	√	43	√	28	√
R21 30% ↑	3	√	6	√	2	√
R21 30% ↓	15	√	25	√	10	√
R22 35% ↑	16	√	22	√	10	√
R22 35% ↓	5	√	4	√	5	√
R31 36% ↑	9	√	11	√	7	√
R31 36% ↓	3	√	2	√	1	√
R32 38% ↑	2	√	4	√	1	√
R32 38% ↓	22	√	46	√	35	√
R41 40% ↑	3	√	5	√	1	√
R41 40% ↓	13	√	12	√	9	√
R42 42% ↑	19	√	23	√	13	√
R42 42% ↓	2	√	3	√	1	√
R51 44% ↑	3	√	4	√	3	√
R51 44% ↓	60	√	68	√	57	√
R52 46% ↑	42	√	30	√	30	√
R52 46% ↓	5	√	9	√	3	√

ANALOG MULTIPLIER - in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)						
Various Detected Faults in Analog Multiplier in the presence of faults with deviations (< 5%)						
Injected Faults	N_{MC}=500, **Avg_dif** = 0.0103 Optimal Order - 16th		N_{MC}=1000, **Avg_dif** = 0.0108 Optimal Order - 15th		N_{MC}=2000, **Avg_dif** = 0.0110 Optimal Order - 15th	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R11 1%↓	0	X	0	X	1	√
R11 3% ↑	8	√	8	√	2	√
R12 2% ↑	1	√	0	X	1	√
R12 1% ↓	7	√	5	√	2	√
R21 3% ↑	0	X	1	√	3	√
R21 2.5%↓	0	X	1	√	1	√
R22 2%↑	1	√	2	√	3	√
R22 3% ↓	3	√	1	√	1	√
R31 4% ↑	0	X	0	X	3	√
R31 3.5% ↓	3	√	6	√	1	√
R32 1% ↑	1	√	0	X	0	X
R32 3% ↓	8	√	10	√	3	√
R41 2%↑	0	X	0	X	0	X
R41 1%↓	0	X	0	X	1	√
R42 3%↑	3	√	1	√	2	√
R42 1%↓	1	√	1	√	1	√
R51 1.5% ↑	0	X	2	√	1	√
R51 1.8% ↓	3	√	0	X	2	√
R52 2.3% ↑	0	X	0	X	1	√
R52 2.9%↓	0	X	0	X	0	X

	Optimal Order - 16th		Optimal Order - 15th		Optimal Order - 15th	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R11 8%↑ R12 10% ↑	5	√	6	√	3	√
R21 20% ↑ R22 15% ↓	6	√	5	√	2	√
R31 20% ↓ R32 20% ↑ R41 10% ↑	23	√	13	√	5	√
R52 30%↓ R51 20% ↑	5	√	5	√	7	√
R11 15% ↑ R12 20% ↓ R42 18 % ↑	78	√	57	√	37	√

Case Study-3: PI Compensator of a Buck Converter

- It is the peak current-mode controlled DC-DC Buck converter using PWM control IC UC3843.
- A key functional block of this controller is the PI compensator (shown in Fig.), which is built using an error amplifier.
- The output voltage (Vout) is divided by the resistor dividetr network (Rf1 and Rf2) and then fed to the error amplifier

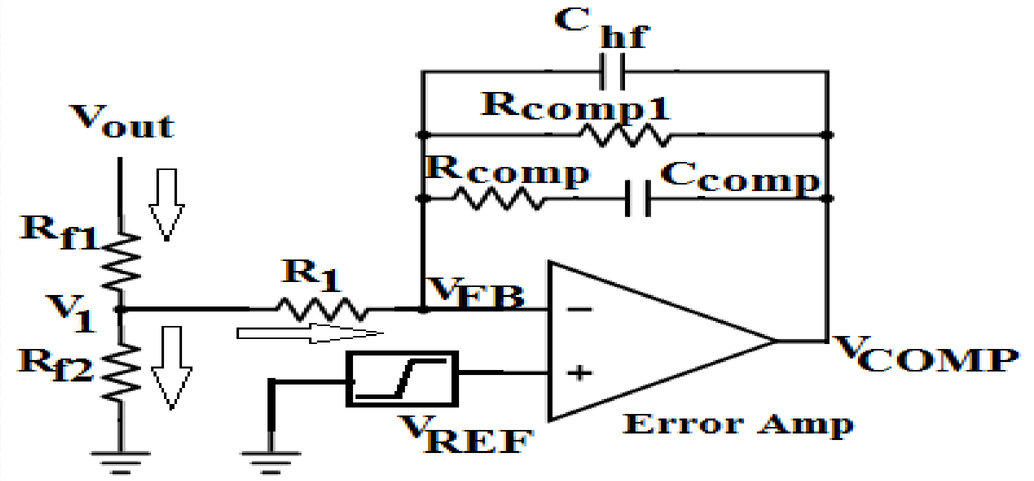


Fig.. PWM controller circuit of buck converter

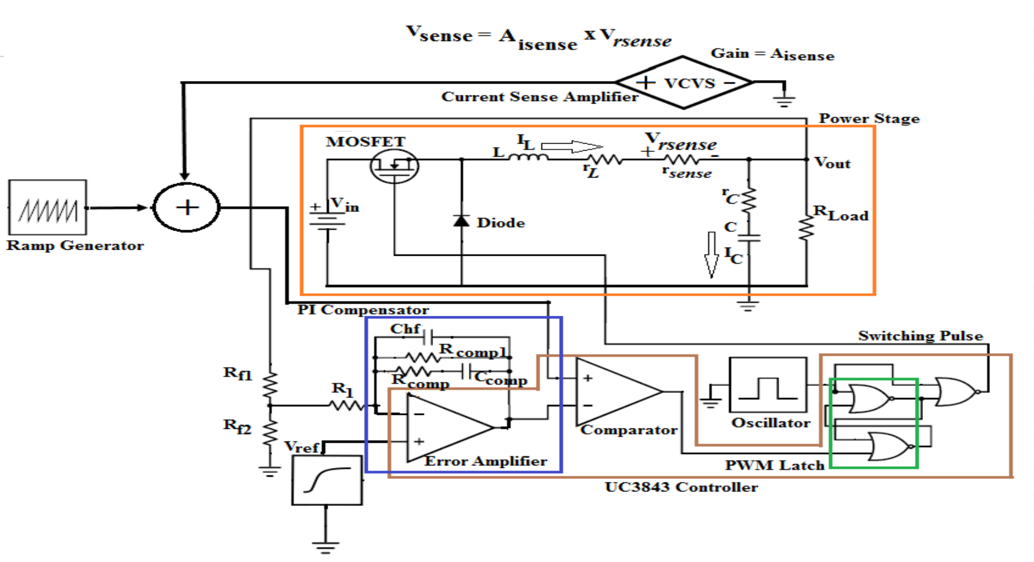


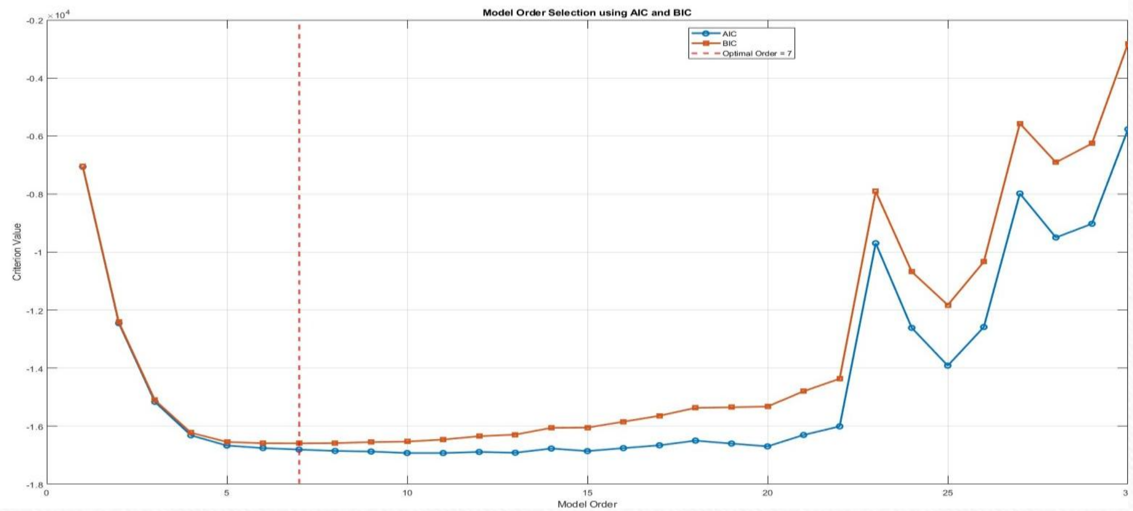
Fig.. Schematic of a current programmed control buck converter

- The controller is crucial to maintain a constant output voltage.
- Therefore, the controller circuit must be properly designed and tested.
- In this study, we focus on parametric fault detection in the controller part of the Buck converter circuit.

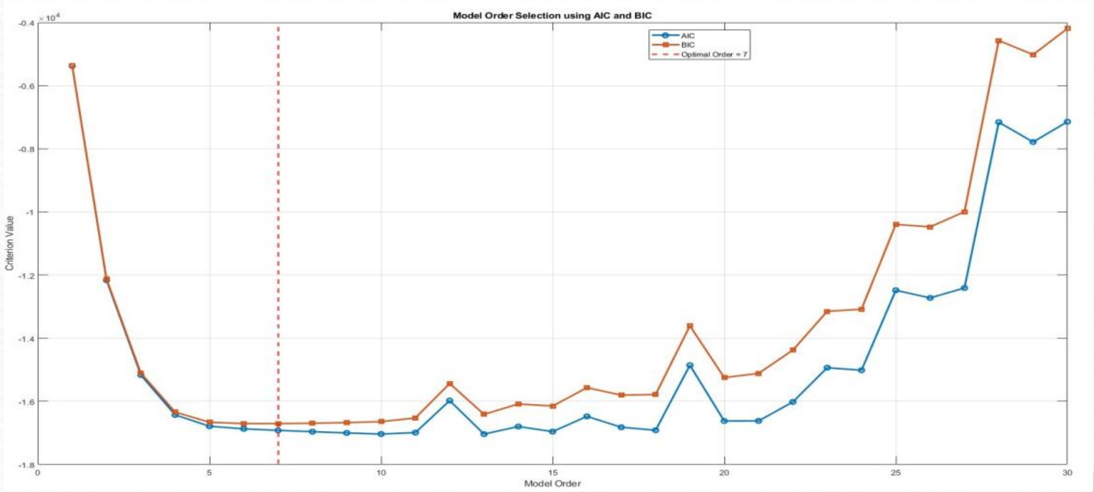
The nominal values are:-R_{f1}=9.76 kΩ, R_{f2}=3.25 kΩ, R_1=1kΩ, C_{hf}=30pF, C_{comp}=2nF, R_{comp1} =10 MΩ, R_{comp}=80 kΩ

Illustration-5 : PI Compensator of a Buck Converter

Determination of optimal Order

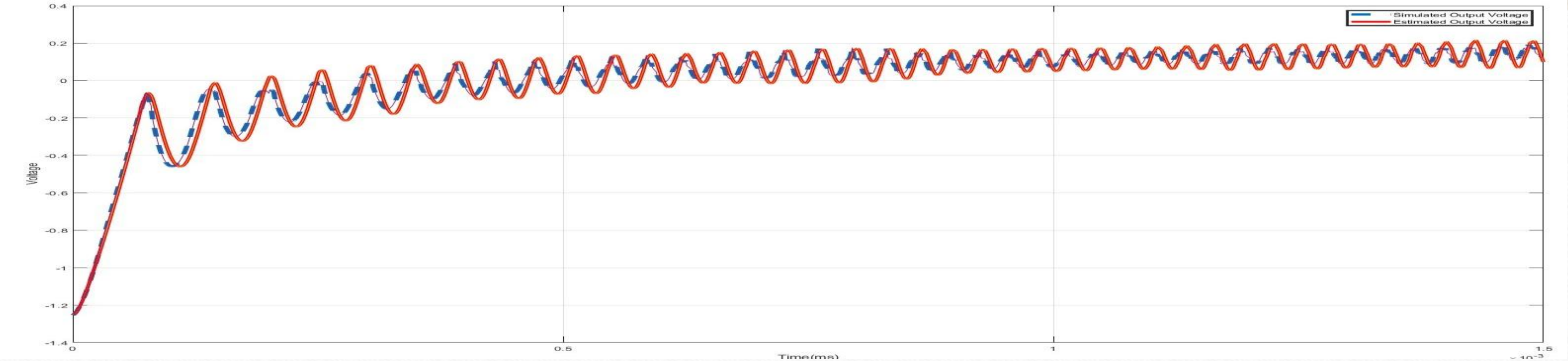


Optimal order plot at Nmc=500



Optimal order plot at Nmc=1000

Simulated Output VS regression model Output



RESULT

PI COMPENSATOR OF A BUCK CONVERTER

Various Detected Faults PI controller in the presence of faults with deviations (5% – 15%) & (20%-50%)

Injected Faults	N_{MC}=500				N_{MC}=1000			
	Optimal Order – 6th, Avg_dif =0.0162		Optimal Order – 7th, Avg_dif =0.0161		Optimal Order – 6th, Avg_dif =0.0164		Optimal Order – 7th, Avg_dif =0.0162	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R1 6% ↑	0	X	1	√	0	X	6	√
R1 5.5% ↓	0	X	1	√	0	X	26	√
Rf2 5.8% ↑	0	X	28	√	0	X	27	√
Rf2 6% ↓	5	√	35	√	5	√	1	√
Rf1 7% ↑	0	X	3	√	0	X	1	√
Rf1 8.5% ↓	0	X	4	√	0	X	32	√
Rcomp 9% ↑	20	√	33	√	16	√	25	√
Rcomp 6.8% ↓	26	√	16	√	26	√	35	√
Rcomp1 7.5%↑	0	X	1	√	0	X	15	√
Rcomp1 5.6%↓	0	X	1	√	0	X	35	√
Chf 8% ↑	18	√	27	√	3	√	2	√
Chf 10 % ↓	0	X	0	X	0	X	35	√
Ccomp 6% ↑	1	√	2	√	1	√	7	√
Ccomp 6% ↓	0	X	1	√	0	√	25	√
R1 43% ↑	1	√	2	√	1	√	5	√
R1 28% ↓	1	√	2	√	1	√	35	√
Rf2 35% ↑	22	√	7	√	18	√	35	√
Rf2 40% ↓	18	√	1	√	0	X	36	√
Rf1 30% ↑	26	√	33	√	26	√	35	√
Rf1 25% ↓	27	√	33	√	27	√	35	√
Rcomp 42% ↑	0	X	24	√	0	X	18	√
Rcomp 38% ↓	0	X	1	√	0	X	35	√
Rcomp1 37%↑	28	√	35	√	28	√	15	√
Rcomp1 40%↓	27	√	36	√	27	√	13	√
Chf 28% ↑	0	X	1	√	0	X	8	√
Chf 35% ↓	0	X	1	√	0	X	35	√
Ccomp 32% ↑	27	√	35	√	27	√	35	√
Ccomp 45%↓	28	√	36	√	28	√	34	√

PI COMPENSATOR OF A BUCK CONVERTER

Various Detected Faults PI controller in the presence of faults with deviations (≥5%)

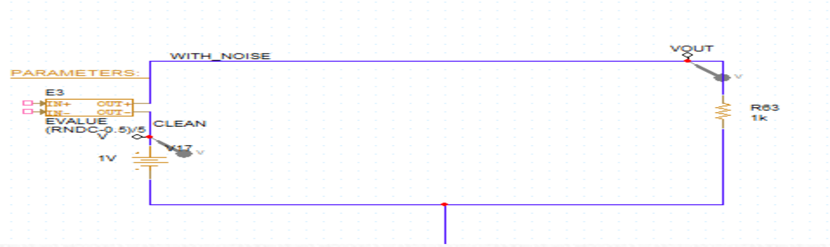
Injected Faults	N_{MC}=500				N_{MC}=1000			
	Optimal Order – 6th, Avg_dif =0.0162		Optimal Order – 7th, Avg_dif =0.0161		Optimal Order – 6th, Avg_dif =0.0164		Optimal Order – 7th, Avg_dif =0.0162	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
Rf1 2%↓	0	X	0	X	0	X	0	X
Rf2 1% ↑	0	X	14	√	0	X	14	√
R1 3% ↑	0	X	0	X	0	X	1	√
Chf 3% ↓	0	X	12	√	0	X	14	√
Rcomp1 2.5% ↑	0	X	34	√	0	X	12	√
Rcomp 3.5% ↓	0	X	0	X	0	X	0	X
Ccomp2% ↑	0	X	15	√	0	X	11	√
R1 2% ↓	0	X	0	X	0	X	0	X
Rcomp1 1.5% ↓	0	X	0	X	0	X	1	√
Rcomp 2%↑	0	X	0	X	0	X	0	X

PI COMPENSATOR OF A BUCK CONVERTER

Various Detected Faults PI controller in the presence of MULTIPLE faults with deviations

Injected Faults	N_{MC}=500				N_{MC}=1000			
	Optimal Order – 6th, Avg_dif =0.0162		Optimal Order – 7th, Avg_dif =0.0161		Optimal Order – 6th, Avg_dif =0.0164		Optimal Order – 7th, Avg_dif =0.0162	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
Ccomp 10%↓ Chf 20%↑ R1 12%↓	24	√	24	√	24	√	36	√
R1 11%↓ Rcomp1 22%↑ Rcomp=13 %↓	27	√	35	√	27	√	35	√
Rcomp1 9%↓ Rcomp= 13%↑ Rf1 18% ↑ Rf2 8% ↓	4	√	0	X	1	√	35	√
Ccomp 15%↓ Chf 11%↑ Rf1 9% ↓ Rf2 19% ↑	3	√	2	√	2	√	36	√
R1 8%↑ Rf1 12% ↓ Rf2 14% ↑	27	√	35	√	27	√	34	√

NOISE ANALYSIS



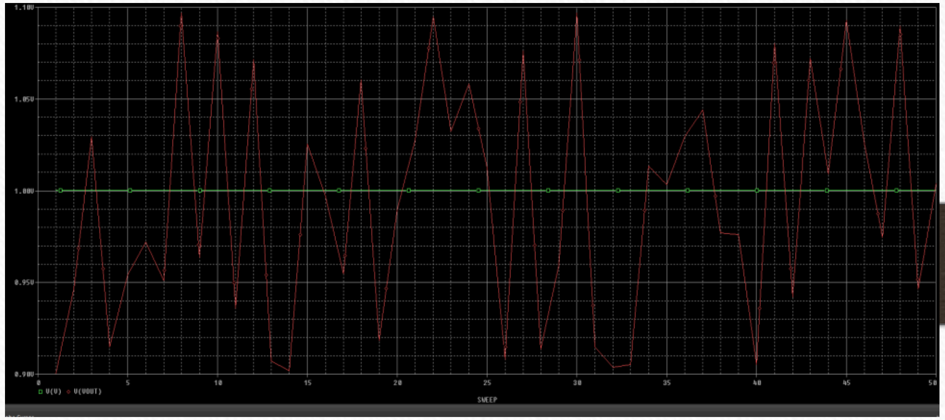
🔷 Why Simulate Noise?

•Real-world circuits are affected by **transient and steady-state noise**.
•Noise impacts behavior, performance, and fault detectability.
•Simulating noise improves **test robustness**.

🔶 Noise Simulation Techniques

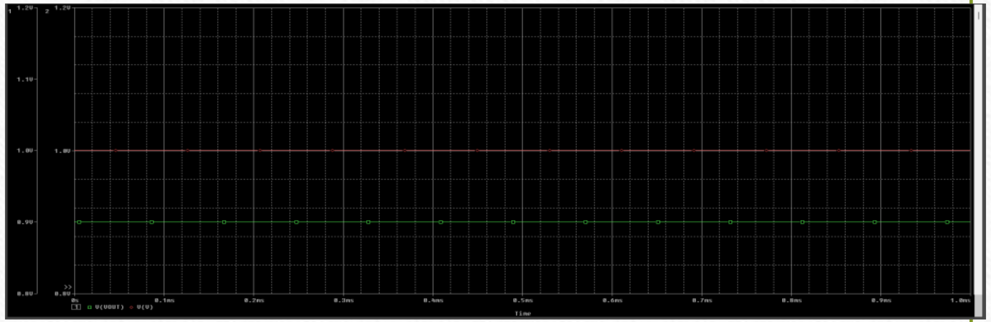
1. Random Noise Source

•Add a voltage/current source with a defined DC value and noise amplitude.
•Simulates real-time fluctuations at each time step.
•Example: 1V ± 0.2V generates a range from 0.9V to 1.1V.



2. RNDR Function (Transient/DC Analysis)

•Injects a constant random value for the full simulation.
•Example: (RNDR - 0.5)/5 → adds ±0.1V random offset.



3. RNDC Function (Sweeps/Monte Carlo)

•Generates different random values per sweep.
•Useful for Monte Carlo, DC Sweep, Temperature Analysis.

COMPARISON

LEADLAG - in case of AC INPUT(SINE WAVE) with NOISE of 0.15mV					
Various Detected Faults in LEADLAG in the presence of faults with deviations (5% – 15%) & (20%-47%)					
N_{MC}=500, Avg_dif = 0.0420, Optimal Order – 18th					
Injected Faults		WITHOUT NOISE		WITH NOISE	
		No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R1 12%↑		113	√	151	√
R1 8% ↓		1	√	73	√
R2 9% ↑		0	X	63	√
R2 6% ↓		0	X	64	√
R3 10% ↑		71	√	61	√
R3 7%↓		0	X	100	√
C1 13%↑		0	X	66	√
C1 15% ↓		3	√	63	√
C2 11% ↑		0	X	62	√
C2 14% ↓		10	√	71	√
R1 20%↑		163	√	170	√
R1 30% ↓		183	√	179	√
R2 32% ↑		34	√	73	√
R2 40% ↓		104	√	124	√
R3 25% ↑		174	√	161	√
R3 45% ↓		185	√	182	√
C1 42% ↑		17	√	77	√
C1 25% ↓		15	√	72	√
C2 35% ↑		38	√	72	√
C2 47% ↓		140	√	149	√

CONCLUSION

- ❑ **Polynomial regression is effective for analog fault testing across both linear and non-linear circuits.**

- ❑ **Fault detection is accurate for:**
  - **Single faults**: Detected reliably at deviations **> ±5%** (within expected design tolerances).
  - **Multiple faults**: Also successfully detected when two or more components deviate beyond tolerance.

- ❑ **For deviations ≤ ±5%**, faults are **not flagged**, as this lies within the allowable tolerance margin set during Monte Carlo construction.

- ❑ **Higher polynomial orders** improve detection capability but may introduce complexity or overfitting.

- ❑ **Noise Robustness:**
  - Verified using RNDR/RNDC noise sources in OrCAD PSpice.
  - Compared coefficients under noisy and clean conditions.

Future Work

- **Fault Diagnosis (Not Just Detection)**
  - Extend current approach to identify *which* component is faulty, not just detect that a fault exists.
  - Use sensitivity ranking and component-wise coefficient deviation tracking.
- **Advanced Noise Modeling**
  - Simulate real-world noise sources including thermal drift, EMI, and fluctuating power supply noise.
  - Analyze model stability under high-noise, low-SNR environments.
- **Integration with Machine Learning**
  - Combine polynomial features with ML classifiers (e.g. Decision Trees, SVMs) to detect and categorize multiple fault types
- **Toolchain Automation**
  - Build a Python/MATLAB-based GUI or pipeline to automate tentire flow: Circuit → Simulation → Regression → Fault Report

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Thank You