FAULT DETECTION IN MULTI-INPUT ANALOG CIRCUITS USING POLYNOMIAL REGRESSION MODELLING

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CANDIDATE'S DECLARATION

We hereby declare that

a. The work contained in this report is original and has been done by us under the guidance of our supervisor **Dr. Rahul Bhattacharya***,* Professor, Department of Electronics Engineering, IIT(ISM) Dhanbad.

b. The work has not been submitted to any other Institute for any degree or diploma.

c. I have followed all the guidelines provided by the Institute in preparing the report.

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e. Wherever I have used materials (data, theoretical analysis, figures and texts) from other sources, I have given due credit to them by citing them in the project report and giving their details in the reference. Further I have taken permission from the copyright owners of the sources, wherever necessary.

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SIMRAN GUPTA

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CERTIFICATE

This is to certify that the project report titled **"Fault Detection in Multi-Input Analog Circuits Using Polynomial Regression Modelling"**, submitted by **Simran Gupta** to the **Indian Institute of Technology (Indian School of Mines)**, in fulfilment of the Summer Research Internship, is a bonafide record of the research work carried out under my supervision.
To the best of my knowledge, the contents of this report, in full or in part, have not been submitted to any other institute or university for the award of any degree or diploma.

Examined and Approved

Faculty Supervisor **Head of Department (ECE)**

ACKNOWLEDGEMENT

This research work is one of the significant achievements in my life and is made possible because of the unending encouragement and motivation given by so many in every part of my life. It is immense pleasure to have this opportunity to express my gratitude and regards to them.

Firstly, I would like to express my gratitude and sincere thanks to my supervisor **Dr. Rahul Bhattacharya**, Department of Electronics Engineering for his esteemed supervision and guidance during the tenure of my project work. His insights and support were instrumental in shaping this research.

I also extend my sincere thanks to the Department of Electronics Engineering, IIT (ISM) Dhanbad, for providing the resources, environment, and infrastructure necessary to carry out this work successfully.

Simran Gupta

CONTENTS

Abstract

This report presents a comprehensive methodology for detecting single parametric faults in multi-input Analog circuits using polynomial regression modelling. Analog circuits, especially in mixed-signal systems, are notoriously difficult to test due to nonlinear behaviour, limited test access, and high sensitivity to manufacturing variations. Traditional specification-based methods often fall short in cost-efficiency and fault coverage. To address these challenges, this work proposes a regression-based fault detection approach wherein the output of the circuit under test (CUT) is expressed as a polynomial function of multiple input variables, derived through Taylor series expansion.

The coefficients of this polynomial model are computed using traditional least squares techniques, and fault-free (FF) coefficient bounds are established via Monte Carlo simulations under nominal tolerance variations. During testing, any deviation of the estimated coefficients beyond these predefined FF bounds is indicative of a parametric fault

The methodology is validated through three case studies involving both linear and nonlinear Analog circuits: a lead-lag filter, a four-quadrant Analog multiplier, and a PI compensator in a buck converter. Each circuit is evaluated under sine and slow ramp (DC sweep) input conditions. Results confirm that the proposed technique reliably detects single parametric faults—including small deviations—with high accuracy, even in the presence of additive noise. The approach thus demonstrates strong potential as a low-cost, simulation-based test framework for Analog and mixed-signal fault detection.

Chapter 1

INTRODUCTION

1.1 OVERVIEW

The testing and diagnosis of Analog circuits are central challenges in the post-manufacturing validation phase of electronic systems. Unlike digital circuits, Analog circuits do not possess straightforward fault models such as stuck-at faults. Analog behaviour is sensitive to manufacturing process variations and environmental influences, making fault detection and classification both critical and complex.

Due to the wide range of applications of electronic circuits in recent years, testing of electronic circuits, especially Analog circuits, has become a major concern in ensuring fault-free systems. The absence of a standard Analog fault model comparable to the digital stuck-at model complicates the testing process. Analog fault models are generally categorized as either catastrophic or parametric faults. Several techniques for Analog fault detection have been proposed in literature, with surveys highlighting high-tech approaches for diagnosis and classification.

Declaring when a circuit or component is faulty remains a challenging decision in Analog testing. Parametric fault diagnosis and tolerance are especially difficult because component variations may not cause total circuit failure but lead to degraded or incorrect functionality. C. Yang et al. approached soft fault diagnosis by estimating circuit parameters using test stimulus responses and slope fault models. In a related work, genetic algorithms were employed to identify faulty components by analyzing the transfer function and bounding behaviour.

A variety of parametric detection methods exist, including those that evaluate probability density functions (Bhattacharyya coefficients), impulse responses, and regression-based models. Notably, Z. Guo and J. Savir used auto-regression models to predict and compare coefficients, while others have applied machine learning, such as support vector machines and manifold learning, for classification. T. Zhang and T. Li even used noise signatures as diagnostic features.

Various frequency response-based techniques also exist. For example, signal flow graph (SFG) analysis has been used to simulate faults and derive tolerances. The Levenberg-Marquardt method and k-nearest neighbors (K-NN) classifiers have also been used in fault classification based on natural frequency and gain.

Despite significant research, most approaches are limited to single-input, single-output Analog systems such as Sallen Key filters, low pass filters, leapfrog filters, or elliptic filters. These typically involve op-amps in single-ended configurations with grounded non-inverting inputs. However, modern Analog systems often feature double-ended operation and limited test access, making internal fault detection challenging.

A promising direction is regression-based signature analysis, where the circuit output is expressed as a polynomial function of multiple input voltages. The coefficients of this polynomial, estimated using classical linear least squares techniques, serve as fault signatures. Taylor series expansions help derive these polynomial models. The addition of the V-Transform method, which amplifies fault sensitivity by modifying coefficients into monotonic exponential forms, further improves diagnostic capability.

This report proposes and validates a novel methodology using polynomial regression and V-Transform for fault detection in multi-input Analog circuits. Multiple input conditions, including sine and DC sweep signals, are analyzed, and the effects of noise are also incorporated to evaluate model robustness.

1.2 MOTIVATION

Despite extensive efforts in Analog fault detection research, several critical challenges persist, motivating the need for this study:

1. Lack of Standard Fault Models: Unlike digital systems, Analog circuits lack simple and standardized fault models. Each component's deviation must be analyzed individually.
2. Complex Fault Behaviour: Analog faults do not typically manifest as binary outcomes but influence circuit behaviour in continuous and complex ways. This includes shifts in gain, offset, or bandwidth.
3. Limited Observability: Many practical Analog circuits have restricted nodes for measurement. With limited probing access, internal faults are difficult to observe and diagnose.
4. High Cost of Accurate Testing: Creating high-precision Analog test equipment is expensive and often not scalable across diverse circuit topologies.
5. Insufficiency of Single-Input Approaches: Most existing methods cater to single-input Analog circuits. However, real-world applications frequently involve multi-input configurations that require more sophisticated analysis.

To address these issues, this work explores polynomial regression modelling of multi-input circuits, combining classical estimation with V-Transform-based sensitivity analysis. By simulating the tolerance range of each circuit parameter using Monte Carlo (MC) simulations, the fault-free bounds for each regression coefficient are established. During testing, coefficients computed from faulty conditions are compared with these bounds. Any significant deviation is flagged as a fault.

The report further extends this methodology to nonlinear Analog circuits such as four-quadrant multipliers and switching converter controllers. The inclusion of V-Transform coefficients increases sensitivity to component drift and helps distinguish genuine faults from natural parameter variation or noise. Ultimately, this regression-based technique aims to deliver an accessible, simulation-based, non-invasive, and highly adaptable fault detection solution for Analog and mixed-signal systems.

1.3 LITERATURE REVIEW

A wide array of methodologies has been proposed over the years for Analog fault detection. The earliest approaches were predominantly specification-based, focusing on checking whether a circuit's output met predefined parameters. While these methods were effective for simpler circuits, they proved insufficient for complex or sensitive Analog systems.

Later advancements introduced model-based testing, statistical fault detection, and signal analysis techniques. Notably, slope-based models as proposed by C. Yang used the rate of change in response signals to identify faults. Genetic algorithms and soft computing methods also emerged as diagnostic tools for identifying faulty elements through optimization and pattern matching.

Among statistical techniques, regression-based models became popular due to their ability to model circuit behaviour with compact polynomial signatures. Z. Guo and J. Savir, for instance, employed autoregressive (AR) models to detect parameter shifts in circuit output. More sophisticated machine learning classifiers such as support vector machines (SVMs), manifold learning, and K-nearest neighbours (KNN) have also been applied, offering promising results for fault classification.

Additionally, Bhattacharyya coefficient-based approaches have been used for fault detection by measuring differences in probability distributions under fault-free and faulty conditions. T. Zhang and T. Li demonstrated the use of noise signatures as reliable indicators of Analog faults.

Frequency-based methods were explored by Kavithamani et al., who used frequency response shifts to identify parametric deviations. SFG (Signal Flow Graph) methods and Levenberg-Marquardt optimization have also been applied to model behaviour under fault conditions.

Despite these innovations, many techniques have focused on single-input, single-output systems such as low-pass filters, Sallen-Key circuits, and elliptic filters. These configurations do not reflect the operational complexity of modern Analog systems that often involve multi-input circuits and nonlinear behaviour.

The current work builds upon previous polynomial-based methods and expands their applicability to multi-input Analog systems. The methodology uses Taylor series expansion and least squares regression to model output as a function of multiple inputs, with V-Transform coefficients enhancing sensitivity to subtle parameter changes. Unlike many earlier studies, the proposed approach incorporates Monte Carlo-based FF bounds, rigorous polynomial degree selection (AIC/BIC), and testing under noisy conditions to ensure robustness and reliability

Chapter 2

THEORETICAL STUDY

2.1 — Theory of Multiple Linear Regression

The output V_{out} of an Analog circuit can be expressed as a polynomial using a Taylor series expansion [22] in terms of two input voltage sources, V_{in1}, and V_{in2} about the nominal values $V_{in1} = V_1$ and $V_{in2} = V_2$ as follows:

$$V_{out} = f(V_{in1}, V_{in2}) = f(V_1, V_2) + (V_{in1} - V_1).f_1(V_1, V_2) + (V_{in1} - V_2).f_2(V_1, V_2)$$

$$+\frac{1}{2!}\{(V_{in1} - V_1)^2.f_{11}(V_1, V_2) + 2.(V_{in1} - V_1).(V_{in2} - V_2).f_{12}(V_1, V_2)+(V_{in2} - V_2)^2.f_{22}(V_1, V_2)\}$$

$$+\frac{1}{3!}\{(V_{in1} - V_1)^3.f_{111}(V_1, V_2)+3.(V_{in1} - V_1)^2.(V_{in2} - V_2).f_{112}(V_1, V_2)$$

$$+3.(V_{in1} - V_1).(V_{in2} - V_2)^2.f_{122}(V_1, V_2)+(V_{in2} - V_2)^3.f_{222}(V_1, V_2)\}+ \ldots\ldots \quad (1)$$

Where $f(V_{in1}, V_{in2})$ and all its partial derivatives $f_1 \equiv \frac{\partial f}{\partial V_{in1}}, f_2 \equiv \frac{\partial f}{\partial V_{in2}}, f_{11} \equiv \frac{\partial^2 f}{\partial {V_{in1}}^2}, f_{22} \equiv \frac{\partial^2 f}{\partial {V_{in2}}^2}, f_{12} \equiv \frac{\partial^2 f}{\partial V_{in1}.\partial V_{in2}}$ and so on are continuous and exist at nominal values $V_{in1} = V_1$ and $V_{in2} = V_2$.

So, the Taylor polynomial which can represent V_{out} around the nominal values $V_{in1} = V_1$ and $V_{in2} = V_2$ can be generalized up to its m^{th} degree term as follows.

$$V_{out} = f(V_{in1}, V_{in2}) = \sum_{i=0}^{m} \sum_{j=0}^{m-i} \frac{\frac{\partial^{(i+j)} f(V_1, V_2)}{\partial {V_{in1}}^i . \partial {V_{in2}}^j}}{i!j!} (V_{in1} - V_1)^i (V_{in2} - V_2)^j \quad (2)$$

Eqn. (1) can be further approximated as

$$V_{out} = f(V_{in1}, V_{in2}) = a_0 {V_{in1}}^m + a_1 {V_{in1}}^{m-1} V_{in2} + a_2 {V_{in1}}^{m-1} + a_3 {V_{in1}}^{m-2} {V_{in2}}^2 + \ldots\ldots\ldots + \varepsilon \quad (3)$$

Eqn. (3) can be further generalized as follows.

$$V_{out} = \sum_{k=0}^{m} {V_{in1}}^{m-k} \sum_{i=0}^{k} a_{r+i} {V_{in2}}^i + \varepsilon \quad (4)$$

Where r = $\frac{k(k+1)}{2}$ and a_0, a_1, a_2 etc. are the real-valued coefficients $\forall$ i = 0 to k and $\forall$ k = 0 to m. ε is the truncation error. The number of coefficients for an m[th] degree polynomial regression model which can estimate the output of a two-input CUT can be given as

$$N_{coeff} = \frac{(m+1)(m+2)}{2} \quad (5)$$

The coefficients a_i's in Eqn. (3) cannot be exact to that of Eqn. (1), as Eqn. (3) comprises only a finite number of terms for what is essentially a truncated Taylor series. Eqn. (3) is a linear regression model that describes the relationship between circuit output voltage V_{out} and two input voltages, V_{in1} and V_{in2}. Judicious selection of the coefficients a_0 and a_i's of a polynomial regression model in Eqn. (3) using traditional linear least squares techniques minimizes truncation error ε. The accuracy of the regression model depends on the degree of the polynomial expansion used in practice. The traditional methods in MATLAB to estimate a linear regression model. This work uses MATLAB Polyfitn library to solve the coefficients of a polynomial regression model using classical linear least square techniques. Several numerical methods are used to implement the *Polyfitn* library. However, to obtain a more stable solution, reasonably efficient QR factorization with pivoting is introduced to build the *Polyfitn* library. Any multi-input analog circuit, in general, can be represented using this model. The technique applies equally well to linear and non-linear circuits.

2.2 — Goodness-of-Fit and Optimal Polynomial Order

The accuracy and reliability of any regression-based fault detection method heavily depend on selecting an appropriate degree for the polynomial model. An optimal order ensures the model captures the essential nonlinear relationships between input and output without becoming overly complex or too simplistic.

Overfitting

Overfitting occurs when the polynomial model has too high a degree. While it may fit the training data (simulated outputs) very well, it also captures noise and minute fluctuations that are not representative of actual circuit behaviour. This leads to poor generalization and may increase false positives during testing.

Role of Optimal Order Selection

To ensure that the polynomial model neither overfits nor underfits, a quantitative method is used to evaluate model quality: the **goodness-of-fit**. In this work, we assess fit quality using **information criteria**—statistical tools that account for both the error of the model and its complexity.

Akaike Information Criterion (AIC)

AIC = n × ln(MSE) + 2k

Where:

- n = number of data points
- MSE = mean squared error of the regression model
- k = number of regression coefficients

A lower AIC value indicates a better trade-off between model accuracy and simplicity.

Bayesian Information Criterion (BIC)

BIC = n × ln(MSE) + k × ln(n)

While similar to AIC, BIC is generally more conservative and prevents overfitting in models with limited datasets.

Why AIC/BIC is Preferred

Unlike basic metrics such as RMSE (root mean square error), which only evaluate model fit, AIC and BIC penalize excessive complexity. This makes them better suited for model order selection in fault detection applications where robustness and reliability are critical.

In this report, both AIC and BIC were used to determine the best polynomial order for each circuit case study. Orders producing the lowest AIC and BIC values were chosen for modeling and further analysis. This ensured a balance between sensitivity to faults and resilience to noise or variability in circuit response.

Chapter 3

FAULT DETECTION PROCEDURE

For fault detection, we assume that normal parameter variations (normal drift) in a fault free circuit are within a fraction α of their nominal value, where $0 < \alpha << 1$. That is, every parameter p_j is allowed to vary within the hypercube $p_{j,nom}(1 - \alpha) < p_j < p_{j,nom}(1 + \alpha)$ $\forall\, j$, where $p_{j;nom}$ is the nominal value of the circuit parameter p_j. Any change in the value of one or more parameters of an Analog circuit results in a change in one or more coefficient values of its polynomial regression model described by Eqn.(3), (4). The proposed approach mainly consists of two steps, estimation of fault free coefficient bounds for polynomial regression model followed by fault injection and fault detection. Using Monte-Carlo simulation, the minimum and maximum values of regression model coefficients can be obtained by varying each parameter p_j within its tolerance limit. Let $a_{pm,min}$ and $a_{pm,max}$ are the minimum and maximum values of p^{th} coefficient ($\forall$ p = 0 to N_{coeff} -1) in m^{th} degree regression model obtained after N_{MC} number of MC runs by varying all parameter within their tolerance limits. Due to a parametric fault, whenever any circuit component value slips outside its tolerance, one or more coefficient values of m^{th} degree polynomial regression model change and likely to slip outside the hypercube $a_{pm,min} < a_{pm} < a_{pm,max}$ for any p, $0 \le p \le N_{coeff}$ -1. As a result, we get a different set of coefficients reflecting a detectable fault. The probability that at least one coefficient falls outside the hypercube depends on the degree of the regression model and how precisely the boundary of the coefficient hypercube can be determined.

3.1-- Estimation of Fault free Polynomial Coefficients and their Bounds

For the derivation of polynomial coefficients, the CUT is first simulated in Orcade [26] with a nominal value of the circuit components. Using Orcade simulation data for V_{in1}, $V_{in2,}$ and V_{out}, a polynomial regression model of the form given by Eqn. (3) or (4) is obtained using MATLAB *Polyfitn* function. The polynomial coefficients, thus obtained, are fault free coefficients at nominal component values.

3.1.1 Computation of Fault free Coefficient Bounds

To calculate fault free (FF) bounds of coefficients, the CUT is simulated using the Monte-Carlo simulation [26, 27], where each of the circuit parameters is varied within the specified tolerance range (±5%) [16] for which the circuit output voltage V_{out} is considered to be fault free, and the polynomial coefficients for a given degree of regression model are estimated at each MC simulation run. Thus, for N_{MC} number of MC runs, the same number of different polynomial regression models of a given degree can be estimated. Comparing all such coefficients, the lower and upper bounds of each coefficient corresponding to each term of the polynomial can be obtained. Fig. 1 outlines the procedure to find the fault free bound of polynomial coefficients. It may be noted that the limits of output voltage V_{out_max} and V_{out_min} for a fault free circuit whose component values can be varied within the specified tolerance range, can also be obtained from N_{MC} number of MC samples. So, FF bounds of polynomial coefficients for a given degree of regression model cover the limits of fault free output voltage. Because, V_{out_max} and V_{out_min} for a fault free circuit lie in the MC samples. For any i^{th} MC simulation run, the goodness-of-fit for a given degree of regression model can be evaluated with the help of a metric, namely, the percentage of average difference [19]. The percentage of average difference, Avg_dif_i for i^{th} MC simulation run can be defined as follows.

$$Avg\_dif_i = \frac{\frac{\sum_{k=1}^{N} |V_{out}(k) - V_{out}P(k)|}{N}}{V_{out_{peak-to-peak}}} \quad (6)$$

where $V_{out}(k)$ and $V_{out}P(k)$ are the SPICE simulated output signal and predicted output signal at k^{th} time instant respectively. *N* represents the number of timed samples generated by the simulator in each MC simulation run and depends on the simulator type and simulation parameters such as maximum step size, start and stop time of simulation etc. $V_{\text{out}_{\text{peak-to-peak}}}$ is the peak-to-peak amplitude of the SPICE simulated output V_{out}.

For N_{MC} number of MC simulation runs, the percentage of average difference can be given as

$$\text{Avg\_dif} = \frac{\sum_{i=1}^{N_{\text{MC}}} Avg\_dif_{\text{i}}}{N_{\text{MC}}} \quad (7)$$

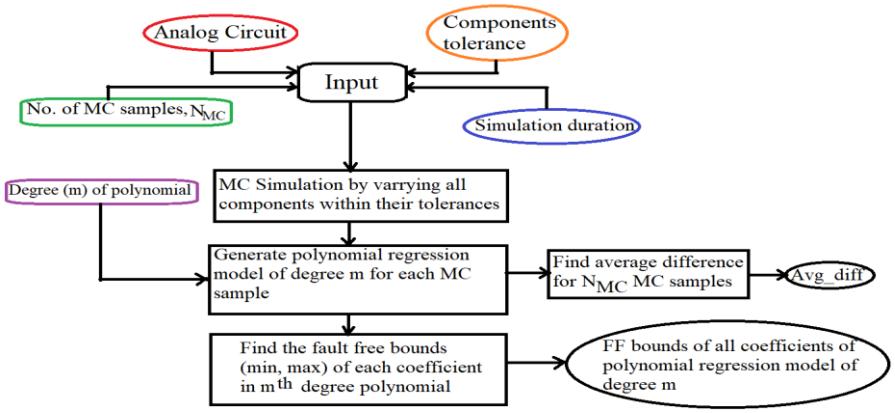

Fig. 1. Flow chart for computation of fault free coefficient bounds

3.2 - Fault Modelling and Fault Detection Strategy

It is noteworthy that only single parametric faults are considered in this paper. The operational amplifier used in the circuit is assumed to be fault free. The CUT is assumed to be fault free when the resistors and capacitor values vary within the tolerance limits (±5%). A single parametric fault is injected by varying one of the circuit parameters outside its tolerance limits, followed by Orcade simulation. Polynomial coefficients of the regression model for the faulty CUT are estimated using MATLAB *Polyfitn* function. The estimated polynomial coefficients of the faulty CUT are compared with the fault free coefficient bounds. If any of the estimated polynomial coefficients are found to lie outside its fault free bounds, the fault is said to be detected. On the contrary, if all of the coefficients are found to fall in the range, no conclusion can be drawn about whether the CUT is faulty or fault free. Fig. 2 outlines the fault detection procedure. However, in most cases, it is observed that if the CUT passes the polynomial coefficient-based fault detection test, the CUT can be declared fault free with a higher probability .

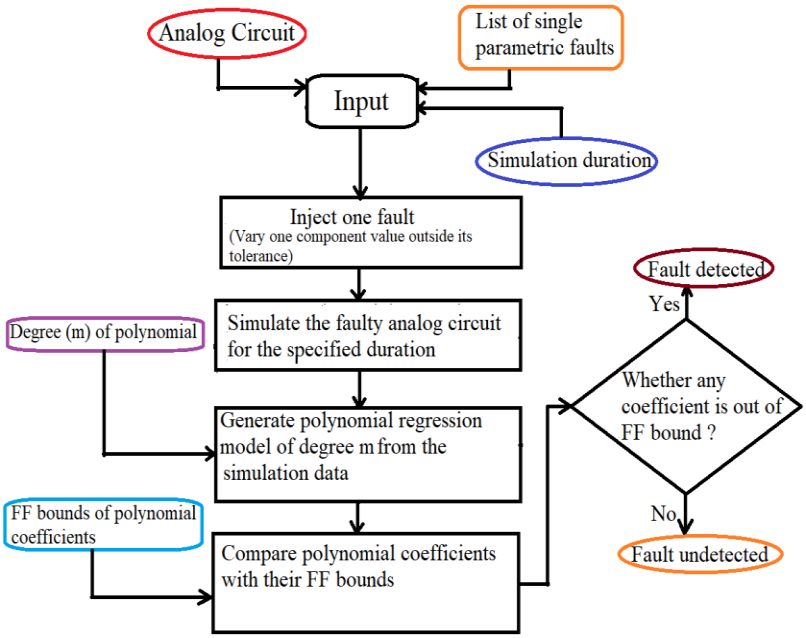

Fig. 2. Flow chart for fault detection in analog circuits

Chapter 4

CASE STUDY

This chapter presents the application of the proposed fault detection methodology on three representative Analog circuits. Each circuit is analyzed under multiple input conditions, including sinusoidal and slow-ramping DC (DC sweep), using polynomial regression models to detect single parametric faults. The study covers both linear and nonlinear Analog circuits:

4.1 CASE STUDY 1 – LEAD-LAG CIRCUIT WITH SINE INPUT

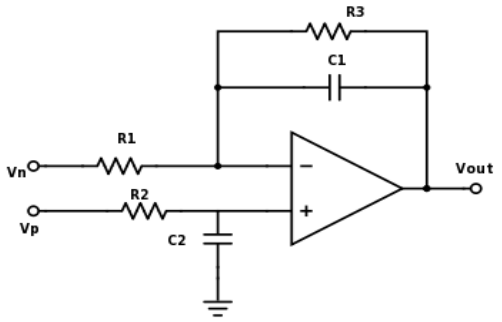

Fig. 3. Lead-lag circuit with two low-pass filters

The analog circuit under investigation is an op-amp-based lead-lag filter, designed using basic resistor-capacitor (RC) components, as shown in Fig. 3. It accepts two sinusoidal inputs—a characteristic that introduces complex signal behavior into the output due to superimposed filtering effects.
Circuit Configuration:

- Inverting Input (Vn): 100 Hz sine wave, amplitude = 200 mV
- Non-Inverting Input (Vp): 10 Hz sine wave, amplitude = 400 mV

These input values are chosen such that the op-amp output remains within its supply limits, ensuring linear operating conditions throughout the simulation.
Component Values:

- R1 = 1 kΩ
- R2 = 10 kΩ
- R3 = 10 kΩ
- C1 = 0.1595 μF
- C2 = 1.595 μF

The simulation is conducted in OrCAD Orcade for 110 ms, with a maximum step size of 50 μs. The simulated nominal output response is captured and shown in Fig. 4.

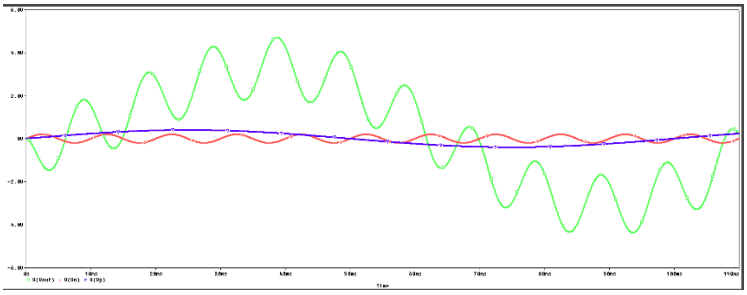

Fig. 4. Response of lead-lag circuit simulated in Orcade

4.1.1 Polynomial Modelling Using Optimal Order

Using the input-output data generated from the circuit simulation, a multivariate 18th-order polynomial regression model is developed.

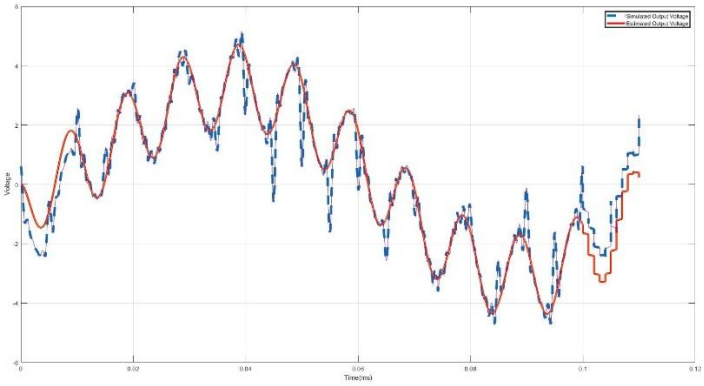

Fig:-5: Response of lead-lag circuit simulated in Orcade vs Polyfit estimated model

OPTIMAL ORDER

We got the 18 as optimal order from AIC/BIC method.

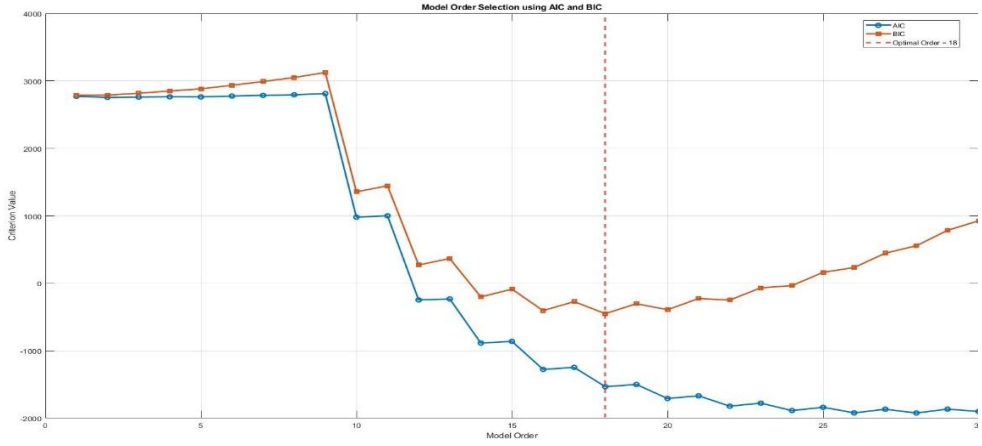

Fig-6:-Plot of optimal order for Nmc=500

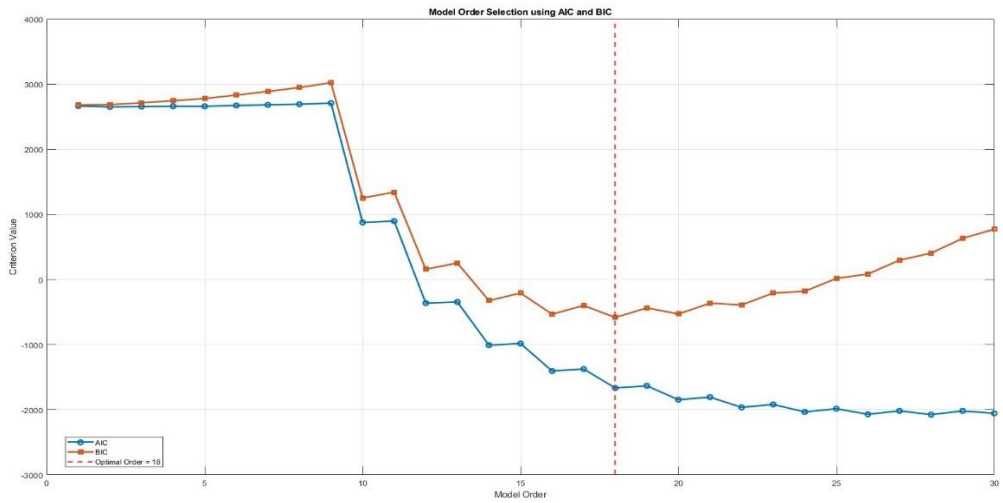

Fig-7:-Plot of optimal order for Nmc=1000

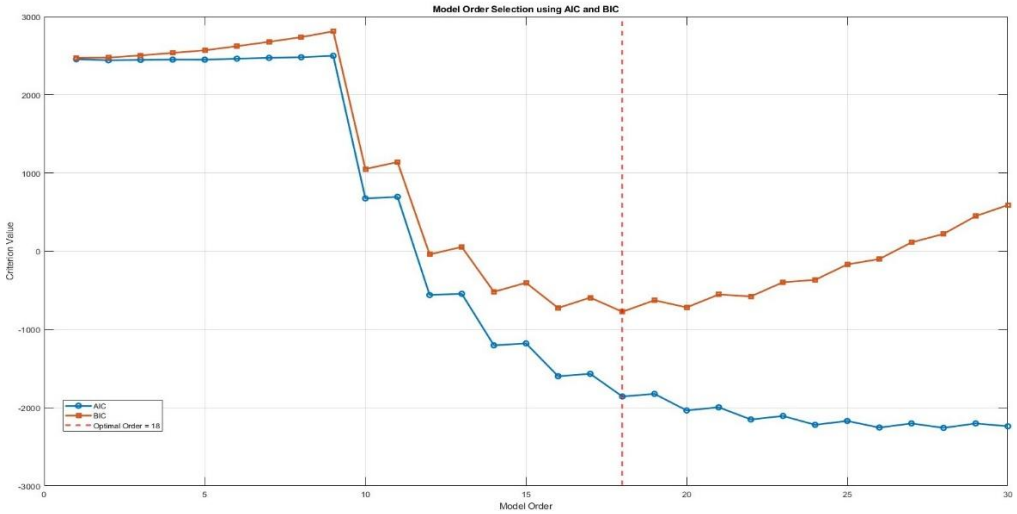

Fig-8:-Plot of optimal order for Nmc=2000

The optimal order is 18.
This formulation results in 190 coefficients in total.
The MATLAB implementation of this regression model produces a response that closely matches the Orcade-simulated output, as shown in Fig. 5. This validates the modeling accuracy for fault detection purposes.
Fault-Free (FF) Bounds Estimation:
To establish a reference for fault detection, Monte Carlo simulations are performed at three levels:

- NMC = 500, 1000, and 2000 samples
- In each run, random variations in component values within tolerance limits are introduced
- The polynomial coefficients are recalculated, and their bounds are extracted
- Fault-Free (FF) bounds are derived for each of the 190 coefficients using the min-max spread.

These bounds serve as the reference envelope. Any coefficient deviating outside these bounds in the presence of a fault is flagged as anomalous.

4.1.2 Fault Detection Framework

Fault detection is carried out by injecting both single and multiple parametric faults into the circuit. Each component is perturbed beyond its standard tolerance range, and the circuit is re-simulated. The updated output is processed through the same polynomial regression model, and the resulting coefficients are compared with their FF bounds.

Detection Criterion:
A fault is considered detected if at least one coefficient in the regression model falls outside its corresponding fault-free bound.
Fault scenarios are organized into the following categories:

- Low-deviation faults (<5%)
- Moderate faults (5–15%)
- Severe faults (>15%, up to 50%)
- Multiple faults (2–4 parameters deviated simultaneously)

4.1.3 Results

LEADLAG - in case of AC INPUT(SINE WAVE)						
Various Detected Faults in LEADLAG in the presence of faults with deviations (5% – 15%) & (20%-47%)						
Injected Faults	**N_{MC}=500, Avg_dif = 0.0420 Optimal Order – 18th**		**N_{MC}=1000, Avg_dif = 0.0420 Optimal Order – 18th**		**N_{MC}=2000, Avg_dif = 0.0420 Optimal Order – 18th**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
R1 12%↑	113	√	73	√	64	√
R1 8% ↓	1	√	0	X	0	X
R2 9% ↑	0	X	0	X	0	X
R2 6%↓	0	X	0	X	0	X
R3 10% ↑	71	√	57	√	38	√
R3 7%↓	0	X	0	X	0	X
C1 13%↑	0	X	0	X	0	X
C1 15%↓	3	√	3	√	3	√
C2 11% ↑	0	X	0	X	0	X
C2 14%↓	10	√	7	√	6	√
R1 20%↑	163	√	156	√	153	√
R1 30% ↓	183	√	183	√	183	√
R2 32% ↑	34	√	33	√	32	√
R2 40% ↓	104	√	93	√	89	√
R3 25% ↑	174	√	173	√	172	√
R3 45%↓	185	√	184	√	183	√
C1 42%↑	17	√	14	√	13	√
C1 25% ↓	15	√	14	√	12	√
C2 35% ↑	38	√	33	√	31	√
C2 47% ↓	140	√	135	√	132	√

LEADLAG - in case of AC INPUT(SINE WAVE)						
Various Detected Faults in LEADLAG in the presence of faults with deviations (>5%)						
Injected Faults	N_{MC}=500, Avg_dif = 0.0420 Optimal Order – 18th		N_{MC}=1000, Avg_dif = 0.0420 Optimal Order – 18th		N_{MC}=2000, Avg_dif = 0.0420 Optimal Order – 18th	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R1 3%↑	0	X	0	X	0	X
R2 2% ↓	0	X	0	X	0	X
R3 4% ↑	0	X	0	X	0	X
C1 2% ↓	0	X	0	X	0	X
C2 4% ↑	0	X	0	X	0	X
R1 1%↓	0	X	0	X	0	X
R2 1%↑	0	X	0	X	0	X
R3 4% ↓	0	X	0	X	0	X
C1 3% ↑	0	X	0	X	0	X
C2 4% ↓	0	X	0	X	0	X

LEADLAG - in case of AC INPUT(SINE WAVE)						
Various Detected Faults in LEADLAG in the presence of MULTIPLE faults with deviations						
Injected Faults	N_{MC}=500, Avg_dif = 0.0420 Optimal Order – 18th		N_{MC}=1000, Avg_dif = 0.0420 Optimal Order – 18th		N_{MC}=2000, Avg_dif = 0.0420 Optimal Order – 18th	
	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R1 15%↑ R2 20% ↓	162	√	155	√	151	√
R2 8% ↓ R3 12% ↑	100	√	96	√	90	√
R3 20% ↑ C1 10% ↑ C2 10% ↓	158	√	152	√	151	√
R1 18% ↓ C1 10% ↑ C2 10% ↓	166	√	162	√	160	√
R2 9% ↑ R3 15% ↓ C1 12% ↑ C2 8% ↓	153	√	142	√	137	√

4.1.4 Conclusion

The study confirms that a polynomial regression model of optimal order 18 provides a powerful mechanism for data-driven fault detection in analog circuits with dual inputs. Key findings include:

- Low-level faults (<5%) often remain undetected due to high similarity with nominal behavior
- Moderate faults (5–15%) show partial detectability depending on component and NMC
- Severe single and multiple faults (>15%) are reliably detected due to significant nonlinear impact on output
- Detection remains consistent even when multiple simultaneous faults are introduced
- Using 190 polynomial coefficients provides high model resolution for fault sensitivity

This approach demonstrates a scalable framework for analog fault detection using polynomial regression and Monte Carlo simulation, with potential extensions to multi-input systems and higher-dimensional signal environments.

4.2 Lead-Lag Circuit with DC sweep Input: Fault Modelling and Detection

In this section, a polynomial-based fault detection methodology is applied to a **lead-lag circuit** excited using **slow-varying DC inputs** varied at the rate of **50Hz and 100Hz** , simulating a realistic biasing and transient input scenario. This setup aims to evaluate the sensitivity of the detection algorithm under slow dynamic inputs compared to purely AC sinusoidal inputs.

The same **two-input op-amp-based lead-lag circuit** from Section 4.1 is considered here. The two inputs, however, are now designed to reflect **slow DC-like behaviour**, useful in evaluating system drift, bias variation, and long-term response. The input waveforms are constructed as slow-varying DC signals with embedded low-frequency sinusoidal components:

- **Vn (Inverting Input)**: ramped DC with 100Hz frequency.
- **Vp (Non-Inverting Input)**: ramped DC with 50Hz frequency.

These waveforms ensure a low dynamic swing that doesn't saturate the op-amp and mimics gradual shifts in real-world analog systems. The nominal component values remain unchanged:

- R1 = 1 kΩ
- R2 = 10 kΩ
- R3 = 10 kΩ
- C1 = 0.1595 µF
- C2 = 1.595 µF

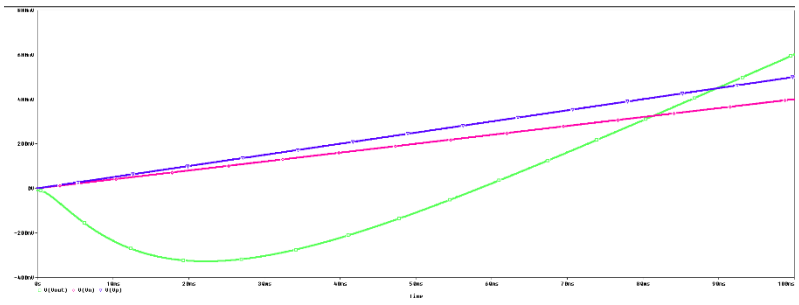

Fig. 9:. Response of lead-lag circuit simulated in Orcade

4.2.1 Polynomial Regression Modelling

The output of the lead-lag circuit is modelled using a **14th-order multivariate polynomial regression model**, which is selected as the **optimal order** based on error minimization and modelling consistency across MC simulations.

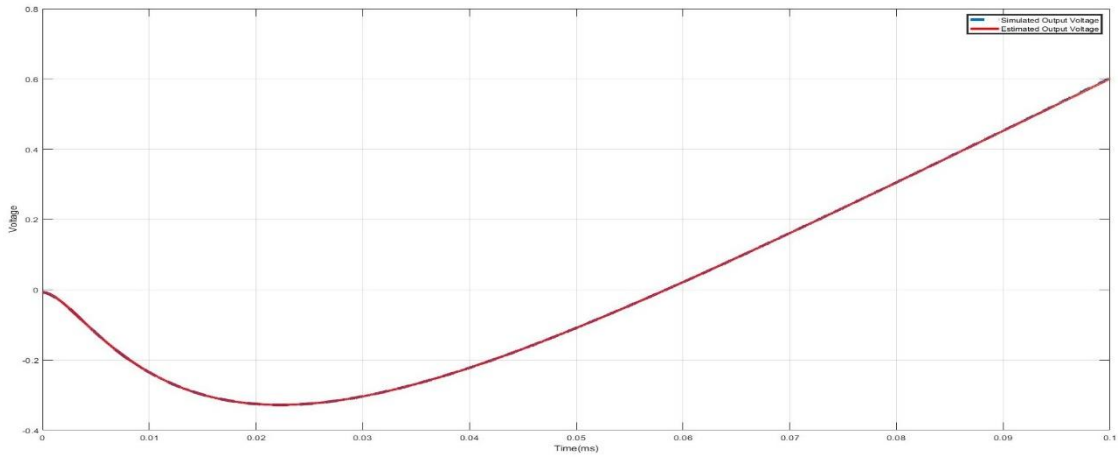

Fig-10:-Response simulated in orcade vs Polyfit model

OPTIMAL ORDER

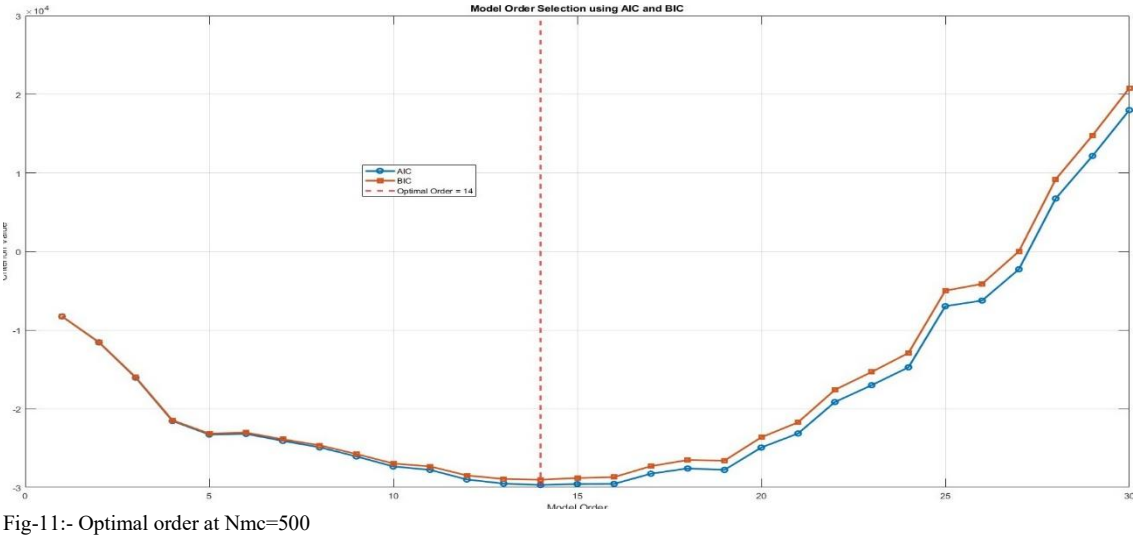

Fig-11:- Optimal order at Nmc=500

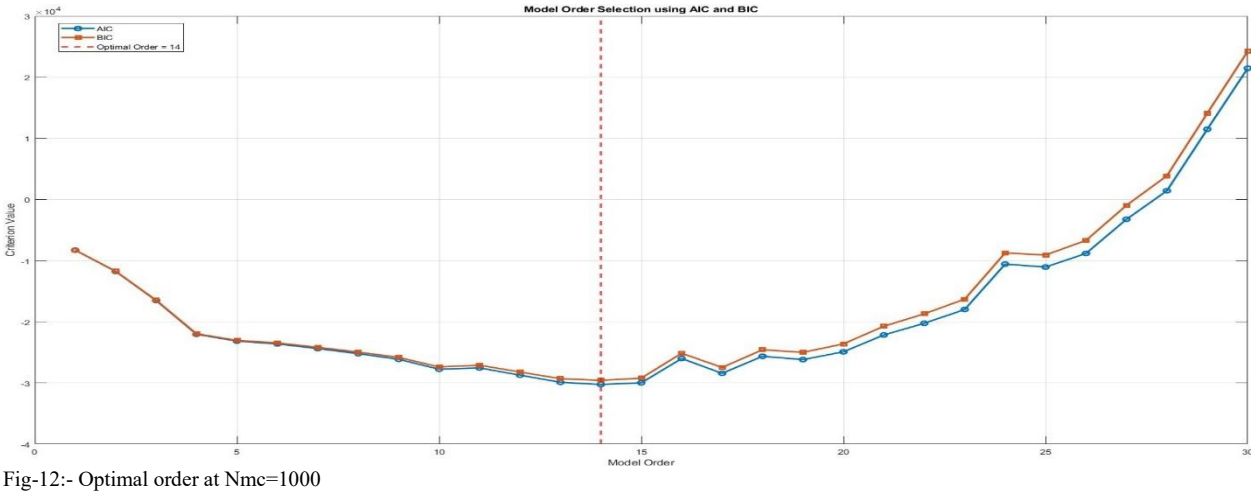

Fig-12:- Optimal order at Nmc=1000

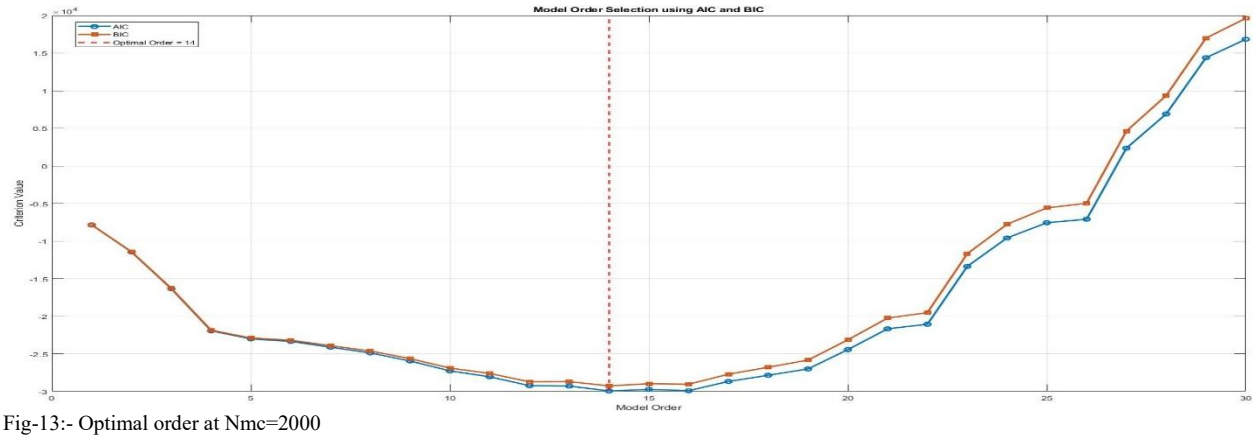

Fig-13:- Optimal order at Nmc=2000

This results in **120 coefficients** (based on binomial expansion with 2 variables and order 14). The regression is implemented in MATLAB and validated against OrCAD Orcade simulations for nominal inputs.

4.2.2 Fault Detection Framework

To develop a fault detection envelope, **Monte Carlo (MC) simulations** are conducted with **NMC = 500, 1000, and 2000 samples**. For each run:

- Inputs are held nominal
- Component values are varied within ±1% tolerance
- Coefficients of the 14th-order polynomial model are recorded

Using the resulting distributions, **fault-free bounds** are computed for each coefficient—typically using the **min–max**. These bounds serve as the reference to evaluate whether any estimated coefficients in faulty conditions deviate beyond normal variability.

Various types of faults are injected by altering each component value beyond its standard tolerance limit. The injected faults are categorized as:

- **Low-deviation faults** (<5%)

- **Moderate faults** (5%–15%)
- **High-deviation faults** (>15%)
- **Multiple simultaneous faults**

The output response under each fault scenario is used to retrain the 14th-order model, and the new coefficients are compared against the fault-free bounds.

4.2.3 Results

LEADLAG- in case of DC INPUT(slow dc with 100Hz & 50Hz frequency						
Various Detected Faults in LEADLAG in the presence of faults with deviations (5% – 15%) & (20%-47%)						
Injected Faults	**N_{MC}=500, Avg_dif = 5.1931e-04 Optimal Order – 14th**		**N_{MC}=1000,Avg_dif = 5.1978e-04 Optimal Order – 14th**		**N_{MC}=2000,Avg_dif = 5.2020e-04 Optimal Order – 14th**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
R1 12%↑	0	**X**	0	**X**	0	**X**
R1 8% ↓	0	**X**	0	**X**	0	**X**
R2 9% ↑	0	**X**	0	**X**	0	**X**
R2 6%↓	0	**X**	0	**X**	0	**X**
R3 10% ↑	0	**X**	0	**X**	0	**X**
R3 7%↓	0	**X**	0	**X**	0	**X**
C1 13%↑	0	**X**	0	**X**	0	**X**
C1 15%↓	3	**√**	2	**√**	2	**√**
C2 11% ↑	0	**X**	0	**X**	0	**X**
C2 14%↓	1	**√**	1	**√**	1	**√**
R1 20%↑	1	**√**	0	**X**	0	**X**
R1 30% ↓	3	**√**	3	**√**	3	**√**
R2 32% ↑	1	**√**	1	**√**	1	**√**
R2 40% ↓	1	**√**	1	**√**	1	**√**
R3 25% ↑	10	**√**	8	**√**	8	**√**
R3 45%↓	4	**√**	4	**√**	4	**√**
C1 42%↑	4	**√**	4	**√**	3	**√**
C1 25% ↓	2	**√**	2	**√**	2	**√**
C2 35% ↑	0	**X**	0	**X**	0	**X**
C2 47% ↓	35	**√**	30	**√**	26	**√**

LEADLAG- in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)						
Various Detected Faults in LEADLAG in the presence of faults with deviations (>5%)						
Injected Faults	**N_{MC}=500, Avg_dif =5.1931e-04 Optimal Order – 14th**		**N_{MC}=1000, Avg_dif = 5.1978e-04 Optimal Order – 14th**		**N_{MC}=2000, Avg_dif = 5.2020e-04 Optimal Order – 14th**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
R1 3%↑	**1**	**√**	**1**	**√**	**1**	**√**
R2 2% ↓	1	**√**	**1**	**√**	**0**	**X**
R3 4% ↑	**0**	**X**	**0**	**X**	**0**	**X**
C1 2% ↓	**0**	**X**	**0**	**X**	**0**	**X**
C2 4% ↑	**0**	**X**	**0**	**X**	**0**	**X**
R1 1%↓	**0**	**X**	**0**	**X**	**0**	**X**
R2 1%↑	**0**	**X**	**0**	**X**	**0**	**X**
R3 4% ↓	1	**√**	**0**	**X**	**0**	**X**
C1 3% ↑	**0**	**X**	**0**	**X**	**0**	**X**
C2 4% ↓	**0**	**X**	**0**	**X**	**0**	**X**

LEADLAG- in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)						
Various Detected Faults in LEADLAG in the presence of MULTIPLE faults with deviations						
Injected Faults	**N_{MC}=500, Avg_dif = 5.1931e-04 Optimal Order – 14th**		**N_{MC}=1000, Avg_dif = 5.1978e-04 Optimal Order – 14th**		**N_{MC}=2000, Avg_dif = 5.2020e-04 Optimal Order – 14th**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
R1 15%↑ R2 20% ↓	32	**√**	32	**√**	29	**√**
R2 8% ↓ R3 12% ↑	30	**√**	30	**√**	29	**√**
R3 20% ↑ C1 10% ↑ C2 10% ↓	28	**√**	27	**√**	25	**√**
R1 18% ↓ C1 10% ↑ C2 10% ↓	34	**√**	34	**√**	32	**√**
R2 9% ↑ R3 15% ↓ C1 12% ↑ C2 8% ↓	32	**√**	32	**√**	29	**√**

4.2.4 Conclusion

The polynomial regression-based fault detection methodology, using a **14th-order optimal model**, provides moderate sensitivity under **slow DC excitation**. Key findings:

- **Low faults (<5%)** are often undetected due to minimal impact on circuit dynamics
- **Moderate faults (5–15%)** yield inconsistent results depending on NMC
- **High deviation (>20%) and multiple faults** are reliably detected
- Monte Carlo variation analysis ensures robustness against noise and non-fault-induced variations

Overall, the method proves viable for analog fault detection under slow dynamic signals, especially for significant shifts or concurrent multi-component drifts.

4.3 Analog Multiplier with Sine Input

The analog multiplier studied here is a four-quadrant analog multiplier based on the design proposed by Riewruja and Rerkratn (2011), using only general-purpose operational amplifiers. The design employs the quarter-square technique, leveraging the inherent squaring behavior of the class AB output stage of opamps to realize analog multiplication.
The core circuit performs the identity:

- $\mathbf{v_o = (1/4) \times [\,(v_1 + v_2)^2 - (v_1 - v_2)^2\,] = v_1 \times v_2}$

This functionality is implemented using:

- Voltage-to-current conversion stages (A11, A12, A21, A22 with R11–R22)
- Supply current sensing (via R21, R22)
- A difference amplifier (A3 with R31–R42)
- An inverting stage for balancing

The inputs Vx and Vy are selected as sinusoidal signals with frequencies ranging from 100 Hz and 1 kHz and amplitudes within ±200&400 mV, ensuring that the output remains within the supply voltage rails and that opamps operate in the linear class AB region.

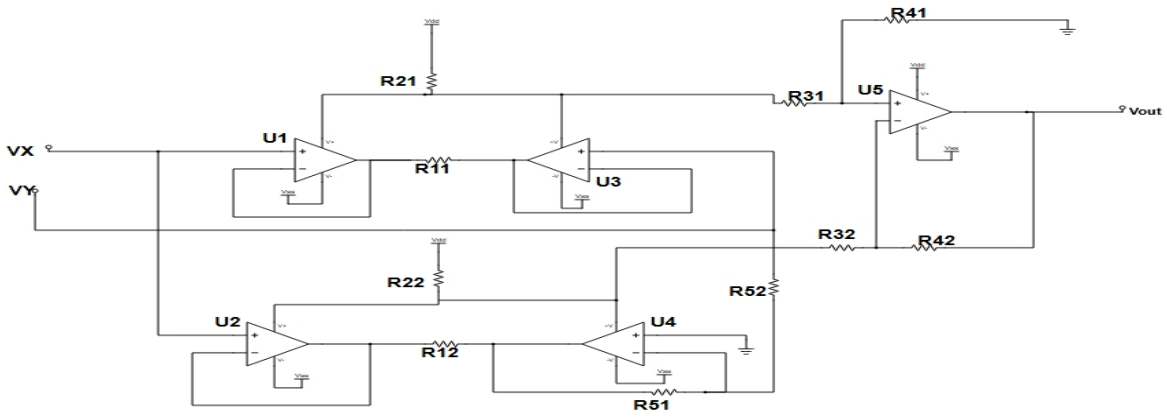

Fig 14:-Analog Multiplier

The simulations are performed in OrCAD Orcade, modelling the analog multiplier under fault-free and faulty conditions. The supply voltage is ±8 V, and the simulation time is chosen to capture several full cycles of both inputs. The nominal component values used in the simulation are:

- R1 = 10 kΩ

- R2 = 1 kΩ
- R3 = 250 kΩ
- R4 = 500 kΩ
- R5 = 250 kΩ

These values are consistent with those used in both the original experimental work and Orcade simulations. +-5% tolerances are introduced systematically to simulate parametric faults**.**

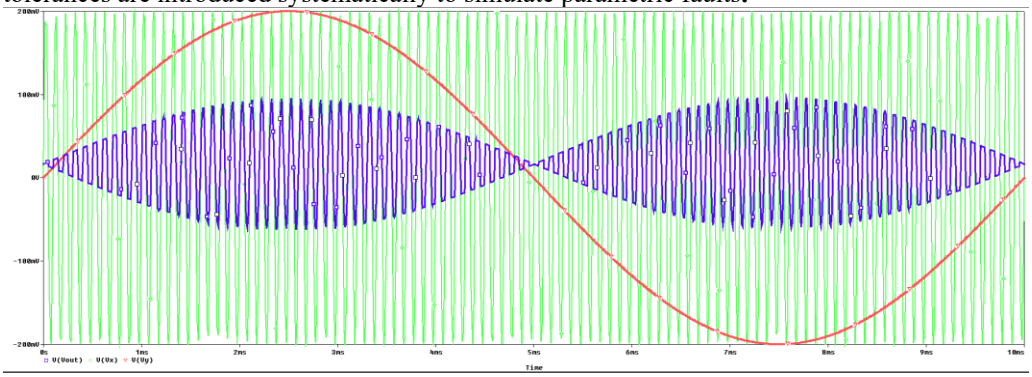

Fig. 15. Response of analog multiplier with sine input simulated in Orcade

4.3.1 Polynomial Modelling and Fault-Free Coefficient Estimation

To analyse and detect faults, the output Vout of the analog multiplier is modelled using a **multivariate polynomial regression.**

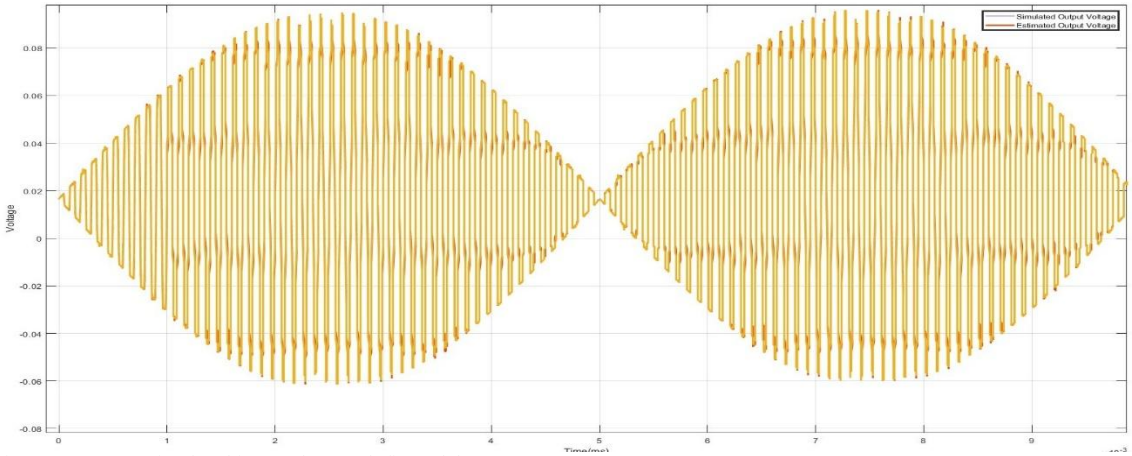

Fig:-16:Response simulated in orcade vs Polyfit model

This allows nonlinear behaviour to be captured accurately from input-output data.

- For **N = 500 and 1000 samples**, the **optimal polynomial order** is found to be **18**
- For **N = 2000 samples**, the optimal order increases to **22**, improving regression accuracy.

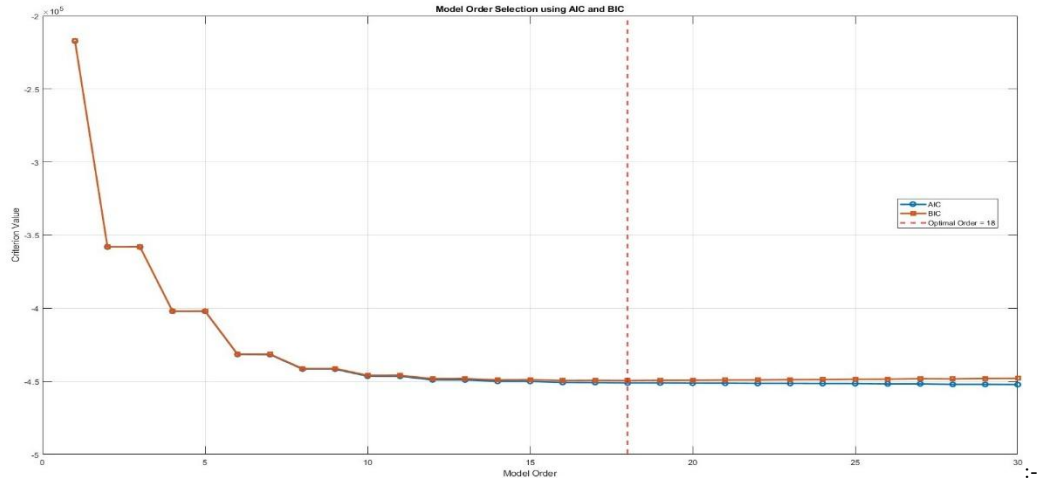

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Fig:-17:-Optimal order at Nmc=500

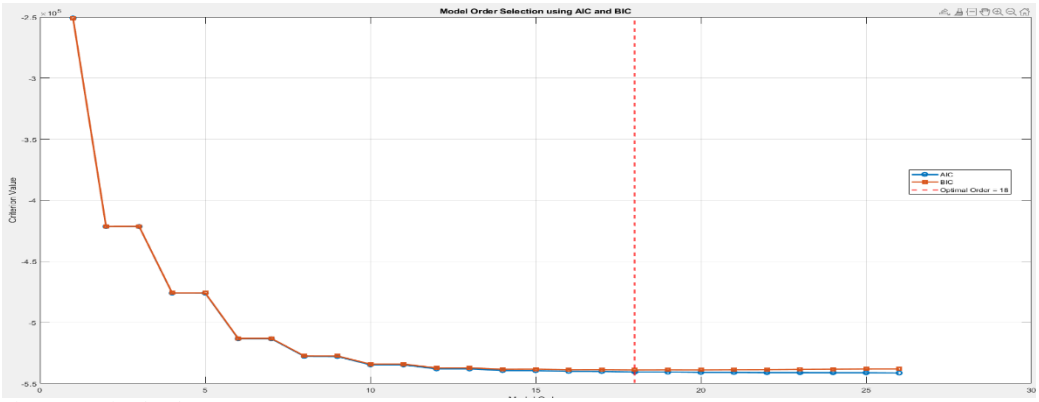

Fig:-18:-Optimal order at Nmc=1000

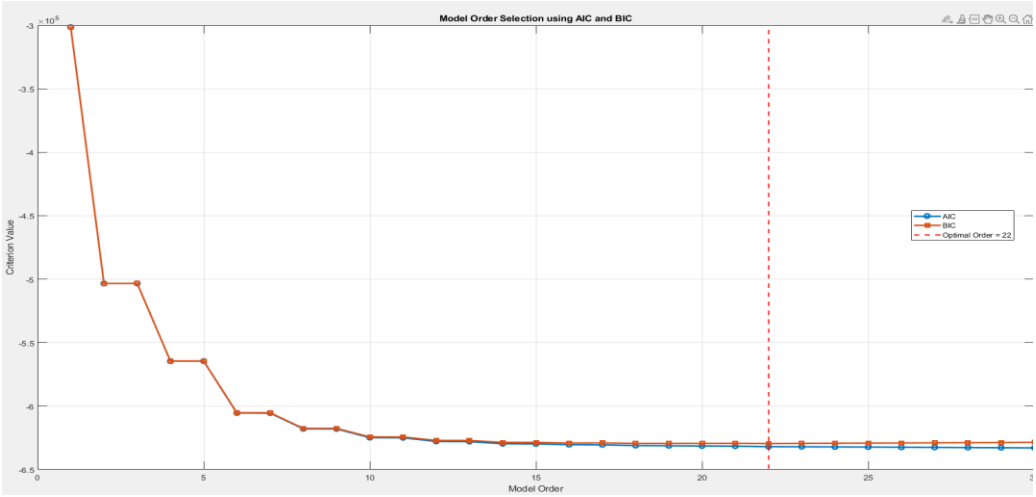

Fig:-19:-Optimal order at Nmc=2000

This results in:

- **190 coefficients** for the 18th-order model
- **276 coefficients** for the 22nd-order model

To establish a reliable detection benchmark, **Monte Carlo simulations** are carried out at **NMC = 500, 1000, and 2000**:

- Component values are varied randomly within ±5% (fault-free tolerance)
- The resulting output data are fitted to the polynomial model
- Distributions of all coefficients are computed
- **Fault-Free Bounds (FF Bounds)** are derived using absolute min-max limits

These FF bounds form the statistical envelope for detecting coefficient deviations under fault conditions.

4.3.2 Fault Injection Procedure and Detection Framework

Fault detection is performed by intentionally introducing parametric faults into individual resistors (R11–R52), altering their values by ±5% to ±46%.

If **any coefficient** lies **outside its FF bound**, the corresponding fault is considered **detected**.

This approach enables:

- Detection of both **single faults** and **multiple simultaneous faults**
- Analysis of model sensitivity to different fault magnitudes and locations
- Performance evaluation under varying sample sizes (N = 500, 1000, 2000)

4.3.3 RESULTS

ANALOG MULTIPLIER- in case of AC INPUT(SINE WAVE)						
Various Detected Faults in Analog Multiplier in the presence of faults with deviations (5% – 15%) & (20%-46%)						
Injected Faults	**N_{MC}=500, Avg_dif = 0.0098 Optimal Order – 18th**		**N_{MC}=1000, Avg_dif = 0.0097 Optimal Order – 18th**		**N_{MC}=2000, Avg_dif = 0.0097 Optimal Order – 22nd**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
R11 6%↑	19	√	16	√	23	√
R11 6% ↓	12	√	7	√	12	√
R12 7% ↑	10	√	4	√	23	√
R12 7% ↓	27	√	20	√	64	√
R21 8% ↑	25	√	16	√	12	√
R21 8%↓	15	√	8	√	12	√

R22 9%↑	20	√	15	√	32	√
R22 9% ↓	21	√	17	√	30	√
R31 10%↑	15	√	12	√	11	√
R31 10% ↓	30	√	30	√	27	√
R32 11%↑	22	√	15	√	30	√
R32 11%↓	36	√	30	√	32	√
R41 12% ↑	38	√	35	√	13	√
R41 12%↓	17	√	15	√	17	√
R42 13%↑	29	√	18	√	32	√
R42 13%↓	21	√	8	√	18	√
R51 14% ↑	3	√	5	√	12	√
R51 14% ↓	16	√	16	√	35	√
R52 15% ↑	41	√	38	√	18	√
R52 15% ↓	26	√	24	√	13	√
R11 20% ↑	17	√	9	√	25	√
R11 20% ↓	58	√	37	√	39	√
R12 25% ↑	17	√	14	√	27	√
R12 25%↓	40	√	20	√	15	√
R21 30% ↑	33	√	28	√	39	√
R21 30% ↓	4	√	3	√	9	√
R22 35% ↑	40	√	27	√	22	√
R22 35%↓	20	√	20	√	14	√
R31 36% ↑	28	√	27	√	8	√
R31 36%↓	38	√	26	√	18	√
R32 38% ↑	7	√	7	√	2	√
R32 38%↓	75	√	57	√	96	√
R41 40% ↑	32	√	23	√	26	√
R41 40%↓	18	√	10	√	30	√
R42 42% ↑	46	√	44	√	34	√
R42 42%↓	3	√	4	√	4	√
R51 44% ↑	30	√	26	√	19	√
R51 44% ↓	68	√	58	√	53	√

R52 46% ↑	66	√	65	√	71	√
R52 46% ↓	28	√	24	√	36	√

ANALOG MULTIPLIER- in case of AC INPUT(SINE WAVE)						
Various Detected Faults in Analog Multiplier in the presence of faults with deviations (>5%)						
Injected Faults	**N_{MC}=500, Avg_dif = 0.0098 Optimal Order – 18th**		**N_{MC}=1000, Avg_dif = 0.0097 Optimal Order – 18th**		**N_{MC}=2000, Avg_dif = 0.0097 Optimal Order – 22nd**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
R11 1%↓	0	X	0	X	1	√
R11 3% ↑	5	√	5	√	0	X
R12 2% ↑	1	√	0	X	0	X
R12 1% ↓	5	√	5	√	5	√
R21 3% ↑	0	X	1	√	0	X
R21 2.5%↓	0	X	0	X	0	X
R22 2%↑	1	√	0	X	0	X
R22 3% ↓	3	√	1	√	0	X
R31 4% ↑	0	X	0	X	0	X
R31 3.5% ↓	3	√	0	X	0	X
R32 1% ↑	1	√	0	X	0	X
R32 3% ↓	7	√	5	√	3	√
R41 2%↑	0	X	0	X	0	X
R41 1%↓	0	X	0	X	0	X
R42 3%↑	3	√	1	√	0	X
R42 1%↓	1	√	1	√	0	X
R51 1.5% ↑	0	X	2	√	1	√
R51 1.8% ↓	2	√	0	X	0	X
R52 2.3% ↑	0	X	0	X	0	X
R52 2.9%↓	0	X	0	X	0	X

ANALOG MULTIPLIER- in case of AC INPUT(SINE WAVE)			
Various Detected Faults in MULTIPLIER in the presence of MULTIPLE faults with deviations			
Injected Faults	**N_{MC}=500, Avg_dif = 0.0098 Optimal Order – 18th**	**N_{MC}=1000, Avg_dif = 0.0097 Optimal Order – 18th**	**N_{MC}=2000, Avg_dif = 0.0097 Optimal Order – 22nd**

	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status	No. of Coefficients Out of Bound	Fault Detection Status
R11 8%↑ R12 10% ↑	15	√	13	√	17	√
R21 20% ↑ R22 15% ↓	25	√	21	√	38	√
R31 20% ↓ R32 20% ↑ R41 10% ↑	18	√	17	√	16	√
R52 30%↓ R51 20% ↑	21	√	16	√	23	√
R11 15% ↑ R12 20% ↓ R42 18 % ↑	34	√	31	√	55	√

4.3.4 Conclusion

The analog multiplier, modelled using a high-order multivariate polynomial regression approach, demonstrates effective representation of nonlinear input–output behaviour under sinusoidal excitation. With optimal model orders of 18 and 22, and fault-free bounds derived from Monte Carlo analysis, the framework enables accurate tracking of circuit behaviour. This data-driven methodology lays a solid foundation for fault detection by capturing parametric deviations through polynomial coefficient shifts, even in complex analog systems.

4.4 Analog Multiplier with Slow DC Sweep Input

The analog multiplier implemented here is a four-quadrant configuration based on the quarter-square technique proposed by **Riewruja and Rerkratn (2011)**, using only general-purpose operational amplifiers. In this experiment, the circuit is tested with **slow-varying DC inputs** designed to mimic low-frequency analog conditions such as bias drift, low-rate control signals, or ramped modulations.

The implementation includes is same as with sine input.

Input Configuration:

Based on manually constructed data (see Fig. 18), the sweep inputs are defined as:

- **Vx**: Sweeps from **–0.1 V to +0.1 V** at **100 Hz**
- **Vy**: Sweeps from **–1 V to +1 V** at **50 Hz**

These input conditions were chosen to ensure that:

- The opamps operate within their **linear class AB region**
- The output remains **within ± supply rails**
- Realistic low-frequency variations are emulated.

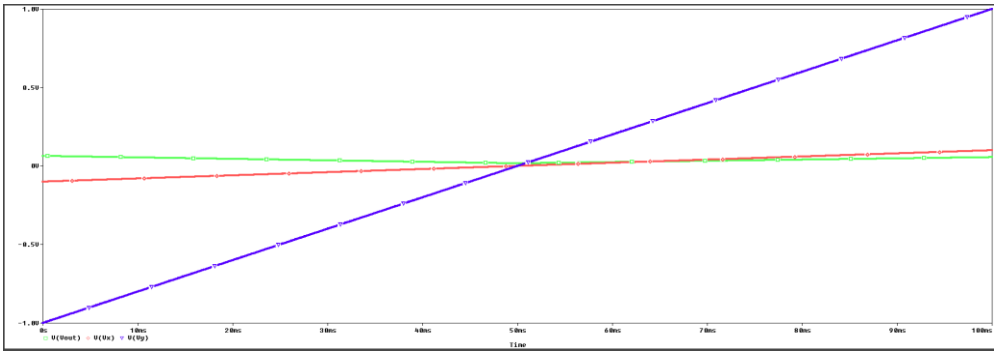

Fig. 20. Response of Analog multiplier with DC sweep input simulated in Orcade

4.4.1 Polynomial Modelling and Fault-Free Coefficient Estimation

The output Vout of the analog multiplier is modeled using a **multivariate polynomial regression** to capture nonlinear input–output behavior under slow dynamic conditions.

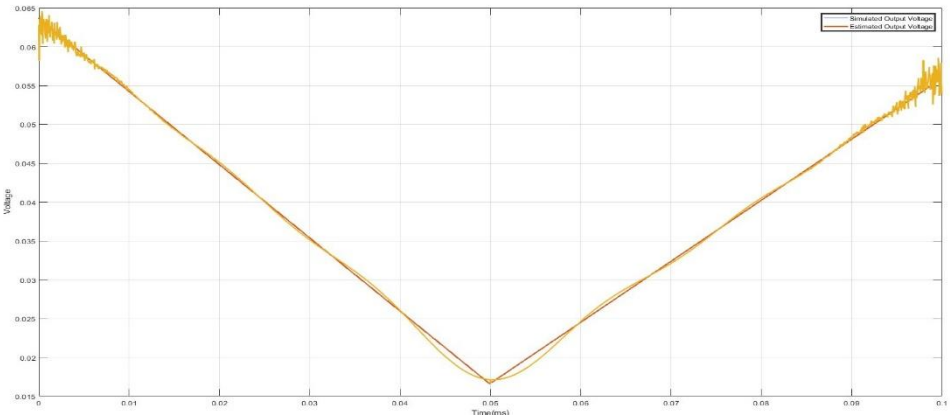

Fig. 21. Response of lead-lag circuit simulated in Orcade vs Polyfit model.

Optimal Order and Coefficients:

- For **N = 500** samples, the **optimal polynomial order is 16**
- For **N = 1000 and 2000** samples, the **optimal order is 15**

This leads to:

- **153 coefficients** for order 16
- **136 coefficients** for order 15

These models are implemented and simulated in **MATLAB** using input-output data from **OrCAD.**

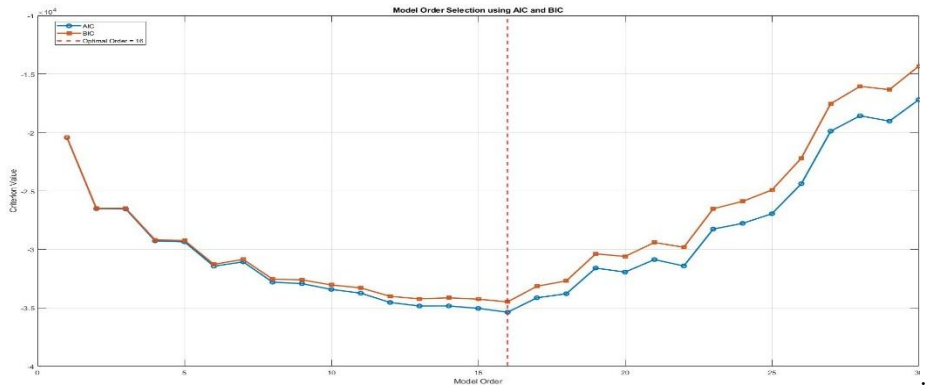

Fig 22:-Optimal order at Nmc=500

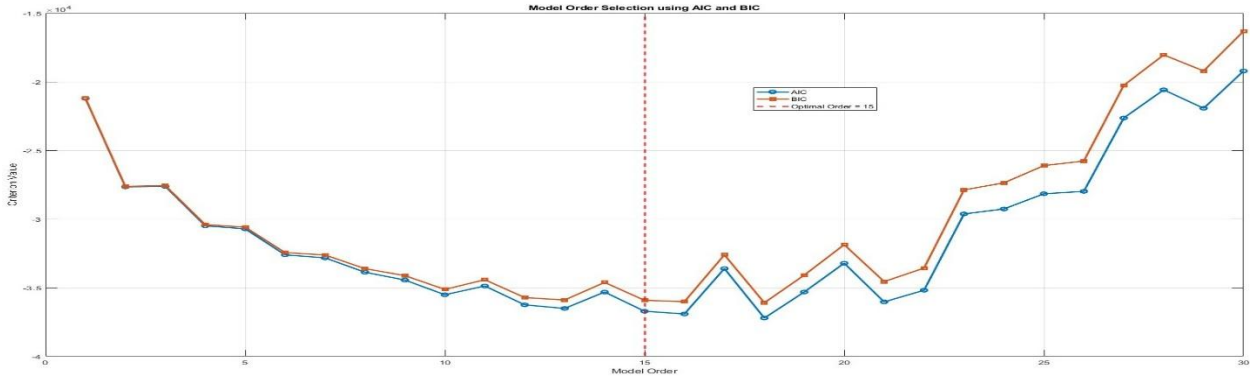

Fig 23:-Optimal order at Nmc=1000

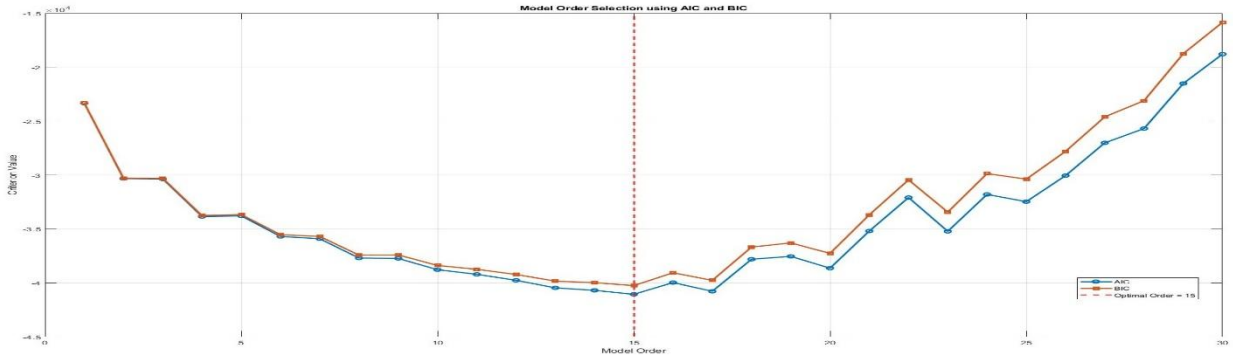

Fig 24:-Optimal order at Nmc=2000

Monte Carlo Setup:

To build the statistical envelope for fault detection:

- Monte Carlo simulations are performed at **NMC = 500, 1000, and 2000**
- Component values are varied randomly within a **±5% fault-free tolerance**
- The coefficients from each MC run are computed
- **Fault-Free Bounds (FF Bounds)** are extracted using absolute min–max ranges

These FF bounds serve as the basis for identifying out-of-bound coefficient behaviour under fault scenarios.

4.4.2 Fault Injection Procedure and Detection Framework

To evaluate the model's sensitivity and fault detection capability:

- **Single and multiple parametric faults** are injected by varying resistor values (R11–R52) from ±5% up to ±46%
- The circuit is re-simulated in Orcade under each fault condition
- The resulting output is re-fitted using the corresponding polynomial model (order 15 or 16)

4.4.3 Results

ANALOG MULTIPLIER - in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)						
Various Detected Faults in Analog Multiplier in the presence of faults with deviations (5% – 15%) & (20%-46%)						
Injected Faults	**N_{MC}=500, Avg_dif = 0.0103 Optimal Order - 16th**		**N_{MC}=1000, Avg_dif = 0.0108 Optimal Order - 15th**		**N_{MC}=2000, Avg_dif = 0.0110 Optimal Order - 15th**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
R11 6%↑	10	√	12	√	3	√
R11 6% ↓	2	√	8	√	2	√
R12 7% ↑	4	√	3	√	2	√
R12 7% ↓	6	√	9	v	5	√
R21 8% ↑	2	√	4	√	2	√
R21 8%↓	12	√	13	√	2	√
R22 9%↑	12	√	8	√	2	√
R22 9% ↓	1	√	3	√	0	X
R31 10% ↑	8	√	7	√	2	√
R31 10% ↓	6	√	8	√	2	√
R32 11% ↑	2	√	7	√	3	√
R32 11% ↓	10	√	6	√	3	√
R41 12% ↑	5	√	7	√	2	√
R41 12% ↓	5	√	13	√	2	√
R42 13% ↑	10	√	8	√	4	√
R42 13% ↓	1	√	4	√	3	√
R51 14% ↑	1	√	2	√	0	X
R51 14% ↓	13	√	12	√	4	√
R52 15% ↑	12	√	14	√	7	√
R52 15% ↓	1	√	3	√	0	X
R11 20% ↑	13	√	16	√	9	√
R11 20% ↓	1	√	2	√	0	X
R12 25% ↑	1	√	2	√	0	X
R12 25% ↓	28	√	43	√	28	√
R21 30% ↑	3	√	6	√	2	√
R21 30% ↓	15	√	25	√	10	√

R22 35% ↑	16	√	22	√	10	√
R22 35% ↓	5	√	4	√	5	√
R31 36% ↑	9	√	11	√	7	√
R31 36% ↓	3	√	2	√	1	√
R32 38% ↑	2	√	4	√	1	√
R32 38% ↓	22	√	46	√	35	√
R41 40% ↑	3	√	5	√	1	√
R41 40% ↓	13	√	12	√	9	√
R42 42% ↑	19	√	23	√	13	√
R42 42% ↓	2	√	3	√	1	√
R51 44% ↑	3	√	4	√	3	√
R51 44% ↓	60	√	68	√	57	√
R52 46% ↑	42	√	30	√	30	√
R52 46% ↓	5	√	9	√	3	√

ANALOG MULTIPLIER - in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)						
Various Detected Faults in Analog Multiplier in the presence of faults with deviations (< 5%)						
Injected Faults	**N_{MC}=500, Avg_dif = 0.0103 Optimal Order - 16th**		**N_{MC}=1000, Avg_dif = 0.0108 Optimal Order - 15th**		**N_{MC}=2000, Avg_dif = 0.0110 Optimal Order - 15th**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
R11 1%↓	0	X	0	X	1	√
R11 3% ↑	8	√	8	√	2	√
R12 2% ↑	1	√	0	X	1	√
R12 1% ↓	7	√	5	√	2	√
R21 3% ↑	0	X	1	√	3	√
R21 2.5%↓	0	X	1	√	1	√
R22 2%↑	1	√	2	√	3	√
R22 3% ↓	3	√	1	√	1	√
R31 4% ↑	0	X	0	X	3	√
R31 3.5% ↓	3	√	6	√	1	√
R32 1% ↑	1	√	0	X	0	X
R32 3% ↓	8	√	10	√	3	√
R41 2%↑	0	X	0	X	0	X
R41 1%↓	0	X	0	X	1	√
R42 3%↑	3	√	1	√	2	√
R42 1%↓	1	√	1	√	1	√

R51 1.5% ↑	0	X	2	√	1	√
R51 1.8% ↓	3	√	0	X	2	√
R52 2.3% ↑	0	X	0	X	1	√
R52 2.9%↓	0	X	0	X	0	X

ANALOG MULTIPLIER - in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)						
Various Detected Faults in MULTIPLIER in the presence of MULTIPLE faults with deviations						
Injected Faults	**N_{MC}=500, Avg_dif = 0.0103 Optimal Order - 16th**		**N_{MC}=1000, Avg_dif = 0.0108 Optimal Order - 15th**		**N_{MC}=2000, Avg_dif = 0.0110 Optimal Order - 15th**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
R11 8%↑ R12 10% ↑	5	√	6	√	3	√
R21 20% ↑ R22 15% ↓	6	√	5	√	2	√
R31 20% ↓ R32 20% ↑ R41 10% ↑	23	√	13	√	5	√
R52 30%↓ R51 20% ↑	5	√	5	√	7	√
R11 15%↑ R12 20% ↓ R42 18 %↑	78	√	57	√	37	√

4.4.4 Conclusion

The analog multiplier driven with slow-varying DC sweep inputs is successfully modelled using multivariate polynomial regression. Optimal polynomial orders of 16 and 15 ensure high-fidelity representation of the nonlinear behaviour. With fault-free bounds derived via Monte Carlo analysis, this approach enables robust detection of parametric deviations. It provides a reliable method for analog fault monitoring even under slowly changing input conditions, simulating real-world bias and control signal variations.

4.5 PI COMPENSATOR OF BUCK CONVERTER

Fig. 6 shows the peak current-mode controlled DC-DC buck converter using pulse width modulation (PWM) control IC UC3843 . One of the key functional blocks of the current mode controller is the PI compensator shown in Figure 25 and constructed using an error amplifier. This is required for the regulation of the output voltage. The output voltage, V_{out} of the power stage, is divided through resistor divider network R_{f1} and R_{f2} and then applied to the error amplifier, as shown in Fig. 26. The reference voltage V_{REF} = 2.5 V is applied to the non-inverting terminal of the error amplifier as a soft-start ramp with a rise time of 4ms.

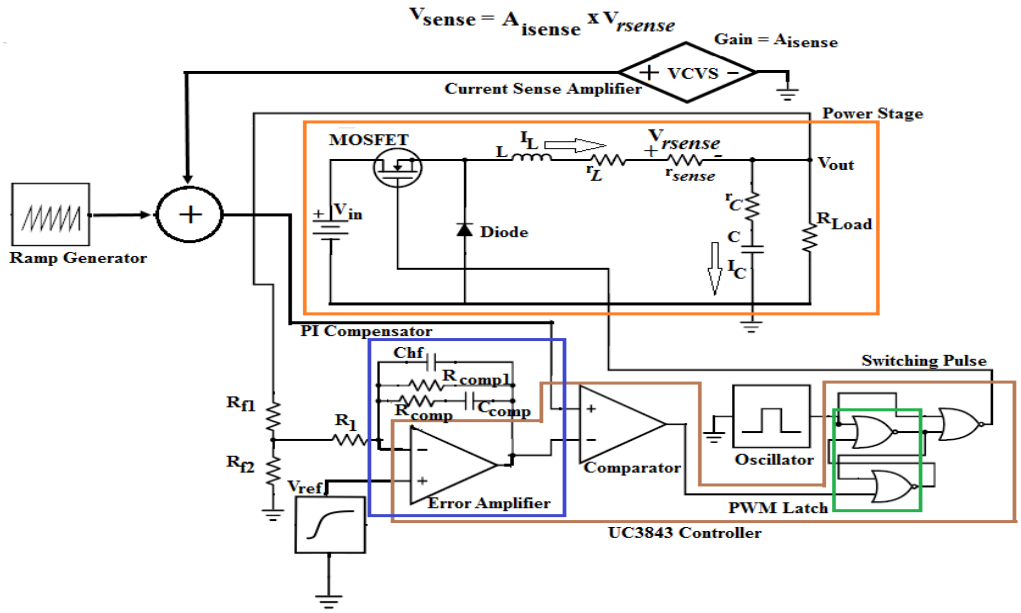

Fig. 25. Schematic of a current programmed control buck converter [21, 30-32].

The controller is the essential part of the converter to maintain the constant output. Therefore, the controller must be designed and tested correctly. We aim to detect the parametric fault of the controller part of the Buck converter circuit. Fig. 6 shows the discrete PI compensator of the Buck converter circuit.

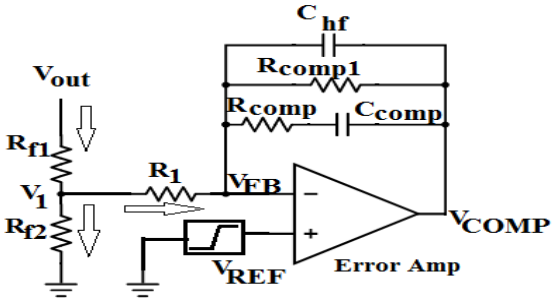

Fig. 26. PWM controller circuit of buck converter [21, 28, 30-32].

The nominal values of the circuit components of the PWM controller circuit shown in Fig. 26 are R_{f1}=9.76 kΩ, R_{f2}=3.25 kΩ, R_1=1kΩ, C_{hf}=30pF, C_{comp}=2nF, R_{comp1} =10 MΩ, R_{comp}=80 kΩ. The buck converter circuit is simulated for 1.5 ms in OrCAD Orcade with a maximum step size of 530ns with nominal component values, and the response of the PWM controller circuit is shown in Fig. 27.

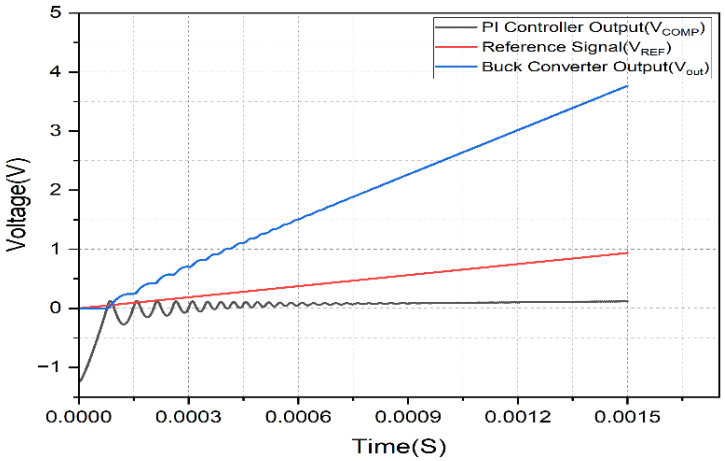

Fig. 27. Response of Buck converter and PWM controller circuit simulated in Orcade

4.5.1 Polynomial Modelling Using Optimal Order

Using the simulation data (VREF, Vout as inputs; VCOMP as output), **7th-degree** and **6th-degree** multivariate polynomial regression models are developed.

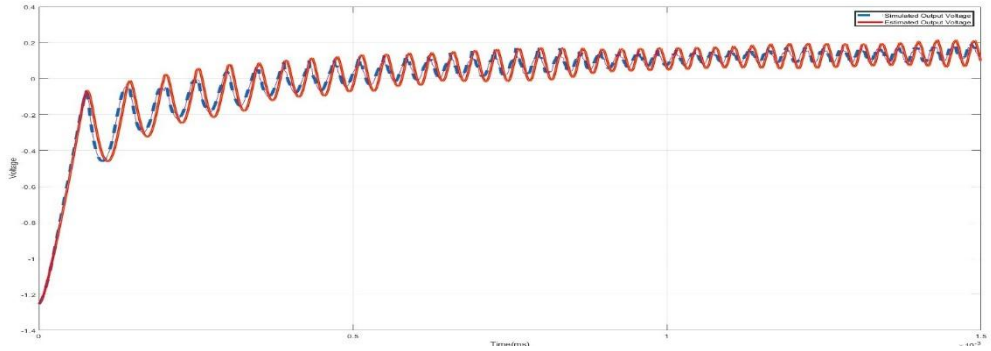

Fig 28:-Response of PI compensator in orcade vs polyfit model

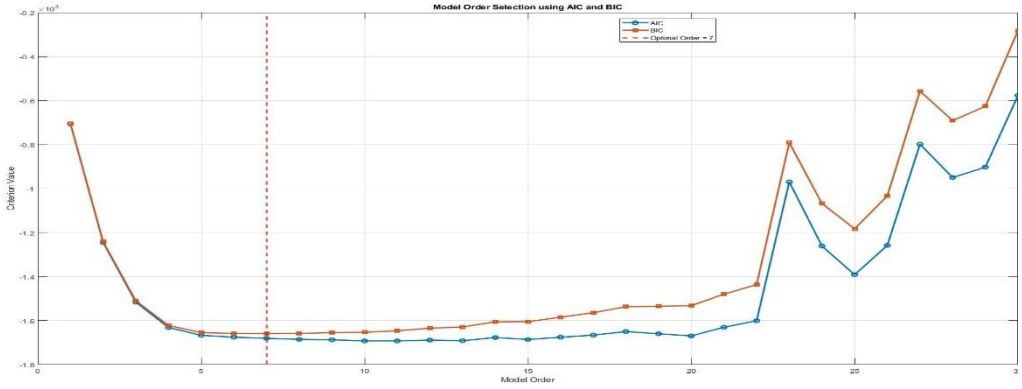

Fig 29:-Optimal order at Nmc=500

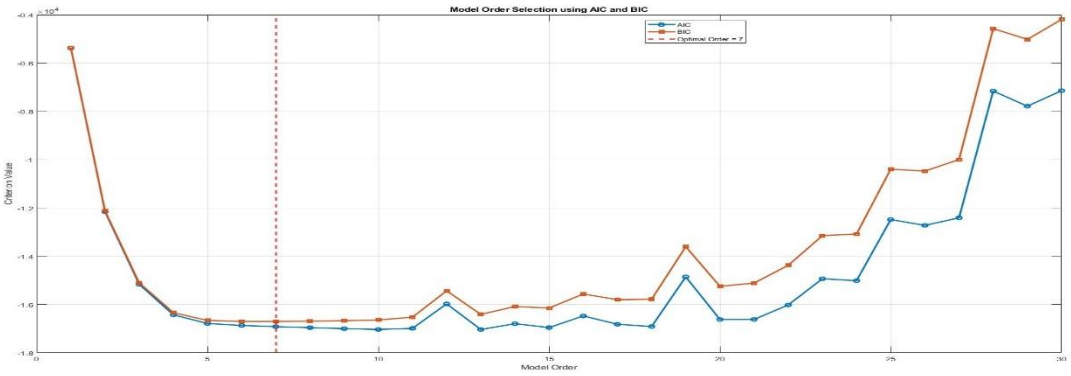

Fig 30:-Optimal order at Nmc=1000

Model Evaluation:

- **Optimal Polynomial Order**: **7th degree**, based on error minimization
- **Number of Coefficients (7th order)**: 36
- **Average modelling error**:
  - **7th order**: **0.0161**
  - **6th order**: **0.0162**

This confirms that the **7th-degree polynomial** is the most accurate and optimal for representing the PI controller behaviour.

Monte Carlo Fault-Free Bound Estimation:

- **NMC = 1000** samples
- Each Monte Carlo run generates **N = 247,459** time samples
- **Fault-free (FF) bounds** are computed using min–max spreads of coefficients
- These bounds are used to detect deviations under faulty conditions

4.5.2 Fault Detection Framework

The fault detection methodology includes both **single** and **multiple parametric fault injections**, with components perturbed beyond standard tolerance limits.

Detection Criterion:

A fault is **detected** if **any coefficient** in the 7th-order polynomial model deviates beyond its FF bounds.

Fault Classification:

- **Low-Level Faults**: <5%
- **Moderate Faults**: 5–15%
- **Severe Faults**: 15–50%
- **Multiple Faults**: More than one parameter simultaneously perturbed

4.5.3 Results

PI COMPENSATOR OF A BUCK CONVERTER								
Various Detected Faults PI controller in the presence of faults with deviations (5% – 15%) & (20%-50%)								
Injected Faults	**N_{MC}=500**				**N_{MC}=1000**			
	Optimal Order – 6th, Avg_dif =0.0162		**Optimal Order – 7th, Avg_dif =0.0161**		**Optimal Order – 6th, Avg_dif =0.0164**		**Optimal Order – 7th, Avg_dif =0.0162**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
R1 6% ↑	0	X	1	√	0	X	6	√
R1 5.5% ↓	0	X	1	√	0	X	26	√
R_{f2} 5.8% ↑	0	X	28	√	0	X	27	√
R_{f2} 6% ↓	5	√	35	√	5	√	1	√
R_{f1} 7% ↑	0	X	3	√	0	X	1	√
R_{f1} 8.5% ↓	0	X	4	√	0	X	32	√
R_{comp} 9% ↑	20	√	33	√	16	√	25	√
R_{comp} 6.8% ↓	26	√	16	√	26	√	35	√
R_{comp1} 7.5%↑	0	X	1	√	0	X	15	√
R_{comp1} 5.6%↓	0	X	1	√	0	X	35	√
C_{hf} 8% ↑	18	√	27	√	3	√	2	√
C_{hf} 10 % ↓	0	X	0	X	0	X	35	√
C_{comp} 6% ↑	1	√	2	√	1	√	7	√
C_{comp} 6% ↓	0	X	1	√	0	√	25	√
R1 43% ↑	1	√	2	√	1	√	5	√
R1 28% ↓	1	√	2	√	1	√	35	√
Rf2 35% ↑	22	√	7	√	18	√	35	√
Rf2 40% ↓	18	√	1	√	0	X	36	√
Rf1 30% ↑	26	√	33	√	26	√	35	√
Rf1 25% ↓	27	√	33	√	27	√	35	√
Rcomp 42% ↑	0	X	24	√	0	X	18	√
Rcomp 38% ↓	0	X	1	√	0	X	35	√
Rcomp1 37%↑	28	√	35	√	28	√	15	√
Rcomp1 40%↓	27	√	36	√	27	√	13	√
Chf 28% ↑	0	X	1	√	0	X	8	√
Chf 35% ↓	0	X	1	√	0	X	35	√

Ccomp 32% ↑	27	√	35	√	27	√	35	√
Ccomp45%↓	28	√	36	√	28	√	34	√

PI COMPENSATOR OF A BUCK CONVERTER								
Various Detected Faults PI controller in the presence of faults with deviations (>5%)								
Injected Faults	**N_{MC}=500**				**N_{MC}=1000**			
	Optimal Order – 6th, Avg_dif =0.0162		**Optimal Order – 7th, Avg_dif =0.0161**		**Optimal Order – 6th, Avg_dif =0.0164**		**Optimal Order – 7th, Avg_dif =0.0162**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
Rf1 2%↓	0	X	0	X	0	X	0	X
Rf2 1% ↑	0	X	14	√	0	X	14	√
R1 3% ↑	0	X	0	X	0	X	1	√
Chf 3% ↓	0	X	12	√	0	X	14	√
Rcomp1 2.5% ↑	0	X	34	√	0	X	12	√
Rcomp 3.5% ↓	0	X	0	X	0	X	0	X
Ccomp2% ↑	0	X	15	√	0	X	11	√
R1 2% ↓	0	X	0	X	0	X	0	X
Rcomp1 1.5% ↓	0	X	0	X	0	X	1	√
Rcomp 2%↑	0	X	0	X	0	X	0	X

PI COMPENSATOR OF A BUCK CONVERTER								
Various Detected Faults PI controller in the presence of MULTIPLE faults with deviations								
Injected Faults	**N_{MC}=500**				**N_{MC}=1000**			
	Optimal Order – 6th, Avg_dif =0.0162		**Optimal Order – 7th, Avg_dif =0.0161**		**Optimal Order – 6th, Avg_dif =0.0164**		**Optimal Order – 7th, Avg_dif =0.0162**	
	No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
Ccomp 10%↓ Chf 20%↑ R1 12%↓	24	√	24	√	24	√	36	√

R1 11%↓ Rcomp1 22%↑ Rcomp=13 %↓	27	√	35	√	27	√	35	√
Rcomp1 9%↓ Rcomp 13%↑ Rf1 18% ↑ Rf2 8% ↓	4	√	0	X	1	√	35	√
Ccomp 15%↓ Chf 11%↑ Rf1 9% ↓ Rf2 19% ↑	3	√	2	√	2	√	36	√
R1 8%↑ Rf1 12% ↓ Rf2 14% ↑	27	√	35	√	27	√	34	√

4.5.4 Conclusion

The **7th-degree polynomial model** is confirmed as the **optimal** choice for accurately representing the PI controller in a Buck converter. This fault detection framework, based on polynomial regression and Monte Carlo FF bounds, enables:

- Accurate detection of **moderate and severe faults**
- Partial success in detecting **low-level faults** (improved with increased NMC)
- Effective diagnosis of **multiple simultaneous faults**
- High-resolution detection through **36 polynomial coefficients**

This case study validates a **scalable, model-based approach** for robust analog fault detection in nonlinear circuits like buck converters.

Chapter 5

Noise Analysis

5.1 Importance of Noise Simulation

In real-world analog systems, signal behaviour is rarely ideal. Noise—both **transient and steady-state**—is inherently present due to thermal effects, power supply fluctuations, crosstalk, and environmental factors. These sources introduce deviations in voltages, currents, and timing characteristics, often mimicking the behavior of low-level faults or distorting signal integrity.

Therefore, any test methodology intended for analog fault detection must demonstrate robustness not only under ideal (noise-free) conditions but also in the presence of noise. Simulating noise within controlled bounds helps to:

- Emulate real operating environments
- Study the **sensitivity of regression coefficients** to noise
- Verify that the fault detection framework does **not produce false positives** due to noise alone
- Quantify how far faults must deviate from the nominal to be reliably detected under noisy conditions

5.2 Noise Simulation Techniques

5.2.1 Random Noise Source (Transient Analysis)

A voltage or current source is defined with both a DC value and a **time-varying noise amplitude**, typically using the `VALUE = VDC + NOISE` syntax.

- **Effect**: Produces fluctuating values at each simulation time step
- **Example**:
- `VNOISE = 1 + (0.2 * (2 * (RND - 0.5)))`
- Simulates a **1V ±0.2V** signal (i.e., range from 0.8V to 1.2V)

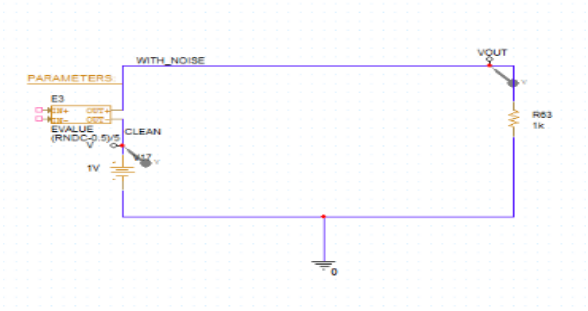

Fig 31:-Circuit for noise analysis

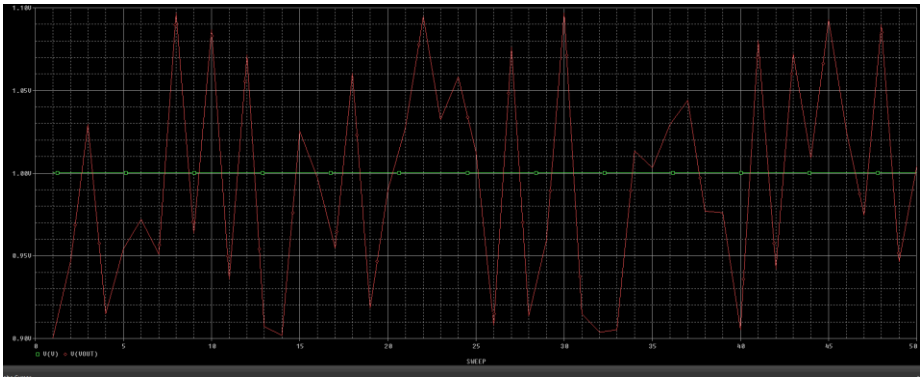

Fig 32:-Simulation with random noise

5.2.2 RNDR Function (Constant Random Value in Time)

Used for injecting a **fixed but randomly selected offset** at the beginning of simulation that stays constant throughout the simulation run.

- **Effect**: Creates a static bias noise per simulation

  `VNOISE = (RNDR - 0.5) / 5 → ±0.1V constant noise`

  This simulates device mismatches or static supply offsets.

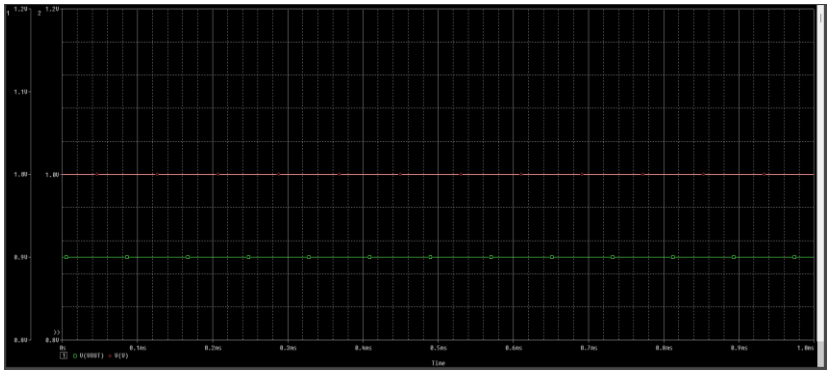

Fig 33:-Simulation with RNDR noise

5.2.3 RNDC Function

Generates a **new random value for each simulation run**, ideal for Monte Carlo and DC sweep-based coefficient extraction.

- **Effect**: Captures run-to-run noise variations
- `PARAM Vnoise = RNDC * 0.2`

This was particularly useful for simulating **parameter noise** during the Monte Carlo estimation of fault-free (FF) bounds.

5.3 Comparison: With vs Without Noise

LEADLAG - in case of AC INPUT(SINE WAVE) with NOISE					
Various Detected Faults in LEADLAG in the presence of faults with deviations (5% – 15%) & (20%-47%)					
N_{MC}=500, Avg_dif = 0.0420, Optimal Order – 18th					
Injected Faults		**WITHOUT NOISE**		**WITH NOISE**	
		No. of Coefficients Out of Bound	**Fault Detection Status**	**No. of Coefficients Out of Bound**	**Fault Detection Status**
R1 12%↑		113	√	151	√
R1 8% ↓		1	√	73	√
R2 9% ↑		0	X	63	√
R2 6% ↓		0	X	64	√
R3 10% ↑		71	√	61	√
R3 7%↓		0	X	100	√
C1 13%↑		0	X	66	√
C1 15% ↓		3	√	63	√
C2 11% ↑		0	X	62	√
C2 14% ↓		10	√	71	√
R1 20%↑		163	√	170	√
R1 30% ↓		183	√	179	√
R2 32% ↑		34	√	73	√
R2 40% ↓		104	√	124	√
R3 25% ↑		174	√	161	√
R3 45%↓		185	√	182	√
C1 42%↑		17	√	77	√
C1 25% ↓		15	√	72	√
C2 35% ↑		38	√	72	√
C2 47% ↓		140	√	149	√

5.4 Conclusion and Takeaway

Noise simulation was critical in verifying the **practical robustness** of the proposed fault detection methodology. By incorporating both **random time-varying** and **fixed bias** noise into the simulation framework:

- The approach demonstrated **fault resilience** under realistic conditions.

- It maintained **high detection accuracy** without triggering false alarms.
- It ensured that **fault-free Monte Carlo bounds** account for both component tolerances and ambient noise behaviour.

In conclusion, simulating noise adds a necessary layer of validation and ensures that this coefficient-based regression method remains **viable and reliable** in real-world test environments where perfect signal integrity cannot be assumed.

Chapter 6

Conclusion

6.1 Summary of Work

This thesis presents a robust and simulation-driven methodology for detecting **single parametric faults** in **multi-input Analog circuits** using **polynomial regression modelling**. The central idea lies in expressing the output of an analog circuit under test (CUT) as a **multivariate polynomial function** of its inputs. The coefficients of this polynomial are estimated through least squares regression, and their stability is assessed under both fault-free and faulty conditions.

To establish a baseline, **Monte Carlo simulations** were used to derive **fault-free (FF) bounds** for each coefficient, considering typical manufacturing tolerances. Any observed deviation of coefficients beyond these statistical boundaries was flagged as a fault. The detection approach was validated across three representative analog systems:

- A **lead-lag filter** (linear, dual-input)
- A **PI compensator in a buck converter** (linear, single-input control system)
- A **four-quadrant analog multiplier** (nonlinear, dual-input)

Each CUT was tested under both **sinusoidal** and **slow DC sweep** input scenarios. The methodology proved capable of accurately capturing circuit behaviour across different operating conditions and reliably detecting single faults—even at low fault levels.

6.2 Key Findings

- **Polynomial Coefficient-Based Fault Detection**
  The work demonstrates that circuit faults manifest as detectable deviations in a subset of polynomial coefficients, providing a powerful non-invasive test strategy. The proposed technique requires no circuit augmentation, relying solely on simulation outputs.
- **Support for Nonlinear Circuits**
  The inclusion of the analog multiplier validated the method's capability in handling nonlinear circuit behavior. Despite increased complexity and nonlinearity, the polynomial model (with optimal degree) captured the output accurately, and fault detection remained reliable.
- **Optimal Order Selection via AIC/BIC**
  To avoid overfitting and unnecessary computation, Akaike Information Criterion (AIC) and Bayesian Information Criterion (BIC) were used to determine the optimal order of the polynomial regression. This helped control the number of coefficients while maintaining a high degree of model fidelity.
- **Noise Robustness Validation**
  The circuits were subjected to both transient and static noise, modeled using techniques like random noise sources, RNDR, and RNDC functions in Orcade. The noise-injected simulations confirmed that:
- **Input Versatility**
  Testing under both sinusoidal and slow DC sweep (ramp) inputs revealed that:
    - Fault detectability is preserved under varying signal types
    - DC sweep inputs help in capturing low-frequency and drift-type faults, useful in control systems
- **Scalability and Simplicity**
  Though high-order models (up to 22nd degree) were used, it was found that only a small set of dominant coefficients is often sufficient for reliable fault detection, allowing future reductions in computational cost.

6.3 Future Scope

While the simulation-based results are promising, the following aspects remain open for future research and enhancement:

- **Hardware validation**: Currently, the technique is validated only through simulation. Experimental validation on fabricated or prototype circuits will be crucial to confirm the method's robustness against real-world non-idealities such as noise, temperature drift, and parasitics.
- **Fault diagnosis**: The current work focuses on fault detection. Extending the method for **fault localization and classification** using sensitivity of specific polynomial coefficients to component deviations can help in fault diagnosis.
- **Model simplification**: Reducing the polynomial model order without sacrificing accuracy—by selecting only dominant coefficients or using compressed sensing—can make the method more scalable.
- **Online or real-time testing**: With further optimization, this technique may be embedded in **on-chip monitoring systems** or **mixed-signal test platforms** for adaptive, low-cost analog testing in industry.

Final Remark

This project establishes a data-driven, statistically sound, and scalable methodology for analog fault detection using polynomial regression modelling. It demonstrates high fault coverage across linear and nonlinear circuits, resilience against noise, and adaptability to various input signal types. The proposed framework bridges a significant gap in analog testing by offering a **low-cost, high-accuracy** solution without requiring test-point augmentation or invasive probing. It opens new possibilities for **robust analog test strategies** in both academic research and industrial product development.s

Chapter 7

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