**FAULT DETECTION IN MULTI-INPUT ANALOG CIRCUITS USING POLYNOMIAL REGRESSION MODELLING**

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INDIAN INSTITUTE OF TECHNOLOGY (ISM), DHANBAD DEPARTMENT OF ELECTRONICS ENGINEERING

Under the Guidance of Presented by

**Dr. Rahul Bhattacharya Simran Gupta**

**Dept. of Electronics Engineering SRIS Research Intern**

**IIT (ISM) Dhanbad B.Tech (ECE)**

**NIT JAMSHEDPUR**

**CANDIDATE’S DECLARATION**

We hereby declare that

1. The work contained in this report is original and has been done by us under the guidance of our supervisor **Dr. Rahul Bhattacharya***,* Professor, Department of Electronics Engineering, IIT(ISM) Dhanbad.
2. The work has not been submitted to any other Institute for any degree or diploma.
3. I have followed all the guidelines provided by the Institute in preparing the report.
4. I have conformed to the norms and guideline given in the Ethical Code of Conduct of my Institute.
5. Wherever I have used materials (data, theoretical analysis, figures and texts) from other sources, I have given due credit to them by citing them in the project report and giving their details in the reference. Further I have taken permission from the copyright owners of the sources, wherever necessary.

Signature of the Student

SIMRAN GUPTA

**DEPARTMENT OF ELECTRONICS ENGINEERING**

**INDIAN INSTITUTE OF TECHNOLOGY (ISM), DHANBAD**

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**CERTIFICATE**

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This is to certify that the project report titled **“Fault Detection in Multi-Input Analog Circuits Using Polynomial Regression Modeling”**, submitted by **Simran Gupta (2022UGEC063)** to the **Indian Institute of Technology (Indian School of Mines)**, in partial fulfilment of the requirements for the award of the degree of **Bachelor of Technology in Electronics and Communication Engineering**, is a bona fide record of the research work carried out under my supervision.

To the best of my knowledge, the contents of this report, in full or in part, have not been submitted to any other institute or university for the award of any degree or diploma.

Examined and Approved

**Faculty Supervisor**  **Head of Department (ECE)**

**ACKNOWLEDGEMENT**

This research work is one of the significant achievements in my life and is made possible because of the unending encouragement and motivation given by so many in every part of my life. It is immense pleasure to have this opportunity to express my gratitude and regards to them.

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Simran Gupta

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**Abstract**

This report presents a comprehensive methodology for detecting single parametric faults in multi-input Analog circuits using polynomial regression modelling. Analog circuits, especially in mixed-signal systems, are notoriously difficult to test due to nonlinear behaviour, limited test access, and high sensitivity to manufacturing variations. Traditional specification-based methods often fall short in cost-efficiency and fault coverage. To address these challenges, this work proposes a regression-based fault detection approach wherein the output of the circuit under test (CUT) is expressed as a polynomial function of multiple input variables, derived through Taylor series expansion.

The coefficients of this polynomial model are computed using traditional least squares techniques, and fault-free (FF) coefficient bounds are established via Monte Carlo simulations under nominal tolerance variations. During testing, any deviation of the estimated coefficients beyond these predefined FF bounds is indicative of a parametric fault. To further enhance sensitivity, the V-Transform technique is employed, exponentially amplifying small coefficient changes and enabling accurate fault detection even under noise.

The methodology is validated through three case studies involving both linear and nonlinear Analog circuits: a lead-lag filter, a four-quadrant Analog multiplier, and a PI compensator in a buck converter. Each circuit is evaluated under sine and slow ramp (slowDC) input conditions. Results confirm that the proposed technique reliably detects single parametric faults—including small deviations—with high accuracy, even in the presence of additive noise. The approach thus demonstrates strong potential as a low-cost, simulation-based test framework for Analog and mixed-signal fault detection.

**Chapter 1**

**INTRODUCTION**

**1.1 OVERVIEW**

The testing and diagnosis of Analog circuits are central challenges in the post-manufacturing validation phase of electronic systems. Unlike digital circuits, Analog circuits do not possess straightforward fault models such as stuck-at faults. Analog behaviour is sensitive to manufacturing process variations and environmental influences, making fault detection and classification both critical and complex.

Due to the wide range of applications of electronic circuits in recent years, testing of electronic circuits, especially Analog circuits, has become a major concern in ensuring fault-free systems. The absence of a standard Analog fault model comparable to the digital stuck-at model complicates the testing process. Analog fault models are generally categorized as either catastrophic or parametric faults. Several techniques for Analog fault detection have been proposed in literature, with surveys highlighting high-tech approaches for diagnosis and classification.

Declaring when a circuit or component is faulty remains a challenging decision in Analog testing. Parametric fault diagnosis and tolerance are especially difficult because component variations may not cause total circuit failure but lead to degraded or incorrect functionality. C. Yang et al. approached soft fault diagnosis by estimating circuit parameters using test stimulus responses and slope fault models. In a related work, genetic algorithms were employed to identify faulty components by analyzing the transfer function and bounding behaviour.

A variety of parametric detection methods exist, including those that evaluate probability density functions (Bhattacharyya coefficients), impulse responses, and regression-based models. Notably, Z. Guo and J. Savir used auto-regression models to predict and compare coefficients, while others have applied machine learning, such as support vector machines and manifold learning, for classification. T. Zhang and T. Li even used noise signatures as diagnostic features.

Various frequency response-based techniques also exist. For example, signal flow graph (SFG) analysis has been used to simulate faults and derive tolerances. The Levenberg-Marquardt method and k-nearest neighbors (K-NN) classifiers have also been used in fault classification based on natural frequency and gain.

Despite significant research, most approaches are limited to single-input, single-output Analog systems such as Sallen Key filters, low pass filters, leapfrog filters, or elliptic filters. These typically involve op-amps in single-ended configurations with grounded non-inverting inputs. However, modern Analog systems often feature double-ended operation and limited test access, making internal fault detection challenging.

A promising direction is regression-based signature analysis, where the circuit output is expressed as a polynomial function of multiple input voltages. The coefficients of this polynomial, estimated using classical linear least squares techniques, serve as fault signatures. Taylor series expansions help derive these polynomial models. The addition of the V-Transform method, which amplifies fault sensitivity by modifying coefficients into monotonic exponential forms, further improves diagnostic capability.

This report proposes and validates a novel methodology using polynomial regression and V-Transform for fault detection in multi-input Analog circuits. Multiple input conditions, including sine and slowDC signals, are analyzed, and the effects of noise are also incorporated to evaluate model robustness.

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**1.2 MOTIVATION**

Despite extensive efforts in Analog fault detection research, several critical challenges persist, motivating the need for this study:

1. Lack of Standard Fault Models: Unlike digital systems, Analog circuits lack simple and standardized fault models. Each component’s deviation must be analyzed individually.
2. Complex Fault Behaviour: Analog faults do not typically manifest as binary outcomes but influence circuit behaviour in continuous and complex ways. This includes shifts in gain, offset, or bandwidth.
3. Limited Observability: Many practical Analog circuits have restricted nodes for measurement. With limited probing access, internal faults are difficult to observe and diagnose.
4. High Cost of Accurate Testing: Creating high-precision Analog test equipment is expensive and often not scalable across diverse circuit topologies.
5. Insufficiency of Single-Input Approaches: Most existing methods cater to single-input Analog circuits. However, real-world applications frequently involve multi-input configurations that require more sophisticated analysis.

To address these issues, this work explores polynomial regression modeling of multi-input circuits, combining classical estimation with V-Transform-based sensitivity analysis. By simulating the tolerance range of each circuit parameter using Monte Carlo (MC) simulations, the fault-free bounds for each regression coefficient are established. During testing, coefficients computed from faulty conditions are compared with these bounds. Any significant deviation is flagged as a fault.

The report further extends this methodology to nonlinear Analog circuits such as four-quadrant multipliers and switching converter controllers. The inclusion of V-Transform coefficients increases sensitivity to component drift and helps distinguish genuine faults from natural parameter variation or noise. Ultimately, this regression-based technique aims to deliver an accessible, simulation-based, non-invasive, and highly adaptable fault detection solution for Analog and mixed-signal systems.

* 1. **LITERATURE REVIEW**

A wide array of methodologies has been proposed over the years for Analog fault detection. The earliest approaches were predominantly specification-based, focusing on checking whether a circuit's output met predefined parameters. While these methods were effective for simpler circuits, they proved insufficient for complex or sensitive Analog systems.

Later advancements introduced model-based testing, statistical fault detection, and signal analysis techniques. Notably, slope-based models as proposed by C. Yang used the rate of change in response signals to identify faults. Genetic algorithms and soft computing methods also emerged as diagnostic tools for identifying faulty elements through optimization and pattern matching.

Among statistical techniques, regression-based models became popular due to their ability to model circuit behaviour with compact polynomial signatures. Z. Guo and J. Savir, for instance, employed autoregressive (AR) models to detect parameter shifts in circuit output. More sophisticated machine learning classifiers such as support vector machines (SVMs), manifold learning, and K-nearest neighbours (KNN) have also been applied, offering promising results for fault classification.

Additionally, Bhattacharyya coefficient-based approaches have been used for fault detection by measuring differences in probability distributions under fault-free and faulty conditions. T. Zhang and T. Li demonstrated the use of noise signatures as reliable indicators of Analog faults.

Frequency-based methods were explored by Kavithamani et al., who used frequency response shifts to identify parametric deviations. SFG (Signal Flow Graph) methods and Levenberg-Marquardt optimization have also been applied to model behaviour under fault conditions.

Despite these innovations, many techniques have focused on single-input, single-output systems such as low-pass filters, Sallen-Key circuits, and elliptic filters. These configurations do not reflect the operational complexity of modern Analog systems that often involve multi-input circuits and nonlinear behaviour.

The current work builds upon previous polynomial-based methods and expands their applicability to multi-input Analog systems. The methodology uses Taylor series expansion and least squares regression to model output as a function of multiple inputs, with V-Transform coefficients enhancing sensitivity to subtle parameter changes. Unlike many earlier studies, the proposed approach incorporates Monte Carlo-based FF bounds, rigorous polynomial degree selection (AIC/BIC), and testing under noisy conditions to ensure robustness and relia

**Chapter 2**

**THEORETICAL STUDY**

**2.1 —** **Theory of Multiple Linear Regression**

The output Vout of an Analog circuit can be expressed as a polynomial using a Taylor series expansion [22] in terms of two input voltage sources, Vin1, and Vin2 about the nominal values Vin1 = V1 and Vin2 = V2 as follows:

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+++ . . . . . . (1)

Where and all its partial derivatives , , and so on are continuous and exist at nominal values Vin1 = V1 and Vin2 = V2 .

So, the Taylor polynomial which can represent Vout around the nominal values Vin1 = V1 and Vin2 = V2 can be generalized up to its mth degree term as follows.

(2)

Eqn. (1) can be further approximated as

………+ℇ (3)

Eqn. (3) can be further generalized as follows.

+ℇ (4)

Where r = and *a0*, *a1, a2* etc.are the real-valued coefficients ∀ *i* = 0 to k and ∀ *k* = 0 to *m*. ℇ is the truncation error. The number of coefficients for an mth degree polynomial regression model which can estimate the output of a two-input CUT can be given as

Ncoeff  (5)

The coefficients *a****i***'s in Eqn. (3) cannot be exact to that of Eqn. (1), as Eqn. (3) comprises only a finite number of terms for what is essentially a truncated Taylor series. Eqn. (3) is a linear regression model that describes the relationship between circuit output voltage Vout and two input voltages, Vin1 and Vin2. Judicious selection of the coefficients *a0* and *a****i***'s of a polynomial regression model in Eqn. (3) using traditional linear least squares techniques minimizes truncation error ε. The accuracy of the regression model depends on the degree of the polynomial expansion used in practice. The traditional methods in MATLAB to estimate a linear regression model. This work uses MATLAB Polyfitn library to solve the coefficients of a polynomial regression model using classical linear least square techniques. Several numerical methods are used to implement the *Polyfitn* library. However, to obtain a more stable solution, reasonably efficient QR factorization with pivoting is introduced to build the *Polyfitn* library. Any multi-input analog circuit, in general, can be represented using this model. The technique applies equally well to linear and non-linear circuits.

**2.2 —** **Goodness-of-Fit and Optimal Polynomial Order**

The accuracy and reliability of any regression-based fault detection method heavily depend on selecting an appropriate degree for the polynomial model. An optimal order ensures the model captures the essential nonlinear relationships between input and output without becoming overly complex or too simplistic.

**Overfitting**

Overfitting occurs when the polynomial model has too high a degree. While it may fit the training data (simulated outputs) very well, it also captures noise and minute fluctuations that are not representative of actual circuit behaviour. This leads to poor generalization and may increase false positives during testing.

**Role of Optimal Order Selection**

To ensure that the polynomial model neither overfits nor underfits, a quantitative method is used to evaluate model quality: the **goodness-of-fit**. In this work, we assess fit quality using **information criteria**—statistical tools that account for both the error of the model and its complexity.

**Akaike Information Criterion (AIC)**

The AIC is defined as:  
  
**AIC = n × ln(MSE) + 2k**

Where:

* *n* = number of data points
* *MSE* = mean squared error of the regression model
* *k* = number of regression coefficients

A lower AIC value indicates a better trade-off between model accuracy and simplicity.

**Bayesian Information Criterion (BIC)**

BIC introduces a stronger penalty on model complexity and is defined as:  
  
**BIC = n × ln(MSE) + k × ln(n)**

While similar to AIC, BIC is generally more conservative and prevents overfitting in models with limited datasets.

**Why AIC/BIC is Preferred**

Unlike basic metrics such as RMSE (root mean square error), which only evaluate model fit, AIC and BIC penalize excessive complexity. This makes them better suited for model order selection in fault detection applications where robustness and reliability are critical.

In this report, both AIC and BIC were used to determine the best polynomial order for each circuit case study. Orders producing the lowest AIC and BIC values were chosen for modeling and further analysis. This ensured a balance between sensitivity to faults and resilience to noise or variability in circuit response.

**Chapter 3**

**FAULT DETECTION PROCEDURE**

For fault detection, we assume that normal parameter variations (normal drift) in a fault free circuit are within a fraction α of their nominal value, where 0 < α << 1. That is, every parameter pj is allowed to vary within the hypercube pj,nom(1 − α) < pj < pj,nom(1 + α) ∀ *j*, where pj;nom is the nominal value of the circuit parameter pj. Any change in the value of one or more parameters of an Analog circuit results in a change in one or more coefficient values of its polynomial regression model described by Eqn.(3), (4). The proposed approach mainly consists of two steps, estimation of fault free coefficient bounds for polynomial regression model followed by fault injection and fault detection. Using Monte-Carlo simulation, the minimum and maximum values of regression model coefficients can be obtained by varying each parameter pj within its tolerance limit. Let apm,min and apm,max are the minimum and maximum values of pth coefficient (∀ p = 0 to Ncoeff -1) in mth degree regression model obtained after NMC number of MC runs by varying all parameter within their tolerance limits. Due to a parametric fault, whenever any circuit component value slips outside its tolerance, one or more coefficient values of mth degree polynomial regression model change and likely to slip outside the hypercube apm,min < apm < apm,max for any p, 0 ≤ p ≤ Ncoeff -1. As a result, we get a different set of coefficients reflecting a detectable fault. The probability that at least one coefficient falls outside the hypercube depends on the degree of the regression model and how precisely the boundary of the coefficient hypercube can be determined.

**3.1-- *Estimation of Fault free Polynomial Coefficients and their Bounds***

For the derivation of polynomial coefficients, the CUT is first simulated in PSpice [26] with a nominal value of the circuit components. Using PSpice simulation data for Vin1,Vin2, and Vout, a polynomial regression model of the form given by Eqn. (3) or (4) is obtained using MATLAB *Polyfitn* function. The polynomial coefficients, thus obtained, are fault free coefficients at nominal component values.

* + 1. ***Computation of Fault free Coefficient Bounds***

To calculate fault free (FF) bounds of coefficients, the CUT is simulated using the Monte-Carlo simulation [26, 27], where each of the circuit parameters is varied within the specified tolerance range (±5%) [16] for which the circuit output voltage Vout is considered to be fault free, and the polynomial coefficients for a given degree of regression model are estimated at each MC simulation run. Thus, for NMC number of MC runs, the same number of different polynomial regression models of a given degree can be estimated. Comparing all such coefficients, the lower and upper bounds of each coefficient corresponding to each term of the polynomial can be obtained. Fig. 1 outlines the procedure to find the fault free bound of polynomial coefficients. It may be noted that the limits of output voltage Vout\_max and Vout\_min for a fault free circuit whose component values can be varied within the specified tolerance range, can also be obtained from NMC number of MC samples. So, FF bounds of polynomial coefficients for a given degree of regression model cover the limits of fault free output voltage. Because, Vout\_max and Vout\_min for a fault free circuit lie in the MC samples. For any ith MC simulation run, the goodness-of-fit for a given degree of regression model can be evaluated with the help of a metric, namely, the percentage of average difference [19]. The percentage of average difference, Avg\_dififor ith MC simulation run can bedefined as follows.

(6)

where Vout(k) and VoutP(k) are the SPICE simulated output signal and predicted output signal at kth time instant respectively. *N* represents the number of timed samples generated by the simulator in each MC simulation run and depends on the simulator type and simulation parameters such as maximum step size, start and stop time of simulation etc. is the peak-to-peak amplitude of the SPICE simulated output Vout.

For NMC number of MC simulation runs, the percentage of average difference can be given as

(7)

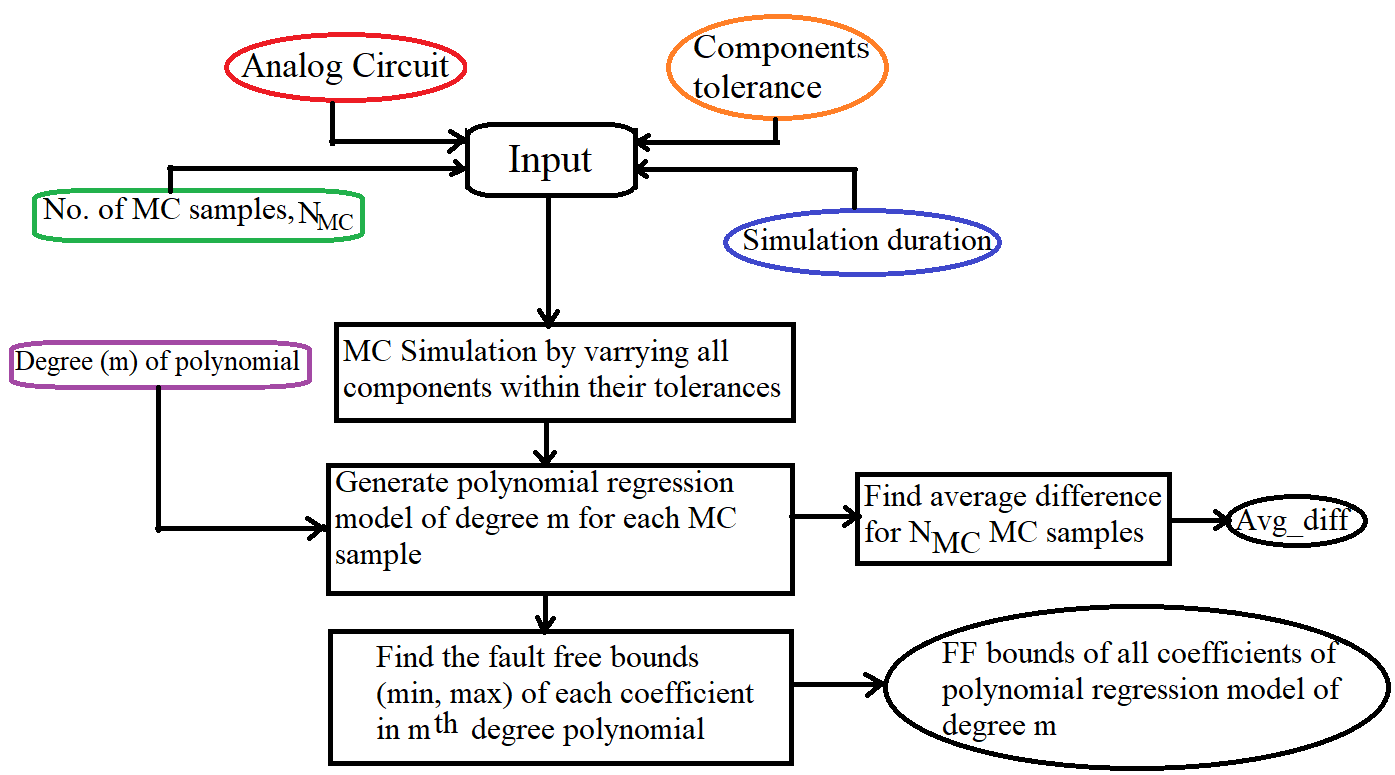
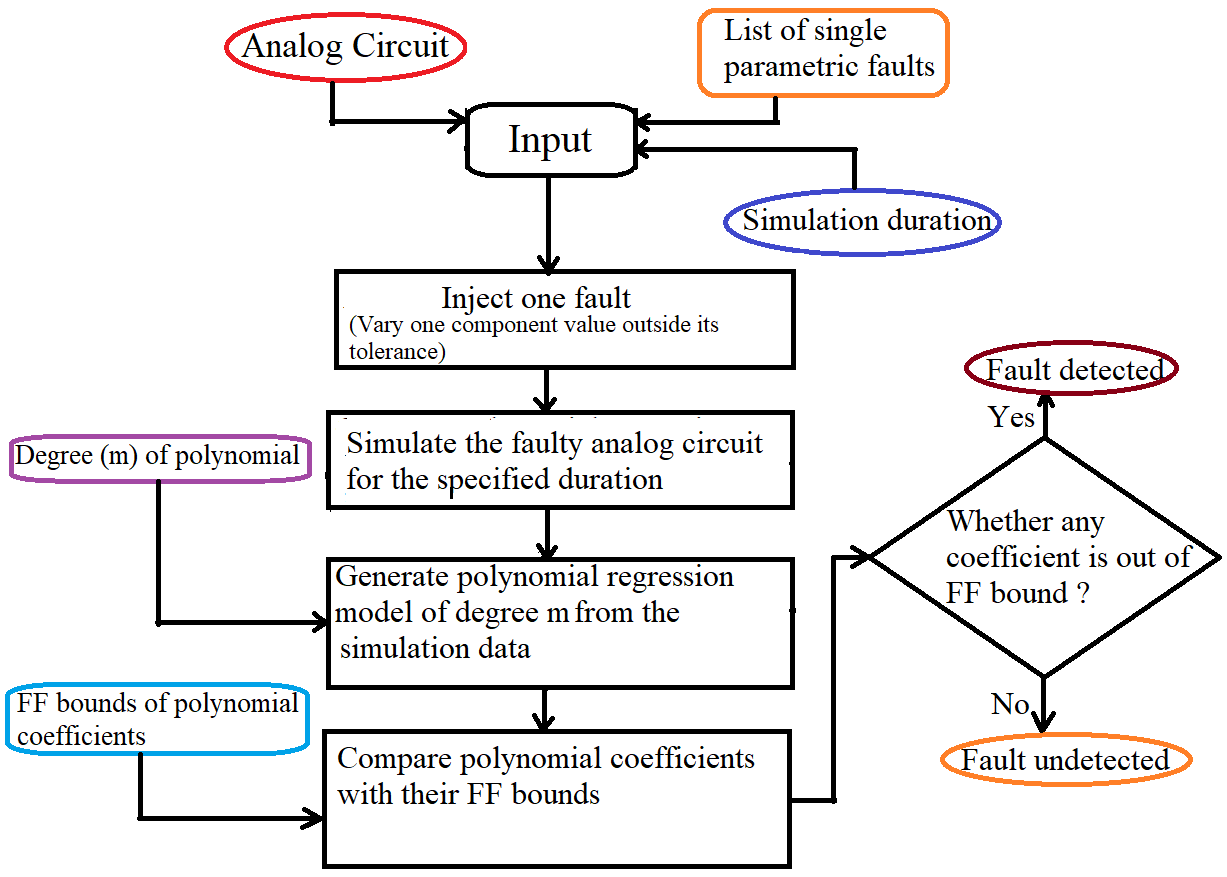


Fig. 1. Flow chart for computation of fault free coefficient bounds

* 1. ***-* Fault Modelling and Fault Detection Strategy**

It is noteworthy that only single parametric faults are considered in this paper. The operational amplifier used in the circuit is assumed to be fault free. The CUT is assumed to be fault free when the resistors and capacitor values vary within the tolerance limits (±5%). A single parametric fault is injected by varying one of the circuit parameters outside its tolerance limits, followed by PSpice simulation. Polynomial coefficients of the regression model for the faulty CUT are estimated using MATLAB *Polyfitn* function. The estimated polynomial coefficients of the faulty CUT are compared with the fault free coefficient bounds. If any of the estimated polynomial coefficients are found to lie outside its fault free bounds, the fault is said to be detected. On the contrary, if all of the coefficients are found to fall in the range, no conclusion can be drawn about whether the CUT is faulty or fault free. Fig. 2 outlines the fault detection procedure. However, in most cases, it is observed that if the CUT passes the polynomial coefficient-based fault detection test, the CUT can be declared fault free with a higher probability [14].



**Fig. 2. Flow chart for fault detection in analog circuits**

**Chapter 4**

**CASE STUDY**

This chapter presents the application of the proposed fault detection methodology on three representative Analog circuits. Each circuit is analyzed under multiple input conditions, including sinusoidal and slow-ramping DC (slowDC), using polynomial regression models to detect single parametric faults. The study covers both linear and nonlinear Analog circuits:

**4.1 CASE STUDY 1 – LEAD-LAG CIRCUIT**

Our project addresses the demand for high-speed multipliers and also contributes to the realm of efficient multiplication by leveraging Vedic Mathematics.

The implementation of an 8-bit multiplier using Xilinx Vivado software demonstrates the effectiveness of Vedic mathematics techniques in digital design. Through the use of the Urdhva-Tiryagbhyam Sutra and various architectures, we aimed to achieve high-speed multiplication with reduced delay and power consumption.

Our simulations in Vivado showed that the Vedic multiplier using different architectures resulted in varying combinational delays. Among the architectures tested, the Vedic Multiplier for 8x8 Bit using vedic method exhibited the lowest combinational delay, indicating its potential for high-speed multiplication.

The results confirm the advantages of using Vedic mathematics in digital design. By leveraging ancient mathematical principles, we were able to create efficient multipliers that outperform conventional methods in terms of speed and resource utilization.

As the number of steps in multiplication is reduced, delay is reduced and hence speed of the multiplier increases. Vedic Algorithm like Urdhav Tiryagbhyam is best suited for high speed application

.Ease of implementation of the design shows that complex modules for DSP and image processing can be simplified using Vedic algorithm.

**4.2 SCOPE OF FUTURE WORK**

In future we will do simulations and synthesis analyses in Vivado showing the Vedic multiplier using different architectures resulting in varying combinational delays.

Vivado will be employed to perform place and route optimization of the synthesized design onto the targeted FPGA device. This optimization step is crucial for achieving optimal performance and resource utilization of the multiplier design.

Overall, In future our aim is to deliver a fully functional 8x8 Vedic multiplier implementation on FPGA, ensuring efficient resource utilization, reliable performance, and adherence to project requirements.

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|  |  |
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**4.3 APPENDIX**

Verilog code for 8-bit Vedic multiplier

module ha(a,b,sum,carry);

input a,b;

output sum,carry;

xor(sum,a,b);

and(carry,a,b);

endmodule

module add\_4\_bit (a,b,sum);

input [3:0] a,b;

output [3:0]sum;

assign sum=a+b;

endmodule

module add\_6\_bit (a,b,sum);

input [5:0] a,b;

output [5:0] sum;

assign sum = a+b;

endmodule

module add\_8\_bit (a,b,sum);

input[7:0] a,b;

output[7:0] sum;

assign sum = a+b;

endmodule

module add\_12\_bit (a,b,sum);

input[11:0] a,b;

output[11:0] sum;

assign sum = a+b;

endmodule

module vedic\_2\_x\_2(a,b,c);

input [1:0]a;

input [1:0]b;

output [3:0]c;

wire [3:0]c;

wire [3:0]temp;

assign c[0]=a[0]&b[0];

assign temp[0]=a[1]&b[0];

assign temp[1]=a[0]&b[1];

assign temp[2]=a[1]&b[1];

ha z1(temp[0],temp[1],c[1],temp[3]);

ha z2(temp[2],temp[3],c[2],c[3]);

endmodule

module vedic\_4\_x\_4(a,b,c);

input [3:0]a;

input [3:0]b;

output [7:0]c;

wire [3:0]q0;

wire [3:0]q1;

wire [3:0]q2;

wire [3:0]q3;

wire [7:0]c;

wire [3:0]temp1;

wire [5:0]temp2;

wire [5:0]temp3;

wire [5:0]temp4;

wire [3:0]q4;

wire [5:0]q5;

wire [5:0]q6;

vedic\_2\_x\_2 z1(a[1:0],b[1:0],q0[3:0]);

vedic\_2\_x\_2 z2(a[3:2],b[1:0],q1[3:0]);

vedic\_2\_x\_2 z3(a[1:0],b[3:2],q2[3:0]);

vedic\_2\_x\_2 z4(a[3:2],b[3:2],q3[3:0]);

assign temp1 ={2'b0,q0[3:2]};

add\_4\_bit z5(q1[3:0],temp1,q4);

assign temp2 ={2'b0,q2[3:0]};

assign temp3 ={q3[3:0],2'b0};

add\_6\_bit z6(temp2,temp3,q5);

assign temp4={2'b0,q4[3:0]};

add\_6\_bit z7(temp4,q5,q6);

assign c[1:0]=q0[1:0];

assign c[7:2]=q6[5:0];

endmodule

module vedic\_8X8(a,b,c);

input [7:0]a;

input [7:0]b;

output [15:0]c;

wire [15:0]q0;

wire [15:0]q1;

wire [15:0]q2;

wire [15:0]q3;

wire [15:0]c;

wire [7:0]temp1;

wire [11:0]temp2;

wire [11:0]temp3;

wire [11:0]temp4;

wire [7:0]q4;

wire [11:0]q5;

wire [11:0]q6;

vedic\_4\_x\_4 z1(a[3:0],b[3:0],q0[15:0]);

vedic\_4\_x\_4 z2(a[7:4],b[3:0],q1[15:0]);

vedic\_4\_x\_4 z3(a[3:0],b[7:4],q2[15:0]);

vedic\_4\_x\_4 z4(a[7:4],b[7:4],q3[15:0]);

assign temp1 ={4'b0,q0[7:4]};

add\_8\_bit z5(q1[7:0],temp1,q4);

assign temp2 ={4'b0,q2[7:0]};

assign temp3 ={q3[7:0],4'b0};

add\_12\_bit z6(temp2,temp3,q5);

assign temp4={4'b0,q4[7:0]};

add\_12\_bit z7(temp4,q5,q6);

assign c[3:0]=q0[3:0];

assign c[15:4]=q6[11:0];

endmodule