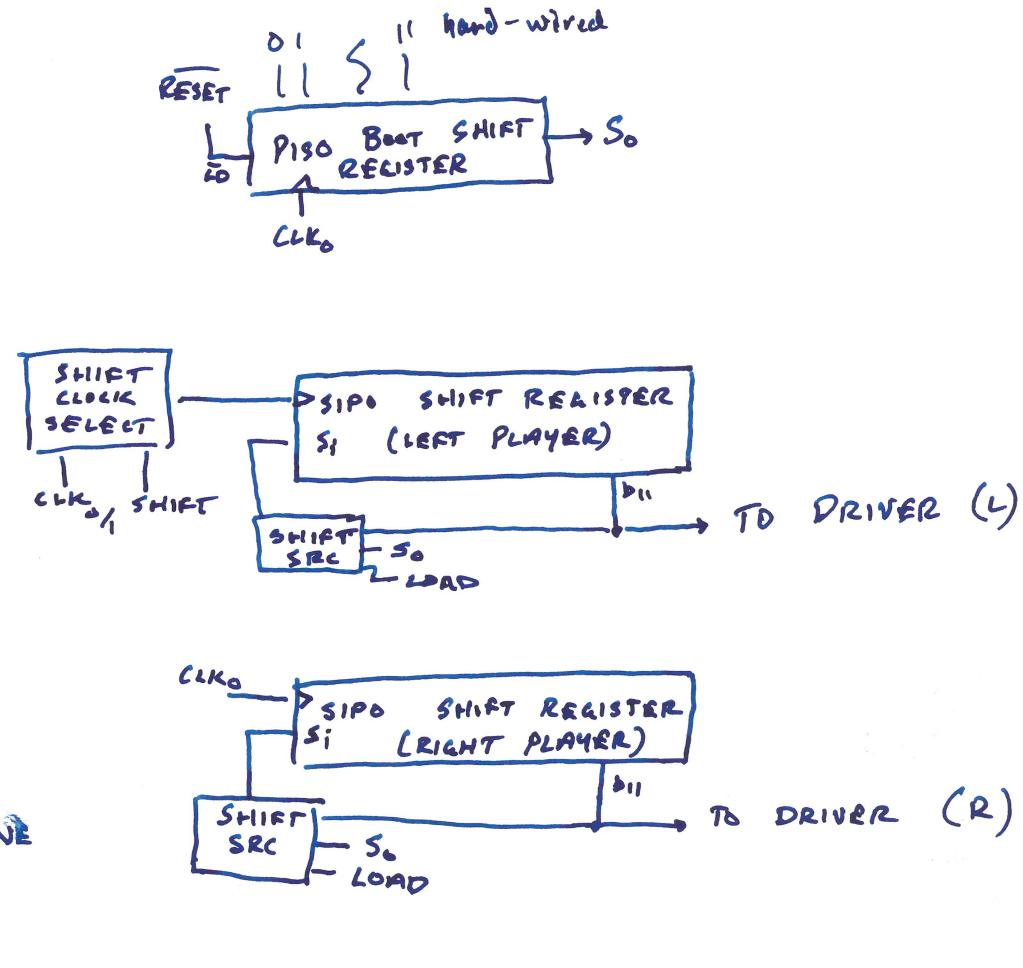
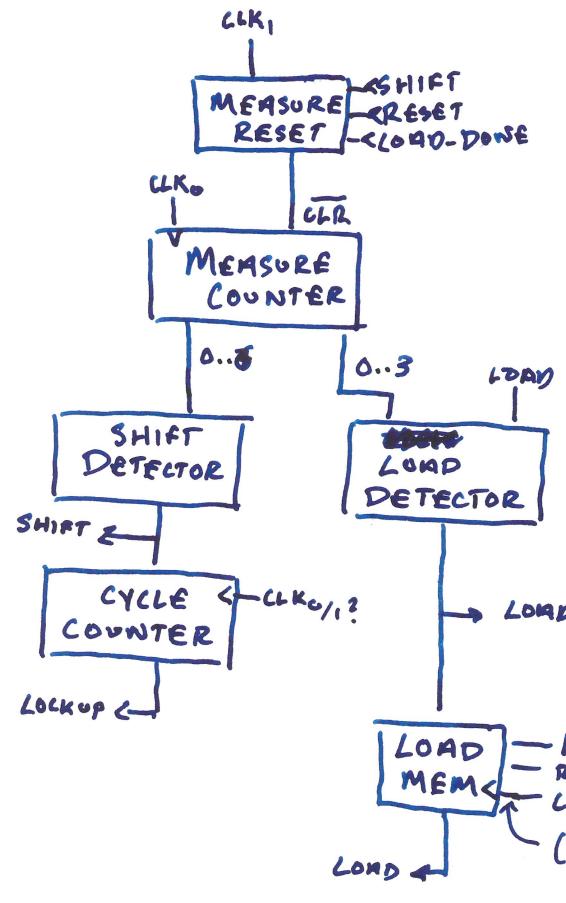


$CLK_0 \rightarrow$   
 $CLK_1 \rightarrow$   
 $RESET \rightarrow$   
 $LOAD\_DONE \rightarrow$   
 $LOAD \rightarrow$   
 $START \rightarrow$   
 $LOCKUP \rightarrow$   
 $S_0 \rightarrow$



# "CLAPPING Music" HARDWARE LAYOUT

- Simon

## OVERVIEW

THE CIRCUIT IS DIVIDED INTO FOUR STATES: RESET, LOAD, "NORMAL", AND LOCKUP. "NORMAL" IS NOT FORMALLY NOTATED AS A SIGNAL OR CONTROL, BUT IS INSTEAD THE ABSENCE OF THE OTHER THREE SIGNALS.

IN RESET, THE MEASURE AND CYCLE COUNTERS ARE BOTH CLEARED AND SET TO 0. THE PISO BOOT REGISTERS PARALLEL-LOAD THE HARD-WIRED "111011010110" STRING THAT REPRESENTS THE PIECE. THE PLAYER REGISTERS ARE CLEARED (SO THAT NOTHING IS PLAYED DURING LOAD). LOAD MEM IS TOGGLED IF  $\overline{\text{LOAD}}$  AT (RESET AND  $\text{CLK}_2 \uparrow$ ). DURING RESET, WHICH MUST BE HIGH FOR AT LEAST ONE  $\text{CLK}_1 \leftrightarrow \text{CLK}_2$  PERIOD,  $\text{CLK}_0$  IS DISABLED TO PREVENT THE IMPROBABLE EVENT THAT RESET +  $\text{CLK}_0$  PROPAGATION AND TIMING ISSUES CREATE AN INCONSISTENT CIRCUIT.

IN LOAD; THE CLOCK + MEASURE COUNTER logic USED FOR "NORMAL" OPERATION ARE BORROWED (IT IS A MINIMALIST PIECE, AFTER ALL) TO BOOTSTRAP THE LEFT/RIGHT PLAYER SHIFT REGISTERS BY SHIFTING IN THE OUTPUT OF THE PISO BOOT REGISTER. DURING LOAD, INPUT TO THESE PLAYER REGISTERS IS DRAWN FROM THE PISO REGISTER. WHEN THE MEASURE COUNTER READS 12, THE LOAD DETECTOR WRITES LOAD-DONE HIGH WHEN  $\text{CLK}_0$  PROPAGATES MEASURE COUNTER

THROUGH A FEW LAYERS OF LOGIC. LOAD-DONE Toggles LOAD TO  $\overline{\text{LOAD}}$ , AND CLEARS THE MEASURE COUNTER: BOTH OCCUR AT  $\text{CLK}_1$ , AND CLEAR LOAD-DONE AS A SIDE EFFECT.

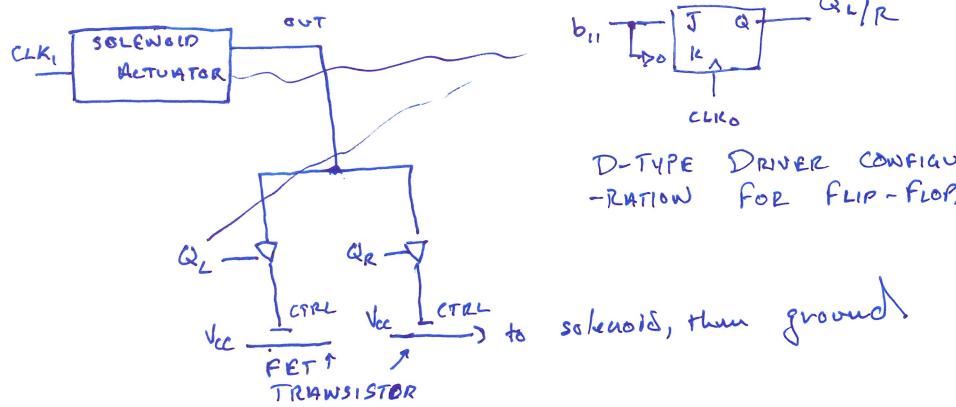
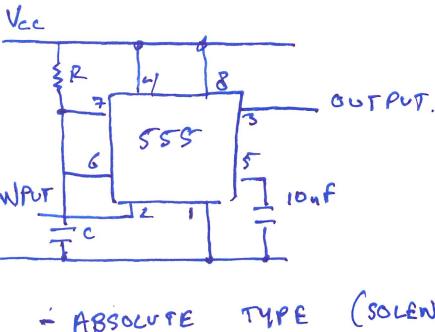
IN "NORMAL", WITH EACH CLOCK ~~SEE~~ PULSE; BOTH PLAYER'S REGISTERS ROTATE ONE BIT POSITION, w/b<sub>11</sub> FEEDING INTO b<sub>0</sub>. b<sub>11</sub> IS ALSO STAGED BY THE DRIVERS, PERPETUATING THE BEAT SIGNAL. THE MEASURE COUNTER IS INCREMENTED. IF MEASURE COUNTER WAS 96, THE SHIFT SIGNAL GOES HIGH, AND THE CYCLE COUNTER IS INCREMENTED.

AT  $\text{CLK}_1$ , IF SHIFT; THE MEASURE COUNTER IS RESET, AND THE LEFT PLAYER IS SHIFTED RIGHT w/out SIGNALLING THE DRIVERS.

LOCKUP IS SET HIGH WHEN THE CYCLE COUNTER REACHES 13, AND DISABLES THE CIRCUIT'S CLOCK: NOTHING WILL MOVE w/out THE  $\text{CLK}_0$  EDGES. RESET CLEARS OUT THE CYCLE COUNTER IMMEDIATELY, REENABLING THE CLOCK FOR THE RESET PHASE □



## MONOSTABLE PWM DETAIL.



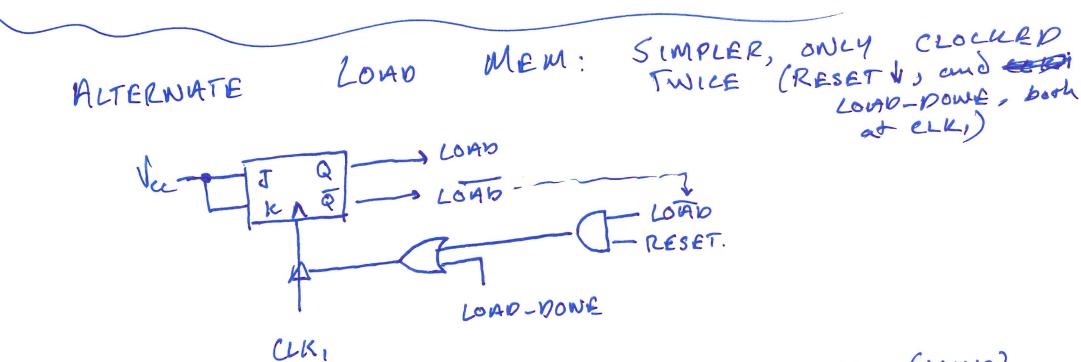
ONE CAN PREVENT THE S555 CHIP FROM FIRING WITH AN OR OF (Q<sub>L</sub>, Q<sub>R</sub>) FEEDING A CONTROL TRANSISTOR BLOCKING CLK<sub>1</sub>.

\* MIKE'S NOTE: ADD A SMALL DIODE IN PARALLEL WITH THE VOLTAGE SUPPLY TO THE SOLENOID. SOMETHING ABOUT ELECTRIC FIELDS COMING BACK INTO THE CIRCUIT.

## DETAILS, CONTINUED.

THE SOLENOID ACTUATOR IS A S555 ~~CHIP~~ SET TO FIRE IN MONOSTABLE MODE.

EXPERIMENTS WILL ALLOW ADJUSTMENT TO A SPECIFIC SOLENOID (POWER) SUPPLY, BUT A 20kΩ 1μF CAPACITOR WITH A 22ms. WILL FIRE.



Toggles ON RESET IFF IT IS LOAD  
INITIALLY, AT CLK<sub>1</sub>, SETTING LOAD TO HIGH.  
Toggles TO 0 AT LOAD-DONE AND CLK<sub>1</sub>.  
(LOAD-DONE IS CLEARED w/CLK<sub>1</sub> PROPAGATIONS)

### RESET / CLOCK POTENTIAL ISSUES:

IT MAY BE A GOOD IDEA TO TIE RESET TO AN OE LINE ENABLING (1) / DISABLING (0) THE CLK<sub>0</sub> SIGNAL: IF SOME PARTS OF THE CIRCUIT (THE BOOT REGISTERS ~~OR~~ OR THE MEASURE COUNTER) DROP THE CLK<sub>0</sub> PULSE WHILE RESET GOES HIGH, THE CIRCUIT WILL BE INCONSISTENT.

WE MIGHT ALSO WANT  $\uparrow$  TO DRIVE CLK<sub>0</sub>, w/ THE PWM 20ms CLOCK: IT'S CLOSE ENOUGH, AND WILL PREVENT ANY PERIODICITY.