Design and Simulation of the Internal Circuitry of the UA741 Analog Integrated Circuits

Sina Kazemi
Undergraduate student of Electrical – Electronic Engineering

Professor: Mehdi Ehsanian

K.N. Toosi University of Technology – EE Faculty

Introduction

Operational amplifiers (op-amps) are fundamental building blocks in analog electronics, widely used in signal processing, control systems, and instrumentation. Among these, the UA741 op-amp is one of the most iconic and extensively utilized due to its versatility, stability, and ease of use.

This project aims to design and simulate the internal circuit of the UA741 operational amplifier using PSPICE, focusing on five stages: the bias network, the input stage, the intermediate gain stage, the output stage, and the short-circuit protection circuit. Each stage plays a vital role in the overall functionality and performance of the op-amp, and their combined operation ensures the UA741 meets its design specifications.

- **Bias Network**: The bias circuit sets the operating point of the transistors within the op-amp, ensuring they function in the correct region of their characteristic curves. This stage is crucial for maintaining consistent performance across various operating conditions.
- **Input Stage**: This stage consists of a differential amplifier that amplifies the difference between the input signals while rejecting any common-mode signals. It significantly influences the input impedance and noise characteristics of the op-amp.
- **Intermediate Gain Stage**: Also known as the voltage gain stage, this amplifies the signal from the input stage to a higher level, providing the necessary voltage gain. This stage employs a common-emitter configuration to achieve high gain.
- **Output Stage:** The Output stage, implemented using a push-pull configuration, is designed to provide the necessary current to drive the load with low output impedance. The push-pull configuration employs a pair of transistors that

alternately conduct to deliver the output signal, improving efficiency and reducing distortion.

- **Short-Circuit Protection Circuit**: This stage protects the op-amp from damage due to excessive current flow, ensuring reliable operation under various conditions. It typically involves current limiting techniques to safeguard the internal components.

Parameter	NPN Transistor	PNP Transistor
β_F	200	50
β_R	2	4
V_{AF}	125V	50V
I_S	10fA	10fA
τ_F	0.35ns	30ns
r_b	200Ω	300Ω
r_c	200Ω	100Ω
r_e	2Ω	10Ω
C_{je}	1.0pF	0.3pF
V_{je}	0.7V	0.55V
M_{je}	0.33	0.5
C_{jc}	0.3pF	1.0pF
V_{jc}	0.55V	0.55V
M_{jc}	0.5	0.5
C_{js}	3.0pF	3.0pF
V_{js}	0.52V	0.52V
M_{js}	0.5	0.5

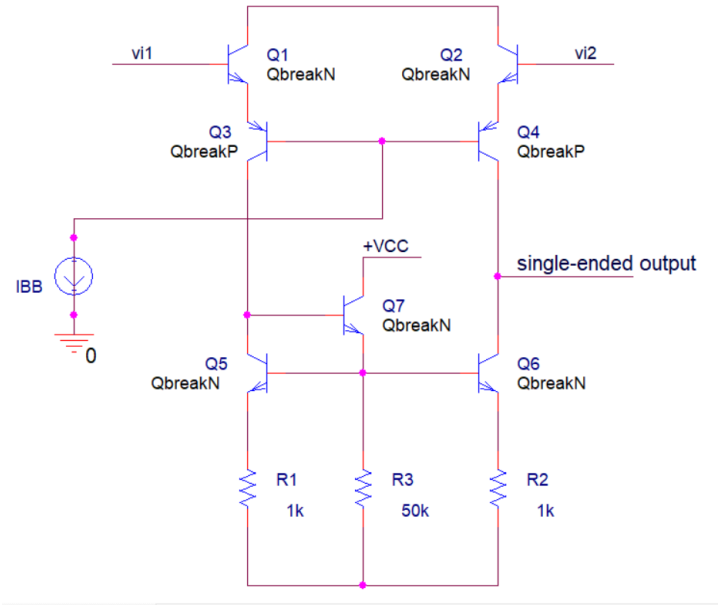
Typical Spice parameters for integrated *npn* and *pnp* transistors [Gray and Meyer, 1984].

Input Stage

The input stage of the UA741 operational amplifier employs a differential circuit, which is biased using the IBB bias current to enhance the Common-Mode Rejection Ratio (CMRR). The details of the IBB bias current will be explained in the bias circuit section. To increase the gain, an active load is used instead of resistors. Additionally, the offset current is significantly reduced, by a factor of approximately β, by incorporating the Q7 transistor. The R3 resistor is included to minimize the systematic offset, which will be further discussed in the second stage.

This differential configuration is crucial for achieving high input impedance and ensuring precise amplification of differential signals. The use of an active load, typically implemented with a current mirror, not only increases the gain but also improves the linearity and bandwidth of the input stage. By minimizing the offset current through Q7 and R3, the amplifier maintains higher accuracy and stability, essential for precision applications.

Furthermore, the choice of components and their configuration in the input stage significantly affects the overall performance of the op-amp. The careful design and optimization of this stage ensure that the UA741 can deliver High performance in terms of noise rejection, signal fidelity, and overall amplification, making it suitable for a wide range of analog signal processing tasks.



Q1 - Q2: Emitter Follower configuration

Q3 - Q4: Common-Base configuration

Q5 - Q6: Active loads

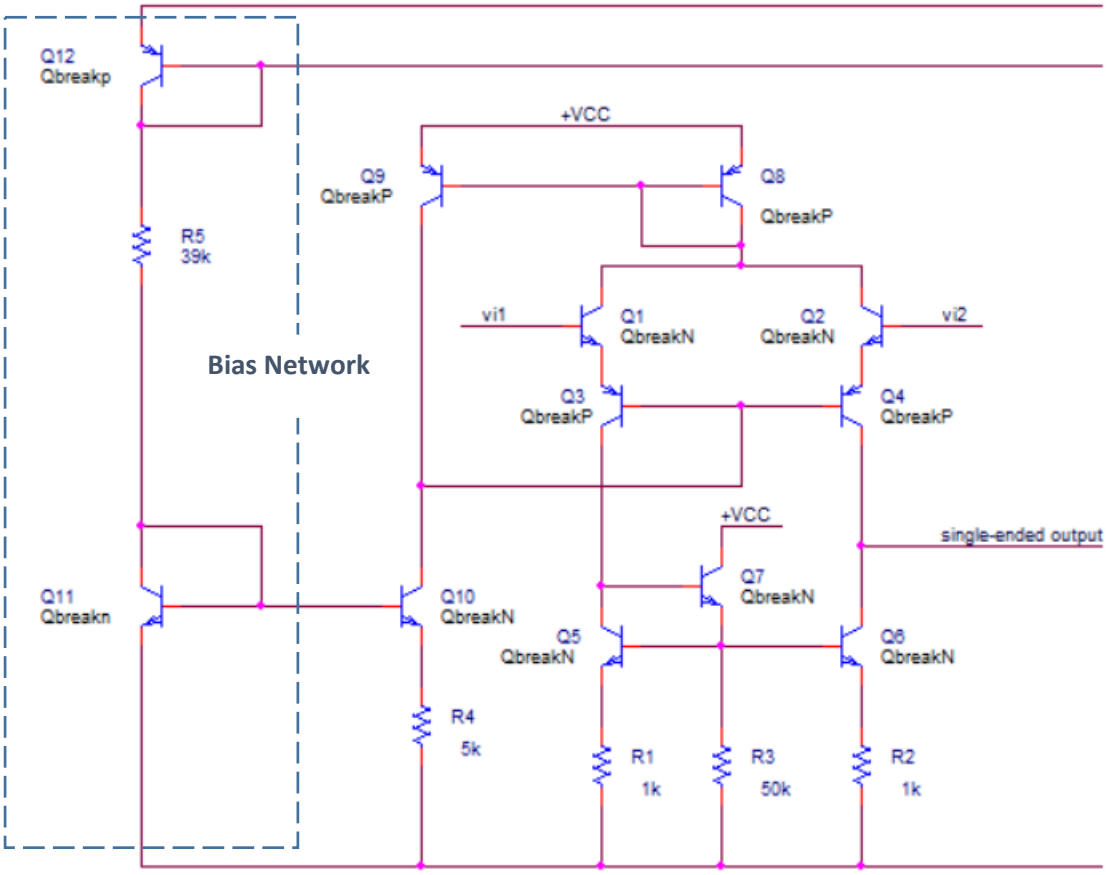
Input stage Differential Amplifier Circuit for noise reduction and pre-amplification gain

Pispice Simulation Files: https://github.com/sina96n/ua741-Design-and-Simulation

Bias Network

To bias the amplifying circuits at their operating points, a Widlar current source is employed using Q11 and R5. Q12 is connected in diode connected form, reducing the DC voltage level by approximately 0.7V, and replicating the current from the reference branch to other parts of the circuit. This configuration reduces the power consumption of the amplifier, as it eliminates the need for separate reference branches for different parts of the circuit.

Q8 and Q9 provide negative feedback specifically for the common-mode operation of the amplifier. This feedback reduces the common-mode gain, thereby enhancing the Common-Mode Rejection Ratio (CMRR).



Bias Network consisting of Q11 and R5 with Q12 in diode connected form to copy the current from reference branch

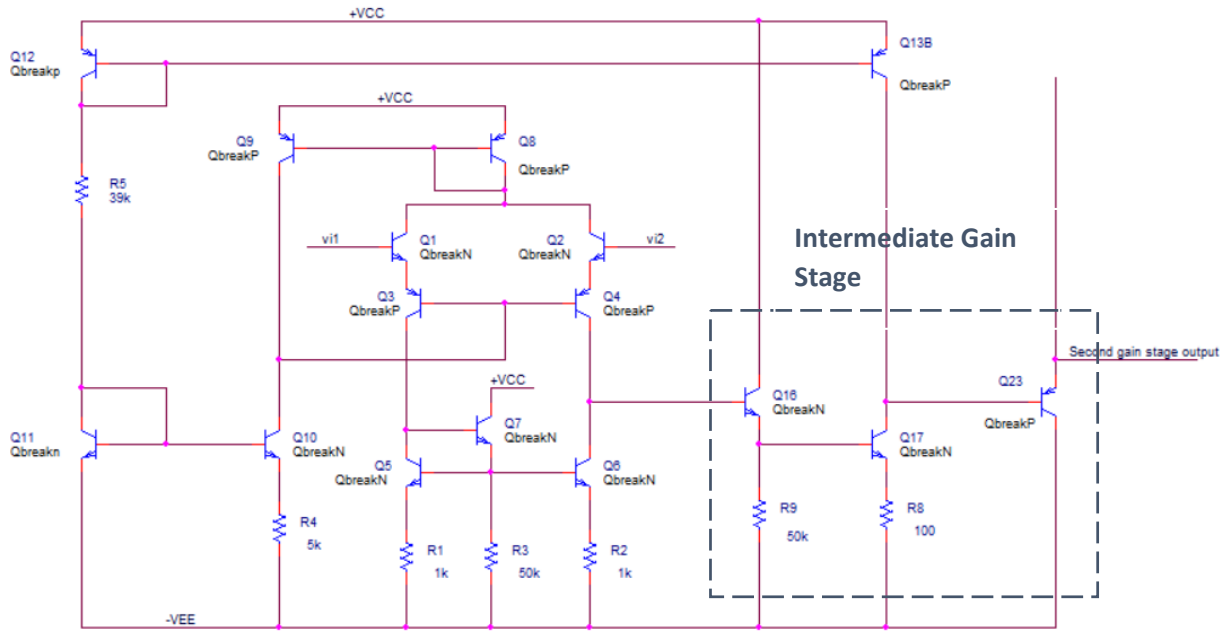
Intermediate Gain Stage

In the second gain stage, a common-emitter configuration using Q17 is employed to achieve higher gain before the output stage. This configuration is chosen for its ability to provide significant voltage gain, which is crucial for amplifying the signal to the desired level. Q16 acts as a buffer to increase the input resistance of the second gain stage, ensuring that the previous stage is not loaded and maintains its performance.

Notably, Q16 and R9 are identical to Q7 and R3, which helps to further reduce the offset at the input stage. This mirroring of components ensures consistent performance and stability throughout the amplifier stages. Additionally, a Q23 buffer is placed at the output of this stage to reduce the output resistance, ensuring better signal delivery to the output stage. This buffer stage is essential for driving the subsequent stages without signal degradation, maintaining the integrity of the amplified signal.

The design of the second gain stage also focuses on improving linearity and minimizing distortion. By carefully selecting the components and their configurations, the stage provides a clean and accurate amplification of the signal. The use of buffers and active loads enhances the overall performance, making the UA741 op-amp capable of handling a wide range of signal amplitudes with high fidelity.

This design ensures that the second gain stage not only amplifies the signal but also preserves its quality, contributing to the performance of the UA741 operational amplifier in various analog applications.



Input stage Differential Amplifier Circuit for noise reduction and pre-amplification gain

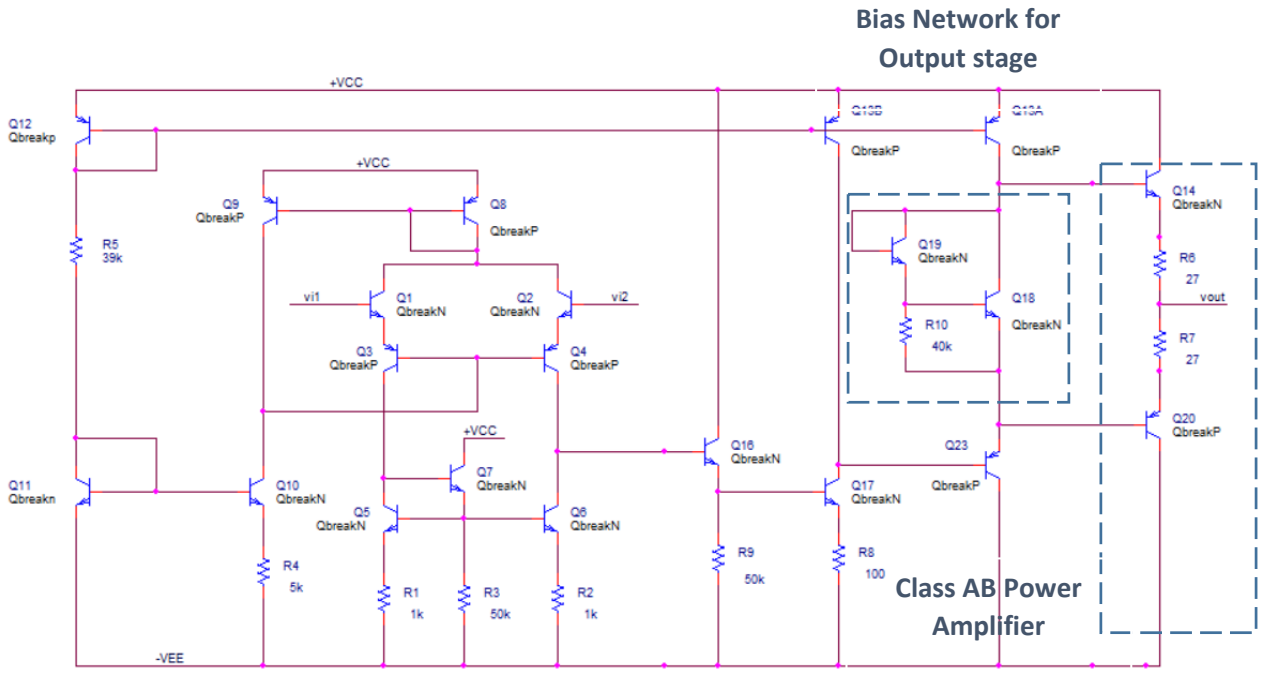
Output Stage / Power Drive

In the output stage, we utilize a Class AB push-pull amplifier configuration, incorporating a voltage multiplier circuit comprising Q18, Q19, and R10. This setup ensures that the output transistors, Q14 (NPN) and Q20 (PNP), are on the verge of turning on. As soon as a signal is applied to the amplifier, these transistors activate instantly, effectively driving the output load. This configuration combines the efficiency of Class B amplifiers with the low distortion of Class A amplifiers, providing a balance between power efficiency and signal fidelity.

For current control, the area of Q13A is designed to be 25% of that of the reference branch. Additionally, the areas of Q14 and Q20 are three times that of the reference branch, providing a high current ratio at the output to handle larger currents efficiently. This scaling ensures that the output stage can deliver the necessary current to drive the load without compromising performance.

The use of the Class AB push-pull configuration, along with precise transistor sizing, enhances the overall linearity and efficiency of the output stage, making it capable of delivering high-quality output signals with minimal distortion and optimal power

usage. This precise design approach ensures that the UA741 operational amplifier performs reliably in various applications, from signal processing to instrumentation.



Power Drive circuit including class AB power amplifier biased with voltage multiplier

Short Circuit Protection

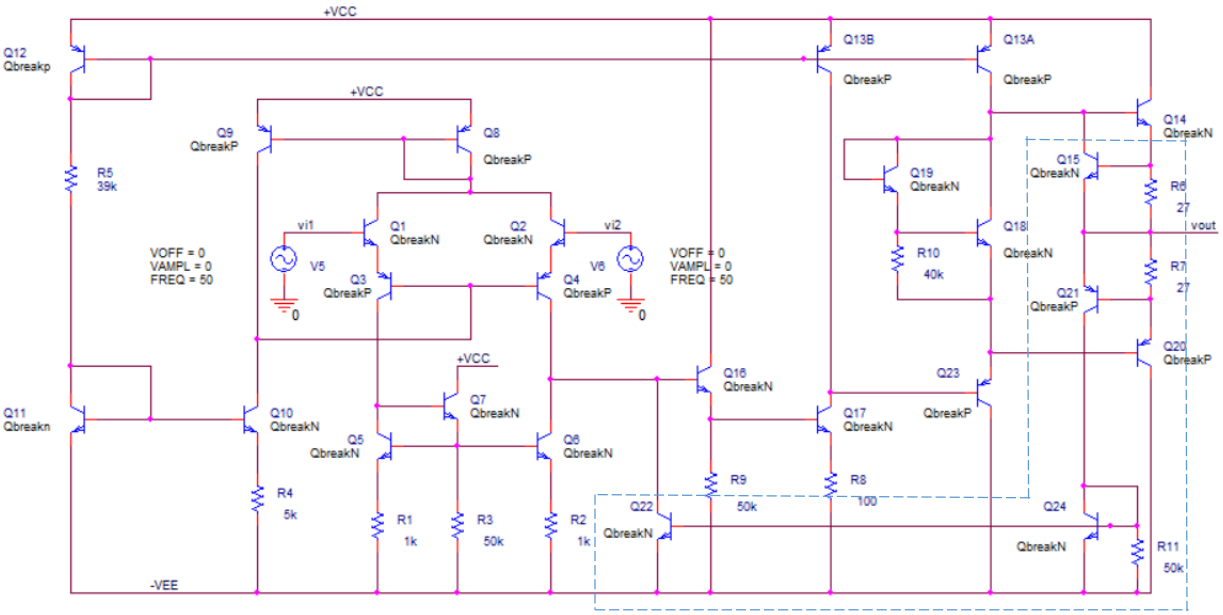
To ensure the UA741 operational amplifier is protected against short circuits, two distinct methods are employed for the ouput NPN and PNP transistors.

For the NPN transistor, the conventional method is utilized, involving Q15 and R6. This approach effectively limits the current through the NPN transistor, preventing damage under short-circuit conditions.

For the PNP transistor, a negative feedback network is applied. This network ensures that if the amplifier's output is shorted, the resulting rise in current is sensed, causing Q16 to turn off. This action quickly reduces the current flow, protecting the amplifier from potential damage. This method provides a reliable and efficient way to safeguard the PNP transistor, enhancing the overall robustness of the amplifier.

Implementing these protection mechanisms is crucial for the reliability and longevity of the UA741 operational amplifier. They ensure that the amplifier can withstand

adverse conditions without sustaining damage, making it more resilient in various applications. This comprehensive approach to short-circuit protection highlights the meticulous design considerations taken to enhance the durability and performance of the UA741 op-amp.



Short circuit protection including negative feedback network Short-Circuit Protection

Pispice Simulation Files: https://github.com/sina96n/ua741-Design-and-Simulation

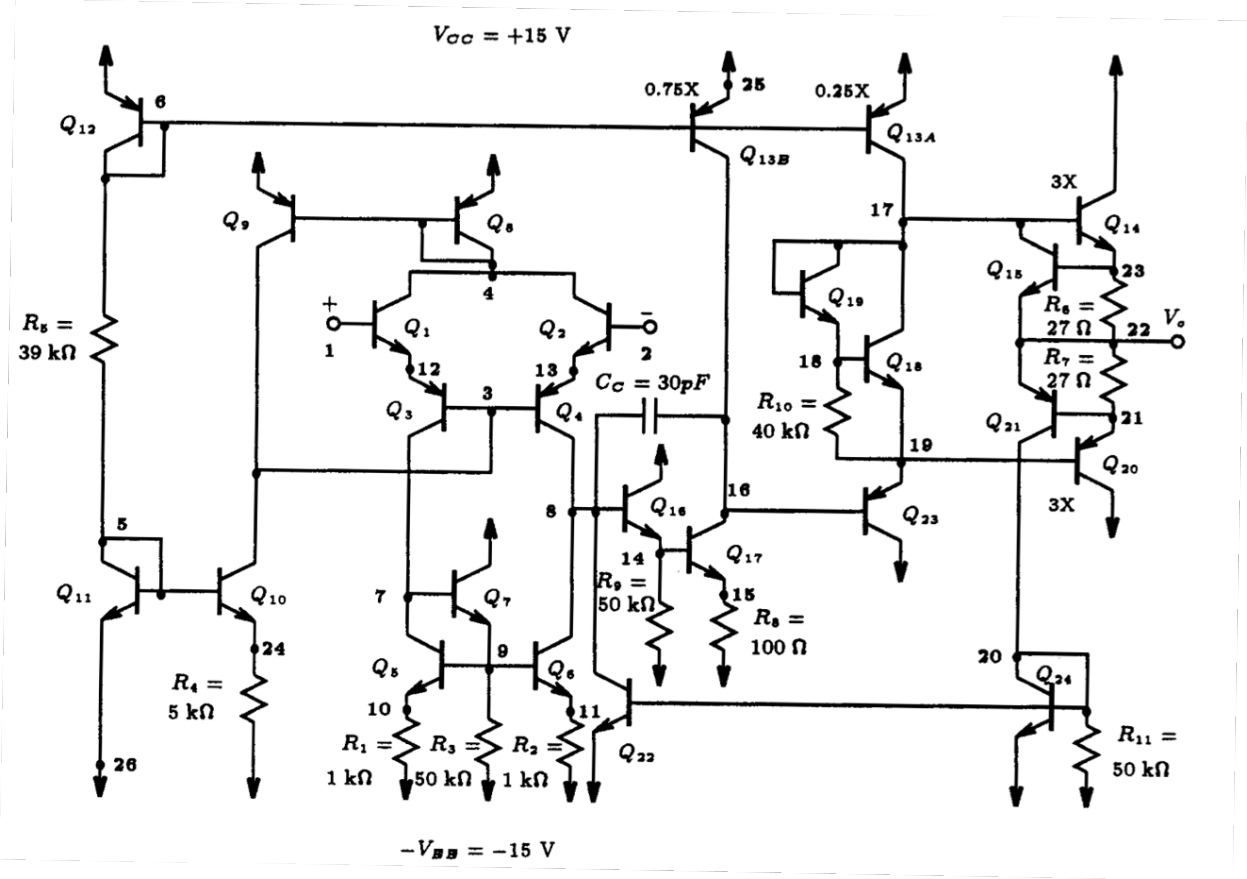
Bias Point Simulation

To begin the simulation process for the UA741 operational amplifier, we first need to establish the bias point of the circuit. This involves applying the power supply voltages and performing a bias point simulation to determine the operating conditions of the amplifier's transistors and other components.

According to the datasheet, we will apply a +15V VCC and a -15V VEE to the circuit, providing the necessary power to the operational amplifier. With these supply voltages in place, we will run a bias point simulation using PSPICE. This simulation will help us identify the quiescent operating points of the transistors, including their collector currents, base-emitter voltages, and other critical parameters.

The bias point simulation is a crucial step as it ensures that all transistors are operating in their intended regions, such as the active region for amplification. Accurate biasing is essential for the amplifier's performance, stability, and linearity.

$V_d = -314.1\ uv$ is applied to prevent any premature saturation.



```
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(    1)-157.1E-06  (    2) 157.1E-06  (    3)   -1.0496  (    4)   14.4540
(    5)  -14.3510  (    6)   14.3420  (    7)  -13.9310  (    8)  -13.7450
(    9)  -14.4640  (   10)  -14.9920  (   11)  -14.9920  (   12)    -.5265
(   13)    -.5263  (   14)  -14.2900  (   15)  -14.9340  (   16)   -1.1909
(   17)     .5834  (   18)     .0348  (   19)    -.5789  (   20)  -15.0000
(   21)    -.0040  (   22) 592.6E-06  (   23)     .0052  (   24)  -14.9020
(   25)   15.0000  (   26)  -15.0000  (  100)    0.0000  (  101)-314.1E-06

    VOLTAGE SOURCE CURRENTS
    NAME          CURRENT

    Vcc          -1.841E-03
    Vee           1.841E-03

    TOTAL POWER DISSIPATION   5.52E-02  WATTS
```

Rather than listing all of the bias point information here, instead, in the Table below, we list the collector current (in uA) of each transistor found in the 741 op amp circuit. These are also compared with the current levels computed using hand analysis by Sedra and Smith. As is self-evident, there is reasonable agreement between the two sets of results.

Transistor	Hand	Spice	Transistor	Hand	Spice
Q_1	9.5	7.68	Q_{13B}	550	658
Q_2	9.5	7.71	Q_{14}	154	170
Q_3	9.5	7.59	Q_{15}	0	~0
Q_4	9.5	7.63	Q_{16}	16.2	17.1
Q_5	9.5	7.55	Q_{17}	550	644
Q_6	9.5	7.56	Q_{18}	165	198
Q_7	10.5	10.8	Q_{19}	15.8	16.2
Q_8	19	14.8	Q_{20}	154	168
Q_9	19	19.4	Q_{21}	0	~0
Q_{10}	19	19.6	Q_{22}	0	~0
Q_{11}	730	732	Q_{23}	180	213
Q_{12}	730	708	Q_{23}	0	~0
Q_{13A}	180	215			

DC collector currents of the 741 circuit in uA as computed by hand analysis and by Spice.

Bode Analysis of the UA741 Operational Amplifier

To analyze the frequency response of the uncompensated UA741 operational amplifier, we performed a Bode plot simulation to observe the gain and phase characteristics over a wide frequency range. The objective is to understand the raw performance of the amplifier without any compensation mechanisms in place.

The UA741 op-amp is known to be internally compensated using Miller compensation to ensure stability under worst-case scenarios, such as when the feedback factor BBB is equal to 1 (unity feedback). However, for this initial simulation, we are examining the amplifier without this internal compensation to identify potential issues and the inherent behavior of the circuit.

During the Bode plot analysis, we encountered a significant challenge. The first internal parasitic capacitor, which was previously defined in the circuit, becomes shorted at approximately 160 GHz. This high frequency is beyond the limits of the real implementation of the BJT op-amps and they won’t happen in rea-life scenarios.

Despite this limitation, it is important to note the following details:

- At lower frequencies, the amplifier exhibits the expected gain characteristics, with a steady gain in the midband region.
- As the frequency increases, we approach the point where the first parasitic capacitor begins to have a significant effect.
- Around 160 GHz, this parasitic capacitor effectively shorts, leading to a rapid decrease in the midband gain. This phenomenon marks the transition from the midband to the upper frequency range where the gain starts to decrease.

This high-frequency behavior indicates that the uncompensated amplifier is susceptible to instability and performance degradation at very high frequencies due to the parasitic effects. Low phase margin beyond this point highlights the need for compensation to ensure stable operation across the intended frequency range.

understanding these upper band details is crucial for designing effective compensation strategies. In the next steps, we will incorporate Miller compensation to stabilize the amplifier and perform further simulations to analyze its compensated performance. This will allow us to achieve a comprehensive understanding of the UA741 op-amp's behavior across a practical frequency range.

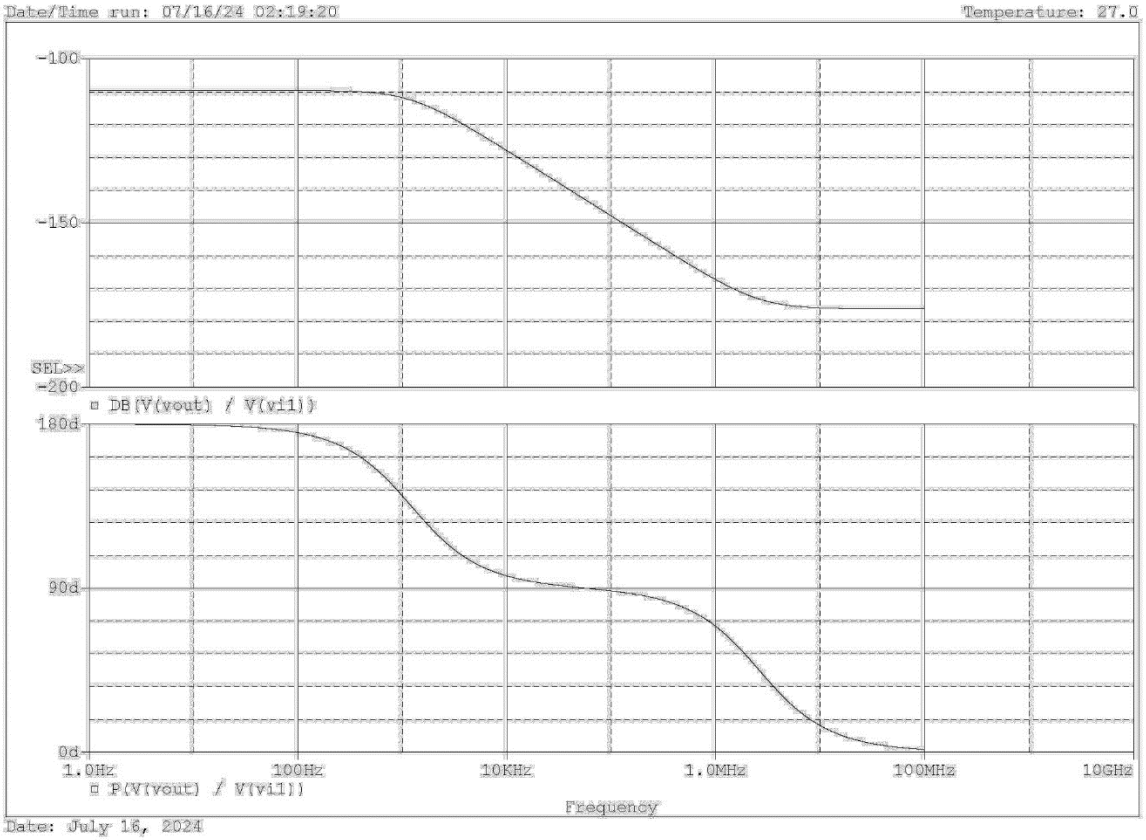
Why We Compensate

Compensation in operational amplifiers is essential to ensure stable operation across a wide range of frequencies and feedback conditions. The primary goals of compensation are to improve the phase margin and gain margin of the amplifier.

- **Phase Margin**: This is the amount of additional phase lag required to bring the total phase shift around the loop to 180 degrees, at which point the system would oscillate. A higher phase margin indicates greater stability and less risk of oscillation. Typically, a phase margin of at least 45-60 degrees is desired for stable operation.
- **Gain Margin**: This is the amount by which the open-loop gain can increase before the system becomes unstable. It provides a measure of how much gain variability the system can tolerate before oscillations occur. A gain margin of at least 6 dB is generally considered acceptable.

To achieve these stability margins, we added a 30 pF compensation capacitor between node 16 and node 8. This placement ensures high impedance at both ends and introduces a negative gain, satisfying the Miller effect conditions. The Miller capacitor rolls off the gain at higher frequencies, effectively shifting the dominant pole to a lower frequency, which increases the phase margin and stabilizes the amplifier.

By implementing this compensation strategy, we ensure that the UA741 operational amplifier operates reliably and maintains its performance across the intended frequency range, preventing undesirable oscillations and ensuring consistent gain and phase characteristics.



Bode Analysis of the UA741 with 30 pF Miller compensation capacitor

Effects of Feedback on the UA741 Operational Amplifier

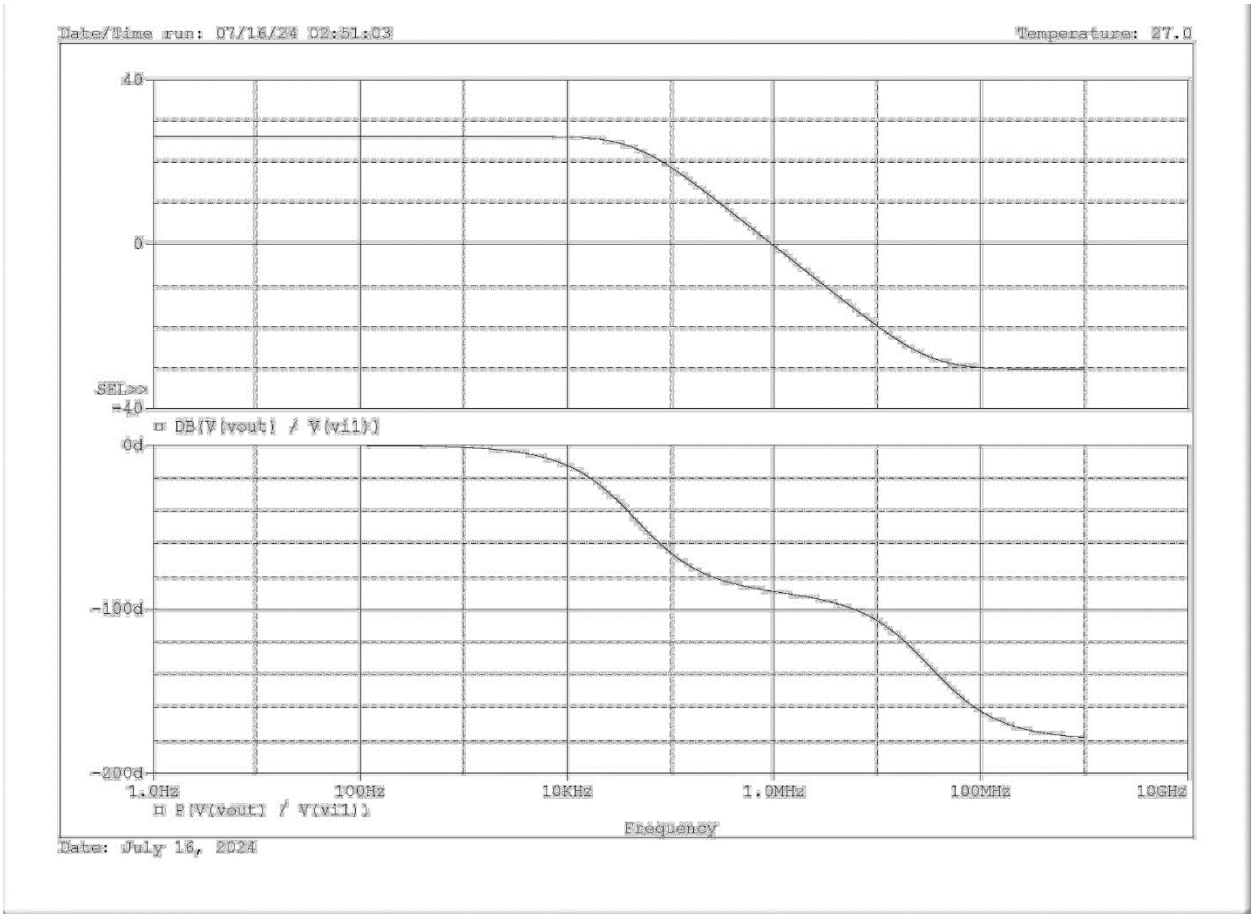
Feedback is a critical technique used in operational amplifier circuits to control various performance parameters. By applying feedback, we can significantly enhance the characteristics of the amplifier. Here are the key effects of feedback on the UA741 operational amplifier:

1. **Increased Bandwidth**:
    - Feedback extends the bandwidth of the amplifier by reducing the gain at higher frequencies. This results in a wider range of frequencies over which the amplifier can operate effectively. Essentially, the gain-bandwidth product remains constant, so as the feedback reduces the gain, the bandwidth increases correspondingly.
2. **Decreased Gain**:

- Applying negative feedback reduces the overall gain of the amplifier. While this might seem like a disadvantage, it actually improves the linearity and reduces distortion. The reduced gain also makes the amplifier more predictable and less sensitive to variations in component values.

3. **Improved Input Resistance**:
   - Negative feedback increases the input resistance of the amplifier. This is beneficial in applications where the amplifier needs to interface with high-impedance sources, as it reduces the loading effect on the signal source and allows for more accurate signal amplification.
4. **Improved Output Resistance**:
   - Feedback decreases the output resistance of the amplifier, making it more capable of driving low-impedance loads. This enhances the ability of the amplifier to deliver power to the load with less signal degradation and better voltage regulation.

Applied Feedback: RF = 100 KΩ, R = 5 KΩ

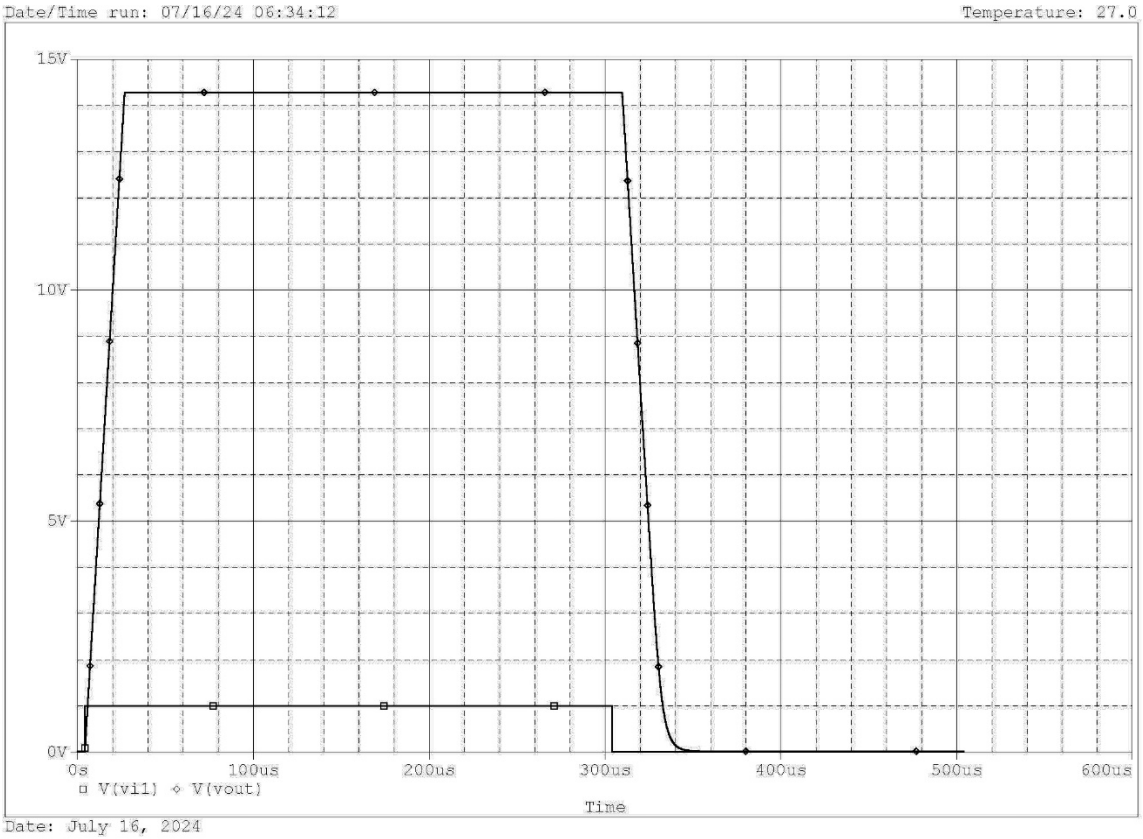


By incorporating these feedback mechanisms into the design of the UA741 operational amplifier, we achieve a more stable, reliable, and versatile amplifier. The improvement in bandwidth, input and output resistances, and linearity ensures that the amplifier performs well across a variety of applications, maintaining high fidelity and consistent performance.

Step Response Analysis

The step response of an operational amplifier is a crucial aspect of its dynamic performance. By analyzing the step response, we can understand how the amplifier reacts to a sudden change in input, which provides insights into its speed, stability, and transient behavior.

To determine the step response, a step input signal is applied to the amplifier, and the resulting output is observed and plotted over time. Key characteristics such as rise time, fall time, overshoot, and delay are analyzed to evaluate the amplifier's performance.



In our simulation, we observed the following:

1. **No Overshoot**: The absence of overshoot in the step response indicates that the amplifier is stable and does not exhibit excessive oscillations when responding to a sudden change in input. This is a desirable trait, as it suggests that the amplifier can settle quickly to its final value without exhibiting instability.
2. **Rise Time**: The rise time, which is the time taken for the output to transition from a low to a high value, was observed to be small. This indicates that the amplifier is capable of responding quickly to an increasing input signal, making it suitable for high-speed applications where fast signal processing is required.
3. **Fall Time**: The fall time, which is the time taken for the output to transition from a high to a low value, was found to be greater than the rise time. This suggests that the amplifier takes longer to respond to a decreasing input signal compared to an increasing one. This asymmetry could be due to differences in the internal circuitry's response to positive and negative transitions.
4. **Turn-off Delay**: The turn-off delay indicates a slight lag in the circuit's response after the input signal is removed. This delay can affect the amplifier's performance in applications requiring precise timing and fast turn-off characteristics.

The step response analysis is important because it provides a comprehensive view of the amplifier's transient behavior, allowing us to:

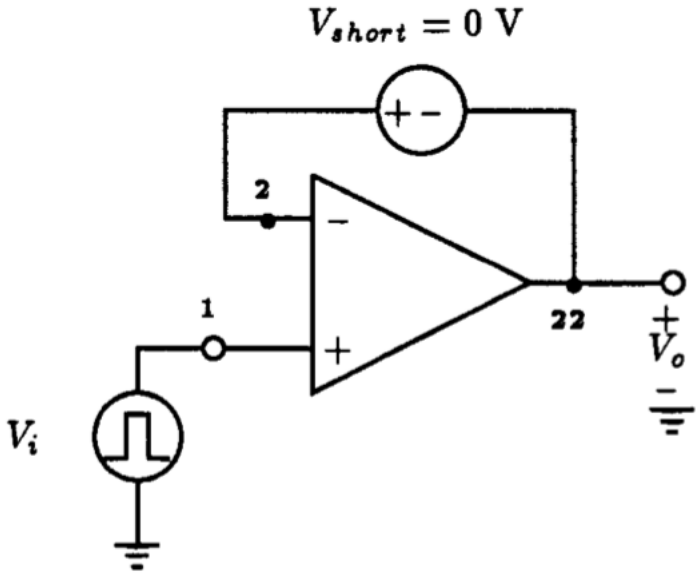
- **Assess Stability**: Ensuring that the amplifier does not overshoot or oscillate, which could lead to signal distortion or instability in the application.
- **Evaluate Speed**: Determining how quickly the amplifier can respond to changes in the input signal, which is critical for high-frequency and fast-switching applications.
- **Identify Delays**: Recognizing any inherent delays in the amplifier's response, which could impact its performance in timing-sensitive applications.

Slew-Rate Limiting of the 741

An important attribute of op amp behavior that usually limits the high-frequency operation of op amp circuits is its slew-rate limiting. Connecting the op amp in a unity-

gain configuration and applying a large voltage pulse to its input will reveal both the positive-going and negative-going slew-rate of this op amp.

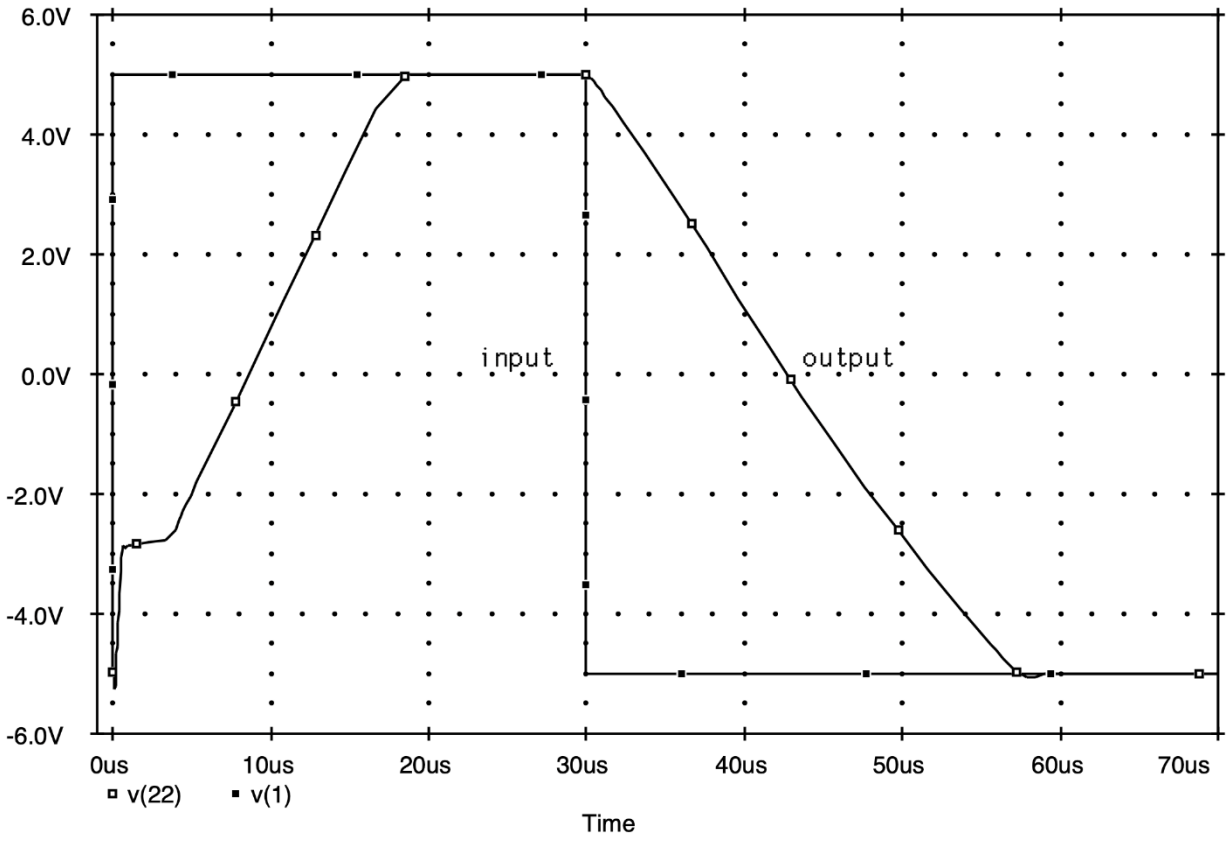
beginning at a low level of -5 V and quickly rising to +5 V one ns after this, staying there for 30 us and then returning to the -5 V level one ns later. It remains at this low level of -5 V for the rest of the duration of the pulse. A transient analysis is requested to compute the response of the op amp circuit arrangement over a 100 us interval using a 0.1 ns sampling interval.



Circuit arrangement for computing op amp positive- and negative-going slew-rate limits.

Both the input pulse to the amplifier and its output response are shown. Here we see that the positive-going portion of the output signal has a very different shape than the negative-going portion. Instead of a gradual rise in the positive-going signal, initially there is small jump in the output voltage of 2.2 volts, followed by the output being held constant at -2.8 V for 3.6 us, then rising linearly to +5 V in 18.2 us. Thus, the positive-going slew-rate is estimated at +0.55 V/us.

The negative-going response behaves more along the lines of what one expects, a steady decline from +5 V to -5 V. As a result, the negative-going slew-rate is found to be -0.39 V/us.



Input and output transient voltage waveforms of the 741 op amp circuit connected in a unity-gain configuration. Both the positive-going and negative-going slew-rate limits of the op amp is evident from these results.

Determining Input and Output Resistances

To accurately determine the input and output resistances of the UA741 operational amplifier, we need to measure the voltage-to-current ratios at the respective nodes. This is done by applying a small sine wave signal and measuring the resulting peak-to-peak (p-to-p) voltage and current at both the input and output nodes.

Procedure for Measuring Input Resistance:

1. **Applying a Sine Wave Signal**: Input a small amplitude sine wave signal at the input node of the amplifier. The signal should be small enough to ensure linear operation but sufficient to generate measurable voltages and currents.
2. **Measuring Peak-to-Peak Voltage and Current**:
    - Measuring the peak-to-peak voltage at the input node.

   - Measuring the peak-to-peak current entering the input node.
3. **Calculating Input Resistance**:
   - Using the formula $R_{in} = \frac{V_{in\ (p-p)}}{I_{in\ (p-p)}}$ to calculate the input resistance.

   This ratio gives us the resistance seen by the input signal, indicating how much the amplifier loads the source driving it.

Procedure for Measuring Output Resistance:

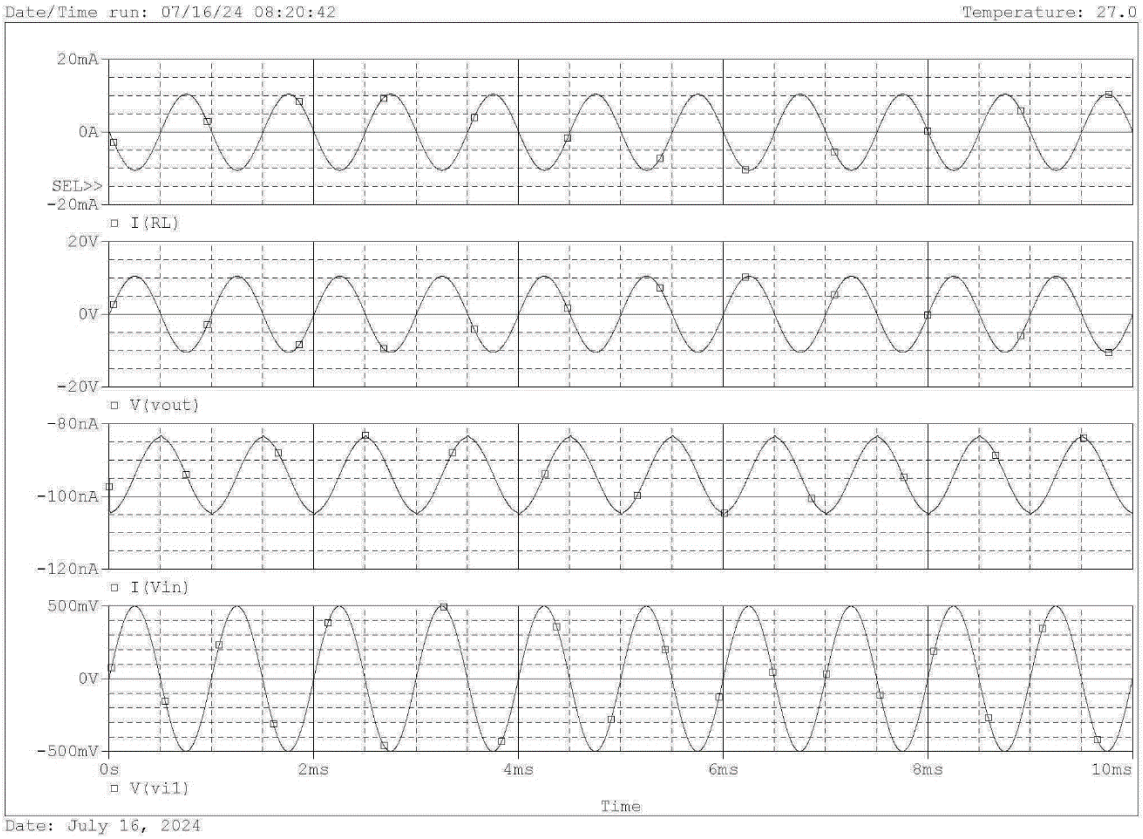
1. **Applying a Sine Wave Signal**: Similarly, we apply a small amplitude sine wave signal at the input to drive the amplifier into operation.
2. **Measuring Peak-to-Peak Voltage and Current**:
   - Measure the peak-to-peak voltage at the output node.
   - Measure the peak-to-peak current at the output node.
3. **Calculate Output Resistance**:
   - Using the formula $R_{out} = \frac{V_{out\ (p-p)}}{I_{out\ (p-p)}}$ to calculate the output resistance.

   This ratio provides the resistance seen by the load connected to the amplifier's output, indicating the amplifier's ability to drive various load impedances.

Importance of Input and Output Resistances

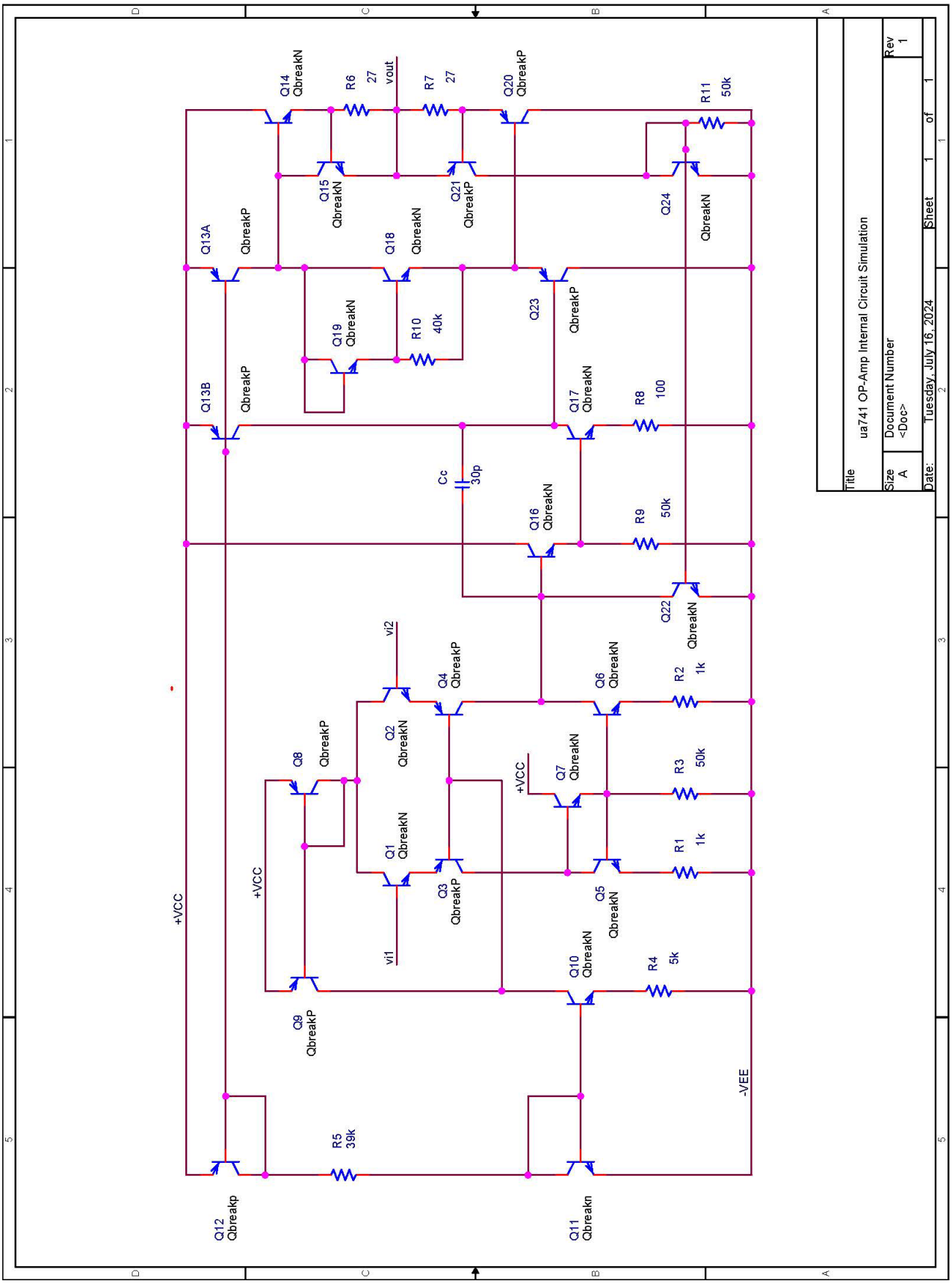
Understanding the input and output resistances of an operational amplifier is crucial for several reasons:

- **Input Resistance:** A high input resistance is desirable because it ensures that the amplifier does not load the signal source significantly, allowing for accurate signal amplification. It is especially important in applications involving high-impedance sources.
- **Output Resistance: A** low output resistance is beneficial as it allows the amplifier to drive low-impedance loads effectively without significant signal loss. It ensures better voltage regulation and power transfer to the load.



Voltage and Current measurements at input and output nodes.

Based on the measurements the input resistance is $R_{in} = 2.35\ M\Omega$ and the output resistance is $R_{out} = 106\ \Omega$ which can be changed using different feedback networks.



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