Digital Computer Design Laboratory

#6 REGISTER FILE

A register file shown in Figure-2 is a 16-register × 32-bit three-ported register file built from a three-ported memory. The register file has two read ports (A1/RD1 and A2/RD2) and one write port (A3/WD3). The 4-bit addresses, A1, A2, and A3, can each access all 2^4 = 16 registers. Two registers can be read and one register written **simultaneously**.

Create *register.sv* with behavioral design and test your design with *register_testbench.sv* .

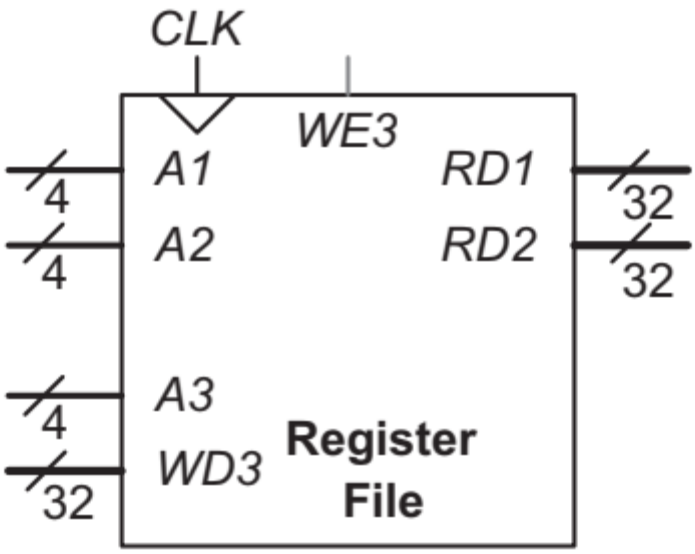

Figure-2

OPTIONAL (+30 points): Squish your design into 4-register × 4-bit three-ported register file, adapt your constraint file and test your design with hardware.