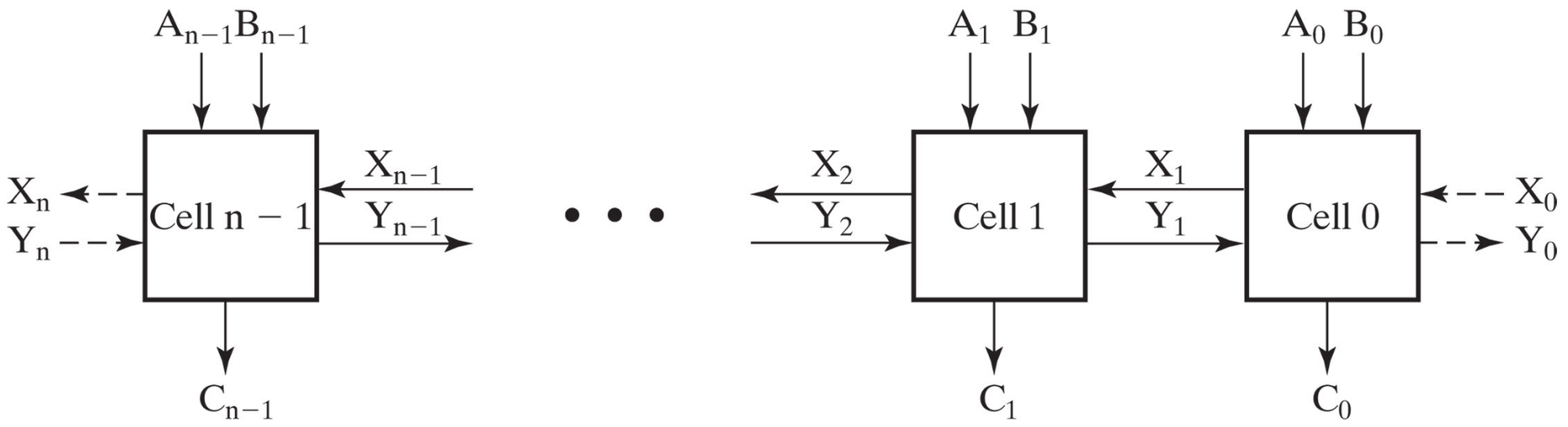
Arithmetic Circuits

Logic Design

Iterative Combinational Circuits

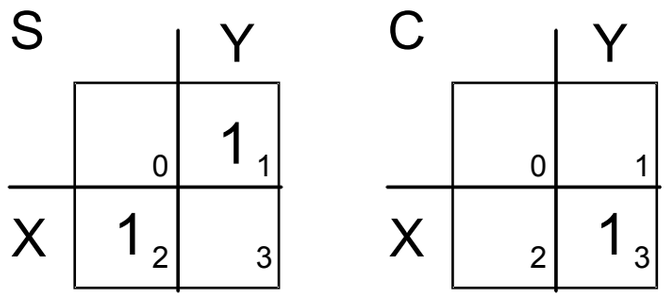
- The function implemented often requires that **the same sub-function** be applied to **each bit** position.
- Thus, a functional block can be designed for the sub-function
  - used repetitively for each bit position of the overall arithmetic block being designed.



Half Adder

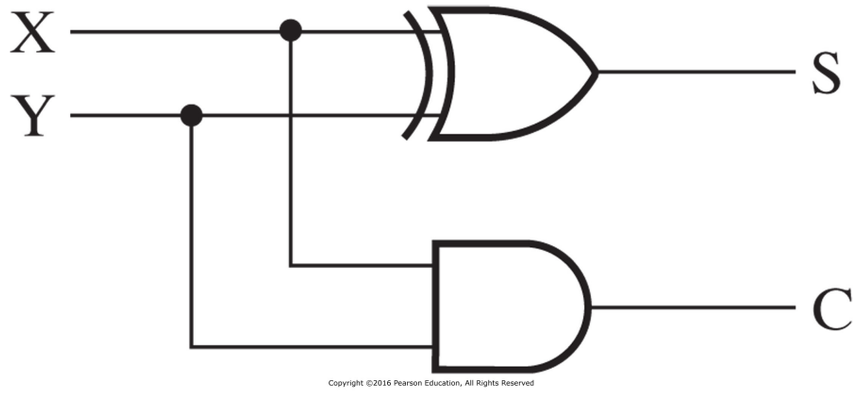
TABLE 3-11
Truth Table of Half Adder

Inputs		Outputs	
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



$S = A\bar{B} + \bar{A}B = A \oplus B$

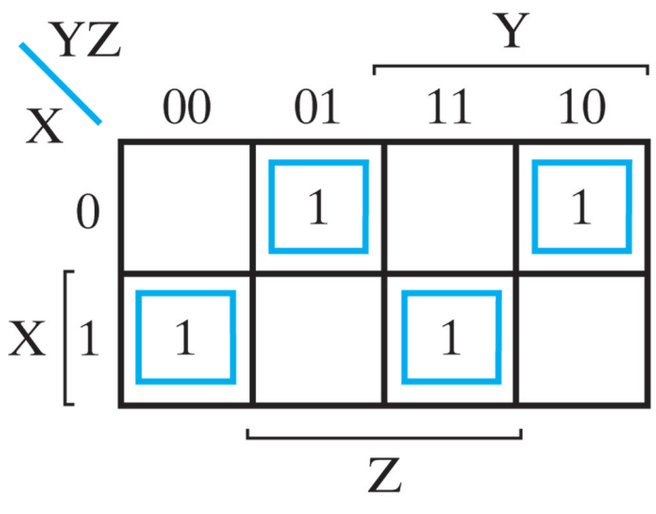
$C = AB$



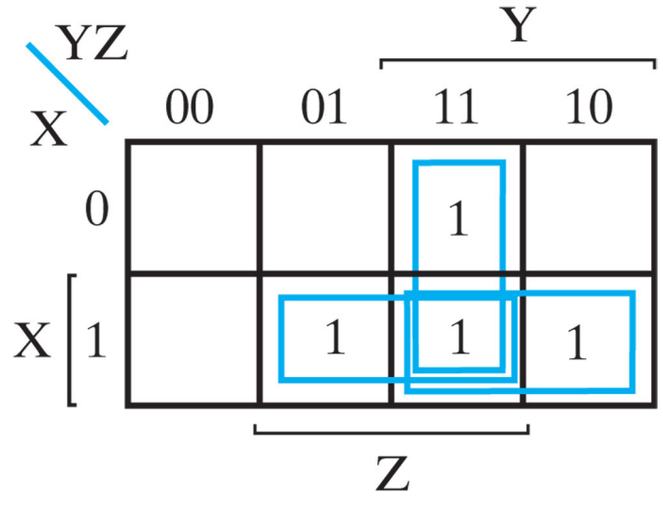
Full Adder

TABLE 3-12
Truth Table of Full Adder

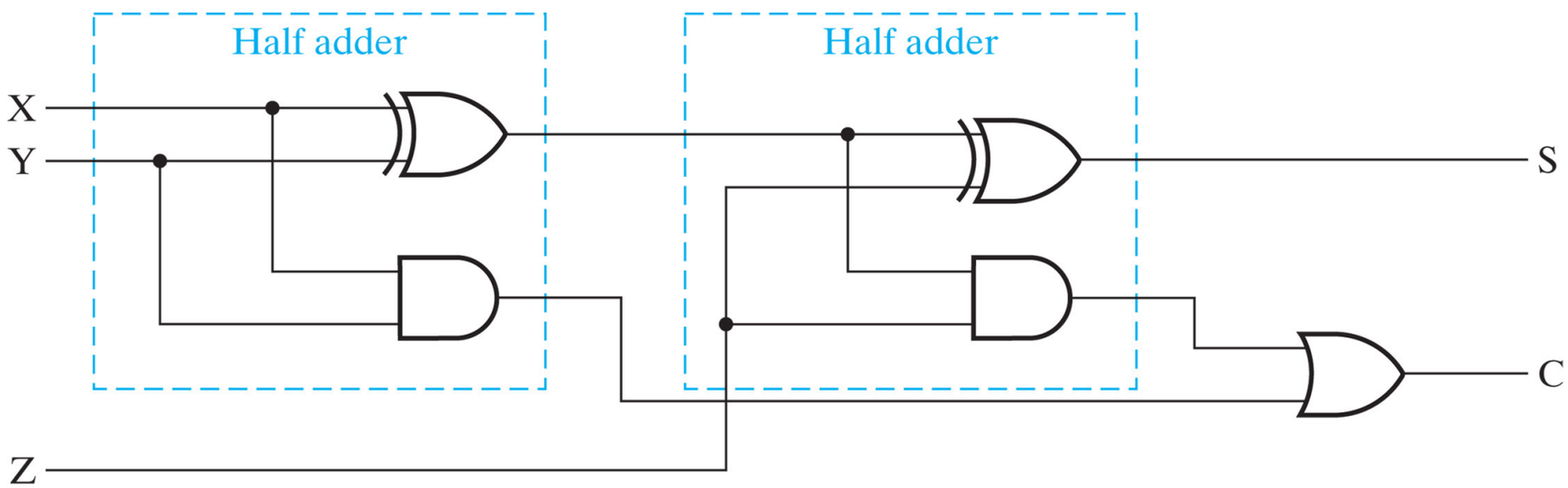
Inputs			Outputs	
X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



$$S = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$$
$$= X \oplus Y \oplus Z$$

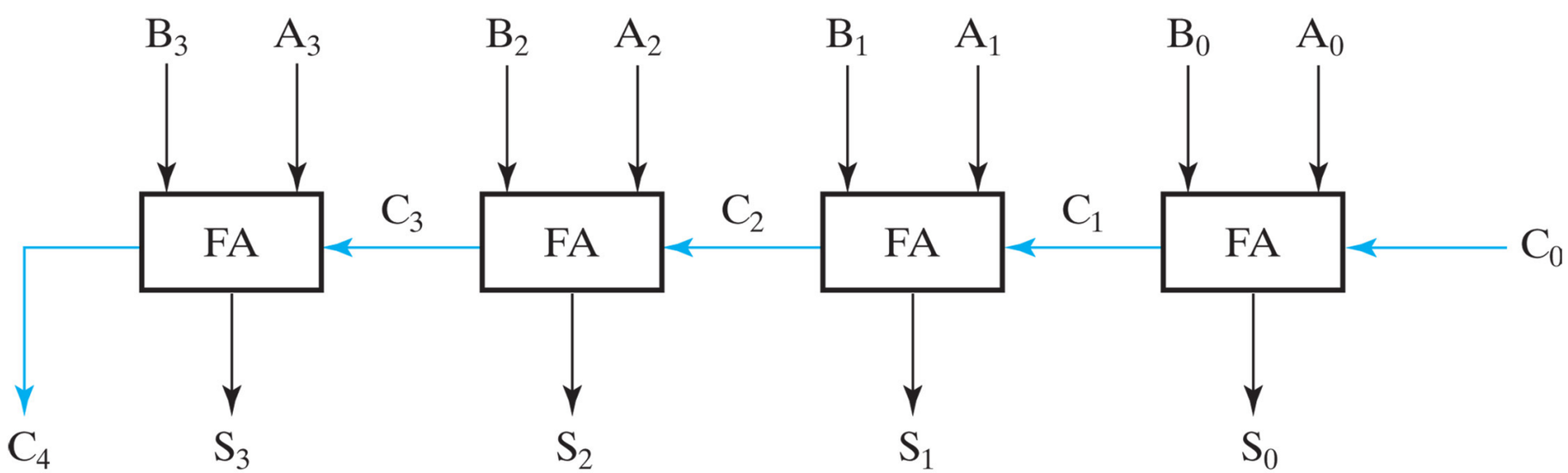


$$C = XY + XZ + YZ$$
$$= XY + Z(X\bar{Y} + \bar{X}Y)$$
$$= XY + Z(X \oplus Y)$$



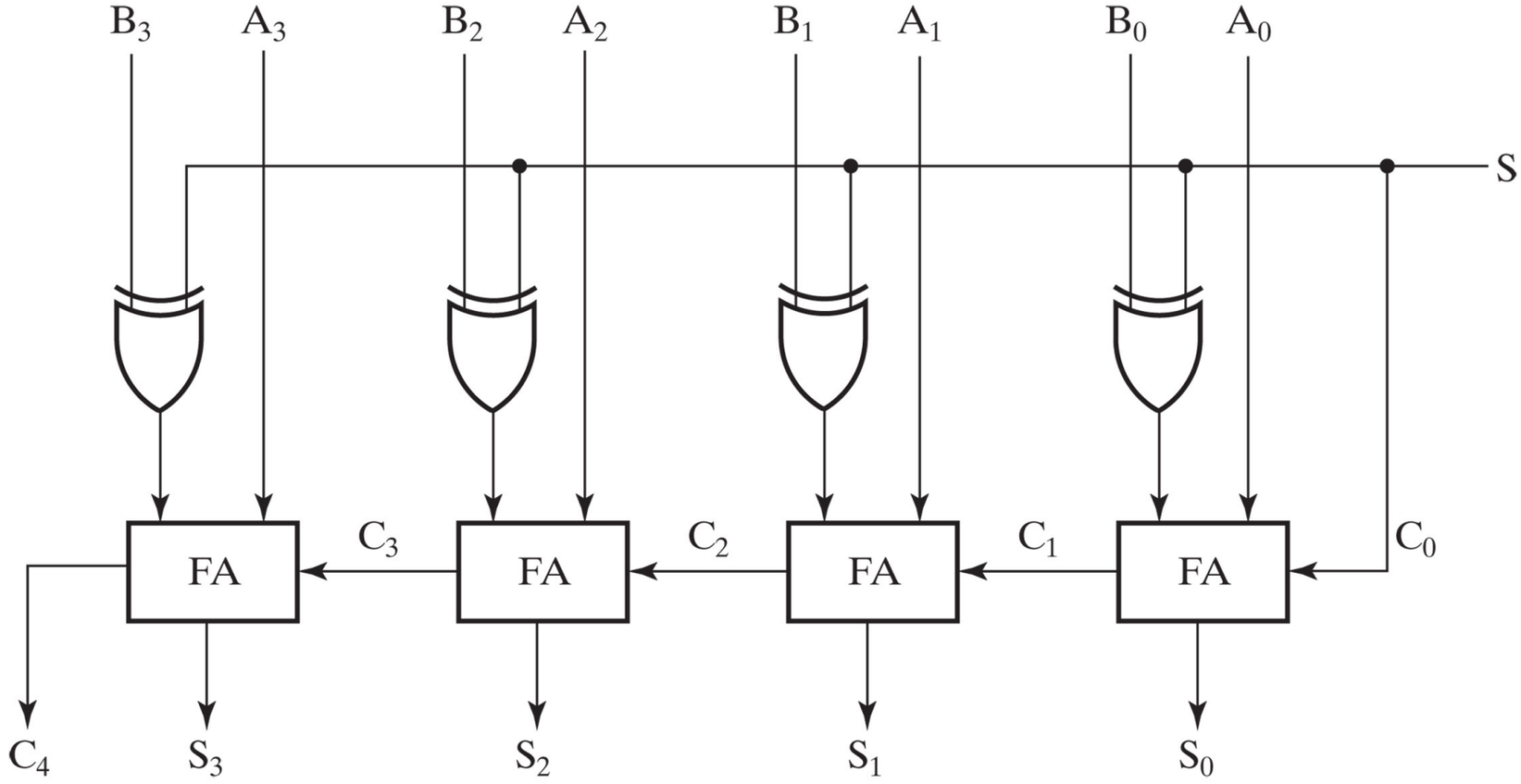
4-bit Ripple Carry Adder

- The full adders are connected **in cascade**, with the carry output from one full adder connected to the carry input of the next full adder.



Adder/Subtractor Circuit

- Using the 2s complement, we have eliminated the subtraction operation and need only the complementer and an adder.
- A – B = A + (-B)
  - Take **2's complement** of B
  - Perform addition of A and 2's complement of B



Addition when S = 0
Subtraction when S = 1