Digital Computer Design

1. Design an N-bit ALU with 4-bit ALUControl signal that fulfills the following operations.

ALUControl$_{3:1}$				**ALUControl$_{3:1}$**			**ALUControl$_0$=0**	**ALUControl$_0$=1**
1	0	0	A or B	0	0	0	A	A+1
1	0	1	A and B	0	0	1	A+B	A+B+1
1	1	0	A XOR B	0	1	0	A+B	A+B'+1
1	1	1	Complement A	0	1	1	B	B+1

2. Design a four bit arithmetic for the following operations.

ALUControl$_{2:1}$		**ALUControl$_0$=0**	**ALUControl$_0$=1**
0	0	A+B	A + B + 1
0	1	B' (complement)	B'+1 (negate)
1	0	A - 1	A
1	1	A + B	A + B' + 1 (subtract)

3. Design an arithmetic unit that performs the following operations. Sketch the schematics.

ALUControl$_{2:1}$		**ALUControl$_0$=0**	**ALUControl$_0$=1**
0	0	B'	B'+1
0	1	A'+B	A'+B+1
1	0	(A+B)'	((A+B)+1)'
1	1	A	A + 1

4. Design 4-bit left and right rotators. Sketch a schematic of your design.

5. Design an 8-bit left shifter using only 24 2:1 multiplexers. The shifter accepts an 8-bit input A and a 3-bit shift amount, shamt$_{2:0}$. The shifter produces an 8-bit output Y. Sketch the schematic of the circuit.

6. Design a 32-bit counter that will either increment by 4 or load a new 32-bit value, D, on each clock edge, depending on a control signal *Load*. When Load = 1, the counter loads the new value D.

7. An *N-bit Johnson counter* consists of an N-bit shift register with a reset signal. The output of the shift register (S_{out}) is inverted and fed back to the input (S_{in}). When the counter is reset, all of the bits are cleared to 0.
(a) Show the sequence of outputs, $Q_{3:0}$, produced by a 4-bit Johnson counter starting immediately after the counter is reset.
(b) How many cycles elapse until an N-bit Johnson counter repeats its sequence? Explain.

(c) Design a decimal counter using a 5-bit Johnson counter, ten AND gates, and inverters. The decimal counter has a clock, a reset, and ten one-hot outputs $Y_{9:0}$. When the counter is reset, Y_0 is asserted. On each subsequent cycle, the next output should be asserted. After ten cycles, the counter should repeat. Sketch a schematic of the decimal counter.
(d) What advantages might a Johnson counter have over a conventional counter?

8. Implement the following functions using a single 16 × 3 ROM. Use dot notation to indicate the ROM contents.

(a) X = AB+BC’D+A’B’
(b) Y = AB+BD
(c) Z = A+B+C+D

9. Specify the size of a ROM that you could use to program each of the following combinational circuits. Is using a ROM to implement these functions a good design choice? Explain why or why not.
(a) a 16-bit adder/subtractor with C_{in} and C_{out}
(b) an 8 × 8 multiplier