Digital Computer Design Laboratory

#1 SystemVerilog

1- Create the following two files **myfunction.sv** and **testbench1.sv**.

```
module myfunction(input  logic a, b, c,
                  output logic y);

  assign y = ~a & ~b & ~c |
              a & ~b & ~c |
              a & ~b &  c;
endmodule
```

myfunction.sv

```
module testbench1();
  logic  a, b, c, y;

  // instantiate device under test
  myfunction dut(a, b, c, y);

  // apply inputs one at a time
  initial begin
    a = 0; b = 0; c = 0; #10;
    c = 1;               #10;
    b = 1; c = 0;        #10;
    c = 1;               #10;
    a = 1; b = 0; c = 0; #10;
    c = 1;               #10;
    b = 1; c = 0;        #10;
    c = 1;               #10;
  end
endmodule
```

testbench1.sv

2- Create a project, add these files, simulate the project and observe the outputs.

3- Create the following files **fulladder.sv**.

```
module fulladder(input  logic a, b, cin,
                 output logic s, cout);

  logic p, g;

  assign p = a ^ b;
  assign g = a & b;

  assign s = p ^ cin;
  assign cout = g | (p & cin);
endmodule
```

fulladder.sv

4- Create a **testbench** for fulladder.

5- Create a project, add these files, simulate the project and observe the outputs.