Digital Computer Design Laboratory

#2 Structural Design

1- Create the following two files **MUX2.sv** and **MUX4.sv**.

```
module mux2(input logic [3:0] d0, d1,
     input logic s,
     output logic [3:0] y);

     assign y = s ? d1 : d0;

endmodule
```

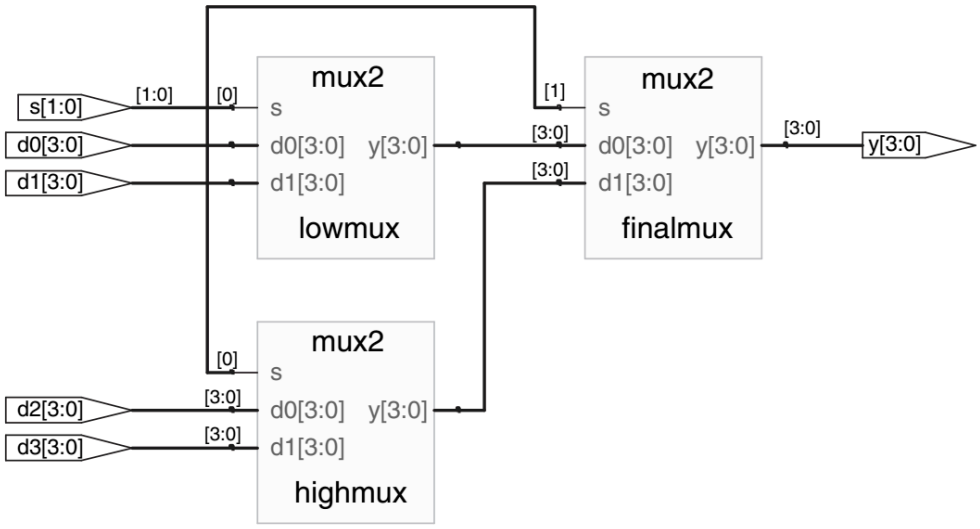
MUX2.sv

```
module mux4(input logic [3:0] d0, d1,
d2, d3,
input logic [1:0] s,
output logic [3:0] y);

     assign y = s[1] ?
     (s[0] ? d3 : d2):
     (s[0] ? d1 : d0);

endmodule
```

MUX4.sv

2- Create a project, add these files, **create testbenches** to simulate the project and observe the outputs.

3- Recreate the 4x1 multiplexer with 2x1 multiplexer to simulate 4x1 MUX circuit given below.



4x1 MUX Sythesized Circuit

4- Create a **testbench** for 4x1 MUX.

5- Create a project, add these files, simulate the project and observe the outputs.