**Digital Computer Design Laboratory**

**#5 SEQUENTIAL LOGIC**

**1-** Create the following flop.sv and testbench4flop.sv.

module flop(input logic clk, input logic d, output logic q);

always @(posedge clk)

q<=d;

endmodule

flop.sv

module testbench4flop();

reg D;

reg clk;

wire Q;

flop dut(clk,D,Q);

initial begin

clk=0;

forever #10 clk = ~clk;

end

initial begin

D <= 0;

#100;

D <= 1;

#100;

D <= 0;

#100;

D <= 1;

end

endmodule

testbench4flop.sv

**2-** Create a project, add these files, simulate the project and observe the outputs.

**3-** Create the FSM by using flop.sv. Create a testbench for your design and simulate your project.

