
Unit-2

Basic computer Architecture

8085 Microprocessor

Explain the features of 8085 in detail.

The features of 8085 include:

1) It is an 8-bit microprocessor i.e. it can accept, process or provide 8-bit data simultaneously.
2) It operates on a single +5V power supply connected at Vcc
3) It operates on clock cycle with 50% duly cycle.
4) It has on chip clock generator this internal clock generator requires tuned circuit like LC, RC or crystal. The internal clock generator divides oscillation frequency by 2 and generates clock signal, which can be used for synchronizing external devices.
5) It can operate with 3 MHz clock frequency.
6) It has 16 address buses, hence it can access 216 64 bytes of memory.
7) It provides 8 bit I/o address to acce4ss (28) 256 I / o ports.
8) In 8085, the lower 8-bit address bus (A0-A7) and data bus (D0-D7) are multiplexed to reduce number of external pins. But due to this, external hardware is required to separate address lines and data lines.
9) It supports 74 instructions with following addressing modes. (a) Immediate, (b) Register, (c) Direct (d) Indirect (e) Implied.
10) The Arithmetic logic unit of 8085 performs a) 8 bit binary addition with or without carry. (b) 16 bit binary addition (c) 2 digit BCD addition (d) 8-bit binary subtraction with or without borrow (e) 8-bit logical AND, OR, EX-OR, complement (NOT) and bit shift operations.
11) It has 8-bit accumulator, flag register, instruction, register, six 8-bit general purpose. Registers (B, C, D, E, H and C) and five 16-bit registers (SP and PC)
12) It provides five hardware interrupts: TRAP, RST 7.5. RST 6.5, RST 5.5 and INTR.
13) It has serial I/O control which allows serial communication.
14) It provides control signals (IO /M, RD, WR) to control bus cycles.
15) The external hardware (another microprocessor or equivalent master) can detect which machine cycle microprocessor is executing using status signals (IO/M, S0, S1) This feature is useful when more than one processors are using common system resources (memory & I/O devices).

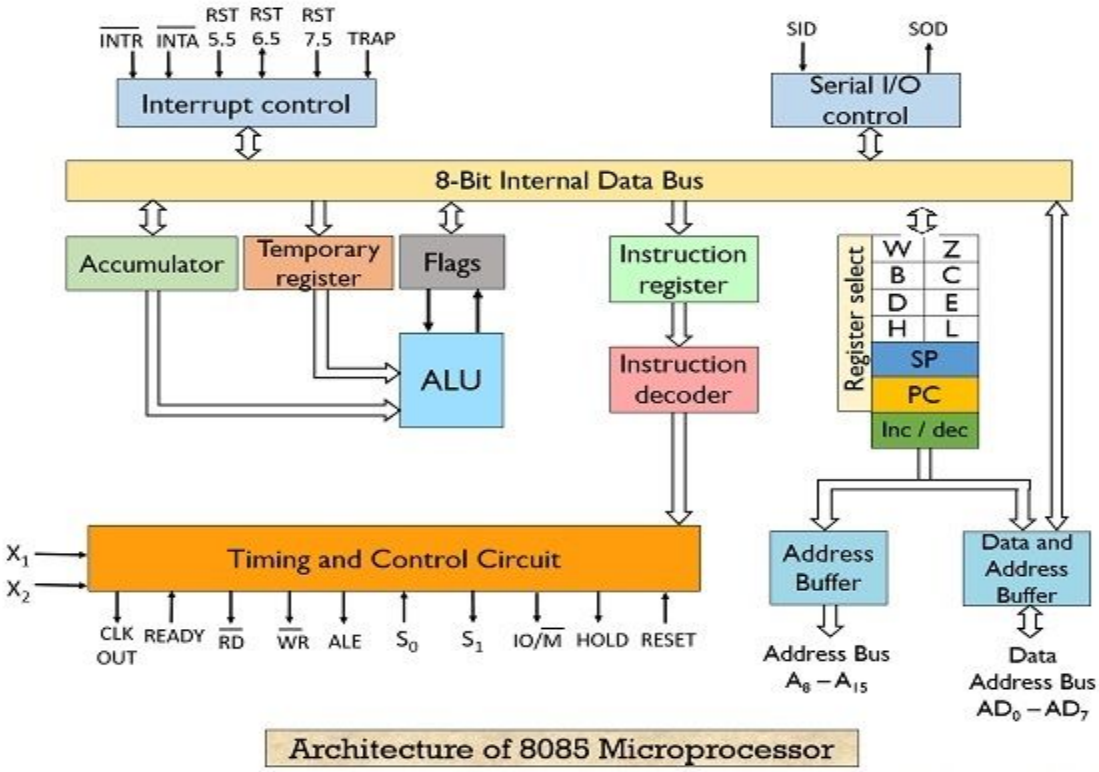
16) It has mechanism by which it is possible to increase its interrupt handling capacity.

17) The 8085 has an ability to share system bus with direct memory access controller. This feature allows to transfer large amount of data from I/O device to memory or from memory to I/O device with high speeds.

Draw and explain the architecture of 8085 microprocessor

There are mainly seven functional units of 8085 microprocessor

1. ***ALU***
2. **Timing and control unit**
3. **Instruction register and decoder**
4. **Register array**
5. **System bus**
6. **Interrupt Control**
7. **Serial I/O Control**



Architecture of 8085 Microprocessor

1. ALU

- The ALU performs the actual numerical and logic operation such as ‘add’, ‘subtract’, ‘AND’, ‘OR’ etc.

- Uses data from memory and from Accumulator to perform arithmetic operation and always stores result of operation in Accumulator.
- The ALU consists of accumulator, flag register and temporary register.

a. Accumulator

- The accumulator is an 8-bit register that is a part of arithmetic/logic unit (ALU). This register is used to store 8-bit data and to perform arithmetic and logical operations. The result of an operation is stored in the accumulator.
- The accumulator is also identified as register A.

b. Flag register

8085 has 8-bit flag register. There are only 5 active flags.

S	Z		AC		P		CY

Fig: 8085 flag register

Flags are flip-flops which are used to indicate the status of the accumulator and other register after the completion of operation.

These flip-flops are set or reset according to the data condition of the result in the accumulator and other registers.

i. Sign flag(S):

Sign flag indicates whether the result of a mathematical or logical operation is negative or positive.
If the result is negative, this flag will be set (i.e. S=1) and if the result is positive, the flag will be reset (i.e. S=0).

ii. Zero flag (Z):

Zero flag indicates whether the result of a mathematical or logical operation is zero or not.
If the result of current operation is zero, the flag will be set (i.e. Z=1) otherwise the flag will be reset (Z=0).
This flag will be modified by the result in the accumulator as well as in the other register.

iii. Auxiliary carry flag (AC):

In operation when a carry is generated by bit D3 and passes on to bit D4, the AC flag will be set otherwise AC flag will be reset.
This flag is used only internally for BCD operation and is not available for the programmer to change the sequence of program with the jump instruction.

iv. Parity flag (P):

This flag indicates whether the current result is of even parity (no. of 1's is even) or odd parity (no. of 1's is odd).
If even parity, P flag will be set otherwise reset.

v. Carry flag (CY):

This flag indicates whether during an addition or subtraction operation carry or borrow is generated or not.
If carry or borrow is generated, the flag will be set otherwise reset.

2. Timing and control unit

- This unit produces all the timing and control signal for all the operation.
- This unit synchronizes all the MP operations with the clock and generates the control signals necessary for communication between the MP and peripherals.

3. Instruction register and decoder

- The instruction register and decoder are part of ALU. When an instruction is fetched from memory, it is loaded in the instruction register.
- The decoder decodes the instruction and establishes the sequence of events to follow.
- The IR is not programmable and cannot be accessed through any instruction.

4. Register array

The register unit of 8085 consists of

✔ Six general-purpose data registers B,C,D,E,H,L

- ✔ Two internal registers W and Z
- ✔ Two 16-bit address registers PC (program counter) and SP (stack pointer)
- ✔ One increment/decrement counter register
- ✔ And, one multiplexer (MUX)

- The six general-purpose registers are used to store 8-bit data. They can be combined as register pairs BC, DE, and HL to perform some 16-bit operations.
- The two internal registers W and Z are used to hold 8-bit data during the execution of some instructions, CALL and XCHG instructions.
- SP is 16-bit registers used to point the address of da ta stored in the stack memory. It always indicates the top of the stack.
- PC is 16-bit register used to point the address of the next instruction to be fetched and executed stored in the memory.

5. System bus

a. Data bus:It carries 'data', in binary form, between MP and other external units, such as memory.
Typical size is 8 or 16 bits.

b. Address bus:It carries 'address' of operand in binary form.
Typical size is 16-bit.

c. Control Bus: Control Bus are various lines which have specific functions for coordinating and controlling MP operations. E.g.: Read/Write control line

6. Interrupt Control

- Interrupt is a signal, which suspends the routine what the MP is doing, brings the control to perform the subroutine, completes it and returns to main routine.
- May be hardware or software interrupts. Some interrupts may be ignored (maskable), some cannot (non-maskable).
- E.g. INTR, TRAP, RST 7.5, RST 6.5, RST 5.5

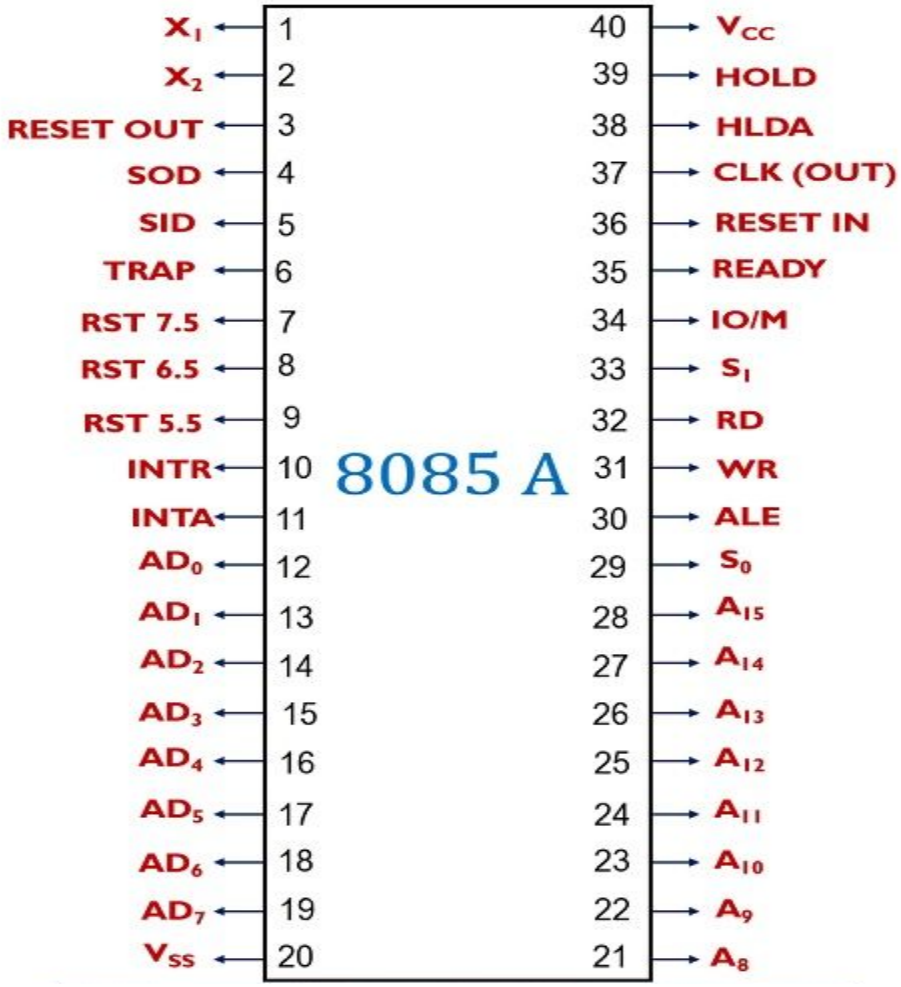
7. Serial I/O Control

- The MP performs serial data input or output (one bit at a time). In serial transmission, data bits are sent over a single line, one bit at a time.
- The 8085 has two signals to implement the serial transmission: **SID** (serial input data) and **SOD** (serial output data).

Draw the Pin Diagram of 8085 Microprocessor

An 8085 microprocessor is an IC with 40 pins and operates with +5V power supply. The pin configuration plays a very important role in understanding the architecture of 8085 microprocessor.

The figure below shows the pin diagram of 8085 showing 40 pin configurations:



The signals of this 40 pin IC is grouped into 7 categories, which are given below:

- Power supply and clock signals
- Data bus
- Address bus
- Serial I/O ports
- Control and status signals
- Interrupts and externally generated signals
- Direct memory access

1.Power supply and clock signals:

In 40 pin configuration, 4 pins are allotted to this particular category.

V_{CC} – Pin number 40 denotes V_{CC}, and an external power supply of + 5 V is provided at this pin.

V_{SS} – Its pin number is 20. This pin shows the grounded connection of the microprocessor.

X_1 and X_2 – These are represented by pin number 1 and 2 respectively in the pin configuration. These 2 pins are connected with a crystal or LC network to maintain the internal frequency of the clock generator.

CLK (OUT) – It is the 37th pin of the 8085 IC and acts as the system clock that keeps the record of time duration required by each operation to get completed.
z
2.Address Bus – This category contains 8 pins.

The address bus has 16 lines i.e.; it can carry 16 bits at a time. However, out of 16, 8 are multiplexed with the data bus and the leftover 8 are separately shown by pin number 21 to 28 in the pin configuration.

These are used to carry the address of data and instruction from the processor to the memory location and is unidirectional in nature. These are denoted by A_8 ***to*** A_{15} that represents the 8 MSB of the memory location or input-output address.

3.Data Bus with multiplexed address bus – This category also contains 8 pins.
The size of the data bus of the 8085 microprocessor is 8 bits. However, to reduce the number of bus lines these 8-bit data bus lines are multiplexed with the 8-bit address bus.These are shown by pin number 12 to 19. The address bus is denoted by A whereas the data bus is denoted by D. The pin configuration denotes the lower order multiplexed address and data bus bits from AD_0 ***to*** AD_7.

4.Serial I/O ports :
It has basically 2 pins.
SID – SID denotes serial input data pin and its pin is numbered as 5. With this pin, data is serially fed to the processor directly through the input devices.
SOD – SOD denotes serial output data pin and its pin number is 4, in the pin configuration of 8085. Once the data is processed in the microprocessor then this pin represents bit by bit results at the output devices.
5.Control and status signals :
Basically, 6 pins of the pin configuration are used by control and status signals.
ALE – ALE is an acronym for address latch enable and is pin number 30 in the configuration. We know that 8 lower order bits of the 16-bit address bus are multiplexed with the 8-bit data bus.
This pin gets enabled at the time when the address is present at the multiplexed address and data bus. Otherwise, it gets disabled showing the absence of an address on the bus.
RD – This pin is numbered 32 in the configuration and a low signal in this pin shows the read operation either from I/O devices or from the memory unit. Thereby indicating that the data bus is now in a state or position to accept the data from the memory or I/O devices.
WR – It is the 31st pin in the pin diagram and a low signal in this pin represents the write operation at the memory or I/O devices. This indicates that the data present in the data bus is to be written into the desired memory address or I/O device by the processor.
IO/M – It is pin number 34 and indicates the selection of a memory address or input-output device. This shows whether the read/write operation is to be carried out at the memory location or at the I/O device. The low signal at this pin shows that operation is performing over memory location. As against, a high signal at this pin represents the operation at I/O device.
S_0 and S_1 – The pins S_0 and S_1 represent the status signal at pin number 29 and 33 respectively. These signals show the type of recent operation of the microprocessor. The table below represents the status of th e data bus under different conditions:

IO/M	S_1	S_2	DATA BUS STATUS
0	0	0	Halt
0	0	1	Memory Write
0	1	0	Memory Read
1	0	1	IO Write
1	1	0	IO Read
0	1	1	Opcode fetch
1	1	1	Interrupt acknowledge

6.Interrupts and Externally generated signals:
Interrupts are the signals that are generated to break the sequence of an ongoing operation. When an interrupt signal is generated then CPU immediately stops its recent task under operation and switches to some other program known as interrupt service routine (ISR).
However, after handling ISR, the CPU gets back to its main program for execution.
In the pin configuration, 5 types of interrupts are shown by 5 different pins from pin number 6 to 10. These pins are used to manage the interrupt.
Basically, there exist 2 types of interrupts:
Maskable Interrupt and **Non- maskable interrupt**
Out of the 5 major interrupts 4 are the maskable interrupts. These are INTR, RST5.5, RST6.5, RST7.5 and are easily manageable interrupts.
However, TRAP is a non-maskable interrupt and holds the topmost priority among all interrupts in the 8085 microprocessor.
RESET IN – It is pin number 36 in the pin diagram. An active low signal at this pin resets the PC of the microprocessor to 0. Or we can say, after resetting the PC holds its initial memory address.
RESET OUT – It is the 3rd pin in the pin diagram. This pin generates a signal to provide information about the resetting of the microprocessor. Also, we can say that once a processor is reset then all the connected devices must also be reset.
So, enabling this signal shows the resetting of the interconnected devices.
INTA: It is the 11th pin of the 8085 pin configuration. A signal at this pin acknowledges the generated interrupt.
7. Direct Memory Access (DMA) :
We are aware of the fact that memory and I/O devices are connected with each other by the microprocessor. So, the intermediator i.e., CPU manages the data transfer between the input-output device and memory.
However, when data in a large amount is to be transferred between I/O devices and memory the CPU gets disabled by tri-stating its buses. And this transfer is manageable by external control circuits. The DMA has 2 pins.
HOLD – This signal is generated at pin number 39. This pin generates a signal to notify the processor that more than one request is present to access the data and address bus.
When this signal gets enabled, the CPU frees the bus after completion of the recent operation. Once the hold signal gets disabled, the processor can access the bus again.

HLDA -This signal is generated at pin number 38. This signal is enabled at the time when the processor gets HOLD signal and it releases HLDA i.e., hold acknowledge signal. In order to show that the multiple requests are kept on hold and will be considered once the bus gets free after the recent operation. After the disabling of hold request, the HLDA signal becomes low.

READY -This is the 35th numbered pin in the pin diagram that maintains synchronization between the processor and peripherals, memory. It is clear that a microprocessor has a much faster response than peripherals and memory.

So, this pin is enabled when the processor as well as the peripherals and memory both become ready to begin the next operation.

In the case when the READY pin is disabled, then the microprocessor is in the WAIT state.

Explain the various addressing modes of 8085 microprocessor with example.

The term addressing modes refers to the way in which the operand of an instruction is specified. The addressing mode specifies a rule for interpreting or modifying the address field of the instruction before the operand is actually executed.

The 8085 has 5 addressing modes. These are:

1. Immediate addressing mode: In an immediate addressing mode, 8 or 16 bit data can be specified as a part of instruction. In 8085, the instructions having 'I' letter fall under this category. "I' indicates immediate addressing mode.

Example: MVI A, 20H: moves 8-bit immediate data(20H) into accumulator.

LXI D,10FF H : moves 16-bit immediate data into DE register pair.

2. Register addressing mode: The register addressing mode specifies the source operand, destination operand or both to be contained in an 8085 registers. This results in faster execution, since it is not necessary to access memory locations for operands.

Example: MOV A, B :Moves the contents of register B into the accumulator.

SPHL: Moves the contents of HL register pair into stack pointer.

3. Direct addressing mode: The direct addressing mode specifies the 16- bit address of the operand within the instruction itself. The second and third bytes of instruction contain this 16 bit address.

Example: LDA 2000H: loads the 8bit contents of memory location 2000H into the accumulator

SHLD 3000H : Stores the HL register pair into two consecutive memory locations. Lower contents of L register into memory location 3000H and higher contents of H register into memory location 3001H.

4. Indirect addressing mode: In indirect addressing mode, the memory address where the operand located is specified by the contents of a register pair.

Example: LDAX B : loads the accumulator with the contents of memory location pointed by BC register pair.

MOV M, A : Stores the contents of accumulator into the memory location pointed by HL register pair

5. Implied addressing mode: In implied addressing mode, Opcode specifies the address of the operands.

Example: CMA: Complements contents of accumulator.

RAL: Rotates the contents of accumulator left through the carry.

Difference between 8085 & 8086 Microprocessor

8085 Microprocessor	8086 Microprocessor
Is an 8 Bit Microprocessor	Is a 16 Bit Microprocessor
Has 8 bit data bus	Has 16 bit data bus
Has 16 bit address line	Has 20 bit address line
Only 64KB of memory can be used (2^{16})	1 MB of memory can be used (2^{20})

Has 5 Flags (Carry , Parity, Sign, Zero, Auxillary Carry)	Has 9 Flags (Carry, parity, Sign, Zero, Auxillary Carry, Direction, Trap, Interrupt, Overflow)
It is Accumulator based processor	It is general purpose Register Based processor
It has no MIN mode or MAX mode	It can operate in any one of MIN or MAX Mode
Does not support popelining	Supports pipelining
Does not support Memory segmentation	Supports Memory Segmentation
Has 6500 transistors	Has 29000 transistors

	8085	8086
1. Size	8 bit microprocessor	16 bit microprocessor
2. Address Bus	16 Bit address bus	20 bit address bus
3. Memory	can access upto 2^16 = 64 KB of memory	can access upto 2^20 = 1MB of memory
4. Instruction Queue	doesn't have an instruction queue	has instruction queue
5.Pipelining	does not support pipelined architechture	supports pipelined architechture
6. Multiprocessing Support	does not support multiprocessing support	supports multiprocessing support
7. I/O	can address 2^8= 256 I/O's	can access 2^16= 65.536/O's
8. Arithmetic support	only supports integer and decimal	supports integer, decimal and ASCII arithmetic
9. Multiplication and Division	Doesn't support	Supports
10. Operating Mides	supports only single operating mode	operates in two modes
11. External Hardware	Requires less	Requires
12. Cost	Low	High
13. Memory segmentation	Memory space is not segmented	Memory space is segmented

8085 Microprocessor	8086 Microprocessor
It is an 8-bit Microprocessor	It is 16 bit microprocessor
It has 16 bit address line	It has 20 bit address line
It has 8 bit data bus	It has 16 bit data bus
Clock speed of 8085 microprocessor is 3 MHZ	Clock speed of 8086 microprocessor vary between 5,8and 10 MHz for different versions.
It has 5 flags	It has 9 flags
It does not support pipelining	It supports pipelining.

It operates on clock cycle with 50% duty cycle.	It operates on clock cycle with 33% duty cycle.
8085 Microprocessor does not support memory segmentation.	8086 microprocessor supports memory segmentation.
It has less number of transistors compare to 8086 microprocessor. It is about 65000 in size.	It has more number of transistors compare to 8085 microprocessor. It is about 29000 in size.
It is accumulator based processor.	it is general purpose register based processor.

8086 Microprocessor

Write the silent features of 8086 Microprocessor

1) 8086 microprocessor is a general purpose register based processor.
2) The size of the data bus in 8086 microprocessor is 16-bit.
3) The size the address bus in 8086 microprocessor is 20-bit.
4) The clock speed in 8086 microprocessor was initially limited to 5MHz but it goes up to 10 MHz nowadays.
5) The flag register in 8086 microprocessor contains 9 flags that is, Overflow Flag, Direction Flag, Interrupt Flag, Trap Flag, Sign Flag, Zero Flag, Auxiliary Flag, Carry Flag and Parity Flag.
6) The microprocessor supports pipe-lining as it has two independent units; the Execution unit (EU) and Bus Interface Unit (BIU).
7) 8086 microprocessor holds a very large number of transistors in its structure. It is about 29000 in size.
8) 8086 microprocessor supports two modes of operation, that is minimum and maximum mode.
9) 8086 microprocessor supports memory segmentation.
10) 8086 microprocessor supports integer, decimal and ASCII arithmetic.
11) It requires more external hardware.
12) 8086 has multiplication and division instructions.
13) 8086 can access up to 1MB of memory.
14) 8086 is a multi-processor configuration microprocessor.
15) The instruction queue is supported in 8086 microprocessor.

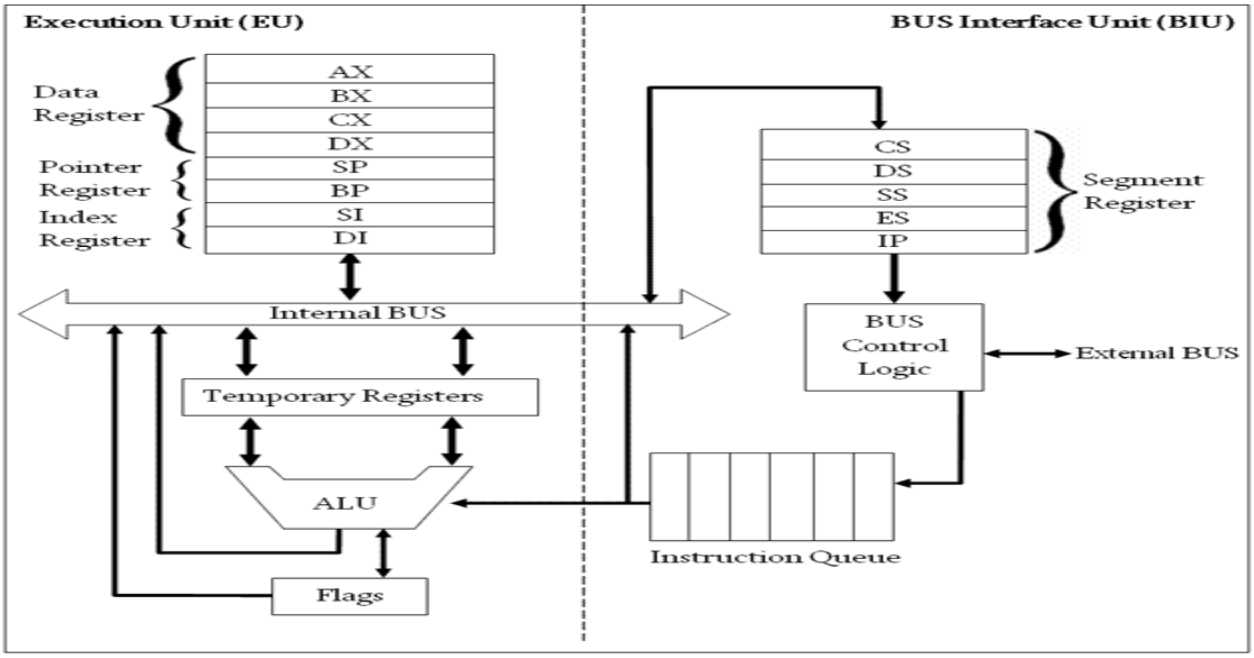
Draw the 8086 architecture with the help of its EU and BIU

The 8086 is a 16-bit microprocessor. The term 16 bit implies that its arithmetic logic unit, its internal registers, and most of its instructions are intended to work with 16 bit binary data. The 8086 has a 16 bit data bus, so it can read data from or write data to memory and ports either 16 bits or 8 bits at a time. The 8086 has a 20 bit address bus

The 8086 CPU is divided into two independent functional units:

1. Bus Interface Unit (BIU)

2. Execution Unit (EU)



Bus Interface Unit (BIU)

It handles all transfers of data and addresses on the buses for the execution unit. •Sends out addresses
•Fetches instructions from memory
•Read / write data from/to ports and memory i.e. handles all transfers of data and addresses on the busses

Execution Unit (EU)

•Tells BIU where to fetch instructions or data from
•Decodes instructions

Explain the 8086 Microprocessor with all functional units

1) EU (Execution Unit)

Execution unit gives instructions to BIU stating from where to fetch the data and then decode and execute those instructions. Its function is to control operations on data using the instruction decoder & ALU. EU has no direct connection with system buses as shown in the above figure, it performs operations over data through BIU.

Let us now discuss the functional parts of 8086 microprocessors.

ALU

It handles all arithmetic and logical operations, like +, −, ×, /, OR, AND, NOT operations.

Flag Register

It is a 16-bit register that behaves like a flip-flop, i.e. it changes its status according to the result stored in the accumulator. It has 9 flags and they are divided into 2 groups − Conditional Flags and Control Flags.

Conditional Flags

It represents the result of the last arithmetic or logical instruction executed. Following is the list of conditional flags −

Carry flag − This flag indicates an overflow condition for arithmetic operations.

Auxiliary flag − When an operation is performed at ALU, it results in a carry/barrow from lower nibble (i.e. D0 – D3) to upper nibble (i.e. D4 – D7), then this flag is set, i.e. carry given by D3 bit to D4 is AF flag. The processor uses this flag to perform binary to BCD conversion.
Parity flag − This flag is used to indicate the parity of the result, i.e. when the lower order 8-bits of the result contains even number of 1's, then the Parity Flag is set. For odd number of 1's, the Parity Flag is reset.
Zero flag − This flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to 0.
Sign flag − This flag holds the sign of the result, i.e. when the result of the operation is negative, then the sign flag is set to 1 else set to 0.
Overflow flag − This flag represents the result when the system capacity is exceeded.
Control Flags
Control flags controls the operations of the execution unit. Following is the list of control flags −
Trap flag − It is used for single step control and allows the user to execute one instruction at a time for debugging. If it is set, then the program can be run in a single step mode.
Interrupt flag − It is an interrupt enable/disable flag, i.e. used to allow/prohibit the interruption of a program. It is set to 1 for interrupt enabled condition and set to 0 for interrupt disabled condition.
Direction flag − It is used in string operation. As the name suggests when it is set then string bytes are accessed from the higher memory address to the lower memory address and vice-a-versa.
General purpose register
There are 8 general purpose registers, i.e., AH, AL, BH, BL, CH, CL, DH, and DL. These registers can be used individually to store 8-bit data and can be used in pairs to store 16bit data. The valid register pairs are AH and AL, BH and BL, CH and CL, and DH and DL. It is referred to the AX, BX, CX, and DX respectively.
AX register − It is also known as accumulator register. It is used to store operands for arithmetic operations.
BX register − It is used as a base register. It is used to store the starting base address of the memory area within the data segment.
CX register − It is referred to as counter. It is used in loop instruction to store the loop counter.
DX register − This register is used to hold I/O port address for I/O instruction.
Stack pointer register
It is a 16-bit register, which holds the address from the start of the segment to the memory location, where a word was most recently stored on the stack.

2) BIU (Bus Interface Unit)

BIU takes care of all data and addresses transfers on the buses for the EU like sending addresses, fetching instructions from the memory, reading data from the ports and the memory as well as writing data to the ports and the memory. EU has no direction connection with System Buses so this is possible with the BIU. EU and BIU are connected with the Internal Bus.
It has the following functional parts −
Instruction queue − BIU contains the instruction queue. BIU gets up to 6 bytes of next instructions and stores them in the instruction queue. When EU executes instructions and is ready for its next instruction, then it simply reads the instruction from this instruction queue resulting in increased execution speed.
Fetching the next instruction while the current instruction executes is called **pipelining**.
Segment register − BIU has 4 segment buses, i.e. CS, DS, SS& ES. It holds the addresses of instructions and data in memory, which are used by the processor to access memory locations. It also contains 1 pointer register IP, which holds the address of the next instruction to executed by the EU.

CS – ***It stands for Code Segment.*** It is used for addressing a memory location in the code segment of the memory, where the executable program is stored.
DS – ***It stands for Data Segment.*** It consists of data used by the program and it accessed in the data segment by an offset address or the content of other register that holds the offset address.
SS – ***It stands for Stack Segment.*** It handles memory to store data and addresses during execution.
ES – ***It stands for Extra Segment.*** ES is additional data segment, which is used by the string to hold the extra destination data.
Instruction pointer – It is a 16-bit register used to hold the address of the next instruction to be executed.

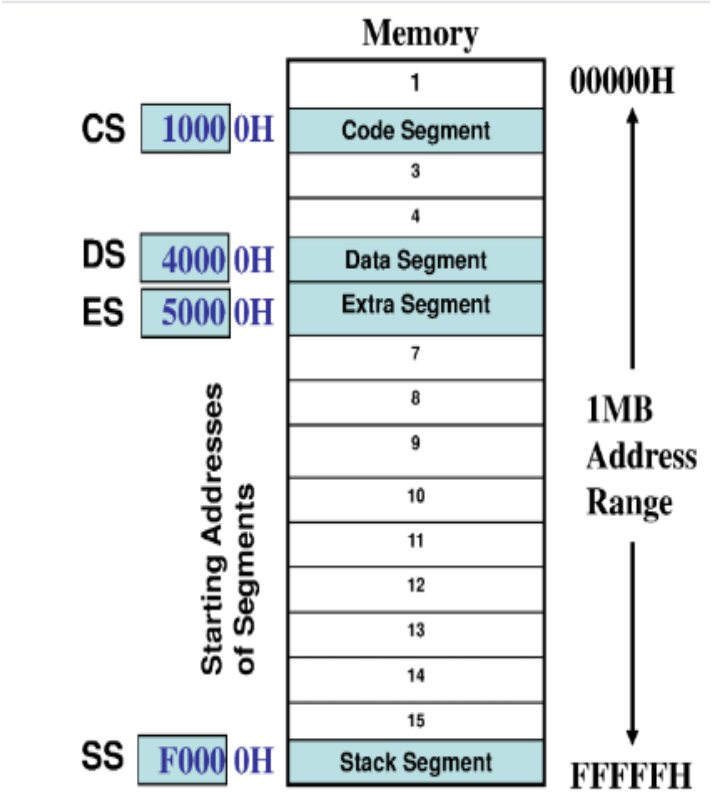
Note: Summary of register

Data Registers
AX = Accumulator Register
BX = Base Register
DX = Data Register
CX = Count Register

Index Registers
SI = Source Index
DI = Destination Index

Segment Registers
DS = Data Segment
SS = Stack Segment
ES = Extra Segment
CS = Code Segment

Pointer Registers
IP = Instruction Pointer
BP = Base Pointer
SP = Stack Pointer



Explain the various addressing modes of 8086 microprocessor with example.

ADDRESSING MODES OF 8086
1) Immediate addressing mode
2) Register addressing mode
3) Direct memory addressing mode
4) Register based indirect addressing mode
5) Register relative addressing mode
6) Base indexed addressing mode
7) Relative based indexed addressing mode

8) Implied addressing mode

1) Immediate addressing mode

The addressing mode in which the data operand is a part of the instruction itself is known as immediate addressing mode.

Example: *MOV CX, 4929 H, ADD AX, 2387 H, MOV AL, FFH*

2) Register addressing mode

It means that the register is the source of an operand for an instruction.

Example: MOV CX, AX ; copies the contents of the 16-bit AX register into
; the 16-bit CX register),
ADD BX, AX

3) Direct addressing mode

The addressing mode in which the effective address of the memory location is written directly in the instruction.

Example: MOV AX, [1592H], MOV AL, [0300H]

4) Register indirect addressing mode

This addressing mode allows data to be addressed at any memory location through an offset address held in any of the following registers: BP, BX, DI & SI.

Example: MOV AX, [BX] ; Suppose the register BX contains 4895H, then the contents
; 4895H are moved to AX
ADD CX, {BX}

5) Based addressing mode

In this addressing mode, the offset address of the operand is given by the sum of contents of the BX/BP registers and 8-bit/16-bit displacement.

Example: MOV DX, [BX+04], ADD CL, [BX+08]

6) Indexed addressing mode

In this addressing mode, the operands offset address is found by adding the contents of SI or DI register and 8-bit/16-bit displacements.

Example: MOV BX, [SI+16], ADD AL, [DI+16]

7) Based-index addressing mode

In this addressing mode, the offset address of the operand is computed by summing the base register to the contents of an Index register.

E***xample:*** ADD CX, [AX+SI], MOV AX, [AX+DI]

8) Based indexed with displacement mode

In this addressing mode, the operands offset is computed by adding the base register contents. An Index registers contents and 8 or 16-bit displacement.

Example: MOV AX, [BX+DI+08], ADD CX, [BX+SI+16]

What is pipeline? Explain instruction pipeline in brief

Pipeline in 8086 is a technique which is used in advanced microprocessors, was the microprocessor executes a second instruction before the completion of first. That is many instructions are simultaneously pipelined at different processing stage.

The advantages of pipelining is performance improvement, we are able to pump more instructions and get improved in processor speed as we are able to execute parts of instructions in parallel to parts of other instruction.

An instruction pipeline reads instruction from the memory while previous instructions are being executed in other segments of the pipeline. Thus we can execute multiple instructions simultaneously. The pipeline will be more efficient if the instruction cycle is divided into segments of equal duration. In the most general case computer needs to process each instruction in following sequence of steps:

1) Fetch the instruction from memory (FI)
2) Decode the instruction (DA)
3) Calculate the effective address
4) Fetch the operands from memory (FO)
5) Execute the instruction (EX)
6) Store the result in the proper place

Instruction Branch

Stage	1	2	3	4	5	6	7	8	9	10	11	12	13
1	FI	DA	FO	EX									
2		FI	DA	FO	EX								
3			FI	DA	FO	EX							
4				FI	---	---	FI	DA	FO	EX			
5								FI	DA	FO	EX		
6									FI	DA	FO	EX	
7										FI	DA	FO	EX

Here the instruction is fetched on first clock cycle in segment 1.
Now it is decoded in next clock cycle, then operands are fetched and finally the instruction is executed. We can see that here the fetch and decode phase overlap due to pipelining. By the time the first instruction is being decoded, next instruction is fetched by the pipeline.
In case of third instruction we see that it is a branched instruction. Here when it is being decoded 4th instruction is fetched simultaneously.

What is Memory Segmented? List out the advantages and disadvantages of memory Segmentation

Segmentation is the process in which the main memory of the computer is logically divided into different segments and each segment has its own base address. It is basically used to enhance the speed of execution of the computer system, so that the processor is able to fetch and execute the data from the memory easily and fast.

Need for Segmentation –

The Bus Interface Unit (BIU) contains four 16 bit special purpose registers (mentioned below) called as Segment Registers.

Code segment register (CS): is used for addressing memory location in the code segment of the memory, where the executable program is stored.

Data segment register (DS): points to the data segment of the memory where the data is stored.

Extra Segment Register (ES): also refers to a segment in the memory which is another data segment in the memory.
Stack Segment Register (SS): is used for addressing stack segment of the memory. The stack segment is that segment of memory which is used to store stack data.

Advantages of the Segmentation The main advantages of segmentation are as follows:

- It provides a powerful memory management mechanism.
- Data related or stack related operations can be performed in different segments.
- Code related operation can be done in separate code segments.
- It allows to processes to easily share data.
- It allows extending the address ability of the processor, i.e. segmentation allows the use of 16 bit registers to give an addressing capability of 1 Megabytes. Without segmentation, it would require 20 bit registers.
- It is possible to enhance the memory size of code data or stack segments beyond 64 KB by allotting more than one segment for each area.

Disadvantages of Memory Segmentation

• It is a costly technique as compared to the other one.
• External fragmentation is there in it.
• Since there is a variably sized partition. So, it is difficult to allocate memory to them.

Important question for Exam:

1) *Draw and explain the pin diagram of 8085 Microprocessor.*
2) *Explain 8086 architecture with the help of its EU and BIU*
3) *Draw the 8086 architecture with the help of its EU and BIU*
4) *Explain the addressing mode of 8085 Microprocessor.*
5) *Explain the addressing mode of 8086 Microprocessor.*
6) *What is pipeline? Explain instruction pipeline in brief*

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