#Define 80286 Microprocessor? Explain the features of 80286 Microprocessor.

80286 Microprocessor is a 16-bit microprocessor that has the ability to execute 16-bit instruction at a time. It has non-multiplexed data and address bus. The size of data bus is 16-bit whereas the size of address bus is 24-bit.It was invented in February 1982 by Intel. 80286 microprocessor was basically an advancement of 8086 microprocessor. Further in 1985, Intel produced upgraded version of 80286 which was a 32-bit microprocessor.

Features of 80286 Microprocessor

- ✓ The Intel 80286 is a high-performance ***16-bit microprocessor.***
- ✓ It has been specially designed for ***multiuser and multitasking systems.***
- ✓ Various versions of 80286 are available that run on ***12.5 MHz,10 MHz and 8MHz clock frequencies.***
- ✓ 80286 is upwardly compatible with 8086 in terms of instruction set. (That is the 8086,8088,80186,80286 CPU family all contain the same instruction set)
- ✓ The memory management which is an important task of the operating system is now supported by a hardware unit called memory management unit.
- ✓ The 80286 is the first CPU to incorporate the integrated memory management unit.
- ✓ It has four-level memory protection and support for virtual memory and operating system
- ✓ It is available in variety of pin packages such as 68-pin PLCC (Plastic Leaded Chip Carrier), Ceramic LCC (Leadless Chip Carrier), and PGA(Pin Grid Array).
- ✓ It has 24 address lines and 16 data lines. υ There are two operating modes for 80286
- ✓ The real address mode
- ✓ The protected virtual memory address mode
- ✓ In real address mode the processor can address up to 1MB of physical memory.
- ✓ The virtual address mode is for multiuser/multitasking system. In this mode of operation the memory management unit can manage up to 1GB of virtual memory.
- ✓ In virtual address mode one user cannot interface with the other. Also users cannot interface with operating system. These features are called protection

#Write some advantage of 80286 Microprocessor over 8086 Microprocessor.

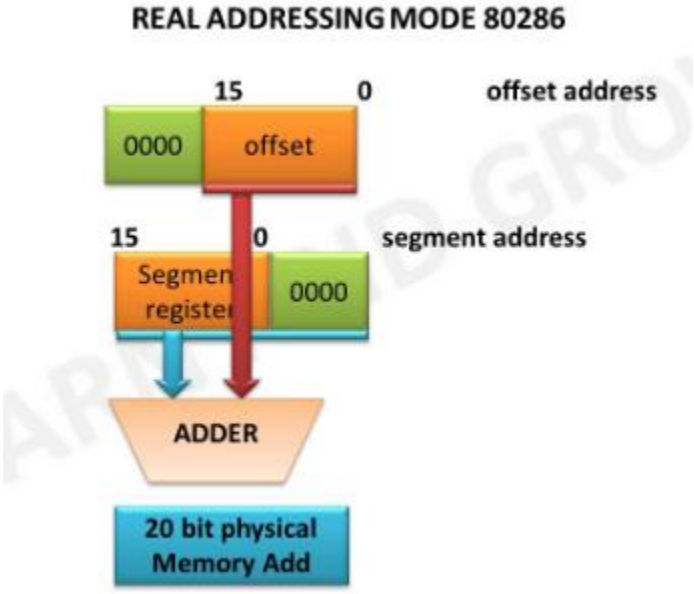
80286 more advantageous than 8086 microprocessor are

- It has non-multiplexed address and data bus that reduces operational speed.
- The addressable memory in case of 80286 is 16 MB.
- It offers an additional adder for address calculation.
- 80286 has faster multipliers that lead to quick operation.
- The performance per clock cycle of 80286 is almost twice when compared with 8086 or 8088.
- 80286 in PVAM can address up to 8192 virtual memory segment of 64k bytes each.
- The 80286 then has a virtual address space of 1 Gigabyte

#Explain the mode of Operating modes of 80286 microprocessor Operating Modes of 80286

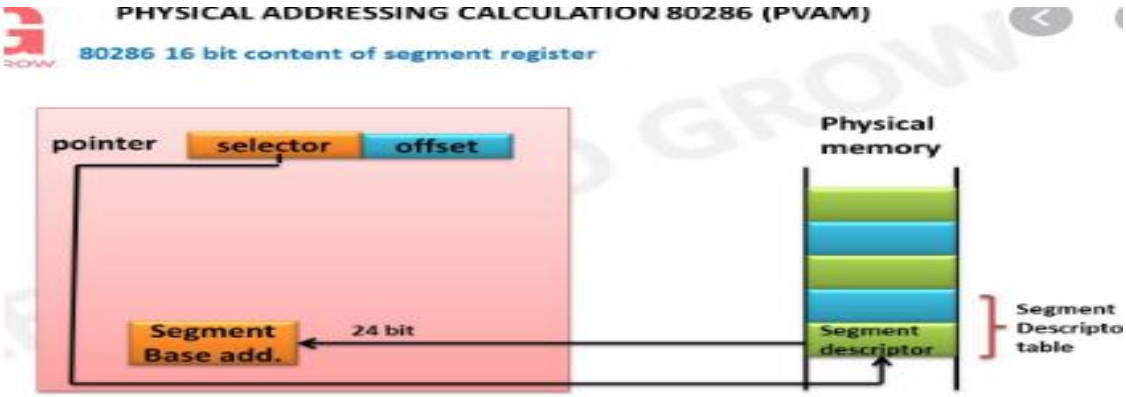
Real Address Mode

- 80286 just act as a faster version of 8086.
- And program for 8086 can be executed without modification in 80286.
- In **real** address mode the processor can address up to **1 MB** of physical memory.



Protected Virtual Address Mode

- 80286 supports multitasking because multiple programs can be executed using virtual memory.
- Able to run several program at the same time
- Able to protect memory space for another program
- In this mode the processor can address up to 16 MB of physical memory whereas 8086 can address only 1 MB.
- In this mode the processor can address up to **1 GB** of virtual memory.
- 80286 can treat external storage as it were physical memory and execute programs that are too large to be contained in physical memory.



As using virtual memory, space for other programs can be saved. Sometimes bulky programs also do exist that cannot be stored in physical memory, so virtual memory is utilized in order to execute large programs. This mode is used in 80286, so that in case of memory failure in real address mode, it can stay in protected manner.

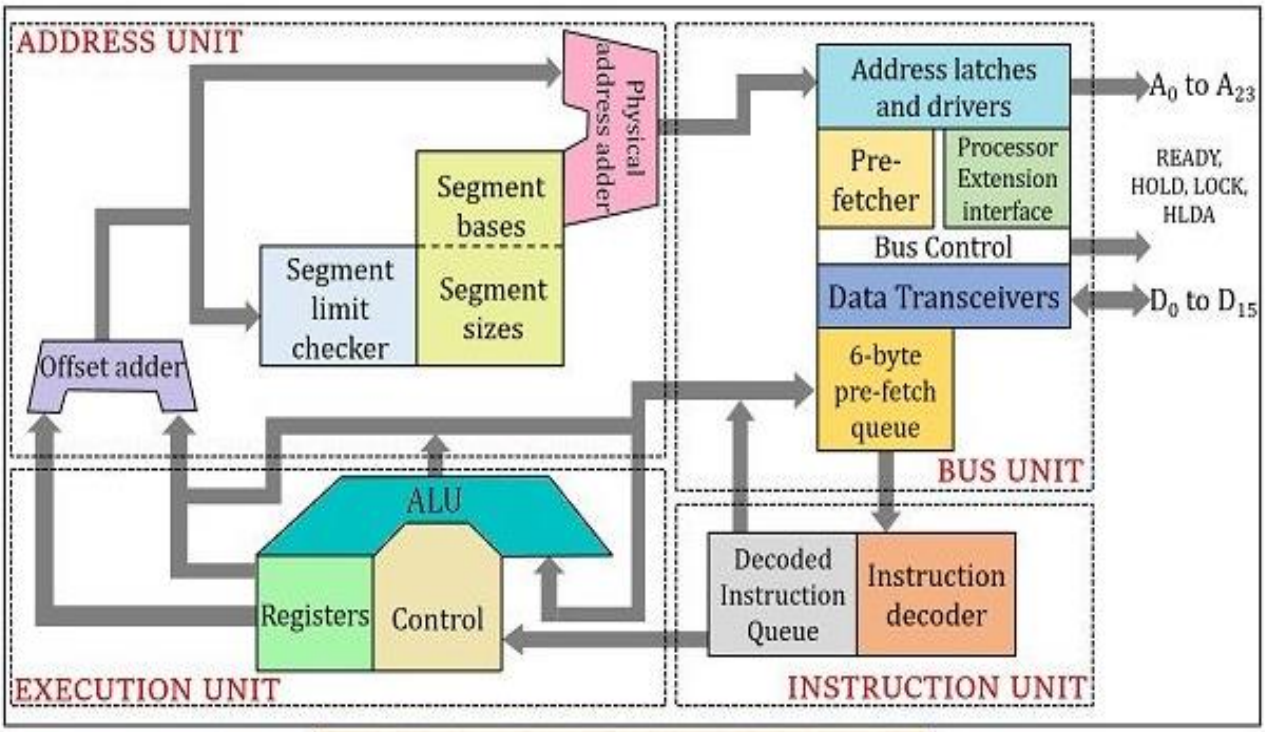
#Write the difference between Real Address Mode and Protected Virtual Address Mode

Real Address Mode	*Protected Virtual Address Mode*
Can only address 1MB of system memory and act as fast 8086	Can address till 16MB of system memory
Doesn't supports the concept of virtual memory.	Supports the concept of virtual memory
Real mode provides not support for memory protection, multitasking, or code privilege levels.	Protected mode provides support for memory protection, multitasking, or code privilege levels.
Initially every processor is in Real Mode i.e MSW PE= 0	Microprocessor will switch to this mode by setting MSW PE- bit

#Draw the Microprocessor of 80286 and explain the functional unit of its.

The CPU, central processing unit of 80286 microprocessor, consists of 4 functional block:

- Address Unit
- Bus Unit
- Instruction Unit
- Execution Unit



Block Diagram of 80286 Microprocessor

Electronics Desk

Internal Block Diagram of 80286 ∪ The CPU may be viewed to contain four functional parts, viz.
(a) Address Unit (AU)
(b) Bus Unit (BU)
(c) Instruction Set (IU)
(d) Execution Unit (EU)

Address unit

Calculate the physical addresses of the instruction and data that the CPU want to access
•Address lines derived by this unit may be used to address different peripherals.
•Physical address computed by the address unit is handed over to the BUS unit.

Bus Interface Unit

•Performs all memory and I/O read and write operations.
•Take care of communication between CPU and a coprocessor.
•Transmit the physical address over address bus A0– A23.
•Prefetcher module in the bus unit performs this task of prefetching.
•Bus controller controls the prefetcher module.
•Fetched instructions are arranged in a 6 – byte prefetch queue.

Instruction Unit

•Receive arranged instructions from 6 byte prefetch queue.
•Instruction decoder decodes up to 3 prefetched instruction and are latched them onto a decoded instruction queue.
•Output of the decoding circuit drives a control circuit in the Execution unit.

Execution unit

•EU executes the instructions received from the decoded instruction queue sequentially. •Contains Register Bank.
•contains one additional special register called Machine status word (MSW) register --- lower 4 bits are only used.
•ALU is the heart of execution unit.
•After execution ALU sends the result either over data bus or back to the register bank.

Or

The Address Unit (AU) is responsible for calculating the physical address of instructions and data that CPU wants to access.

This physical address computed by the address unit is handed over to the Bus Unit (BU) of the CPU.

The address latches and drivers in the bus unit transmit the physical address thus formed over the address bus A0-A23.

One of the major function of the bus unit is to fetch instruction bytes from the memory.

The Instruction Unit(IU) accepts instructions from the prefetch queue and an instruction decoder decodes them one by one. υ The output from the decoding circuit drives a control circuit in the Execution Unit (EU) is responsible for instructions received from the decoded instruction queue, which sends the data part of the instruction over the data bus.

#Explain the register used in 80286

The 80286 CPU contains almost the same set of registers, as in 8086

(a) Eight 16-bit general purpose registers

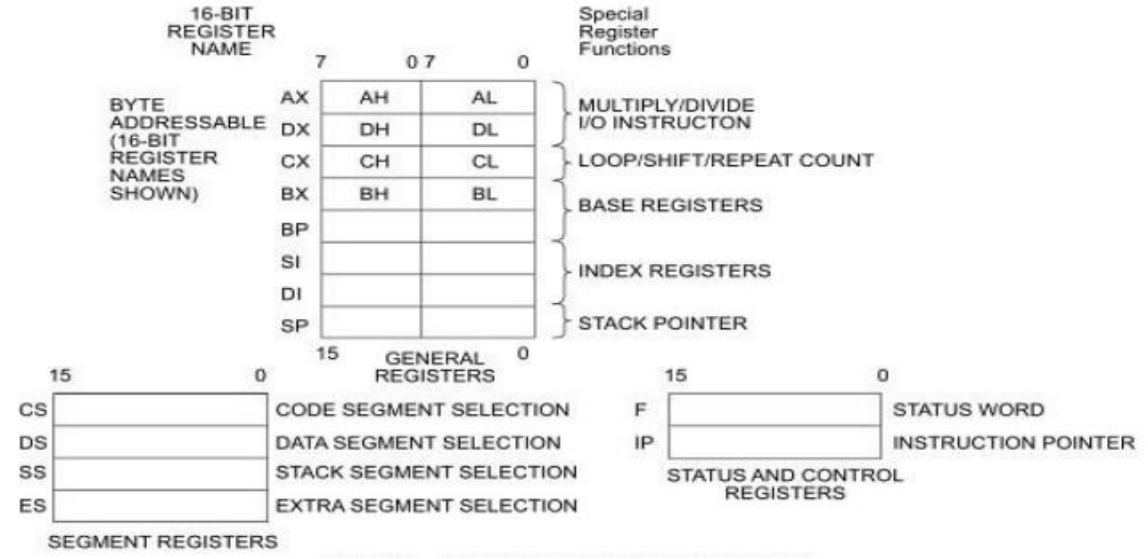
(b) Four 16-bit segment registers

(c) Status and control register

(d) Instruction Register

The flag register bits D0, D2, D4, D6, D7 and D11 are modified according to the result of the execution of logical and arithmetic instructions. These are called status flag bits.

Register Set of 80286



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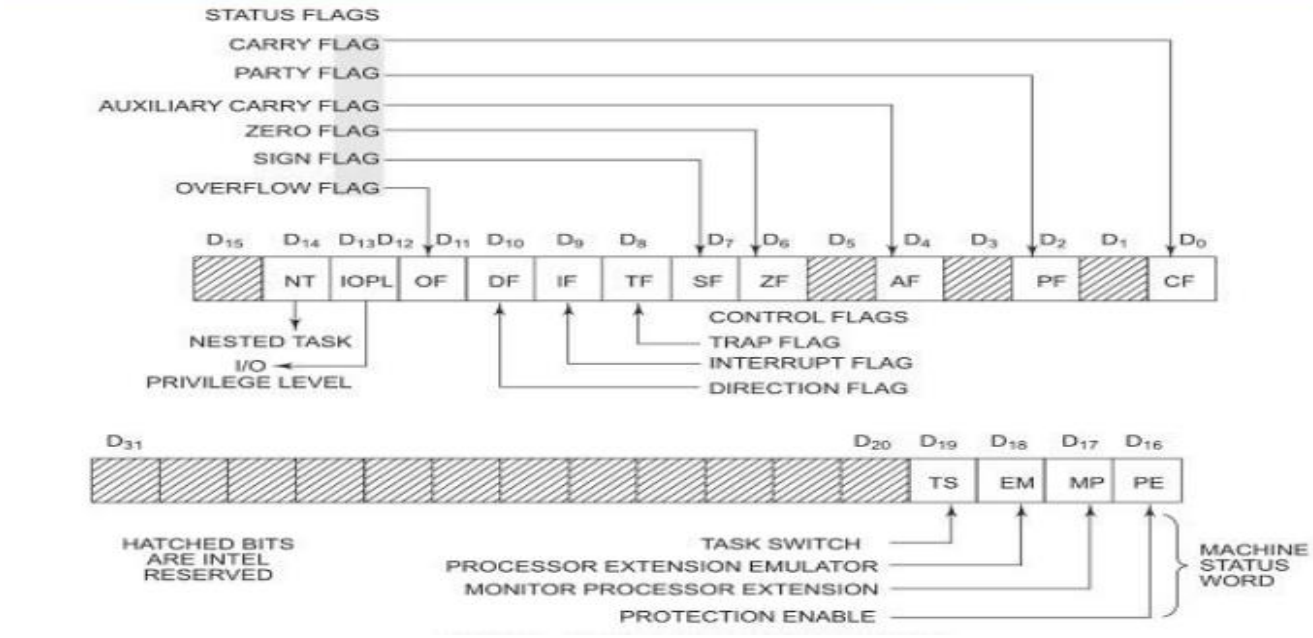
80286 Flag Register



The additional fields available in 80286 flag registers are,

IOPL-I/O Privilege Field (bits D12 and D13)
NT - Nested Task flag (bit D14)
PE - Protection Enable (bit D16)
MP – Monitor Processor Extension (bit D17)
Processor Extension Evaluator (bit D19)

Machine Status Flag (MSW)

The machine status word consists of four flags.

- These are – PE,MP,EM, and TS of the four lower order bits D19 to D16 of the upper word of the flag register.
- The LMSW and SMSW instructions are available in the instruction set of 80286 to write and read the MSW in real address mode.

#Explain Privilege level of 80286 Microprocessor

There are four types of privilege levels

1. 00 - kernel level (highest privilege level)
2. 01 - OS services
3. 10 - OS extensions
4. 11 - Applications (lowest privilege level)

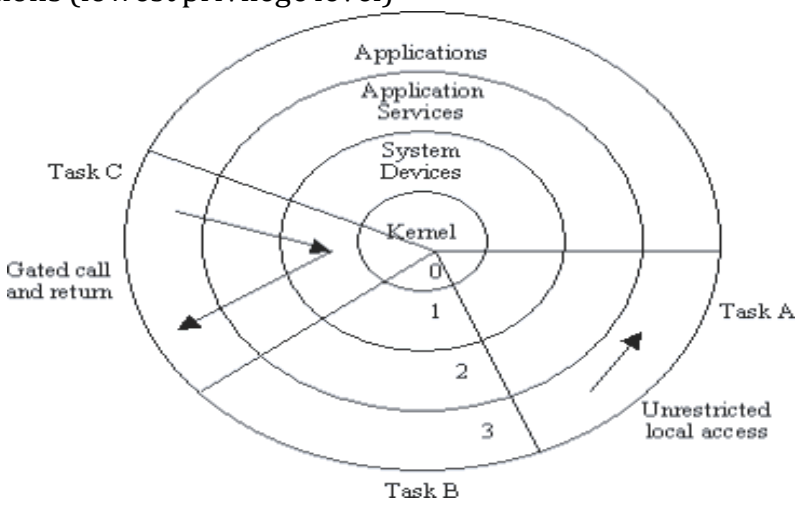


Figure: Privilege Level

- Each task assigned a privilege level, which indicates the priority or privilege of that task.
- It can only changed by transferring the control, using gate descriptors, to a new segment.
- A task executing at level 0, the most privileged level, can access all the data segment defined inGDT and LDT of the task.
- A task executing at level 3, the least privileged level, will have the most limited access to data andother descriptors.
- The use of rings allows for system software to restrict tasks from accessing data.
- In most environments, the operating system and some device drivers run in ring 0 and applicationsrun in ring 3.

#Explain LDT, GDT and IDT. Differentiate LDT and GDT

Global Descriptor Table (GDT):

- The 80286 has a single Global Descriptor Table (**GDT**) which is shared between all tasks and addresses up to 512MB of the virtual address space.
- The **Global Descriptor Table** or GDT is a data structure used by Intel x86-family processors starting with the 80286 in order to define the characteristics of the various memory areas used during program execution, including the base address, the size and access privileges like execute-ability and write-ability.

Local Descriptor Table (LDT):

- Each task will have its own Local Descriptor Table (LDT) which is a private 512MB of address space.
- LDT is essential to implement separate address spaces for multiple processes.
- The operating system will switch the current LDT when scheduling a new process, using the LDTmachine instruction.

Descriptor Table (LDT):

- IDT used to store interrupt gates and task gate

  LIDT instruction is used to Load Interrupt Descriptor table.

Differentiate LDT and GDT:

- LDT is actually defined by a descriptor inside the GDT, while the GDT is directly defined by a linearaddress.
- The lack of symmetry between both tables is underlined by the fact that the current LDT can be automatically switched on certain events, notably if TSS-based multitasking is used, while this is not possible for the GDT.
- The LDT also cannot store certain privileged types of memory segments.
- The LDT is the sibling of the Global Descriptor Table (GDT) and similarly defines up to 8191 memory segments accessible to programs.
- LDT (and GDT) entries which point to identical memory areas are called *aliases*.
- Instruction to load GDT is LGDT(Load Global Descriptor Table) and instruction to load LDT is LLDT(Load Global Descriptor Table). Both are privileged instructions.

#Write the Features of 80386 Microprocessor

Features of 80386 Microprocessor

- The 80386 microprocessor is an enhanced version of the 80286 microprocessor
- Memory-management unit is enhanced to provide memory paging.
- The 80386 also includes **32-bit** extended registers and a 32-bit address and data bus. These extended registers include ***EAX, EBX, ECX, EDX, EBP, ESP, EDI, ESI, EIP*** *and EFLAGS.*
- The 80386 has a physical memory size of 4GBytes that can be addressed as a virtual memory with up to **64TBytes.**
- The 80386 is operated in the pipelined mode, it sends the address of the next instruction or memory data to the memory system prior to completing the execution of the current instruction
- This allows the memory system to begin fetching the next instruction or data before the current is completed. This increases access time.
- The instruction set of the 80386 is enhanced to include instructions that address the **32-bit extended register set.**
- The 80386 memory manager is similar to the 80286, except the physical addresses generated by the MMU are **32 bits wide instead of 24-bits.**
- The concept of paging is introduced in 80386
- 80386 support three operating modes:
  - ✓ ***Real Mode(default)***
  - ✓ ***Protected Virtual Address Mode (PVAM)***
  - ✓ ***Virtual Mode***
- The memory management section of 80386 supports virtual memory, paging and four levels of protection.
- The 80386 includes special hardware for task switching

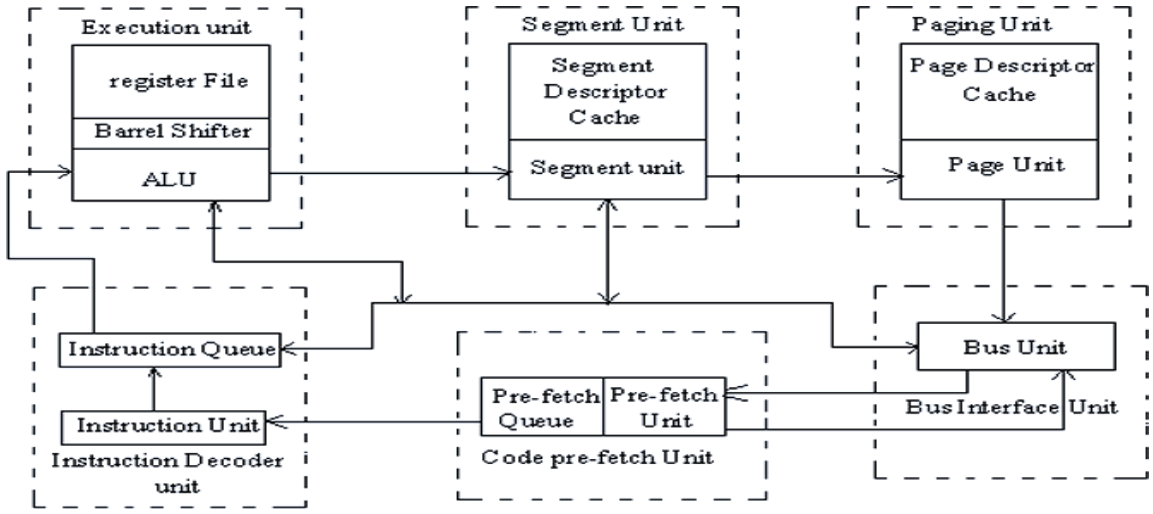
#Explain the architecture of the80386 with a neat block diagram.

- The internal architecture of the 80386 includes six functional units that operate in parallel. The parallel operation is called as pipeline processing.
- Fetching, decoding execution, memory management, and bus access for several instructions are performed simultaneously.

The six functional units of the 80386 are

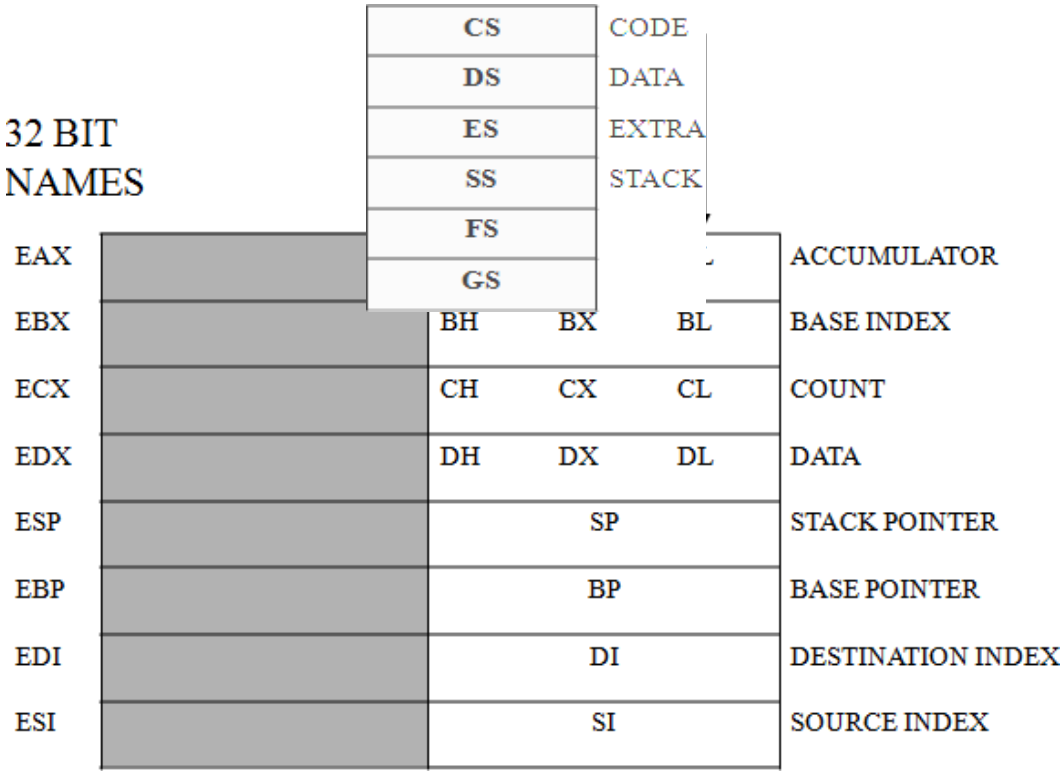
1.Bus Interface Unit
2.Code Pre-fetch Unit

3.Instruction Decoder Unit
4.Execution Unit
5.Segmentation Unit
6.Paging Unit



- The ***Bus Interface Unit*** connects the 80386 with memory and I/O. Based on internal requests for fetching instructions and transferring data from the code pre-fetch unit, the 80386 generates the address, data and control signals for the current bus cycles.
- The code pre-fetch unit pre-fetches instructions when the bus interface unit is not executing the bus cycles. It then stores them in a 16-byte instruction queue for decoding by the instructiondecode unit.
- The ***instruction decode unit*** translates instructions from the pre-fetch queue into micro-codes. The decoded instructions are then stored in an instruction queue (FIFO) for processing by the execution unit.
- The ***execution unit*** processes the instructions from the instruction queue. It contains a control unit, a data unit and a protection test unit.
- The ***control unit*** contains microcode and parallel hardware for fast multiply, divide and effective address calculation. The unit includes a 32-bit ALU, 8 general purpose registers and a 64-bit barrel shifter for performing multiple bit shifts in one clock. The data unit carries out data operations requested by the control unit.
- The ***protection test unit*** checks for segmentation violations under the control of microcode.
- The ***segmentation unit*** calculates and translates the logical address into linear addresses at the request of the execution unit.
- The translated linear address is sent to the paging unit. Upon enabling the paging mechanism, the 80386 translates these linear addresses into physical addresses. If paging is not enabled, the physical address is identical to the linear address and no translation is necessary.

#Explain Register organization of 80386



The Register organization of 80386 is as follows:

Figure:80386 General Purpose, Index and Pointer Register

General Purpose Register

- Registers EAX, EBX, ECX, EDX, EBP, EDI and ESI are regarded as general purpose or multipurposeregisters.

- EAX (ACCUMULATOR): The accumulator is used for instructions such as multiplication, division andsome of the adjustment instructions. In 80386 and above, the EAX register may also hold the offsetaddress of a location in memory system.
- EBX (BASE INDEX): This can hold the offset address of a location in the memory system in all version of the microprocessor. It the 80386 and above EBX also can address memory data.
- ECX (count): This acts as a counter for various instructions.
- EDX (data): EDX is a general-purpose registers that holds a part of the result for multiplication or part of the division. In the 80386 and above this register can also address memory data.

Pointer and Index Register

- ***EBP (Base Pointer):*** EBP points to a memory location in all version of the microprocessor for memory data transfers.
- ***ESP (Stack Pointer):*** ESP addresses an area of memory called the stack. The stack memory is a data LIFO data structure. The register is referred to as SP if used in 16 bit mode and ESP if referredto as a 32 bit register.
- ***EDI (Destination index):*** EDI often addresses string destination data for the string instruction. It also functions as either a 32-bit (EDI) or 16-bit (DI) general-purpose register.
- ***ESI (Source index):*** ESI can either be used as ESI or SI. It is often used to the address source

string data for the string instructions. Like EDI ESI also functions as a general-purpose registers.

80386 Segment Register

- **CS (Code):** The code segment is a section of memory that holds the code used by the microprocessor. The code segment registers defines the starting address of the section of memoryholding code.
- **SS (Stack):** The stack segment defines the area of memory used for the stack. The stack entry point is determined by the stack segment and stack pointer registers. The BP registers also addresses data within the stack segment.
- **DS (Data)** – The data section contains most data used by a program. Data are accessed in the data segment by an offset address of the contests of other registers that hold the offset address.
- **ES (extra)** – The extra segment is used to hold information about string transfer and manipulation
- **FS and GS** – These are supplement segment registers available in the 80386 and above microprocessors to allow two additional memory segments for access by programs.

EIP (Instruction Pointer):

EIP addresses the next instruction in a section of memory defined as a code segment. This register is IP (16bit) when microprocessor operates in the real mode and EIP (32 bits) when 80386 and above operate in protected mode

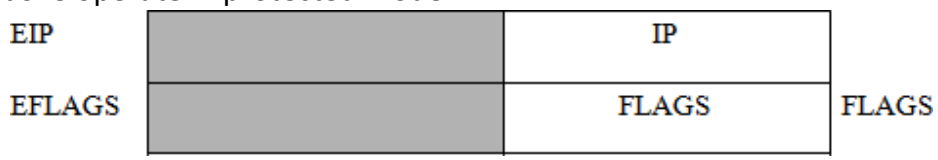


Figure:80386 Instruction Pointer and Flag Register

Flag Register:

Indicates the condition of the microprocessor and controls its operations. Flag registers are also upward compatible since the 8086-80268 have 16bit registers and the 80386 and above have EGLAF register (32 bits)

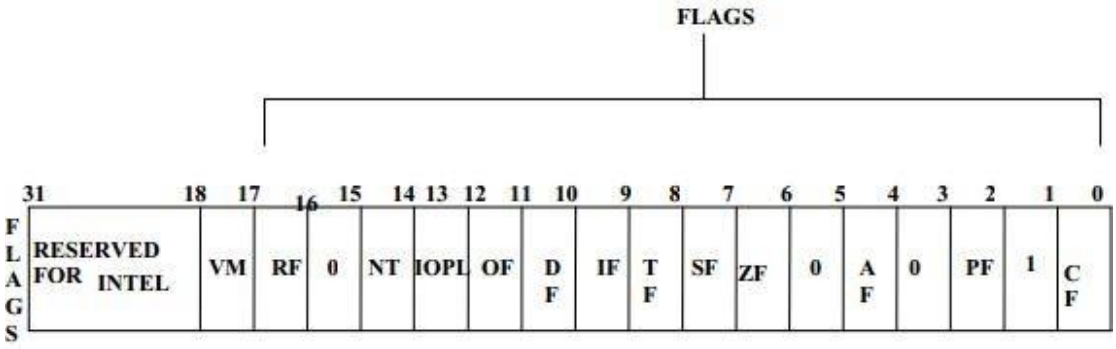


Figure: 80386 Flag Register

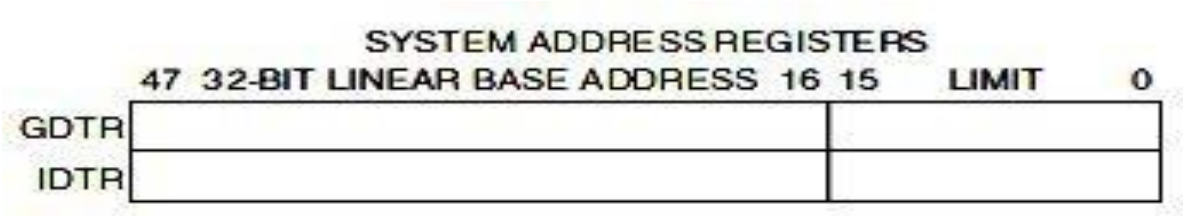
- **IOPL (I/O Privilege level):** IOPL is used in protected mode operation to select the privilege level for I./O devices. IF the current privilege level is higher or more trusted than the IOPL, I/O executedwithout hindrance. If the IOPL is lover than the current privilege level, an interrupt occurs, causingexecution to suspend. Note that

an IPOL is 00 is the highest or more trusted; if IOPL is 11, it's the lowest or least trusted.

- **NT (Nested Task):** The nested task flag is used to indicate that the current task is nested within another task in protected mode operation. This flag is when the task I nested by software.
- **RF (Resume):** The resume flag is used with debugging to control the resumption of execution after the next instruction.
- **VM (Virtual Mode):** The VM flag bit selects virtual mode operation in a protected mode system.
- Note: All the other flag bit is having similar description as in 8086 flag register.

System Address Register:

Four memory management registers are used to specify the locations of data structures which control segmented memory management.



- GDTR (Global Descriptor Table Register) and IDTR (Interrupt Descriptor Table Register) be loadedwith instructions which get a **6 byte** data item from memory

  -LDTR (Local Descriptor Table Register) and TR (Task Register) can be loaded with instructions whichtake a 16-bit **segment selector** as an operand.

Special 80386 Register

- Control Register: Four Control Register (CR0-CR3)
- Debug Register: Eight Debug Register (DR0-DR7)
- Test Register: Two Test Register (TR6-TR7)

#Explain the concept of paging in 80386 Microprocessor

Paging Operation: Paging is one of the memory management techniques used for virtual memory multitasking operating

•The segmentation scheme may divide the physical memory into a variable size segments but the paging divides the memory into a fixed size pages.

•The segments are supposed to be the logical segments of the program, but the pages do not have any logical relation with the program.

•The pages are just fixed size portions of the program module or data. system.

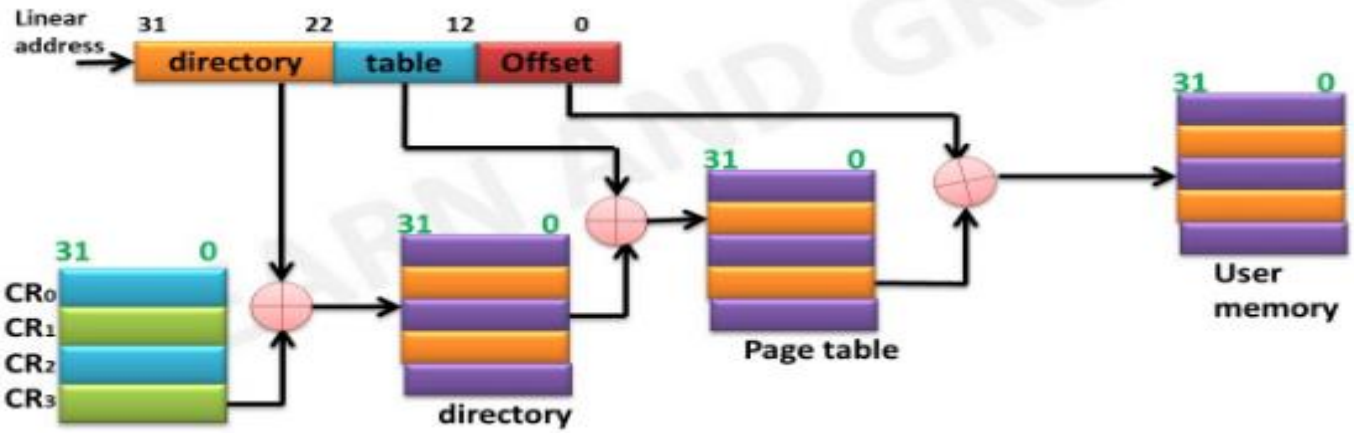
The advantage of paging scheme is that the complete segment of a task need not be in the physical memory at any time.

•Only a few pages of the segments, which are required currently for the execution need to be available in the physical memory. Thus the memory requirement of the task is substantially reduced, relinquishing the available memory for other tasks.

•Whenever the other pages of task are required for execution, they may be fetched from the secondary storage.

•The previous page which are executed, need not be available in the memory, and hence the space occupied by them may be relinquished for other tasks.

Thus paging mechanism provides an effective technique to manage the physical memory for multitasking systems.



Paging Unit:

The paging unit of 80386 uses a two level table mechanism to convert a linear address provided by segmentation unit into physical addresses. The paging unit converts the complete map of a task into pages, each of size 4K. The task is further handled in terms of its page, rather than segments. The paging unit handles every task in terms of three components namely page directory, page tables and page itself.

Paging Descriptor Base Register:

The control register CR2 is used to store the 32-bit linear address at which the previous page fault was detected. The CR3 is used as page directory physical base address register, to store the physical starting address of the page directory. The lower 12 bit of the CR3 are always zero to ensure the page size aligned directory. A move operation to CR3 automatically loads the page table entry caches and a task switch operation, to load CR0 suitably.

Page Directory :

This is at the most 4Kbytes in size. Each directory entry is of 4 bytes,thus a total of 1024 entries are allowed in a directory. The upper 10 bits of the linear address are used as an index to the corresponding page directory entry. The page directory entries point to page tables.

•Page Tables:

Each page table is of 4Kbytes in size and many contain a maximum of 1024 entries. The page table entries contain the starting address of the page and the statistical information about the page. •The upper 20 bit page frame address is combined with the lower 12 bit of the linear address. The address bits A12- A21 are used to select the 1024 page table entries. The page table can be shared between the tasks.

- The P bit of the above entries indicate, if the entry can be used in address translation.
- If P=1, the entry can be used in address translation, otherwise it cannot be used.
- The P bit of the currently executed page is always high.
- The accessed bit A is set by 80386 before any access to the page. If A=1, the page is accessed, else unaccessed.
- The D bit (Dirty bit) is set before a write operation to the page is carried out. The D-bit is undefined for page director entries.
- The OS reserved bits are defined by the operating system software.
- The User / Supervisor (U/S) bit and read/write bit are used to provide protection. These bits are decoded to provide protection under the 4 level protection model.
- The level 0 is supposed to have the highest privilege, while the level 3 is supposed to have the least privilege.
- This protection provide by the paging unit is transparent to the segmentation unit.

Exam Questions:

- ***Explain the architecture of the80386 with a neat block diagram.***
- Explain Register organization of 80386 microprocessor
- ***Explain the architecture of the80386 with a neat block diagram***
- Explain the concept of paging in 80386 Microprocessor

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