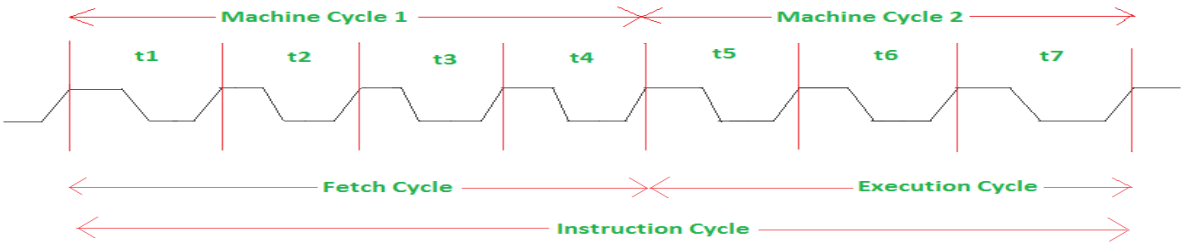
Unit-3

Instruction cycle

Time required to execute and fetch an entire instruction is called ***instruction cycle.*** It consists:

- **Fetch cycle –** The next instruction is fetched by the address stored in program counter (PC) and then stored in the instruction register.
- **Decode instruction –** Decoder interprets the encoded instruction from instruction register.
- **Reading effective address –** The address given in instruction is read from main memory and required data is fetched. The effective address depends on direct addressing mode or indirect addressing mode.
- **Execution cycle –** consists memory read (MR), memory write (MW), input output read (IOR) and input output write (IOW)



Instruction cycle in 8085 microprocessor

The time required by the microprocessor to complete an operation of accessing memory or input/output devices is called ***machine cycle.*** One time period of frequency of microprocessor is called **t-state.** A t-state is measured from the falling edge of one clock pulse to the falling edge of the next clock pulse. Fetch cycle takes four t-states and execution cycle takes three t-states.

Note:

Instruction Cycle: The time required to execute an instruction is called instruction cycle.

Machine Cycle: The time required to access the memory or input/output devices is called machine cycle.

T-State: The machine cycle and instruction cycle takes multiple clock periods. A portion of an operation carried out in one system clock period is called as T-state.

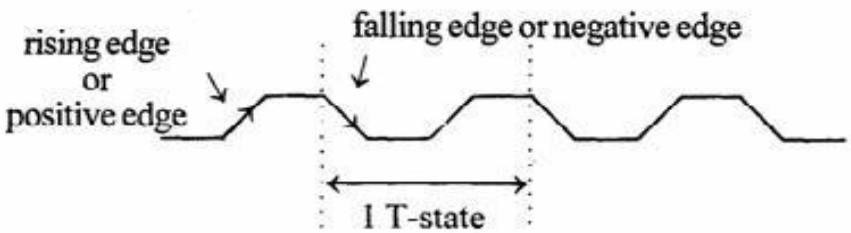
MACHINE CYCLES OF 8085:

The 8085 microprocessor has 5 (Five) basic machine cycles. They are

1. Op-code fetch cycle (4T)
2. Memory read cycle (3 T)
3. Memory write cycle (3 T)
4. I/O read cycle (3 T)
5. I/O write cycle (3 T)

- Each instruction of the 8085 processor consists of one to five machine cycles, i.e., when the 8085 processor executes an instruction, it will execute some of the machine cycles in a specific order.
- The processor takes a definite time to execute the machine cycles. The time taken by the processor to execute a machine cycle is expressed in T-states.
- One T-state is equal to the time period of the internal clock signal of the processor.
- The T-state starts at the falling edge of a clock.

Note : Time period, T = 1/f ; where f = Internal clock frequency



Timing Diagram of 8085 Microprocessor

Timing Diagram is a graphical representation. It represents the execution time taken by each instruction in a graphical format. The execution time is represented in T-states

Point to remember while making timing diagram.

- **CLK (OUT)** : It is the 37th pin of the 8085 IC and acts as the system clock that keeps the record of time duration required by each operation to get completed.

- ***A_8 to A_{15}*** :The address bus is a group of sixteen lines i.e A0-A15. The address bus is unidirectional, i.e., bits flow in one direction from the microprocessor unit to the peripheral devices and uses the high order address bus.

- ***AD_0 to AD_7***: The address bus is denoted by A whereas the data bus is denoted by D. The pin configuration denotes the lower order multiplexed address and data bus bits from ***AD_0 to AD_7***.

Control and Status Signals:

- ALE – It is an Address Latch Enable signal. It goes high during first T state of a machine cycle and enables the lower 8-bits of the address, if its value is 1 otherwise data bus is activated.
- IO/M' – It is a status signal which determines whether the address is for input-output or memory. When it is high(1) the address on the address bus is for input-output devices. When it is low(0) the address on the address bus is for the memory.
- SO, S1 – These are status signals. They distinguish the various types of operations such as halt, reading, instruction fetching or writing.

- RD' – It is a signal to control READ operation. When it is low the selected memory or input-output device is read.
- WR' – It is a signal to control WRITE operation. When it goes low the data on the data bus is written into the selected memory or I/O location.

Operations	$IO/\overline{M}$	S_0	S_1
Opcode Fetch	0	1	1
Memory Read	0	1	0
Memory Write	0	0	1
I/O Read	1	1	0
I/O Write	1	0	1
Interrupt Ack.	1	1	1

Opcode fetch machine cycle of 8085:

- Each instruction of the processor has one byte opcode.
- The opcode are store in memory. So the processor executes the opcode fetch machine cycle to fetch the opcode from memory.
- Hence, every instruction starts with opcode fetch machine cycle.
  - The time taken by the processor to execute the opcode fetch cycle is 4T.
  - In this time, the first, 3 T-states are used for fetching the opcode from memory and the remaining T-states are used for internal operations by the processor.

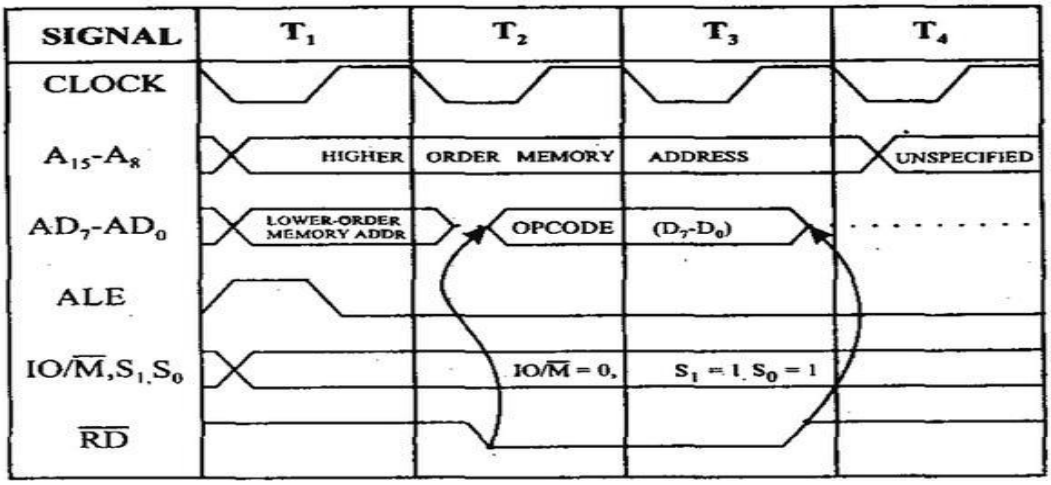


Fig - Timing Diagram for Opcode Fetch Machine Cycle

2. Memory read cycle (3 T)

- The memory read machine cycle is executed by the processor to read a data byte from memory.
- The processor takes 3T states to execute this cycle.
- The instructions which have more than one byte word size will use the machine cycle after the opcode fetch machine cycle

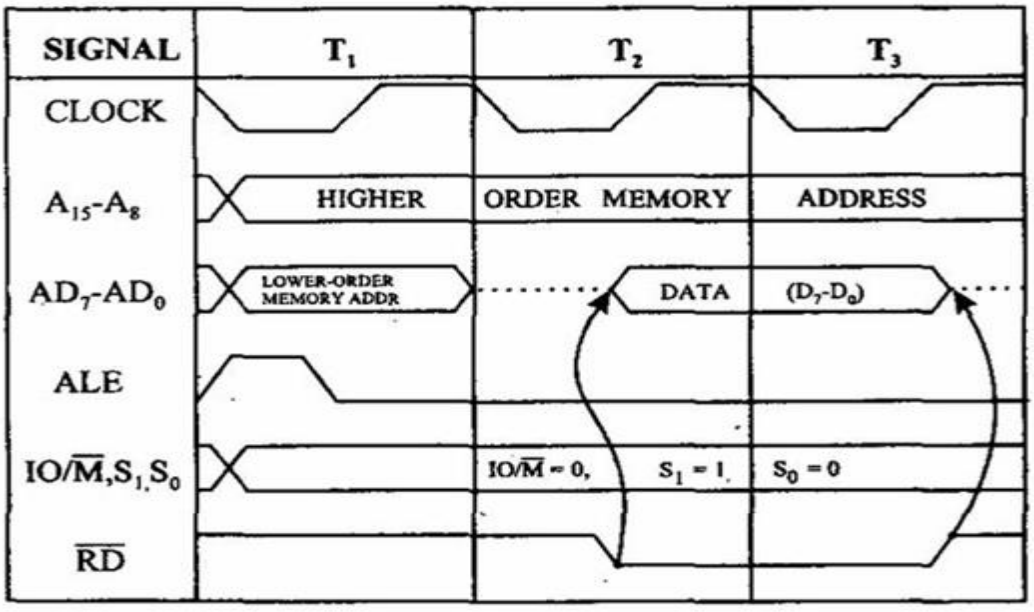
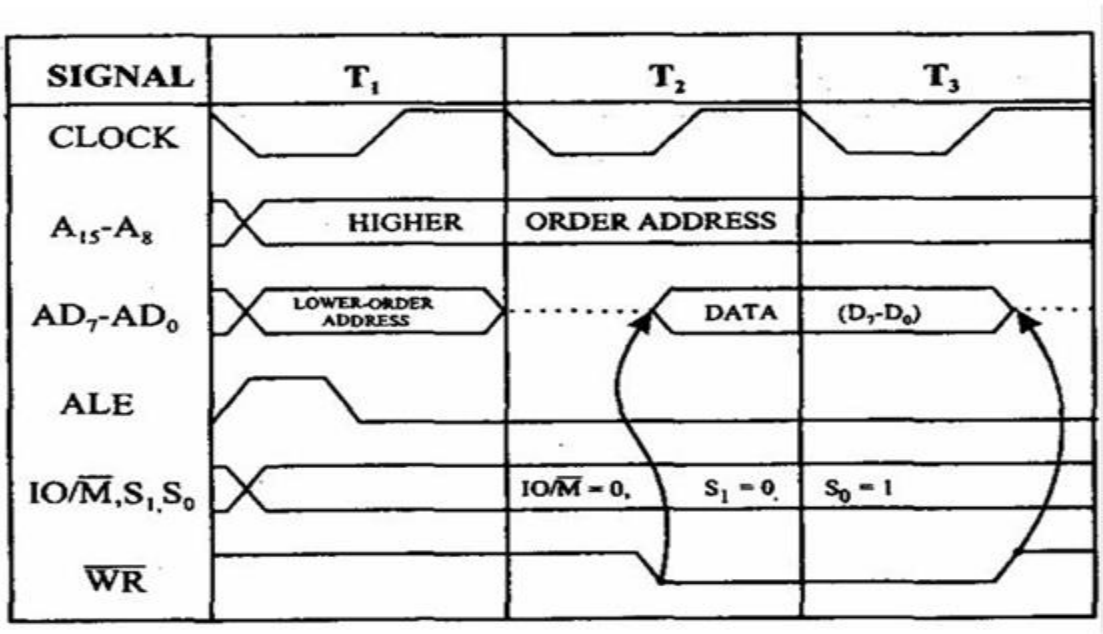


Fig - Timing Diagram for Memory Read Machine Cycle

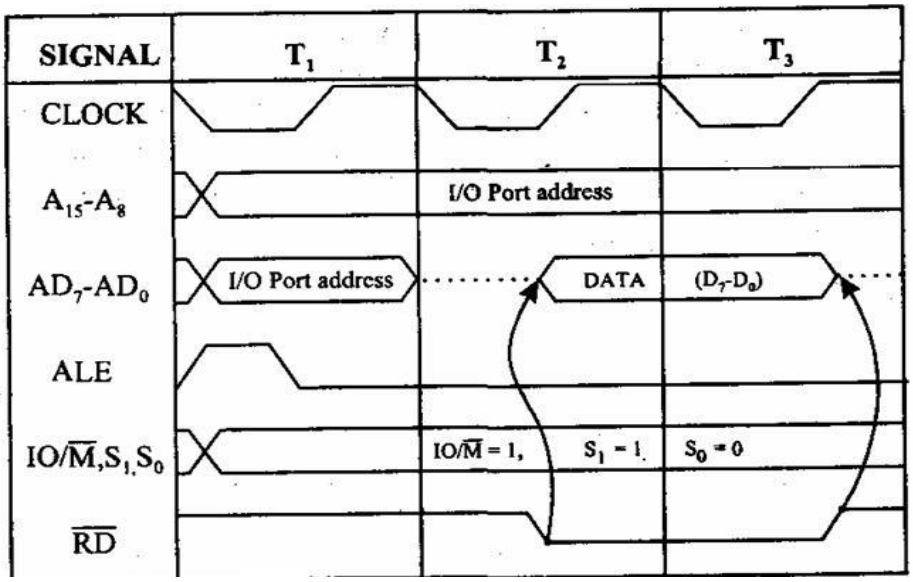
Memory Write Machine Cycle of 8085:

- The memory write machine cycle is executed by the processor to write a data byte in a memory location.
- The processor takes,3T states to execute this machine cycle.



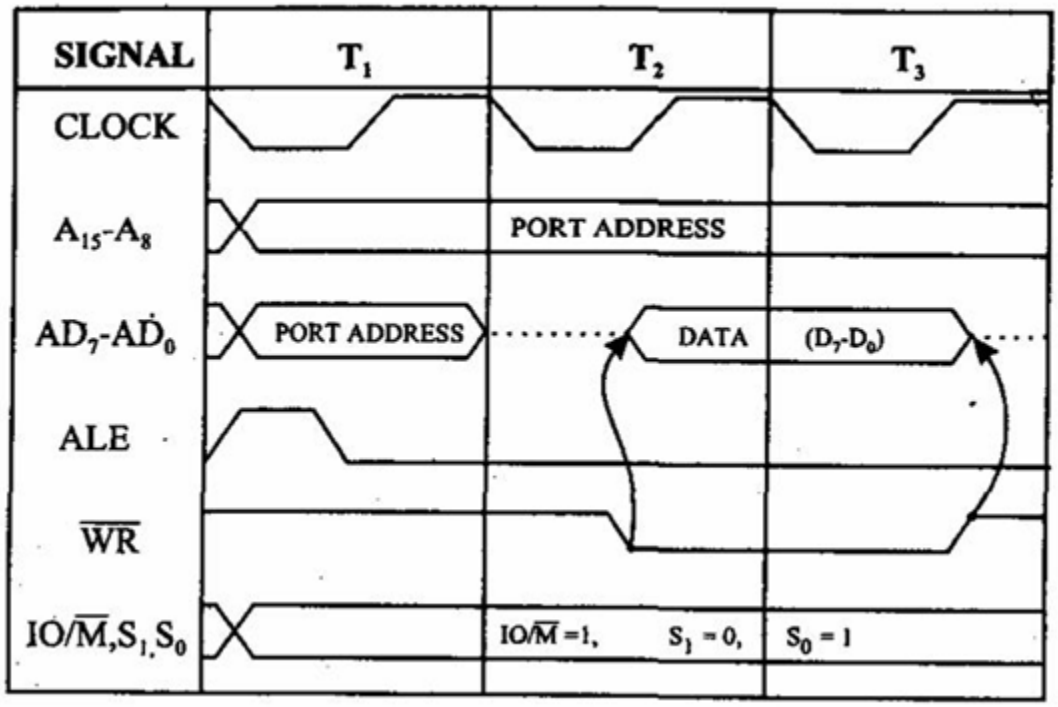
I/O Read Cycle of 8085:

- The I/O Read cycle is executed by the processor to read a data byte from I/O port or from the peripheral, which is I/O, mapped in the system.
- The processor takes 3T states to execute this machine cycle.
- The **IN** instruction uses this machine cycle during the execution



I/O write cycle (3 T)

- The I/O write machine cycle is executed by the processor to write a data byte in the I/O port or to a peripheral, which is I/O, mapped in the system
- The processor takes, 3T states to execute this machine cycle



Timing Diagram of MOV, MVI, IN, OUT, LDA, STA

i)MOV

E.g. MOV A,B

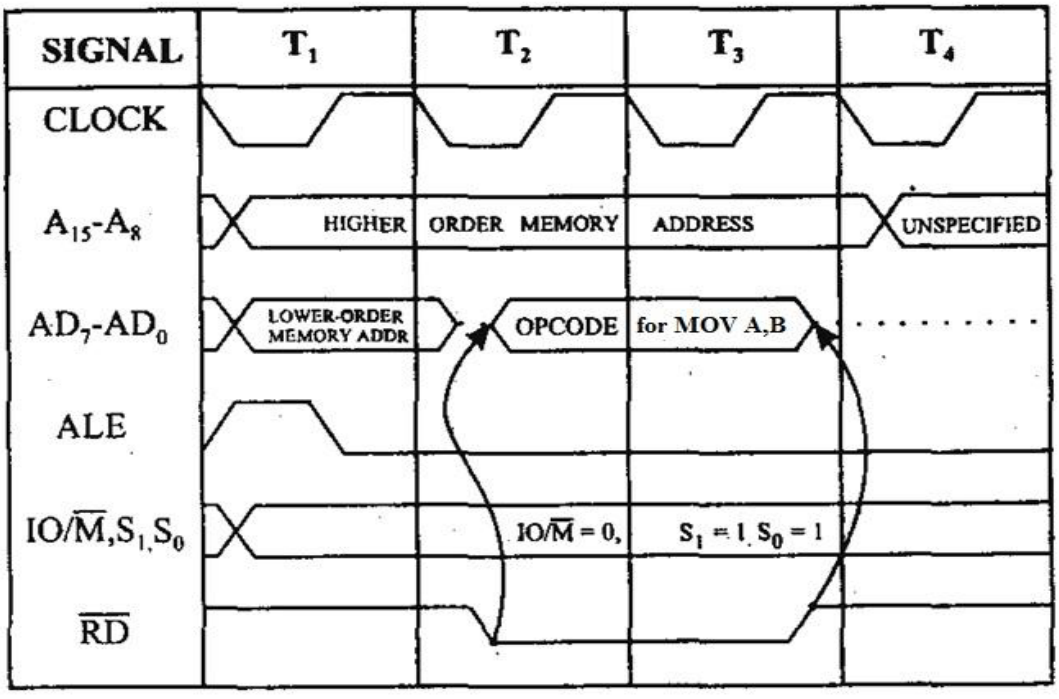
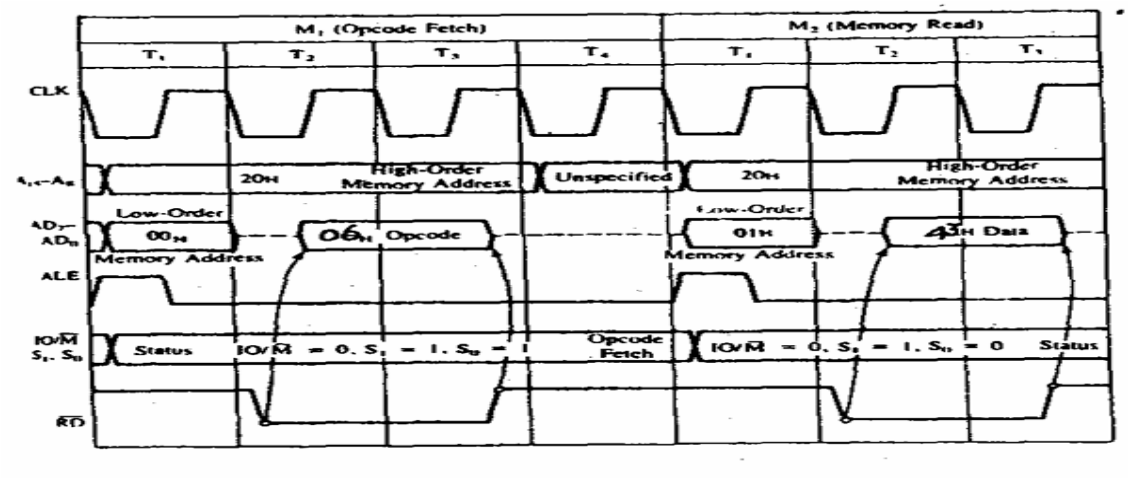


Fig: Timing Diagram for MOV A,B

ii) Timing diagram for MVI B, 43H.

Address	Mnemonics	Opcode
2000	MVI B, 43_H	06_H
2001		43_H

- Fetching the Opcode 06H from the memory 2000H. (OF machine cycle)
- Read (move) the data 43H from memory 2001H. (memory read)



- Fig: Timing Diagram for MVI B, 43H

IN Timing diagram for IN C0H

- Fetching the Op-code DBH from the memory 4125H.
- Read the port address C0H from 4126H.
- Read the content of port C0H and send it to the accumulator.
- Let the content of port is 5EH

Address	Mnemonics	Opcode
4125	IN $C0_H$	DB_H
4126		$C0_H$

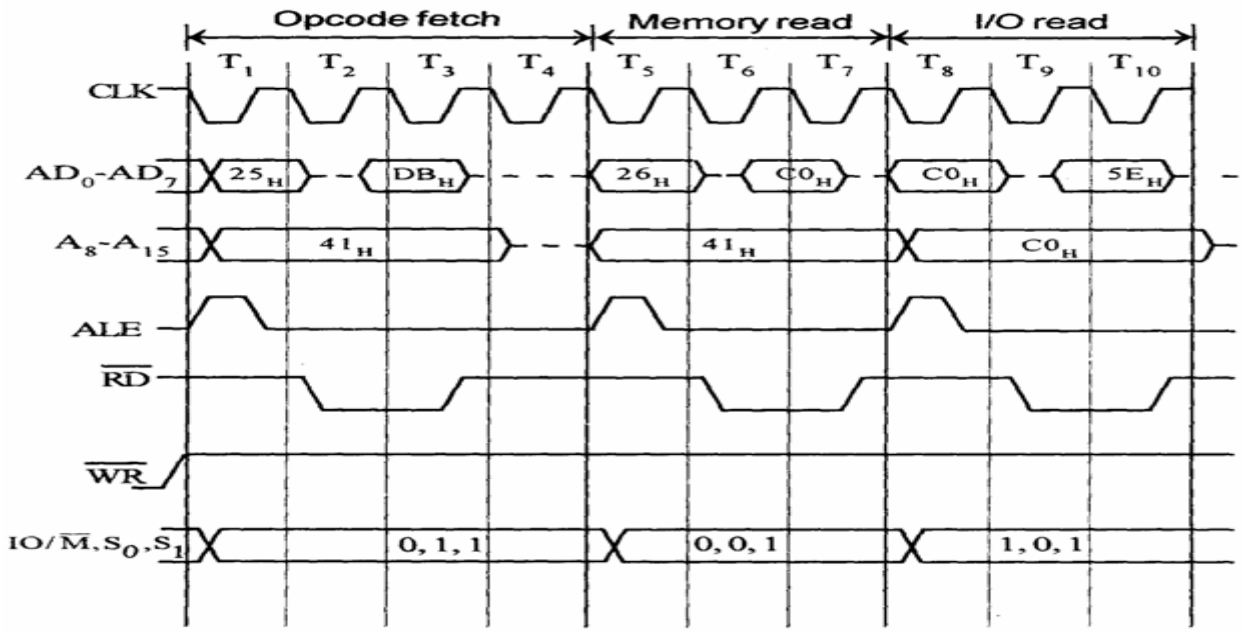


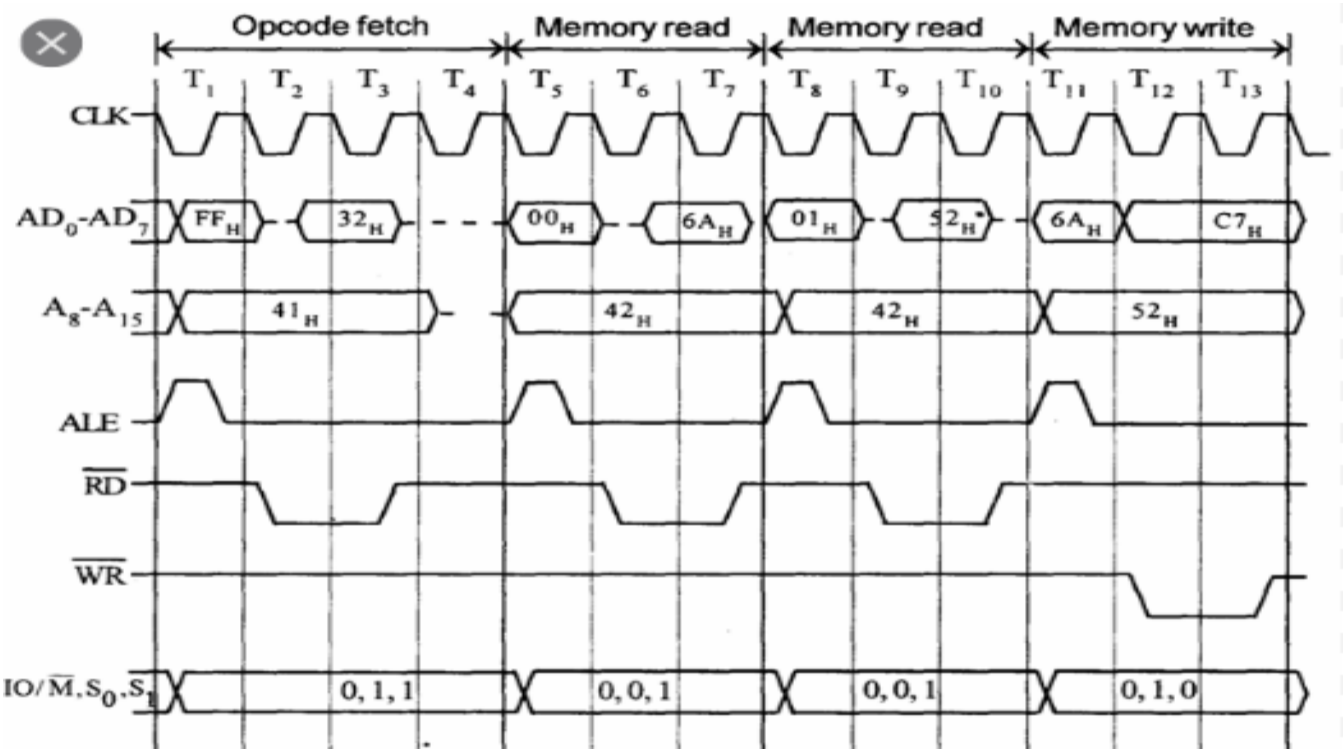
Fig: Timing Diagram for IN C0H

Timing diagram for STA 526AH

Step to solve

- STA means Store Accumulator -The contents of the accumulator is stored in the specified address (526A).
- The Opcode of the STA instruction is said to be 32H. It is fetched from the memory 41FFH (see fig). - *OF machine cycle*
- Then the lower order memory address is read(6A). – *Memory R*
- Read the higher order memory address (52).- *Memory Read Machine Cycle.*
- The combinations of both the addresses are considered and the content from accumulator is written in 526A. – *Memory Write Machine Cycle*
- Assume the memory address for the instruction and let the content of accumulator is C7H. So, C7H from accumulator is now stored in 526A

Address	Mnemonics	Opcode
41FF	STA 526A$_H$	32$_H$
4200		6A$_H$
4201		52$_H$



Memory Interfacing and generation of chip select signal

A microprocessor has to be interfaced with various peripherals to perform various functions. Let's discuss about the Interfacing techniques in detail.

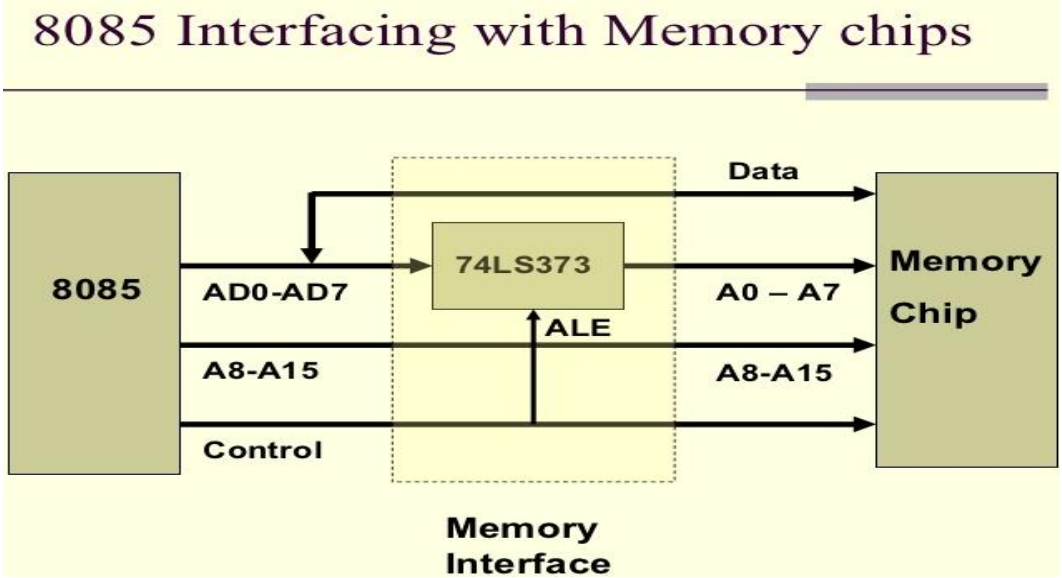
- We know that a microprocessor is the CPU of a computer.
- A microprocessor can perform some operation on a data and give the output. But to perform the operation we need an input to enter the data and an output to display the results of the operation.

Interfacing Types

There are two types of interfacing in context of the 8085 processor.

(a) Memory Interfacing.

(b) I/O Interfacing.



1. Microprocessor 8085 can access 64Kbytes memory since address bus is 16-bit. But it is not always necessary to use full 64Kbytes address space. The total memory size depends upon the application.
2. Generally EPROM (or EPROMs) is used as a program memory and RAM (or RAMs) as a data memory. When both, EPROM and RAM are used, the total address space 64Kbytes is shared by them.
3. The capacity of program memory and data memory depends on the application.
4. It is not always necessary to select 1 EPROM and 1 RAM. We can have multiple EPROMs and multiple RAMs as per the requirement of application.
5. We can place EPROM/RAM anywhere in full 64 Kbytes address space. But program memory (EPROM) should be located from address 0000H since reset address of 8085 microprocessor is 0000H.
6. It is not always necessary to locate EPROM and RAM in consecutive memory ***For example:*** If the mapping of EPROM is from 0000H to OFFFH, it is not must to locate RAM from 1000H. We can locate it anywhere between 1000H and FFFFH. Where to locate memory component totally depends on the application.

The memory interfacing requires to:

- **Select the chip**
- **Identify the register**
- **Enable the appropriate buffer.**

Microprocessor system includes memory devices and I/O devices. It is important to note that microprocessor can communicate (read/write) with only one device at a time, since the data, address and control buses are common for all the devices. In order to communicate with memory or I/O devices, it is necessary to decode the address from the microprocessor. Due to this each device (memory or I/O) can be accessed independently.

Control Signals of 8085

The 8085 Microprocessor provides RD and WR signals to initiate read or write cycle. Because these Control Signals of 8085 are used both for reading/writing memory and for reading/writing an input device, it is necessary to generate separate read and write signals for memory and I/O devices.

The 8085 provides IO/M signal to indicate whether the initiated cycle is for I/O device or for memory device. Using IO/M signal along with RD and WR, it is possible to generate separate four Control Signals of 8085.

$\overline{\text{MEMR}}$	(Memory Read)	: To read data from memory.
$\overline{\text{MEMW}}$	(Memory Write)	: To write data in memory.
$\overline{\text{IOR}}$	(I/O Read)	: To read data from I/O device.
$\overline{\text{IOW}}$	(I/O Write)	: To write data in I/O device.

Exam Questions:

- ***Define Instruction Cycle, Machine Cycle and T-state and draw the timing diagram of Opcode fetch cycle.***
- ***Draw the timing diagram of MVI A, 32H and explain it.***
- ***Draw the timing diagram of STA 526 AH and explain its.***
- ***Draw the timing diagram of MOV A,B and explain its.***

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