Distributed I/O Tier
system specification

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Revision table

Date	Version	Comments
2018-12-20	First draft	First draft released for comments
2019-02-28	2nd draft	Including input from Creotech
2019-03-29	3rd draft	Including monitoring-related backplane connectors
2019-04-11	4th draft	Including input from CERN Eq groups
2019-05-06	1.0 release	Ready for crate mechanics & backplane design
2020-07-XX	2.0 release	Completed crate design

1 Introduction

Controls and data acquisition systems in accelerators often involve a computing platform (VME, PICMG 1.3, MTCA.4...) connected to Distributed I/O Tier electronics using a fieldbus communication link (Figure 1). The devices in the Distributed I/O Tier communicate directly with various sensors and actuators and are deployed close to the machine. Since these areas are frequently exposed to radiation and because of the very specific needs of CERN systems, these modules not being commercially available, are usually custom in-house developments. Currently, we are missing a centrally supported service at CERN for the custom electronics in this layer.
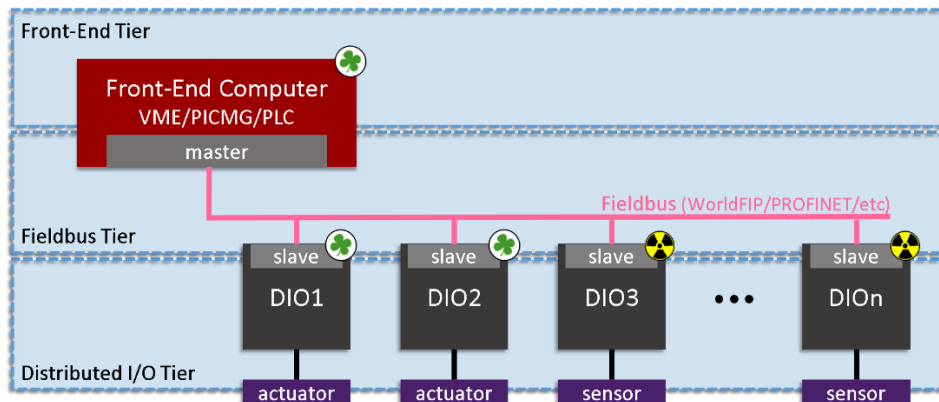

Figure 1: Three lowest hardware layers of a typical control system

The Distributed I/O Tier project aims at offering a new, modular and reusable hardware kit for various renovations and new systems to be deployed for the High Luminosity LHC (HL-LHC) in 2025. The kit to cover the requirements of the equipment groups in both radiation-exposed and radiation-free areas will consist of the following components (Figure 2):
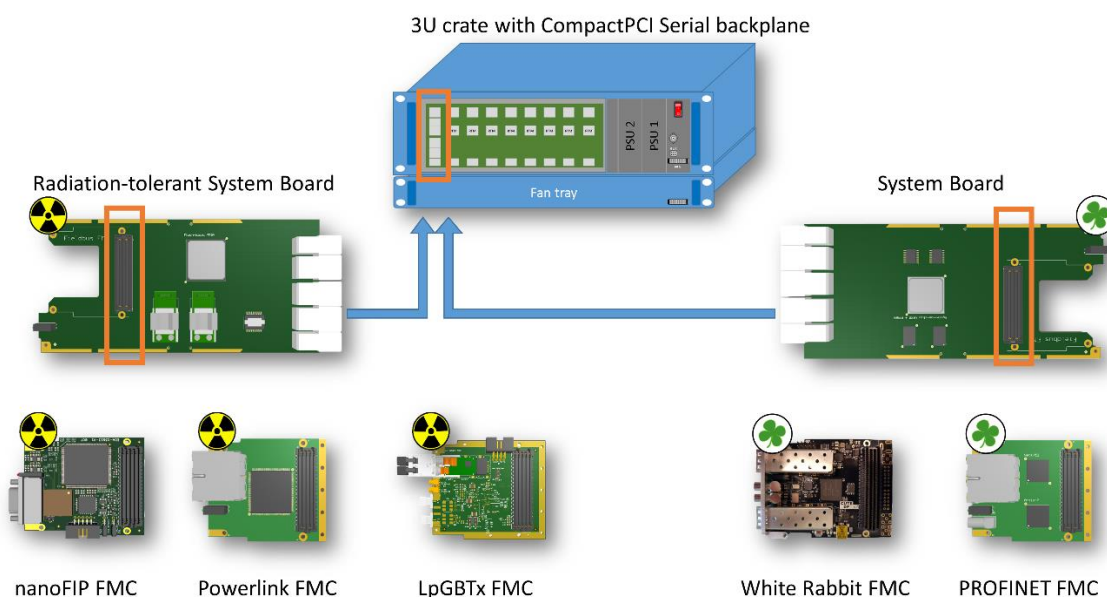

Figure 2: Distributed I/O Tier modular and reusable hardware kit

- A **low-cost CompactPCI Serial chassis** with a backplane, redundant power supplies (either off-the-shelf or radiation-tolerant in-house designed) and an optional fan tray.
- Two generic **FPGA-based System Boards** (radiation-tolerant and non-radiation-tolerant) that interface with the application-specific peripheral boards plugged into the other slots of the 3U crate. Each System Board features a high-performance FPGA for the application-specific logic. A small fraction of the FPGA resources is dedicated to standardised crate diagnostics. The System Boards have an LPC FMC slot, where a fieldbus slave mezzanine is plugged to provide communication with a master and the higher layers of the control system.
- A set of interchangeable, radiation-tolerant and non-radiation-tolerant **fieldbus communication mezzanines** in the FMC format that implement various communication standards: WorldFIP, Powerlink, LpGBTx, White Rabbit or PROFINET.

This document specifies the Distributed I/O Tier chassis, its components that are common to all equipment groups as well as the customization options to adapt it to specific needs of a particular use case.

2 Main 3U crate backplane

There are two options foreseen for the backplane of a Distributed I/O Tier crate. The general recommendation is to use a common CompactPCI Serial backplane (section 2.1). CompactPCI Serial was selected among many industrial modular electronics standards because it features a fully passive backplane and a robust connector targeting transportation applications. Being fully passive, and providing a set of connections in star topology (Figure 3) the backplane enables the use of its lines as a set of single-ended or differential lanes for simple communication mechanisms like fast SPI or even direct I/O connections. The DI/OT crate does not make use of the CompactPCI Serial high-speed interconnects (PCIe/SATA/USB) specification, as it would be too complex for the radiation-exposed systems.

By selecting this default and standard approach for DI/OT crate, peripheral boards designed by a specific equipment group can be reused also by other groups. However, in case a particular application cannot benefit from the common CompactPCI Serial backplane (section 2.1), one can also design a custom application-specific backplane preserving some common characteristics with the common backplane (section 9.1).
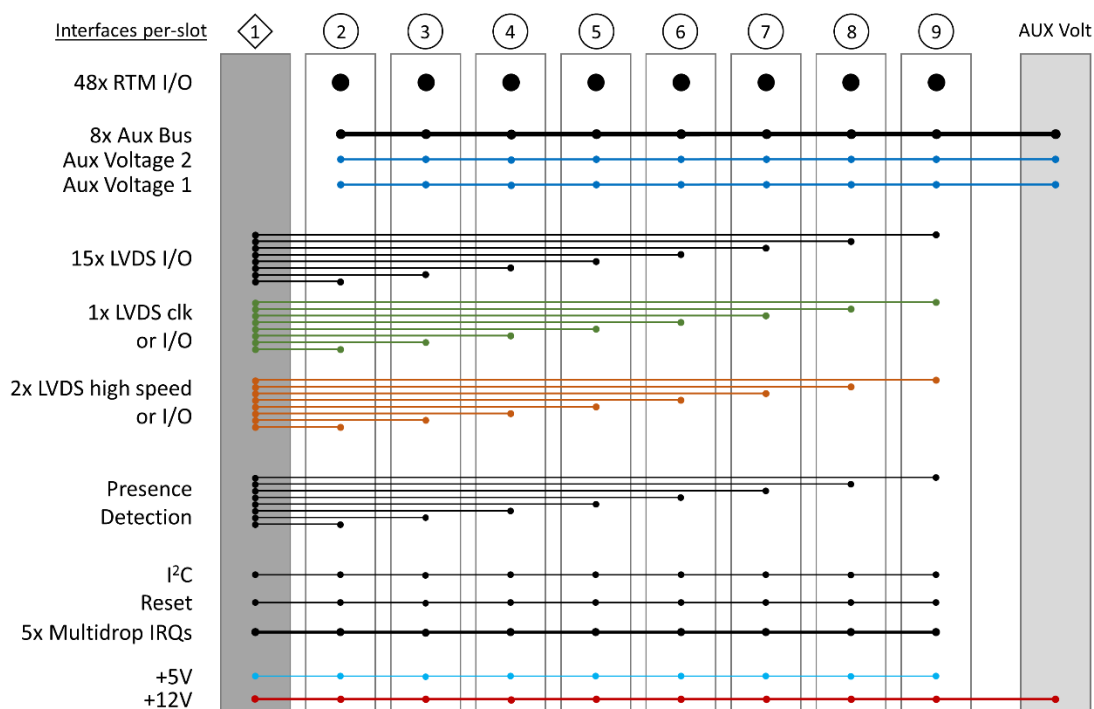

Figure 3: Common backplane connections topology (1 - System Slot; 2-9 - Peripheral Slots)

2.1 Common CompactPCI Serial backplane

<u>Development by:</u> BE-CO and external company
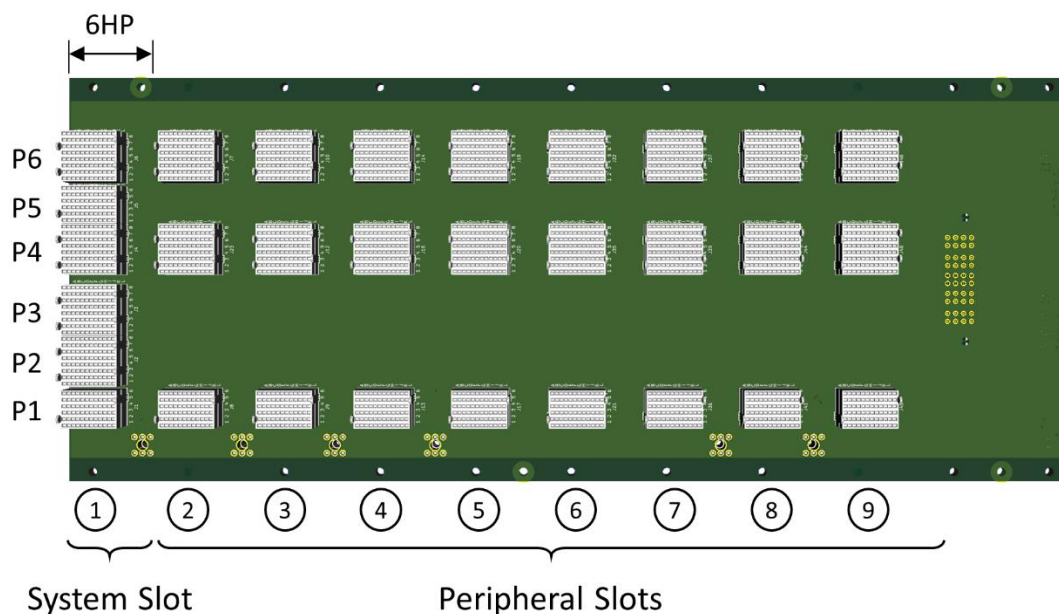
Figure 4: Common CompactPCI Serial DI/OT backplane (front view)
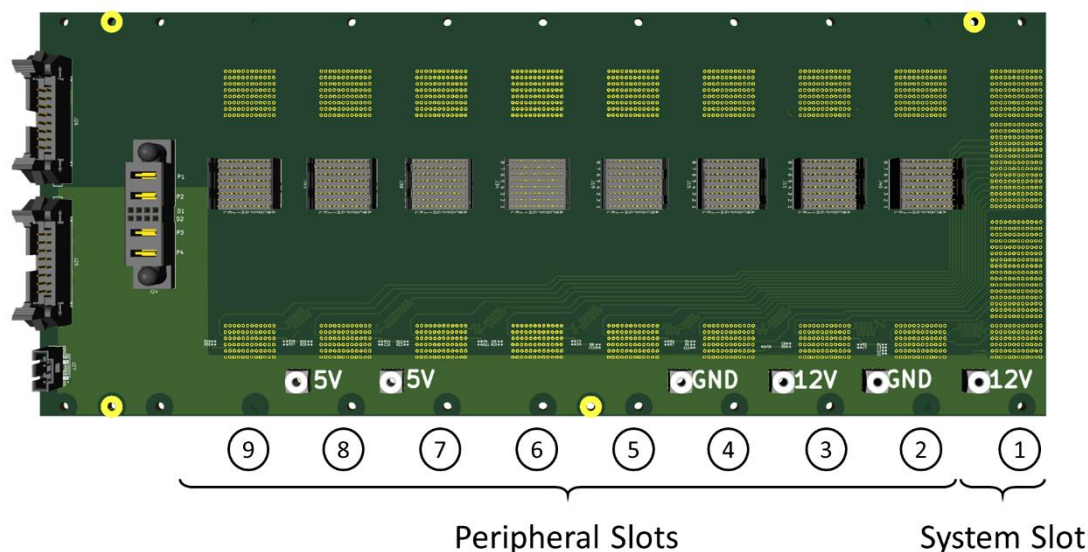
Figure 5: Common CompactPCI Serial DI/OT backplane (back view)

The backplane shall be designed and manufactured according to the CompactPCI Serial specification PICMG CPCI-S.0 [1], taking into account the following characteristics:

2.1.1   The backplane shall have 9 slots – 1 System Slot and 8 Peripheral Slots. The System Slot hosts one of the generic FPGA-based System Boards (radiation-tolerant or non-radiation-tolerant variant as described in section 1) while 8 Peripheral Slots host application-specific boards designed by equipment groups for the needs of their systems.

2.1.2   The System Slot shall be placed on the left side of the backplane.

2.1.3   The System Slot shall have a width of 6HP (Horizontal Pitch) i.e. 30.48mm. All Peripheral Slots shall have a width of 6HP.

2.1.4   All Peripheral Slots shall be populated with P1 (72-pin), P4 (96-pin) and P6 (96-pin) Airmax connectors. P1 provides power and differential pairs for communication between Peripheral Slots and the System Slot. P6 provides additional differential pairs for communication with the System Slot. P4 RTM (Rear Transition Module) connector provides additional connectivity with optional rear modules and the rest of the Peripheral Boards.
Note: Tx and Rx lanes for CPCI-S PCIe, USB3.0, SATA, Ethernet interfaces are crossed in the backplane.

2.1.5   CPCI-S.0 [1] standard allows two connection topologies of differential pairs available in P6 connectors of the System Slot and all Peripheral Slots (mesh or single star). The DI/OT backplane shall use a single star topology between the System Slot and 8 Peripheral Slots.

2.1.6   To lower the cost of the backplane, only 16 differential pairs going from the System Slot to the P1 of 8 Peripheral Slots (2 differential pairs per Peripheral Slot) are foreseen to handle high-speed communication (e.g. using MGT FPGA transceivers). Lanes n_PE_Tx00, n_PE_Rx00 (where n is a slot number 1..8) in Table 44 and Table 45 of the CPCI-S.0 standard [1] shall be used for this purpose and routed accordingly to ensure signal integrity, controlled differential impedance 100Ω and length matching with 5mm tolerance.
Note: The actual use of these lanes depends on the System Board design. E.g. in radiation–exposed areas, these high-speed lanes can be used for low-speed communication.

2.1.7   The 8 differential pairs (one per Peripheral Slot) going from the System Slot to the 8 Peripheral Slots ($n\_PE\_CLK+/-$ in rows 5 and 6 of the System Slot connector P5 according to CPCI-S.0 standard [1]) shall provide low-noise distribution of high quality clocks to each of the Peripheral Boards.
Note: The actual use of these lanes depends on the System Board design. E.g. in radiation–exposed areas, these clock distribution lanes can be used for low-speed communication.

2.1.8   The remaining 120 differential pairs (15 pairs per Peripheral Slot) going from the System Slot to 8 Peripheral Slots will be used as low-speed communication (e.g. SPI links) or user-defined I/Os. Therefore their routing constraints can be relaxed to reduce the cost of the backplane (they will not carry Gbps transfer rates from gigabit FPGA transceivers and they will not be length-matched).

2.1.9   All differential pairs going to a particular Peripheral Slot shall be length matched with 5mm tolerance.

2.1.10   Geographical addressing signals (GA0-3) shall be grounded/open for each slot as defined in CPCI-S.0 standard [1].

2.1.11   All backplane signals not mentioned in this section (+12V, +5V, GND, general purpose multi-drop lines, PSU control signals, reset) shall be routed as specified in the CPCI-S.0 standard [1].

2.1.12   *PWRBTN#* and *PRST#* lines defined in CPCI-S.0 standard in the System Slot P1 connector shall be routed to *AUX* IDC connector (Figure 5) in the back of the backplane (full pinout in Table 4).
Note: These single-ended lines will be connected to the FPGA on the System Board, so their functionality can be programmed by the user depending on final application (e.g. to expose UART interface in the front panel).

2.1.13   The 11 signals of a System Slot P2 connector that are defined as "general purpose I/O" (in Table 44 and Table 45 of PICMG CPCI-S.0 [1]), shall be connected to a set of IDC-type connectors (*Utility(PSU)*, *FAN TRAY* in Figure 5) in the back of the backplane. These lines will be used for wiring

of the components required by crate diagnostics and monitoring (e.g. PMBus for PSU and fan tray monitoring).

2.1.14   The IDC-type connectors (*Utility(PSU)*, *FAN TRAY*, *AUX*) shall be equipped with latches to prevent lose contacts, keying to prevent improper insertion (Amphenol 53611-G16-8LF for *Utility* and *FANTRAY*; Molex 1719730004 for *AUX*) and be placed on the left side of the backplane (looking from the back, Figure 5) to allow the use of short ribbon cables to connect to power backplanes and front panel connector.

2.1.15   The pin assignment of the 11 "general purpose I/O" of the System Slot P2 (in Table 44 and Table 45 of CPCI-S.0 [1]) and their wiring to the IDC connectors shall be done according to Table 1.

IO pin	Name	IDC conn	IO pin	Name	IDC conn
P2-07A	*M_SCL*	*Utility(PSU), FANTRAY*	P2-07B	*M_SDA*	*Utility(PSU), FANTRAY*
P2-08B	*P_RST*	*Utility(PSU)*	P2-08C	*P_IO0*	*Utility(PSU)*
P2-07D	*P_IO1*	*Utility(PSU)*	P2-07E	*P_IO2*	*Utility(PSU)*
P2-07G	*P_PRES0*	*Utility(PSU)*	P2-07H	*P_PRES1*	*Utility(PSU)*
P2-07J	*F_RST*	*FANTRAY*	P2-07K	*F_IO0*	*FANTRAY*
P2-08J	*F_IO1*	*FANTRAY*	--	--	--

Table 1: System Slot "general purpose I/O" assignment

2.1.16   The full pinout of IDC connectors (*Utility*, *FANTRAY*, *AUX*) shall be done according to Table 2, Table 3 and Table 4.

2.1.17   The I^{2}C bus that is shared among all the backplane slots (backplane pins *IC_SCL, IC_SDA*) shall <u>not</u> be wired to the *Utility(PSU)* connector as defined by the CPCI-S.0 standard. Instead, the I^{2}C bus exposed through the *Utility(PSU)* connector (pins *M_SCL*, *M_SDA*) is driven directly by the System Board according to Table 1.

2.1.18   The pin assignment of the Peripheral Slot P4 (RTM) connector shall be compliant with P4 connector in Table 47 and Table 48 of the PICMG CPCI-S.0 [1] standard. The front P4 (RTM) connector (Figure 4) for each slot shall be wired to a mating Airmax connector in the back (Figure 5).

2.1.19   P4 (RTM) I/Os of row 1 (8 signals) are used to distribute two auxiliary voltages provided either by one of the Peripheral Boards, or through the *Aux Volt* connector (Figure 5). For this reason, two power planes (*Vaux1*, *Vaux2*) shall be created in the P4(RTM) space of the backplane and connected to P4(RTM) pins according to Table 5.

2.1.20   The *Aux Volt* connector shall be the FCI PwrBlade with 4 power contacts and 8 signal contacts (e.g. 51740-10200802AALF). It shall be placed on the back side of the backplane and its pinout shall be done according to Table 6. In case Peripheral Boards need to be provided with a specific voltage (e.g. to power analog front-end), an auxiliary power supply can be plugged to *Aux Volt* connector. It inputs +12V DC and produces desired auxiliary voltages (*Vaux1* and *Vaux2*) that are then distributed to all Peripheral Slots over *P4(RTM)* connectors (Table 5).

2.1.21   The width of *Aux Volt* rear slot shall be 4HP (Horizontal Pitch).

2.1.22   Corresponding P4 (RTM) I/Os of row 2 (8 signals) shall be connected between all Peripheral Slots. This way an 8-line bus is created that can be used for board-to-board communication (See Table 5).

Note: PCB traces of 8-line bus shall be wide enough to match the current rating of the Airmax connector (0.95A per pin).

2.1.23 The placement, dimensions and tolerance of the mounting holes shall be compliant with section 3.7.1 of the PICMG CPCI-S.0 specification [1].

2.1.24 Power (12V, 5V, GND) shall be provided to the backplane through screw terminals (power bugs) rated for ≥ 50A – see Figure 5 for the proposed power bugs layout.

2.1.25 The signal integrity of the backplane design shall be fully simulated prior the production.

2.1.26 The signal integrity of the backplane shall be measured after the production. Additional, passive System Board and Peripheral Board shall be designed to interface measurement equipment with the backplane.

Pin no.	Signal	Pin no.	Signal
1	n/c	2	GND
3	GND	4	n/c
5	RTN_Sense	6	PS_ON#
7	+12V_Sense	8	PWR_FAIL#
9	P_PRES0	10	P_PRES1
11	M_SDA	12	M_SCL
13	P_RST	14	P_IO0
15	P_IO1	16	P_IO2

Table 2: Utility(PSU) connector pinout

Pin no.	Signal	Pin no.	Signal
1	GND	2	GND
3	F_RST	4	+12V
5	M_SCL	6	GND
7	+5V	8	+12V
9	M_SDA	10	GND
11	F_IO0	12	+12V
13	F_IO1	14	GND
15	GND	16	+12V

Table 3: FANTRAY connector pinout

Pin no.	Signal	Pin no.	Signal
1	GND	2	+5V
3	PWRBTN#	4	PRST#

Table 4: AUX connector pinout

Pin	A	B	C	D	E	F	G	H	I	J	K	L
4-08	GND	IO	IO	GND	IO	IO	GND	IO	IO	GND	IO	IO
4-07	IO	IO	GND	IO	IO	GND	IO	IO	GND	IO	IO	GND
4-06	GND	IO	IO	GND	IO	IO	GND	IO	IO	GND	IO	IO
4-05	IO	IO	GND	IO	IO	GND	IO	IO	GND	IO	IO	GND
4-04	GND	IO	IO	GND	IO	IO	GND	IO	IO	GND	IO	IO
4-03	IO	IO	GND	IO	IO	GND	IO	IO	GND	IO	IO	GND
4-02	GND	Bus[0]	Bus[1]	GND	Bus[2]	Bus[3]	GND	Bus[4]	Bus[5]	GND	Bus[6]	Bus[7]
4-01	Vaux1	Vaux1	GND	Vaux1	Vaux1	GND	Vaux2	Vaux2	GND	Vaux2	Vaux2	GND

Table 5: Peripheral Slot P4(RTM) connector pinout

P1	P2	D1	D2	P3	P4
		Bus[6]	Bus[7]		
		C1	C2		
		Bus[4]	Bus[5]		
GND	+12V	B1	B2	Vaux1	Vaux2
		Bus[2]	Bus[3]		
		A1	A2		
		Bus[0]	Bus[1]		

Table 6: AUX VOLT connector pinout

3 Crate powering

3.1 Main power supply

<u>Development by:</u> BE-CO, R2E, TE-EPC (rad-tol variant)

The main power supply receives 230V AC and produces +12V and +5V that are distributed over the main backplane (common CompactPCI Serial or custom application-specific) to the System Board and all Peripheral Boards (Figure 6). Each board produces locally, with low power DC-DC converters and/or LDOs the specific voltages that are needed for its operation.

In radiation-free applications an off-the-shelf 300W main power supply would be used while for radiation-exposed areas a custom rad-tolerant development will be done. Both types of main power supplies shall meet the following characteristics:

3.1.1 Input voltage: 230V AC, 50Hz

3.1.2 Outputs: +12V, +5V

3.1.3 Output power for rad-tolerant variant: 10W (+5V), 100W (+12V)

3.1.4 Output power for off-the-shelf variant: 10W (+5V), 300W (+12V)

3.1.5 Ripple and noise: <100mVpp (+12V), <20mVpp (+5V)

3.1.6 Radiation tolerance (for rad-tolerant variant): ≥ 500Gy

3.1.7 Switching frequency: 250kHz – 1MHz

3.1.8 Physical dimensions: 100mm x 160mm x 37mm (8HP)

3.1.9 Cassette enclosure for high voltage separation and heat dissipation

3.1.10 PMBus monitoring interface (specified in section 8.4). In case of the rad-tolerant PSU, PMBus is implemented by the Monitoring Module (specified in section 8.2).

3.1.11 Current sharing line to enable operation in redundancy configuration

3.1.12 Remote On/Off switching

3.1.13 Connector: PwrBlade FCI 51939-667. The pinout compatible with the convention agreed among CompactPCI manufacturers (see Table 7).

3.1.14 The power supply plugs to a power backplane (section 3.2) which is a separate PCB connecting DC voltages and monitoring signals with cables to the main backplane.

P1	P2	P3	P4	P5	D1	D2	D3	D4	D5	D6	P6	P7	P8	P9
LINE	NEUTRAL	PE	DC_IN	DC_RTN	N/A	PWR_FAIL	PRESENT	GND	DEG	+5V	GND	GND	+12V	+12V
					C1	C2	C3	C4	C5	C6				
					N/A	N/A	GND	A0	+5V	+5V				
					B1	B2	B3	B4	B5	B6				
					N/A	+12VCS	PS_ON	A1	SCL	GND				
					A1	A2	A3	A4	A5	A6				
					N/A	RTN_Sense	+12V_Sense	A2	SDA	ENABLE				

Table 7: PwrBlade FCI 51939-667 power connector pinout
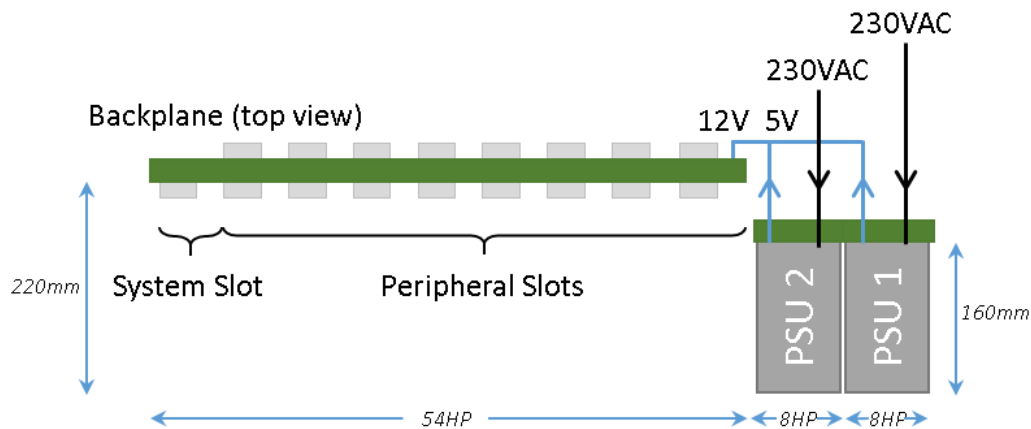

Figure 6: Main PSU powering scheme

3.2 Power backplane

Development by: BE-CO and external company or off-the-shelf product

The role of the power backplane is to interface between the main power supply and the main 3U backplane. The reason of having a power backplane separated from the main backplane is the difference in depth between the System and Peripheral boards (220mm) and the standard CompactPCI Serial power supplies (160mm) – please see section 4 for more details. It is also useful to have it as a separate module for more flexibility on crate mechanical assembly (only one power backplane can be mounted in case redundancy is not needed, power supplies can be placed in the back of the crate if required).
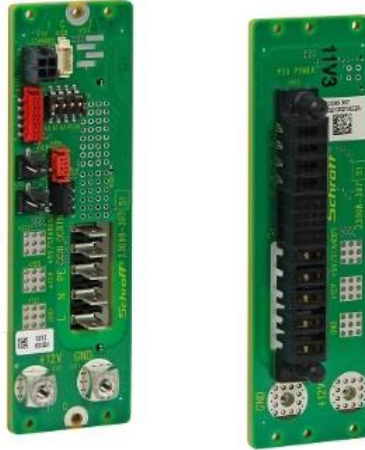
Figure 7: Off-the-shelf power backplane example (back and front side)

The power backplane shall meet the following characteristics:

3.2.1   The backplane shall have mechanical dimensions of 100mm x 8HP (40.64m).

3.2.2   The backplane shall use FCI 51940-473 power connector (receptacle for FCI 51939-667) to interface with the main DI/OT power supply (section 3.1)

3.2.3   The pinout of FCI 51940-473 shall be consistent with the convention agreed among CompactPCI manufacturers (see Table 7).

3.2.4   The 230V AC FASTON terminals of the power connector shall be accessible through a hole in the backplane (Figure 7) to ensure no high voltage signals are routed through the backplane. Moreover, this way no high voltage contacts are exposed (to avoid electrocution) when the 230V FASTON plugs are isolated.

3.2.5   The backplane shall expose two utility connectors (*Utility1*, *Utility2*) with PSU monitoring signals (pinout according to Table 8) using IDC connectors with latches to prevent loose contacts. These two connectors are used to daisy-chain two power backplanes and the main 3U DI/OT backplane (section 2.1). Signals are directly wired between *Utility1* and *Utility2* with some of them being crossed according to Table 8.

3.2.6   The backplane shall have a jumper that will allow to open/close the *CUR_SHARE* line between *Utility1* and *Utility2*.

3.2.7   The backplane shall wire the signals of the utility connector to the FCI 51940-473 power connector according to Table 8.

3.2.8   The backplane shall expose +12V, +5V and GND rails using screw terminals (power bugs) rated for ≥ 50A.

3.2.9   The backplane shall be equipped with a DIP switch to configure the addressing lines of the FCI power connector (pins C4, B4, A4). Each of these signals shall be connected to GND or floating depending on the DIP switch position.

Signal	Utility1 pin	Utility2 pin	FCI pin	Signal	Utility1 pin	Utility2 pin	FCI pin
CUR_SHARE	1	1	B2	GND	2	2, 10	D4
GND	3	3, 16	D4	PS_ON#	6	6	B3
RTN_Sense	5	5	A2	PWR_FAIL#	8	8	D2
+12V_Sense	7	7	A3	P_PRES1	10	9	--
P_PRES0	9	--	D3	M_SCL	12	12	B5
M_SDA	11	11	A5	P_IO0	14	14	B1
P_RST	13	13	A1	P_IO2	16	15	D1
P_IO1	15	--	C1	--	--	--	--

Table 8: Power backplane control signals wiring

3.3 Aux power supply

Developed by: Equipment groups

In the cases when a specific voltage cannot be produced locally on a Peripheral Board, one can also design and use an auxiliary power supply according to the following characteristics:

3.3.1 An aux power supply is highly recommended to be a specialized Peripheral Board or an RTM Board that receives +12V from the P1 backplane connector and produces the required voltage levels on bus lines of the P4 connector (see section 2.1) to be distributed to all Peripheral Boards (Figure 8).
Note: various designs (e.g. QPS electronics, DOROS system) have shown that a very clean voltage for analog front-end can be generated using a cascade of DC-DC regulator with one (ripple and noise < 5mVpp) or multiple LDOs (ripple and noise ~ 10µVpp). Please see [2] for measurement results of 2mVpp ripple on 5V power rail generated by the cascade: Traco AC/DC (TPP-40 105) →Murata DC/DC (MEJ2D0515SC) →Texas Instr.LDO (TPS7A49)

3.3.2 If an aux power supply is placed in the last slot of the main backplane, its maximum width can be 10HP. In this case, a 4HP front metal plate next to PSU1 (described in section 4.1) shall be removed.

3.3.3 If 10HP is not sufficient, an aux power supply can be a cassette occupying several peripheral slots, e.g. to host a linear power supply with a 50Hz transformer. In such case the Aux PSU cassette would directly receive 230V AC, produce the auxiliary voltages with a linear regulator and forward the 230V AC to the main PSU (Figure 9).

3.3.4 The distribution of auxiliary voltages is done over the P4 connector of the common backplane (section 2.1) or in a fully custom backplane (section 9.1).

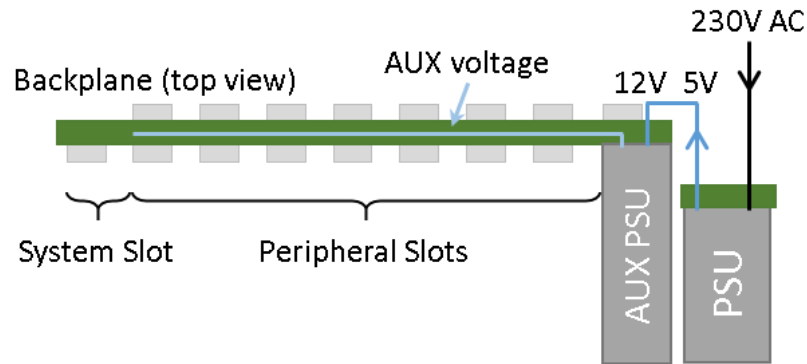3.3.5 Aux voltages are distributed only to peripheral boards, the system slot does not receive them.

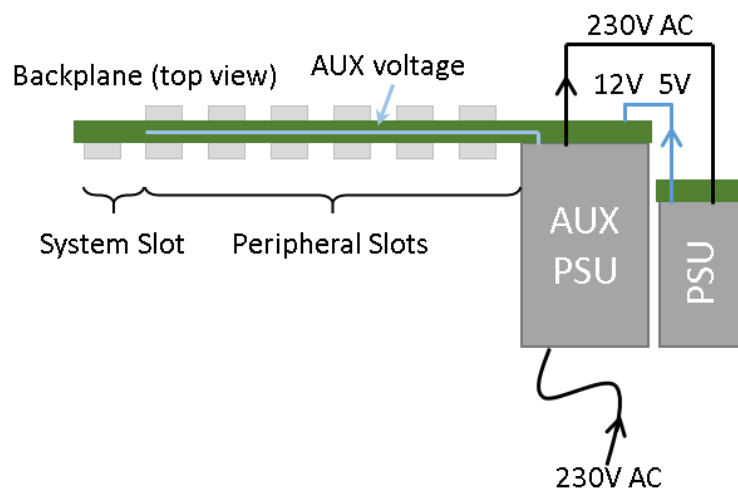*Figure 8: Powering scheme with Aux PSU (using the common backplane)*

Figure 9: Powering scheme with aux linear PSU (using a custom backplane)

4 3U Chassis mechanics and cabling

Developed by: BE-CO with equipment groups and external company

To cover the requirements of various systems the chassis is modular and consists of:

- 3U CompactPCI Serial crate assembled from standard 3U sub-rack components (available from various crate manufacturers and through CERN stores). It hosts the main backplane (described in 2.1), two power backplanes (described in 3.2), and a front panel (described in 4.2).
- Optional 1U fan tray, which can be mounted below or on top of the main chassis (described in section 5).
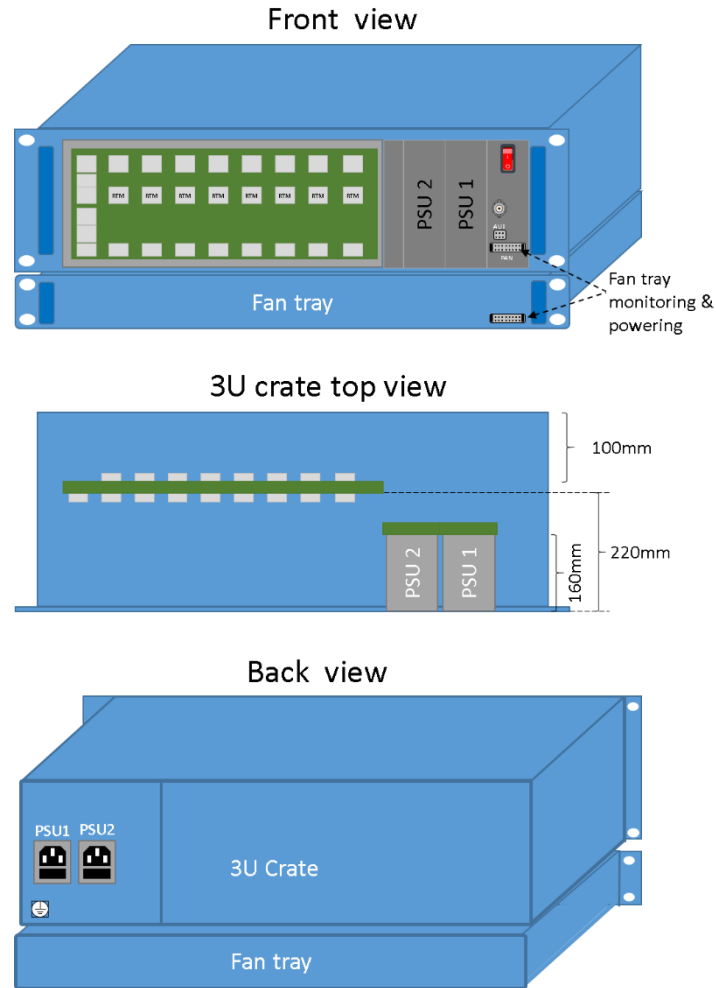
Figure 10: DIOT crate and fan tray mockup

4.1 Main 3U crate

The main 3U crate shall be compliant with the following characteristics:

4.1.1 Height shall be 3U (3 rack units)

4.1.2 Width shall be 19" with 84 HP (horizontal pitch) usable space.

4.1.3 The crate shall be assembled from standard 3U sub-rack components compatible with the mechanical standards IEC 60297-3 and IEEE 1101.10-1996 [3].

4.1.4 The crate shall be equipped with rack mounting holes and front handles.

4.1.5 The crate shall be equipped with a front and rear attachment plane compliant with section 8 of the IEEE 1101.10-1996 standard [3], to enable locking each front and rear board using an IEEE Injector/Ejector Handle.

4.1.6 The crate shall be equipped with 2 power backplanes (as defined in section 3.2) to host two main power supplies (section 3.1) in a load sharing redundancy configuration – a current sharing signaling cable shall be connected between the two power backplanes (Figure 12).

4.1.7 Both power supply slots shall be placed on the right side of the main backplane (PSU1, PSU2 in Figure 10).

4.1.8 The crate shall mount and connect the front panel as defined in section 4.2.

4.1.9 The crate shall mount a 4HP front metal cover to fill free space between the PSU1 and the last backplane slot. This front metal cover shall be equipped with EMC gasket.

4.1.10 The rear metal cover of the crate shall be split in two segments: 26 HP (Horizontal Pitch) metal panel hosting two 230V AC IEC power entry sockets and the earth screw; 58 HP (Horizontal Pitch) metal panel covering the rest of the rear space. In case there is a need to plug rear modules, the 58 HP metal panel will be removed.

4.1.11 The crate shall have perforated bottom and top covers (Ø4mm) to allow better airflow.

4.1.12 The crate and fan tray enclosure shall be compliant with IP2X rating.

4.1.13 The crate shall host the common CompactPCI Serial backplane (section 2.1) – power and signaling cabling, and backplane mounting holes shall be placed accordingly.

4.1.14 The crate shall host front boards (System Board and Peripheral Boards) which are 220mm long. Therefore the backplane needs to be mounted 60mm deeper than in regular CPCIs crates.

4.1.15 Each slot of the crate shall have a width of 6HP. Card guide rails shall be mounted accordingly.

4.1.16 220mm card guide rails according to IEEE 1101.10 shall be used. For the System Slot (slot 1) a red guide rail shall be used (e.g. Schroff P/N 64560-091), while for all Peripheral Slots (slot 2-9) gray guide rails shall be used (e.g. Schroff P/N 64560-092).

4.1.17 The crate shall leave 100mm of rear space behind the backplane for optional rear transition modules or an expansion backplane. The mechanics of the crate shall provide metal supports for the 100mm card guide rails for optional rear modules. However, these rails shall not be mounted.

4.1.18 The crate shall provide mechanical mounting and cabling of the monitoring components specified in section 0.

4.1.19 The *Utility*(*PSU)* connector of the main backplane shall be connected using a ribbon cable with the Utility connectors of both power backplanes (Figure 12).

4.1.20 Two 230V AC IEC power entry sockets with a fuse and EMC filter shall be placed in the back of the crate (Figure 10) and wired with FASTON terminals to the front panel (Figure 12). These power entry modules shall be compatible with a locking mechanism to prevent accidental removal (e.g. V-Lock from Schurter, IEC-LOCK from Schaffner).

4.1.21 The earth screw shall be placed in the back of the crate and connected to earth contacts of 230V AC IEC power sockets as depicted in Figure 12.

4.1.22 The cabling of the crate shall be done according to wiring diagram in Figure 12.

4.1.23 All outer covers of the crate (top, bottom, left, right, front, back) shall be powder coated with color RAL XXXX (**TBD** influence on EMC).
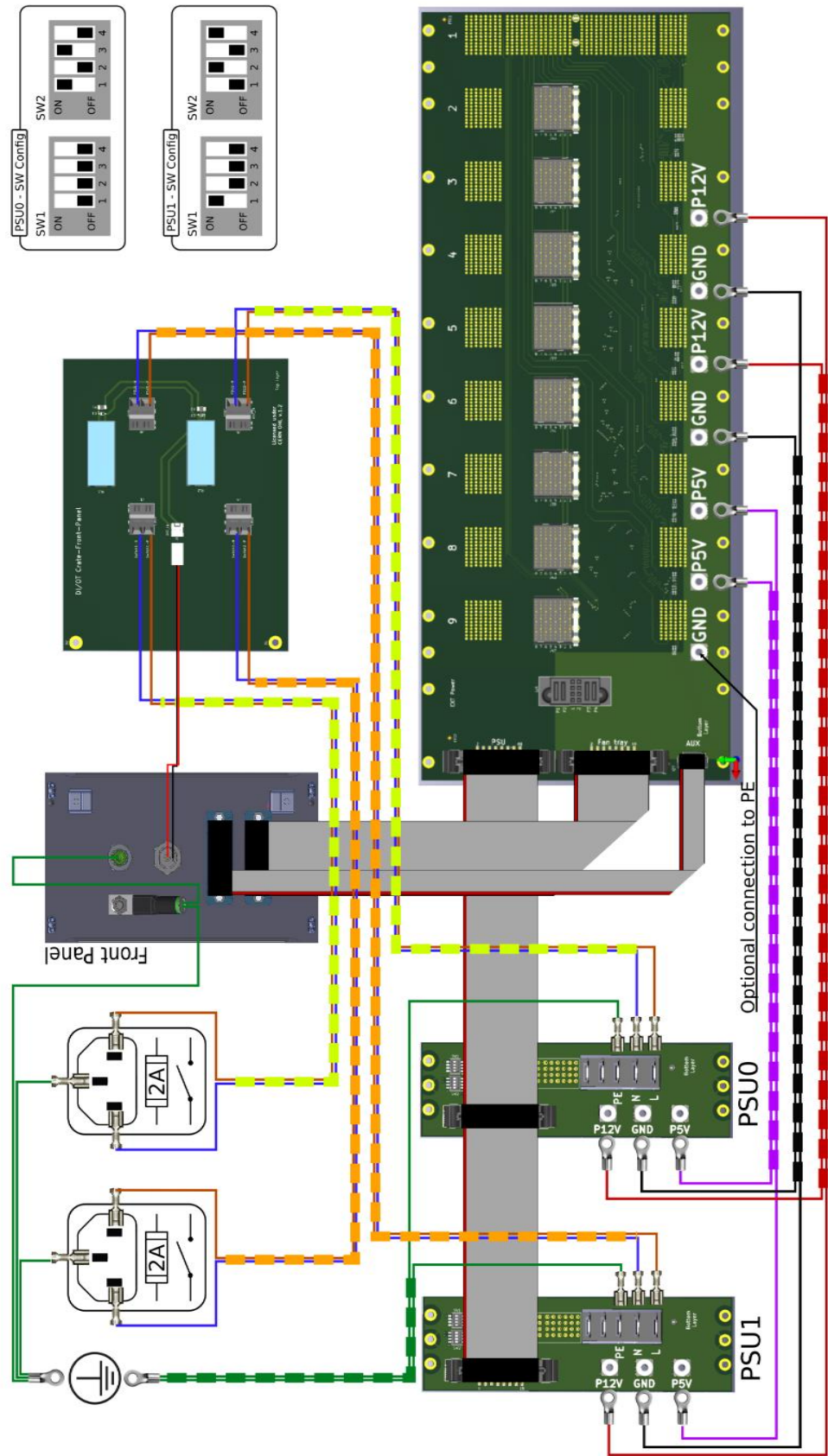
4.2 Front panel

Figure 11: Crate front panel

The front panel module (Figure 11) shall be compliant with the following characteristics:

4.2.1 The front panel shall be installed on the right side of the crate, next to the power supplies (Figure 10) and have a width of 14HP.

4.2.2 The front panel shall be equipped with an EMC gasket.

4.2.3 The front panel shall host an ESD plug for connecting ESD bracelet when manipulating the boards, a BNC connector for external power cycling, a fan tray connector and an AUX connector.

4.2.4 The fan tray connector shall be a female 15-pin DSUB with screws preventing accidental removal (Amphenol 53611-G16-8LF). It shall be connected through a ribbon cable to the fan connector in the main backplane (pinout specified in Table 3).

4.2.5 The Front AUX connector shall be a female 15-pin DSUB with screws preventing accidental removal. It shall be connected to the signals arriving from the 4-pin Back AUX connector (wired to the AUX connector on the main backplane) and 12V arriving from the fan tray connector according to Table 9.

4.2.6 The BNC connector can optionally input an external signal (5V TTL, active high) that is used for power cycling the crate. It shall drive a relay connected in series with the power button to break on request the 230V AC power going to the power supplies.

4.2.7 The aforementioned components shall be placed on a PCB screwed to the metal plate of the front panel to ensure proper and reliable mounting.

Signal	Front Aux pin	Back Aux pin	Signal	Front Aux pin	Back Aux pin
GND	1	1	*PRST#*	4	4
+5V	2	2	*GND*	5	1
PWRBTN#	3	3	*+12V*	6	--

Table 9: Front panel Aux connectors pin assignment

Figure 12: DI/OT crate wiring diagram (back view of the front panel and backplanes)

version 1.1

5   Fan tray

Developed by: BE-CO with equipment groups or off-the-shelf fan tray

The fan tray is an additional module to the main 3U CompactPCI Serial crate. It could be placed in the rack, below or above the 3U crate for systems that require better heat dissipation (e.g. deployed in radiation-free areas). Either an off-the-shelf 12VDC powered or a custom made fan tray can be used. The custom made fan tray shall contain BLDC (Brushless DC) fans, temperature sensors and a monitoring module (the same one used for power supply monitoring) and should meet the following requirements:

5.1.1   The fan tray's height shall be 1U (1 rack unit)

5.1.2   The fan tray's width shall be 19".

5.1.3   The fan tray shall be equipped with rack mounting holes and front handles

5.1.4   The placement of fans inside the fan tray shall be such to provide air flow for all the front cards and the power supplies.

5.1.5   The fan tray shall receive power and control signals through a 16-pin IDC connector (with latches to prevent accidental removal) from the main 3U chassis. The fans inside the fan tray shall be powered from +12V and the monitoring module from +5V. There is no additional power supply mounted inside the fan tray.

5.1.6   The fan tray shall draw not more than 36W from the +12V power provided by the IDC connector. Note: This estimation is a safe upper limit based on the current that can be provided over the IDC connector (1A per-pin, current pinout of the connector in Table 3 dedicates 4 pins to provide +12V power). It can be reached in radiation-free areas where powerful, off the shelf PSU is used (e.g. 300W). In radiation-exposed areas the fan tray is expected to draw not more than 10-15W.

5.1.7   The fan tray shall host a monitoring module (the same one as used for power supply monitoring, see section 8.2 for details) that communicates with the System Board of the 3U crate over a PMBus interface.

5.1.8   The pinout of the front connector of the fan tray shall be identical to that of the IDC connector exposed on the front panel of the main 3U crate (see Table 3).

5.1.9   The fan tray shall feature a fully passive board hosting a front IDC connector, fan connectors and pin headers to plug the monitoring module.

5.1.10   The fan tray shall ensure air flow at the level of 360 CFM (Cubic Feet per Minute) (three fans each providing 120 CFM) - **TBD** further simulations are ongoing.
Note: This is based on DI/OT proof of concept off-the-shelf crate. Thermal simulations to be done, to determine what's the sufficient minimum air flow, especially that in radiation-exposed areas the main power supply can provide 100W total power (comparing to 300W outside radiation).

6   System Board

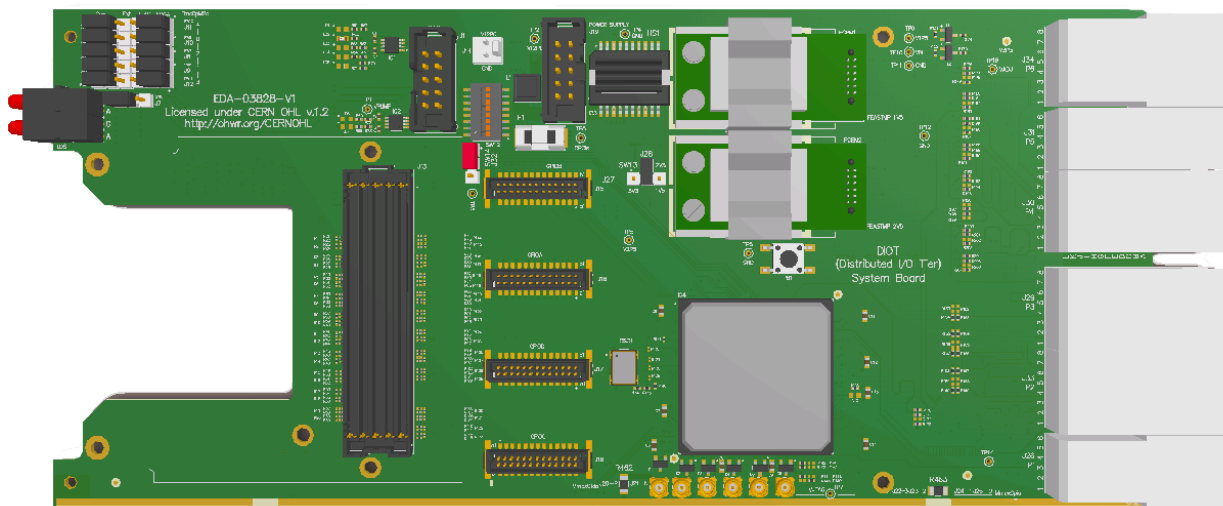<u>Developed by:</u> BE-CO with equipment groups

Figure 13: DI/OT System Board example

The common Distributed I/O Tier System Board (Figure 13) is the main FPGA-based board in the DI/OT crate. It is the main crate controller that communicates with application-specific peripheral boards, fieldbus mezzanine and is responsible for crate monitoring. The project foresees a design of two variants of the system board (radiation-tolerant and non-radiation-tolerant) of the following characteristics:

6.1.1   The board's dimensions are 100mm x 220mm x ≤ 6HP

6.1.2   The board shall be equipped with an LPC FMC connector to host a communication mezzanine.

6.1.3   In addition to point 6.1.2, the non-radiation-tolerant variant of the system board shall connect 3 of the HPC gigabit transceiver interfaces to the FPGA to support in total 4 high speed transceivers of a communication mezzanine.

6.1.4   The board may host any other (not only communication) LPC FMC mezzanine if required by the application.

6.1.5   The FPGA selection for radiation-tolerant variant shall be made between a Flash-based FPGA (e.g. SmartFusion2) and a radiation-hard SRAM-based NanoXplore FPGA (NG-Medium).

6.1.6   The non-radiation-tolerant variant shall feature a System-on-Chip (e.g. Xilinx Zynq/Zynq Ultrascale). A more powerful unit is required outside radiation since for those applications equipment groups will be implementing more complex data processing.
         <u>Note:</u> If a DI/OT installation spans across both radiation-exposed and radiation-free areas, one can also use the radiation-tolerant variant of the System Board in radiation-free areas to keep the whole system homogeneous.

6.1.7   The board shall have a set of 6 Airmax connectors (P1 – P6) to communicate with the DIOT backplane, following the CompactPCI Serial specification PICMG CPCI-S.0 [1] (see table below).

Designator	Rows	Pins	Walls	P/N
P1	6	72	4	10052825-101LF
P2, P3, P4	8	96	2	10052837-101LF
P5	6	72	2	10052824-101LF
P6	8	96	4	10052838-101LF

6.1.8 The pinout of the P1 – P6 Airmax connectors shall be compatible with the CompactPCI Serial specification PICMG CPCI-S.0 [1], with the difference that all the PCIe, USB, SATA, Ethernet lanes are used as general purpose differential lanes for simple communication with peripheral boards (e.g. using fast SPI or direct I/O connections).

6.1.9 The system board shall produce locally, using DC-DC converters and LDOs, voltage levels required for the FPGA, FMC mezzanine and all other on-board components.

6.1.10 The FPGA of the System Board shall connect to the 11 general purpose I/O lines ("IO" signals in Table 44 and Table 45 of PICMG CPCI-S.0 [1]) to use them for various monitoring-related interfaces (e.g. PSUs PMBus, Fan tray monitoring) according to Table 1.

7   Peripheral Boards

Developed by: Equipment groups

7.1   Specification

Peripheral boards are the application-specific boards, to be installed in slots 2-9 of the 3U crate. They are designed by the equipment groups to fit a specific application and share some common characteristics to be re-usable between groups:

7.1.1 The board's dimensions are 100mm x 220mm x ≤ 6HP
Note: Peripheral Board can be wider than 6HP, but in that case it will block adjacent backplane peripheral slots.

7.1.2 The board shall use a 72-pin P1 Airmax connector (see table in 6.1.7) to communicate with the System Board over the common CompactPCI Serial backplane. The P1 connector provides:

- Power: +12V, +5V, GND
- 14 LVDS differential pairs between the Peripheral Slot and the System Slot of which:
  - *<slot>_mtx_p/n; <slot>_mrx_p/n* – 2 pairs are routed for high-speed communication (e.g. MGT FPGA transceivers)
  - *<slot>_clk_p/n* – 1 pair is routed to provide a low skew clock distribution to this slot
  - *<slot>_d[0..10]_p/n* – 11 pairs can be used for any sort of communication up to tens-Mbps (e.g. fast SPI or direct I/O connections).
- *RST_N* – a reset line common to all Peripheral Slots.
- *I2C_SCL, I2C_SDA* - a service I2C bus, shared between all the slots, used for Peripheral Boards identification.
- *SHARED_BUS[0..4]* – 5 multi-drop single-ended lines shared between all the slots. Those can be used as internal interlock lines.
- *<slot>_SERVMOD_N* single-ended signal used for Peripheral Board identification

7.1.3   In the case of radiation-tolerant variant of the System Board, MGT FPGA transceivers are not used, therefore *<slot>_mtx_p/n; <slot>_mrx_p/n* differential pairs are connected to regular FPGA I/Os and can be used for general purpose communication (like *<slot>_d[0..10]_p/n*).

7.1.4   Optionally, a P6 Airmax connector can be used if more communication lanes between the Peripheral Slot and the System Slot are needed. The P6 connector provides:

- *<slot>_d[11..14]_p/n* – 4 LVDS differential pairs between the Peripheral Slot and the System Slot that can be used for any sort of communication up to tens-Mbps (e.g. fast SPI or direct I/O connections).

7.1.5   Optionally, a 96-pin P4 Airmax connector (RTM) can be used if direct communication between Peripheral Slots is required or if a Peripheral Slot needs an RTM (Rear Transition Module). The P4 connector provides:

- *Vext1; Vext2* – two voltage levels provided from the external power supply
- *RTM_BUS[0..7]* – 8 single-ended lines shared between all the Peripheral Slots. Each line can carry up to 0.95A. Those can be used for inter-board communication.
- *RTM_IO[0..47]* – 48 pins are routed to the back of the backplane for RTM communication.

7.1.6   If the functionality of the P4, P6 connectors is not needed, the connectors may not be placed on the Peripheral Board.

7.1.7   The board receives through the P1 connector +12V (main power rail) and +5V (low power standby rail) and should produce locally, using DC-DC or LDO, the voltages required to its operation. The total power provided by the power supplies for the 12V is 100W (for radiation-tolerant in-house designed PSU) and for the +5V is 10W; this includes the consumption of the System Board and of the Fan Tray (if needed).

7.1.8   Auxiliary voltages (e.g. for analog frontend) can be provided through the P4 (RTM) connector (see section 2.1).

7.1.9   The pinout of the P1 (and optionally P6) Airmax connectors shall be compatible with the CompactPCI Serial specification PICMG CPCI-S.0 [1] , with the difference that all the PCIe, USB, SATA, Ethernet lanes are used as general purpose differential lanes for simple communication with peripheral boards (e.g. using fast SPI or direct I/O connections).

7.1.10   If additional shielding is needed (e.g. for an analog front-end), a peripheral board can be housed in a 3U cassette.

7.1.11   If a custom application-specific backplane is used, the selection of the connector for peripheral boards is up to the designer (e.g. DIN-type connectors can be used if needed).
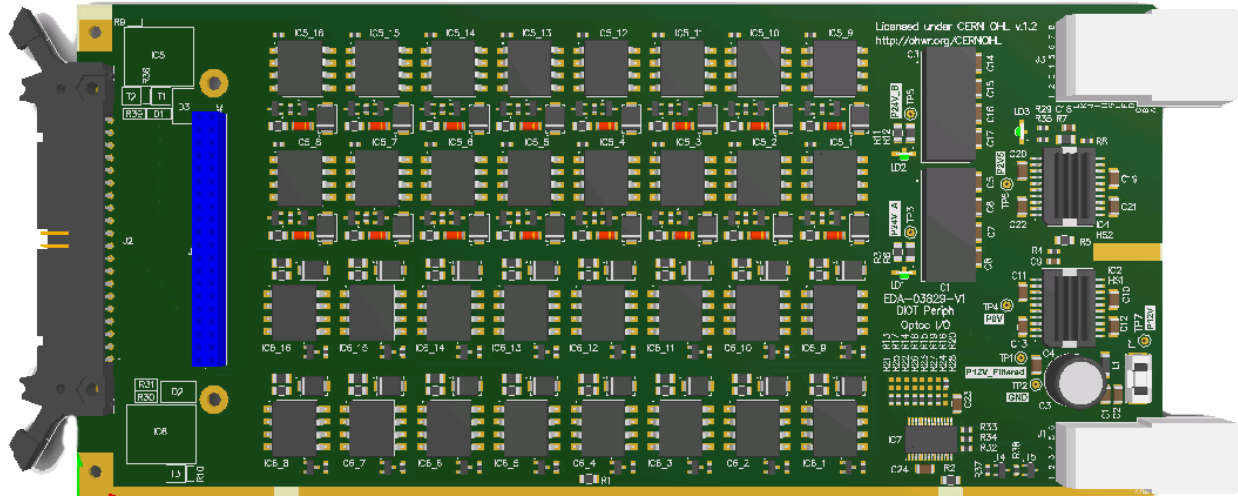
Figure 14: DI/OT Peripheral Board example

7.2 Peripheral Boards identification and remote reprogramming

To ensure the means of identification, each Peripheral Board (and its RTM if available) shall be equipped with I2C EEPROM that could be dynamically attached to the service I2C bus. Peripheral Boards are identified by the system board using the combination of *<slot>_SERVMOD_N* signal and the service I2C bus. *<slot>_SERVMOD_N* signal is used to enable Service Mode for a given Peripheral Board. When in Service Mode, Peripheral Board attached I2C EEPROMS to the shared I2C bus and selected backplane I/O lines to JTAG TAP (if the board features an FPGA).
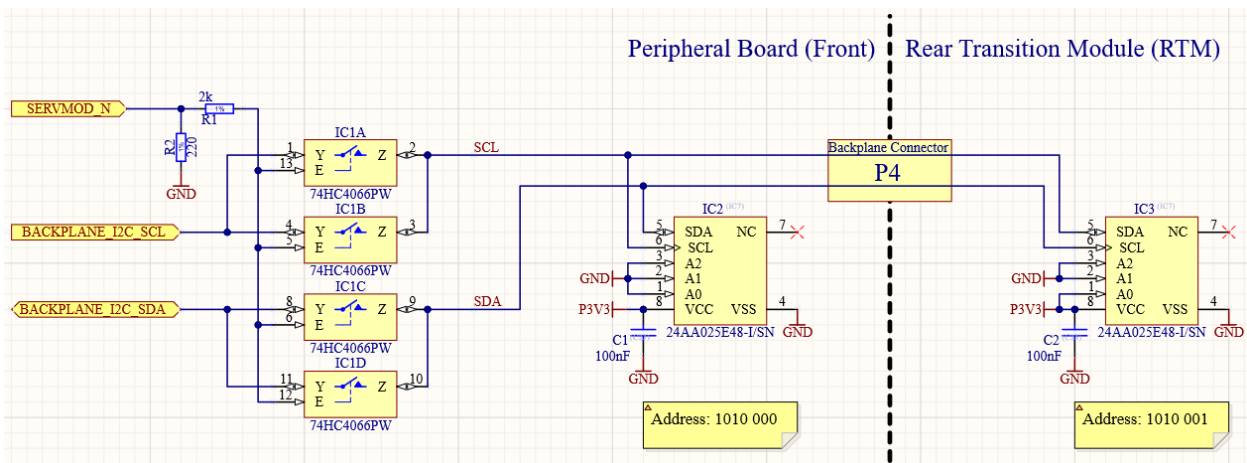

Figure 15: Circuit required for Peripheral Board identification

Identification procedure:

1. System Board reads *<slot>_SERVMOD_N* state (low = board inserted in a given peripheral slot)
2. System Board drives *<slot>_SERVMOD_N* high to attach identification EEPROM/-s to the shared I2C bus
3. System Board reads unique ID and additional information about Peripheral Board and RTM (if present)
4. After the identification cycle is finished System Board releases *<slot>_SERVMOD_N* for this slot.

<u>Attention:</u>   Digital switches and EEPROMs from Figure 15 are not qualified for radiation-exposed applications. **TODO:** Check EEPROM and digital switch recommendation for radiation-tolerant boards.

<u>Backplane P1 connector pins have dual IO/JTAG function (selectable with *<slot>_SERVMOD_N*):</u>
- A3 (*<slot>_d0_p*) – TDI
- D3 (*<slot>_d1_p*)– TDO
- B4 (*<slot>_d2_p*)– TMS
- H4 (*<slot>_d3_p*)– TCK
- K4 (*<slot>_d4_p*)– nTRST

8   Crate monitoring

Developed by: BE-CO with Equipment groups

Monitoring of the DIOT crate is implemented in the main FPGA of the System Board and utilizes 11 general purpose I/O backplane lines to communicate with the power supplies and the optional fan tray. Following the PICMG CPCI-S.0 specification [1], the communication with these modules is based on the I^{2}C interface. According to the standard an I^{2}C System Management Bus is shared between the power supplies, fan tray, and all the peripheral boards. In the DIOT crate two separate I^{2}C busses are distinguished:

- I^{2}C System Management Bus – exposed on the utility connector (as defined in the CPCI-S.0 standard), but connected to the System Slot using 2 of the general purpose I/O backplane lines (see *M_SCL*, *M_SDA* lines in Table 1). It is used to read monitoring quantities of the power supplies and the fan tray.
- I^{2}C Peripheral Bus – shared bus between the System Slot and all Peripheral Slots (utilizes *IC_SCL*, *IC_SDA* backplane lines). It is used to read the board ID of each Peripheral Board for autodetection.

8.1   Monitored Quantities

In this section the measurements that comprise the readout part of the diagnostics are described.

8.1.1   For each main PSU, voltage and current monitoring for each of the power rails (12V / 5V) shall be provided, along with one temperature (might be worth it to put more, one ambient and two major loads, **TBD**) readout.

8.1.2   Multiple temperature sensors shall be supported by means of the monitoring modules in the PSU(s) and the optional fan tray. These may be mounted on the top or bottom grill, the backplane or in otherwise strategic locations, depending on the application.

8.1.3   Depending on the fan test results (**TBD**) the user may be able to monitor the speed of the fans in the optional fan tray and control the fan set-points.

8.2   Monitoring module

Developed by: BE-CO

A monitoring module shall be developed to provide PMBus (I^{2}C–based) monitoring and control for the PSU(s) and the fan tray. It shall be a small form-factor module (Figure 16) that can be mounted on a motherboard.
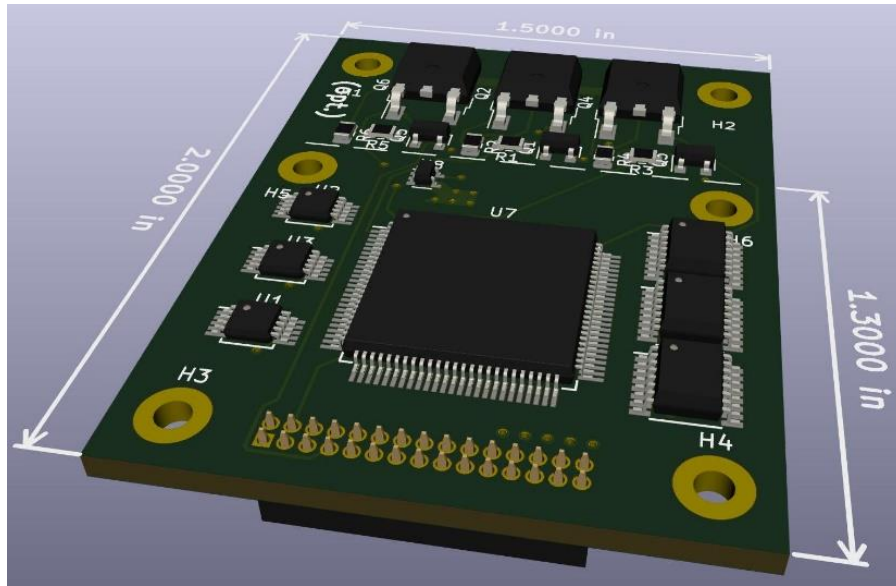
Figure 16: Mockup of the monitoring module

8.2.1   When driving fans, the module shall be powered by 12V and 5V power rails. When it is not driving any fans, supplying the 5V power rail will be enough (e.g. inside the PSU).

8.2.2   A reset signal from the FPGA on the System Board shall be provided to the microcontroller in case a watchdog fails in radiation-exposed areas and it enters a fault condition (e.g. line *P_RST* in Table 2).

8.2.3   A subset of the PMBus protocol (specified in section 8.4) shall be used to interface with the monitoring module. Two pins shall be used to set the module's I^{2}C address.

8.2.4   Voltage and current monitoring of up to three power rails shall be supported.

8.2.5   Up to three temperature sensors of PT100/PT1000 type (or I^{2}C, **TBD**) shall be supported.

8.2.6   PWM control of up to three 12V fans shall be provided. Up to 1A of current shall be provided to each fan.

8.2.7   If the fans provide a dedicated PWM control pin, the power FET part of the module becomes redundant. Thus, a reduced-size version of the module may also be produced (notice the dashed line in Figure 16) or jumpers can be added to reroute the 12V so that the same board might be physically cut, **TBD**.

8.2.8   If the fans provide speed sense pins, speed measurements shall be also made available through the PMBus interface.

8.2.9   An SWD (Serial Wire Debug) programming interface shall be provided through the main connector and through an on-board header connector.

8.2.10 Exact details of this module have to remain **TBD** for now (most probably it will feature ATSAMD21G18 microcontroller, radiation tests are ongoing).

8.3   Monitoring software services

8.3.1   CCS

8.3.2   COSMOS

8.3.3   Remote reprogramming framework

8.4   PMBus for DI/OT

9 Customization examples

This section lists examples how the common and modular DI/OT hardware kit can be customized for various applications.

9.1 Custom application-specific backplane

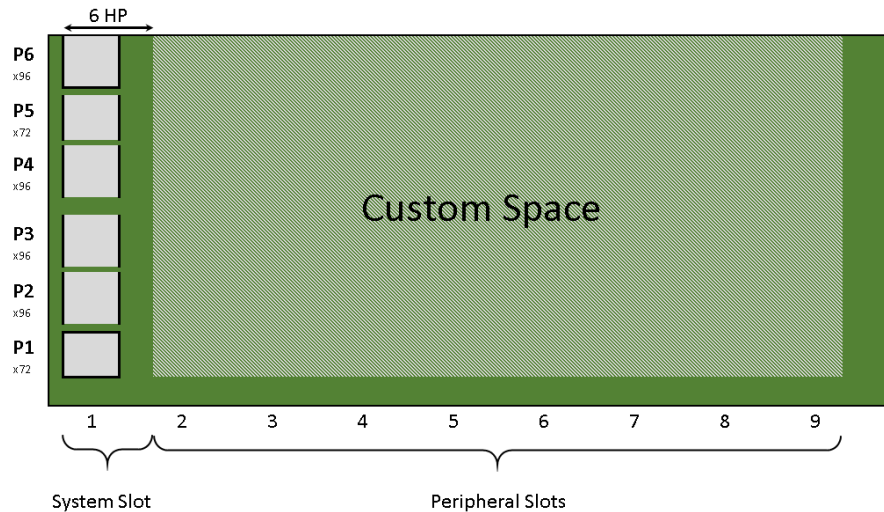Development by: Equipment groups

Figure 17: Custom DIOT backplane

A fully custom backplane may be designed for applications with constrains that cannot be fulfilled by the common DI/OT backplane. Such a custom backplane shall have the following characteristics for compatibility with the DI/OT crate mechanics:

9.1.1   The backplane shall have a System Slot made of P1 – P6 Airmax connectors and 6HP width, as specified in section 2.1 and the Compact PCI Serial PICMG CPCI-S.0 [1] standard.

9.1.2   The backplane shall have a set of IDC connectors (*Utility(PSU)*, *FANTRAY*, *AUX*) as defined in section 2.1.

9.1.3   The backplane shall distribute +12V and +5V power from the main power supply to the System Slot and IDC connectors (*Utility(PSU)*, *FANTRAY*).

9.1.4   The backplane shall have mounting holes compatible with a common DI/OT backplane (section 2.1).

9.1.5   The backplane shall not be more than 54 HP wide (including the System Slot) in case it has to fit in the crate mechanics as defined in section 4.1.

9.1.6   The rest of the backplane ("Custom space") can host any application-specific connectors and additional signal wiring. It can for example be used to distribute any non-standard auxiliary voltages to Peripheral Boards (e.g. for analog front-ends) or to host I/O BNC connectors for external sensors/actuators.

10 References

[1] PICMG CompactPCI Serial (CPCI–S.0) Rev 2.0
https://www.picmg.org/openstandards/compactpci-serial/
(inside CERN only) https://wikis.cern.ch/download/attachments/103445302/PICMG%20CPCI-S.0.pdf

[2] Measurements of power supply ripple and noise for uQDS crate
https://wikis.cern.ch/download/attachments/103445337/UQDS_PSU_Ripple.pdf

[3] IEEE 1101.10-1996 standard
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