Distributed I/O Tier system specification

Draft for comments

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Revision table

Date	Version	Comments
2018-12-20	First draft	First draft released for comments
2019-02-28	2nd draft	Including input from Creotech
2019-03-29	3rd draft	Including monitoring-related backplane connectors

1 Introduction

Controls and data acquisition systems in accelerators often involve a computing platform (VME, PICMG 1.3, MTCA.4…) connected to Distributed I/O Tier electronics using a fieldbus communication link (Figure 1). The devices in the Distributed I/O Tier communicate directly with various sensors and actuators and are deployed close to the machine. Since these areas are frequently exposed to radiation and because of the very specific needs of CERN systems, these modules not being commercially available, are usually custom in-house developments. Currently, we are missing at CERN a centrally supported service for the custom electronics in this layer.

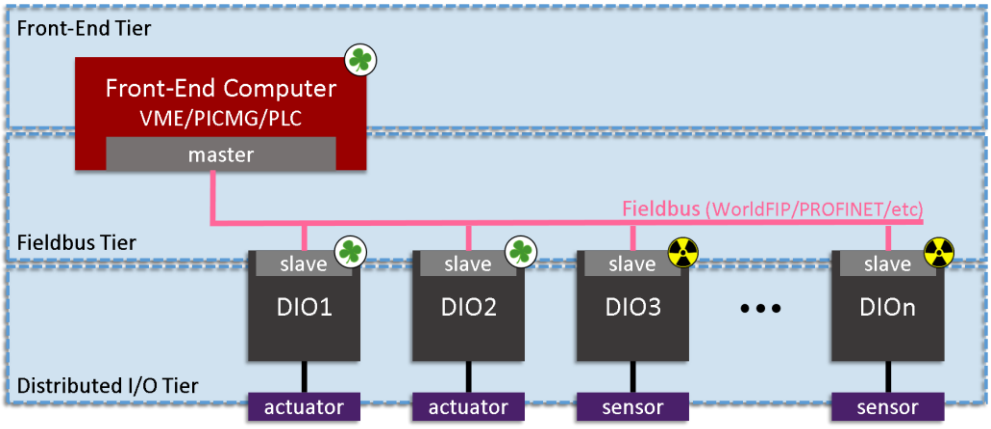

Figure 1: Three lowest hardware layers of a typical control system

The Distributed I/O Tier project aims at offering a new, modular and reusable hardware kit for various renovations and new systems to be deployed for the High Luminosity LHC (HL-LHC) in 2025. The kit to cover the requirements of the equipment groups in both radiation-exposed and radiation-free areas will consist of the following components (Figure 2):

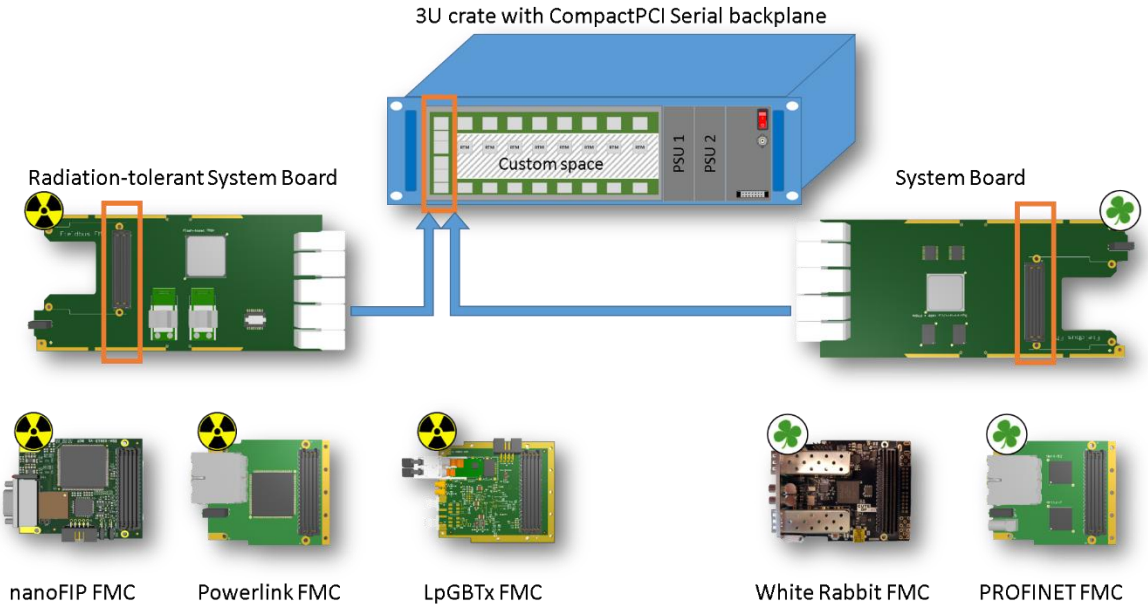

Figure 2: Distributed I/O Tier modular and reusable hardware kit

- A **low-cost CompactPCI Serial chassis** with a backplane and redundant power supplies (either off-the-shelf or radiation-tolerant in-house designed).
- Two generic **FPGA-based System Boards** (radiation-tolerant and non-radiation-tolerant) that interface with the application-specific peripheral boards plugged into the other slots of the 3U crate. Each System Board features a high-performant FPGA for the application-specific logic. A small fraction of the FPGA resources is dedicated to standardized crate diagnostics. The System Boards have an FMC slot, where a fieldbus slave mezzanine is plugged to provide communication with a master and the higher layers of the control system.
- A set of interchangeable, radiation-tolerant and non-radiation-tolerant **fieldbus communication mezzanines** in the FMC format that implement various communication standards: WorldFIP, Powerlink, LpGBTx, White Rabbit or PROFINET.

This document specifies the Distributed I/O Tier chassis, its components that are common to all equipment groups as well as the customization options to adapt it to specific needs of a particular use case.

2 Main 3U crate backplane

There are two options foreseen for the backplane of a Distributed I/O Tier crate. The general recommendation is to use a common CompactPCI Serial backplane (section 2.1). CompactPCI Serial was selected among many industrial modular electronics standards because it features a fully passive backplane and a robust connector targeting transportation applications. Being fully passive, the backplane enables the use of its lines as a set of single-ended or differential lanes for simple communication mechanisms like fast SPI or even direct I/O connections. The DI/OT crate does not make use of the CompactPCI Serial high-speed interconnects (PCIe/SATA/USB) specification, as it would be too complex for the radiation-exposed systems.

By selecting this default and standard approach for DI/OT crate, peripheral boards designed for a specific equipment group can be reused also by other groups. However, in case a particular application cannot benefit from the common CompactPCI Serial backplane (section 2.1), one can also design a custom application-specific backplane (section 0).

2.1 Common CompactPCI Serial backplane

Development by: BE-CO and external company

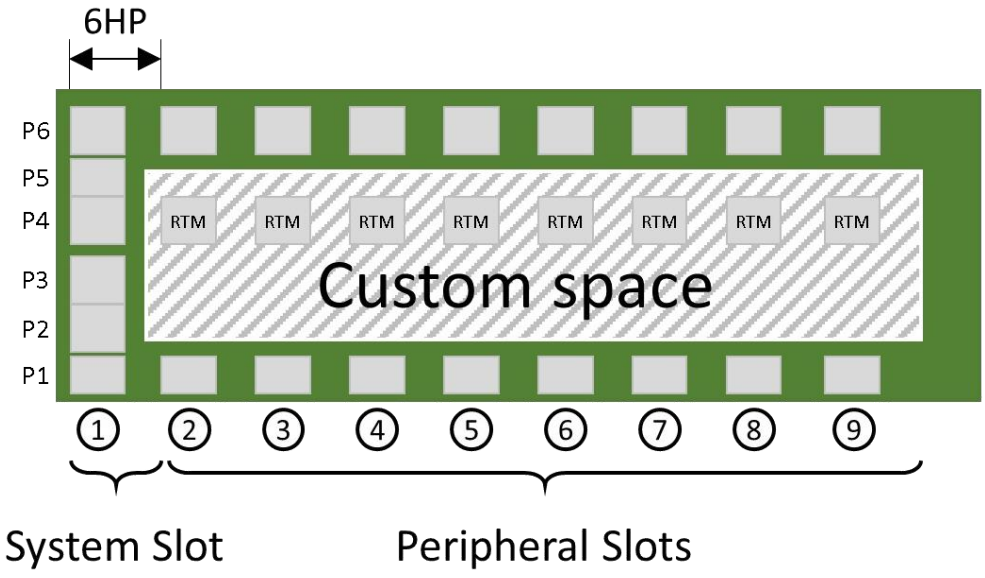

Figure 3: Common CompactPCI Serial DI/OT backplane (front view)

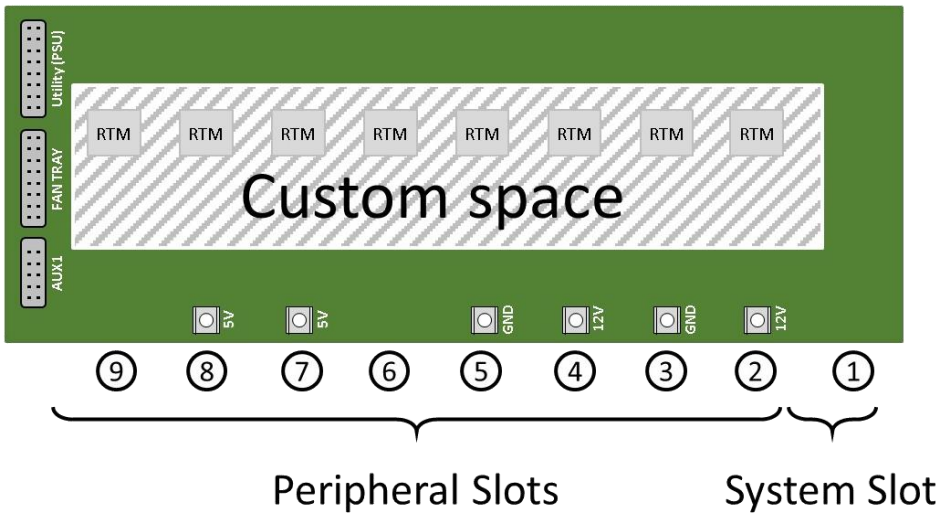

Figure 4: Common CompactPCI Serial DI/OT backplane (back view)

The backplane shall be designed and manufactured according to the CompactPCI Serial specification PICMG CPCI-S.0 [1], taking into account the following characteristics:

2.1.1 The backplane shall have 9 slots – 1 System Slot and 8 Peripheral Slots.

2.1.2 The System Slot shall be placed on the left side of the backplane.

2.1.3 The System Slot shall have a width of 6HP (~30mm). All Peripheral Slots shall have a width of 6HP.

2.1.4 All Peripheral Slots shall be populated with P1 (72-pin), P4 (RTM, 96-pin) and P6 (96-pin) Airmax connectors. P1 and P6 ensure communication with the System Slot, while P4 (RTM) provides additional connectivity with optional rear modules and the rest of the Peripheral Boards.

2.1.5 P6 connectors shall provide a single star topology between the System Slot and 8 Peripheral Slots.

2.1.6 To lower the cost of the backplane, only 16 differential lanes going from the System Slot to 8 Peripheral Slots (2 differential lanes per Peripheral Slot) are foreseen to handle high-speed communication (e.g. using MGT FPGA transceivers). They shall be routed accordingly to ensure

signal integrity. Designer is free to select which differential pairs going always to P1 of Peripheral Slots to route this way.

2.1.7 The 8 differential lanes going from the System Slot to 8 Peripheral Slots (*n_PE_CLK+/-* in rows 5 and 6 of connector P5 according to CPCI-S.0 standard [1]) shall provide low-noise distribution of high quality clocks to each of the Peripheral Boards.

2.1.8 All the rest of differential lanes will be used as fast SPI links or user-defined I/Os therefore their routing constraints can be relaxed to reduce the cost of the backplane (they will not carry Gbps transfer rates from gigabit FPGA transceivers).

2.1.9 All differential pairs going to a particular Peripheral Slot shall be length matched.

2.1.10 Geographical addressing signals (GA0-3) shall be grounded/open for each slot as defined in CPCI-S.0 standard [1].

2.1.11 All backplane signals not mentioned in this section shall be routed as specified in CPCI-S.0 standard [1].

2.1.12 The 11 signals of a System Slot connector that are defined as "general purpose I/O" (in Table 44 and Table 45 of PICMG CPCI-S.0 [1]), shall be connected to a set of IDC connectors (*Utility(PSU)*, *FAN TRAY*, *AUX* in Figure 4) in the back of the backplane. These lines will be used for wiring of the components required by crate diagnostics and monitoring (e.g. PMBus for PSU and fan tray monitoring).

2.1.13 The IDC connectors (*Utility(PSU)*, *FAN TRAY*, *AUX*) shall be equipped with latches to prevent lose contacts.

2.1.14 The pin assignment of the 11 "general purpose I/O" and their wiring to the IDC connectors shall be done according to Table 1.

Note: IDC connector *AUX* has no predefined function and therefore is reserved for any future needs.

IO pin	Name	IDC conn	IO pin	Name	IDC conn
P2-07A	*M_SCL*	*Utility(PSU), FANTRAY*	P2-07B	*M_SDA*	*Utility(PSU), FANTRAY*
P2-08B	*P_RST*	*Utility(PSU)*	P2-08C	*P_IO0*	*Utility(PSU)*
P2-07D	*P_IO1*	*Utility(PSU)*	P2-07E	*P_IO2*	*Utility(PSU)*
P2-07G	*F_RST*	*FANTRAY*	P2-07H	*F_IO0*	*FANTRAY*
P2-07J	*F_IO1*	*FANTRAY*	P2-07K	*C_IO0*	*AUX*
P2-08J	*C_IO1*	*AUX*	--	--	--

Table 1: System Slot "general purpose I/O" assignment

2.1.15 The full pinout of IDC connectors (*Utility*, *FANTRAY*, *AUX*) shall be done according to Table 2, Table 3 and Table 4.

2.1.16 The I^2C bus that is shared among all the backplane slots (backplane pins *IC_SCL, IC_SDA*) shall not be wired to the *Utility(PSU)* connector as defined by the CPCI-S.0 standard. Instead, the I^2C bus exposed through the *Utility(PSU)* connector (pins *M_SCL*, *M_SDA*) is driven directly by the System Board according to Table 1.

2.1.17 The backplane shall have a keep-out area between P1 and P6 connectors of the Peripheral Slots (marked with gray stripes in Figure 3 and Figure 4), where no routing of P1 and P6 signals shall be present – power and ground planes are allowed. If there is such a requirement, one can design a customized backplane by copying the layout of the default backplane (System Slot connections to P1 and P6 of all Peripheral Slots) and populating the "Custom space" with desired connectors and

signaling. The default version of this backplane makes use of the “Custom space” to host P4 connectors (marked *RTM* in Figure 3).

Note: the original idea of having a cutout for the whole “Custom space”, as described in the initial specification, was dropped as it would compromise the backplane stiffness. Metal supports cannot be fabricated with enough accuracy to prevent deformation and eventually connector damage.

2.1.18 The pin assignment of the Peripheral Slot P4 (RTM) connector shall be compliant with P4 connector in Table 47 and Table 48 of PICMG CPCI-S.0 [1] standard. The front P4 (RTM) connector (Figure 3) for each slot shall be wired to a mating Airmax connector in the back (Figure 4). Additionally, corresponding I/Os of raw 1 and 2 (16 signals) shall be connected between all Peripheral Slots. This way 16 busses are created that can be used either for board-to-board communication or distribution of auxiliary voltages.

2.1.19 The placement, dimensions and tolerance of the mounting holes shall be compliant with section 3.7.1 of the PICMG CPCI-S.0 specification [1].

2.1.20 Power (12V, 5V, GND) shall be provided to the backplane through power-bugs capable of carrying at least 300W on 12V rail and 10W on 5V rail – see Figure 4 for proposed power bugs layout.

Pin no.	Signal	Pin no.	Signal
1	*RTN_Sense*	2	*+5V*
3	*+12V_Sense*	4	*PS_ON#*
5	*PWRBTN#*	6	*PWR_FAIL#*
7	*WAKE_IN#*	8	*PRST#*
9	*M_SDA*	10	*M_SCL*
11	*P_RST*	12	*P_IO0*
13	*P_IO1*	14	*P_IO2*

Table 2: Utility(PSU) connector pinout

Pin no.	Signal	Pin no.	Signal
1	*GND*	2	*GND*
3	*F_RST*	4	*+12V*
5	*M_SCL*	6	*GND*
7	*+5V*	8	*+12V*
9	*M_SDA*	10	*GND*
11	*F_IO0*	12	*+12V*
13	*F_IO1*	14	*GND*
15	*GND*	16	*+12V*

Table 3: FANTRAY connector pinout

Pin no.	Signal	Pin no.	Signal
1	*GND*	2	*+5V*
3	*C_IO0*	4	*C_IO1*
5	*GND*	6	*+12V*

Table 4: AUX connector pinout

2.2 Custom application-specific backplane

Development by: Equipment groups

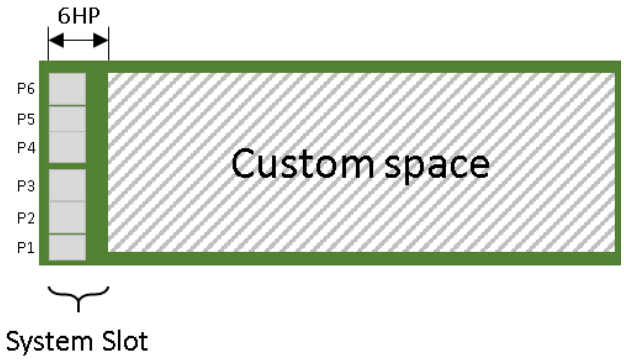

Figure 5: Custom DIOT backplane

A fully custom backplane may be designed for applications with constrains that cannot be fulfilled by the common DI/OT backplane. Such a custom backplane shall have the following characteristics for compatibility with the DI/OT crate mechanics:

2.2.1 The backplane shall have a System Slot made of P1 – P6 Airmax connectors and 6HP width, as specified in section 2.1 and Compact PCI Serial PICMG CPCI-S.0 [1] standard.

2.2.2 The backplane shall have a set of IDC connectors (*Utility(PSU)*, *FANTRAY*, *AUX*) as defined in section 2.1.

2.2.3 The backplane shall distribute +12V and +5V power from the main power supply to the System Slot and IDC connectors (*Utility(PSU)*, *FANTRAY*).

2.2.4 The backplane shall have mounting holes compatible with a common DI/OT backplane (section 2.1).

2.2.5 The backplane width shall not be more than 54 HP (including the System Slot) in case it has to fit in the crate mechanics as defined in section 4.

2.2.6 The rest of the backplane ("Custom space") can host any application-specific connectors and additional signal wiring. It can for example be used to distribute any non-standard auxiliary voltages to Peripheral Boards (e.g. for analog front-end) or to host I/O BNC connectors for external sensors/actuators.

3 Crate powering

3.1 Main power supply

Development by: BE-CO, R2E, TE-EPC (rad-tol variant)

The main power supply inputs 230V AC and produces +12V and +5V DC-DC switched voltage that is distributed over the main backplane (common CompactPCI Serial or custom application-specific) to a System Board and all Peripheral Boards (Figure 6). Each board produces locally, with low power DC-DC converters and/or LDOs the specific voltages that are needed for its operation.

In radiation-free applications an off-the-shelf 300W main power supply would be used while in radiation-exposed areas a custom rad-tolerant development will be done. Both types of the main power supplies shall meet the following characteristics:

3.1.1 Input voltage: 230V AC, 50Hz
3.1.2 Outputs: +12V, +5V
3.1.3 Output power for rad-tolerant variant: 10W (+5V), 100W (+12V)
3.1.4 Output power for off-the-shelf variant: 10W (+5V), 300W (+12V)
3.1.5 Ripple and noise: <100mVpp (+12V), <20mVpp (+5V)
3.1.6 Radiation tolerance (for rad-tolerant variant): ≥ 500Gy
3.1.7 Switching frequency: 250kHz – 1MHz
3.1.8 Physical dimensions: 100mm x 160mm x 37mm (8HP)
3.1.9 Cassette enclosure for high voltage separation and heat dissipation
3.1.10 PMBus monitoring interface (specified in section 8). In case of the rad-tolerant PSU, PMBus is implemented by the Monitoring Module (specified in section 8.2).
3.1.11 Current sharing line to enable operation in redundancy configuration
3.1.12 Remote On/Off switching
3.1.13 Connector: PwrBlade FCI 51939-667. The pinout compatible with the convention agreed among CompactPCI manufacturers (see Table 5).
3.1.14 The power supply plugs to a power backplane (section 3.2) which is a separate PCB connecting DC voltages and monitoring signals with cables to the main backplane.

P1	*P2*	*P3*	*P4*	*P5*	*D1*	*D2*	*D3*	*D4*	*D5*	*D6*	*P6*	*P7*	*P8*	*P9*
LINE	**NEUTRAL**	**GND**	**DC_IN**	**DC_RTN**	**N/A**	**PWR_FAIL**	**PRESENT**	**COM**	**DEG**	**+5V**	**COM**	**COM**	**+12V**	**+12V**
					C1	*C2*	*C3*	*C4*	*C5*	*C6*				
					N/A	**N/A**	**COM**	**A0**	**+5V**	**+5V**				
					B1	*B2*	*B3*	*B4*	*B5*	*B6*				
					N/A	**+12VCS**	**PS_ON**	**A1**	**SCL**	**COM**				
					A1	*A2*	*A3*	*A4*	*A5*	*A6*				
					N/A	**+12V_Sense**	**RTN_Sense**	**A2**	**SDA**	**ENABLE**				

Table 5: PwrBlade FCI 51939-667 power connector pinout

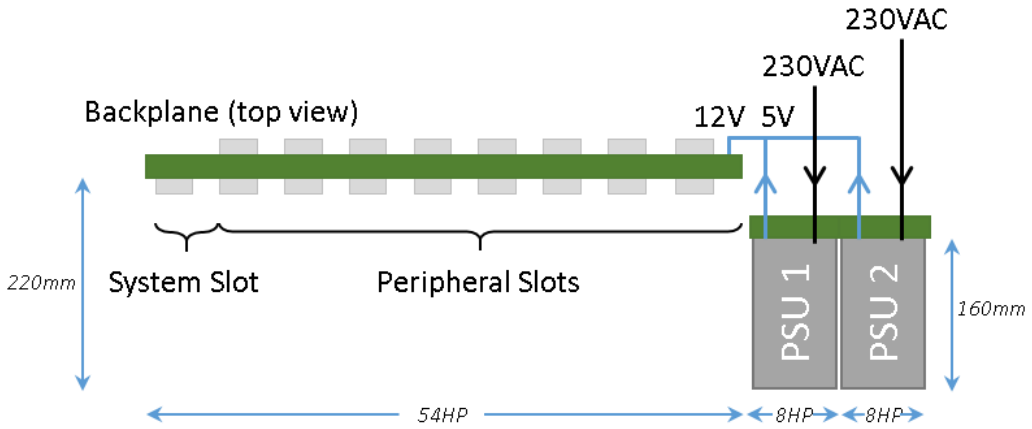

Figure 6: Main PSU powering scheme

3.2 Power backplane

Development by: BE-CO and external company or off-the-shelf product

The role of the power backplane is to interface between the main power supply and the main 3U backplane. The reason of having a power backplane separated from the main backplane is the difference in depth between the System and Peripheral boards (220mm) and the standard CompactPCI Serial power supplies (160mm) – please see section 4 for more details. It is also useful to have it as a separate module for more flexibility on crate mechanical assembly (only one power backplane can be mounted in case redundancy is not needed, power supplies can be placed in the back of the crate if required).

Figure 7: Off-the-shelf power backplane example (bottom and top side)

The power backplane shall meet the following characteristics:

3.2.1 The backplane shall use FCI 51940-473 power connector (receptacle for FCI 51939-667) to interface with the main DI/OT power supply (section 3.1)

3.2.2 The pinout of FCI 51940-473 shall be consistent with the convention agreed among CompactPCI manufacturers (see Table 5).

3.2.3 The 230V AC FASTON terminals of the power connector shall be accessible through a hole in the backplane (Figure 7) to ensure no high voltage signals are routed through the backplane. Moreover, this way no high voltage contacts are exposed (to avoid electrocution) when 230V FASTON plugs are isolated.

3.2.4 The backplane shall expose a utility connector with PSU monitoring signals (pinout according to Table 2) using an IDC connector with latches to prevent lose contact.

3.2.5 The backplane shall wire the signals of the utility connector to the FCI 51940-473 power connector according to Table 6.

3.2.6 The backplane shall expose +12V, +5V and GND rails using power-bugs.

3.2.7 The backplane shall be equipped with a DIP switch to configure addressing lines of the FCI power connector (pins C4, B4, A4). Each of these signals shall be connected to GND or floating depending on the DIP switch position.

Signal	Utility pin	FCI pin	Signal	Utility pin	FCI pin
RTN_Sense	1	A3	*+5V*	2	D6
+12V_Sense	3	A2	*PS_ON#*	4	B3
PWRBTN#	5	--	*PWR_FAIL#*	6	D2
WAKE_IN#	7	--	*PRST#*	8	--
M_SDA	9	A5	*M_SCL*	10	B5
P_RST	11	A1	*P_IO0*	12	B1
P_IO1	13	C1	*P_IO2*	14	D1

Table 6: Power backplane control signals wiring

3.3 Aux power supply

Developed by: Equipment groups

In the cases when a specific voltage cannot be produced locally on a Peripheral Board, one can also design and use an auxiliary power supply according to the following characteristics:

3.3.1 An aux power supply is highly recommended to be a specialized Peripheral Board or an RTM Board that inputs +12V from P1 backplane connector and produces required voltage levels on bus lines of P4 connector (see section 2.1) to be distributed to all Peripheral Boards (Figure 8).
Note: various designs (e.g. QPS electronics, DOROS system) have shown that a very clean voltage for analog front-end can be generated using a cascade of DC-DC regulator with one (ripple and noise < 5mVpp) or multiple LDOs (ripple and noise ~ 10µVpp). Please see [2] for measurement results of 2mVpp ripple on 5V power rail generated by the cascade: Traco AC/DC (TPP-40 105) →Murata DC/DC (MEJ2D0515SC) →Texas Instr.LDO (TPS7A49)

3.3.2 In the case where 6HP is not sufficient, an aux power supply can be a cassette occupying several peripheral slots, e.g. to host a linear power supply with a 50Hz transformer. In such case the Aux PSU cassette would directly input 230V AC, produce auxiliary voltages with a linear regulator and forward 230V AC to the main PSU (Figure 9).

3.3.3 The distribution of auxiliary voltages is done over P4 connector of a common backplane (section 2.1) or in a fully custom backplane (section 0).

3.3.4 Aux voltages are distributed only to peripheral boards, system slot does not receive them.

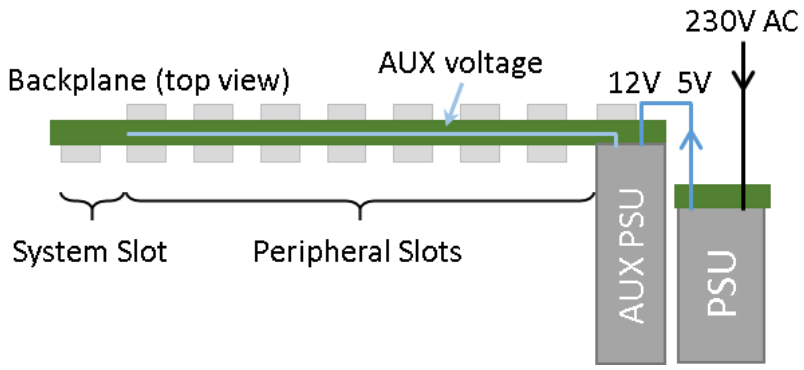

Figure 8: Powering scheme with Aux PSU

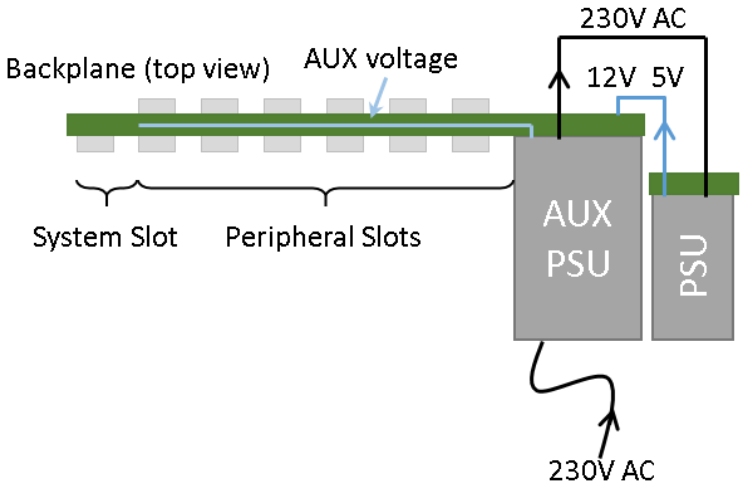

Figure 9: Powering scheme with aux linear PSU

4 3U Chassis mechanics

Developed by: BE-CO with equipment groups and external company

To cover the requirements of various systems the chassis is modular and consists of:

- 3U CompactPCI Serial crate assembled from a standard 3U sub-rack components (available from various crate manufacturers and through CERN stores). It hosts the main backplane (described in 2.1), two power backplanes (described in 3.2), and a front panel (described in 4.2).
- Optional 1U fan tray, which can be mounted below or on top of the main chassis (described in section 5).

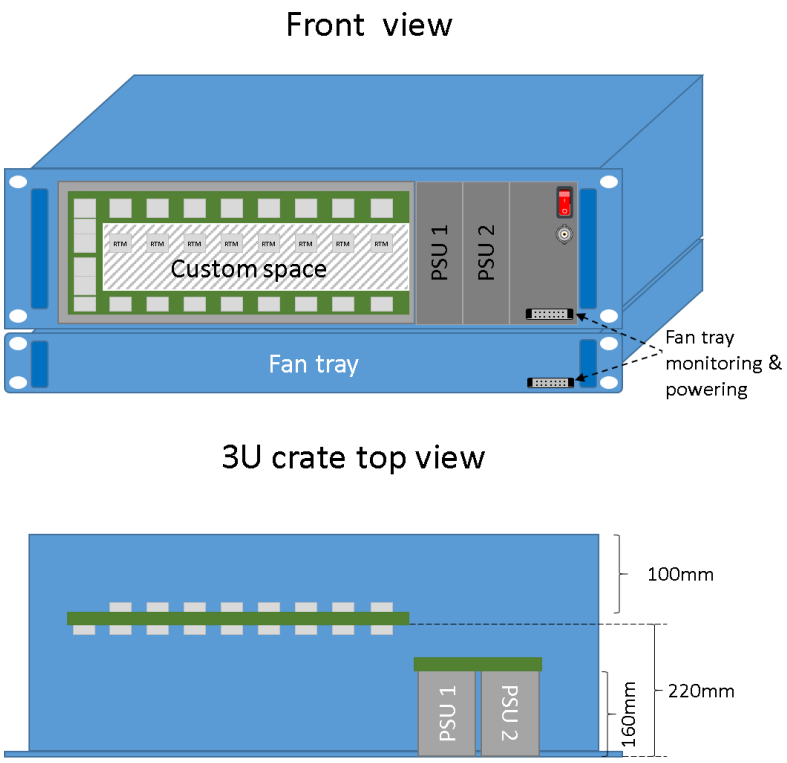

Figure 10: DIOT crate and fan tray mockup

4.1 Main 3U crate

The main 3U crate shall be compliant with the following characteristics:

4.1.1 Height shall be 3U (3 rack units)

4.1.2 Width shall be 19” with 84 HP (horizontal pitch) usable space.

4.1.3 The crate shall be equipped with rack mounting holes and front handles

4.1.4 The crate shall be equipped with 2 power backplanes (as defined in section 3.2) to host two main power supplies (section 3.1) in a load sharing redundancy configuration – a current sharing signaling cable shall be connected between the two power backplanes.

4.1.5 Both power supply slots shall be placed on the right side of the main backplane (PSU1, PSU2 in Figure 10).

4.1.6 The crate shall have perforated bottom and top covers to allow better airflow.

4.1.7 The crate shall be prepared to host the common CompactPCI Serial backplane (section 2.1) – power and signaling cabling, and backplane mounting holes shall be placed accordingly.

4.1.8 The crate shall host front boards (System Board and Peripheral Boards) which are 220mm long. Therefore the backplane needs to be mounted 60mm deeper than in regular CPCIs crates.

4.1.9 Each slot of the crate shall have a width of 6HP. Card guide rails shall be mounted accordingly.

4.1.10 220mm card guide rails according to IEEE 1101.10 shall be used. For the System Slot (slot 1) red guide rail shall be used (e.g. Schroff P/N 64560-091), while for all Peripheral Slots (slot 2-9) gray guide rails shall be used (e.g. Schroff P/N 64560-092).

4.1.11 The crate shall leave 100mm of rear space behind the backplane for optional rear transition modules or an expansion backplane.

4.1.12 The crate shall provide mechanical mounting and cabling of the monitoring components specified in section 8.
4.1.13 The crate shall mount and connect the front panel as defined in section 4.2.
4.1.14 The *Utility*(*PSU)* connector of the main backplane shall be connected using a ribbon cable with Utility connectors of both power backplanes (Figure 12).
4.1.15 230V AC IEC power entry socket with a fuse and EMC filter shall be placed in the back of the crate and wired with FASTON terminals to both power backplanes.
4.1.16 The cabling of the crate shall be done according to wiring diagram in Figure 12.
4.1.17 All outer covers of the crate (top, bottom, left, right, front, back) shall be powder coated with color RAL XXXX (**TBD**).

4.2 Front panel

Figure 11: Front panel mockup

The front panel module (Figure 11) shall be compliant with the following characteristics:

4.2.1 The front panel shall be installed on the right side of the crate, next to the power supplies (Figure 10) and have a width of 14HP to cover all the remaining front space.
4.2.2 The front panel shall host an on/off power switch, BNC connector for external power cycling and a fan tray connector.
4.2.3 The fan tray connector shall be a 16-pin IDC with latches preventing accidental removal (e.g. 3M 3000 Series). It shall be connected through a ribbon cable to the fan connector in the main backplane (pinout specified in Table 3).
4.2.4 The BNC connector can optionally input an external signal (5V TTL, active high) that is used for power cycling the crate. It shall drive a relay connected in series with the power button to break on request the 230V AC power going to the power supplies.
4.2.5 The aforementioned components shall be placed on a PCB screwed to the metal plate of the front panel to ensure proper and reliable mounting.

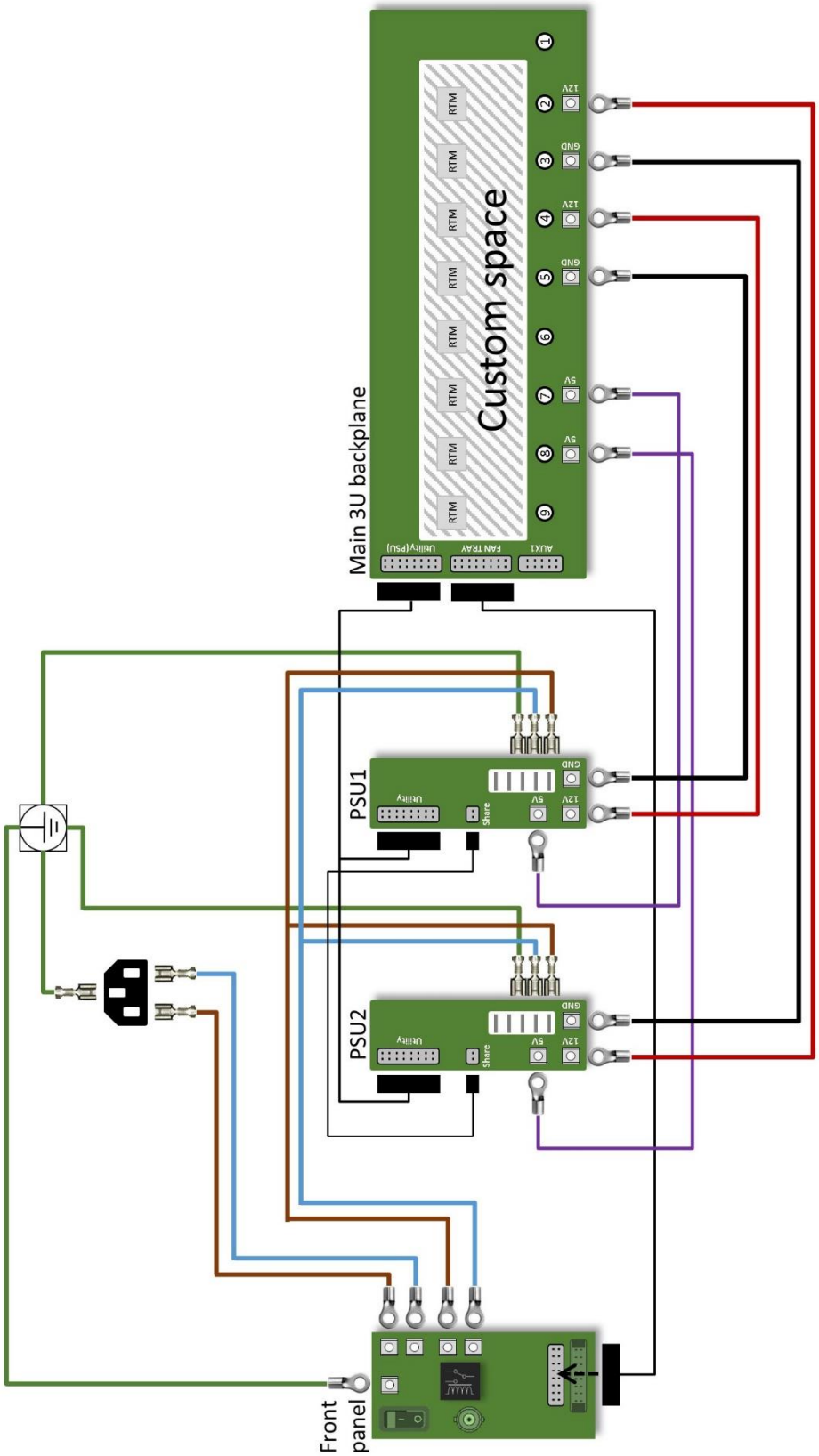

Figure 12: DI/OT crate wiring diagram (back view of the front panel and backplanes)

5 Fan tray

Developed by: BE-CO with equipment groups or off-the-shelf fan tray

The fan tray is an additional module to the main 3U CompactPCI Serial crate. It could be placed in the rack, below or above the 3U crate for systems that require better heat dissipation (e.g. deployed in radiation-free areas). Either an off-the-shelf 12VDC powered or a custom made fan tray can be used. The custom made fan tray shall contain BLDC fans, temperature sensors and a monitoring module (the same one used for power supply monitoring) and should meet the following requirements:

5.1.1 The fan tray's height shall be 1U (1 rack unit)

5.1.2 The fan tray's width shall be 19".

5.1.3 The fan tray shall be equipped with rack mounting holes and front handles

5.1.4 The placement of fans inside the fan tray shall be such to provide air flow for all the front cards and the power supplies.

5.1.5 The fan tray shall receive power and control signals through a 16-pin IDC connector (with latches to prevent accidental removal) from the main 3U chassis. The fans inside the fan tray shall be powered from +12V and the monitoring module from +5V. There is no additional power supply mounted inside the fan tray.

5.1.6 The fan tray shall draw not more than 36W from the +12V power provided by the IDC connector.
Note: The IDC connector can carry max 1A per-pin. Current pinout of the connector (Table 3) dedicates 4 pins to provide +12V power.

5.1.7 The fan tray shall host a monitoring module (the same one as used for power supply monitoring, see section 8.2 for details) that communicates with the System Board of a 3U crate over PMBus interface.

5.1.8 The pinout of the front connector of the fan tray shall be identical to that of the IDC connector exposed on the front panel of the main 3U crate (see Table 3).

5.1.9 The fan tray shall feature a fully passive board hosting a front IDC connector, fan connectors and pin headers to plug the monitoring module.

5.1.10 The fan tray shall ensure air flow at the level of 360 CFM (three fans each providing 120 CFM) - **TBD** further simulations are ongoing.
Note: This is based on DI/OT proof of concept off-the-shelf crate. Thermal simulations to be done, to determine what's the sufficient minimum air flow, especially that in radiation-exposed areas the main power supply can provide 100W total power (comparing to 300W outside radiation).

6 System Board

Developed by: BE-CO with equipment groups

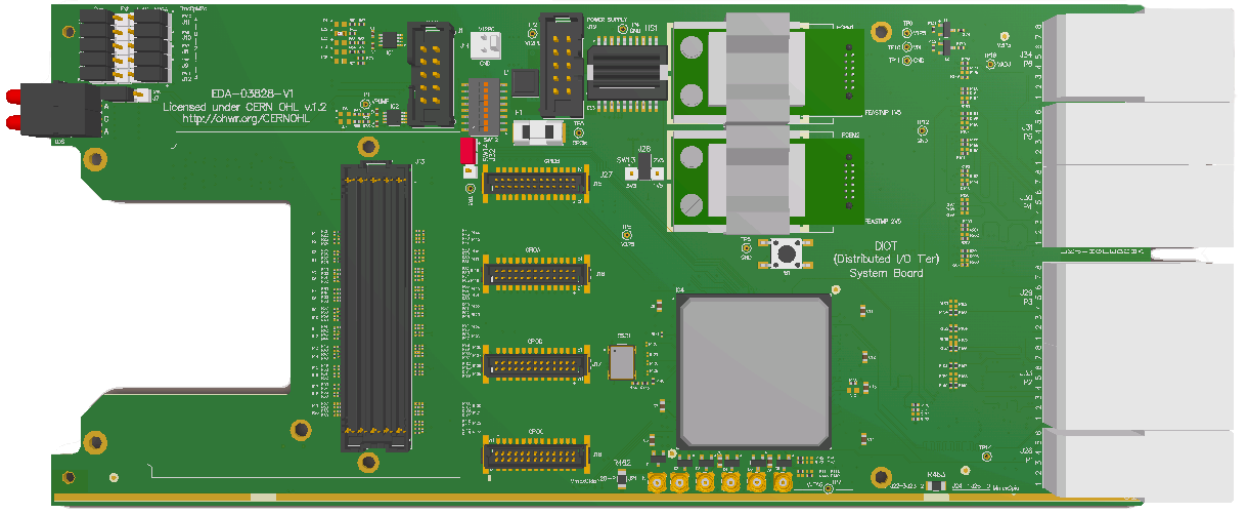

Figure 13: DI/OT System Board example

A common Distributed I/O Tier System Board (Figure 13) is a main FPGA-based board in the DI/OT crate. It is a main crate controller that communicates with application-specific peripheral boards, fieldbus mezzanine and is responsible for crate monitoring. The project foresees a design of two variants of the system board (radiation-tolerant and non-radiation-tolerant) of the following characteristics:

6.1.1 The board's dimensions are 100mm x 220mm x ≤ 6HP

6.1.2 The board shall be equipped with an LPC FMC connector to host a communication mezzanine

6.1.3 In addition to point 6.1.2, the non-radiation-tolerant variant of the system board shall connect 3 of the HPC gigabit transceiver interfaces to the FPGA to support in total 4 high speed transceivers of a communication mezzanine.

6.1.4 The FPGA selection for radiation-tolerant variant shall be made between a Flash-based FPGA (e.g. SmartFusion2) and a radiation-hard SRAM-based NanoXplore FPGA (NG-Medium).

6.1.5 The non-radiation-tolerant variant shall feature a System-on-Chip (e.g. Xilinx Zynq/Zynq Ultrascale).

6.1.6 The board shall have a set of 6 Airmax connectors (P1 – P6) to communicate with the DIOT backplane, following the CompactPCI Serial specification PICMG CPCI-S.0 [1] (see table below).

Designator	Rows	Pins	Walls	P/N
P1	6	72	4	10052825-101LF
P2, P3, P4	8	96	2	10052837-101LF
P5	6	72	2	10052824-101LF
P6	8	96	4	10052838-101LF

6.1.7 The pinout of P1 – P6 Airmax connectors shall be compatible with CompactPCI Serial specification PICMG CPCI-S.0 [1], with the difference that all the PCIe, USB, SATA, Ethernet lanes are used as a

general purpose differential lanes for simple communication with peripheral boards (e.g. using fast SPI or direct I/O connections).

6.1.8 The system board shall produce locally, using DC-DC converters and LDOs, voltage levels required for the FPGA, FMC mezzanine and all other on-board components.

6.1.9 The FPGA of the System Board shall connect to the 11 general purpose I/O lines (“IO” signals in Table 44 and Table 45 of PICMG CPCI-S.0 [1]) to use it for various monitoring-related interfaces (e.g. PSUs PMBus, Fan tray monitoring) according to Table 1.

7 Peripheral Boards

Developed by: Equipment groups

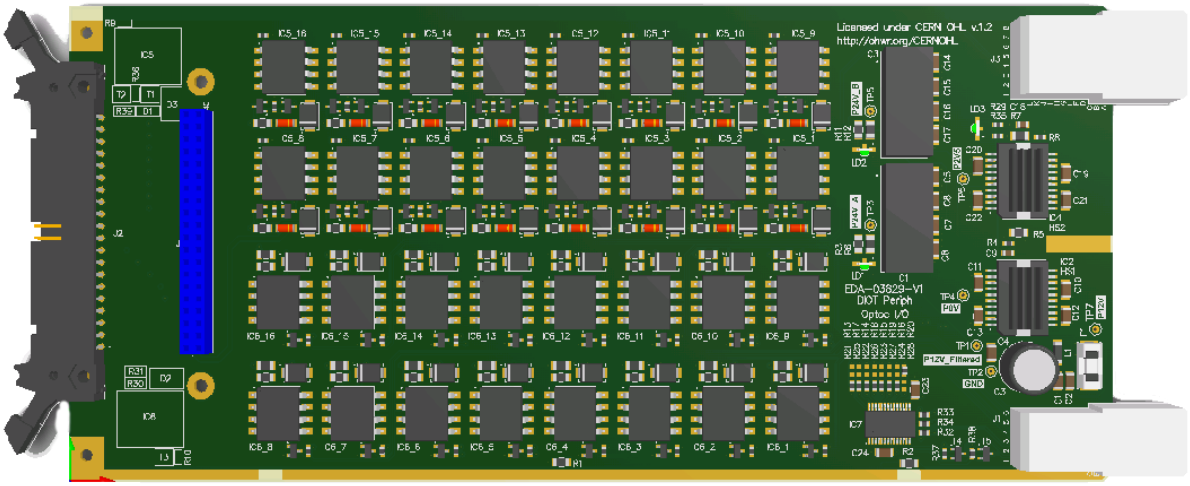

Figure 14: DI/OT Peripheral Board example

7.1.1 The board’s dimensions are 100mm x 220mm x ≤ 6HP

7.1.2 The board shall use P1 Airmax connector (see table in 6.1.6) to communicate with a system board over the common CompactPCI Serial backplane. Optionally, P6 Airmax connector can be used if more communication lanes are needed.

7.1.3 If a custom application-specific backplane is used, the selection of the connector for peripheral boards is up to the designer (e.g. DIN-type connectors can be used if needed).

7.1.4 The pinout of P1 (and optionally P6) Airmax connectors shall be compatible with CompactPCI Serial specification PICMG CPCI-S.0 [1] , with the difference that all the PCIe, USB, SATA, Ethernet lanes are used as a general purpose differential lanes for simple communication with peripheral boards (e.g. using fast SPI or direct I/O connections).

7.1.5 The board receives through P1 connector +12V (main power rail) and +5V (low power standby rail) and should produce locally (using DC-DC or LDO) the voltages required to its operation. Alternatively, auxiliary voltages (e.g. for analog frontend) can be provided through the P4 (RTM) connector (see section 2.1).

7.1.6 If additional shielding is needed (e.g. for an analog front-end), a peripheral board can be housed in a 3U cassette.

8 Crate monitoring

Developed by: BE-CO with Equipment groups

Monitoring of the DIOT crate is implemented in the main FPGA of the System Board and utilizes 11 general purpose I/O backplane lines to communicate with the power supplies and an optional fan tray. Following the PICMG CPCI-S.0 specification [1], the communication with these modules is based on the I^2C interface. According to the standard an I^2C System Management Bus is shared between the power supplies, fan tray, and all the peripheral boards. In the DIOT crate two separate I^2C busses are distinguished:

- I^2C System Management Bus – exposed on the utility connector (as defined in CPCI-S.0 standard), but connected to the System Slot using 2 of the general purpose I/O backplane lines (see *M_SCL*, *M_SDA* lines in Table 1). It is used to read monitoring quantities of the power supplies and the fan tray.
- I^2C Peripheral Bus – shared bus between the System Slot and all Peripheral Slots (utilizes *IC_SCL*, *IC_SDA* backplane lines). It is used to read board ID of each Peripheral Board for autodetection mechanism.

8.1 Monitored Quantities

In this section the measurements that comprise the readout part of the diagnostics are described.

8.1.1 For each main PSU, voltage and current monitoring for each of the power rails (12V / 5V) shall be provided, along with one temperature (might be worth it to put more, one ambient and two major loads, **TBD**) readout.

8.1.2 Multiple temperature sensors shall be supported by means of the monitoring modules in the PSU(s) and the optional fan tray. These may be mounted on the top or bottom grill, the backplane or in otherwise strategic locations, depending on the application.

8.1.3 Depending on the fan test results (**TBD**) the user may be able to monitor the speed of the fans in the optional fan tray and control the fan set-points.

8.2 Monitoring module

Developed by: BE-CO

A monitoring module shall be developed to provide PMBus (I^2C–based) monitoring and control for the PSU(s) and the fan tray. It shall be a small form-factor module (Figure 15) that can be mounted either on a motherboard or directly on a chassis.

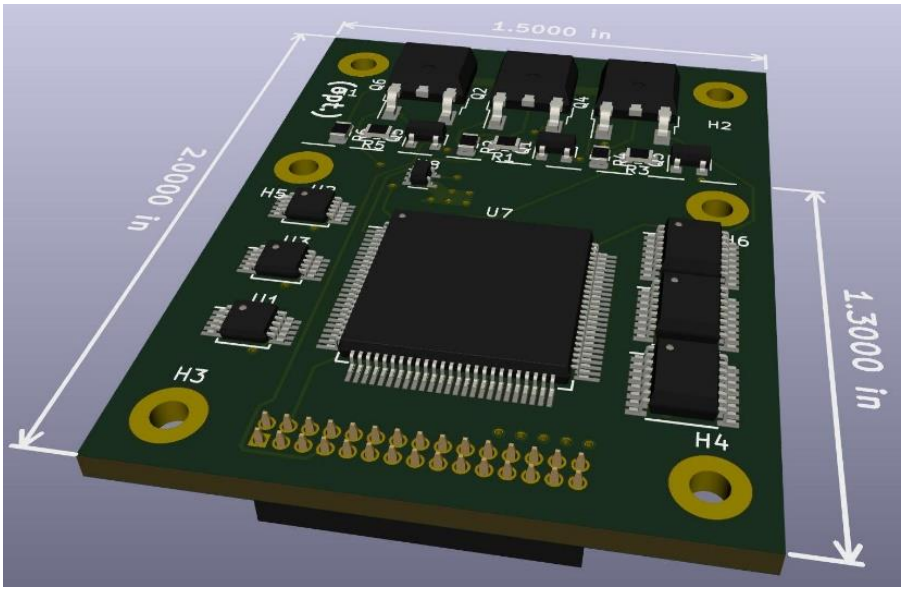

Figure 15: Mockup of the monitoring module

8.2.1 When driving fans, the module shall be powered by 12V and 5V power rails. When it is not driving any fans, supplying the 5V power rail will be enough (e.g. inside the PSU).

8.2.2 A reset signal shall be provided to the microcontroller in case a watchdog fails in radiation-exposed areas and it enters a fault condition (e.g. line *P_RST* in Table 2).

8.2.3 A subset of the PMBus protocol (specified in section 8.4) shall be used to interface with the monitoring module. Two pins shall be used to set the module's I^2C address.

8.2.4 Voltage and current monitoring of up to three power rails shall be supported.

8.2.5 Up to three temperature sensors of PT100/PT1000 type (or I^2C, **TBD**) shall be supported.

8.2.6 PWM control of up to three 12V fans shall be provided. Up to 1A of current shall be provided to each fan.

8.2.7 If the fans provide a dedicated PWM control pin, the power FET part of the module becomes redundant. Thus, a reduced-size version of the module may also be produced (notice the dashed line in Figure 15) or jumpers can be added to reroute the 12V so that the same board might be physically cut, **TBD**.

8.2.8 If the fans provide speed sense pins, speed measurements shall be also made available through the PMBus interface.

8.2.9 An SWD programming interface shall be provided through the main connector and through an on-board header connector.

8.2.10 Exact details of this module have to remain **TBD** for now (most probably it will feature ATSAMD21G18 microcontroller, radiation tests are ongoing).

8.3 Monitoring software services

8.3.1 CCS

8.3.2 COSMOS

8.3.3 Remote reprogramming framework

8.4 PMBus for DI/OT

9 Customization examples

This section lists examples how the common and modular DI/OT hardware kit can be customized for various applications.

9.1 BLM controller

Developed by: BE-BI

For a renovation of the LHC BLM system, the following customization of a DI/OT system is proposed:

9.1.1 Custom BLM backplane designed according to section 0. This custom backplane will host a common System Board, BLECF2 connector for a BLM acquisition card, 8 BNC connectors for BLM high voltage detectors, BLEIPU connector for auxiliary BLM power supply (Figure 16).

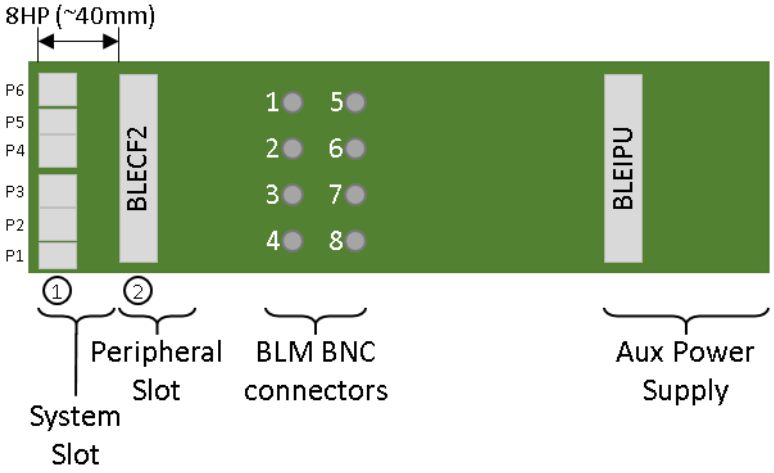

Figure 16: Custom BLM backplane proposal

9.1.2 BLEIPU used as an Aux Power Supply according to section 3.3 – it inputs 230V AC, produces with a transformer and a linear regulator clean voltage for a BLM analog front-end, and provides 230V AC to the main power supply (section 3.1). The auxiliary "clean" voltage produced by the BLEIPU is distributed to BLECF2 connector in the custom BLM backplane.

9.1.3 As an alternative to 9.1.2, BLEIPU can be a Peripheral Board generating required voltages for BLM analog front-end. The measurements documented in report [2] prove that BLM requirements for ripple and noise < 10mVpp on a 5V power rail can be satisfied with a cascade of DC-DC regulator and an LDO.

9.1.4 An optional fan tray defined in section 0 is installed on top of the main 3U chassis. Fan tray is powered and monitored from the main 3U chassis through a front panel connector (Figure 17).

9.1.5 Common System Board implements crate and PSU monitoring and any additional slow control needed. It uses a WorldFIP network (already deployed at the BLM locations in the tunnel) to communicate with higher layers of the control system. Optionally, the System Board can also implement an independent remote reprogramming channel for in-field, remote reconfiguration of an FPGA placed on BLECF2 board.

9.1.6 DI/OT 3U crate together with the fan tray can be placed in any standard 19" cabinet with any external 19" mechanical components that are required by the BLM system (air deflector, cables holder, etc.).

Figure 17: Customized BLM DI/OT setup proposal

10 References

[1] PICMG CompactPCI Serial (CPCI–S.0) Rev 2.0
https://www.picmg.org/openstandards/compactpci-serial/
(inside CERN only) https://wikis.cern.ch/download/attachments/103445302/PICMG%20CPCI-S.0.pdf

[2] Measurements of power supply ripple and noise for uQDS crate
https://wikis.cern.ch/download/attachments/103445337/UQDS_PSU_Ripple.pdf