

Copyright WUT ISE 2021.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Project/Equipment		DiPho_digital.PrjPcb	
Document		Designer	Piotr Daniel
 Faculty of Electronics and Information Technology <small>WARSAW UNIVERSITY OF TECHNOLOGY</small>		Drawn by	P. Daniel
		Check by	-
		Last Mod.	-
		File	DiPho_digital.SchDoc
Print Date		07.01.2023	12:04:20
Sheet		1 of 4	Rev. 1
WUT ISE		Contact	piotrmaciejdaniel@gmail.com

**DiPho digital**  
**top schematic**

A

B

C

D

E

A

B

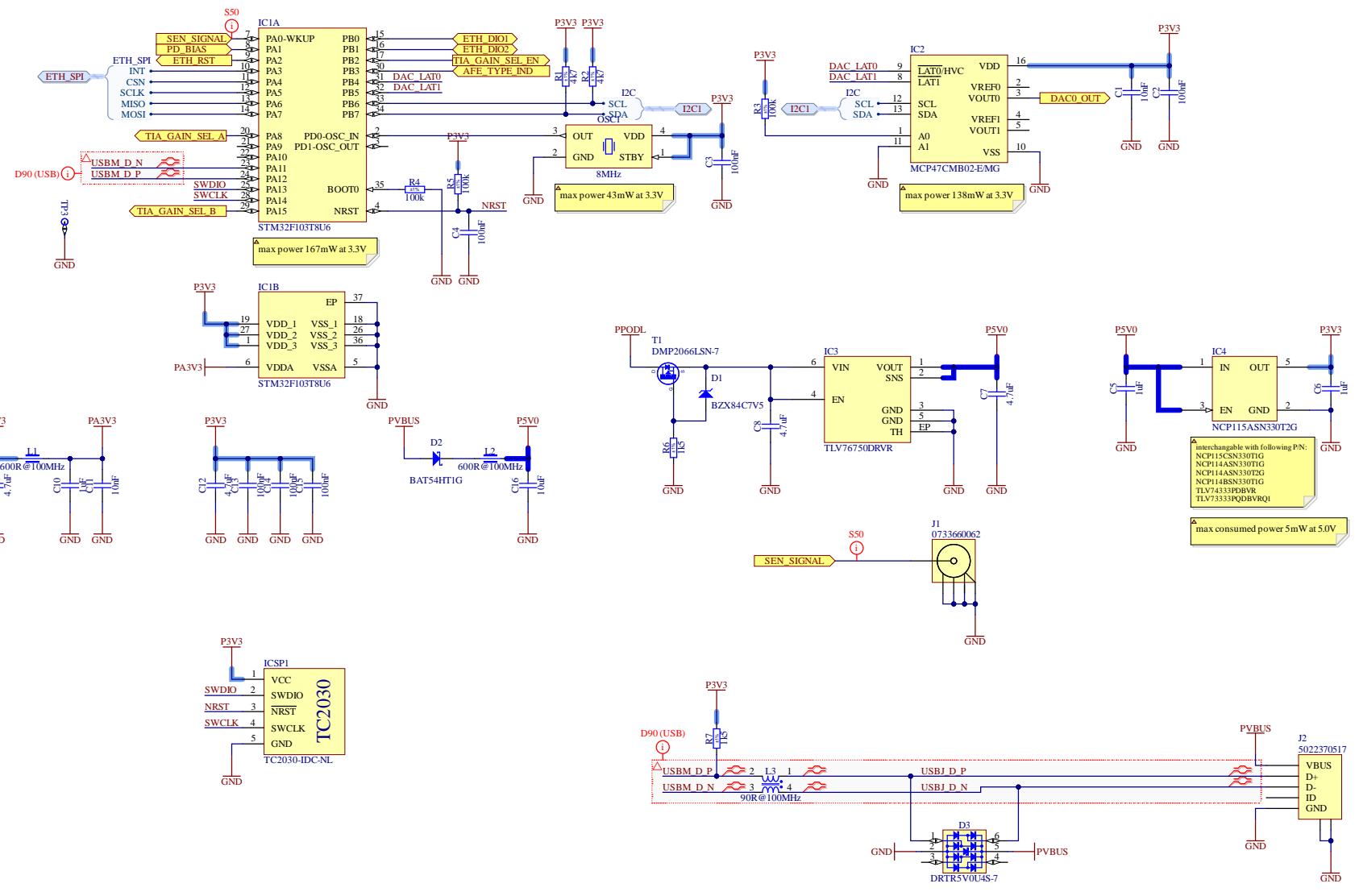
C

D

E

POWER BUDGET:									
RAIL	P3V3 R	P5V0 R	MCU	PHY	OTHER	AFE BOARD	TOTAL	CURRENT	
P3V3	n/a	n/a	210mW	258mW	143mW	15mW	626 mW	189.70mA	
P5V0	975mW	n/a	n/a	n/a	5mW	290mW	1270mW	254.00mA	
PPoDL 6V	n/a	1560mW	n/a	n/a	10mW	n/a	1570mW	261.67mA	
PPoDL 8V	n/a	2080mW	n/a	n/a	10mW	n/a	2090mW	261.25mA	

CURRENT REQUIREMENTS:									
RAIL	MINIMUM CURRENT								
P3V3	195mA								
P5V0	260mA								
PPoDL	270mA								



Copyright WUT ISE 2021.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohw.org/CERN/OHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Project/Equipment		DiPho_digital.PrjPcb	
Document		Designer: Piotr Daniel	
		Drawn by: P. Daniel	
		Check by: -	
		Last Mod.: -	
		File: mcu.SchDoc	
		Print Date: 07.01.2023 12:04:20	
		Sheet: 2 of 4	
		Rev: A3	
		Contact: piotrmaciejdaniel@gmail.com	



**DiPho digital**  
**MCU and IO**

WUT ISE

Contact: piotrmaciejdaniel@gmail.com

Sheet: 2 of 4

Rev: A3

A

B

C

D

E

A

B

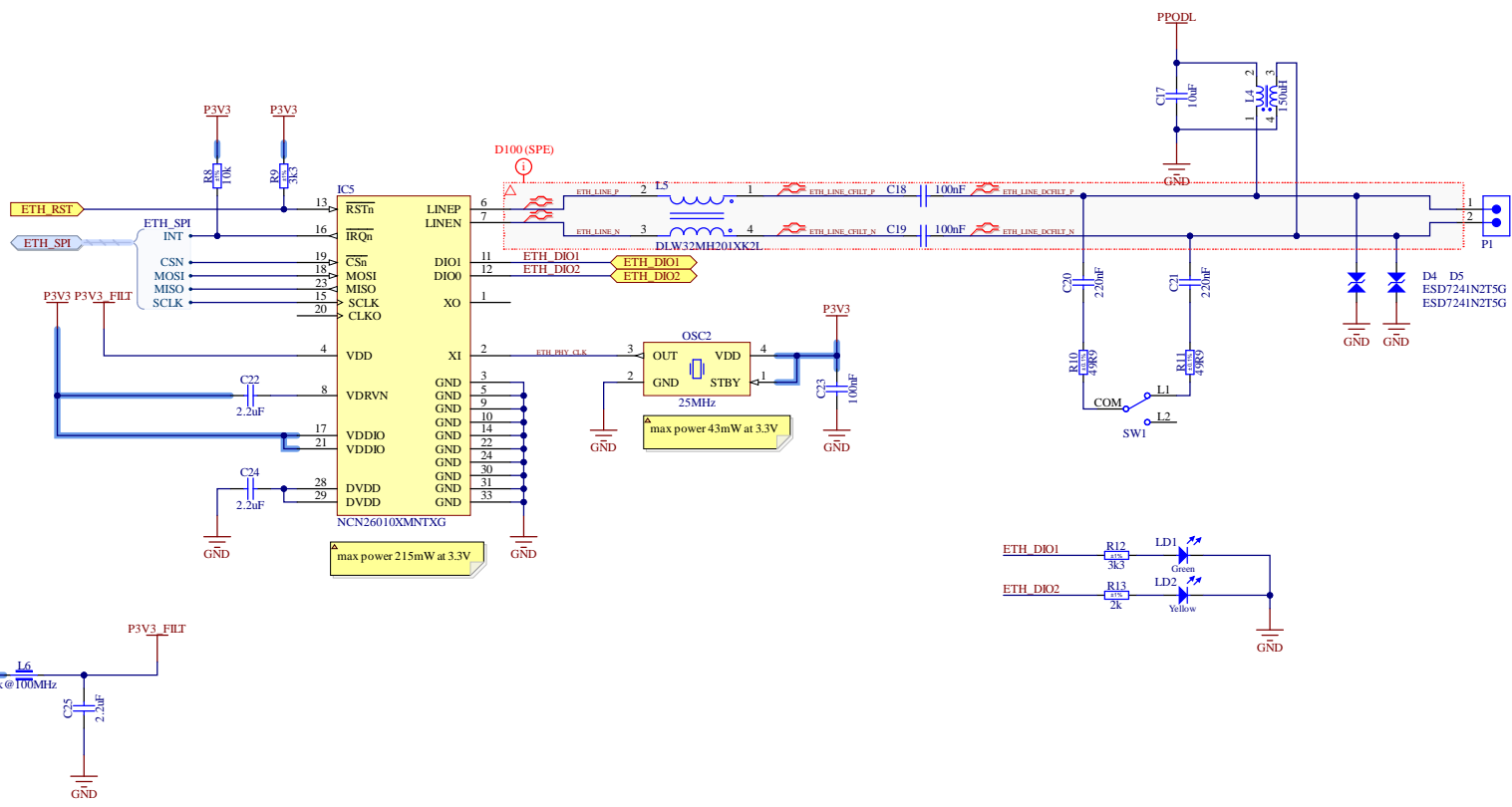
C

D

E

12345

12345

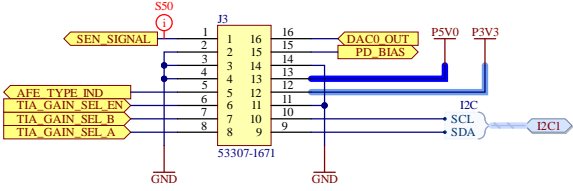


Copyright WUT ISE 2021.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Project/Equipment		DiPho_digital.PrjPcb	
Document		DiPho digital PHY schematic	
Designer		Piotr Daniel	10-12-2021
Drawn by		P. Daniel	10-12-2021
Check by		-	-
Last Mod.		-	23.12.2022
File		ethernet_SchDoc	-
Print Date		07.01.2023 12:04:21	-
Contact		piotrmaciejdaniel@gmail.com	Sheet 3 of 4
WUT ISE		-	Rev. 1





Copyright WUT ISE 2021.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Project/Equipment		DiPho_digital.PrjPcb	
Document		Designer	Piotr Daniel
 Faculty of Electronics and Information Technology <small>WARSAW UNIVERSITY OF TECHNOLOGY</small>		Drawn by	P. Daniel
		Check by	*
		Last Mod.	27.11.2022
		File	b2b_connector.SchDoc
		Print Date	07.01.2023 12:04:21
		Sheet	4 of 4
		Rev	1
		Contact	piotrmaciejdaniel@gmail.com

**DiPho digital**  
**b2b con schematic**

WUT ISE

