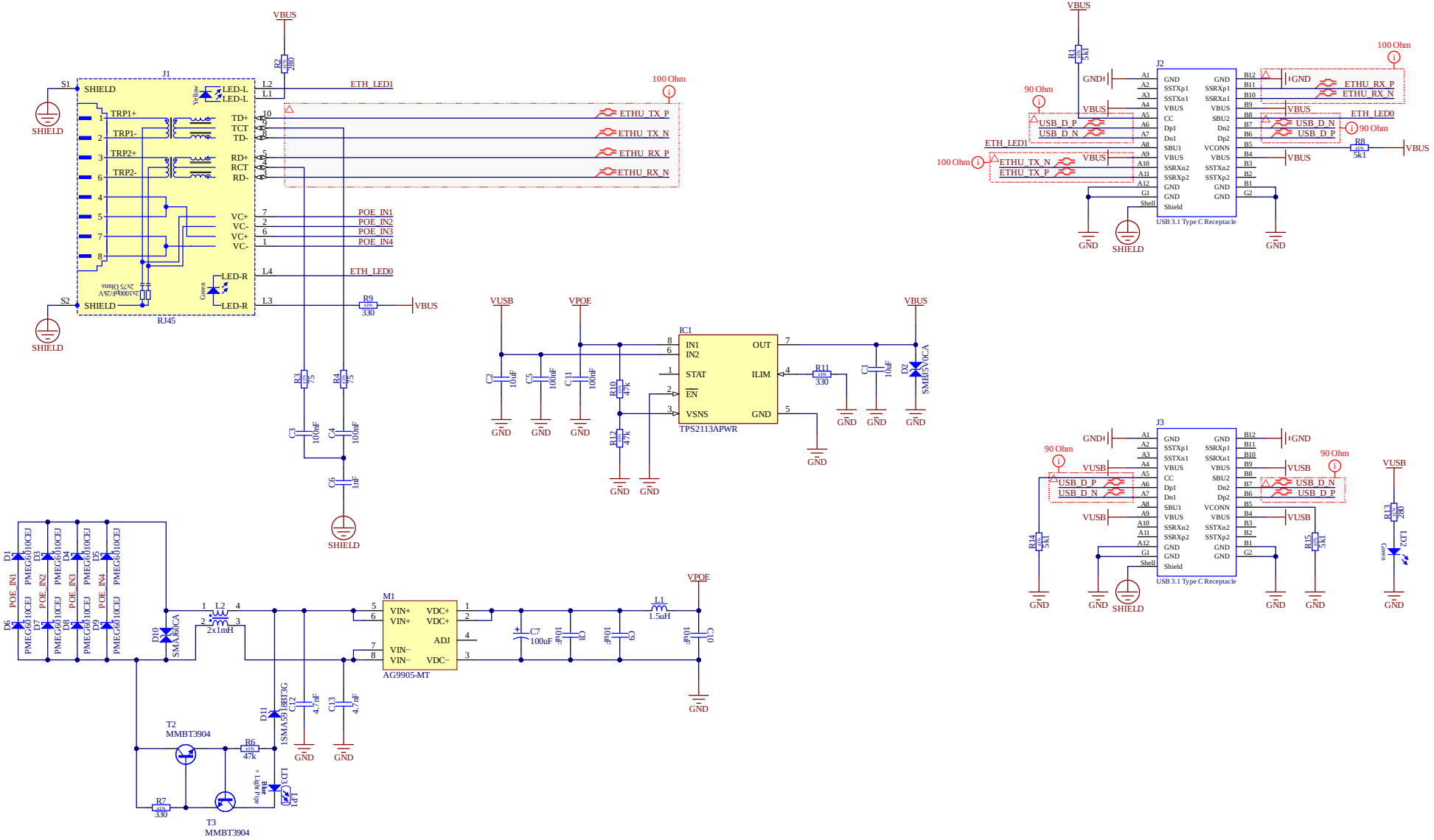

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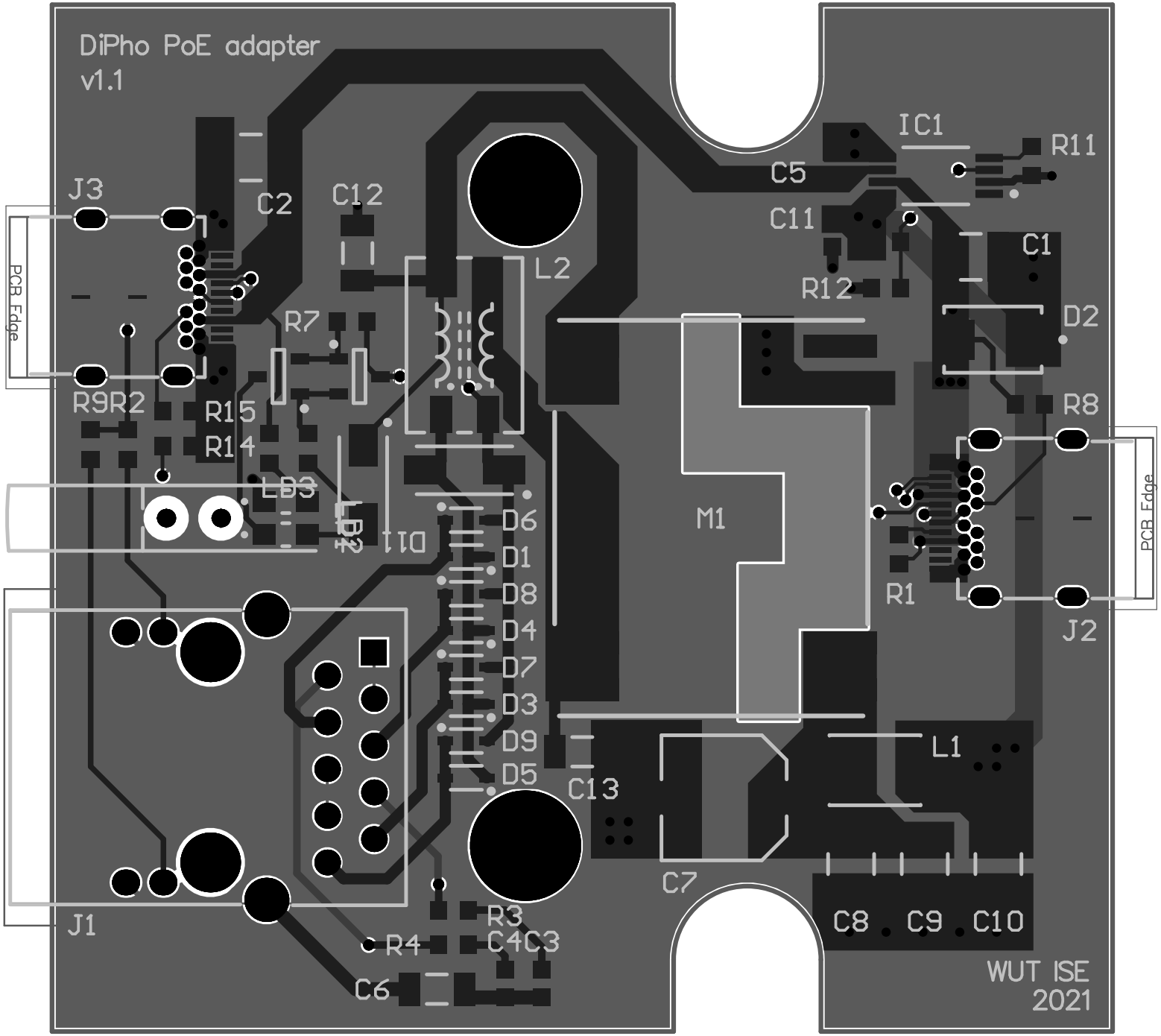
Project/Equipment	DiPho_PoE_adapter.PrjPcb		
Document	**DiPho adapter schematic**	Designer	Piotr Daniel
Faculty of Electronics and Information Technology, Warsaw University of Technology		Drawn by	P.Daniel 12.2021
		Check.by	-
		Last Mod.	- 30.01.2022
		File	DiPho_PoE_adapter.SchDoc
		Print Date	30.01.2022 17:31:06 Sheet 1 of 1
WUT ISE	Contact piotrmaciejdaniel@gmail.com	Size A3	Rev 1


DiPho PoE adapter
v1.1
J3
C2
C12
L2
IC1
R11
C5
C11
C1
R12
D2
R7
R9R2
R15
R14
R8
LD3
D2
D1
D6
D1
D8
D4
D7
D3
D9
D5
M1
R1
J2
PCB Edge
PCB Edge
L1
C13
C7
C8
C9
C10
J1
R4
R3
C4C3
C6
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