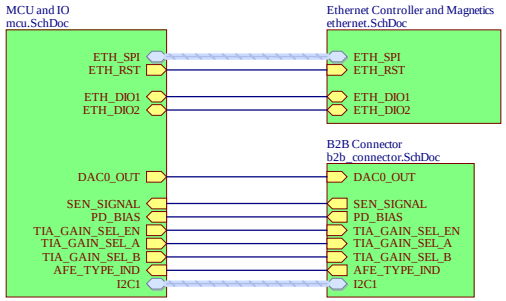


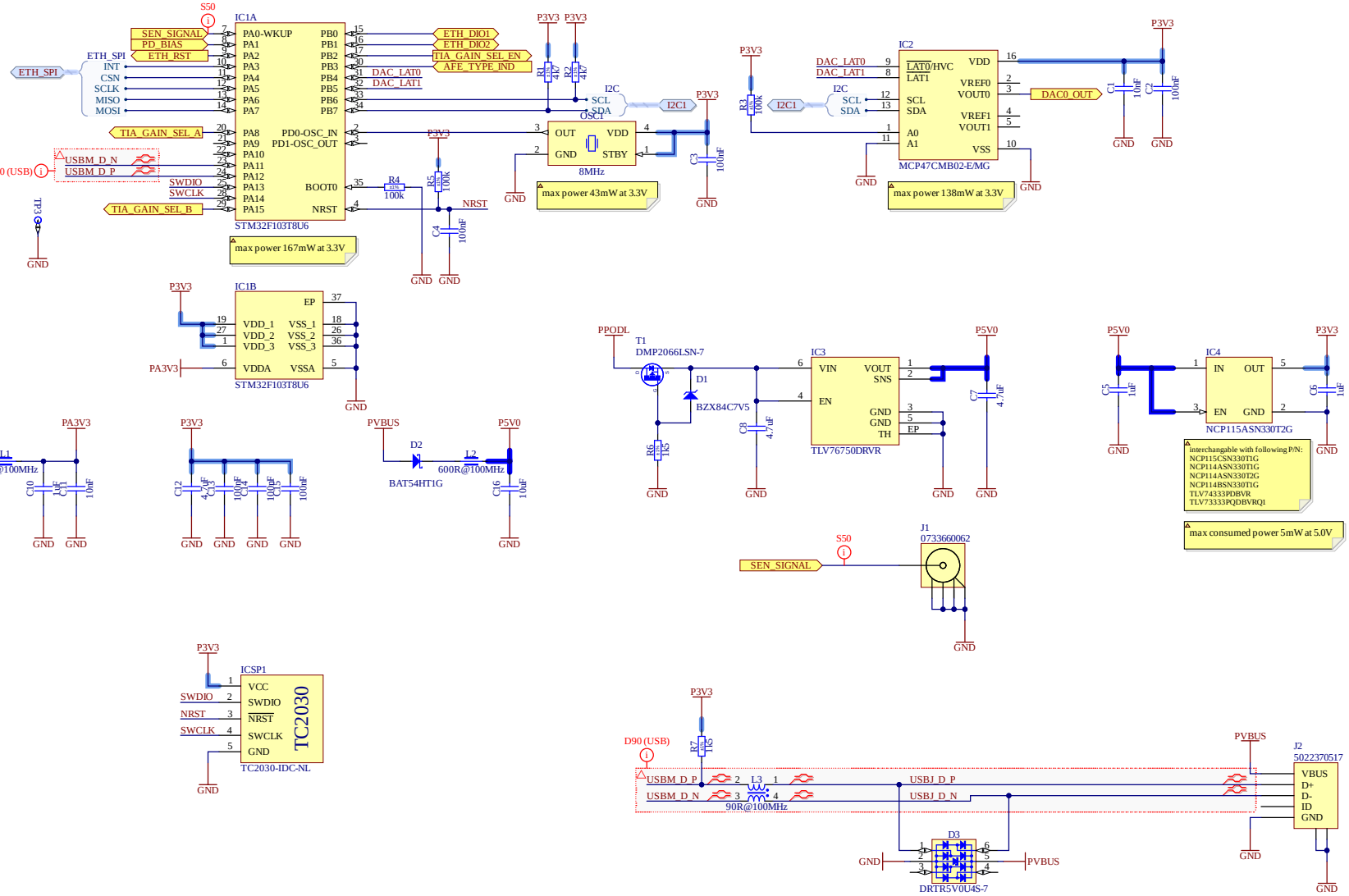
Project/Equipment	DiPho_digital.PrjPcb		
Document	**DiPho digital top schematic**	Designer	Piotr Daniel
		Drawn by	P. Daniel 10-12.2021
		Check.by	* -
		Last Mod.	- 27.11.2022
		File	DiPho_digital.SchDoc
		Print Date	07.01.2023 12:04:20 Sheet 1 of 4
Faculty of Electronics and Information Technology, Warsaw University of Technology	*WUT ISE*	Contact	piotrmaciejdaniel@gmail.com Size A3 Rev 1

POWER BUDGET:

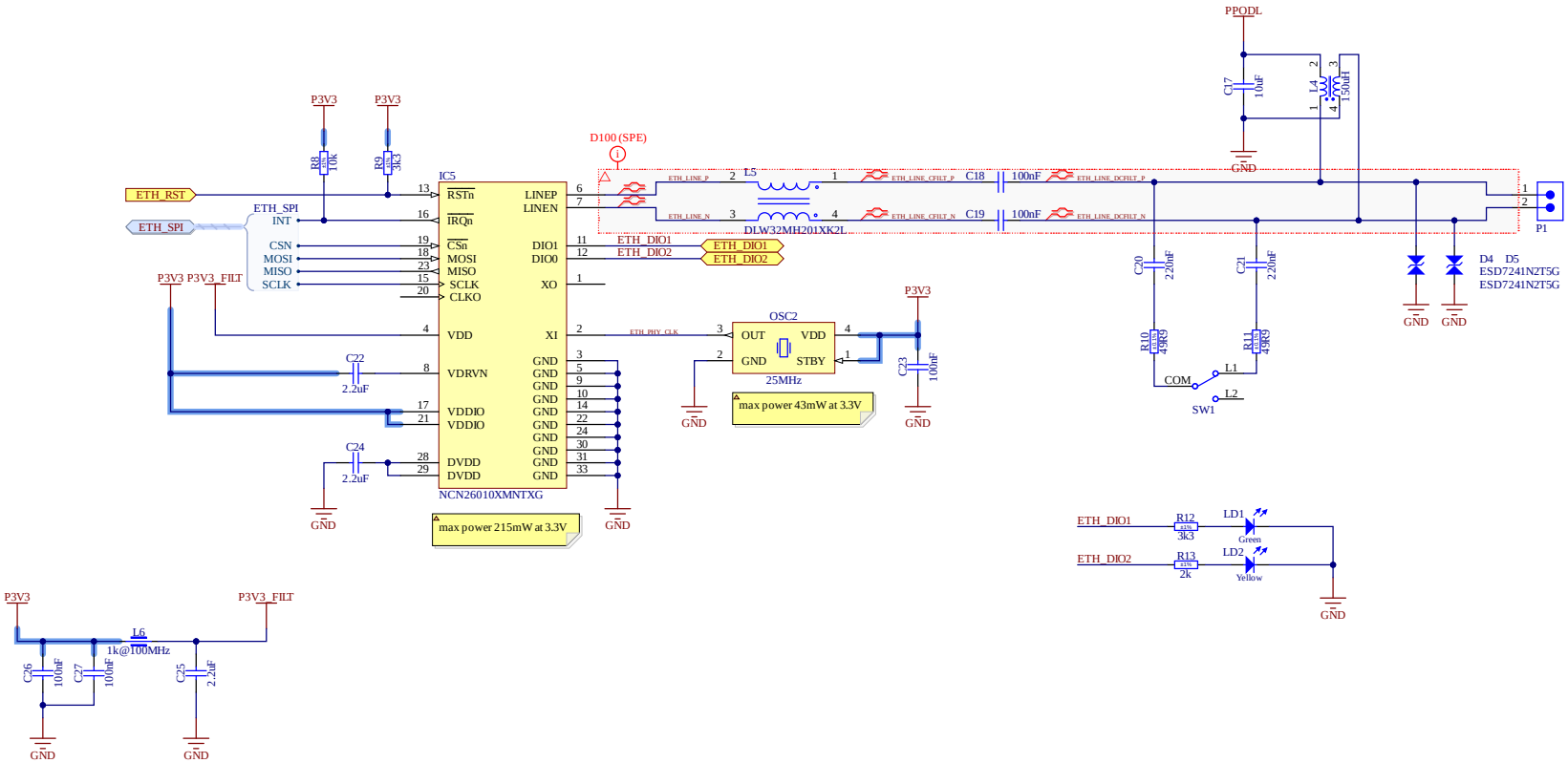
RAIL	P3V3 R	P5V0 R	MCU	PHY	OTHER	AFE BOARD	TOTAL	CURRENT
P3V3	n/a	n/a	210mW	258mW	143mW	15mW	626 mW	189.70mA
P5V0	975mW	n/a	n/a	n/a	5mW	290mW	1270mW	254.00mA
PPoDL 6V	n/a	1560mW	n/a	n/a	10mW	n/a	1570mW	261.67mA
PPoDL 8V	n/a	2080mW	n/a	n/a	10mW	n/a	2090mW	261.25mA

CURRENT REQUIREMENTS:

RAIL	MINIMUM CURRENT
P3V3	195mA
P5V0	260mA
PPoDL	270mA



Project/Equipment	DiPho_digital.PrjPcb
Document	
Faculty of Electronics and Information Technology, Warsaw University of Technology	**DiPho digital MCU and IO**
Designer	Piotr Daniel
Drawn by	P. Daniel 10-12.2021
Check.by	-
Last Mod.	- 27.11.2022
File	mcu.SchDoc
Print Date	07.01.2023 12:04:20
Sheet	2 of 4
WUT ISE	Contact piotrmaciejdaniel@gmail.com
Size	A3
Rev	1



Project/Equipment DiPho_digital.PrjPcb

Document

Faculty of Electronics and Information Technology
WARSAW UNIVERSITY OF TECHNOLOGY

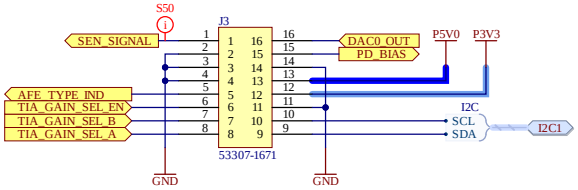
DiPho digital PHY schematic

Designer	Piotr Daniel	
Drawn by	P. Daniel	10-12.2021
Check.by		-
Last Mod.	-	23.12.2022
File	ethernet.SchDoc	
Print Date	07.01.2023 12:04:21	Sheet 3 of 4

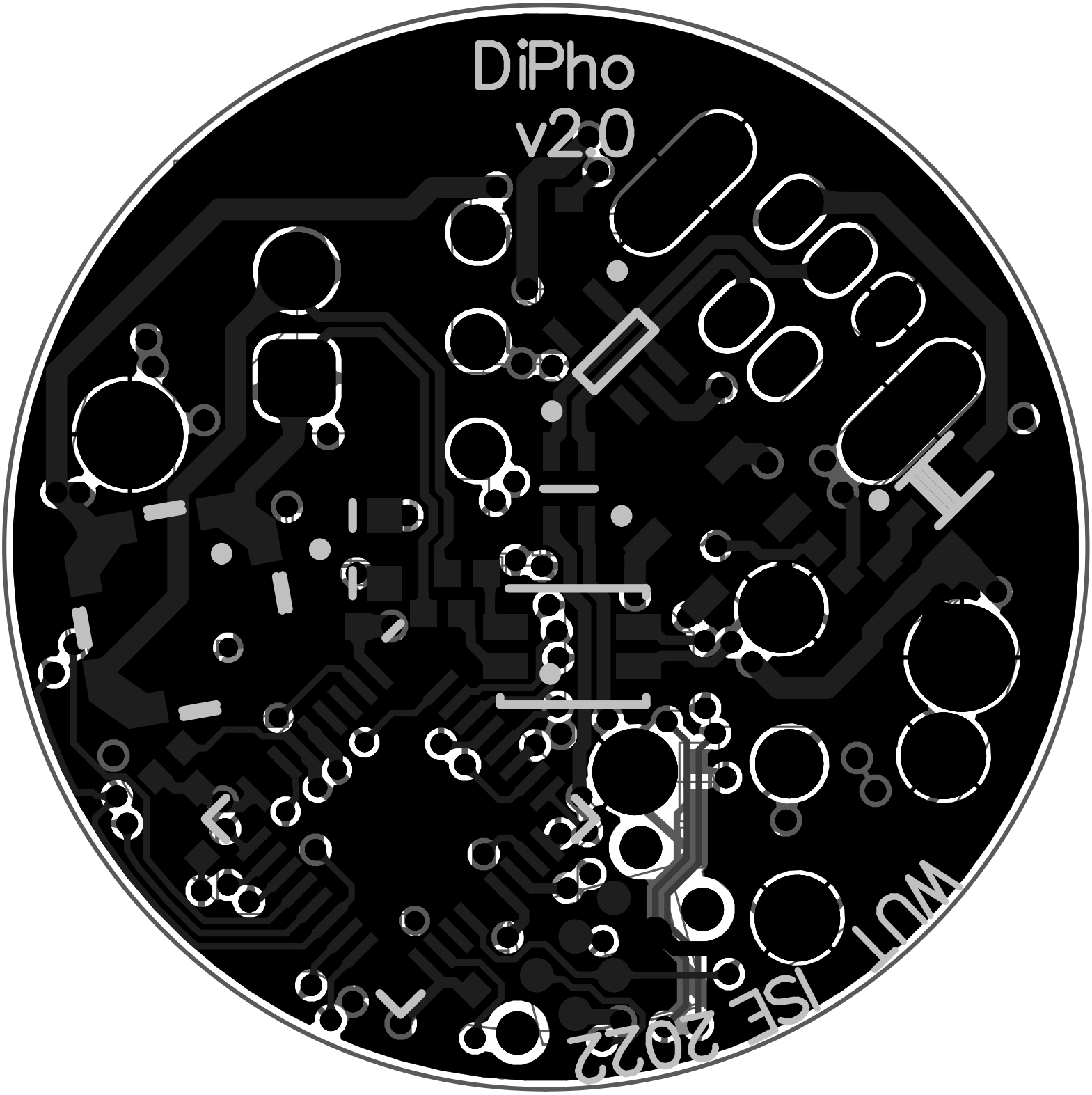
WUT ISE

Contact piotrmaciejdaniel@gmail.com

Size A3 | Rev 1



Project/Equipment	DiPho_digital.PrjPcb		
Document		Designer	Piotr Daniel
Faculty of Electronics and Information Technology, Warsaw University of Technology	**DiPho digital b2b con schematic**	Drawn by	P. Daniel 10-12.2021
		Check.by	*
		Last Mod.	27.11.2022
		File	b2b_connector.SchDoc
		Print Date	07.01.2023 12:04:21 Sheet 4 of 4
WUT ISE	Contact piotrmaciejdaniel@gmail.com	Size	A3
		Rev	1


DiPho
v2.0
WUT ISE 2022