Cheko: high-density electrode driver for scalable ion-trap quantum computing

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1 Background

Quantum computing experiments with trapped ions need an increasing number of electrodes when scaling up their number of qubits, for the purposes of ion shuttling (as required to implement many quantum gate schemes) and compensating stray electric fields (which decrease the fidelity of operations).

An example of an ion trap with a large number of electrodes is the NIST microfabricated "racetrack" ion trap[1], with 150 trapping zones, which was used to demonstrate transport of atomic ions between the legs of a 'Y'-type junction, as well as the use of a basic component design library that can be quickly assembled to form structures optimized for a particular experiment.
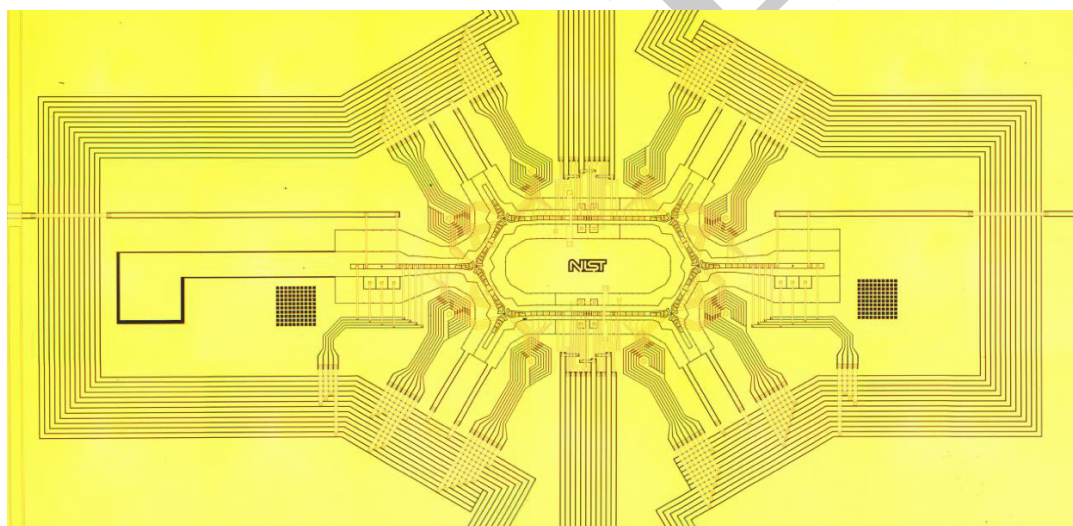

Figure 1: The "racetrack" ion trap, measuring a few millimeters. Credits: J.Amini/NIST

Ion traps operate in a ultra-high vacuum environment, while control signals originate from the laboratory at atmospheric pressure. Directly accessing all the electrodes from the ion trap from the laboratory requires electrical connections between vacuum and atmosphere sides ("vacuum feedthroughs"). They are costly and a potential source of vacuum leaks that cause malfunction of the entire apparatus requiring weeks or months of repair. Furthermore, cabling on both vacuum and atmosphere sides becomes difficult and a potential source of signal integrity problems. Due to all these issues, in the NIST racetrack[1] ion trap, only 48 electrical potentials could be controlled, with groups of the 150 electrodes sharing one potential. The authors nevertheless suggested repeating the hexagonal pattern of the structure as a way to scale the design to higher number of qubits – which would be problematic with typical vacuum chamber and control system design.

Transport waveforms for ions are commonly generated by a spline interpolator[2] using digital signal processing, and a CIC interpolator could also be used. The amount of bandwidth required to determine a spline waveform is much less than the bandwidth of the resulting waveform. Therefore, it can be seen as wasteful to consume expensive vacuum feedthrough bandwidth by transferring the "uncompressed" waveform instead of the more compact spline (or CIC) representation.

This document proposes moving the interpolator, DAC, and electrode driver closer to the ion trap, on the vacuum side, thereby optimizing use of the available vacuum feedthrough bandwidth and alleviating cabling issues. A new device, codenamed "Cheko", would be placed next to the trap electrodes, receive bandwidth-optimized digital control commands from an external control system in the laboratory, and drive the trap electrodes.

2   Architecture

A low-pin-count digital interface going over the vacuum feedthrough, exposing the Cheko devices to the external control system, carries commands that program the trap electrode voltages. A command consists in a timestamp, channel number, and interpolator data. Commands are buffered inside the device until their respective timestamps are reached, at which point the interpolator data is sent into the corresponding channel. The Cheko devices contain a timestamp counter and a means of synchronizing it with the external control system via a special command. The interpolator continuously generates high-bandwidth data for its DAC channel based on the received data. The interpolator is based on cascaded integrator-comb (CIC) filters. The output of the DAC is amplified to drive its trap electrode.

In order to save the maximum amount of pins, the master device is responsible for avoiding buffer overflows by keeping track of the buffer space available in Cheko devices and the timestamps issued, without the Cheko devices returning backpressure information. A simple status line is used to report errors such as violations of this scheme.

Several Cheko devices can be placed in one vacuum chamber, and share certain pins such as the electrical power supply pins, the clock signal, the status line, and even the data pins if an addressing scheme is implemented.
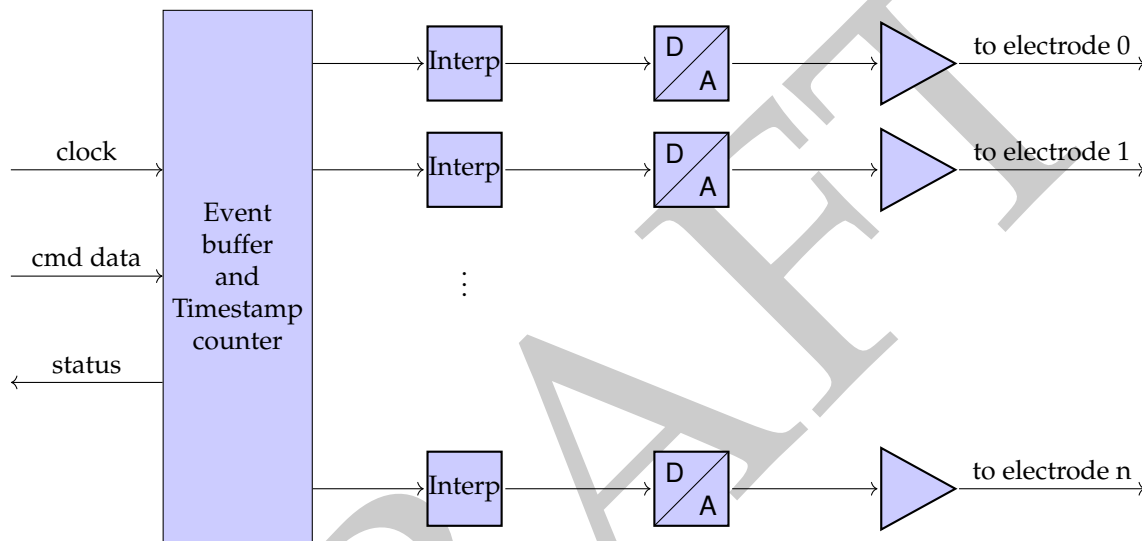

Figure 2: Block diagram of the Cheko device.

3   Specifications

3.1   Electrical

- Voltage: ± 5V to ± 10V. This is a requirement from the physics of surface ion traps.
- Permissible output capacitance: 5pF (TBC). The trap electrode and its connection to the driver are modeled by a capacitor.
- Sample rate: 10MHz to 100MHz.
- Slew rate: 100V$/\mu$s (TBC).
- Current drive capability: 500μA (TBC) per channel. Derived from permissible output capacitance and slew rate.
- Number of channels: 30 to 100.

3.2   Size

The electrode area of the racetrack ion trap[1] with its 150 regions only measures 2x4mm. For a scalable control system, the amount of space used by the electronics that drives these 150 regions must not be significantly larger; or wiring eventually becomes intractable again. From this, it becomes clear that custom ASIC technology is an interesting candidate. It will remain a challenging goal: as a ballpark estimate of the size required, the AD5592R 8-channel DAC is offered by Analog Devices in bare die form measuring 2x2mm. Nevertheless, even if a size of 2x4mm for 150 channels is not achieved, a miniature local electrode control system would be a significant improvement over the systems currently used.
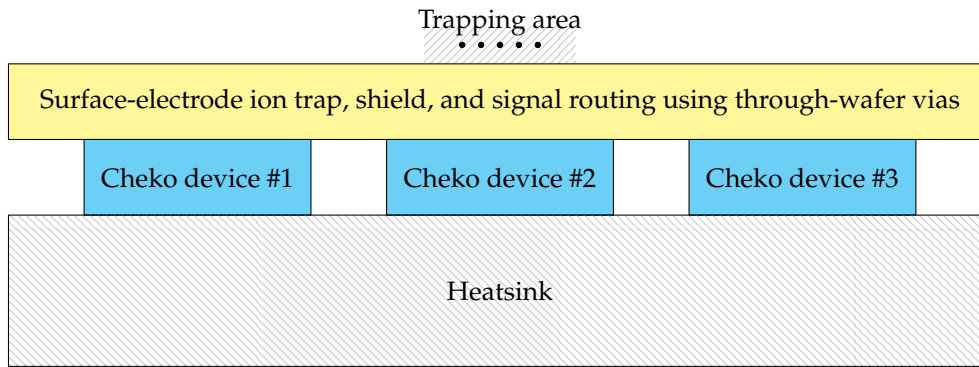
Trapping area

Figure 3: Cheko devices could be placed between the ion trap and a heatsink, using flip-chip mounting.

3.3 Temperature range

Some, but not all, ion trap experiments are done in a cryostat, in particular to reduce ion heating rates and improve vacuum[3] (in terms of both pumping speed and ultimate pressure achieved). To address a wider range of ion trap experiments, it is desirable that the device be operable at low temperatures (3 to 10K) as well as room temperature.

3.4 Vacuum

The device must be operable in a ultra-high vacuum environment. It must not outgas and must have a sufficient means of dissipating the heat it generates, such as being mounted to the wall of the vacuum chamber acting as heatsink.

4 Ecosystem and integration

Cheko will be compatible with the popular ARTIQ[4] control and data acquisition system, and will be part of the Sinara[5] hardware family. A simple interface module, in the EEM form factor, connects the digital signals of one or several Cheko devices to the FPGA of carrier cards such as Kasli or Kasli-SoC.
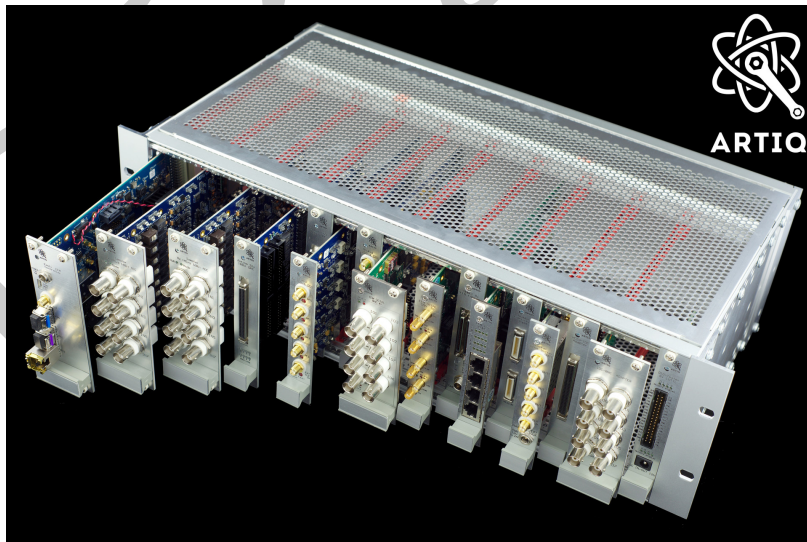

Figure 4: A Sinara crate with a Kasli FPGA carrier (left) and various modules in the EEM form factor.

Since Cheko devices already contain time-tracking logic, they operate as simplified DRTIO leaf nodes. RTIO commands originating from ARTIQ kernels are serialized by gateware inside the FPGA carrier card and transmitted to the Cheko devices via the EEM cable, adapter card, and cable between the vacuum chamber and the Sinara crate.

References

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[3] M. Niedermayr, R. Blatt. *Cryogenic surface ion traps.* Dissertation. `https://quantumoptics.at/images/publications/dissertation/niedermayr_diss.pdf`

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