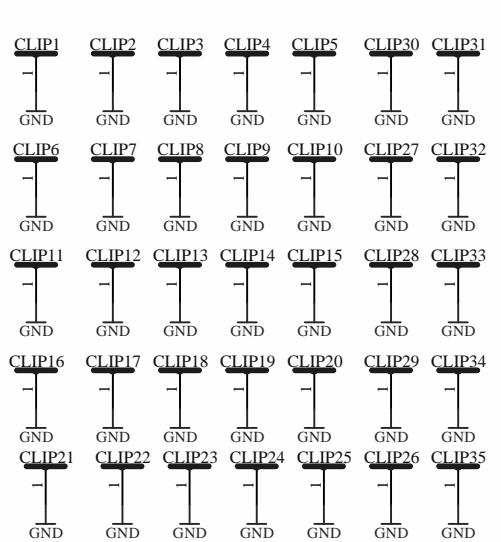
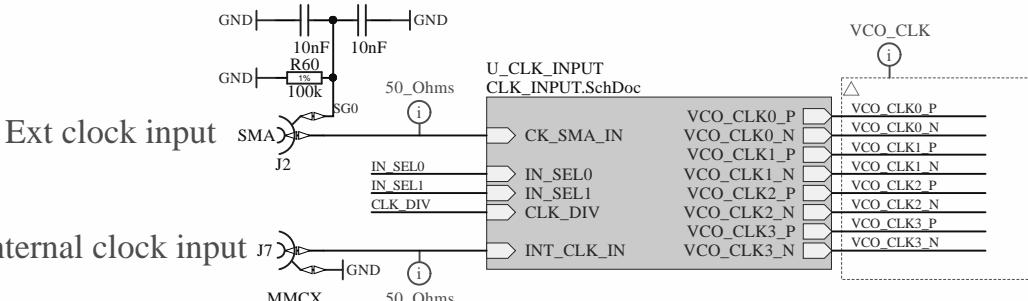


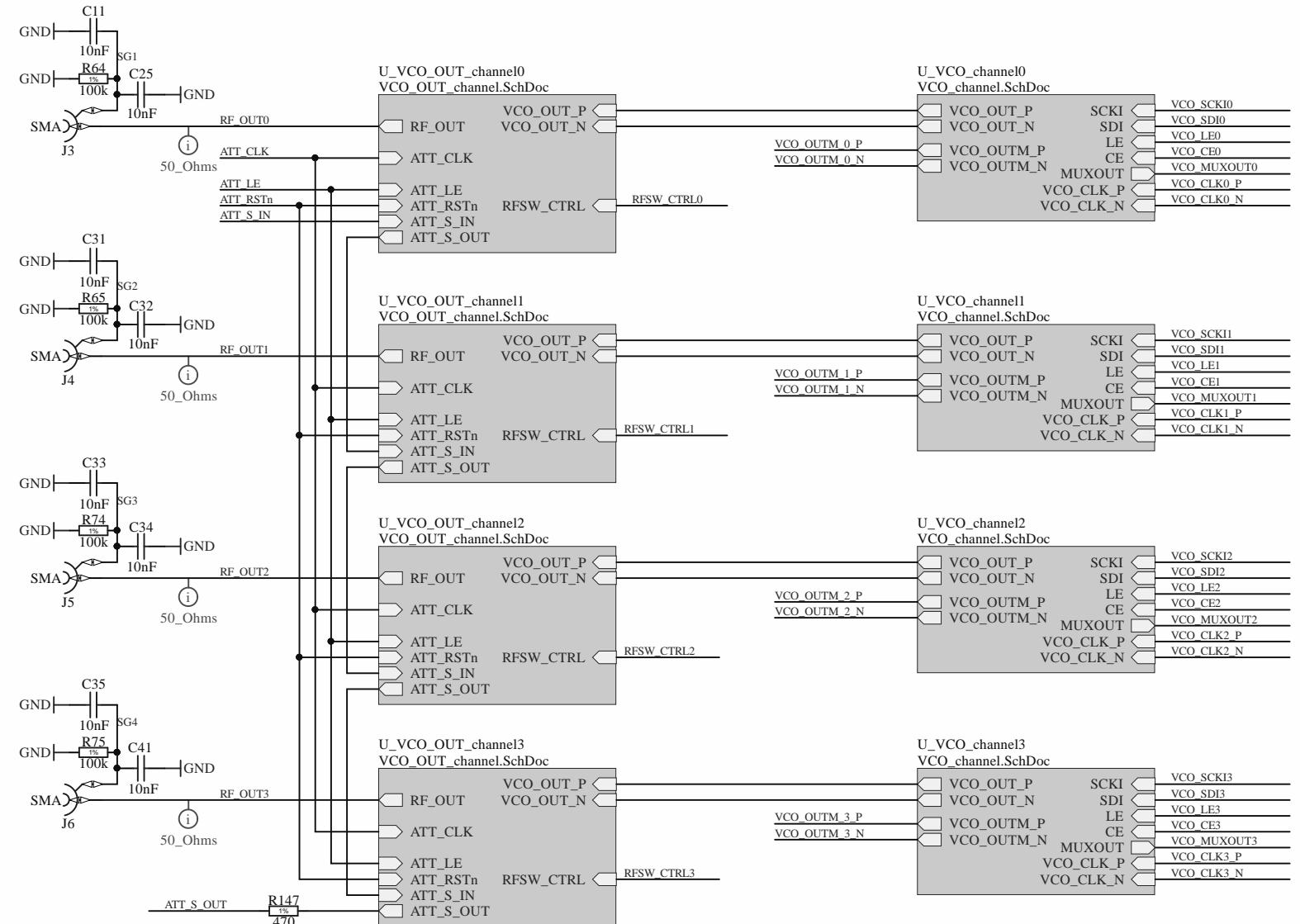
shield clips



Input frequency range:
10MHz-600MHz



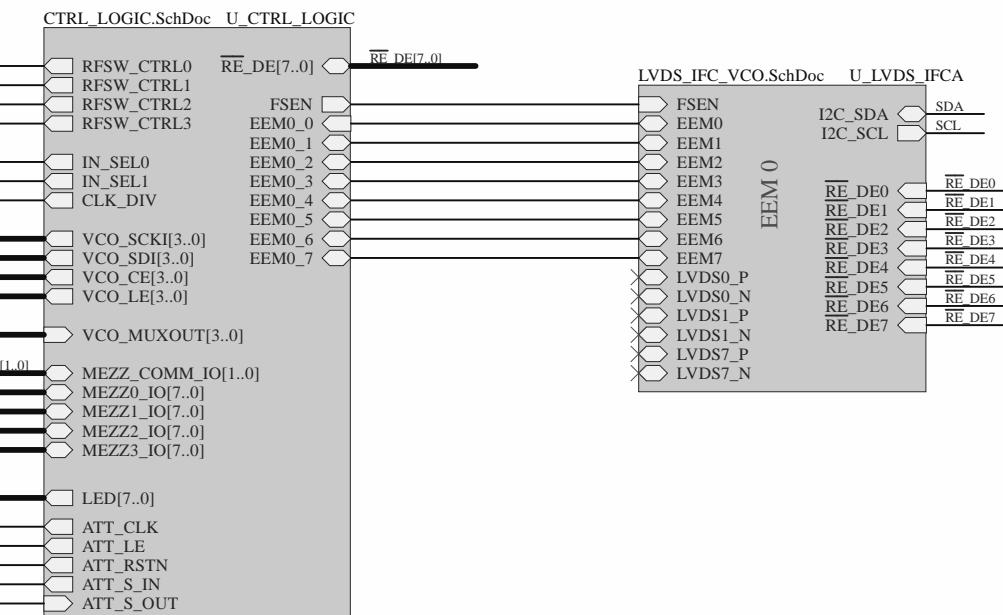
Output SMAs



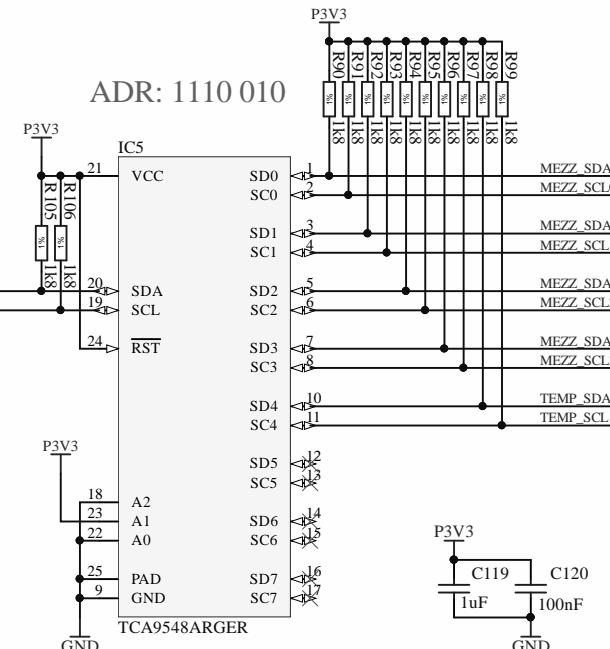
SMA Insulating washers

WASHER1	D11.1xd6.6	WASHER2	D11.1xd6.6
WASHER3	D11.1xd6.6	WASHER4	D11.1xd6.6
WASHER5	D11.1xd6.6	WASHER6	D11.1xd6.6
WASHER7	D11.1xd6.6	WASHER8	D11.1xd6.6
WASHER9	D11.1xd6.6	WASHER10	D11.1xd6.6

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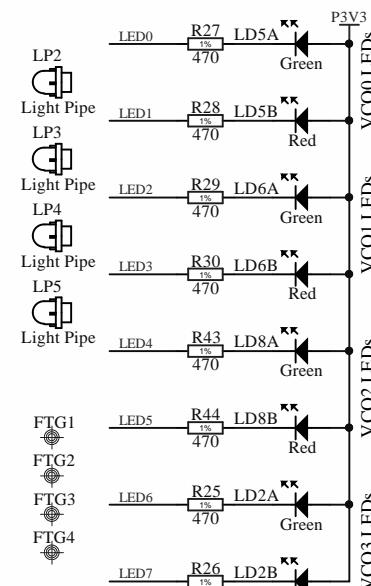
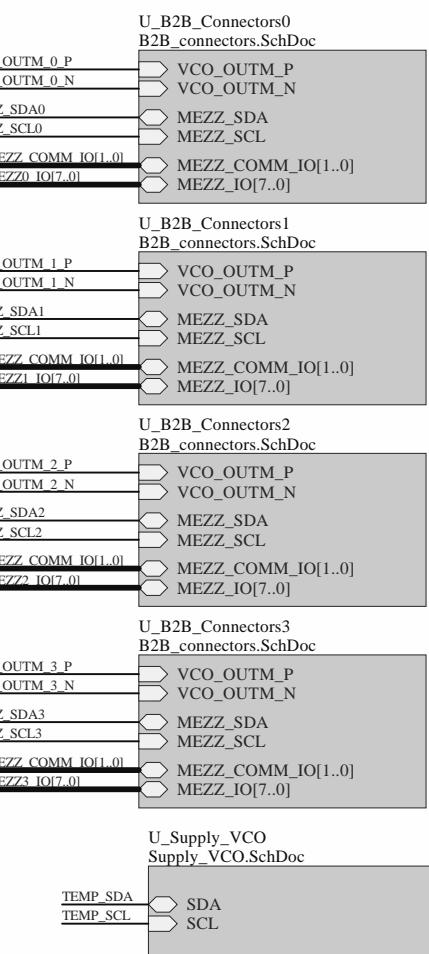


ADR: 1110 010



I2C tree:

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  "AFE3_EEPROM": {"path": [3], "addr": 0x50},
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Project/Equipment ARTIQ/SINARA

Document

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Sheet

1 of 8

Size

A3

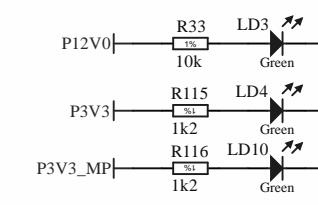
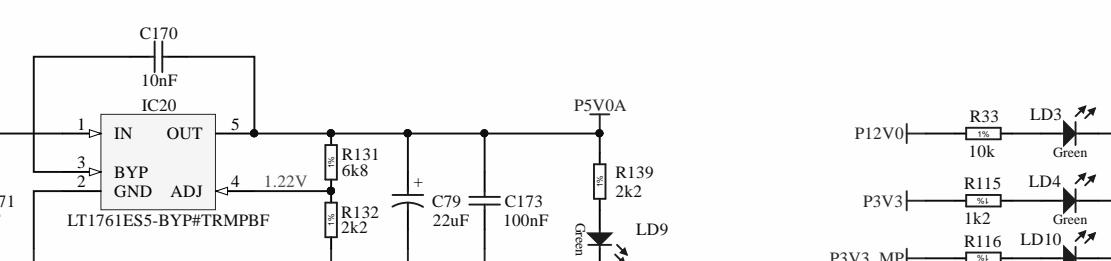
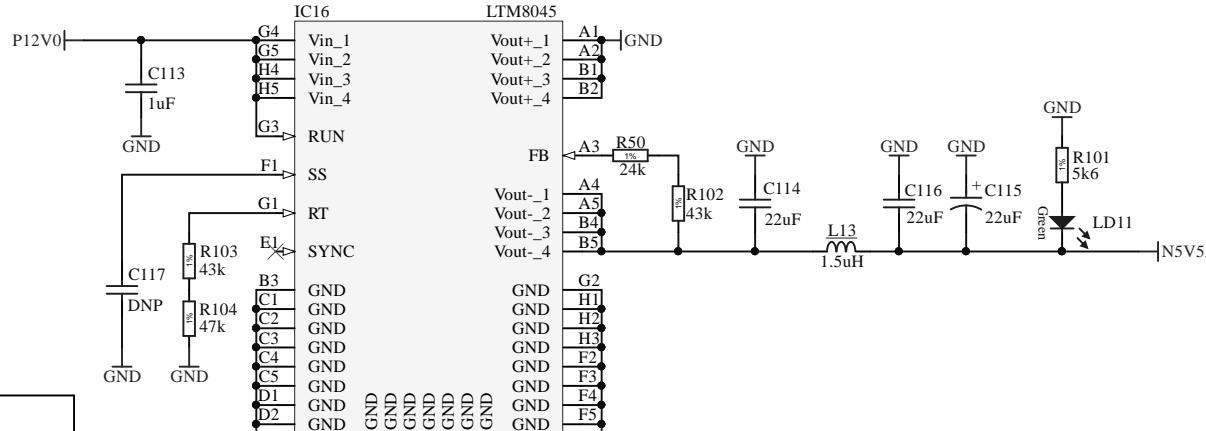
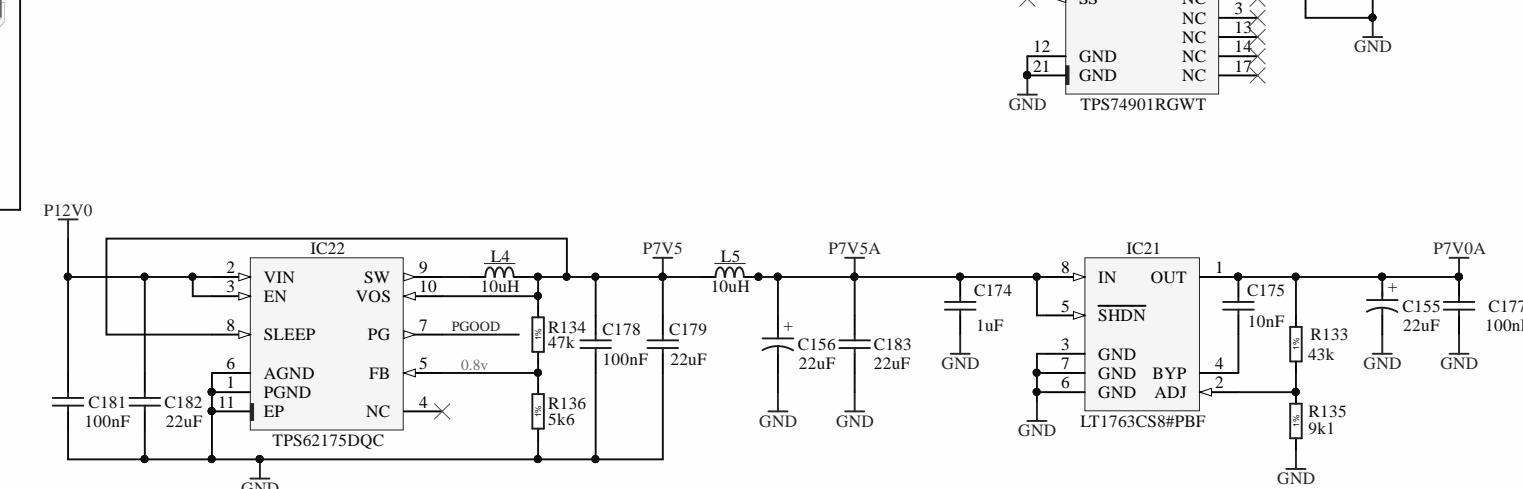
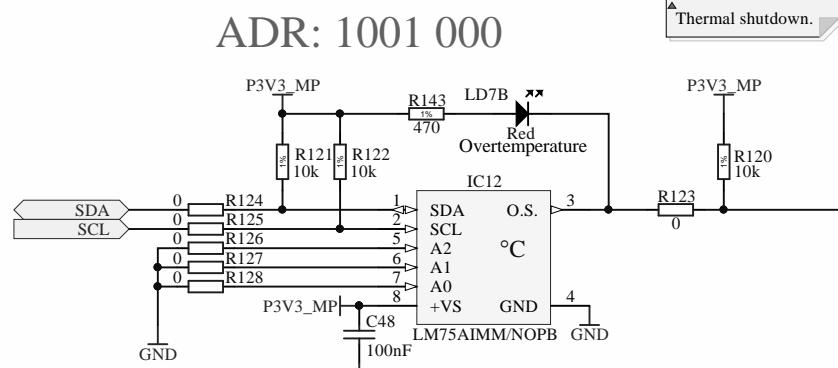
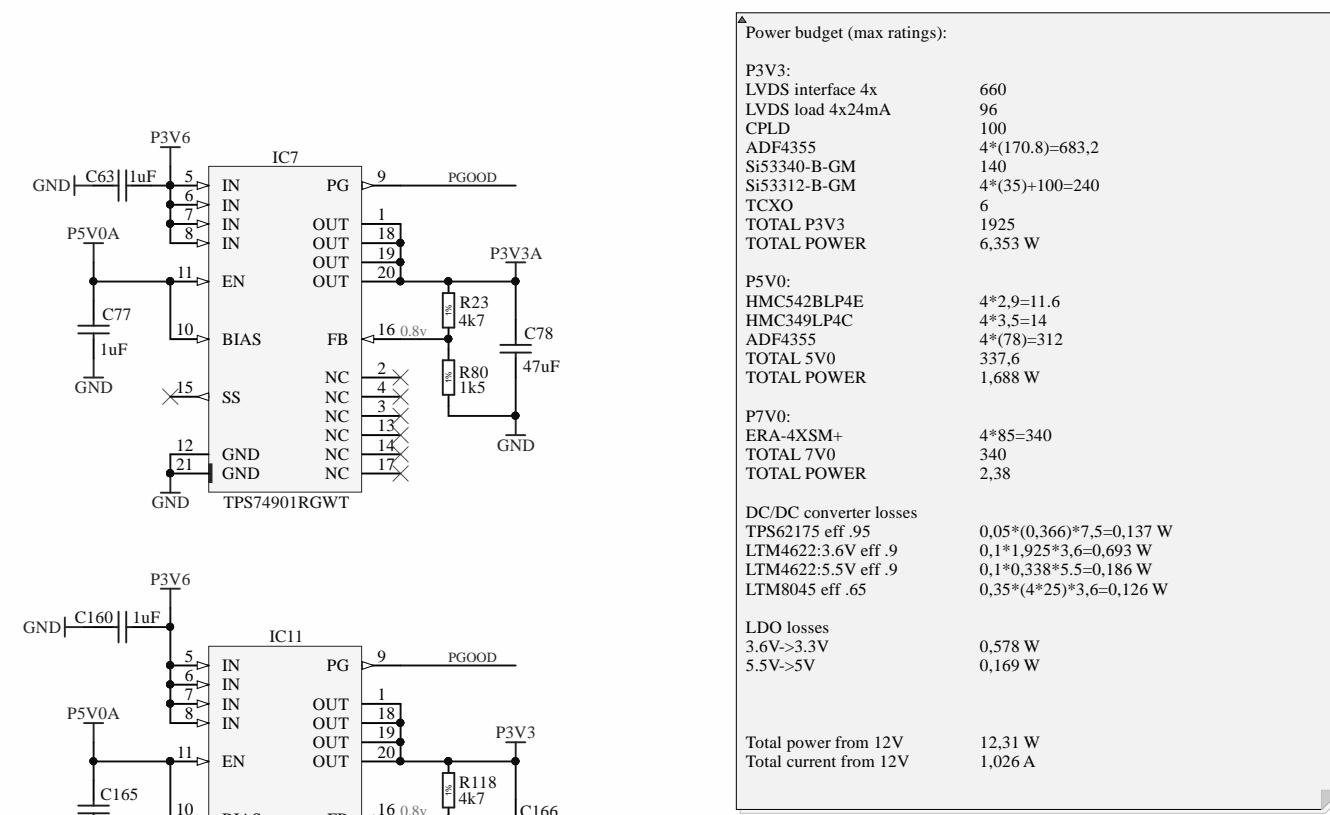
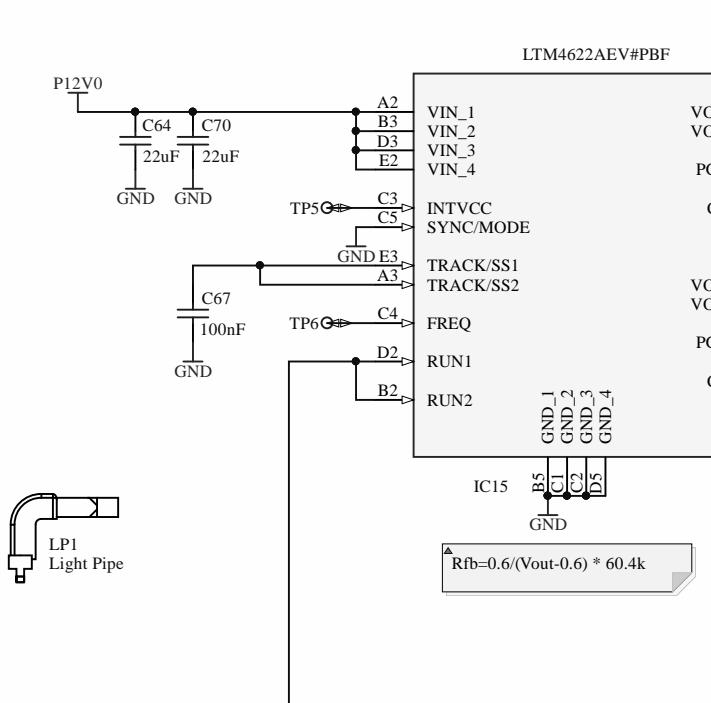
Rev

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ISE

Warsaw University of Technology Nowowiejska 15/19

ARTIQ

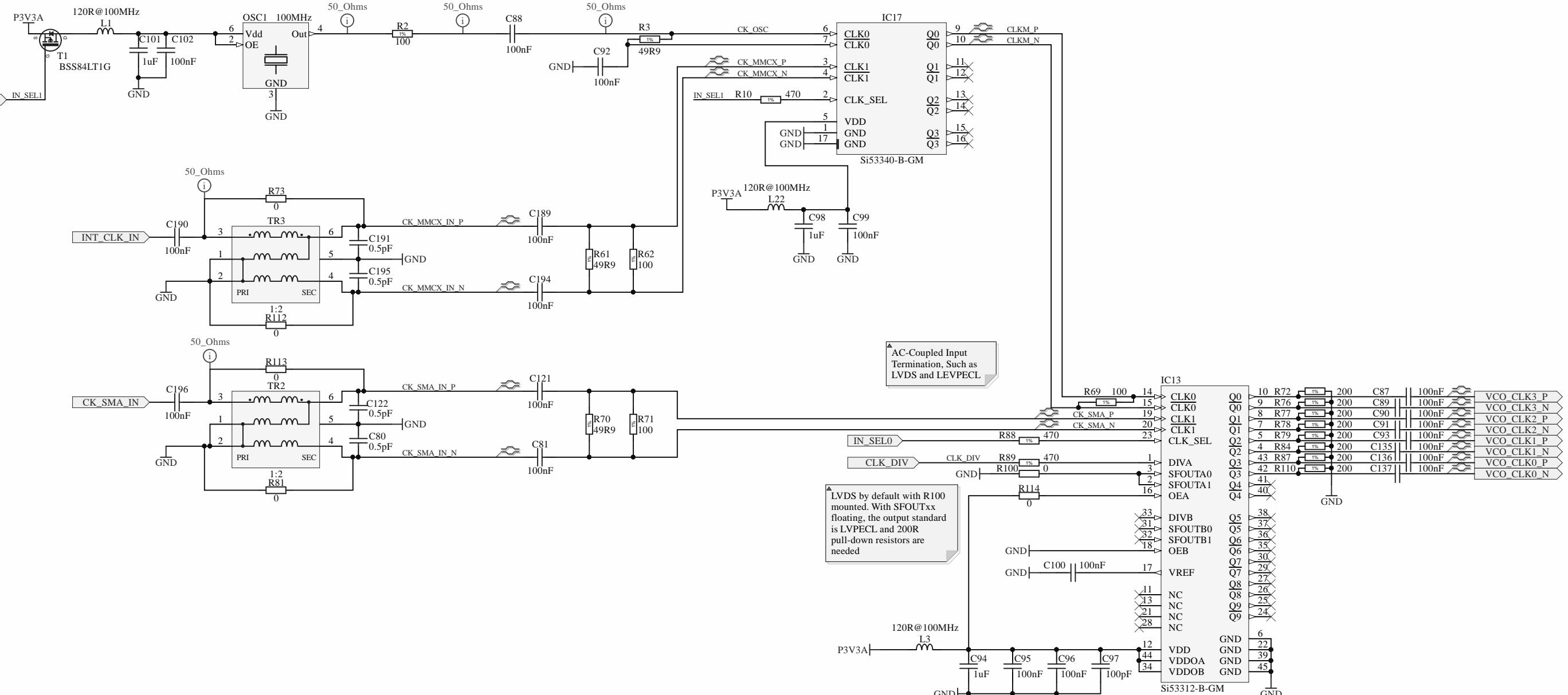


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Project/Equipment ARTIQ/SINARA

Power supply DC/DC & LDOs

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	Drawn by K.B.
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Warsaw University of Technology Nowowiejska 15/19	Size A3 Rev -



IN SEL0	IN SEL1	
0	0	XO
0	1	MMCX
1	0	SMA
1	1	SMA

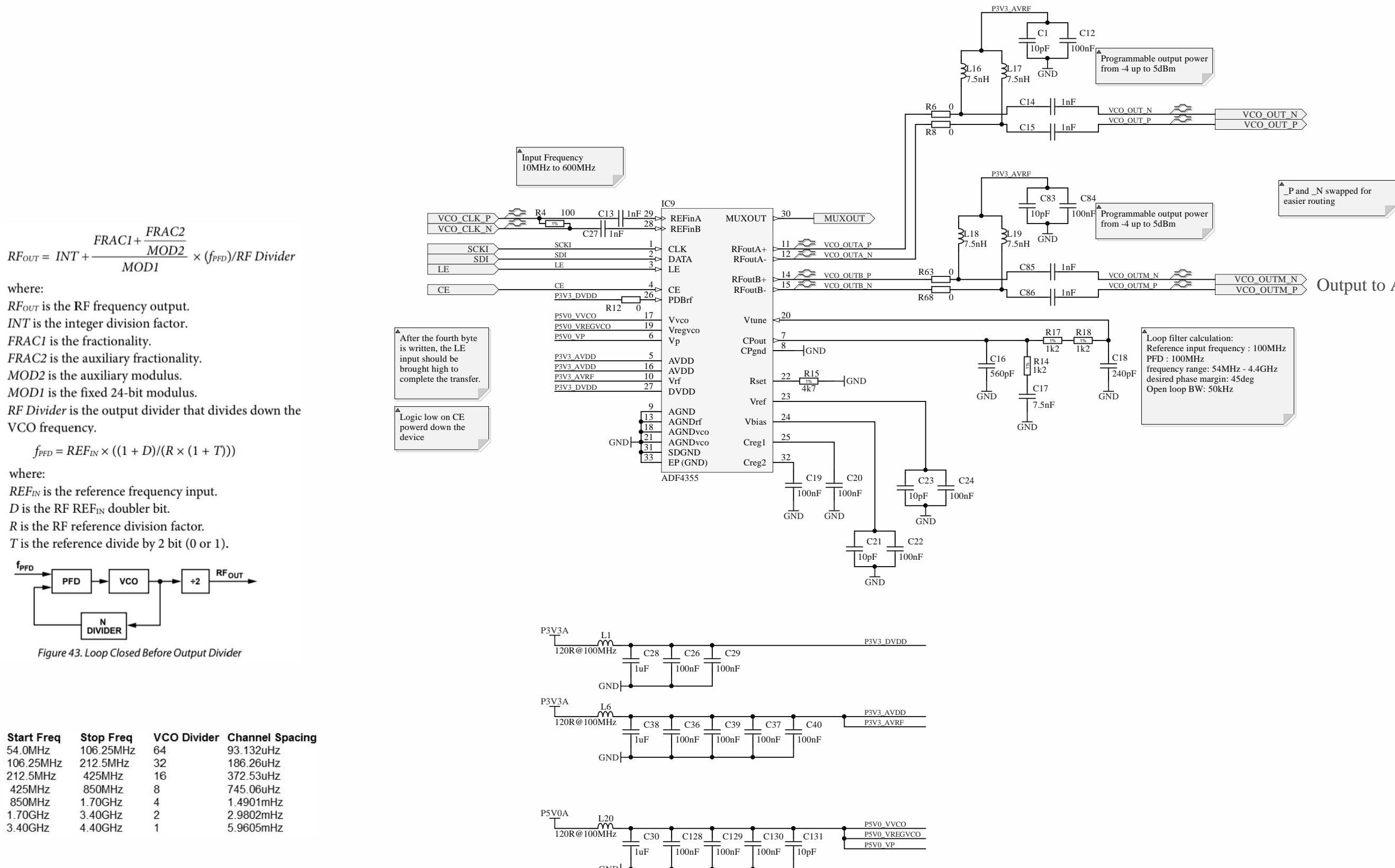
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卷之三十一
七言律诗(1956-1966)

Clock distribution and generation

Project/Equipment	ARTIQ/SINARA	
Document	<i>Clock distribution and generation</i>	Designer K.B.
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		Check by -
		Last Mod. - 2018-12-16
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		Print Date 2018-12-16 19:40:56 Sheet 3 of 8
	Warsaw University of Technology ISE Nowowiejska 15/19	Size A3 Rev
		ARTIQ A3



$$RF_{OUT} = INT + \frac{FRAC1 + FRAC2}{MOD2} \times (f_{PFD})/RF\text{ Divider}$$

where:
 RF_{OUT} is the RF frequency output.
 INT is the integer division factor.
 $FRAC1$ is the fractionality.
 $FRAC2$ is the auxiliary fractionality.
 $MOD2$ is the auxiliary modulus.
 $MOD1$ is the fixed 24-bit modulus.
 $RF\text{ Divider}$ is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T)))$$

where:
 REF_{IN} is the reference frequency input.
 D is the RF REF_{IN} doubler bit.
 R is the RF reference division factor.
 T is the reference divide by 2 bit (0 or 1).

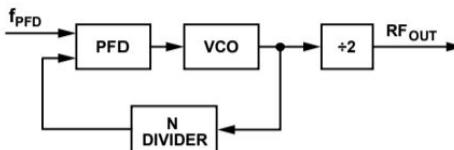
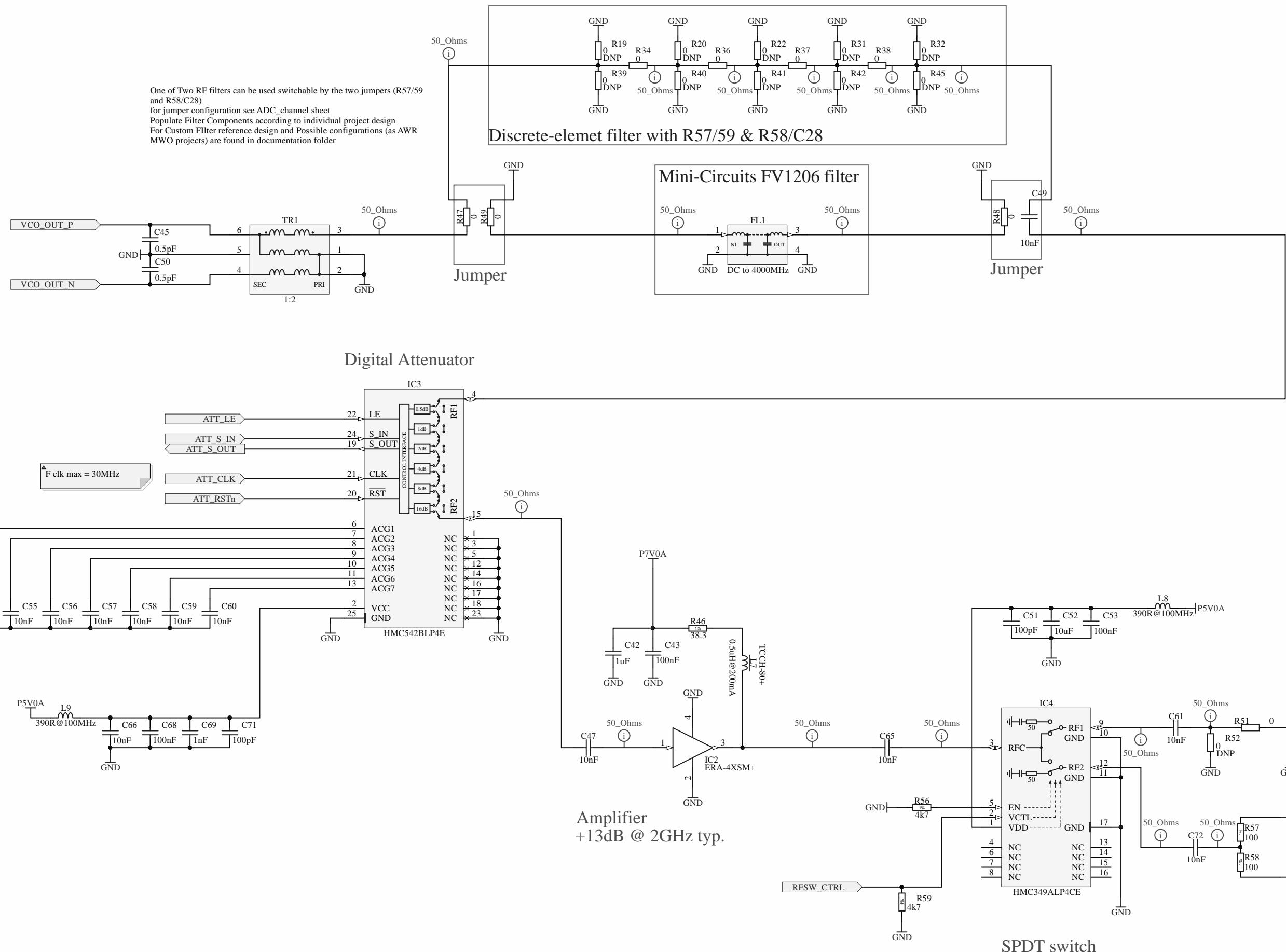


Figure 43. Loop Closed Before Output Divider

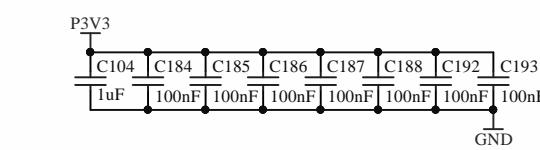
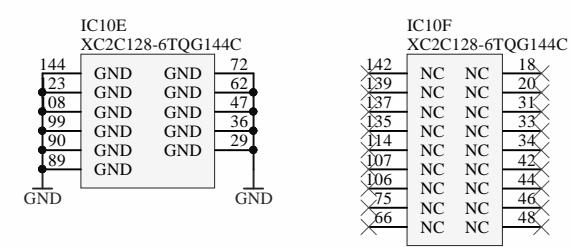
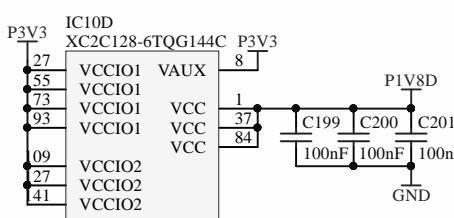
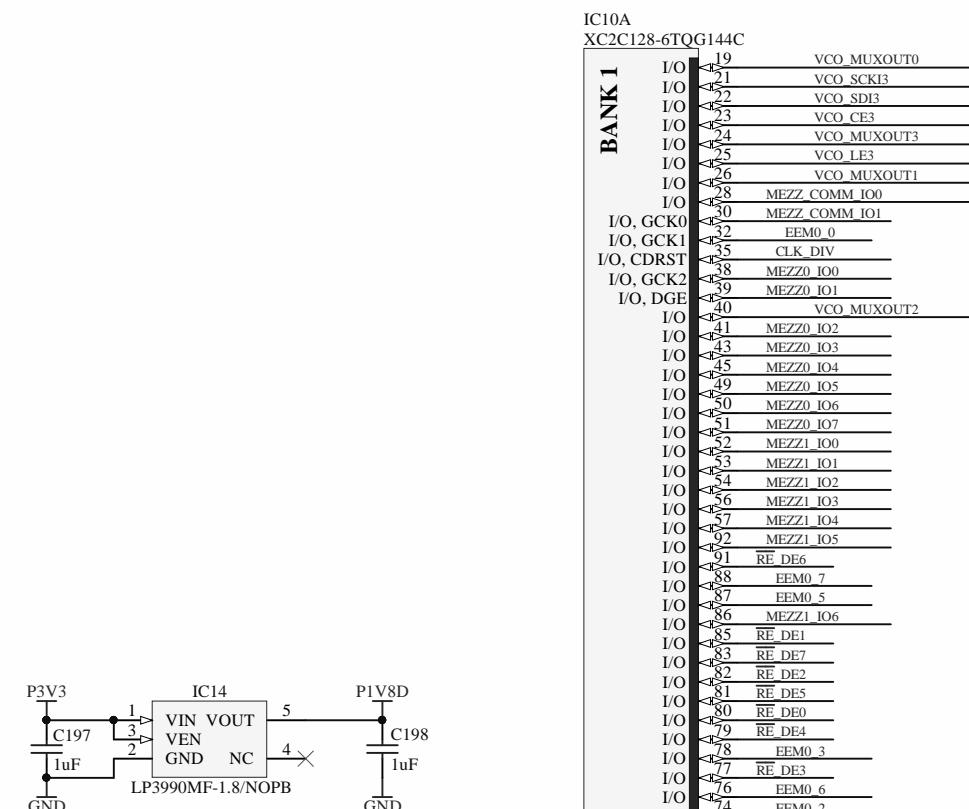
Start Freq	Stop Freq	VCO Divider	Channel Spacing
54.0MHz	106.25MHz	64	93.132uHz
106.25MHz	212.5MHz	32	186.26uHz
212.5MHz	425MHz	16	372.53uHz
425MHz	850MHz	8	745.06uHz
850MHz	1.70GHz	4	1.4901mHz
1.70GHz	3.40GHz	2	2.9802mHz
3.40GHz	4.40GHz	1	5.9605mHz

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		ARTIQ	

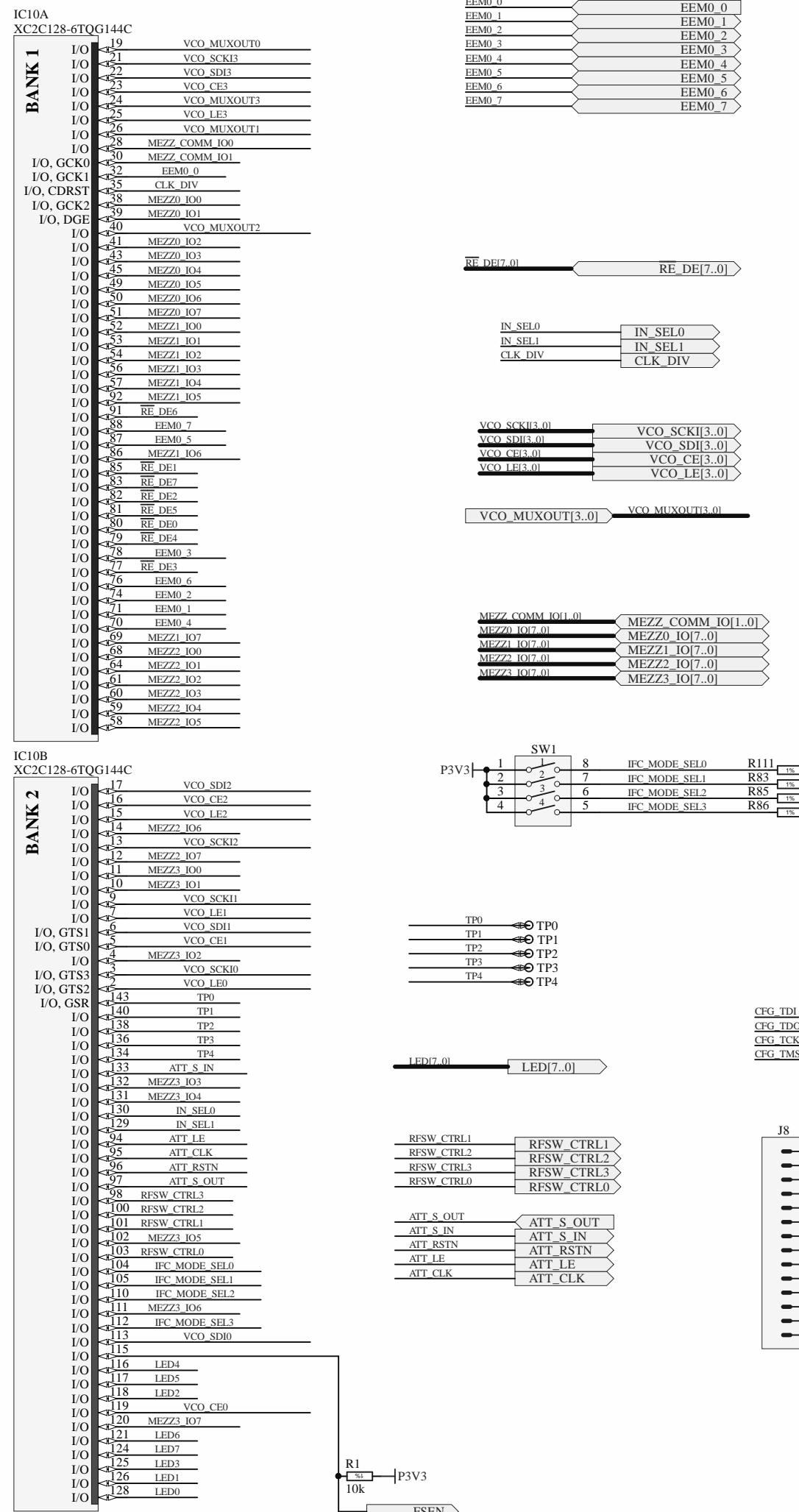


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A

B

C

D

E

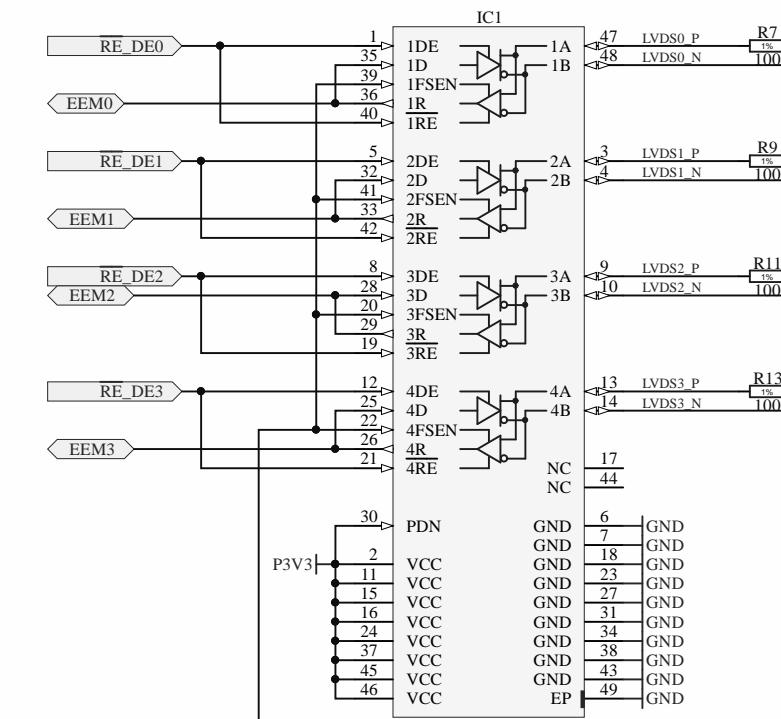
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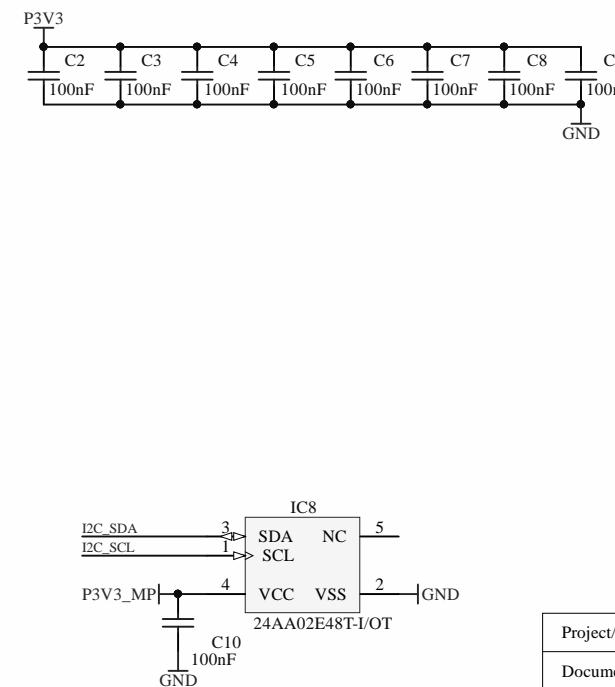
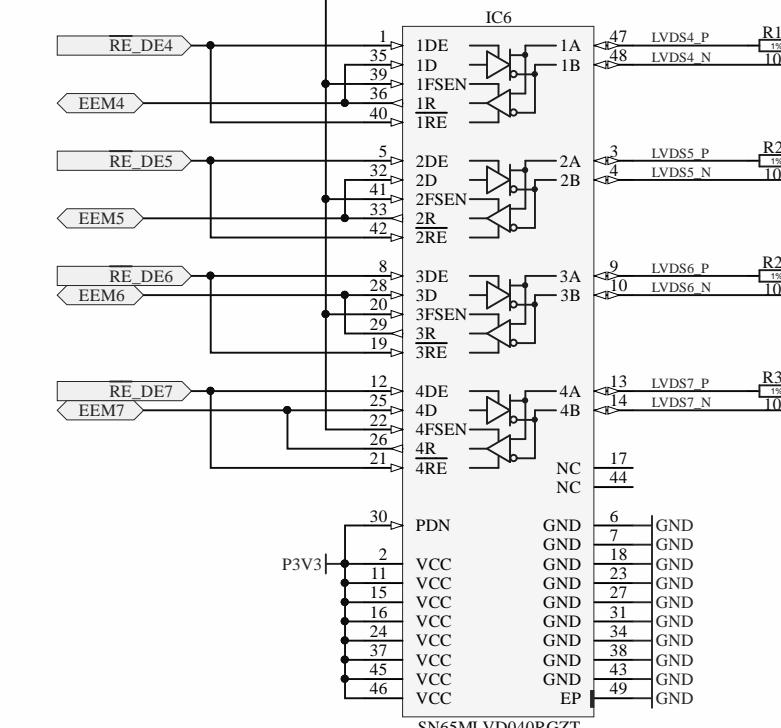
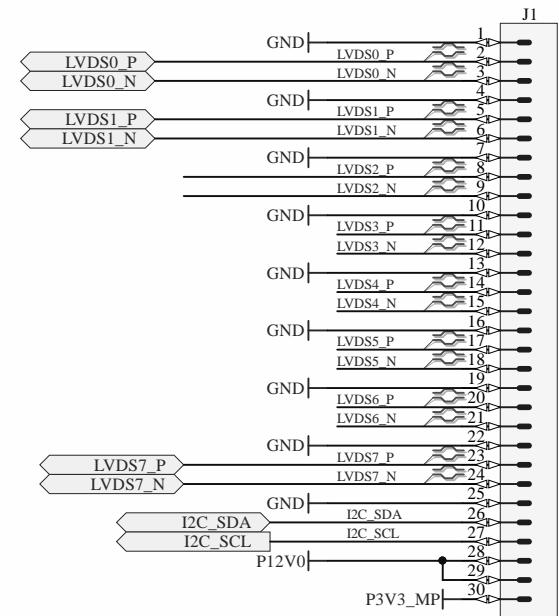
C

D

E



EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A



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Document

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LVDS to LVTTI interface & EEM connector

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Nowowiejska 15/19

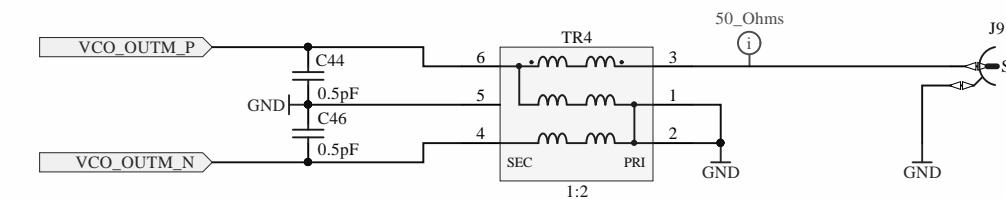
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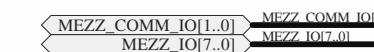
ARTIQ

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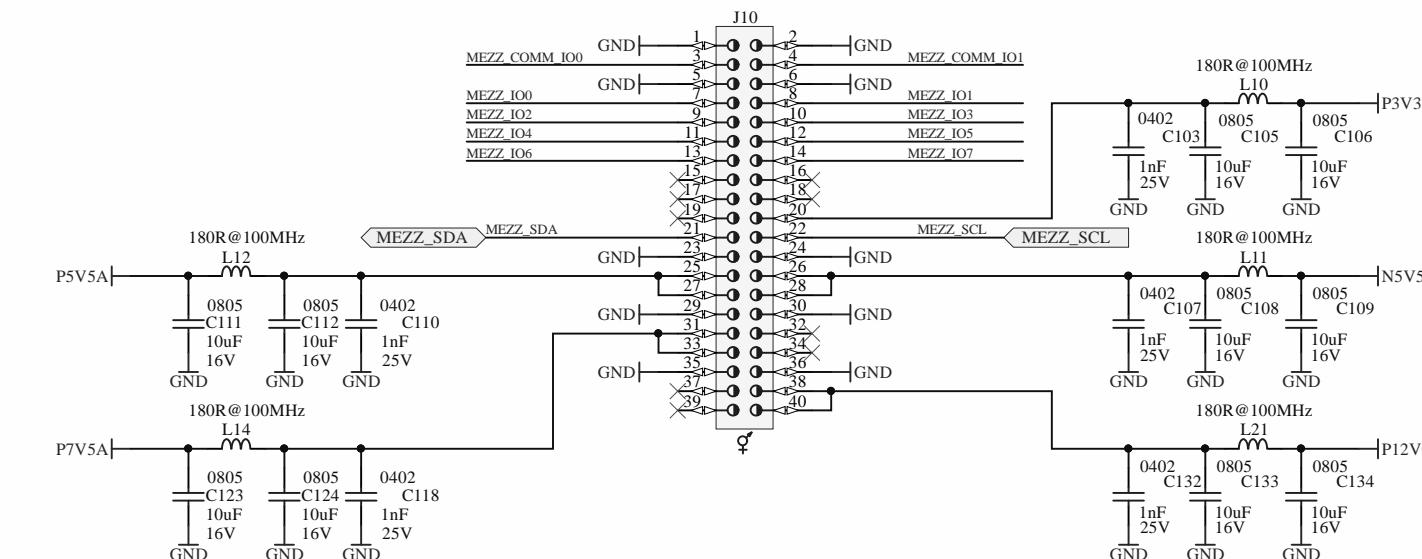
Board-2-Board Analog Connector



B



Board-2-Board Digital Connectors

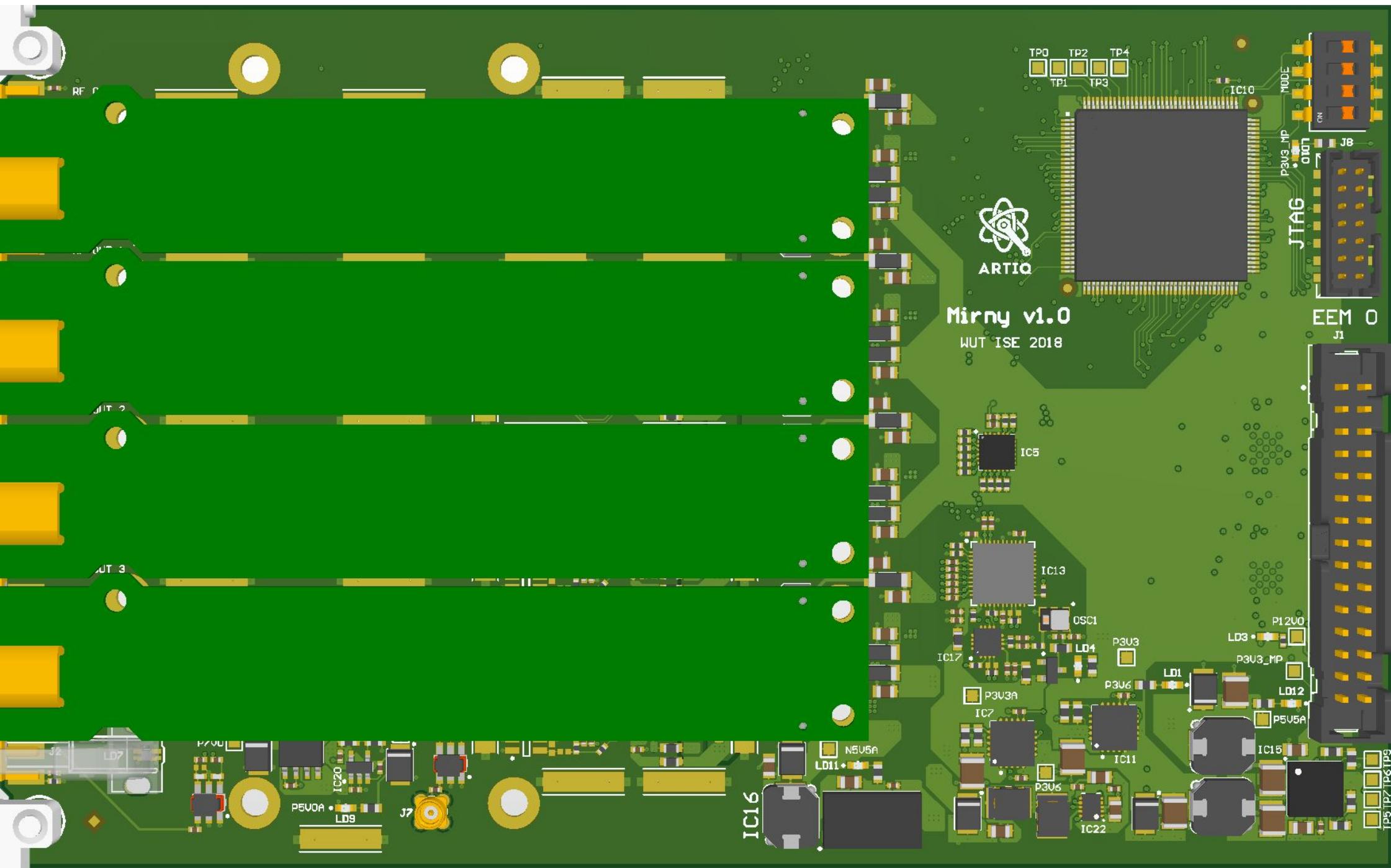


C

B

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	Warsaw University of Technology ISE Nowowiejska 15/19		Size A3 Rev
		ARTIQ	A3 -

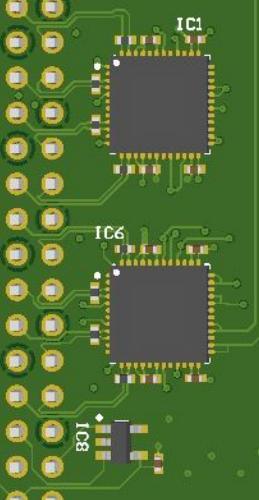




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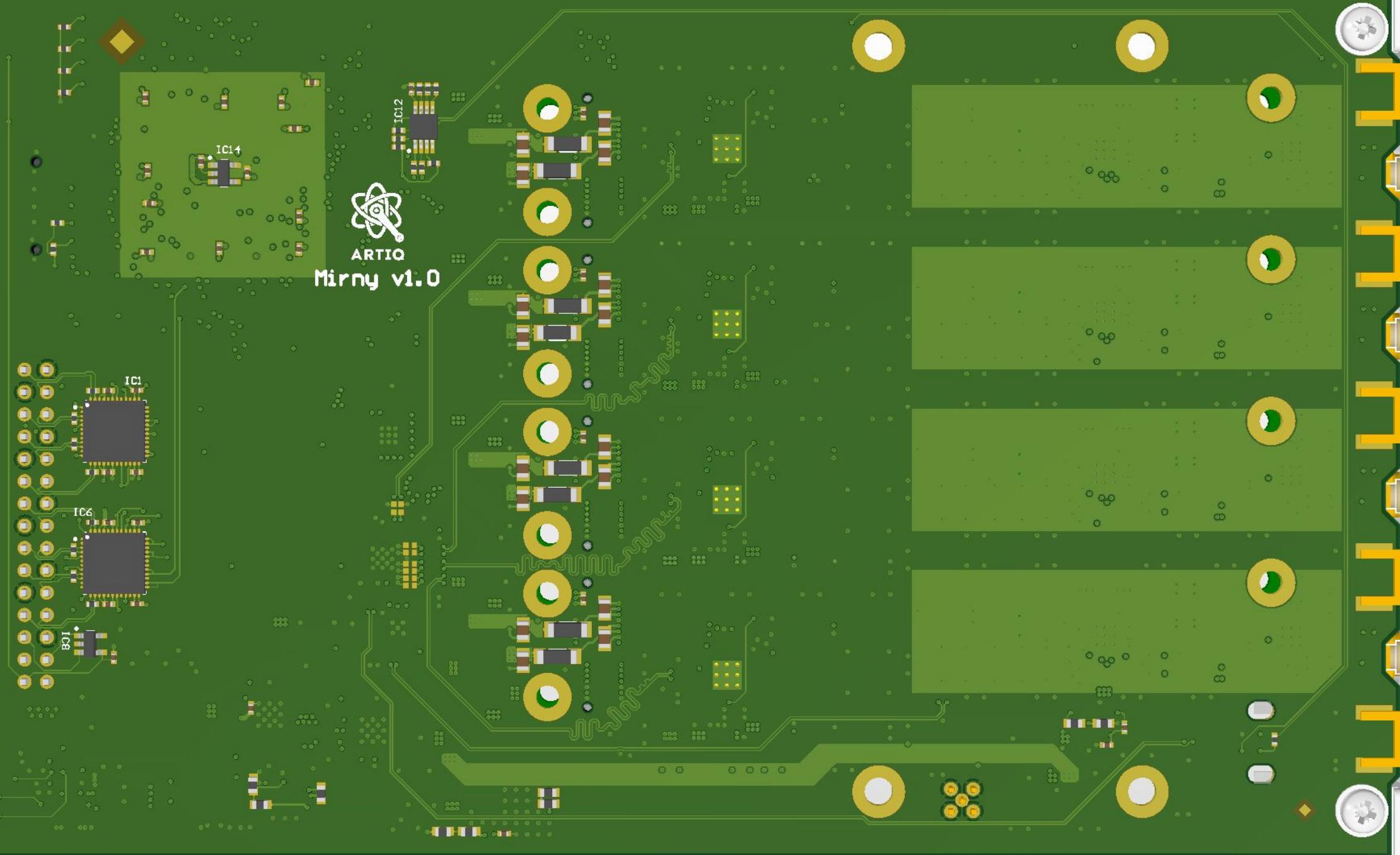
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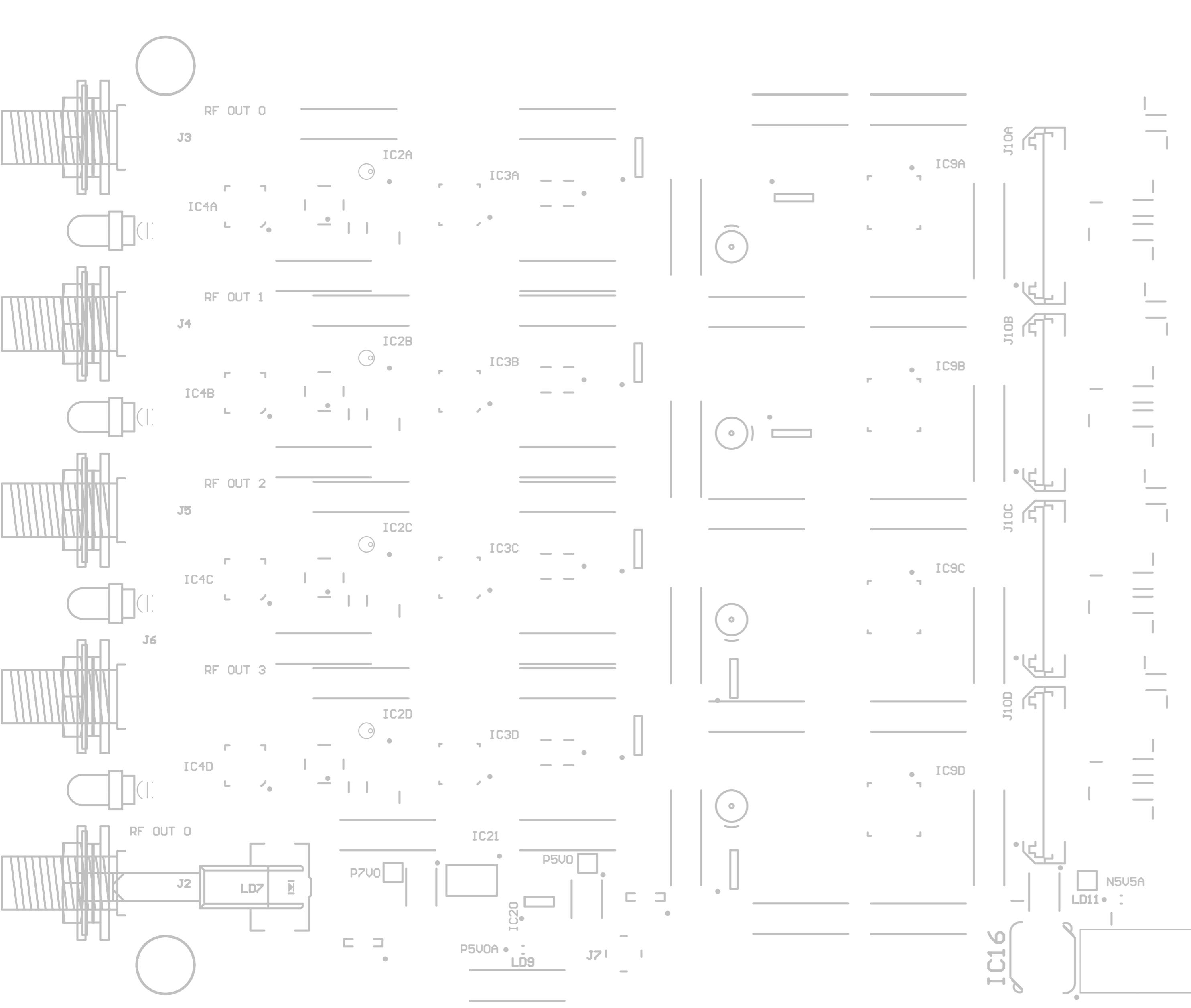
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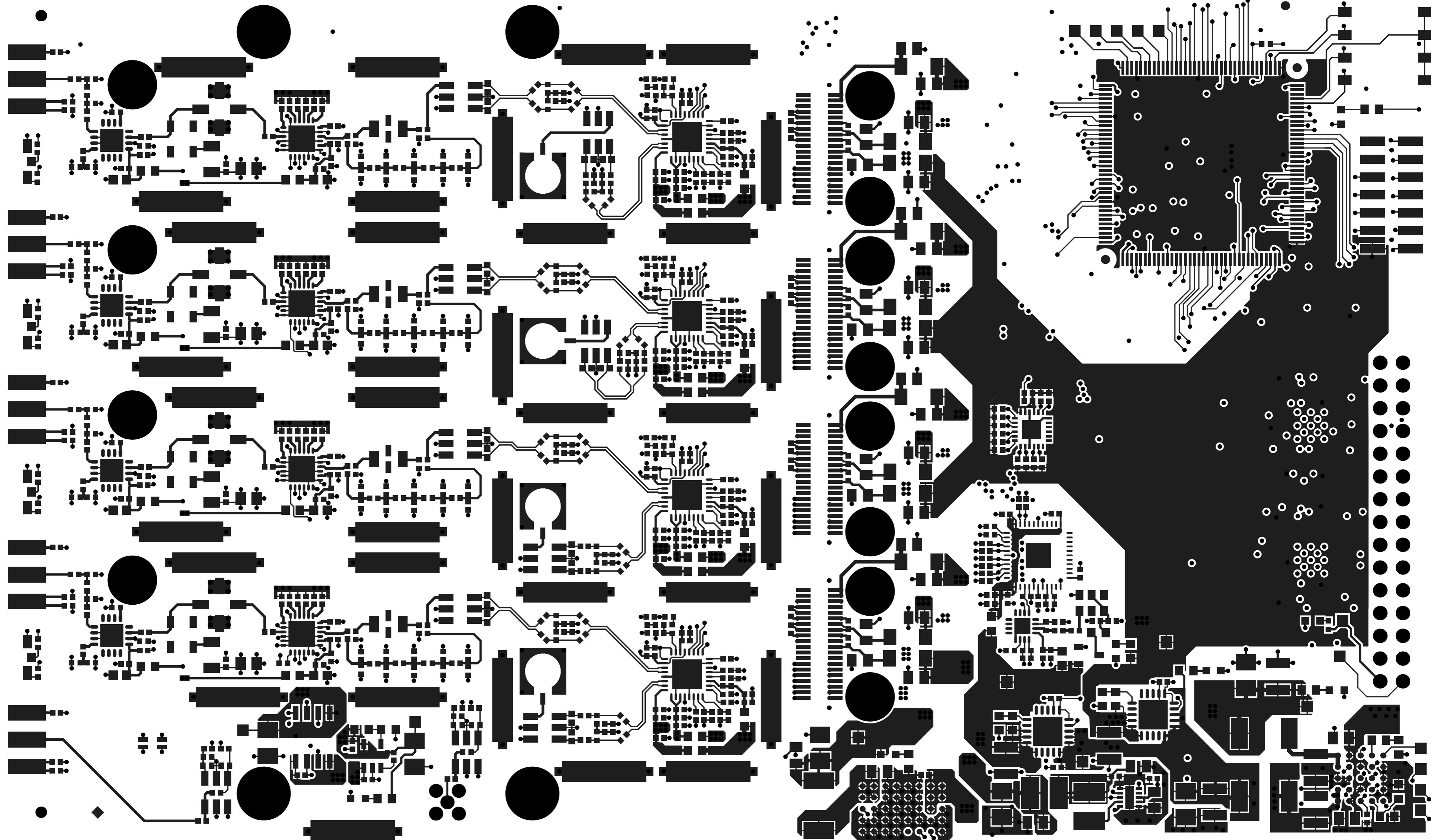


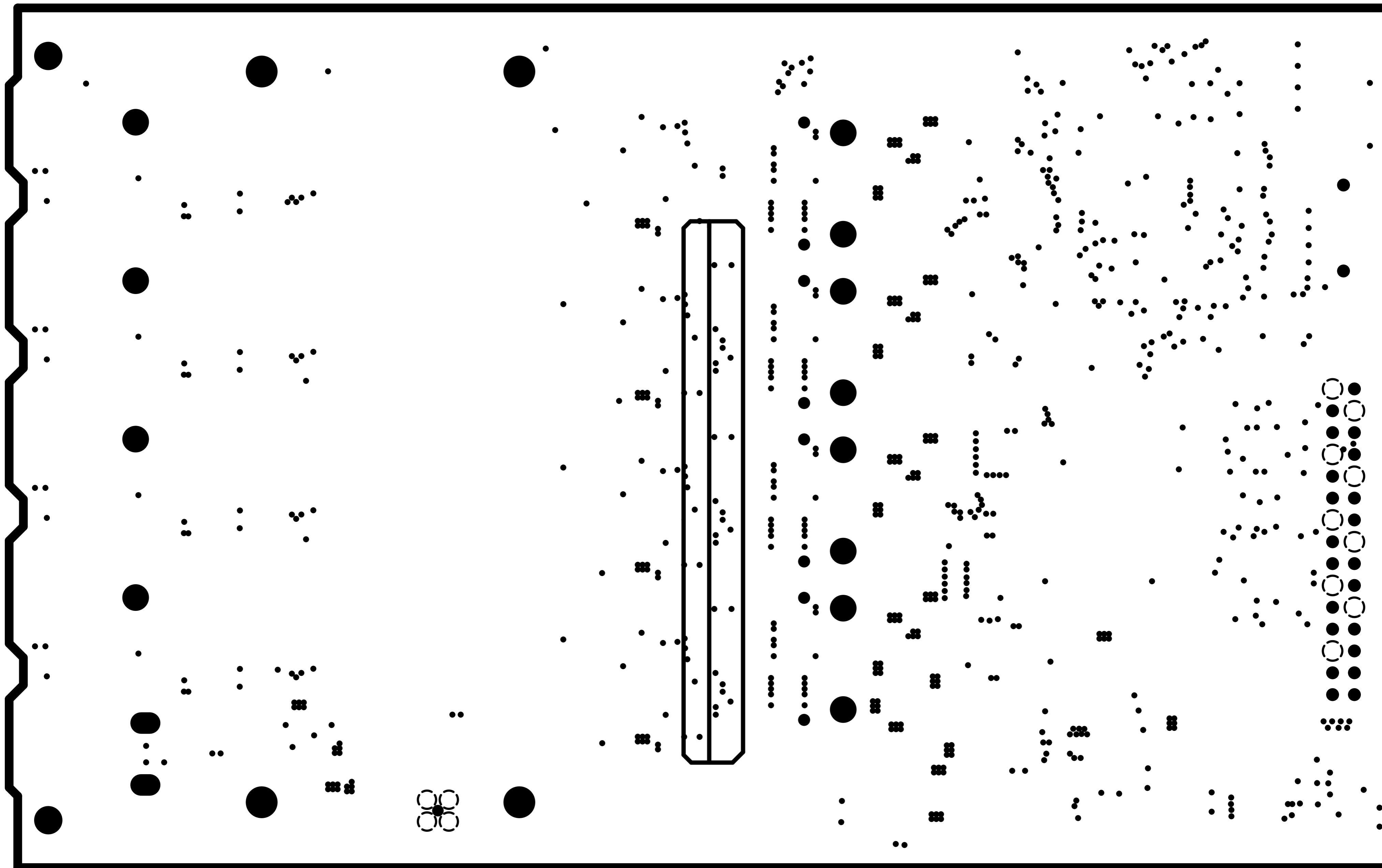
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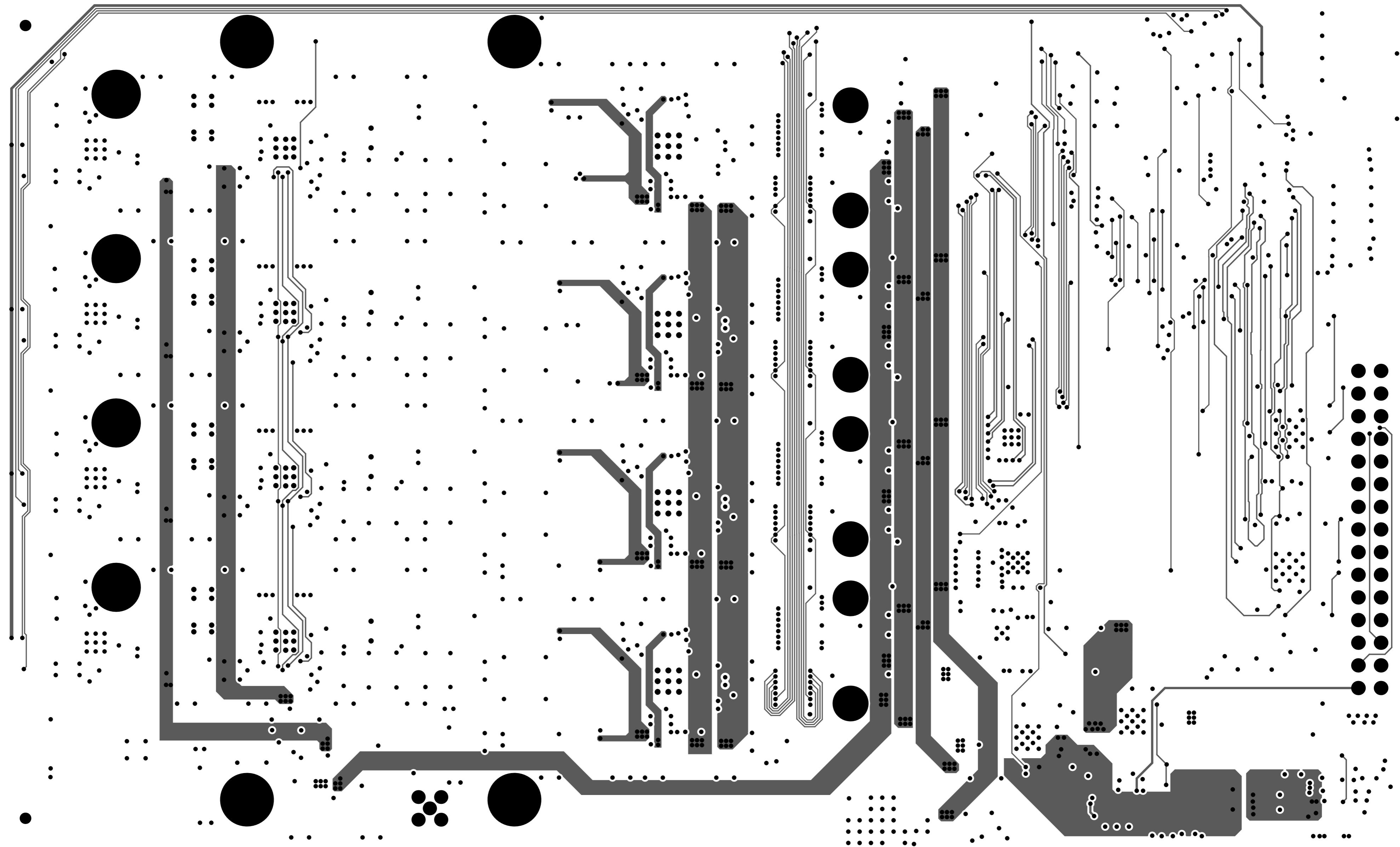
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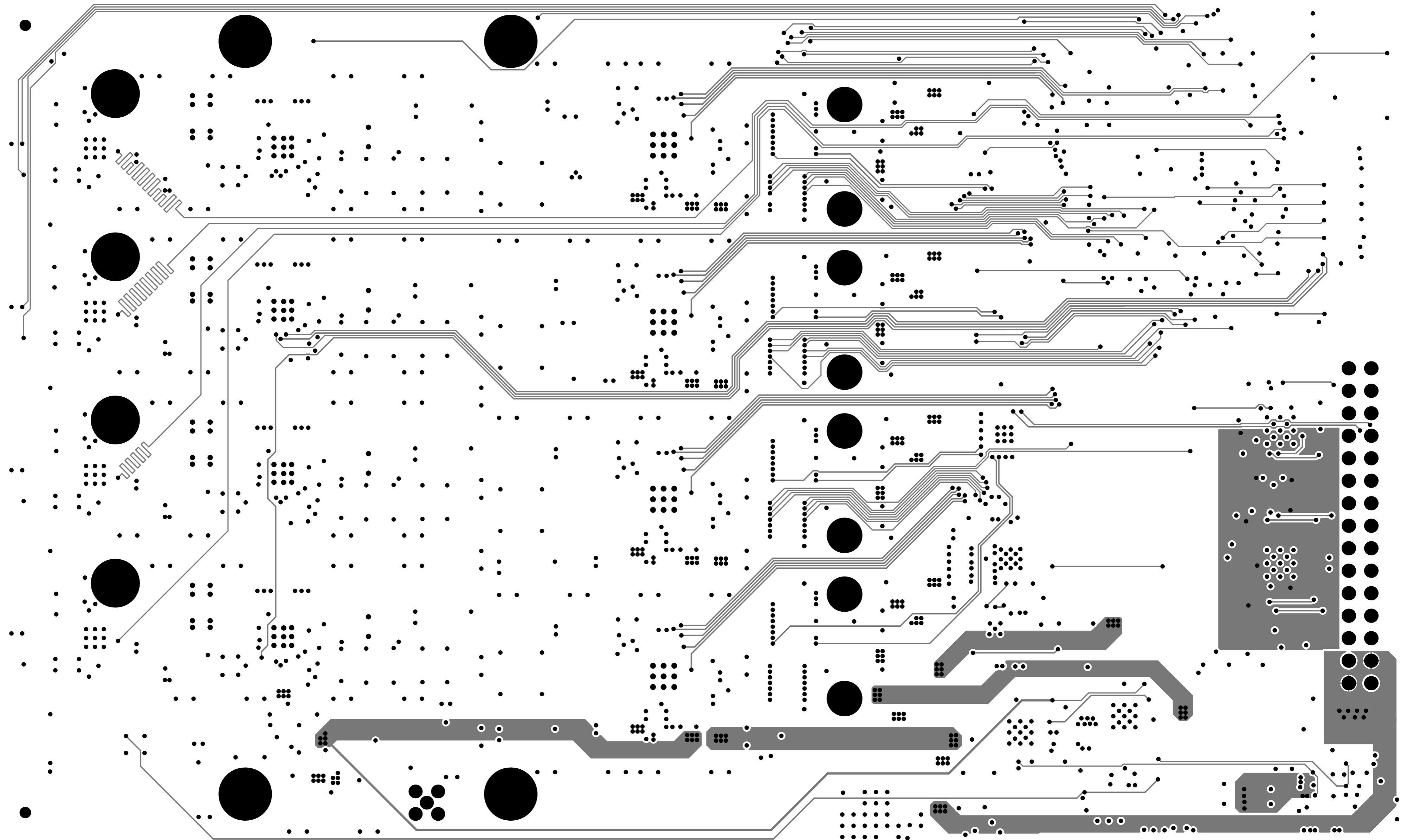


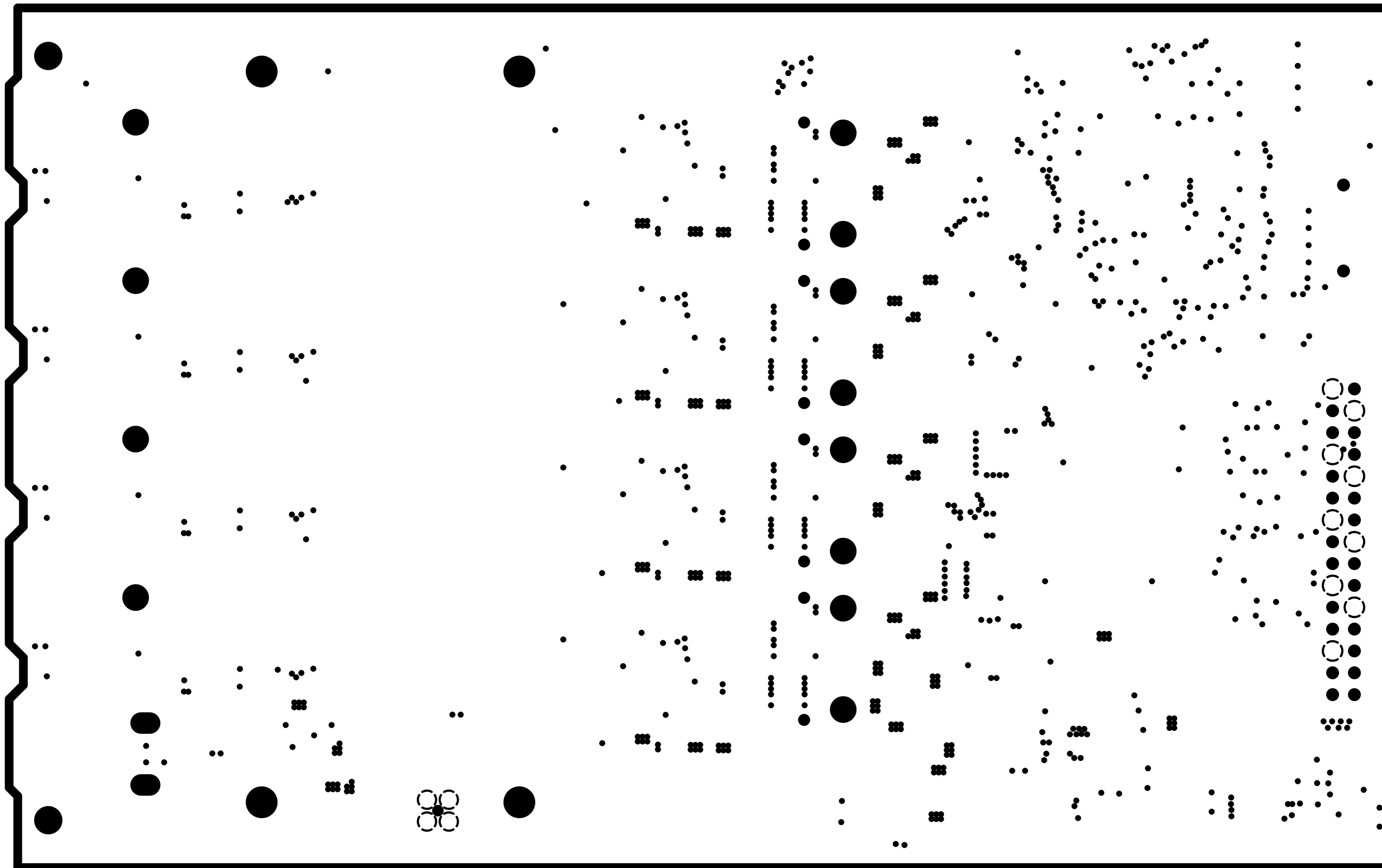


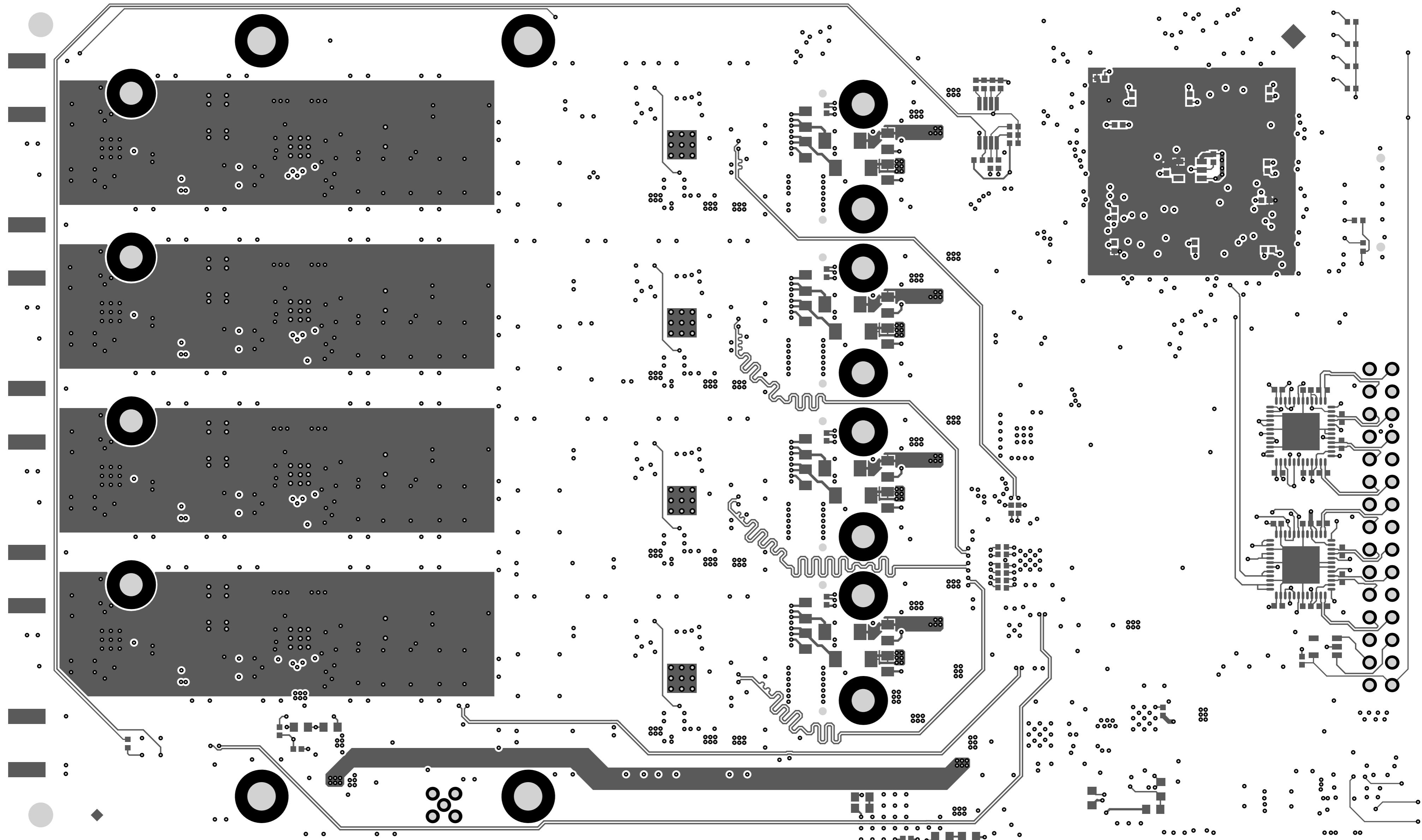












IC8

IC6

IC1



IC14



IC15



ARATIO

Mifrah At.0



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	1,34mil	3,5	
3	L1	Copper	2,28mil		
4	Dielectric1	FR4	7,09mil	3,66	
5	P2	Copper	0,71mil		
6	Dielectric 9	FR4	18,11mil	4,2	
7	L3	Copper	0,71mil		
8	Dielectric 8		7,09mil	4,2	
9	L4	Copper	0,71mil		
10	Dielectric4	FR4	18,11mil	4,2	
11	P5	Copper	0,71mil		
12	Dielectric3	FR4	7,09mil	4,2	
13	L6	Copper	2,28mil		
14	Bottom Solder	Solder Resist	1,34mil	3,5	
15	Bottom Overlay				