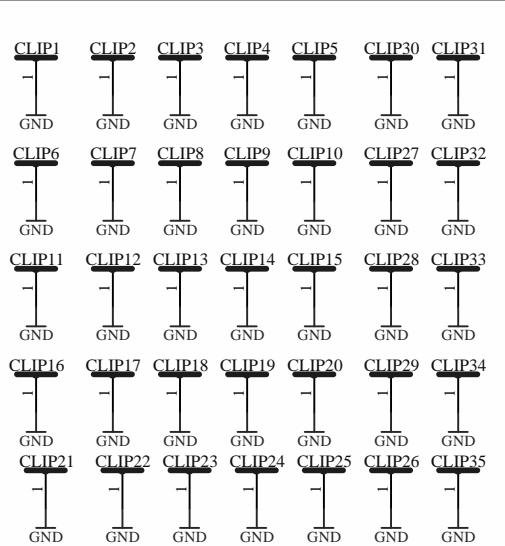
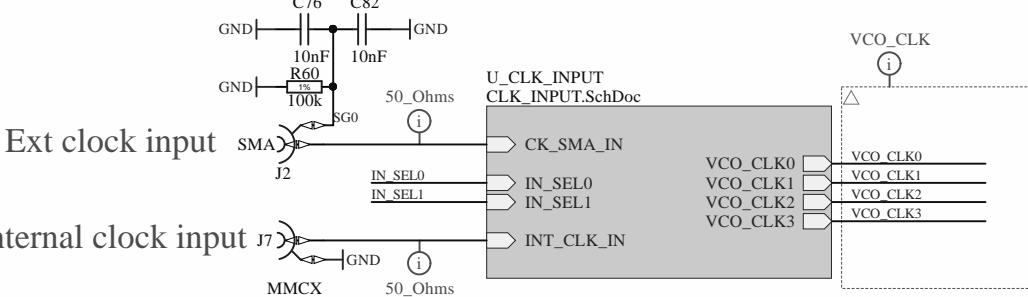


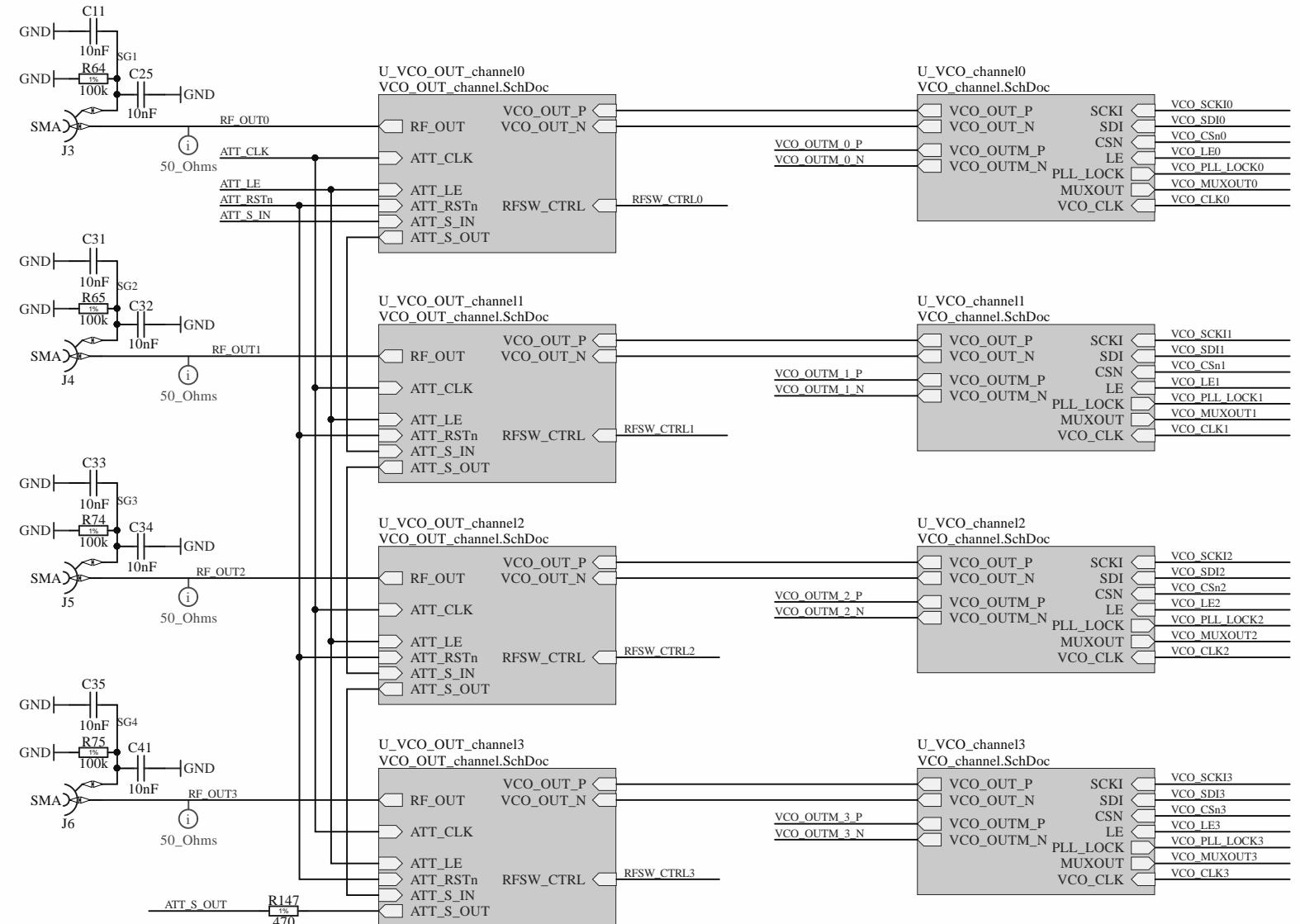
shield clips



Input frequency range:
10MHz-250MHz



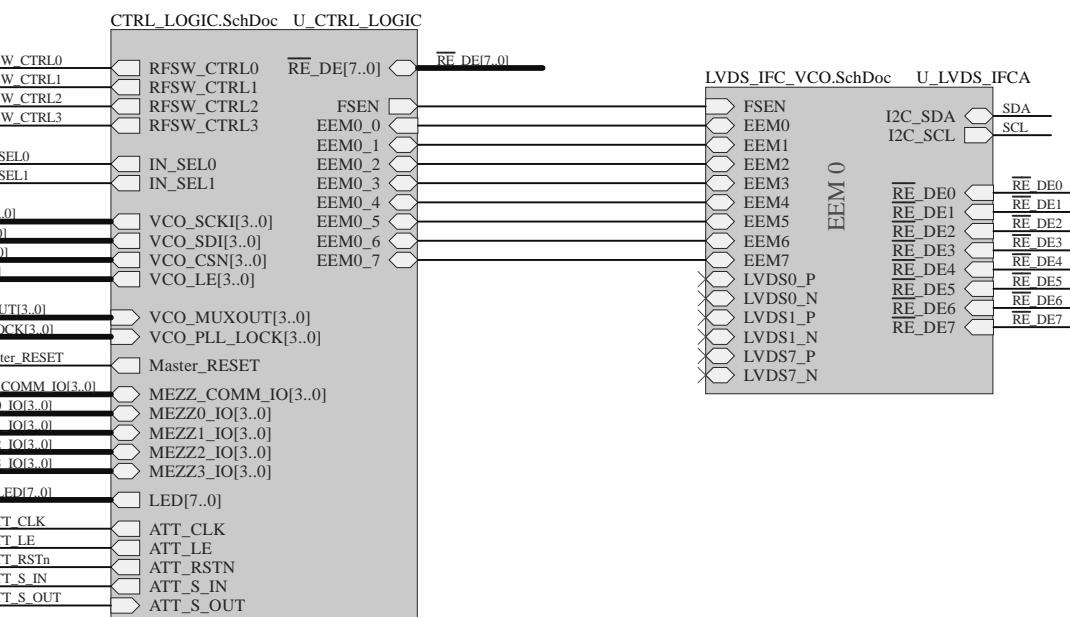
Output SMAs



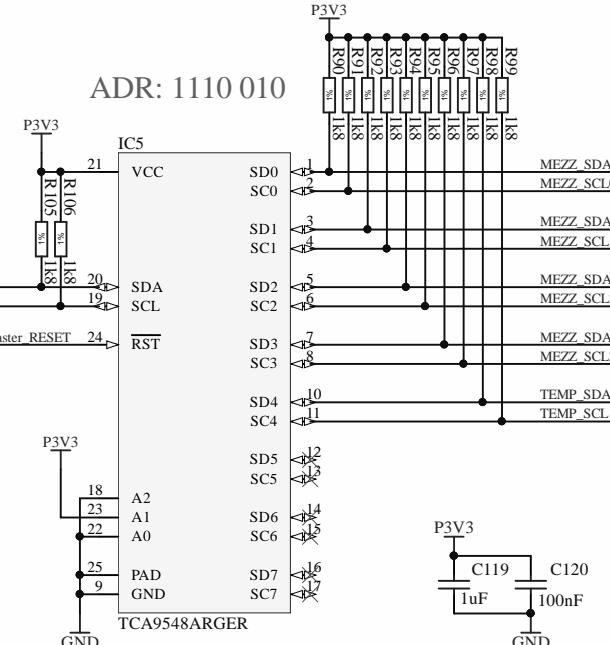
SMA Insulating washers

WASHER1	D11.1xd6.6	WASHER2	D11.1xd6.6
WASHER3	D11.1xd6.6	WASHER4	D11.1xd6.6
WASHER5	D11.1xd6.6	WASHER6	D11.1xd6.6
WASHER7	D11.1xd6.6	WASHER8	D11.1xd6.6
WASHER9	D11.1xd6.6	WASHER10	D11.1xd6.6

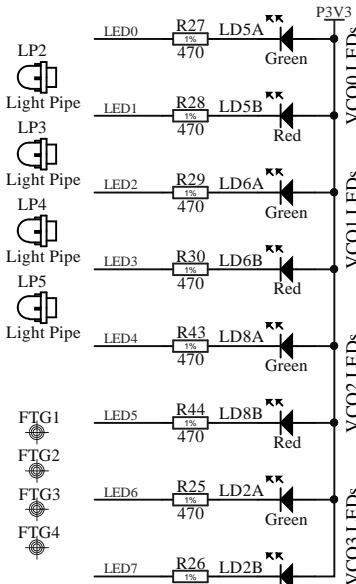
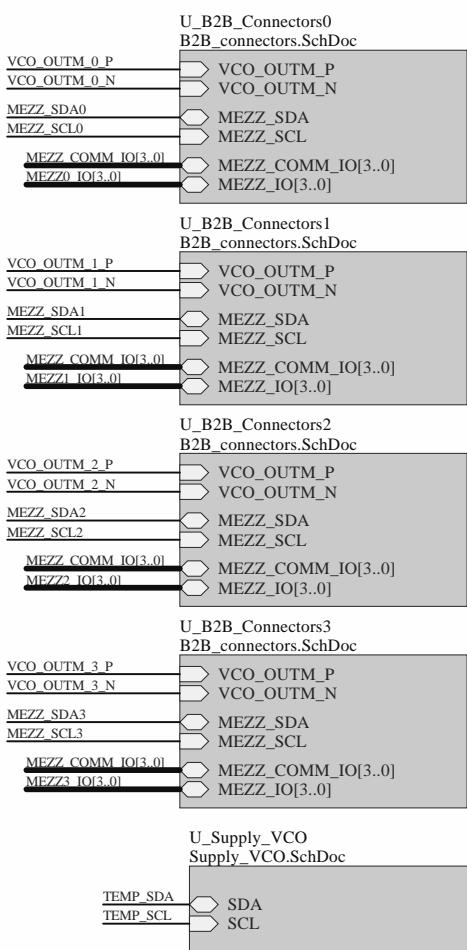
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ADR: 1110 010



I2C tree:
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Project/Equipment ARTIQ/SINARA

Document

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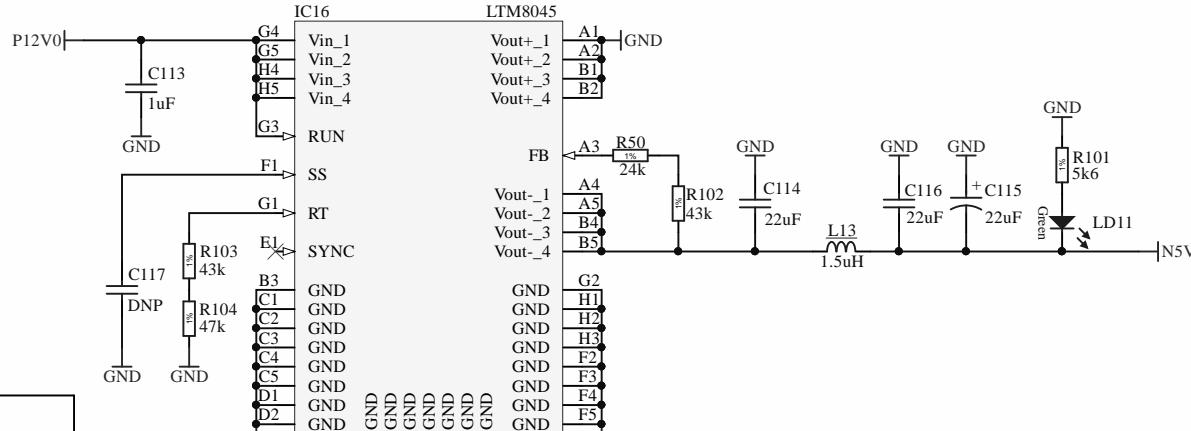
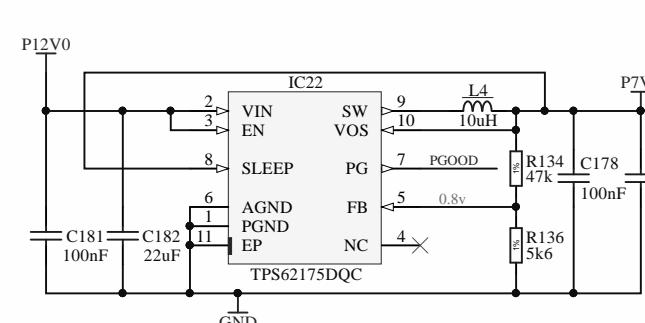
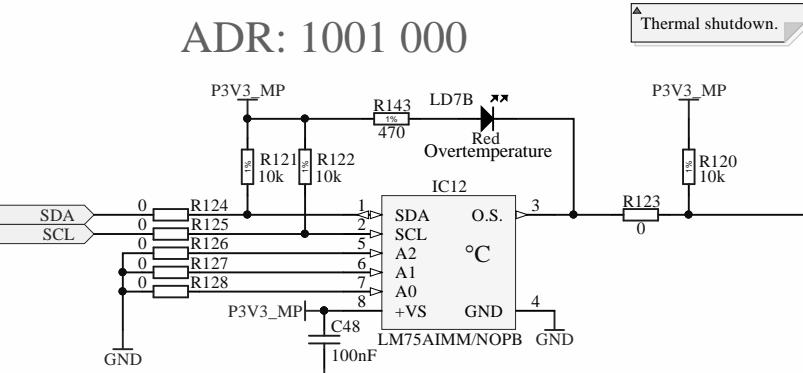
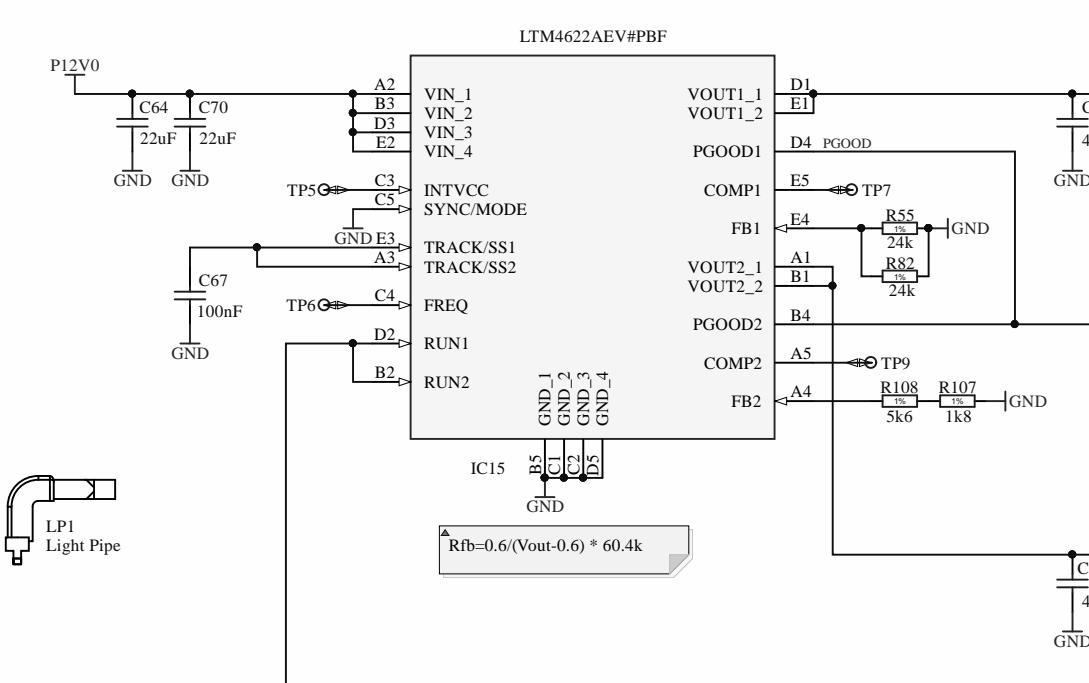
3U VCO/PLL (MIRNY) v1.0
Top entity

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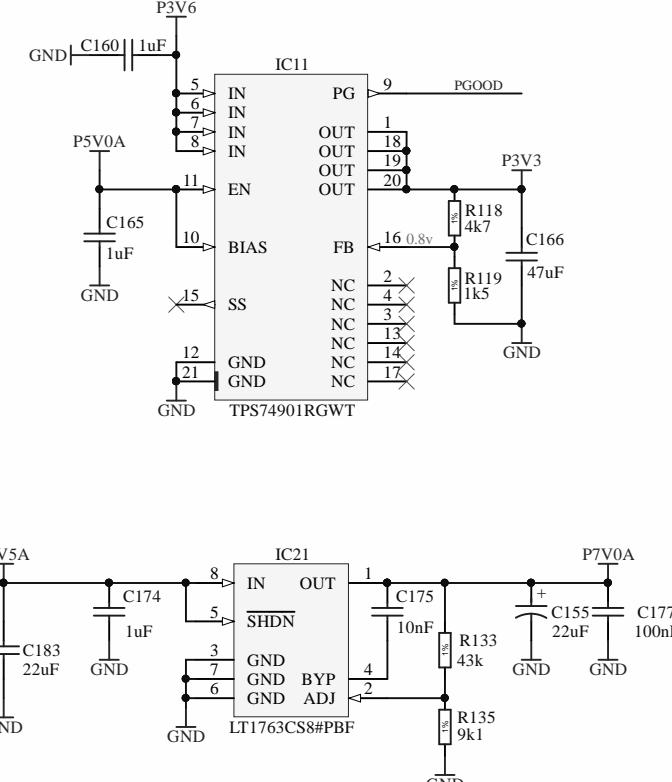
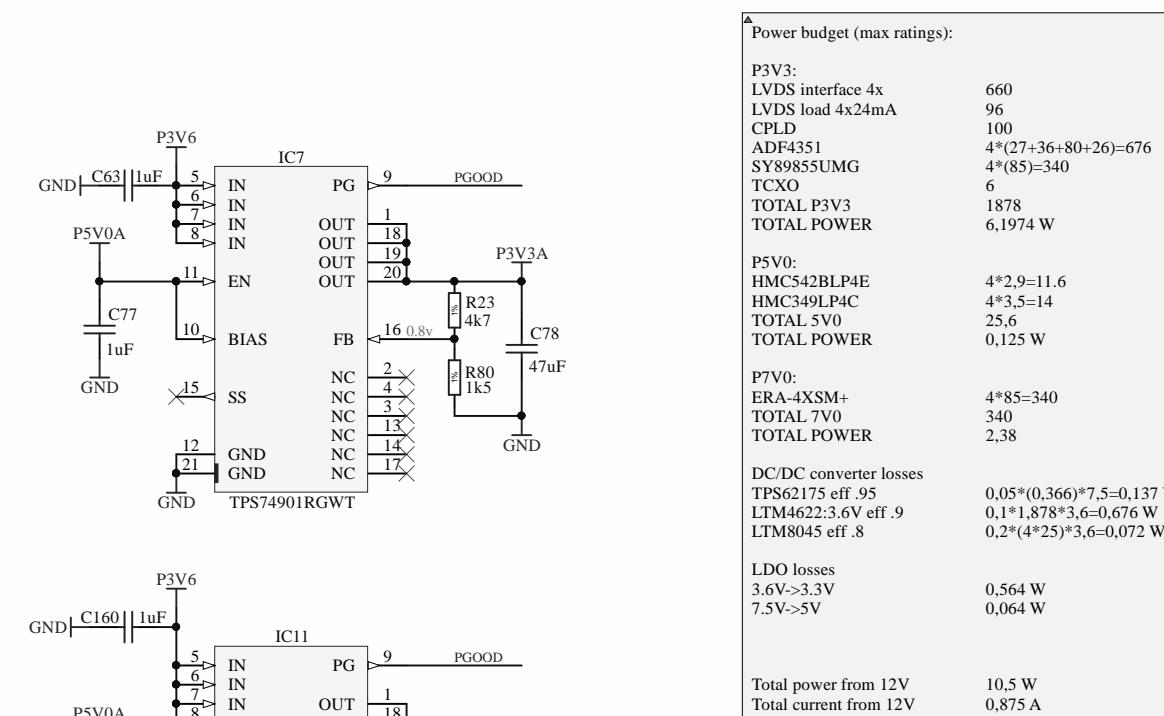
Nowowiejska 15/19

Designer K.B.	Drawn by K.B.	XX/XX/XXXX
Check-by	-	
Last Mod.	-	2018-12-06
File Mirny.schdoc	Print Date 2018-12-06 14:27:39	Sheet 1 of 8
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ARTIQ



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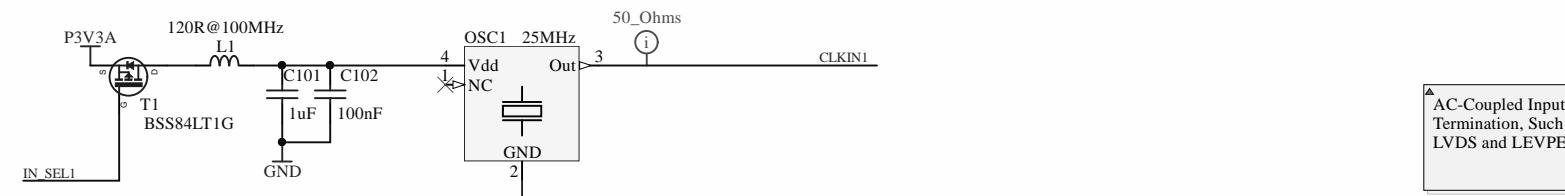
Power budget (max ratings):	
P3V3:	660
LVDS interface 4x	96
LVDS load 4x24mA	100
CPLD	100
ADF4351	4*(27+36+80+26)=676
SY8985UMG	4*(85)=340
TCXO	6
TOTAL P3V3	1878
TOTAL POWER	6,1974 W
P5V0:	4*2,9=11.6
HMC542BLP4E	4*3,5=14
HMC349LP4C	25,6
TOTAL 5V0	0,125 W
TOTAL POWER	0,125 W
P7V0:	4*85=340
ERA-4XSM+	340
TOTAL 7V0	2,38
TOTAL POWER	2,38
DC/DC converter losses	0,05*(0,366)*7,5=0,137 W
TPS62175 eff .95	0,1*1,878*3,6=0,676 W
LTM4622:3.6V eff .9	0,2*(4*25)*3,6=0,072 W
LDO losses	0,564 W
3.6V->3.3V	0,064 W
Total power from 12V	10,5 W
Total current from 12V	0,875 A

N5V5A \oplus TP8
P3V3 \oplus TP12
P3V3A \oplus TP13
P3V3_MP \oplus TP14
P3V0A \oplus TP15
P5V0A \oplus TP16
P5V5A \oplus TP10
P7V0A \oplus TP17
P12V0 \oplus TP18

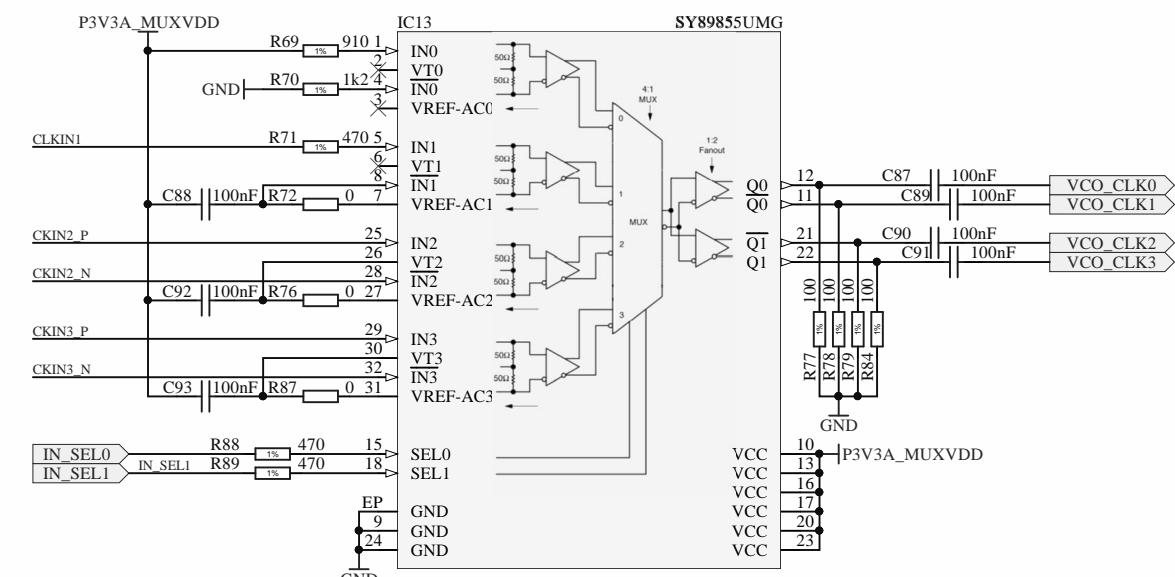
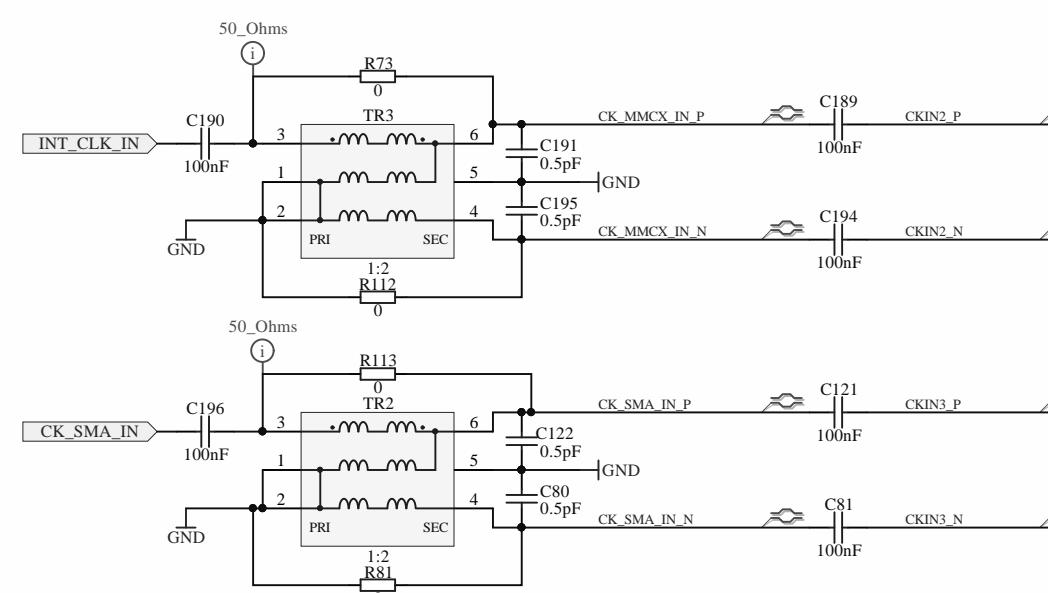
Project/Equipment	ARTIQ/SINARA
Document	Designer K.B. Drawn by K.B. XX/XX/XXXX
Cannot open file D:\Dropbox\DESIGN\SMTCASES\SI	Check by - Last Mod. - 2018-12-05
File Supply_VCO.SchDoc	File Supply_VCO.SchDoc
Warsaw University of Technology Nowowiejska 15/19	Print Date 2018-12-06 14:27:39
ISE	Sheet 2 of 8
ARTIQ	Size A3 Rev -

Power supply DC/DC & LDOs

A



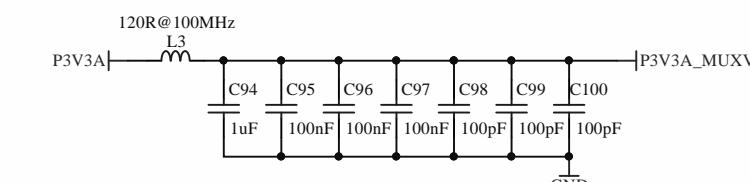
▲ AC-Coupled Input Termination, Such as LVDS and LEVPE



TRUTH TABLE

SEL1	SEL0	
0	0	IN0 Input Selected
0	1	IN1 Input Selected
1	0	IN2 Input Selected
-	-	XO MMCX SMA

-
XO
MMCX
SMA



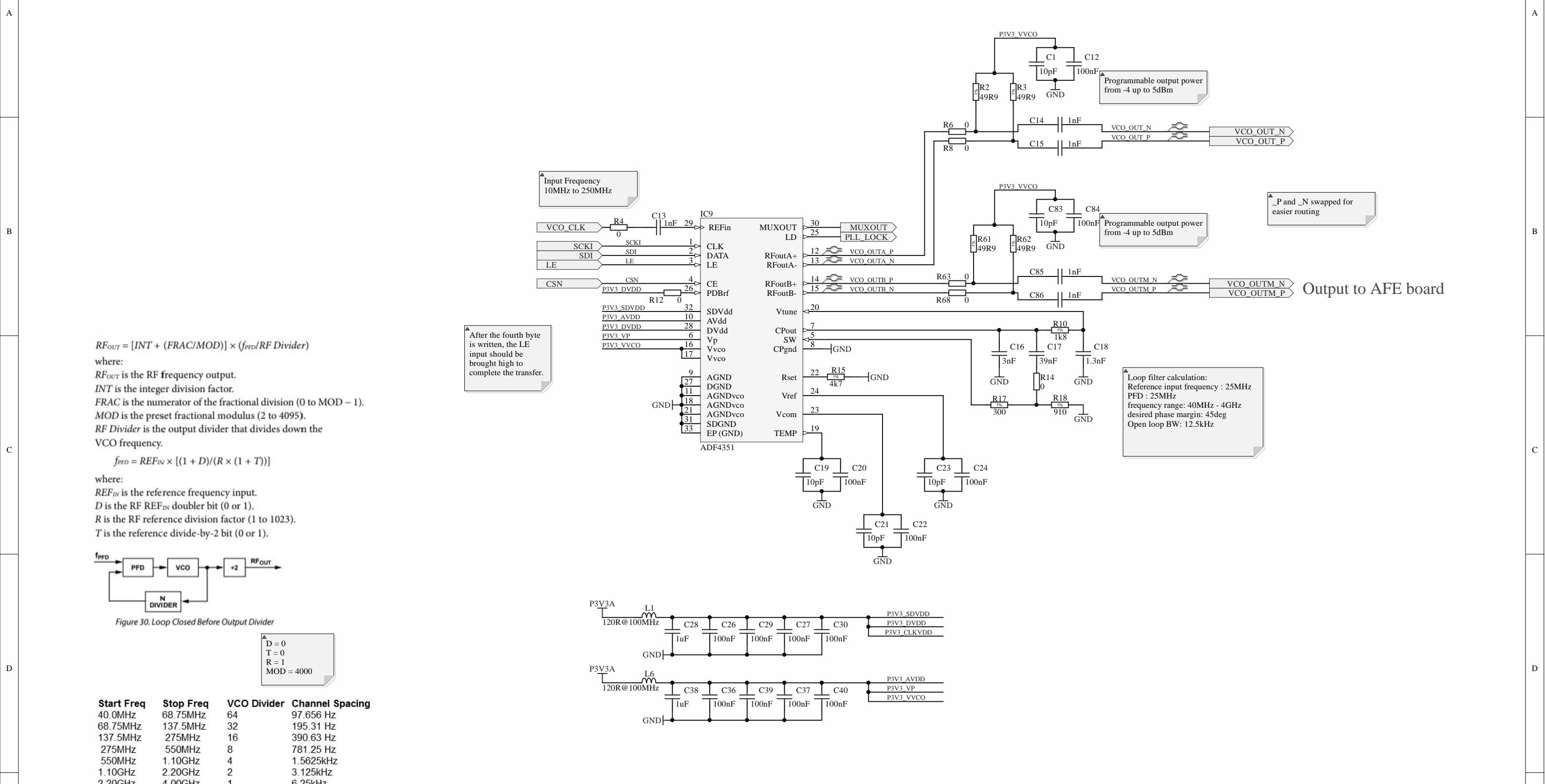
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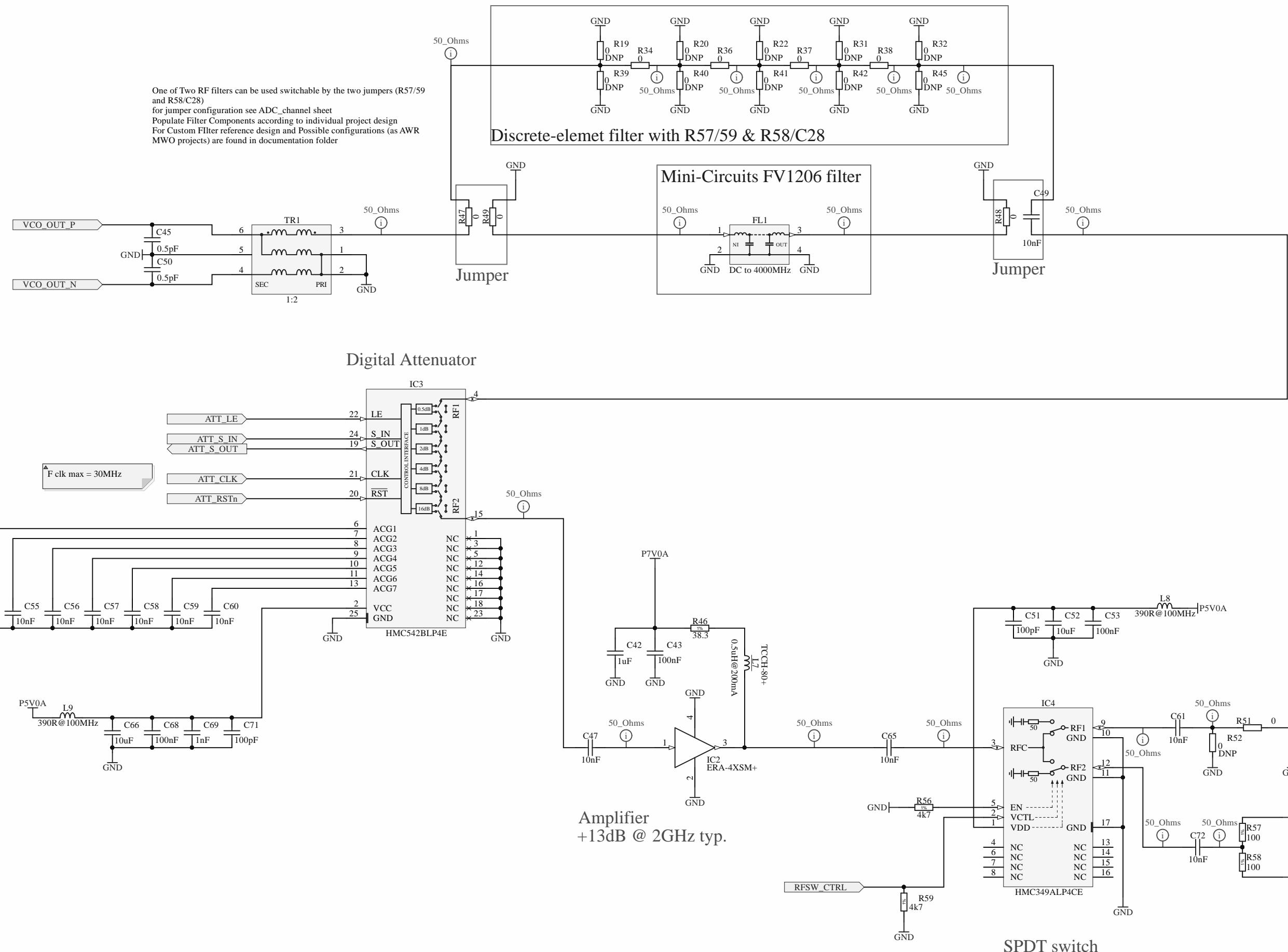
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Clock distribution and generation

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		Print Date 2018-12-06 14:27:39	Sheet 3 of 8
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		ARTIQ	





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**Output stage :
Attenuator, amplifier and filter**

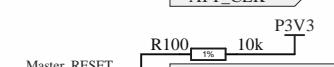
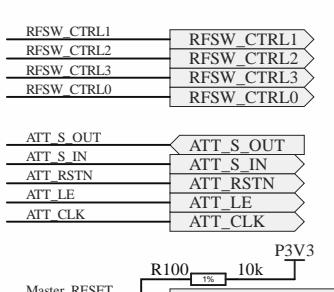
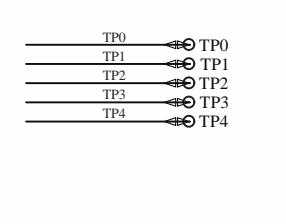
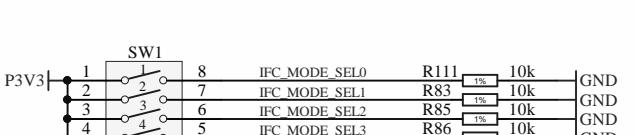
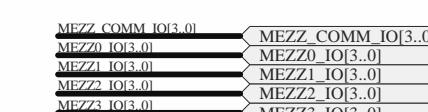
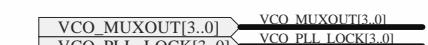
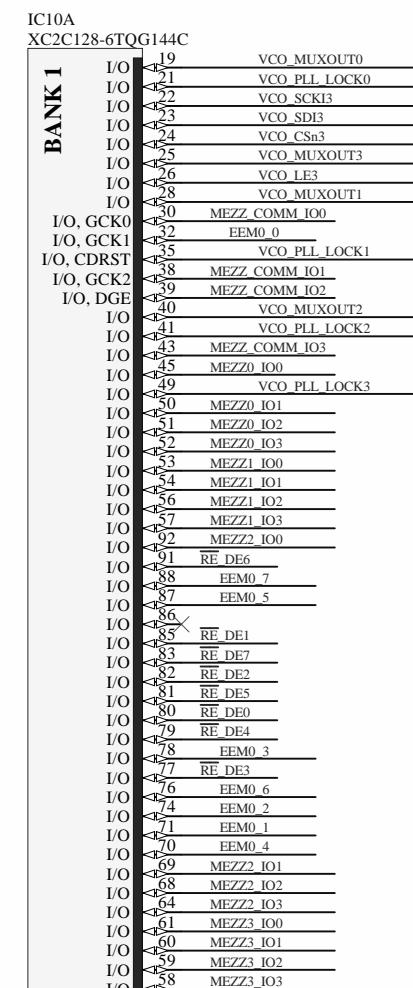
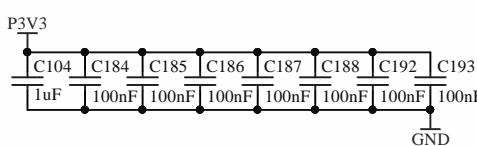
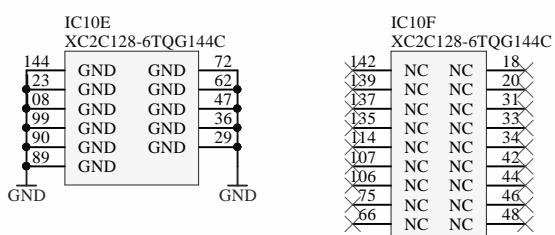
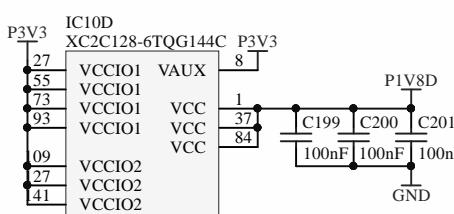
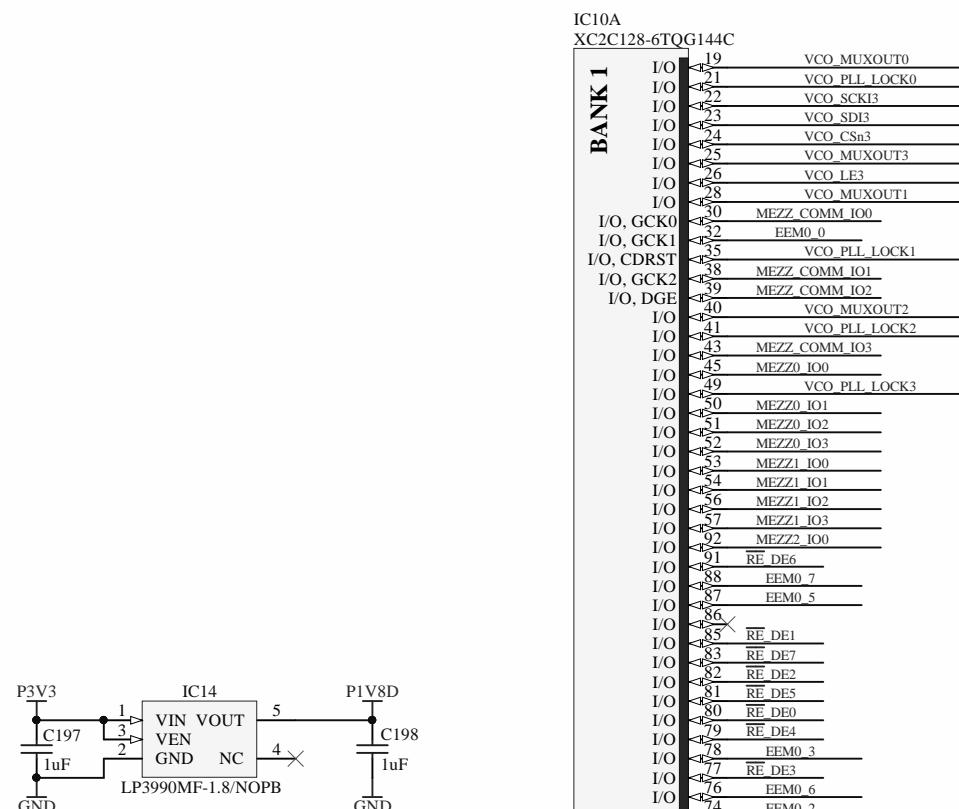
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Nowowiejska 15/19

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File VCO_OUT_channel.SchDoc	Print Date 2018-12-06 14:27:40	Sheet 5 of 8

Size A3 Rev -

ARTIQ

A



A

B

C

D

E

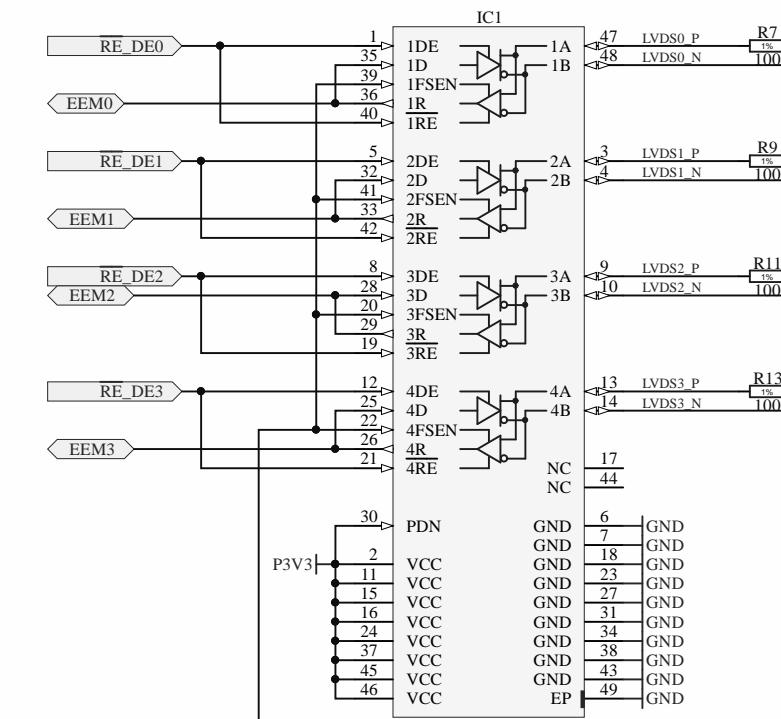
A

B

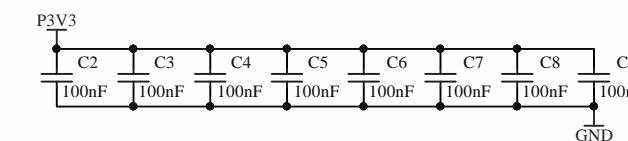
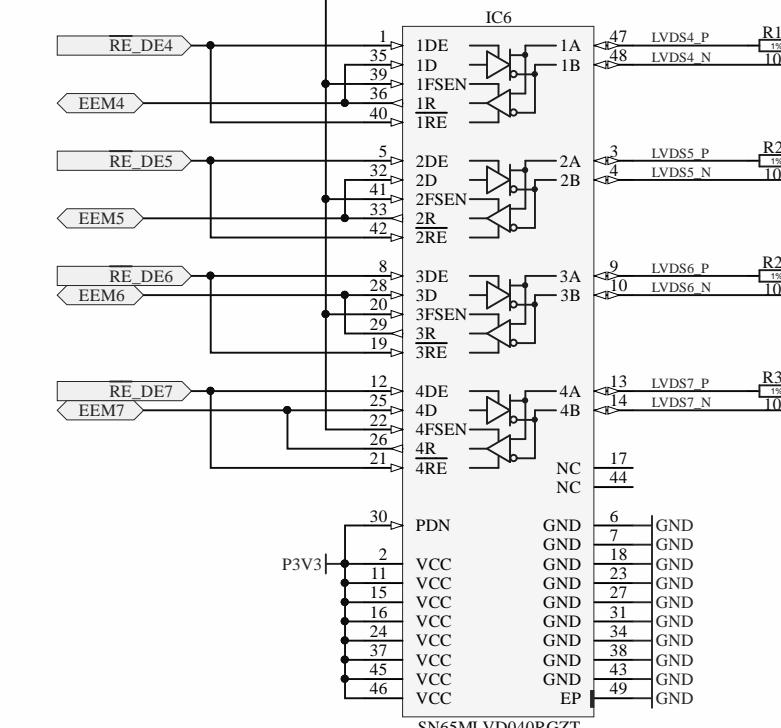
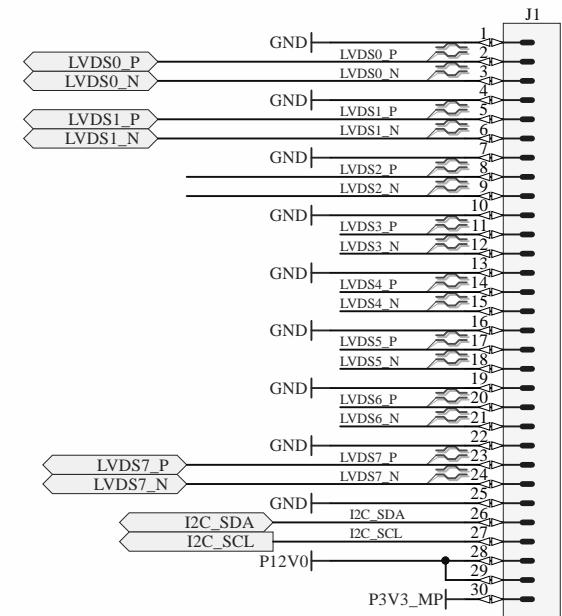
C

D

E



EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A



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File LVDS IFC_VCO.SchDoc	Print Date 2018-12-06 14:27:40	Sheet 7 of 8

Size A3	Rev -
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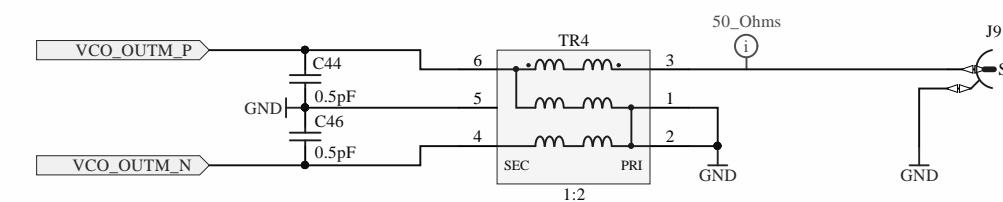
LVDS to LVTTL
interface & EEM connector

ARTIQ

A

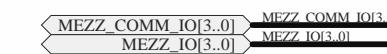
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Board-2-Board Analog Connectors

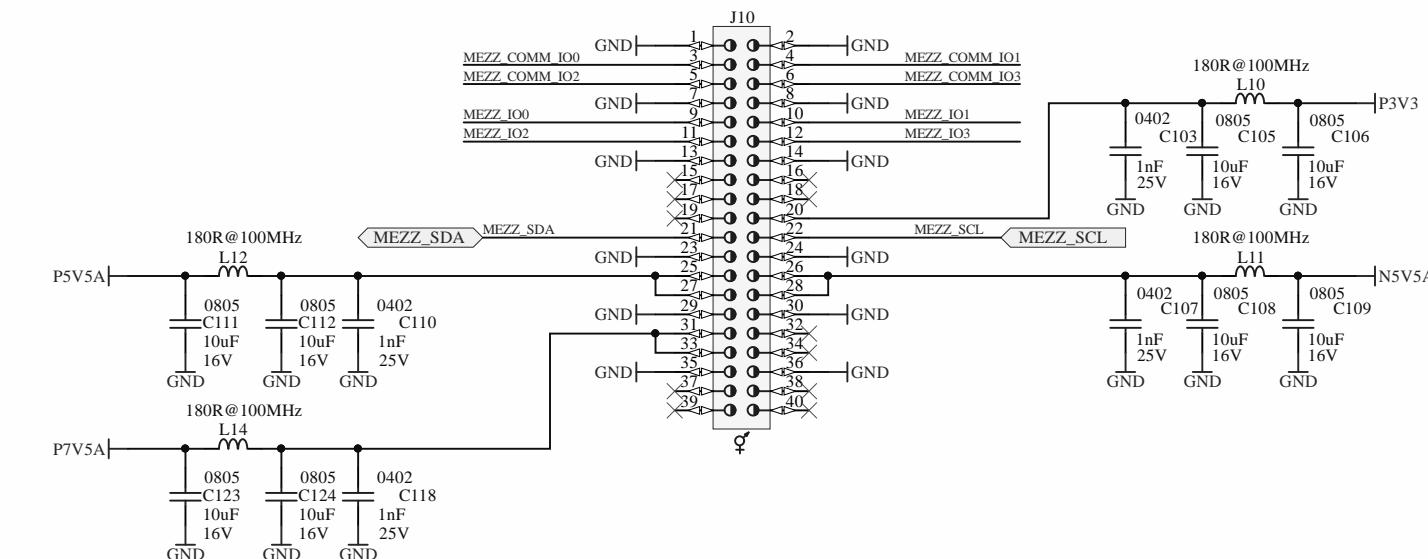


B

B



Board-2-Board Digital Connectors



C

C

D

D

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Last Mod. - 2018-12-06
File B2B_connectors.SchDoc
Print Date 2018-12-06 14:27:40

AFE Mezzanine Connectors

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Last Mod. -	2018-12-06	
File B2B_connectors.SchDoc	Print Date 2018-12-06 14:27:40	Sheet 8 of 8
		Size A3 Rev -

ARTIQ

E

TP0 TP2 TP4
TP1 TP3

Mirny v1.0
WUT ISE 2018

IC5

OSC1
IC13

LD4

P3U3A

LD3

P3U3

LD1

P3U6

LD12

P5U5A

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

P5U0A

LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

P5U0A

LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

P5U0A

LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

P5U0A

LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

P5U0A

LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

P5U0A

LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

P5U0A

LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

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LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

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LD11

J2

LD7

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LD9

J7

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LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

P5U0A

LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

P5U0A

LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

P5U0A

LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

P5U0A

LD1

P3U0

LD3

P3U3_MP

LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

J2

LD7

P7U0

LD9

J7

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J7

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LD1

P3U0

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LD12

P5U5

LD15

IC15

IC22

IC20

N7U5A

LD11

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LD1

P3U0

<p



ARTIQ

Mirny v1.0

IC14

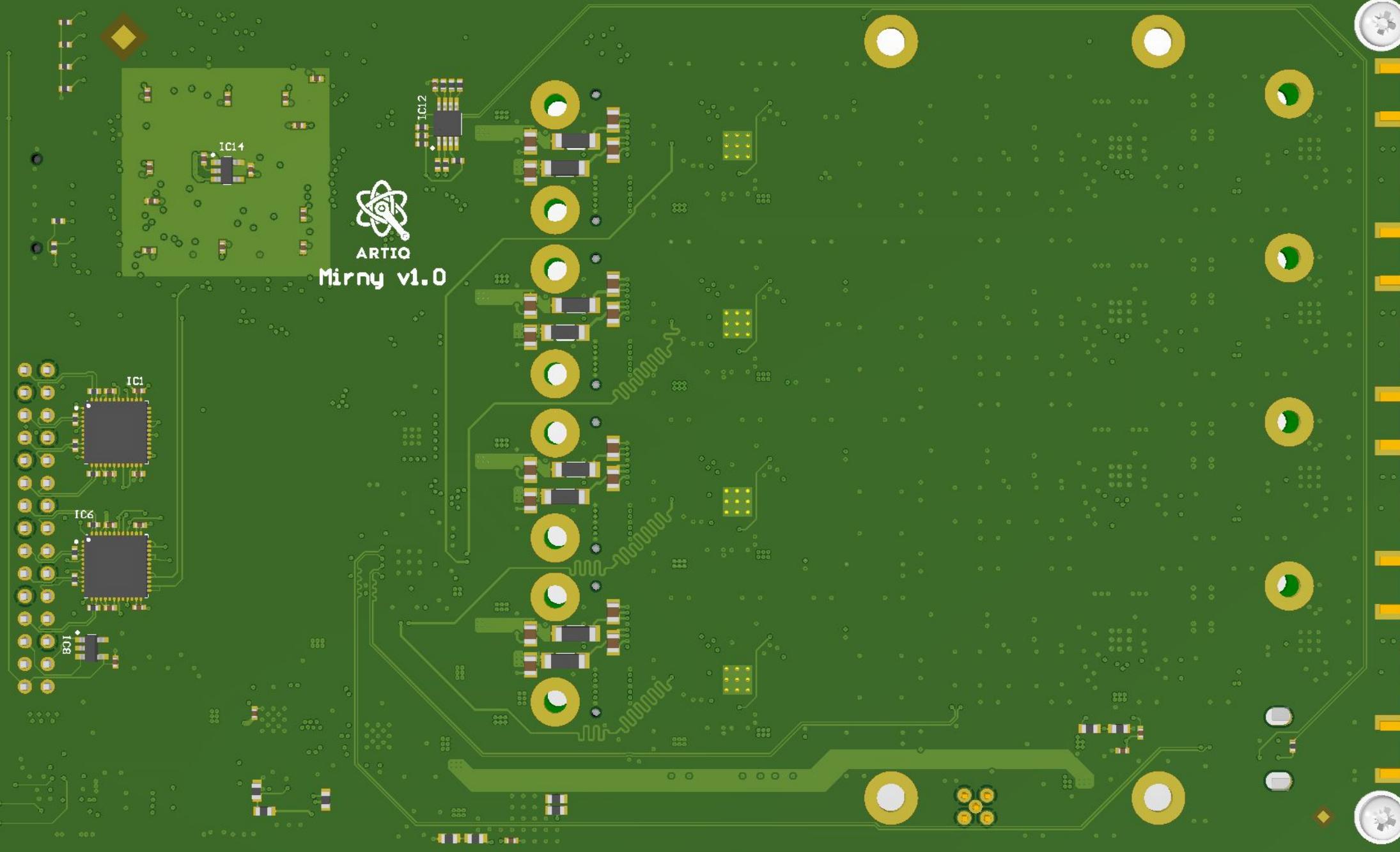
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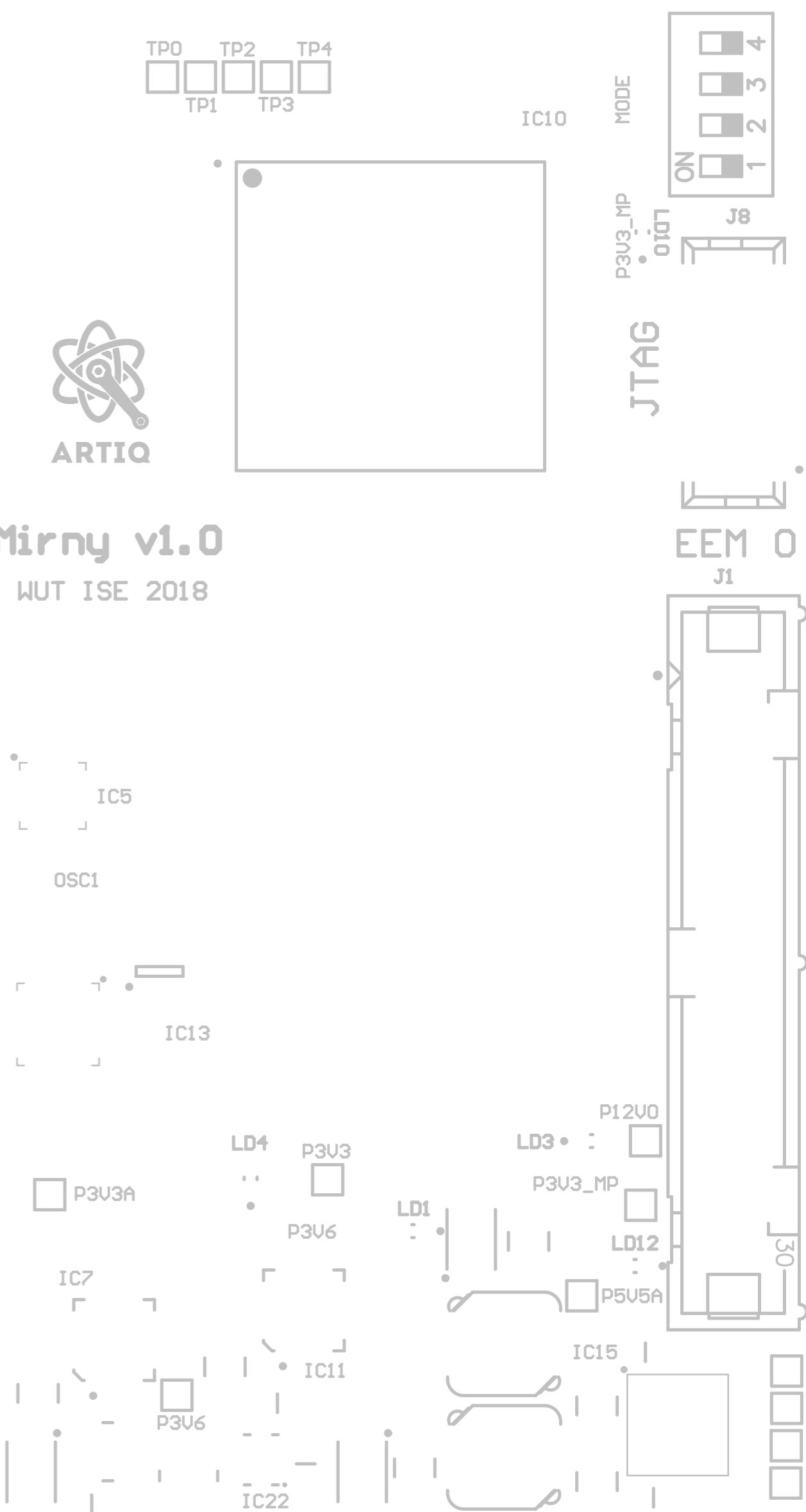
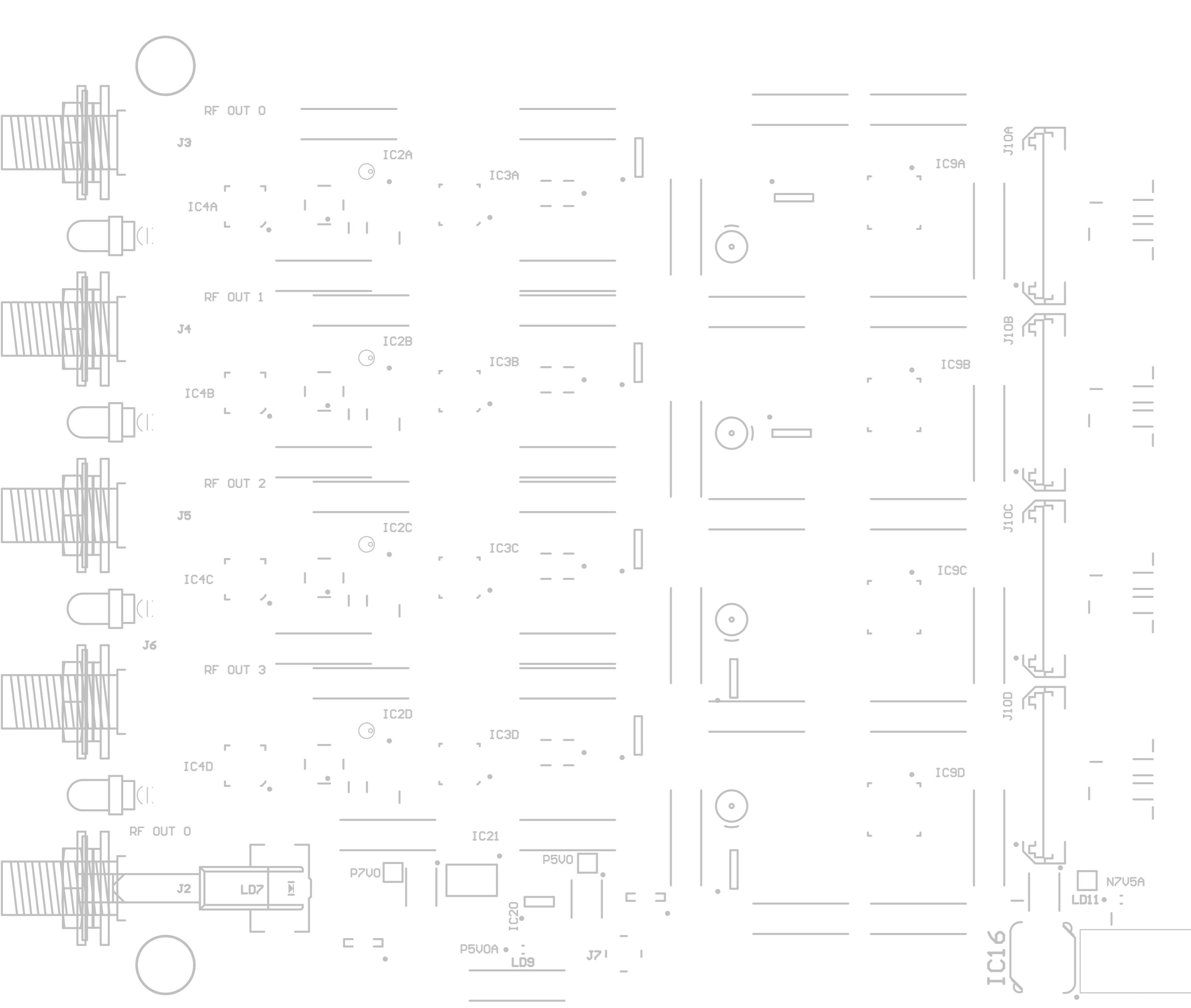


IC1

IC6

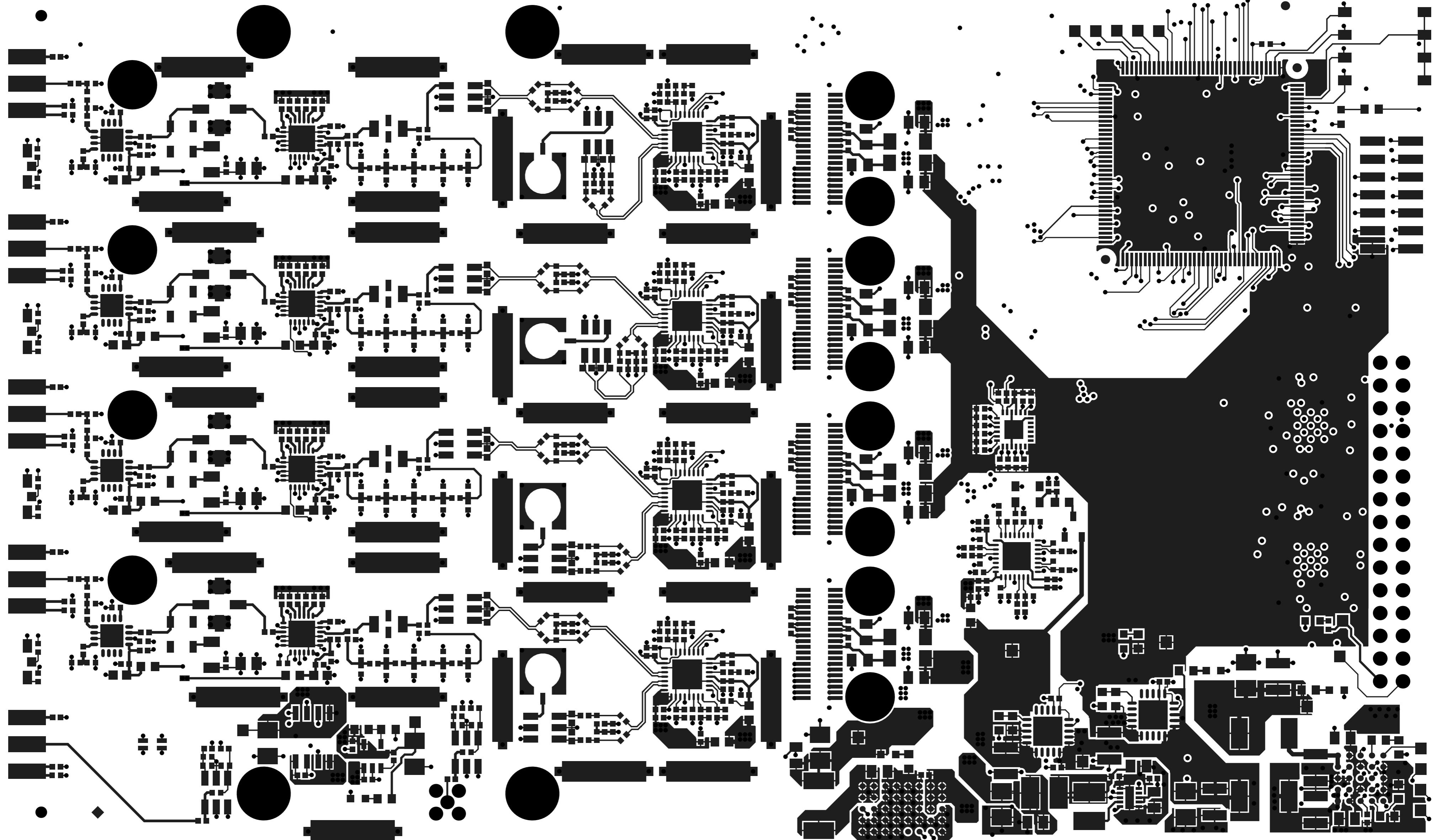
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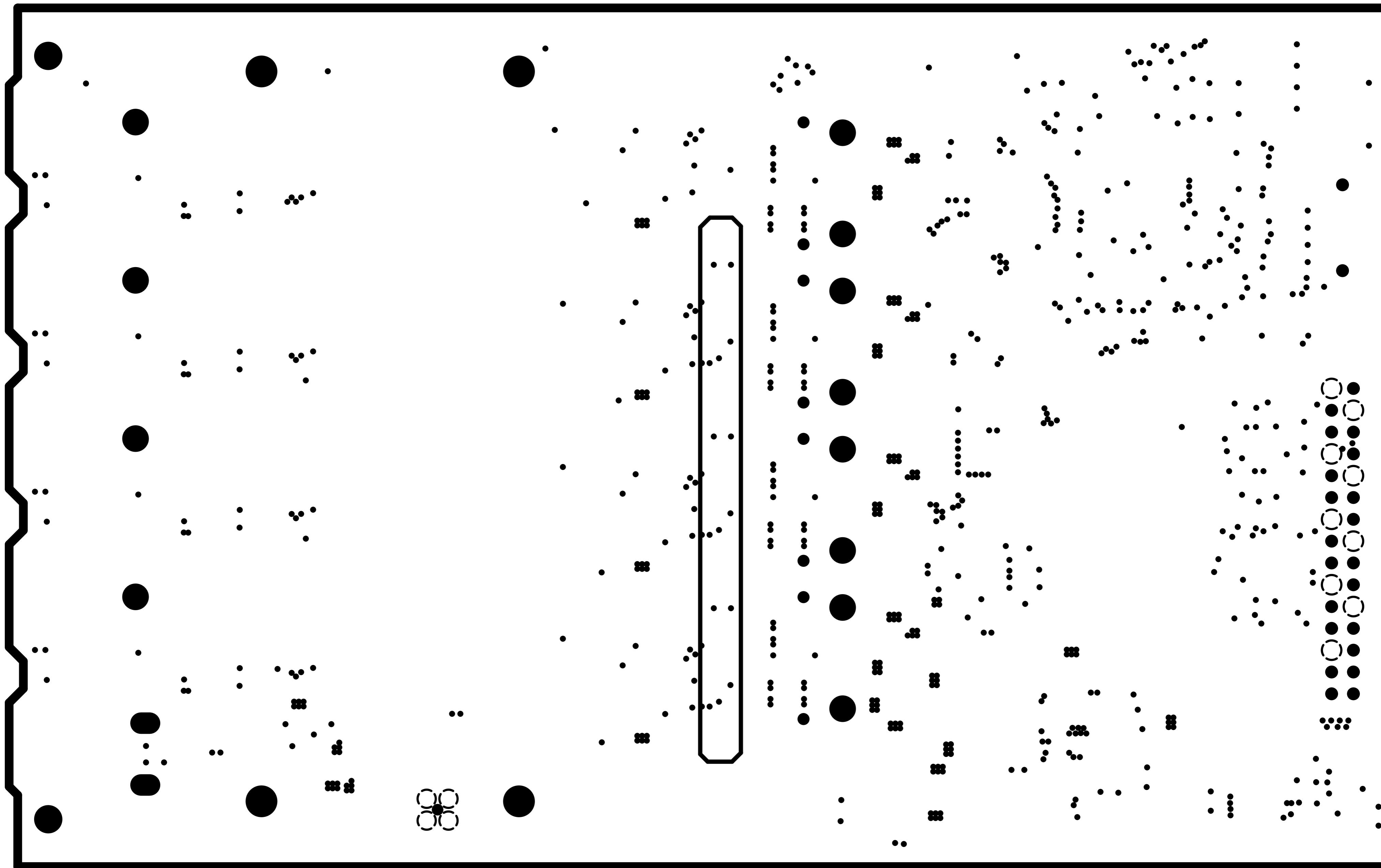


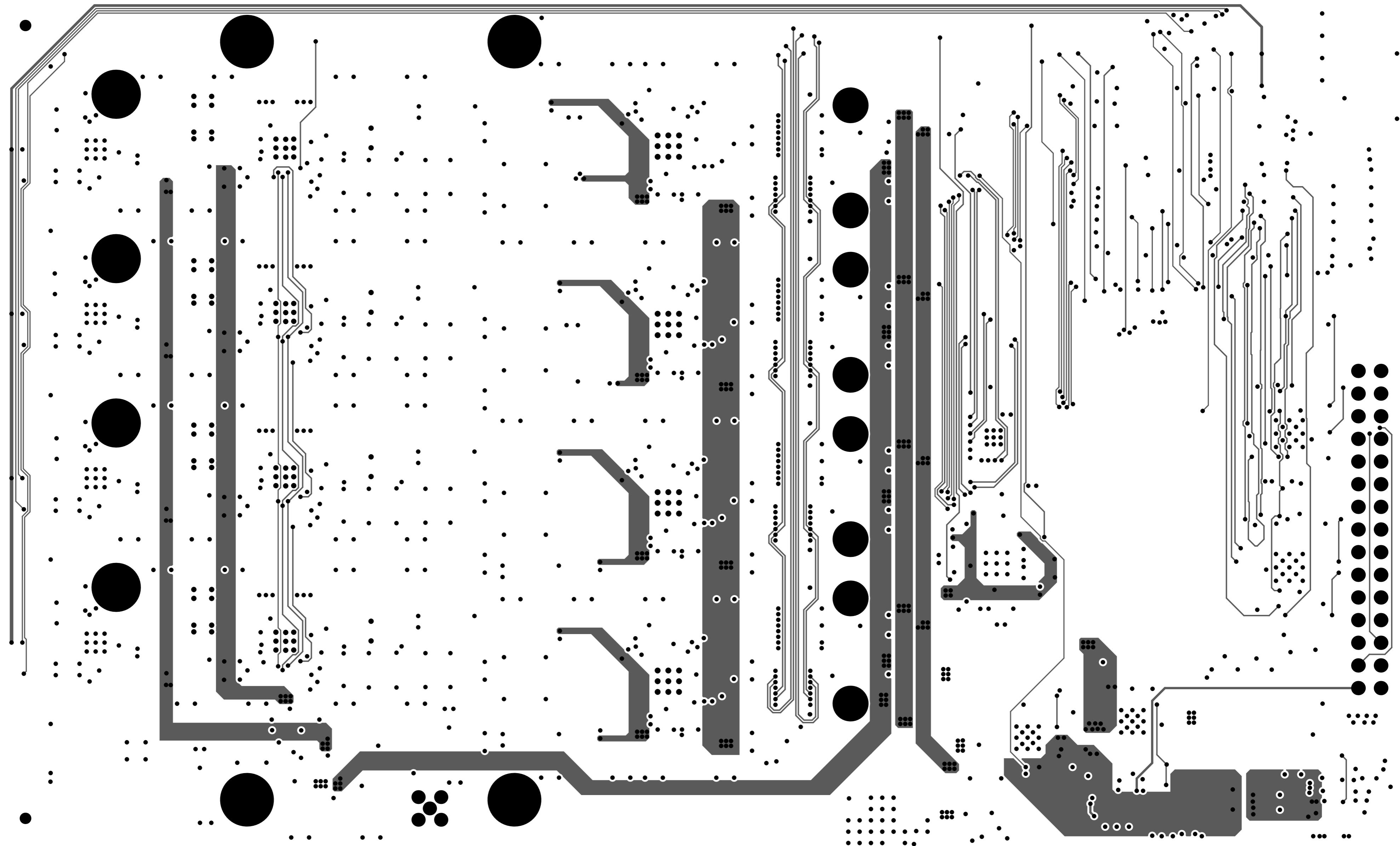


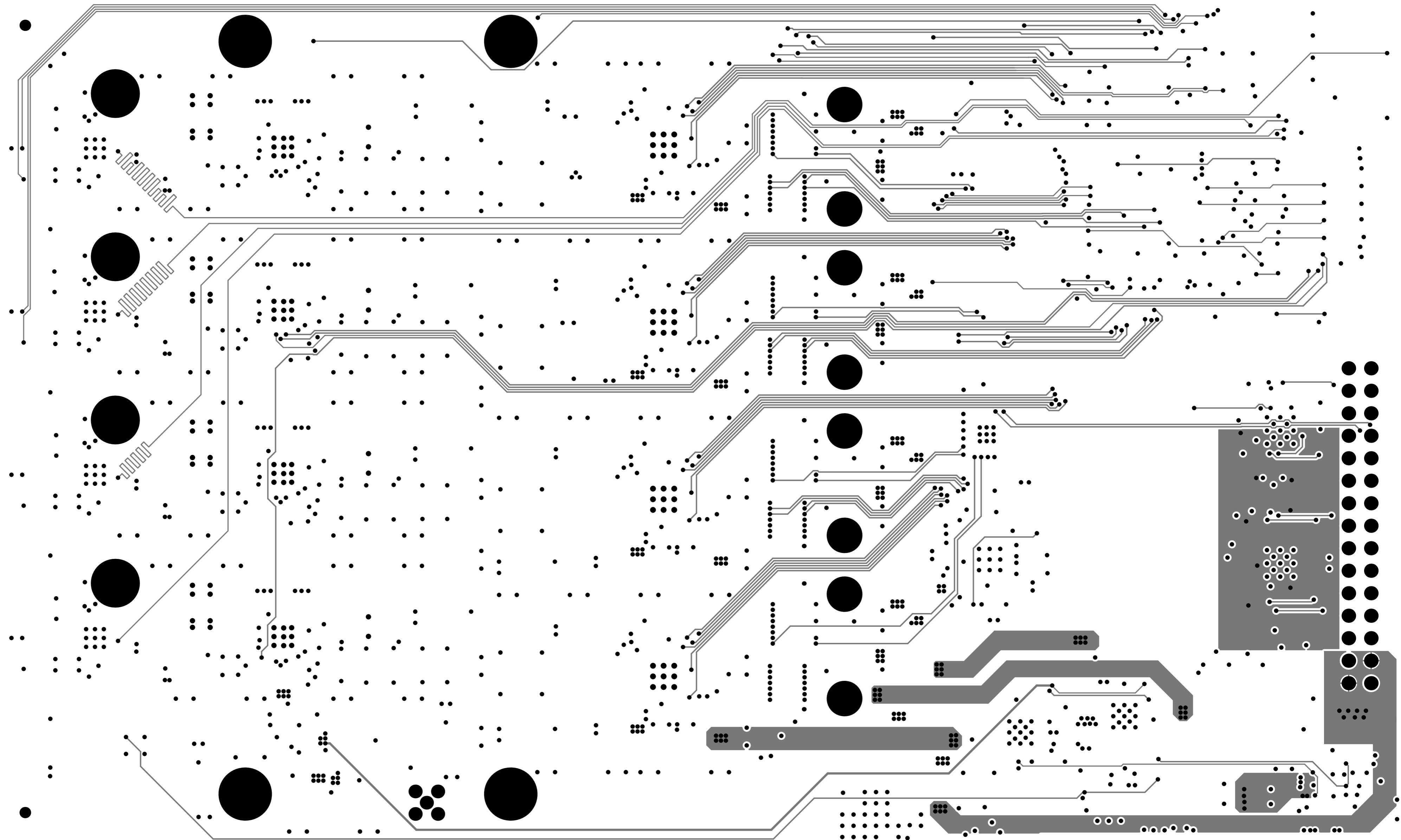
Mirny v1.0
WUT ISE 2018

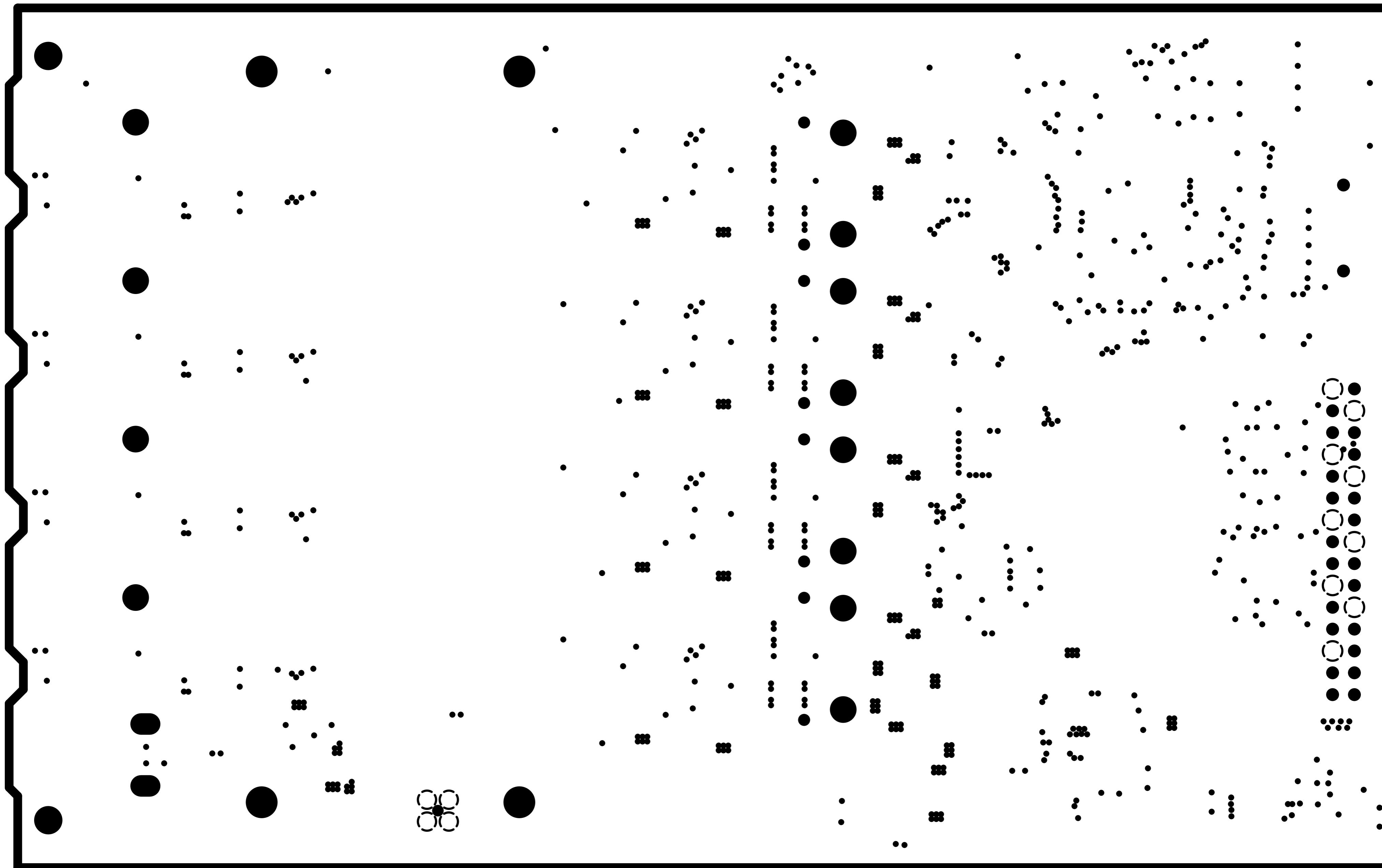


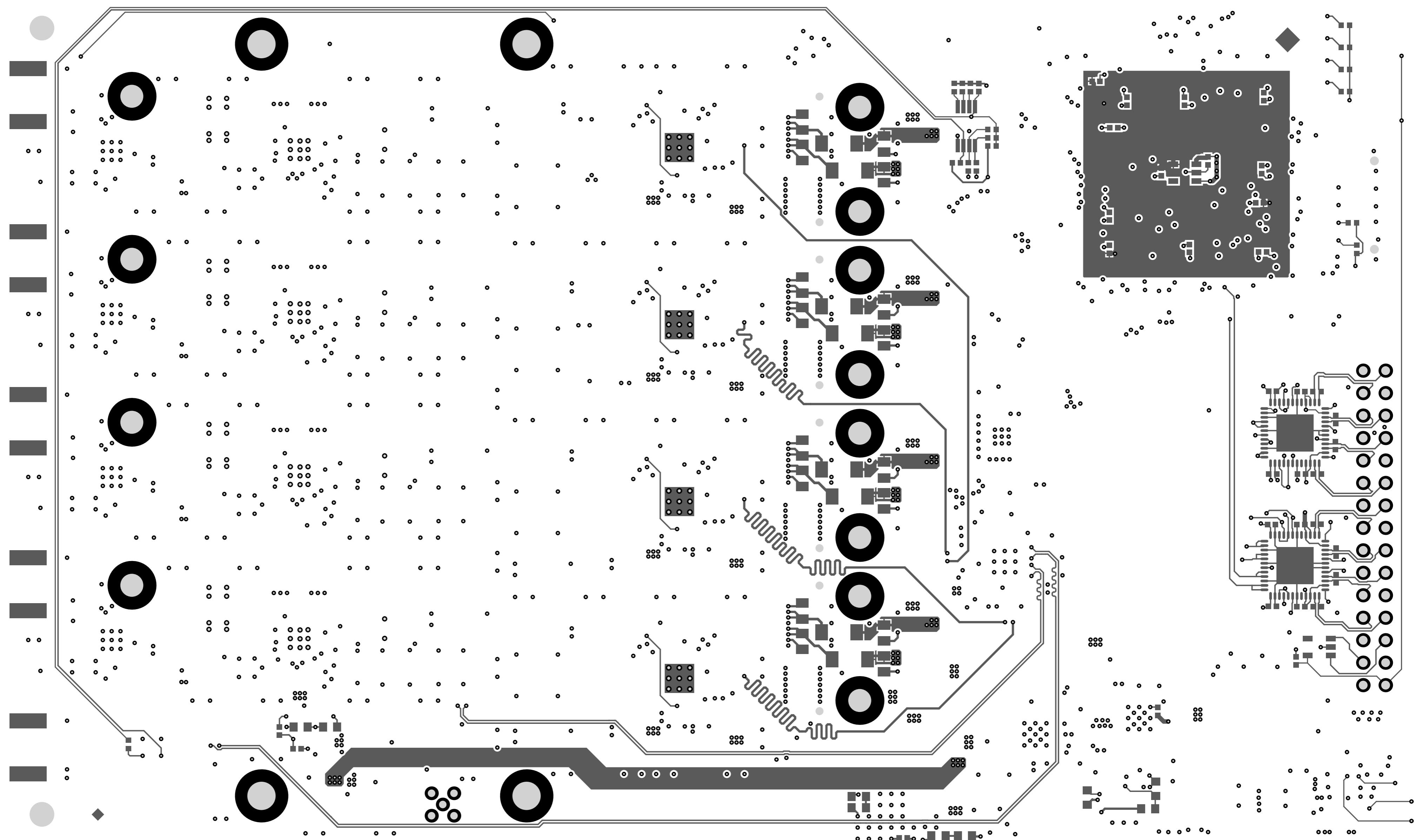












IC8

IC6

IC1

IC14

IC15



Mifrah Atto

ARATIO



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	1,34mil	3,5	
3	L1	Copper	2,28mil		
4	Dielectric1	FR4	7,09mil	3,66	
5	P2	Copper	0,71mil		
6	Dielectric 9	FR4	18,11mil	4,2	
7	L3	Copper	0,71mil		
8	Dielectric 8		7,09mil	4,2	
9	L4	Copper	0,71mil		
10	Dielectric4	FR4	18,11mil	4,2	
11	P5	Copper	0,71mil		
12	Dielectric3	FR4	7,09mil	4,2	
13	L6	Copper	2,28mil		
14	Bottom Solder	Solder Resist	1,34mil	3,5	
15	Bottom Overlay				