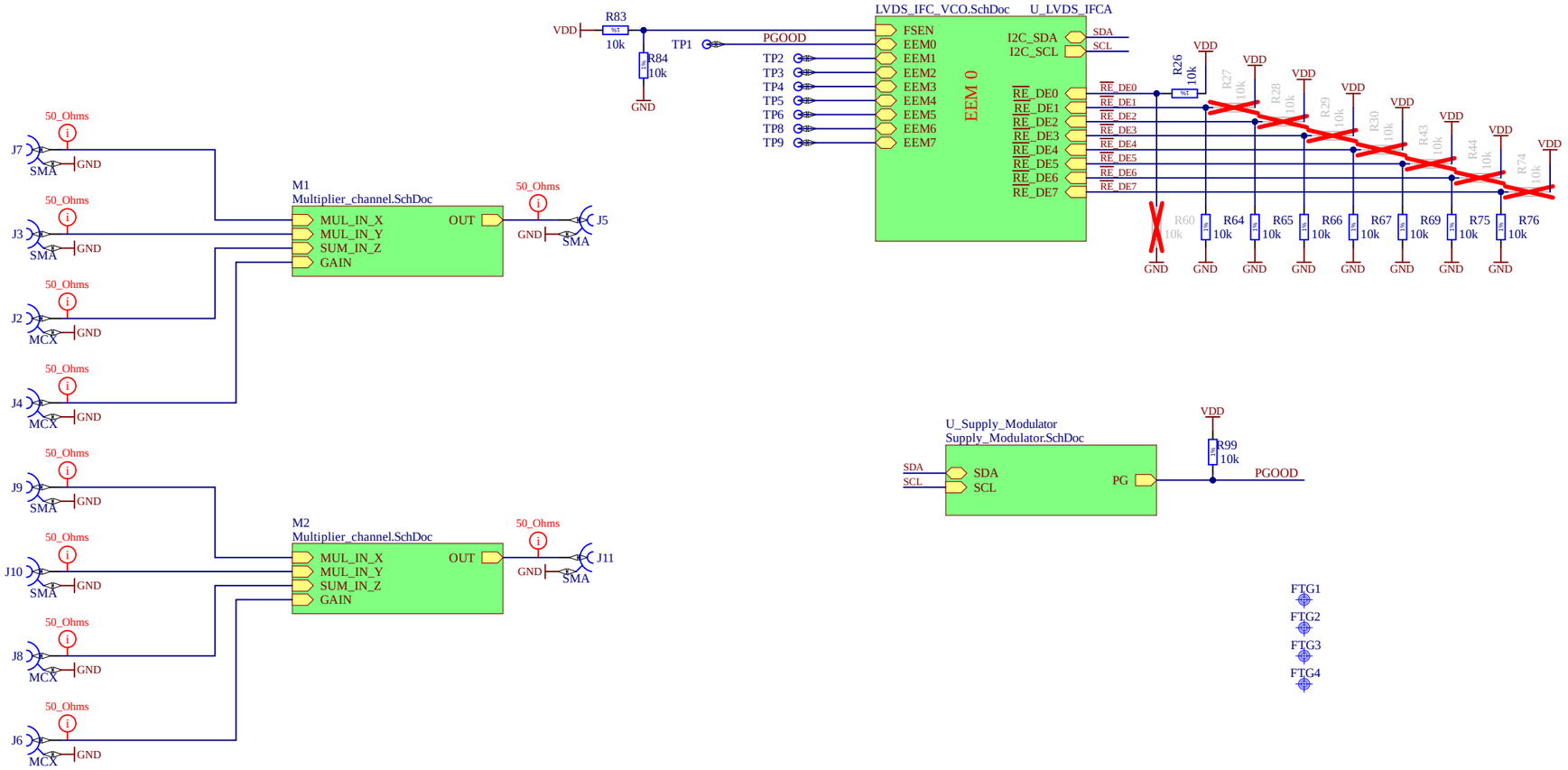
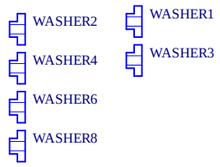
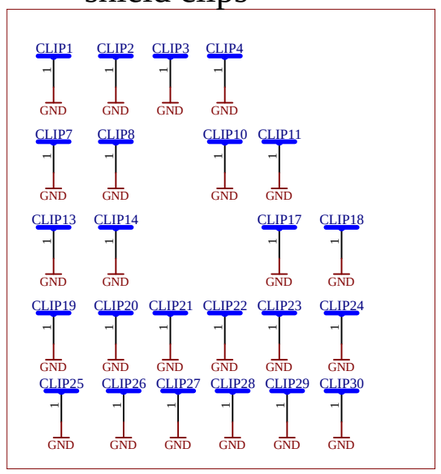


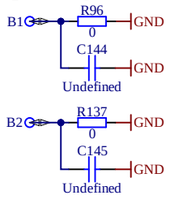
SMA Insulating washers



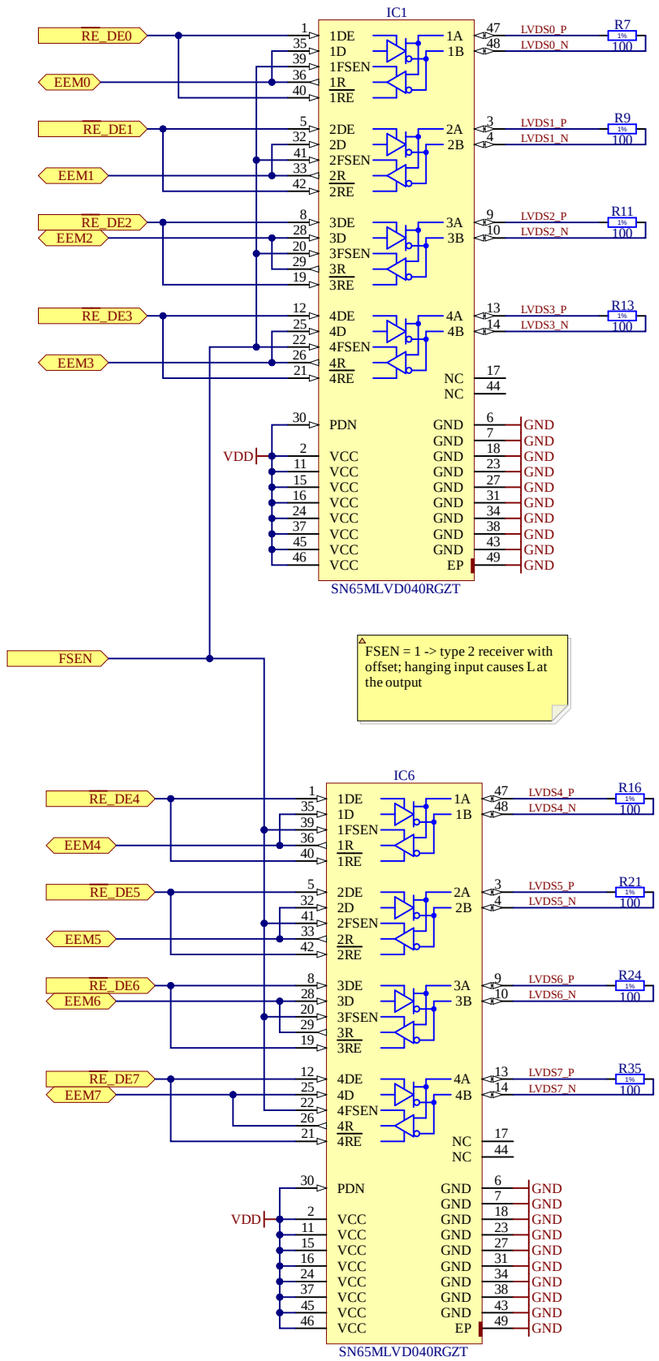
shield clips



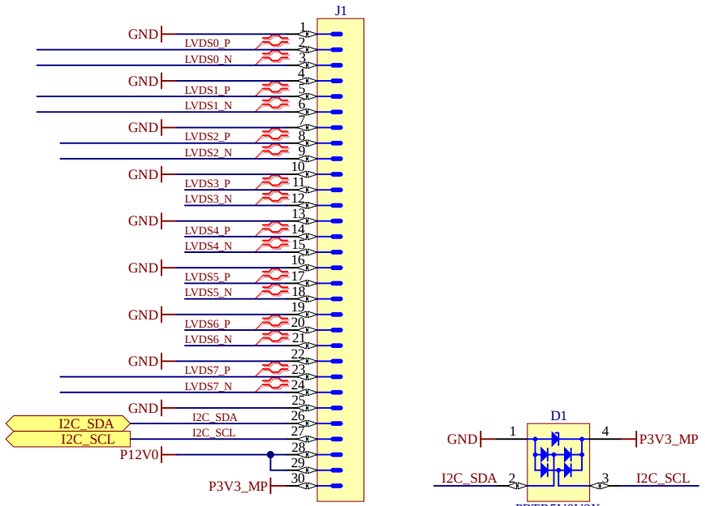
Front panel grounding

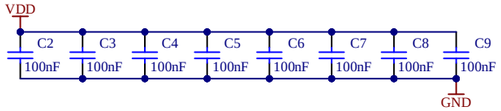


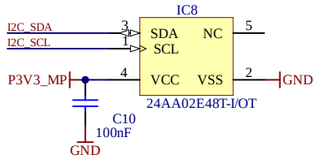
Project/Equipment	ARTIQ/SINARA		
Document	**Modulator v1.0** **Top entity**	Designer shanasz	
Cannot open file D:\Dropbox\DESIGNS\MTCA_projects\SI		Drawn by shanasz	XX/XX/XXXX
		Check.by	-
		Last Mod. -	08.09.2023
		File Modulator.schdoc	
		Print Date 08.09.2023 14:44:24	Sheet 1 of 6
Warsaw Univeristy of Technology *Nowowiejska 15/19*	*ISE*	ARTIQ	Size A3 / Rev -



EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A







Project/Equipment	ARTIQ/SINARA		
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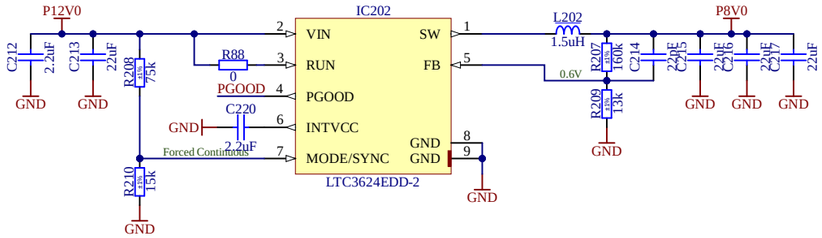
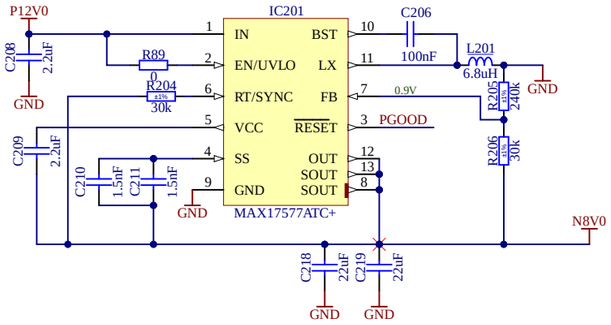
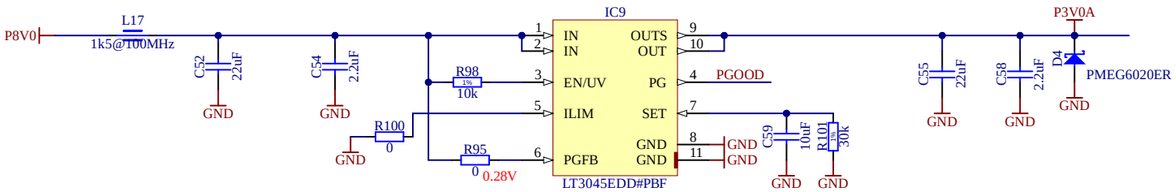
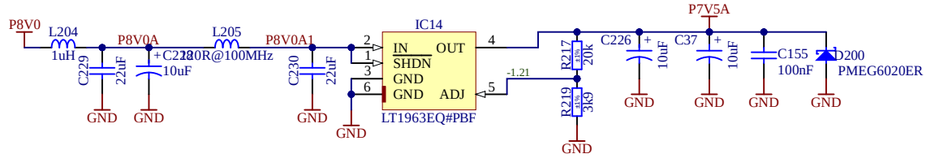
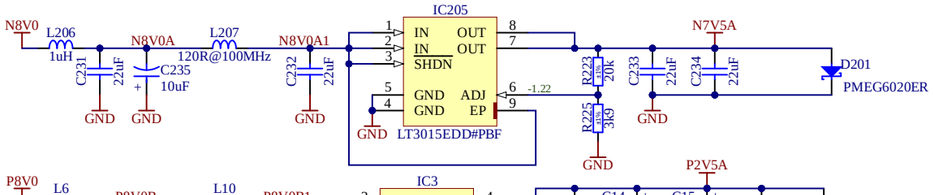
		Drawn by shanasz	XX/XX/XXXX
		Check.by	-
		Last Mod. -	08.09.2023
Cannot open file D:\Dropbox\DESIGNS\MTCA_projects\SI		File LVDS_IFC_VCO.SchDoc	
		Print Date 08.09.2023 14:44:25	Sheet 2 of 6
Warsaw Univeristy of Technology Nowowiejska 15/19	*ISE*	ARTIQ	Size A3 / Rev -

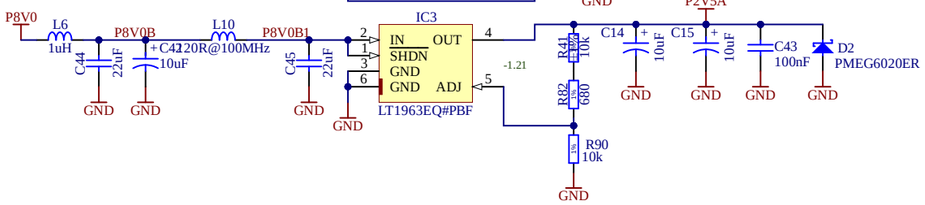


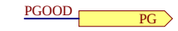


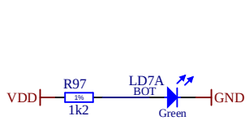






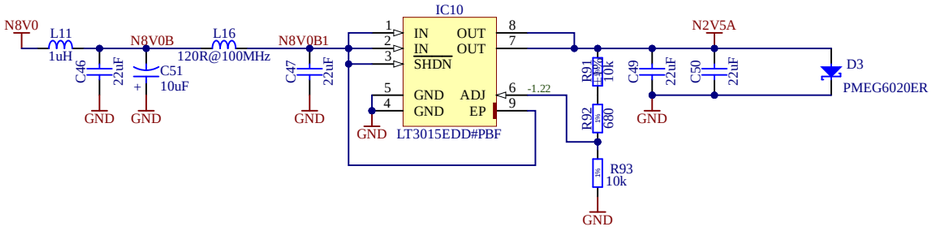


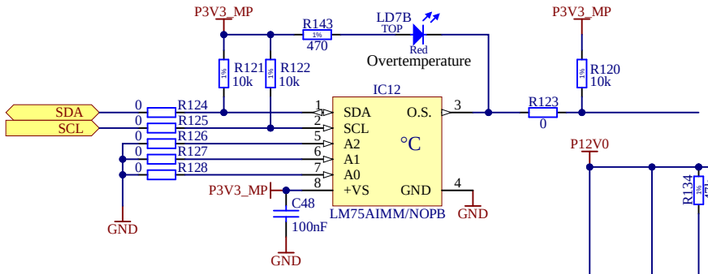




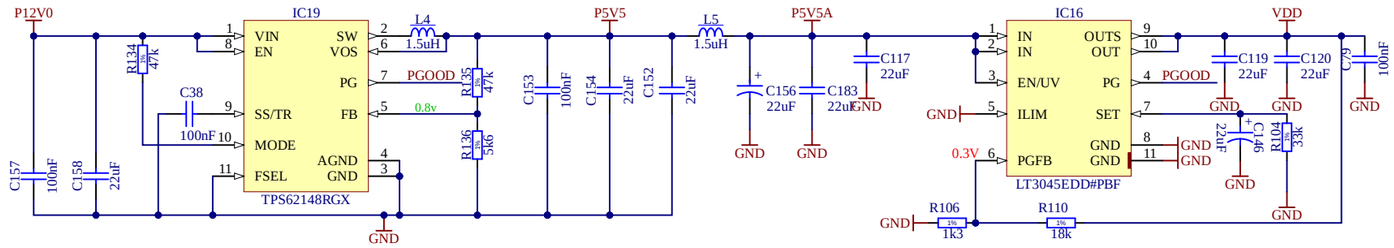
ADR: 1001 000

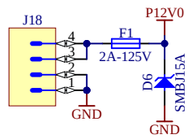
Thermal shutdown.

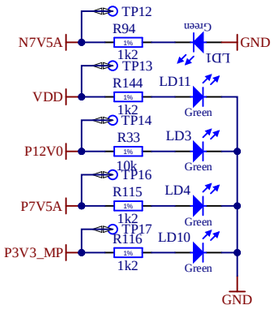




constant PWM
1.25MHz
slow start







Project/Equipment	ARTIQ/SINARA
Document	**Modulator v1.0** **DC/DC & LDOs**
Designer	shanasz
Drawn by	shanasz XX/XX/XXXX
Check.by	-
Last Mod.	- 08.09.2023
File	Supply_Modulator.SchDoc
Print Date	08.09.2023 14:44:25 Sheet 3 of 6
Cannot open file D:\Dropbox\DESIGNS\MTCA_projects\SI	Warsaw Univeristy of Technology Nowowiejska 15/19 ISE
	ARTIQ Size A3 Rev -

vs. Temperature Differential Output Impedance	f = dc f = 200 MHz f = 2 GHz	±19 0 75 500	mV Ω Ω Ω

50_Ohms
SW4A
R23A 0
R56A ±1% 8R2
R77A 442
R58A 0
SUM_IN_Z
IN1
IN_conditioning.SchDoc
IN_50R_500R
CM
OUT_P
OUT_N
MX_IN_Z_P
MX_IN_Z_N

SW1A
R78A 0
R22A ±1% 8R2
R80A 442
R79A 0
MUL_IN_Y
IN2
IN_conditioning.SchDoc
MX_IN_Y_P
MX_IN_Y_N

MUL_IN_X
IN3
IN_conditioning.SchDoc
MX_IN_X_P
MX_IN_X_N

Max 2Vpp = 10dBm @ 50R, for X,Y,Z

G=1

X and Y pins swapped for better signal integrity on PCB. Signals are crossed for the second time on OUT_conditioning sheet so the gain is positive/

Max 2Vpp differentially @ X,Y,Z

Multiplier inputs are matched to 500R @DC and 150R @ 2GHz. 100R line between amp and mult is shorter than 10mm, so no matching R is needed.

GAIN
R31A Undefined

Max 2,2Vpp differentially @ X = 2Vpp and Y = 1V

IC5A
ADL5391ACP
GADJ
ENBL
ZPLS
ZMNS
YPLS
YMNS
XPLS
XMNS
WPLS
WMNS
VMID
VPOS
VPOS
COMM
COMM
EP
P2V5
R32A 0
N2V5
L8A 120R@100MHz
L7A 120R@100MHz
C25A 100pF
C26A 100nF
C27A 4.7uF
C22A 100pF
C23A 100nF
C24A 4.7uF
C20A 100nF
GND
CM
MX_OUT_W_P
MX_OUT_W_N

OUT1
OUT_conditioning.SchDoc
IN_P
IN_N
OUT_RF
OUT

IOUTfs = 30mA
RI=24,95
Vfs=0.7485Vpp

EVALUATION BOARD

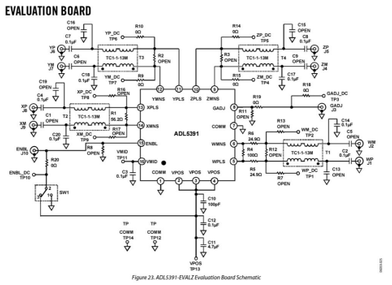


Figure 23. ADL5391-EVALZ Evaluation Board Schematic

Project/Equipment	ARTIQ/SINARA		
Document	***Modulator v1.0*** ***Modulator channel***	Designer shanasz	
		Drawn by shanasz	XX/XX/XXXX
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		Last Mod. -	08.09.2023
		File Multiplier_channel.SchDoc	
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Cannot open file D:\Dropbox\DESIGNS\MTCA_projects\SI	*Warsaw Univeristy of Technology* *Nowowiejska 15/19*	***ISE***	ARTIQ Size A3 Rev -

vs. Temperature Differential Output Impedance	f = dc f = 200 MHz f = 2 GHz	±19 0 75 500
		mV Ω Ω Ω

50_Ohms
SW4B
R23B 0
R56B ±1% 8R2
R77B 442
R58B 0
SUM_IN_Z
IN1
IN_conditioning.SchDoc
IN_50R_500R
CM
OUT_P
OUT_N
MX_IN_Z_P
MX_IN_Z_N

SW1B
R78B 0
R22B ±1% 8R2
R80B 442
R79B 0
MUL_IN_Y
IN2
IN_conditioning.SchDoc
MX_IN_Y_P
MX_IN_Y_N

MUL_IN_X
IN3
IN_conditioning.SchDoc
MX_IN_X_P
MX_IN_X_N

Max 2Vpp = 10dBm @ 50R, for X,Y,Z

G=1

X and Y pins swapped for better signal integrity on PCB. Signals are crossed for the second time on OUT_conditioning sheet so the gain is positive/

Max 2Vpp differentially @ X,Y,Z

Multiplier inputs are matched to 500R @DC and 150R @ 2GHz. 100R line between amp and mult is shorter than 10mm, so no matching R is needed.

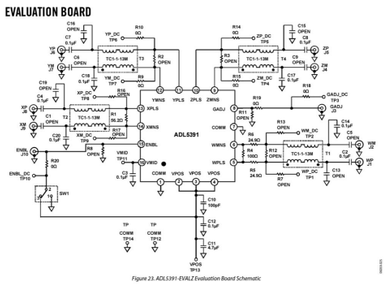
GAIN
R31B Undefined

Max 2,2Vpp differentially @ X = 2Vpp and Y = 1V

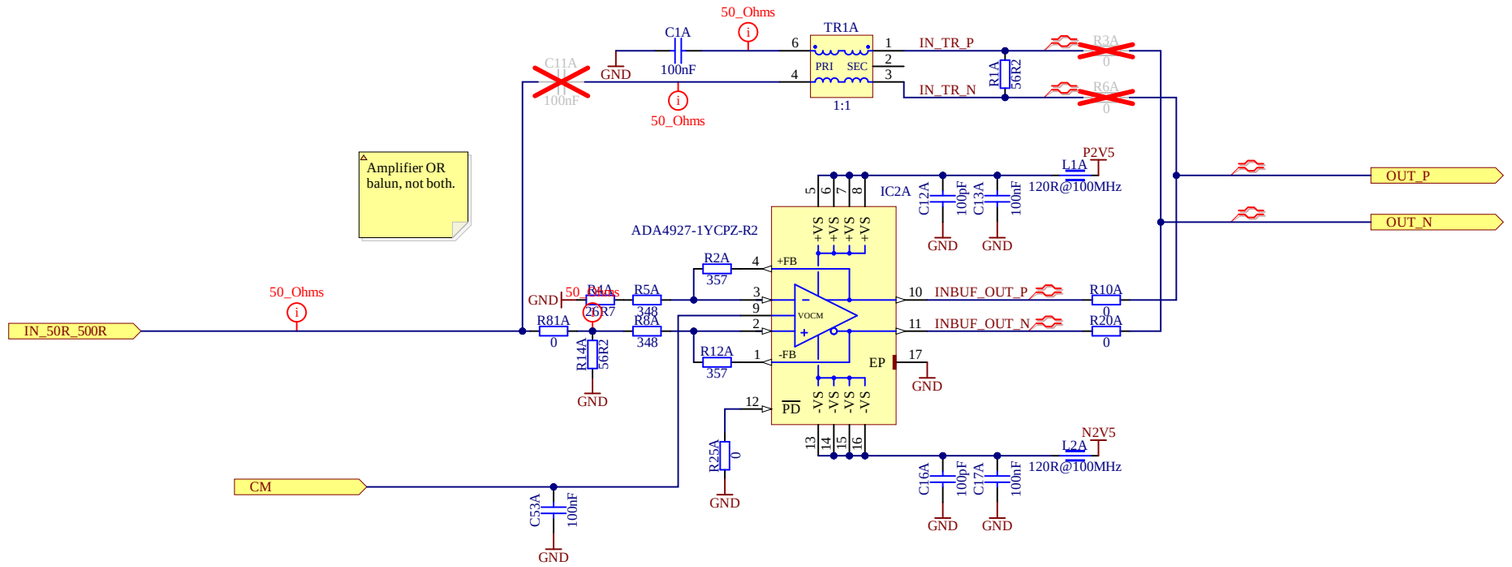
IC5B
ADL5391ACP
GADJ WPLS WMNS ENBL VMID ZPLS ZMNS VPOS VPOS YPLS YMNS VPOS COMM COMM XPLS XMNS EP
P2V5
R32B 0
N2V5
L8B 120R@100MHz
L7B 120R@100MHz
C25B 100pF
C26B 100nF
C27B 4.7uF
C22B 100pF
C23B 100nF
C24B 4.7uF
C20B 100nF
GND
CM

OUT1
OUT_conditioning.SchDoc
IN_P
IN_N
OUT_RF
OUT
MX_OUT_W_P
MX_OUT_W_N

IOUTfs = 30mA
RI=24,95
Vfs=0.7485Vpp



Project/Equipment	ARTIQ/SINARA			
Document	**Modulator v1.0** **Modulator channel**	Designer shanasz		
		Drawn by shanasz	XX/XX/XXXX	
		Check.by	-	
		Last Mod. -	08.09.2023	
		File Multiplier_channel.SchDoc		
		Print Date 08.09.2023 14:44:25	Sheet 4 of 6	
Cannot open file D:\Dropbox\DESIGNS\MTCA_projects\SI	*Warsaw Univeristy of Technology* *Nowowiejska 15/19* **ISE**	ARTIQ	Size A3	Rev -



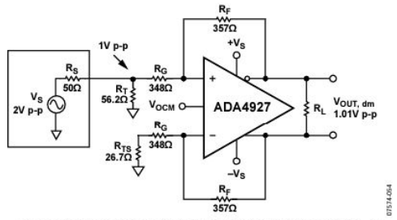


Figure 54. Terminated Single-Ended-to-Differential System with G = 1

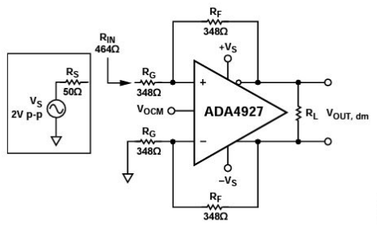


Figure 50. Calculating Single-Ended Input Impedance R_{IN}

Project/Equipment	ARTIQ/SINARA		
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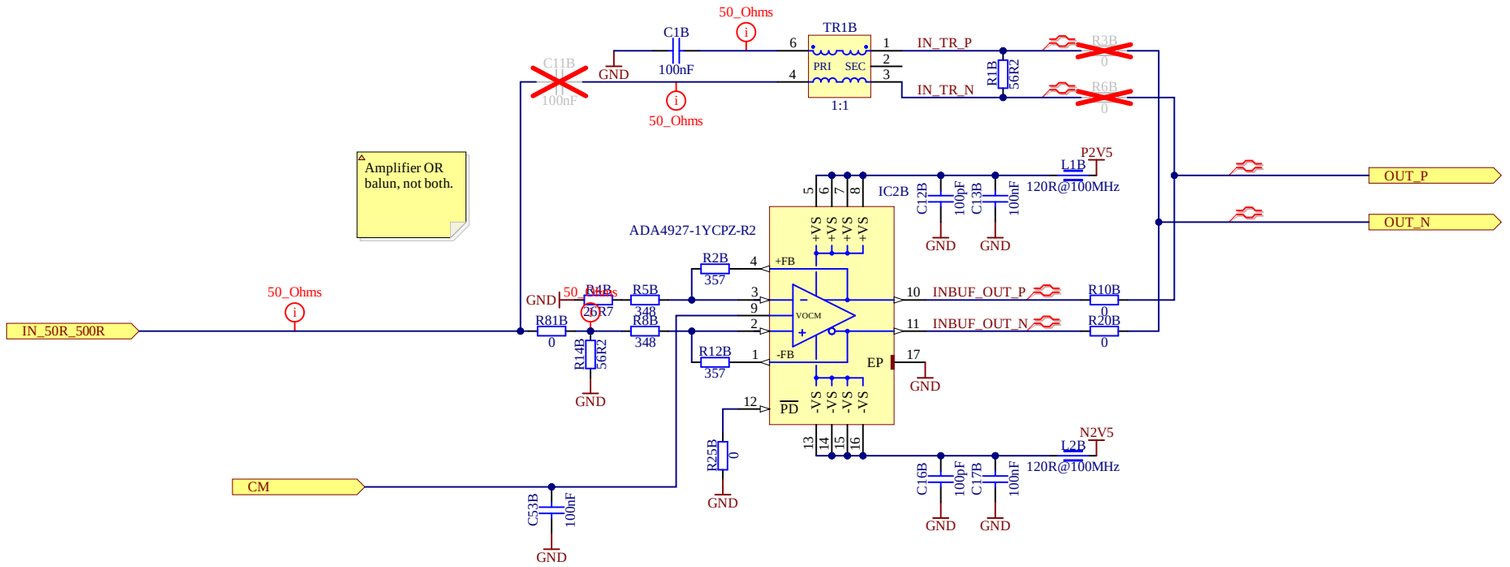
Cannot open file D:\Dropbox\DESIGNS\MTCA_projects\SI		Drawn by shanasz	XX/XX/XXXX
		Check.by	-
		Last Mod. -	08.09.2023
		File IN_conditioning.SchDoc	
		Print Date 08.09.2023 14:44:25	Sheet 5 of 6
Warsaw Univeristy of Technology ***ISE*** *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -



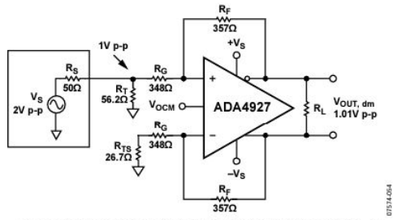


Figure 54. Terminated Single-Ended-to-Differential System with G = 1

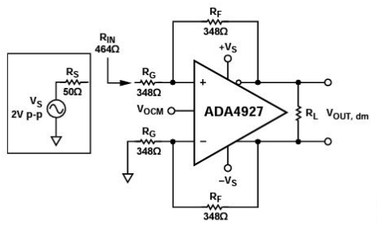


Figure 50. Calculating Single-Ended Input Impedance R_{IN}

Project/Equipment	ARTIQ/SINARA		
Document	***Modulator v1.0*** ***Input signal conditioning***	Designer shanasz	
Cannot open file D:\Dropbox\DESIGNS\MTCA_projects\SI		Drawn by shanasz	XX/XX/XXXX
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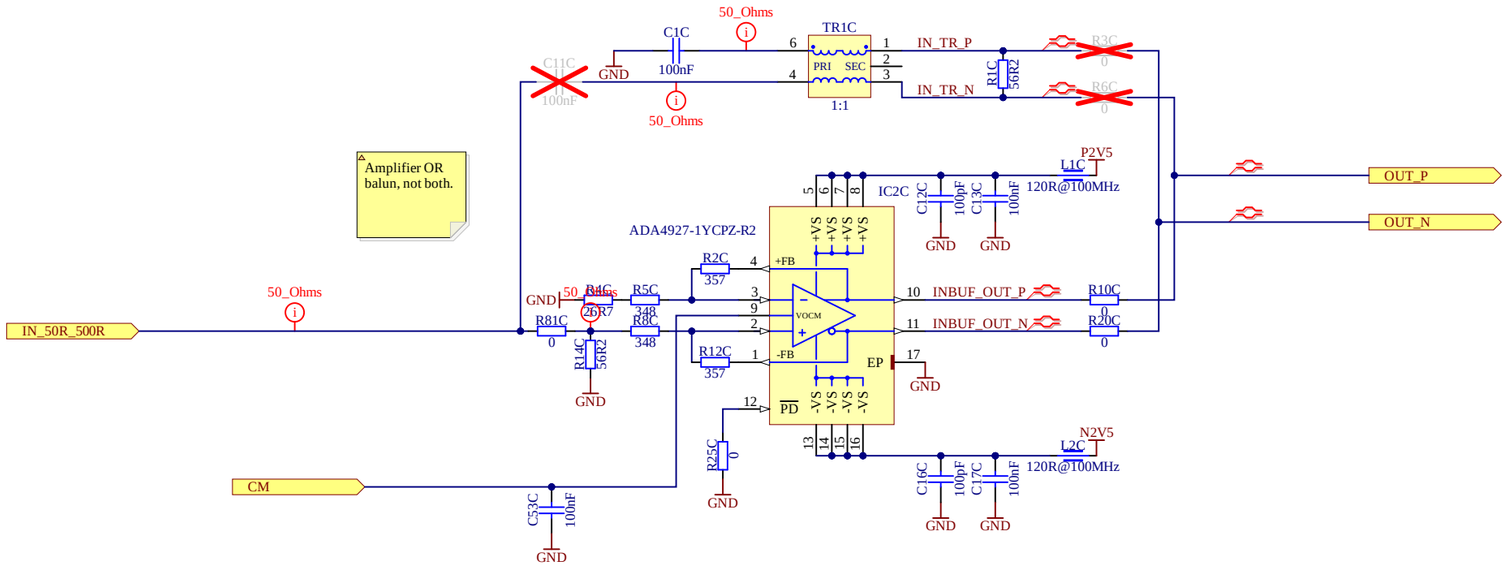
Warsaw Univeristy of Technology ***ISE*** *Nowowiejska 15/19*	ARTIQ	Size A3	Rev -



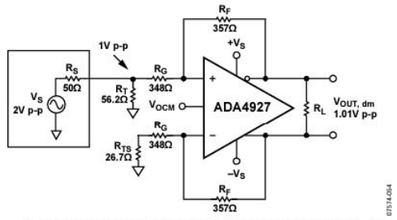


Figure 54. Terminated Single-Ended-to-Differential System with G = 1

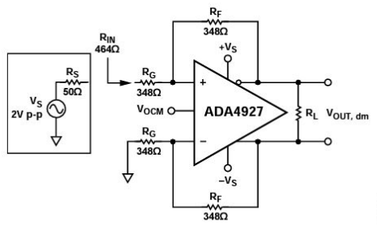


Figure 50. Calculating Single-Ended Input Impedance R_{IN}

Project/Equipment	ARTIQ/SINARA		
Document	***Modulator v1.0*** ***Input signal conditioning***	Designer shanasz	
		Drawn by shanasz	XX/XX/XXXX
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		Last Mod. -	08.09.2023
		File IN_conditioning.SchDoc	
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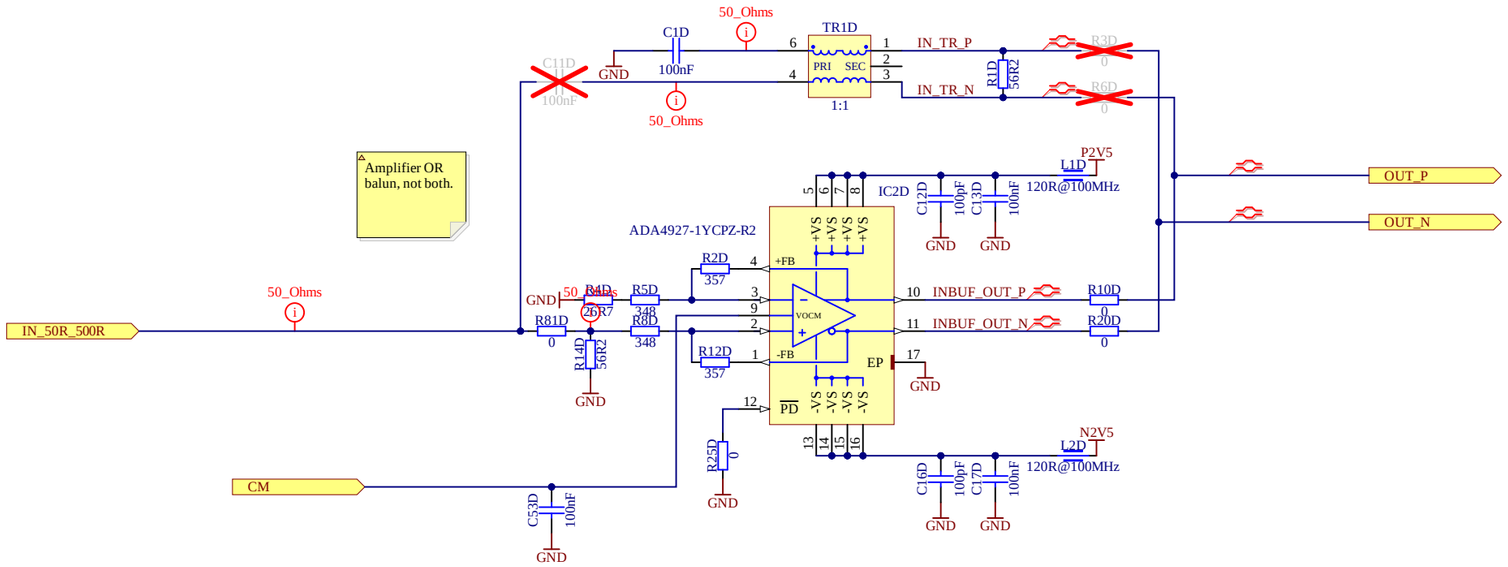

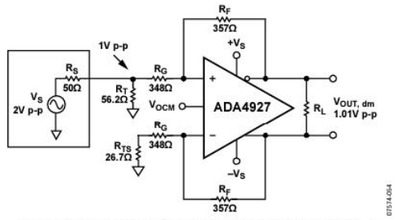

Figure 54. Terminated Single-Ended-to-Differential System with G = 1

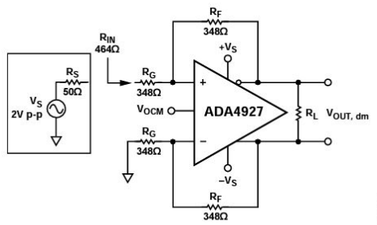

Figure 50. Calculating Single-Ended Input Impedance R_{IN}

Project/Equipment	ARTIQ/SINARA		
Document	**Modulator v1.0** **Input signal conditioning**	Designer shanasz	
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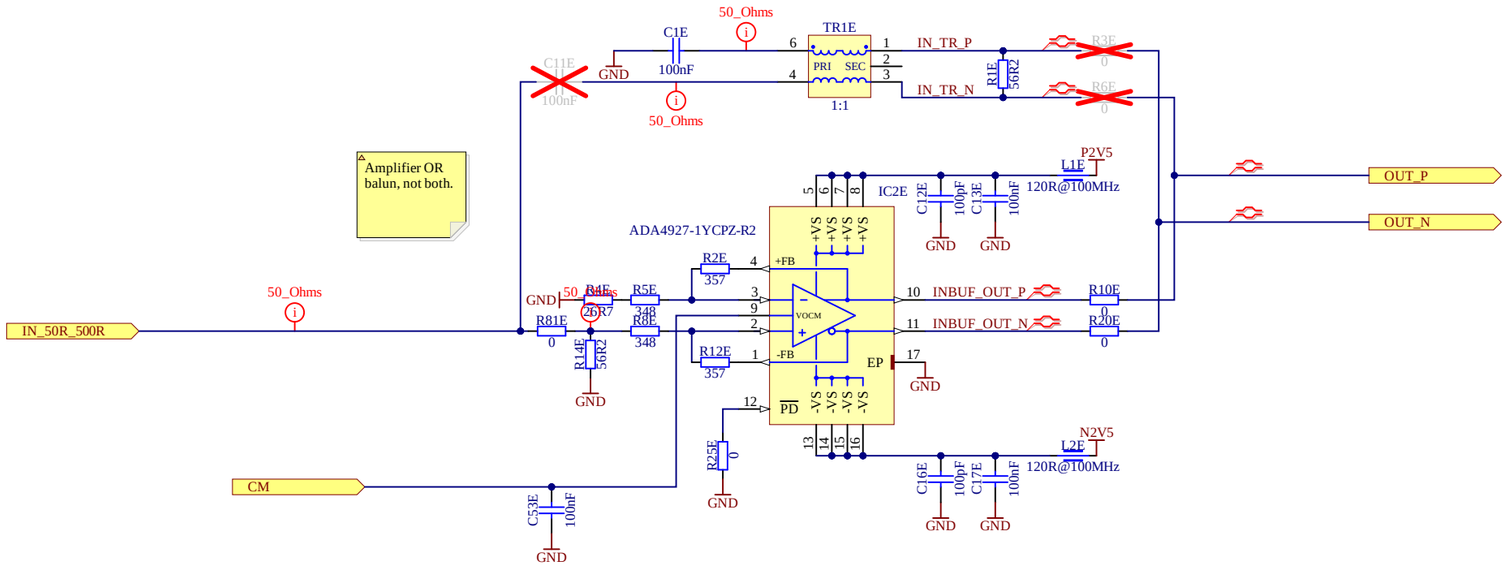

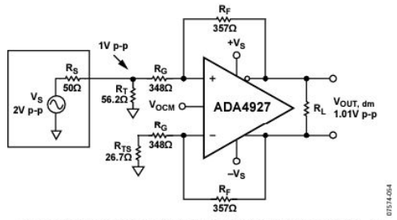

Figure 54. Terminated Single-Ended-to-Differential System with G = 1

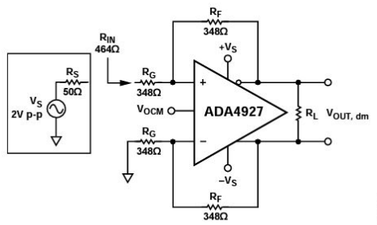

Figure 50. Calculating Single-Ended Input Impedance R_{IN}

Project/Equipment	ARTIQ/SINARA		
Document	**Modulator v1.0** **Input signal conditioning**	Designer shanasz	
		Drawn by shanasz	XX/XX/XXXX
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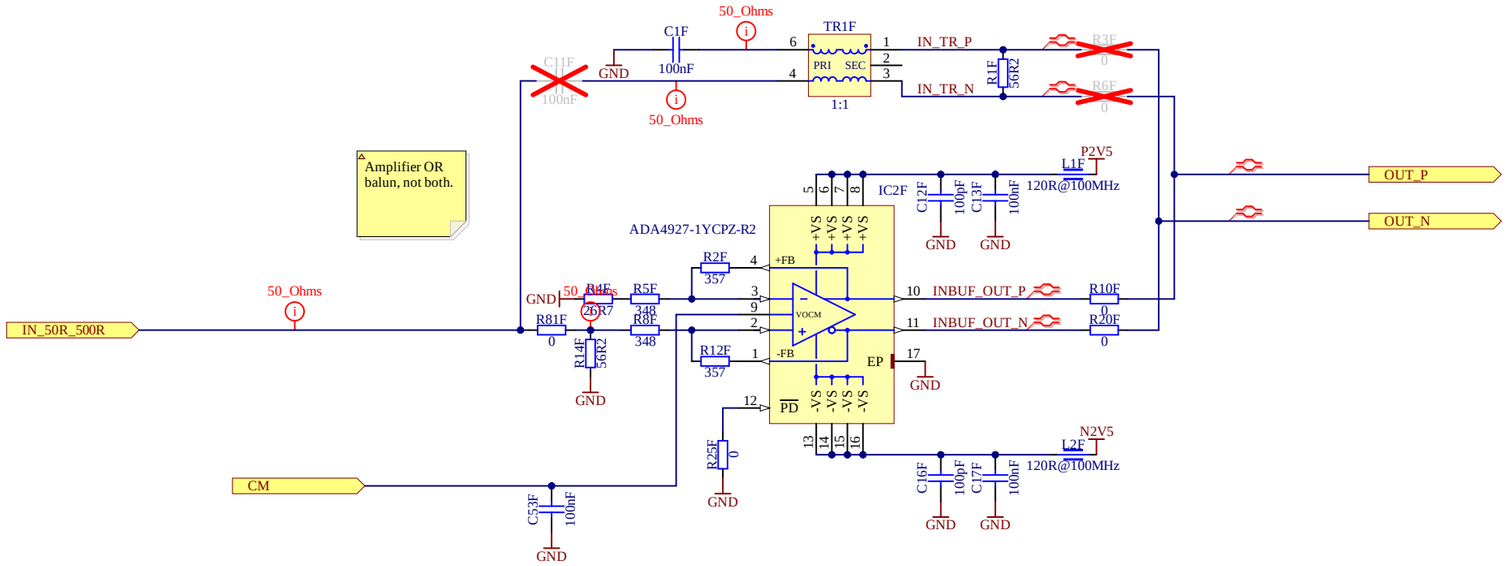
		Print Date 08.09.2023 14:44:25	Sheet 5 of 6
Warsaw Univeristy of Technology *Nowowiejska 15/19*	***ISE***	ARTIQ	Size A3 / Rev -



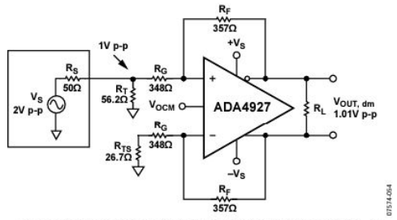


Figure 54. Terminated Single-Ended-to-Differential System with G = 1

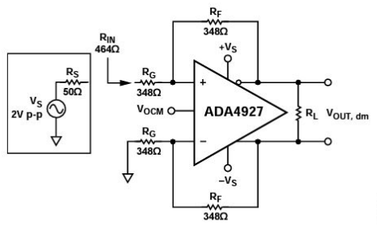


Figure 50. Calculating Single-Ended Input Impedance R_{IN}

Project/Equipment	ARTIQ/SINARA		
Document	**Modulator v1.0** **Input signal conditioning**	Designer shanasz	
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R15 may match the multiplier output, but will cause a gain loss. R34 and R39 may be changed to 24R if better matching is

Balun and THS3217 both connected to ADA4927 output. Amplifiers may be bypassed. One of the amplifiers may be disconnected. On the PCB THS3217 input and balun are placed very close to ADA4927 output, to minimize signal integrity issues.

THS3217IRGV: 10Vpp @ 1MHz ... 100MHz
ADA4927: 1Vpp @ 1MHz ... 2GHz

120R is a diff-amp 100R matching. May be removed if 2xRg input impedance is required.

Due to multiplier output impedance, buffer output voltage will fall form 2Vpp @ DC, via 1.8Vpp @ 200MHz, to 1,2Vpp @ 1-2GHz

G=1 @ DC

VO1: 1,2Vpp
Switch losses = 17%
We need a gain of 9.5 to generate 10Vpp output

For output frequencies < 10MHz solder out the capacitors and directly connect one of the paths. Bottom frequency defined by the coupling caps.

Output amplifier selector, 1 = 10Vpp, 0 = 1Vpp

0 = filter bypass. 1 = filter on.

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	ARTIQ

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