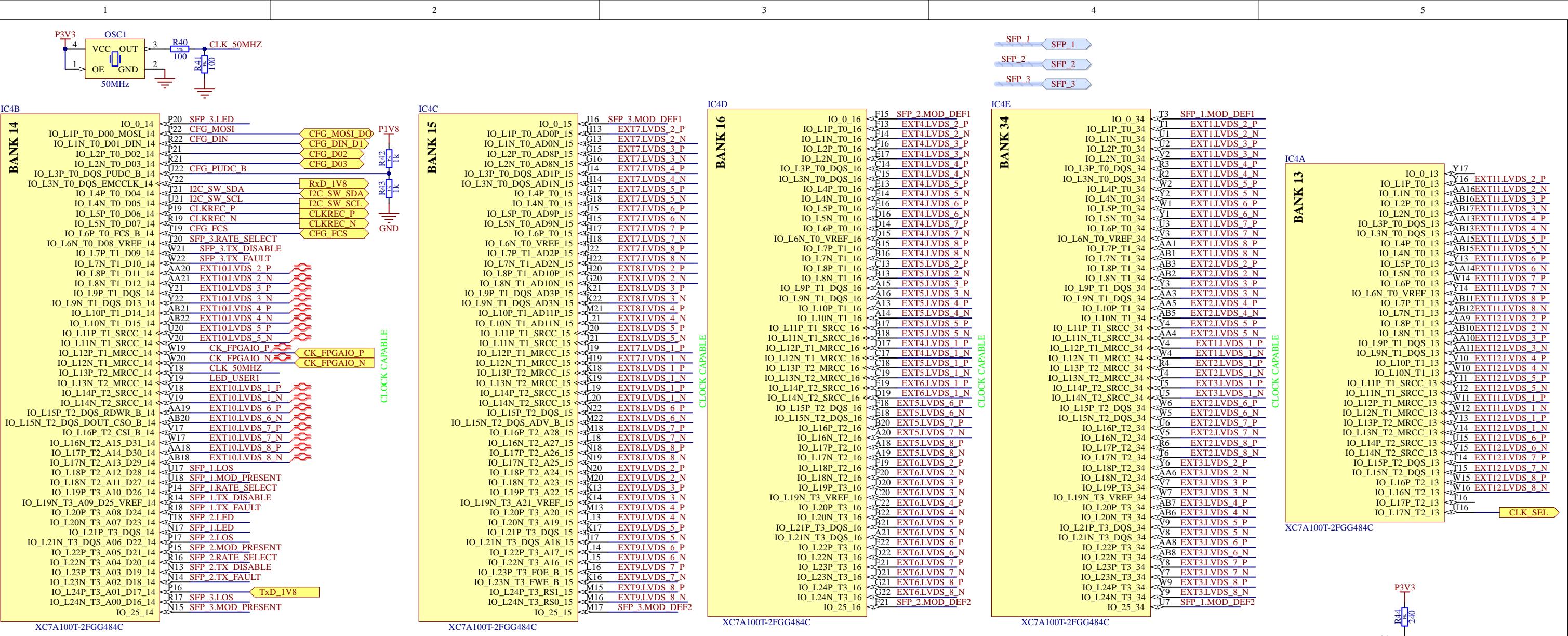
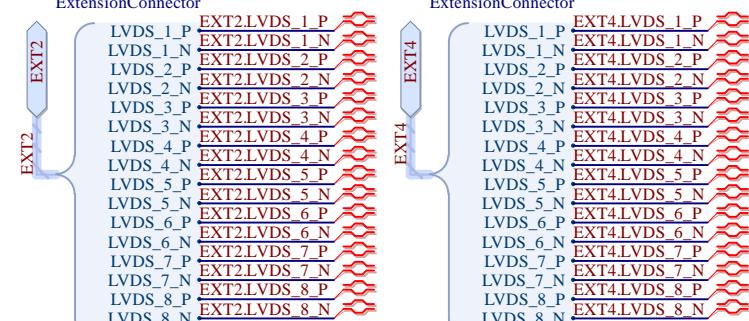
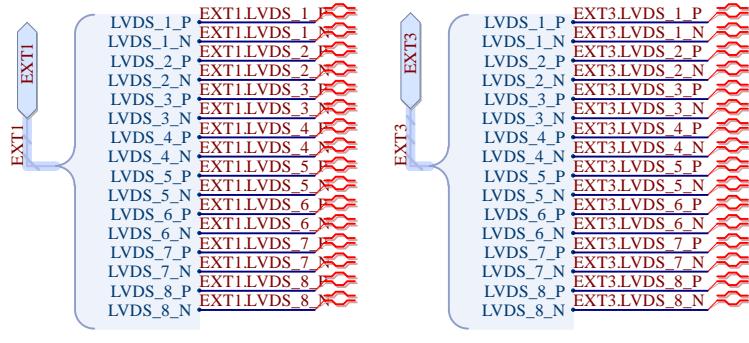


**ADD LEDS  
ADD fiducials**

Project/Equipment		ARTIQ/SINARA	
Document	PCB_3U_Kasli.PrjPCB TOP.SchDoc	Designer G.K. Drawn by G.K. Check by - Last Mod. - File TOP.SchDoc Print Date 11.08.2017 08:44:09	XX/XX/XXXX - 10.08.2017 TOP.SchDoc Sheet 1 of 12 Warsaw University of Technology ISE Nowowiejska 15/19
Cannot open file D:\Dropbox\DESIGN\SMTCA_projects\SI		Size A3 Rev -	



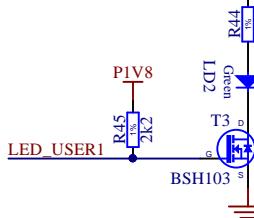
XC7A100T-2FGG484C



XC7A100T-2FGG484C

XC7A100T-2FGG484C

XC7A100T-2FGG484C



Project/Equipment ARTIQ/SINARA

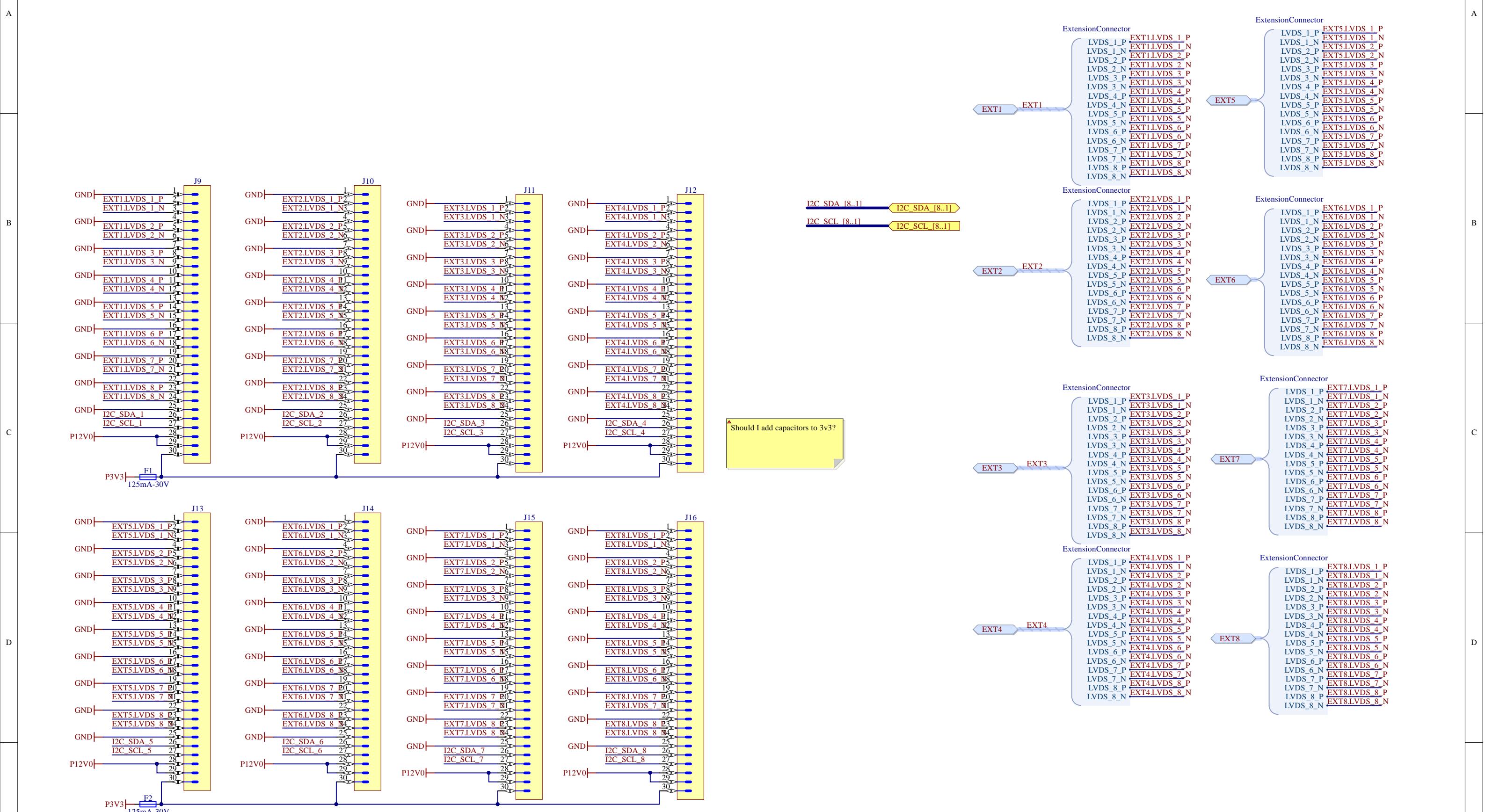
Document

Cannot open file D:\Dropbox\DESIGN\SMTCAs\projects\SI

PCB\_3U\_Kasli.PrjPCB  
FPGA.schdoc

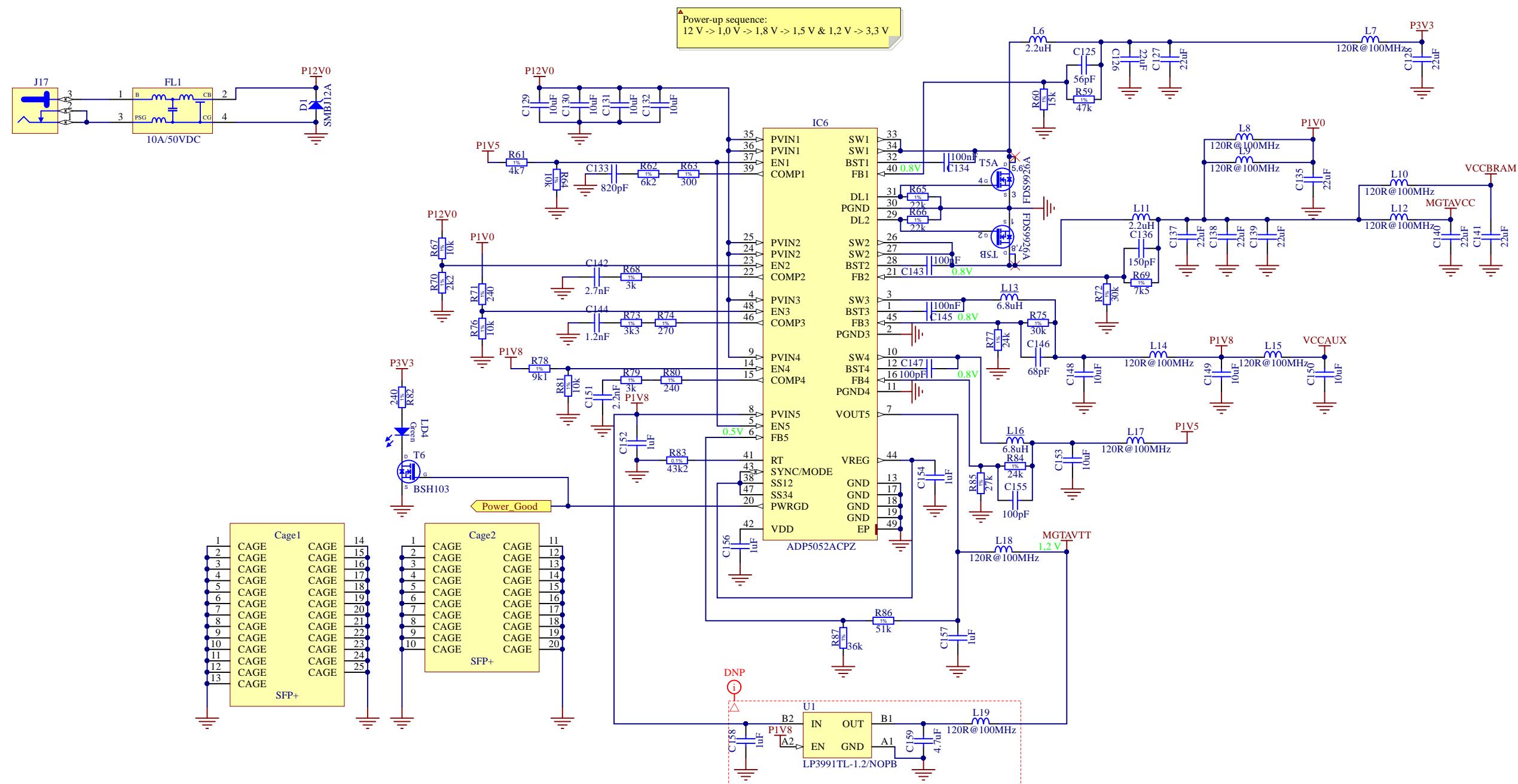
Designer G.K.	Drawn by G.K.	XX/XX/XXXX
Check-by	-	
Last Mod.-	10.08.2017	
File FPGA.schdoc	Print Date 11.08.2017 08:44:10	Sheet 2 of 12
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Document		Designer G.K.	Drawn by G.K.
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Last Mod. -		-	10.08.2017
File IDC_EXT_Connectors.SchDoc	Print Date 11.08.2017 08:44:11	Sheet 3 of 12	
Warsaw University of Technology ISE Nowowiejska 15/19			
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**IDC\_EXT\_Connectors.SchDoc**



Project/Equipment		ARTIQ/SINARA	
Document		Designer G.K.	Drawn by G.K.
Cannot open file D:\Dropbox\DESIGN\SMTCAs\projects\SI		XX/XX/XXXX	-
Last Mod. -		-	10.08.2017
File PowerSupplies.SchDoc			
Print Date 11.08.2017 08:44:11			Sheet 4 of 12
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<b>PCB_3U_Kasli.PrjPCB PowerSupplies.SchDoc</b>		ARTIQ	

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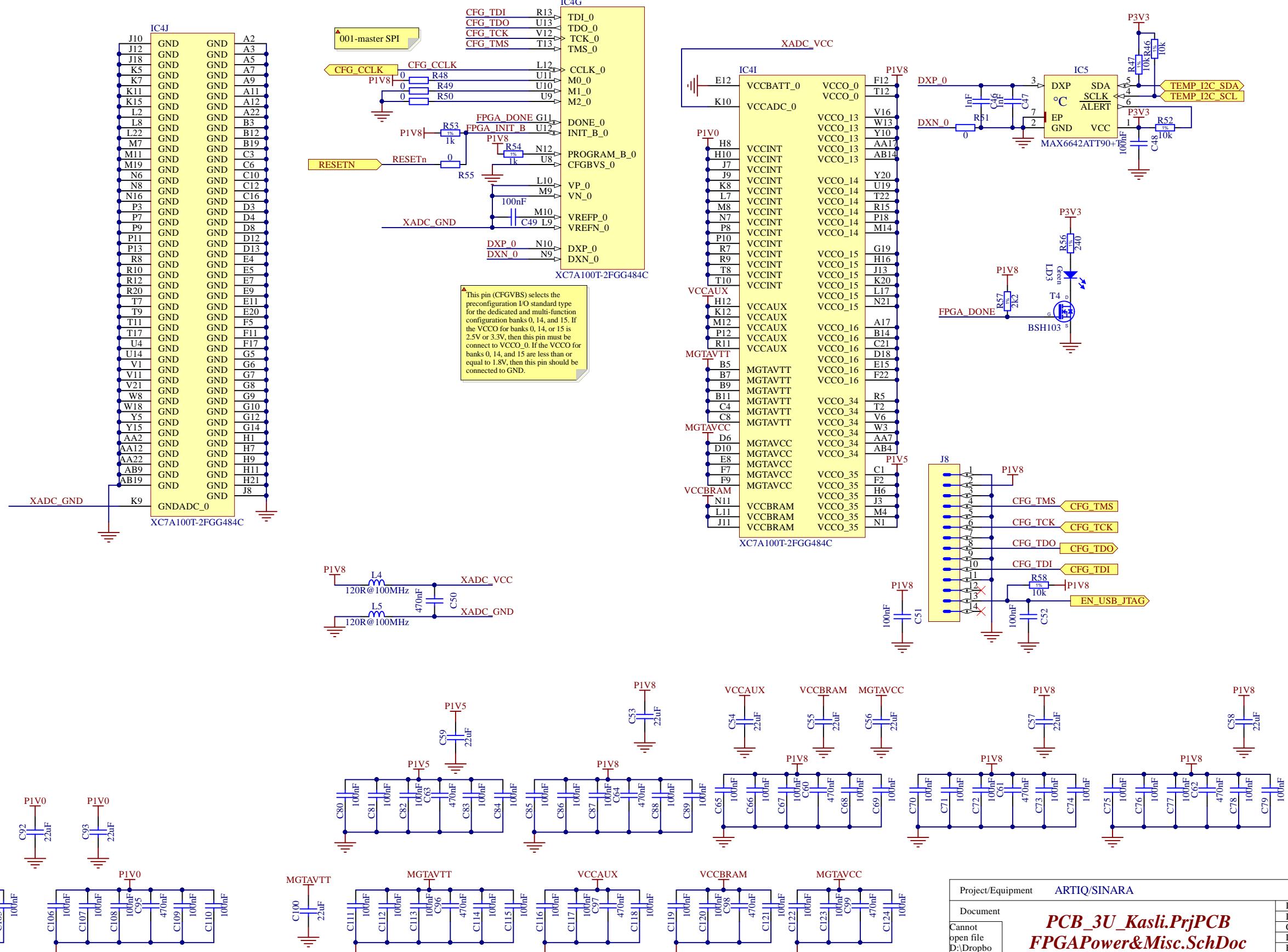
A

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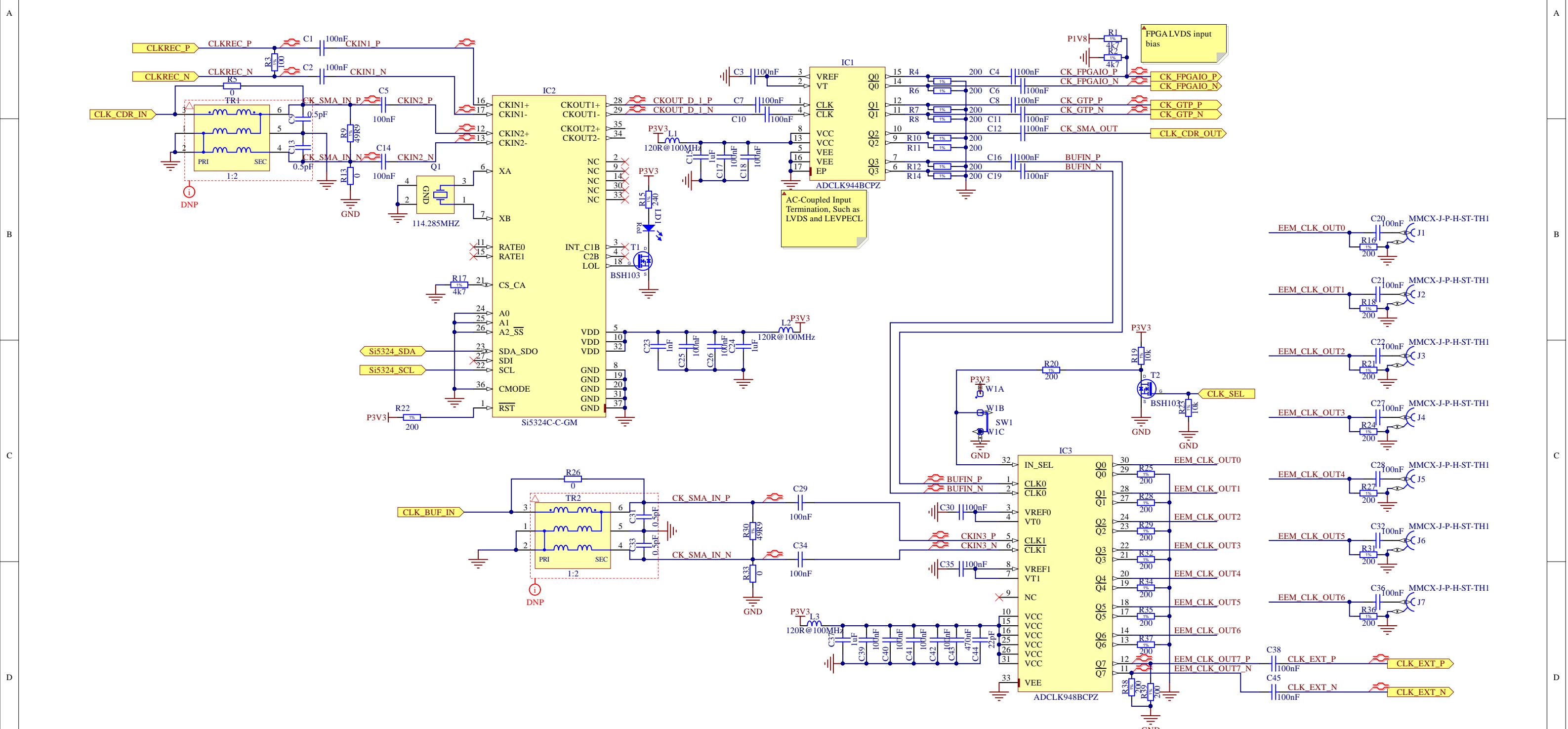
D

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Project/Equipment	ARTIQ/SINARA		
Document	PCB_3U_Kasli.PrjPCB		
Cannot open file D:\Dropbox\DESIGN\SMTCA_projects\SI	FPGAPower&Misc.SchDoc		
Designer G.K.	Drawn by G.K.	Check by	XX/XX/XXXX
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File FPGAPower&Misc.SchDoc	Print Date 11.08.2017 08:44:12	Sheet 5 of 12	Size A3 Rev -
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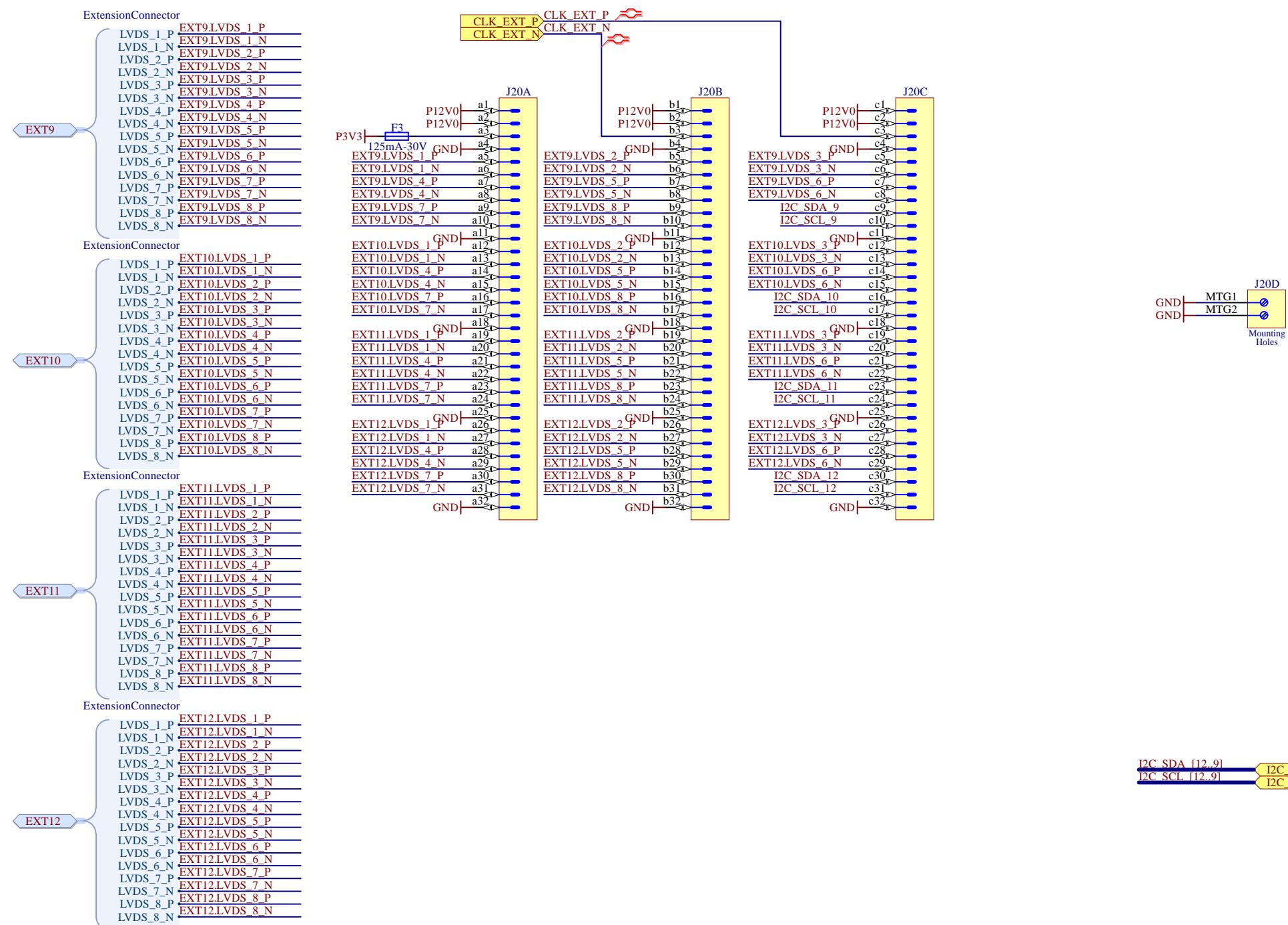
Document

Cannot open file  
D:\Dropbox\DESIGN\SMTCAs\_\projects\SI

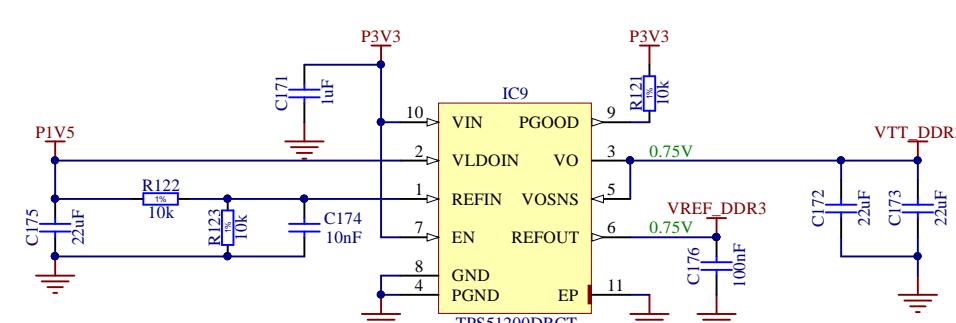
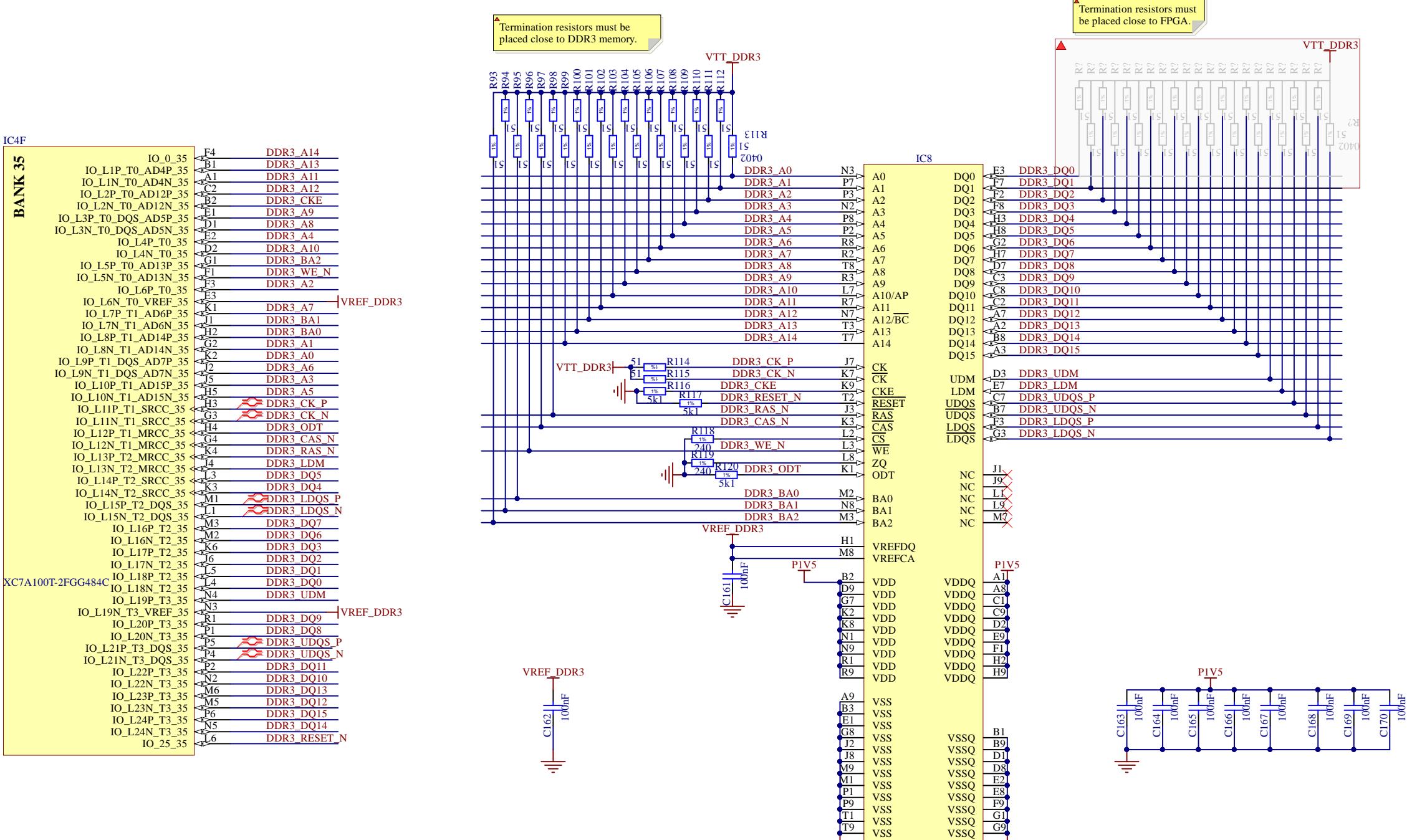
PCB\_3U\_Kasli.PrjPCB  
ClockRecovery.SchDoc

Designer G.K.	Drawn by G.K.	XX/XX/XXXX
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File ClockRecovery.SchDoc	Print Date 11.08.2017 08:44:12	Sheet 6 of 12
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Cannot open file D:\Dropbox\DESIGN\SMTCA_projects\SI	Designer G.K. Drawn by G.K. Check by - Last Mod. - 10.08.2017 File BackplaneConnector.SchDoc Print Date 11.08.2017 08:44:12 Sheet 7 of 12
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Project/Equipment		ARTIQ/SINARA	
Document		Designer G.K.	Drawn by G.K.
Cannot open file D:\Dropbox\DESIGN\SMTCA\_projects\SI		XX/XX/XXXX	
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Last Mod. -		10.08.2017	
File FPGA_SDRAM.SchDoc			
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Sheet 8 of 12			
Warsaw University of Technology ISE Nowowiejska 15/19			
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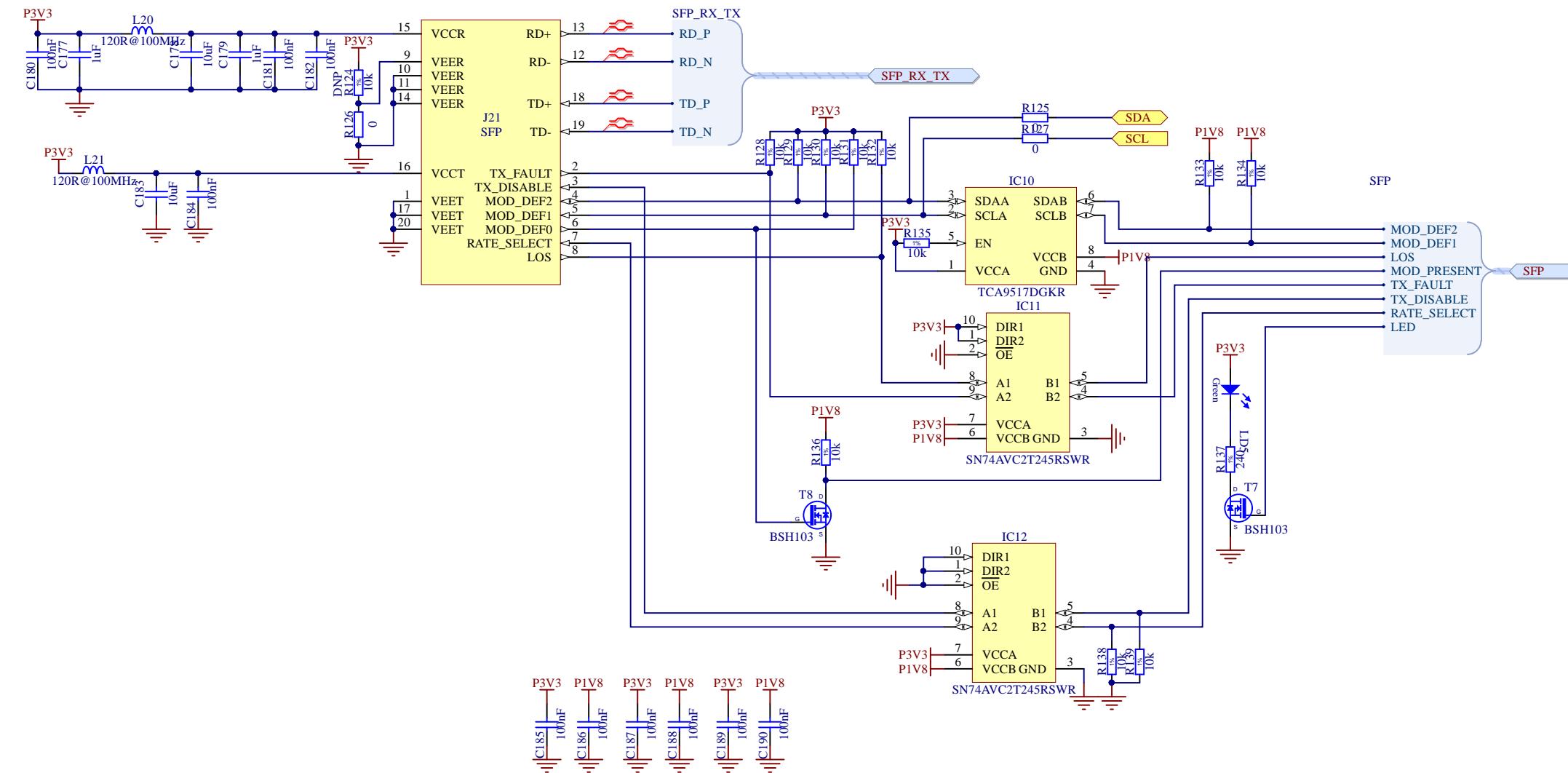
A

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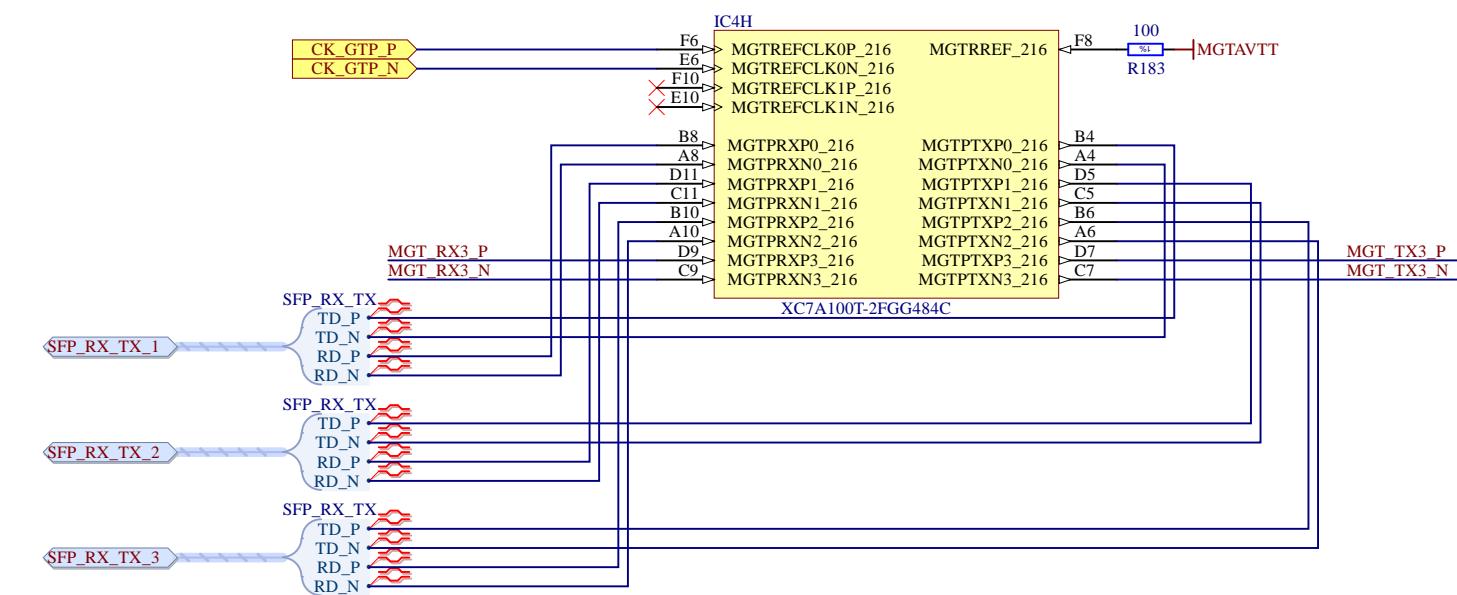
D

E



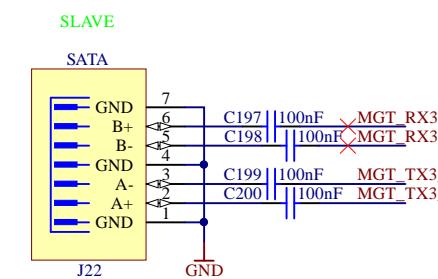
Project/Equipment	ARTIQ/SINARA
Document	PCB_3U_Kasli.PrjPCB
Cannot open file D:\Dropbox\DESIGN\SMTCA_projects\SI	sfp.SchDoc
Last Mod.	11.08.2017
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File sfp.SchDoc	
Print Date 11.08.2017 08:44:13	
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Last Mod. -	11.08.2017
File sfp.SchDoc	
Print Date 11.08.2017 08:44:13	
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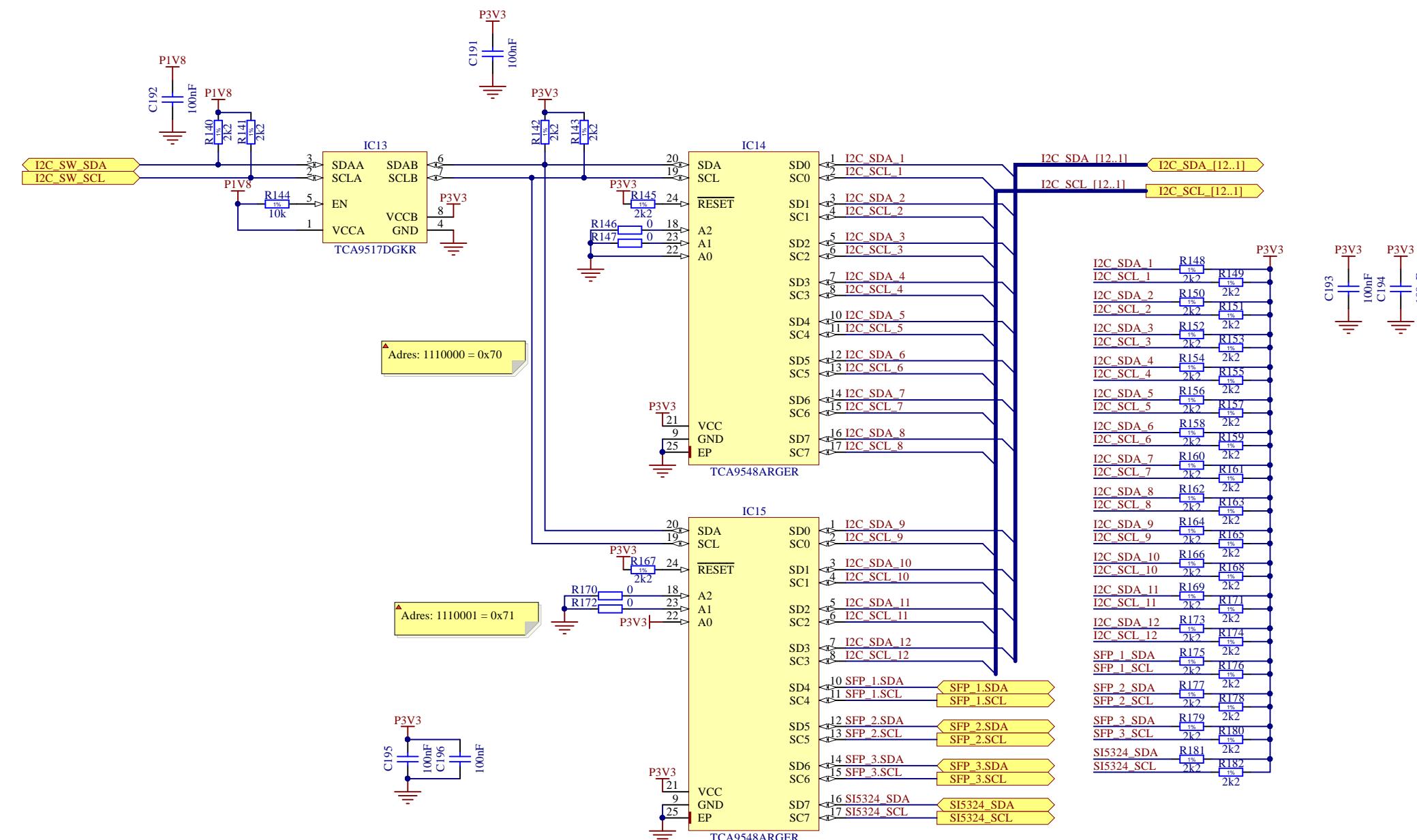
C

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Project/Equipment	ARTIQ/SINARA
Document	PCB_3U_Kasli.PrjPCB FPGAGTP.SchDoc
Cannot open file D:\Dropbox\DESIGN\SMTCA_projects\SI	Designer G.K. Drawn by G.K. Check by - Last Mod. - 10.08.2017 File FPGAGTP.SchDoc Print Date 11.08.2017 08:44:13
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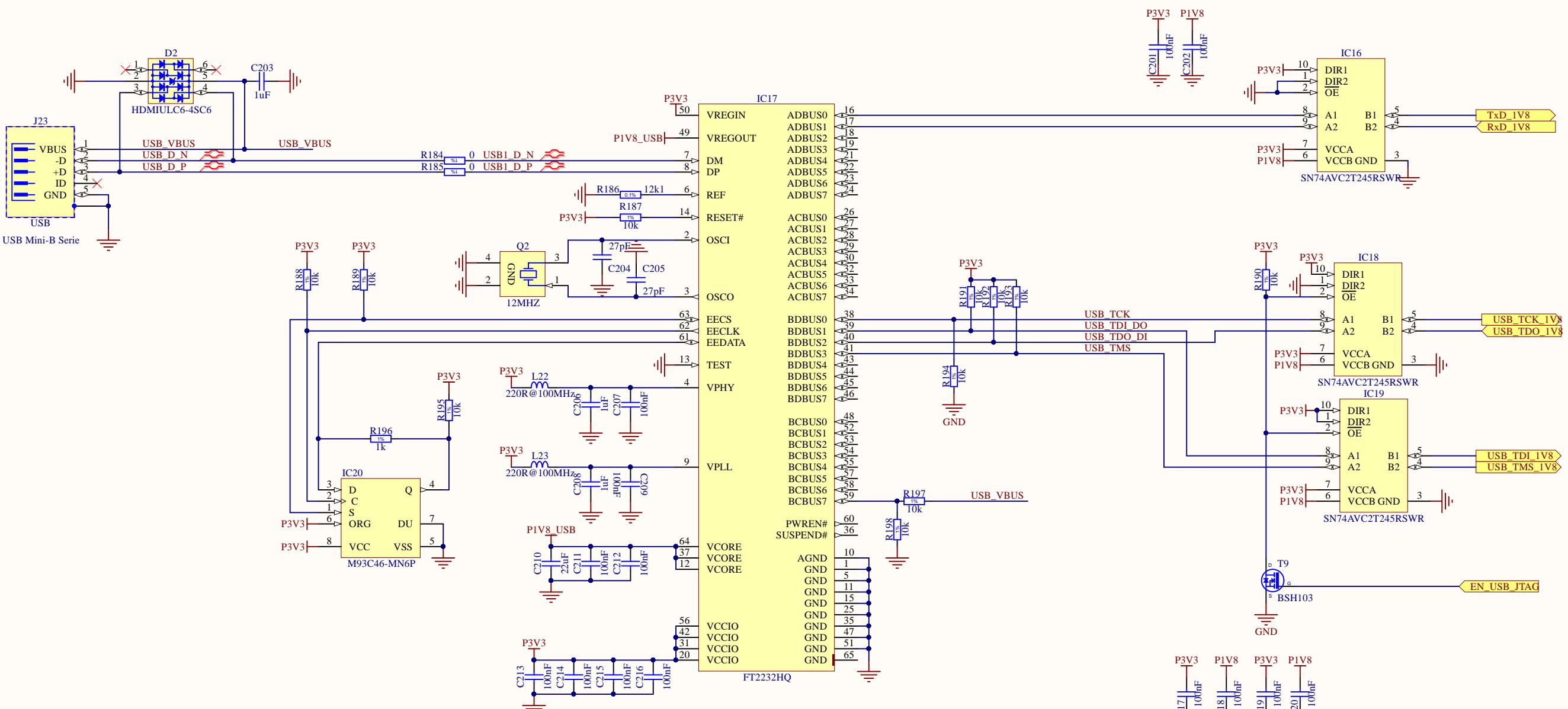
Cannot open file  
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**PCB\_3U\_Kasli.PrjPCB**  
**FPGA\_I2C.SchDoc**

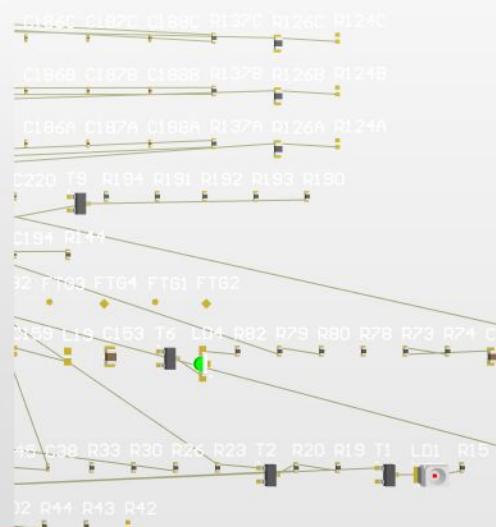
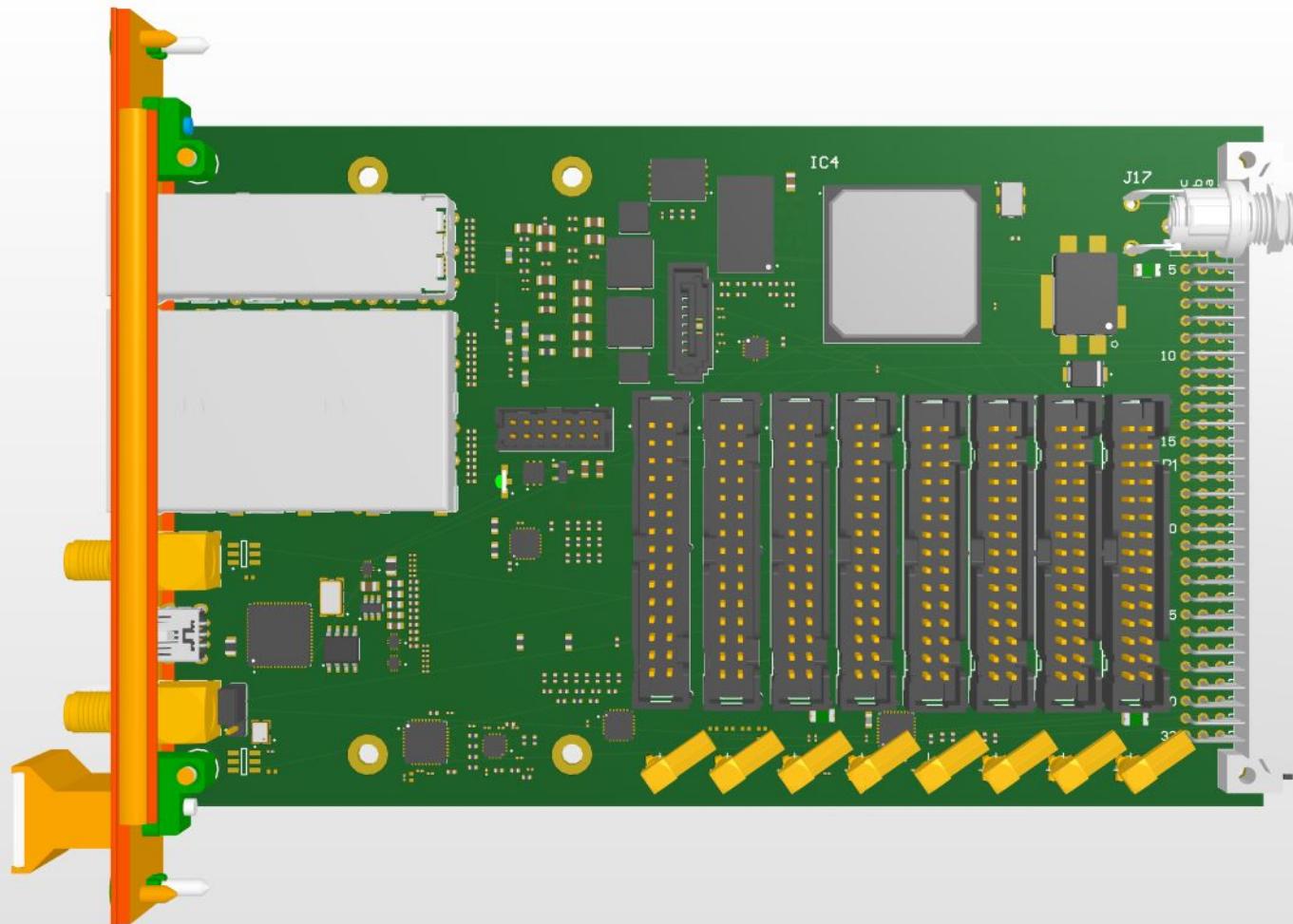
Designer G.K.	Drawn by G.K.	XX/XX/XXXX
Check by	-	
Last Mod.	-	10.08.2017
File	FPGA_I2C.SchDoc	
Print Date	11.08.2017 08:44:13	Sheet 11 of 12
		Size A3 Rev -

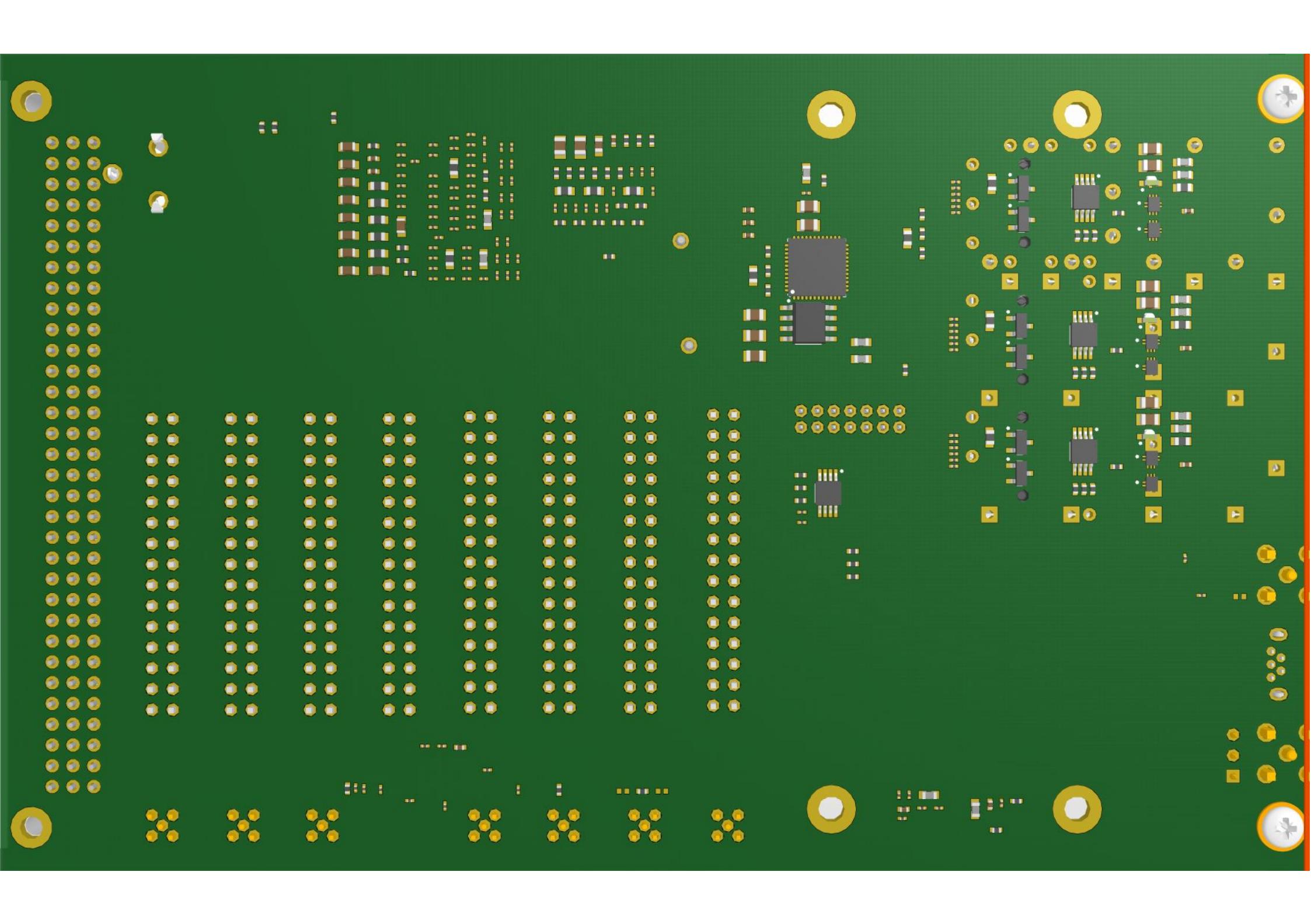
Warsaw University of Technology ISE  
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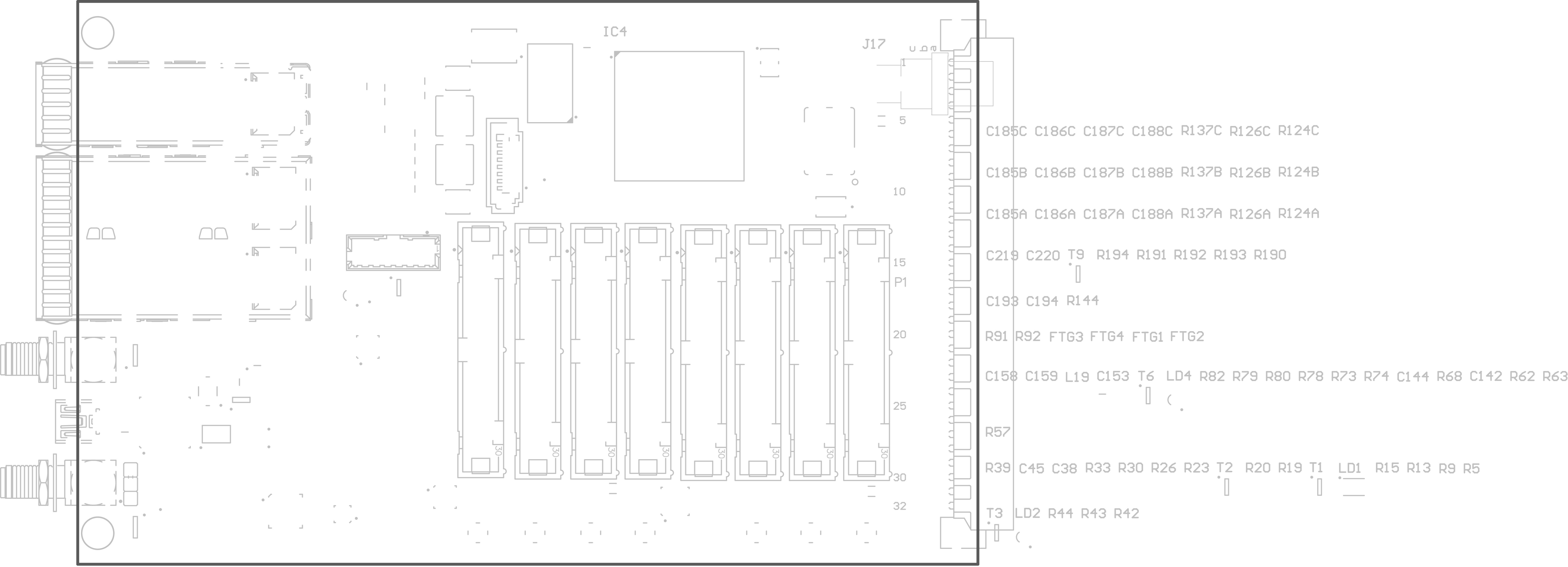
ARTIQ

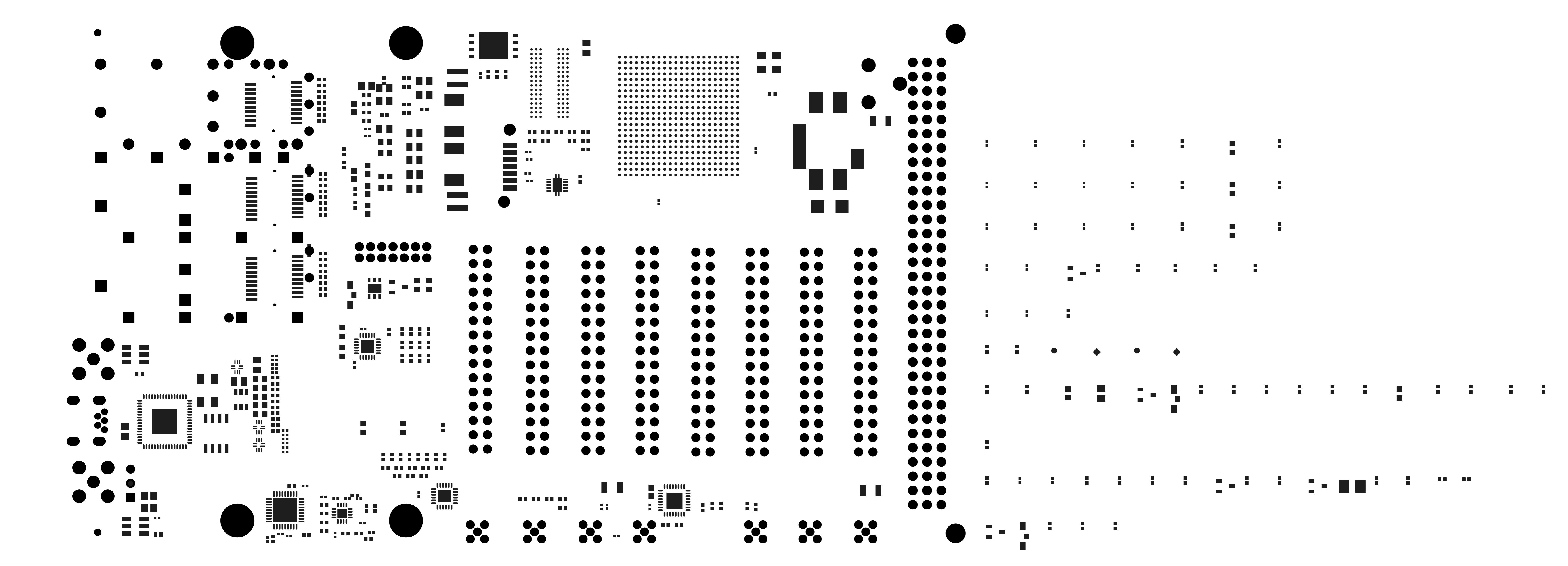


Title		
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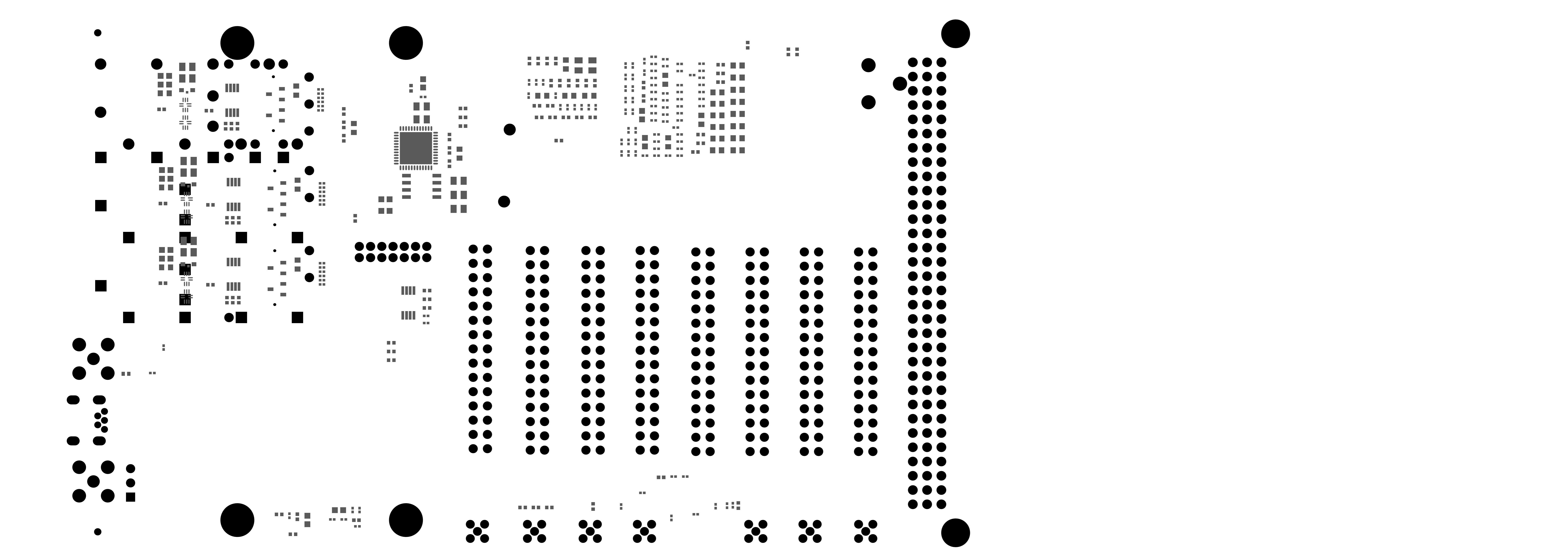


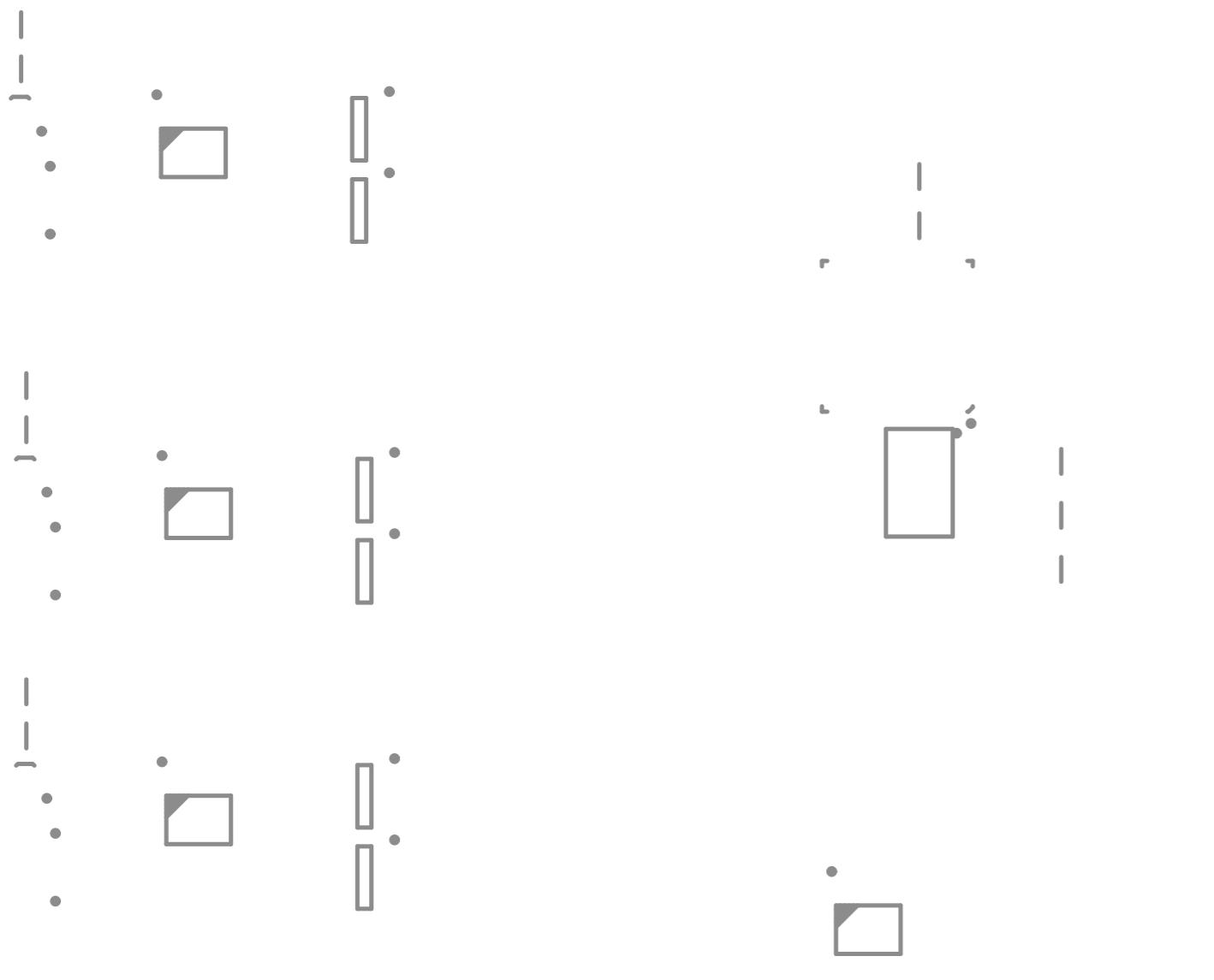












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