

A

A

B

B

C

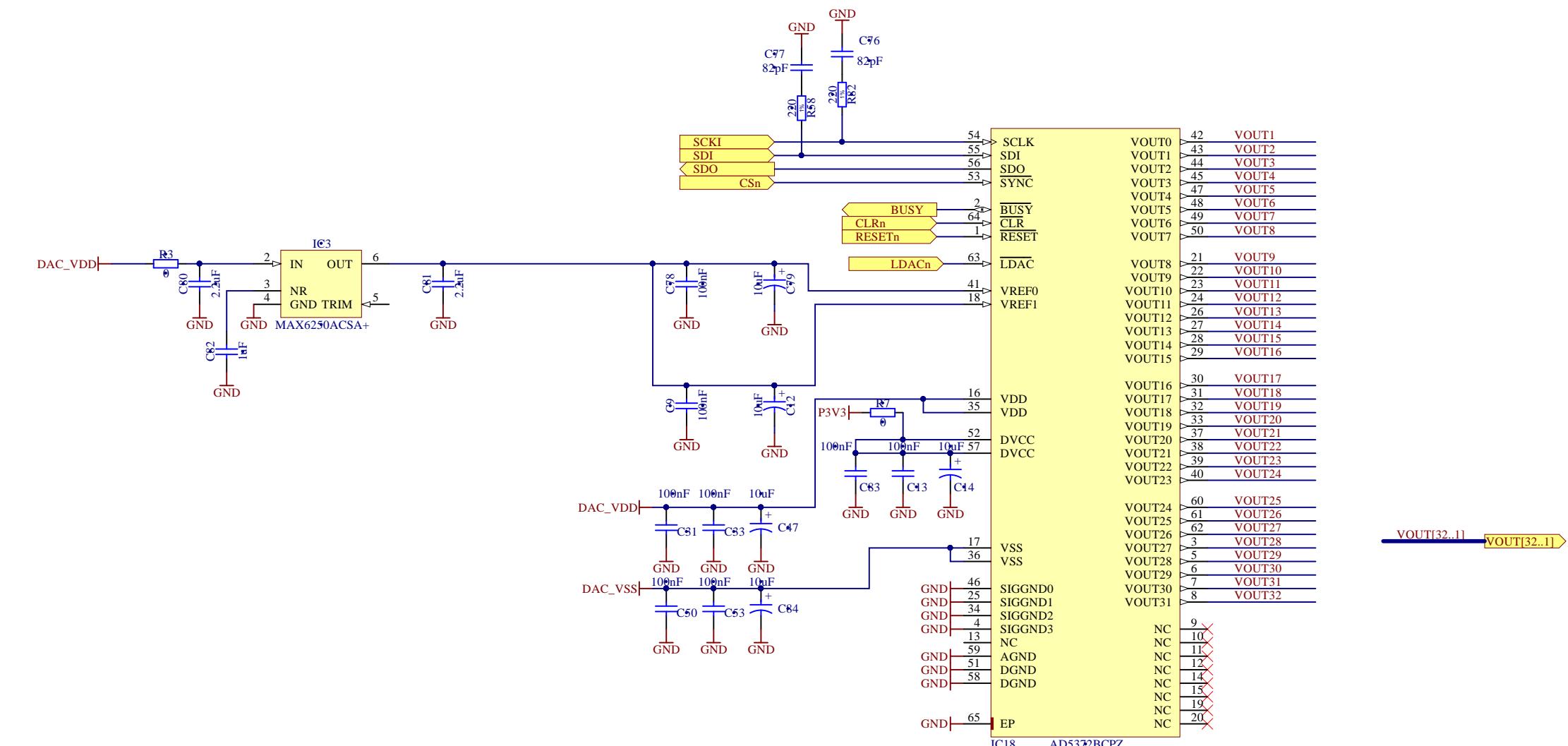
C

D

D

E

E



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Project/Equipment ARTIQ/SINARA

Document



DAC & reference

Designer G.K.	Drawn by G.K.	XX/XX/XXXX
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Last Mod.	14.05.2017	
File DAC_32CH.SchDoc	Print Date 14.05.2017 12:35:25	Sheet 2 of 7

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Nowowiejska 15/19

ARTIQ

Size A3 Rev -

A

B

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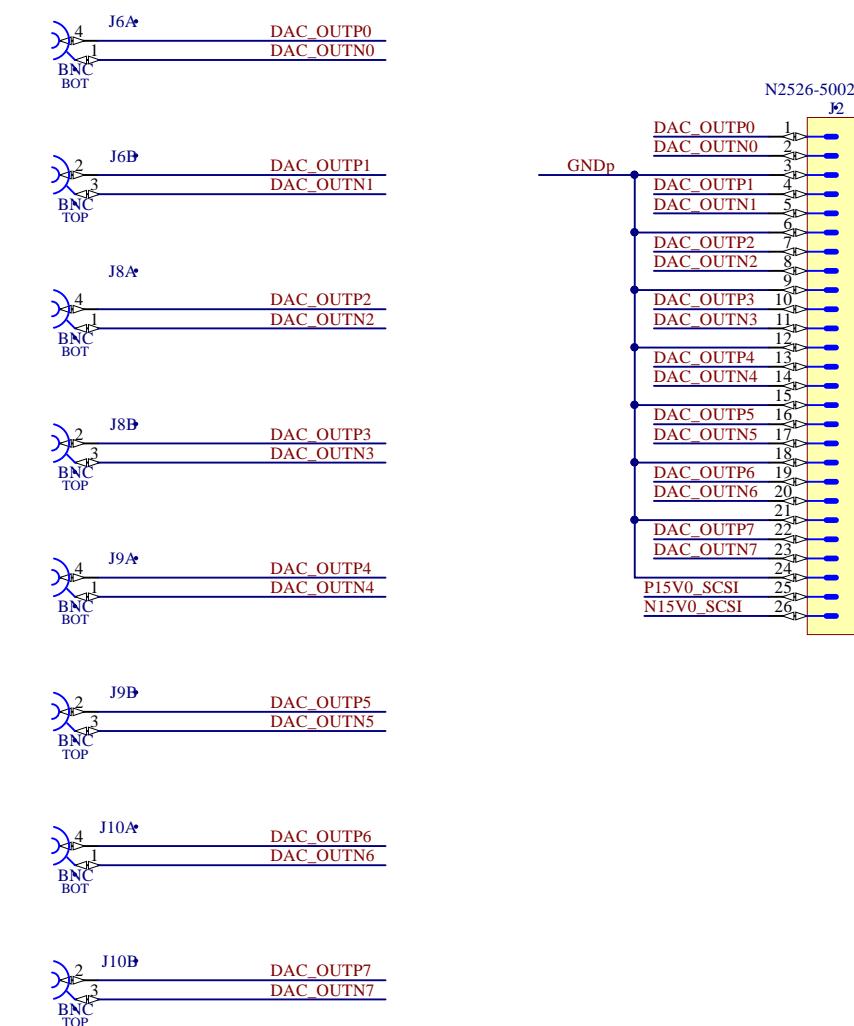
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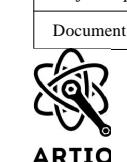
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E



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IDC to BNC adapter

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	Check by -
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ARTIQ

Size A3 Rev -

A

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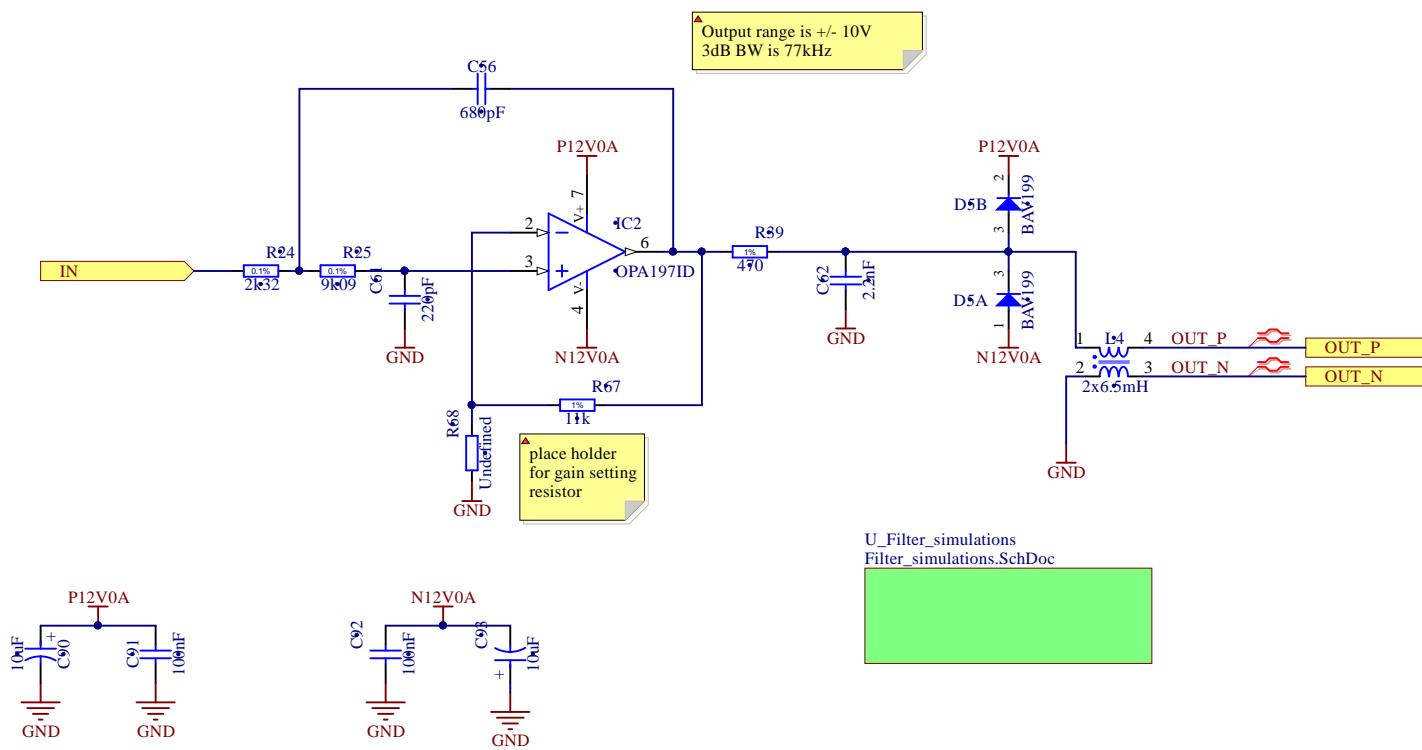
A

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Project/Equipment ARTIQ/SINARA

Document



Output filter

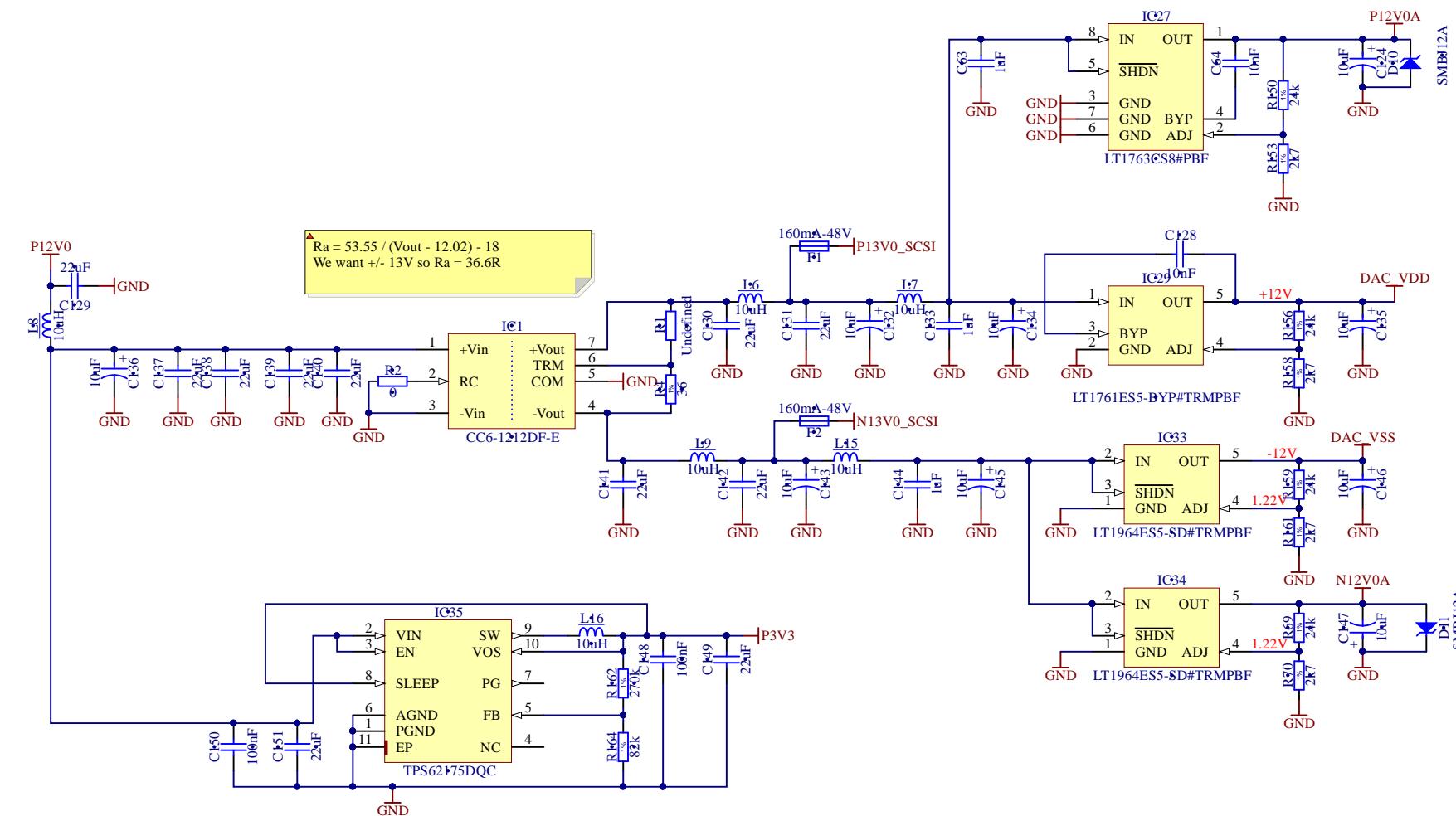
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ARTIQ

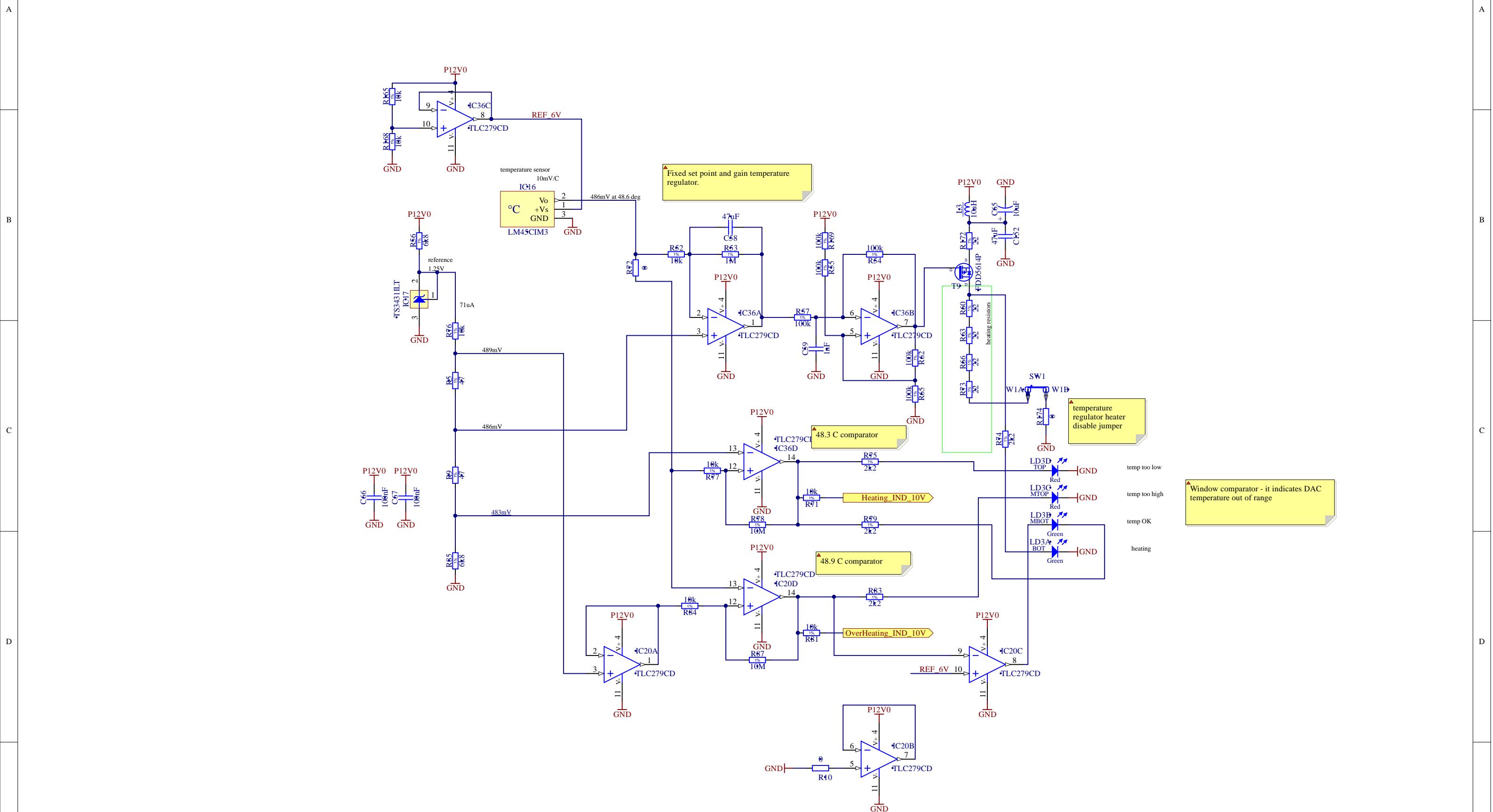
Size A3 Rev -

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A

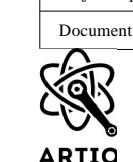


	+13V rail	-13V rail	3.3V	12V
48mA	48mA	48mA		
16mA	16mA	16mA		
			2mA	
			18mA	
			16mA	
3mA				
100mA	100mA	330mA	96mA	
20mA				
136mA				



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Project/Equipment ARTIQ/SINARA

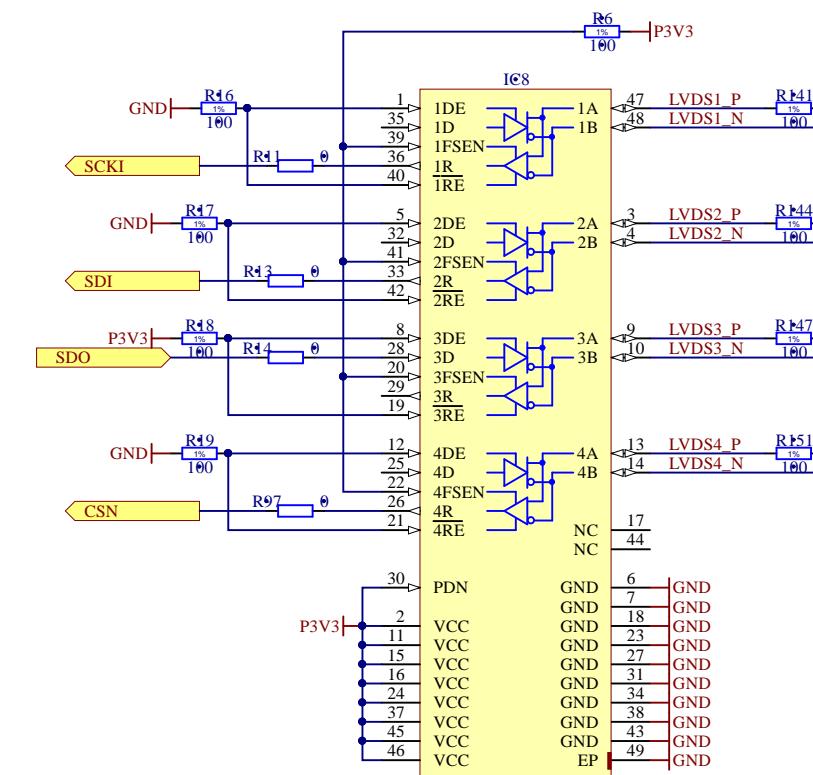


Thermal management

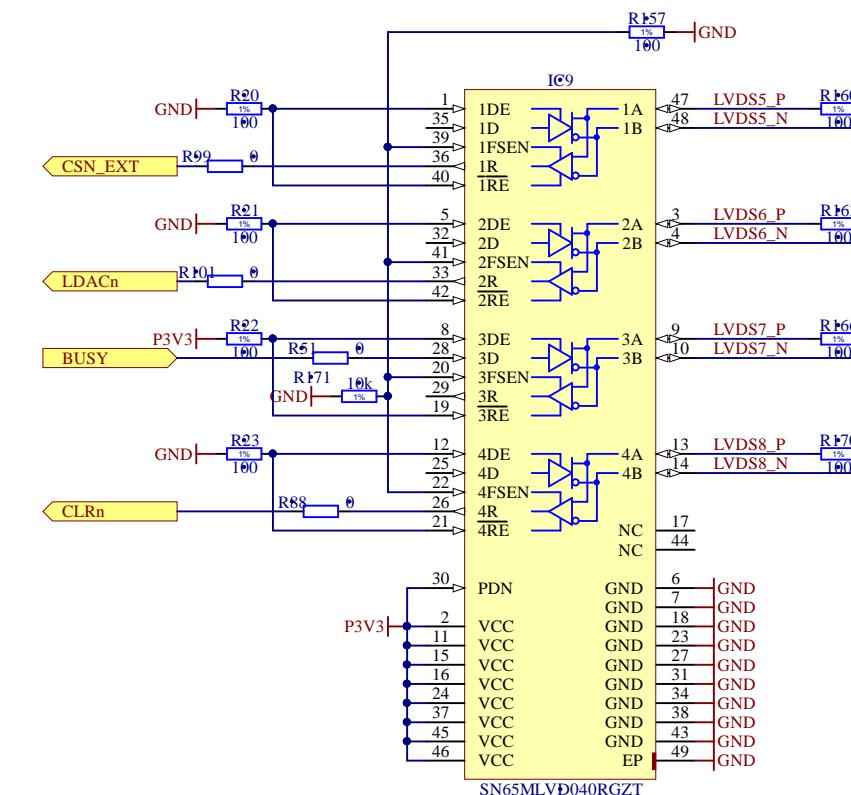
Warsaw University of Technology ISE Nowowiejska 15/19

ARTIQ

A

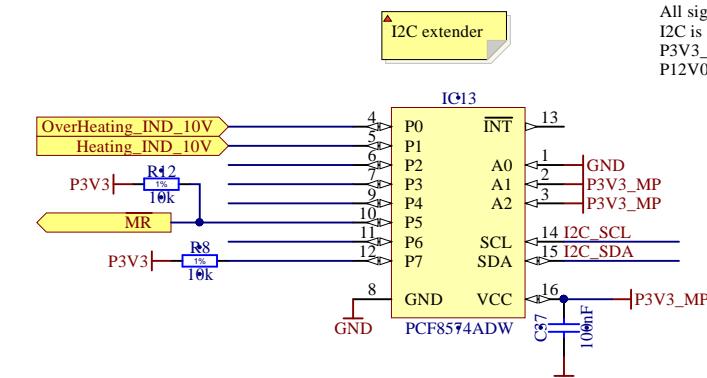


▲ LVDS<> LVCMS
translators

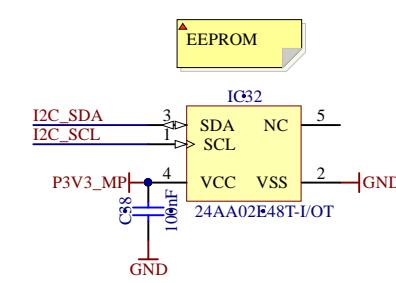
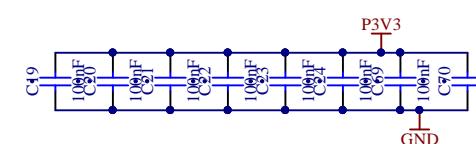
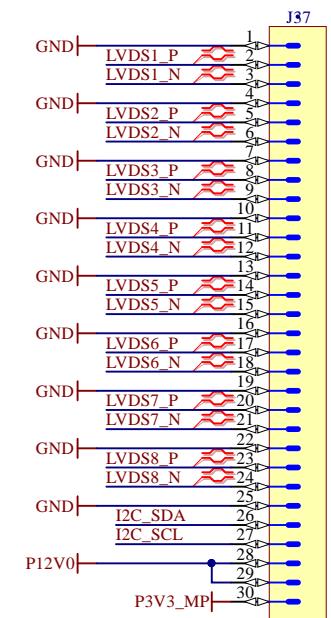


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This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMS
P3V3_MP can handle up to 20mA
P12V0 current is up to 500mA



Project/Equipment ARTIQ/SINARA

Document



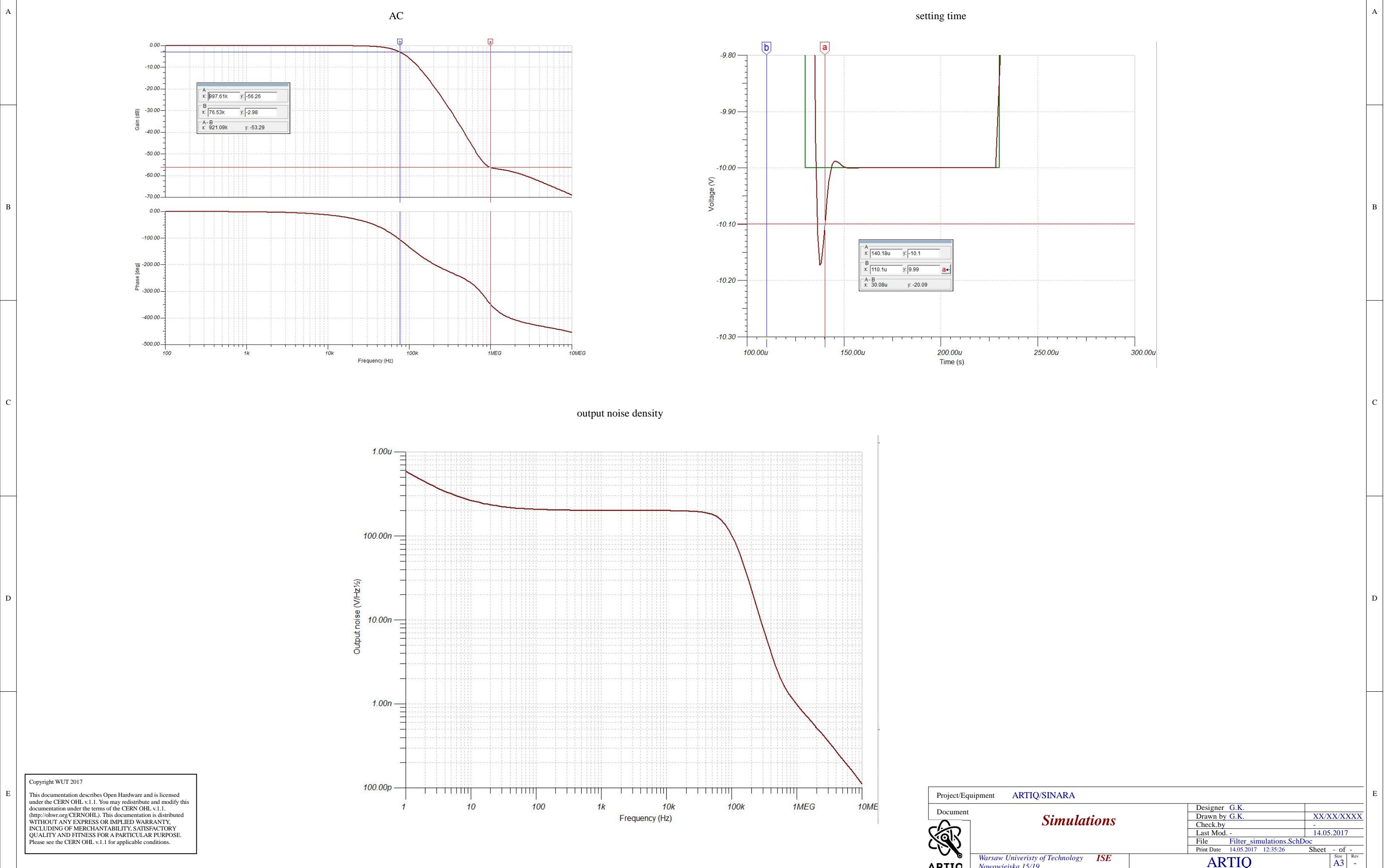
LVDS & I2C interfaces

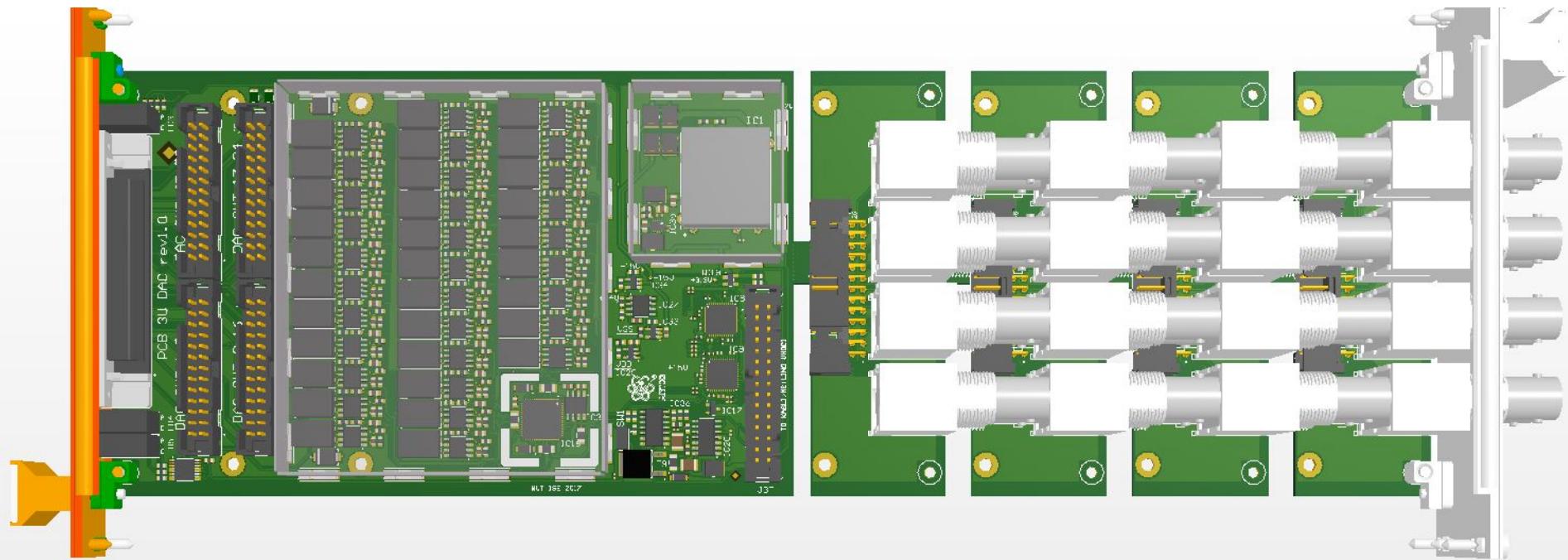
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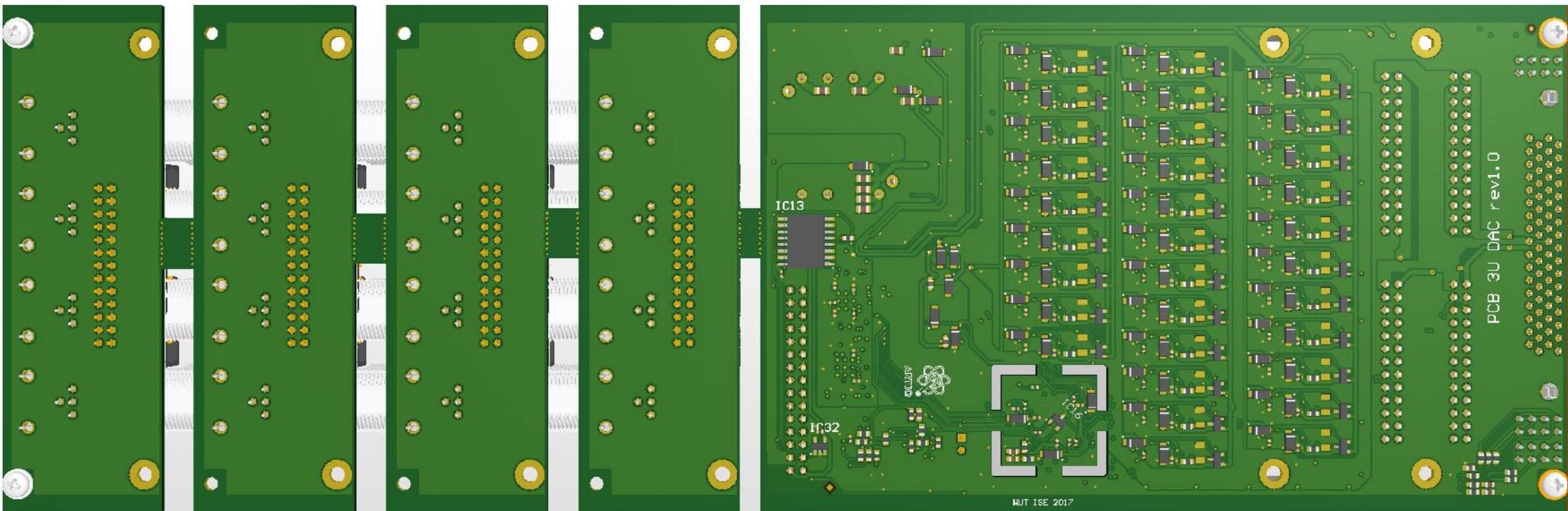
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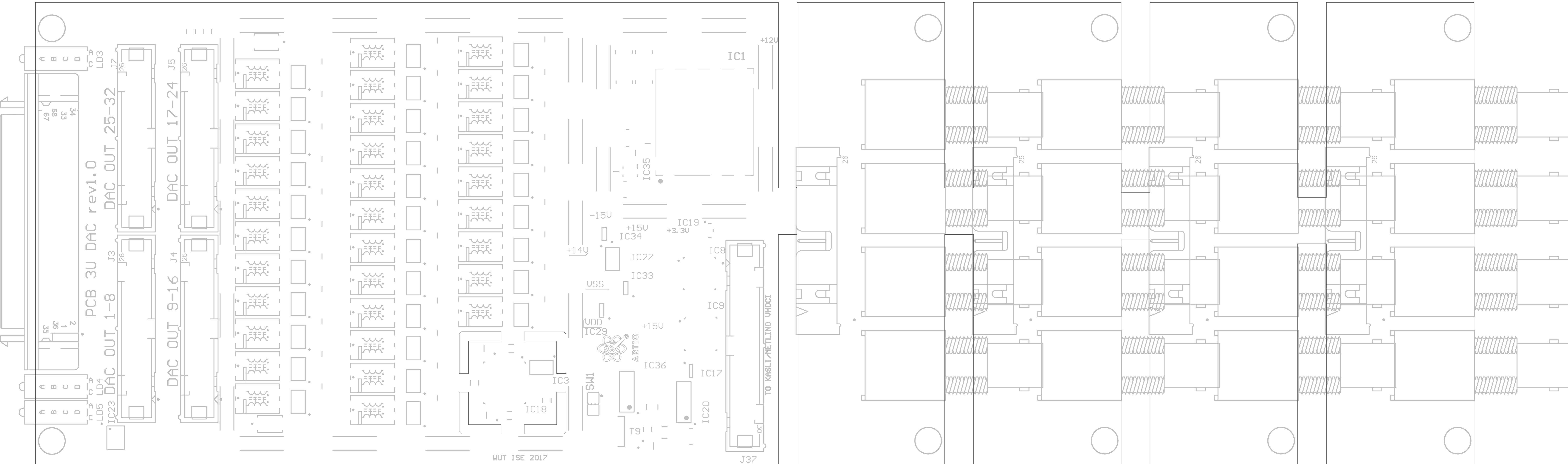
ARTIQ

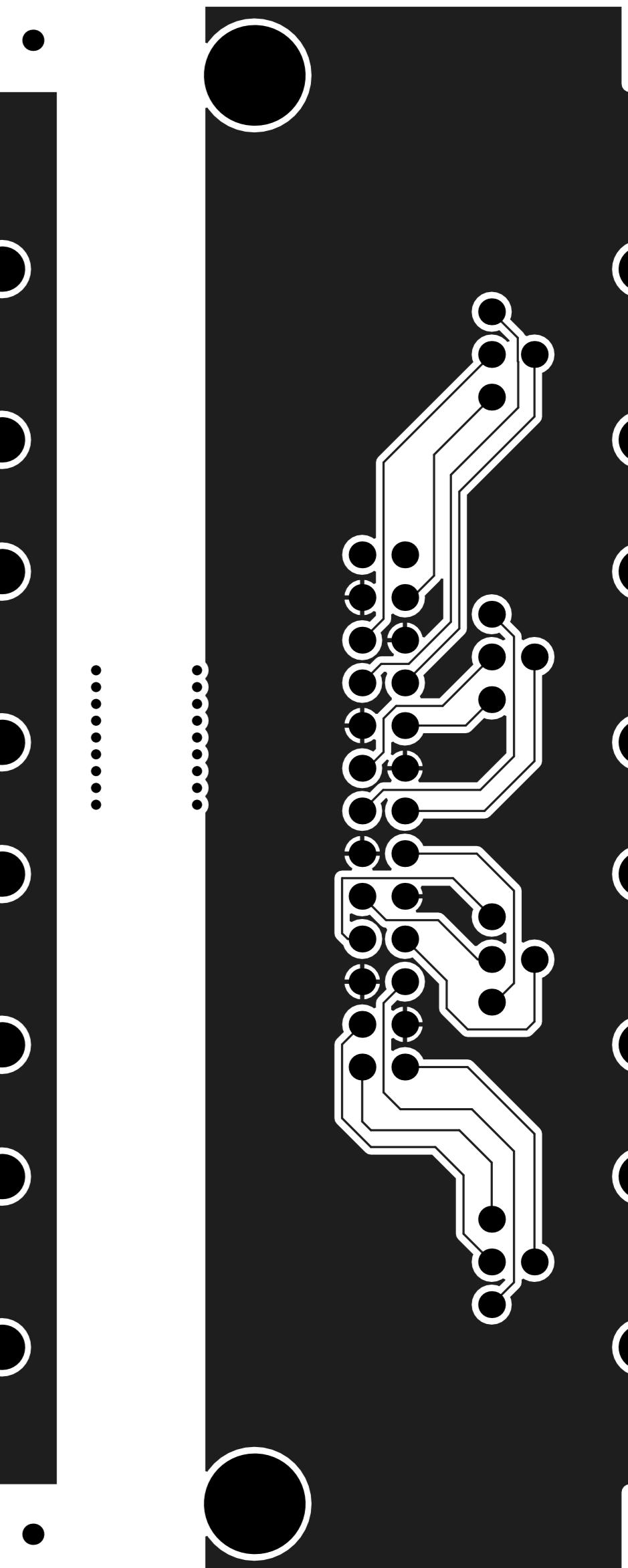
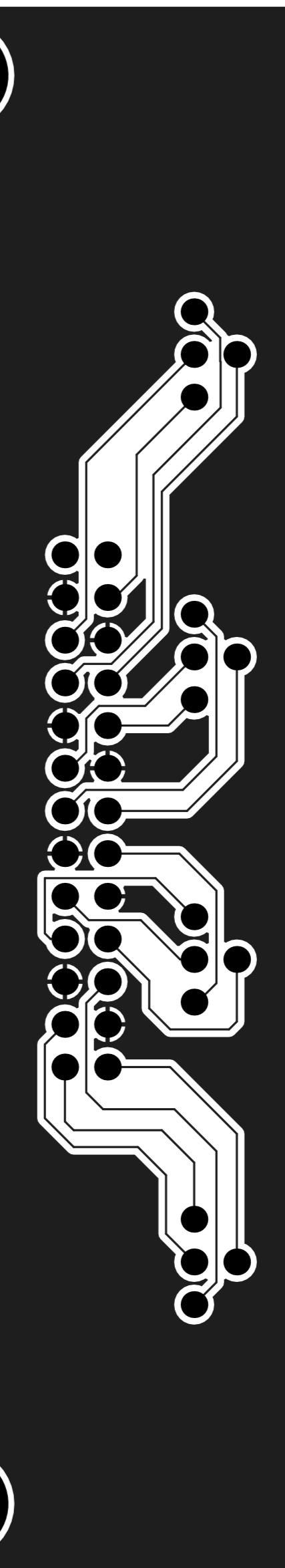
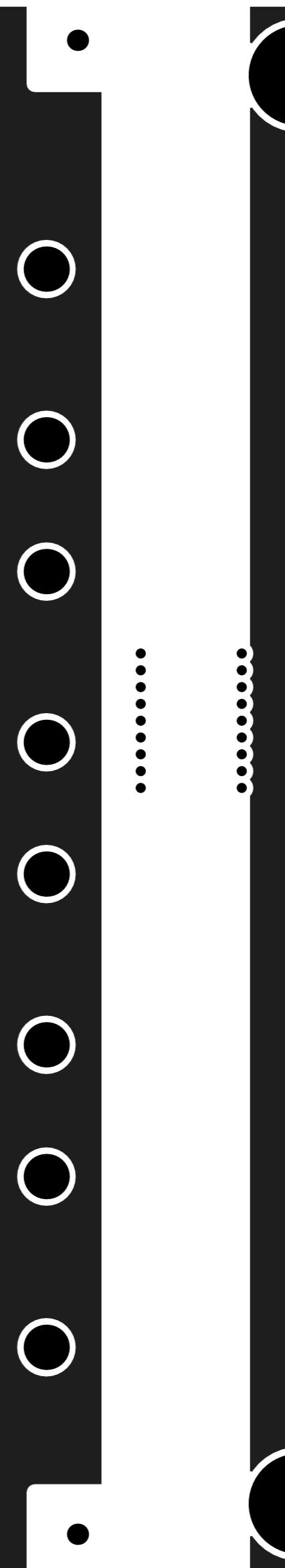
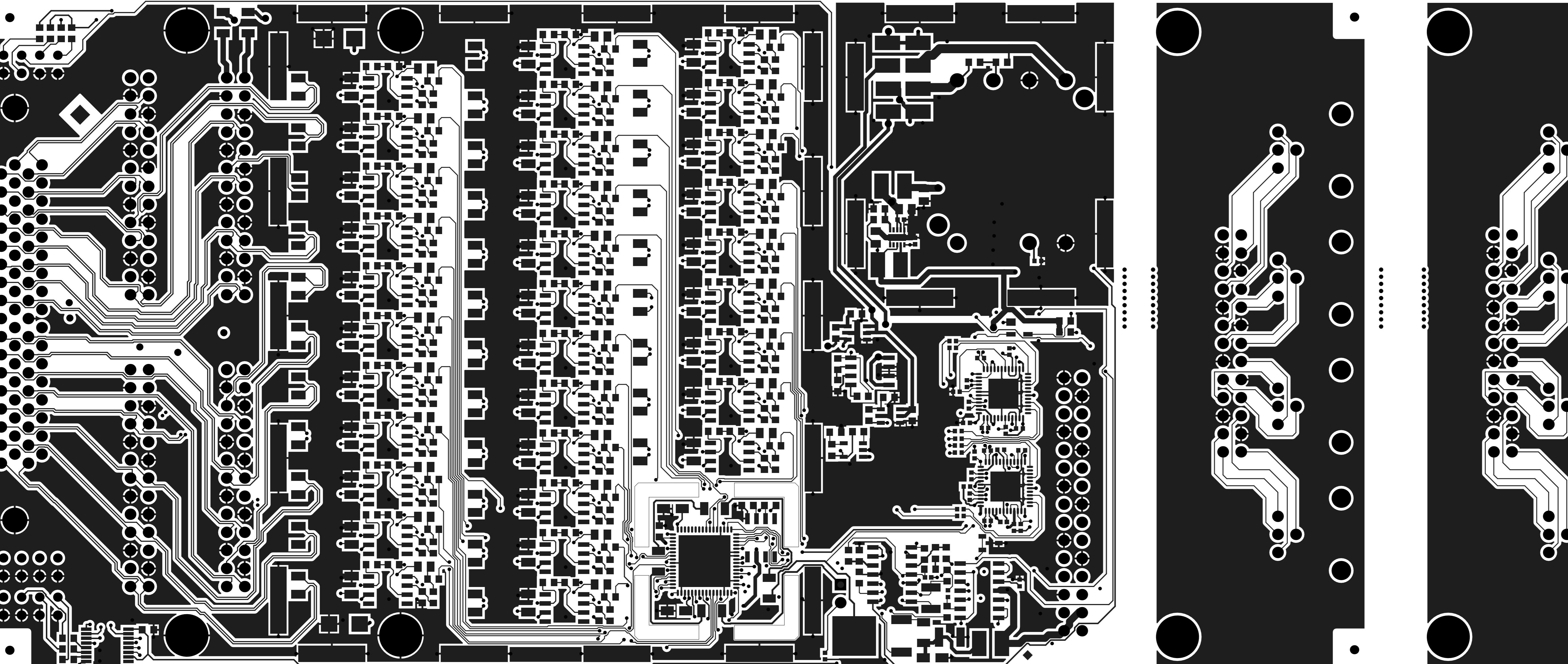
Simulations include DAC noise model



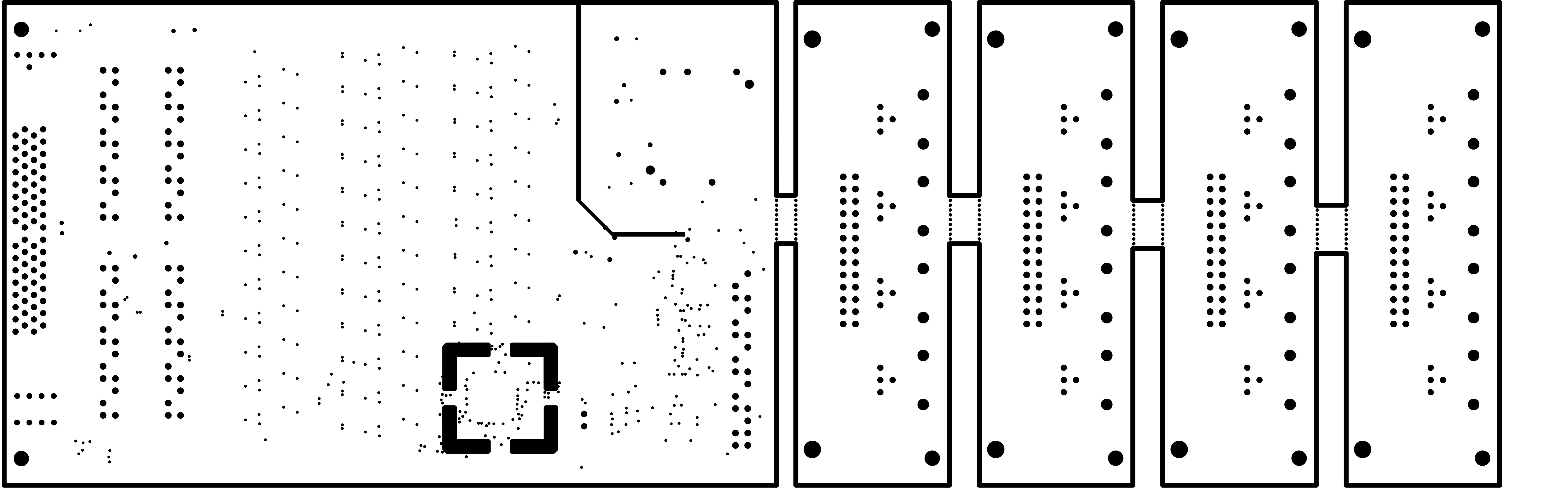


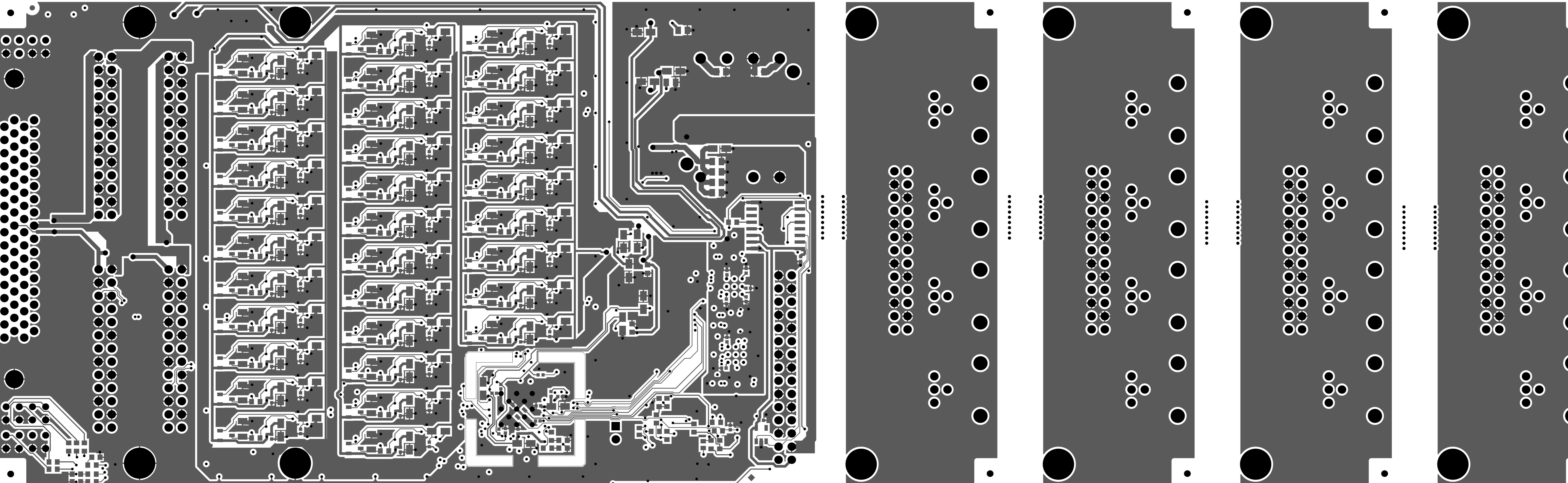






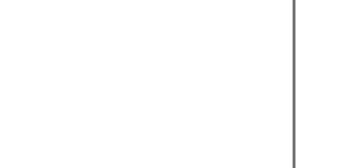
□ □
□ □





bCB 3U DYC 1.6V1.0

MUL USE 2012



ARRI

IC32



IC33



IC13

IC1N



IC1P

