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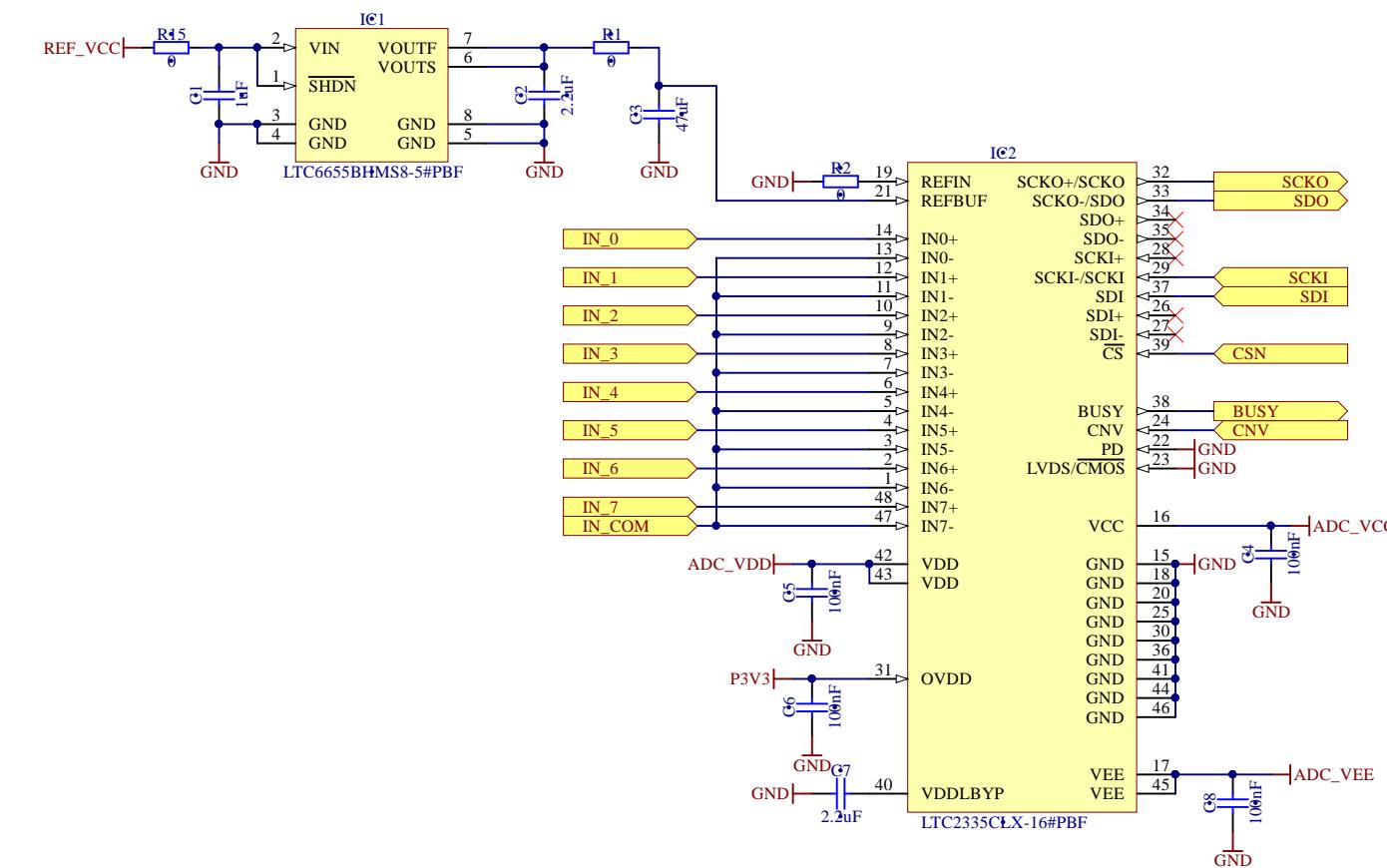
A

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E



Project/Equipment 3U ADC

Document

**ADC + reference**

Designer G.K.	Drawn by G.K.	XX/XX/XXXX
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Warsaw University of Technology ISE
Nowowiejska 15/19

ARTIQ

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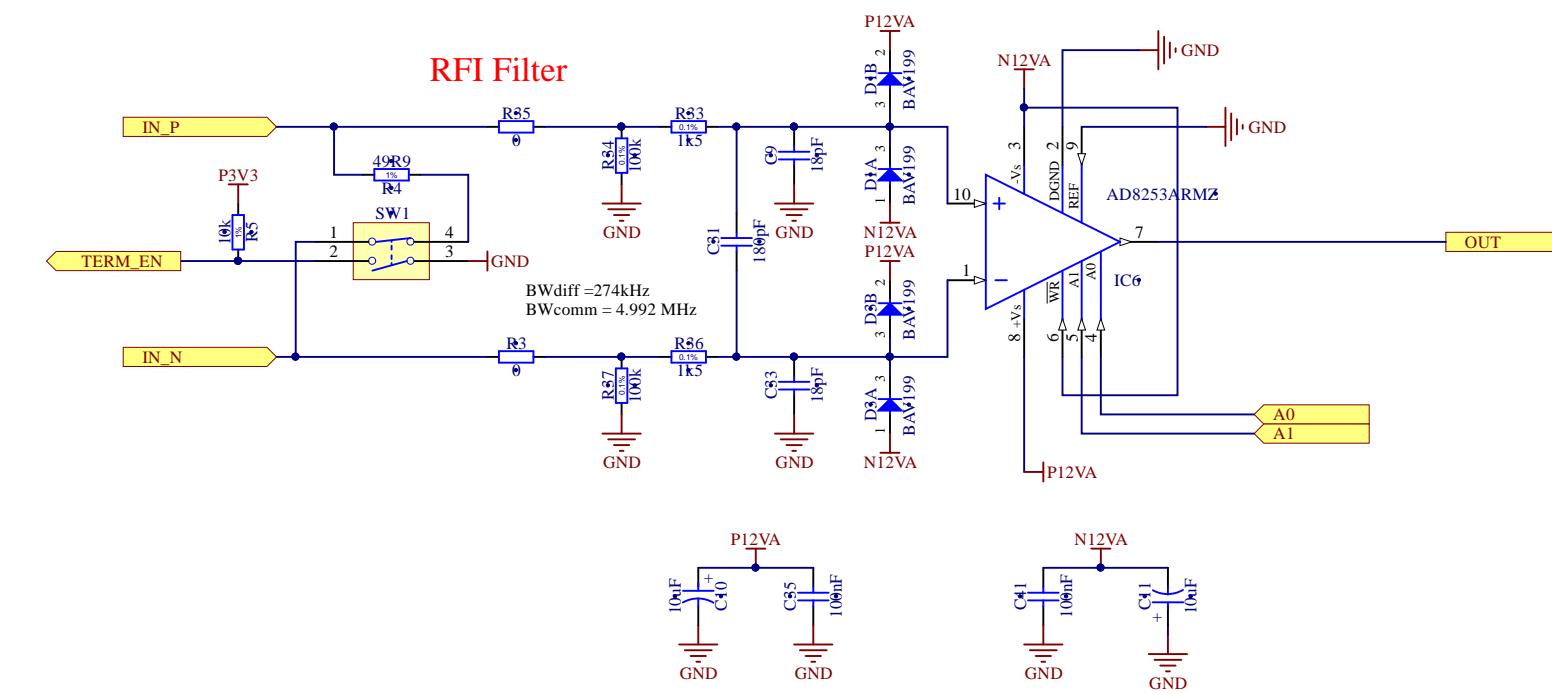
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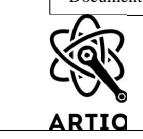
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Project/Equipment 3U ADC

Document

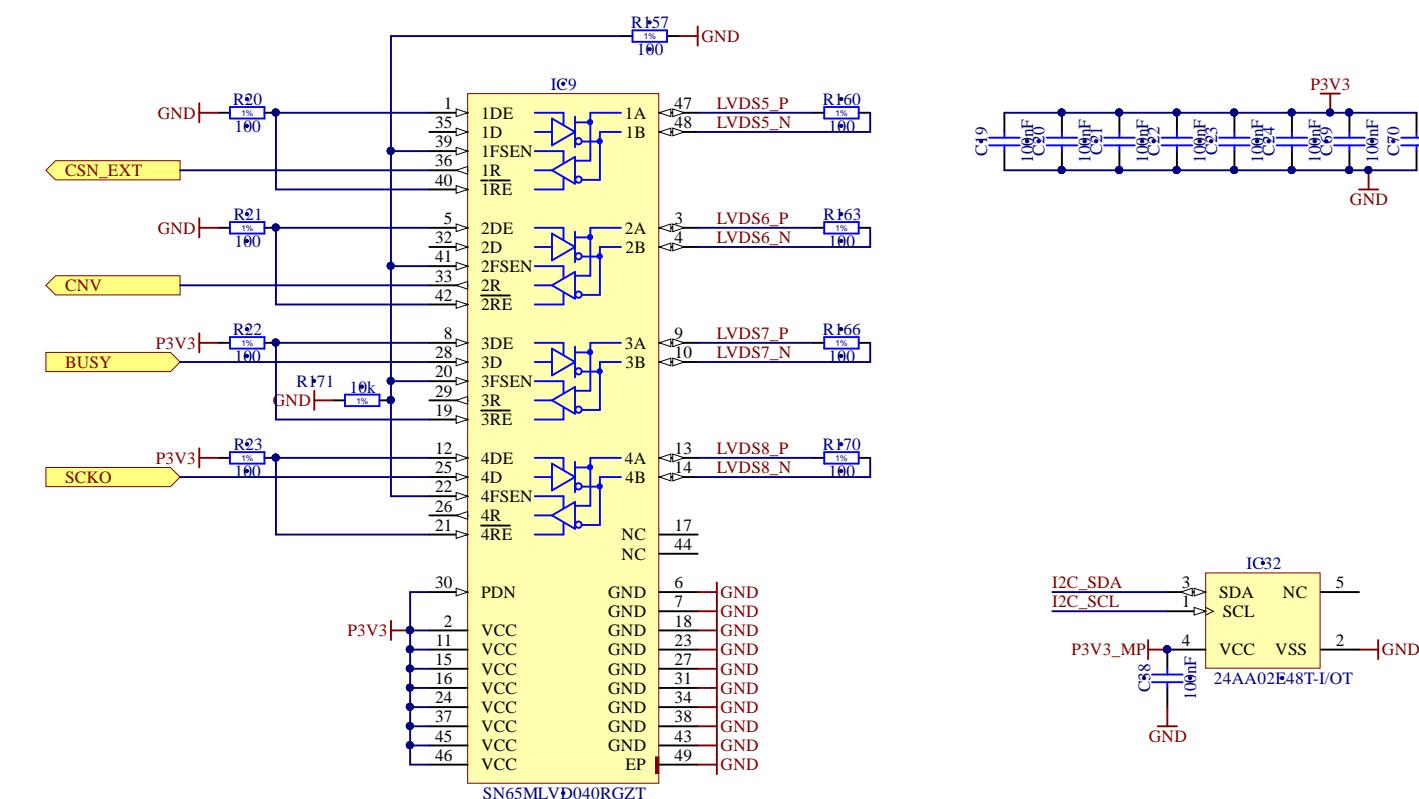
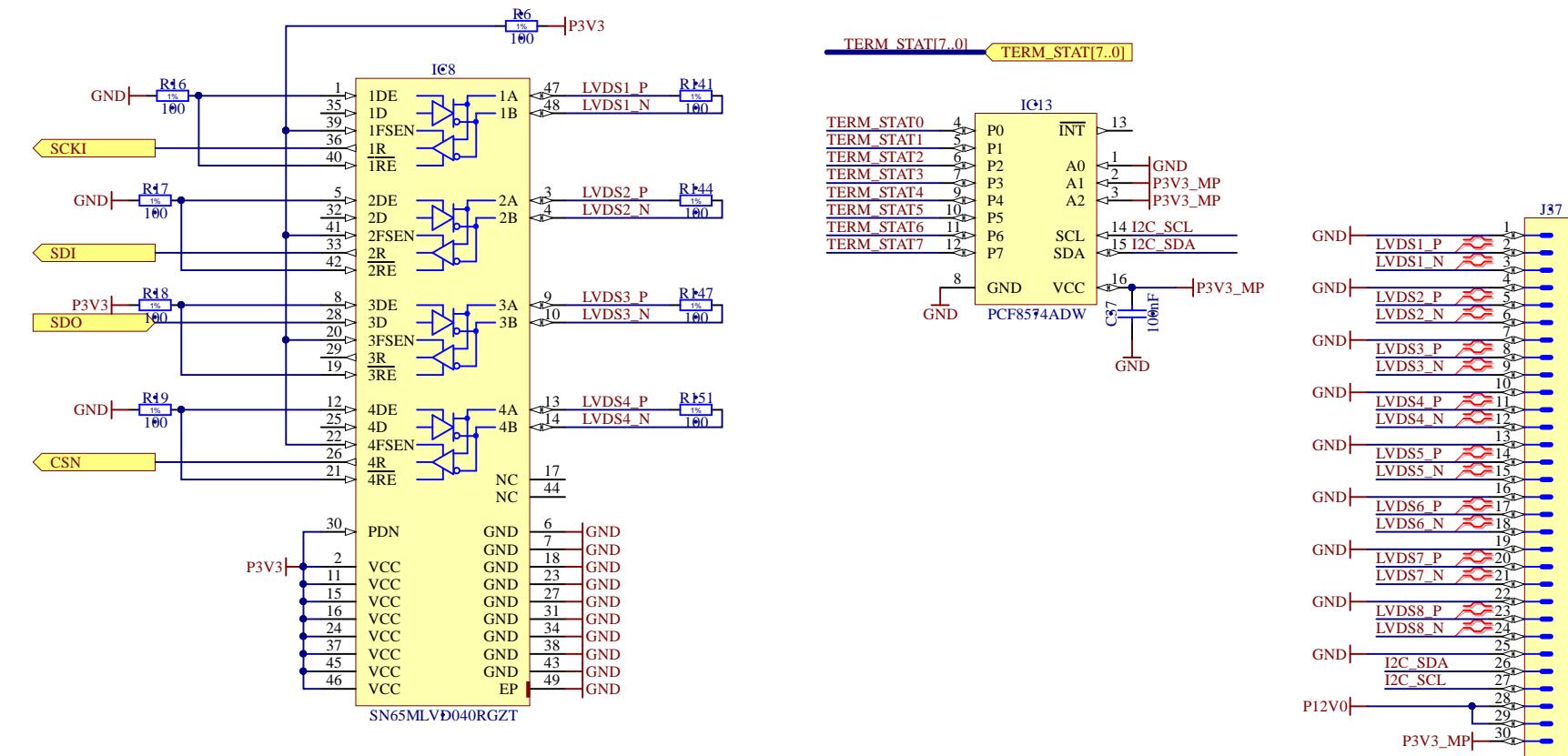


Input chnnanel DPGA

Designer G.K.	Drawn by G.K.	XX/XX/XXXX
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This module connects to Kasli or to VHDCI Metlino breakout board
 All signals are LVDS, in case of Metlino VCC is 1.8V
 I2C is 3.3V LVCMOS
 P3V3_MP can handle up to 20mA
 P12V0 current is up to 500mA

please make a list of IC names and functions in corner of schematic for easier reading



Project/Equipment 3U ADC

Document



LVDS Interface I2C logic

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Multi-channel ADC, codenamed Novogorny. This is intended to be a medium-performance design, targeting slow feedback loops and data-logging applications. It will not aim for anything particularly ambitious in terms of noise/drift/speed/channel count, and is likely to be based on an IC like the ADAS3022. "Cheap and simple" is the goal here.

Specification below, based on the discussion at #153:

Channel-count: 8
Connectors: insulated BNCs, front panel based on 3U_BNC module
Resolution: 16-bit, with RMS noise and drift in a +1K "typical lab environment" < a few LSB.

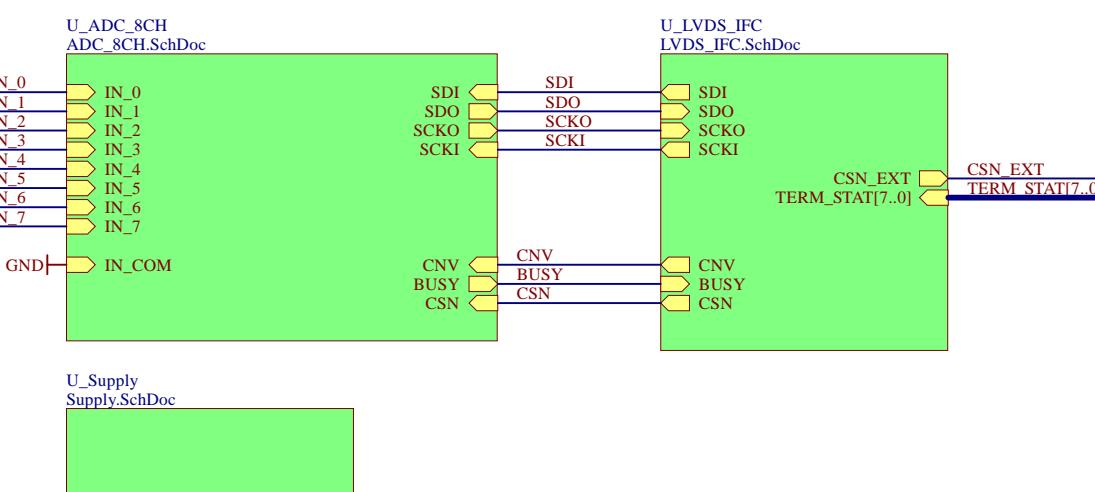
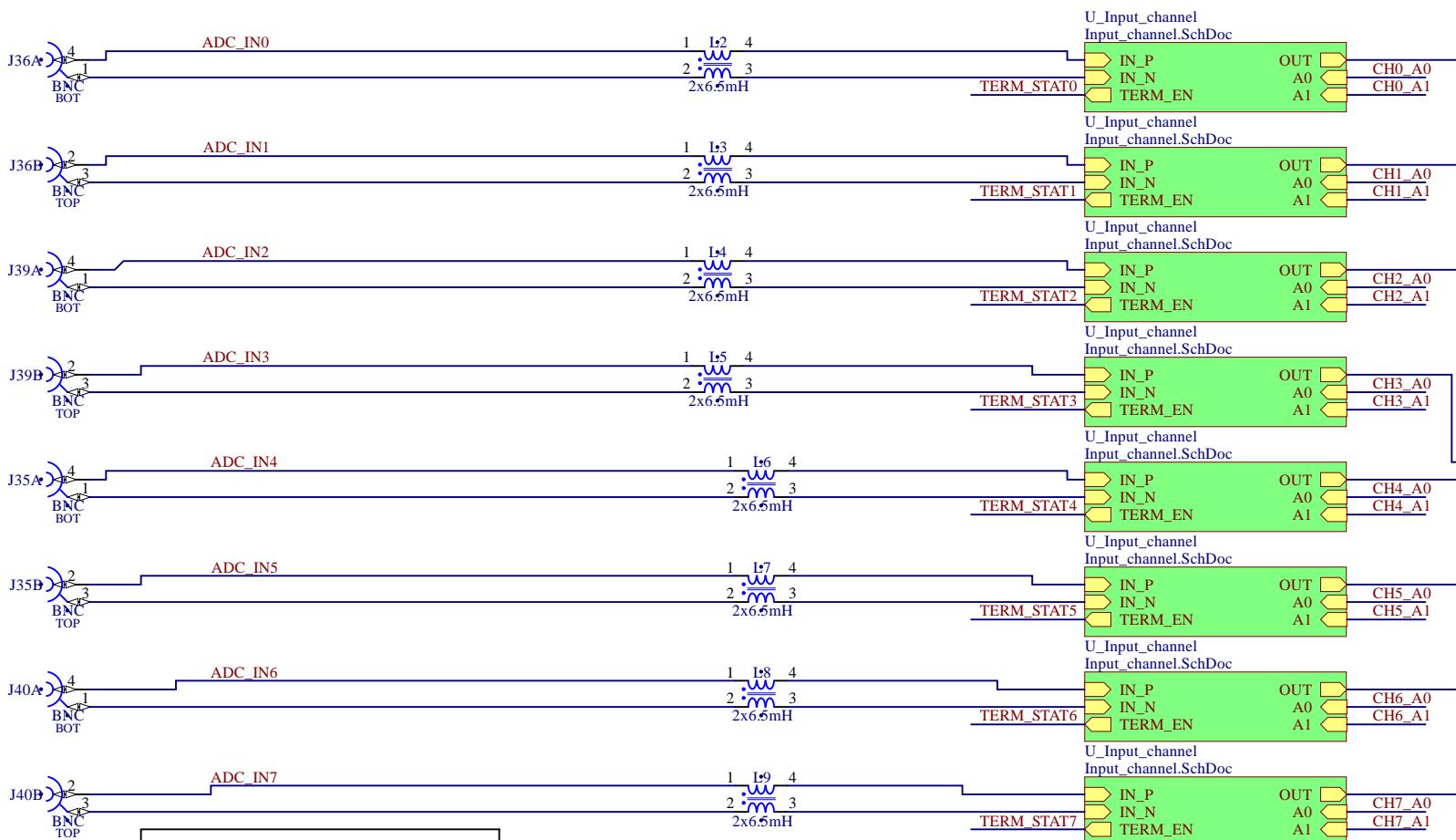
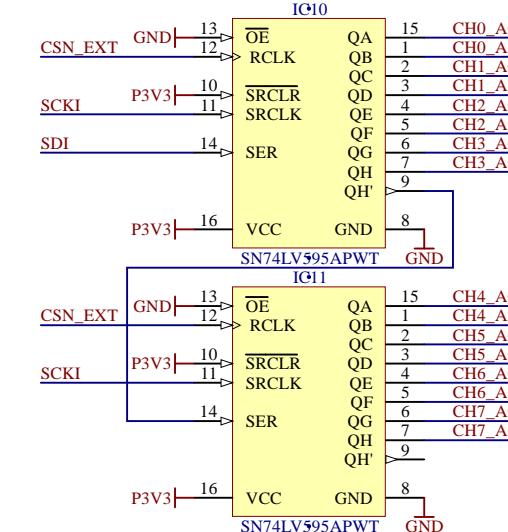
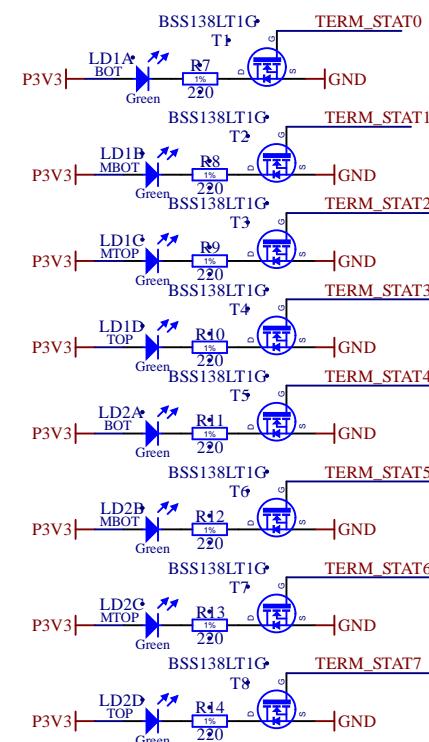
Sample rate: >100kSPS for a single channel (1MSPS would be nice)

Input range: +/-10V max, ideally with several gain/range settings

Front-end: basic common-mode + differential-mode filters to minimise RFI issues in a lab environment. Filter cut-off chosen to avoid compromising ADC bandwidth too much. Suitable protection diodes (eg so 10V can be connected to the input when the board is not powered)

Gounding: 10k between input grounds and circuit ground. Either keep grounds for all inputs isolated from each other (preferred) or tie input grounds together, and add suitable common mode chokes.

Input termination: 10k to input grounds. This is a low speed board, so 50R termination not required.



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Project/Equipment 3U ADC

Document



3U ADC - top 8 channel ADC

FTG17
FTG18
FTG19
FTG20

A3

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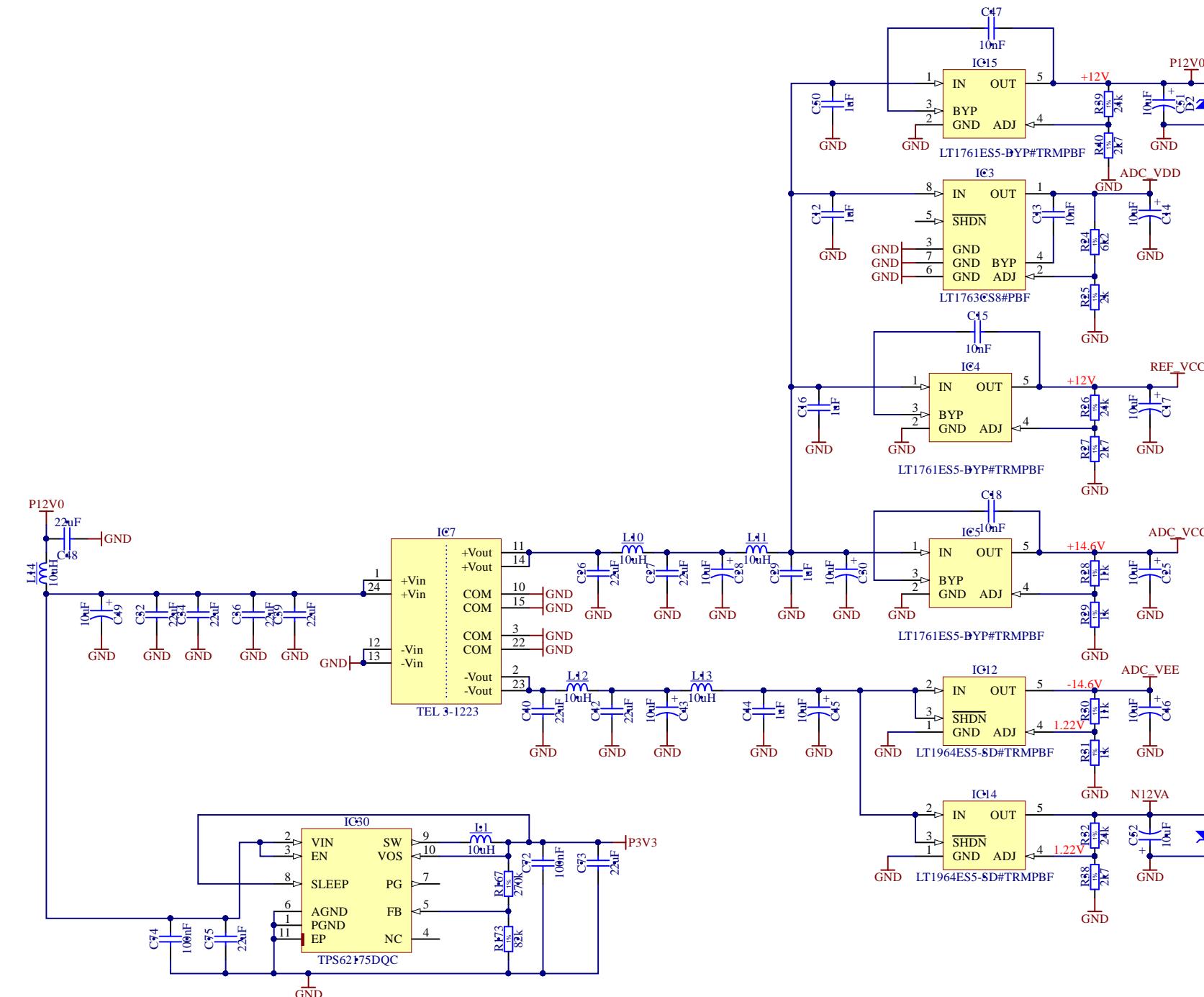
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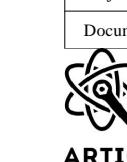
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ADC_VDD
Power losses
 $P_1 = (15V-5V) * 14.5mA = 145mW$
 $\text{Th}_{jc}=35K/W$
 $T_c=35*0.145=5K$

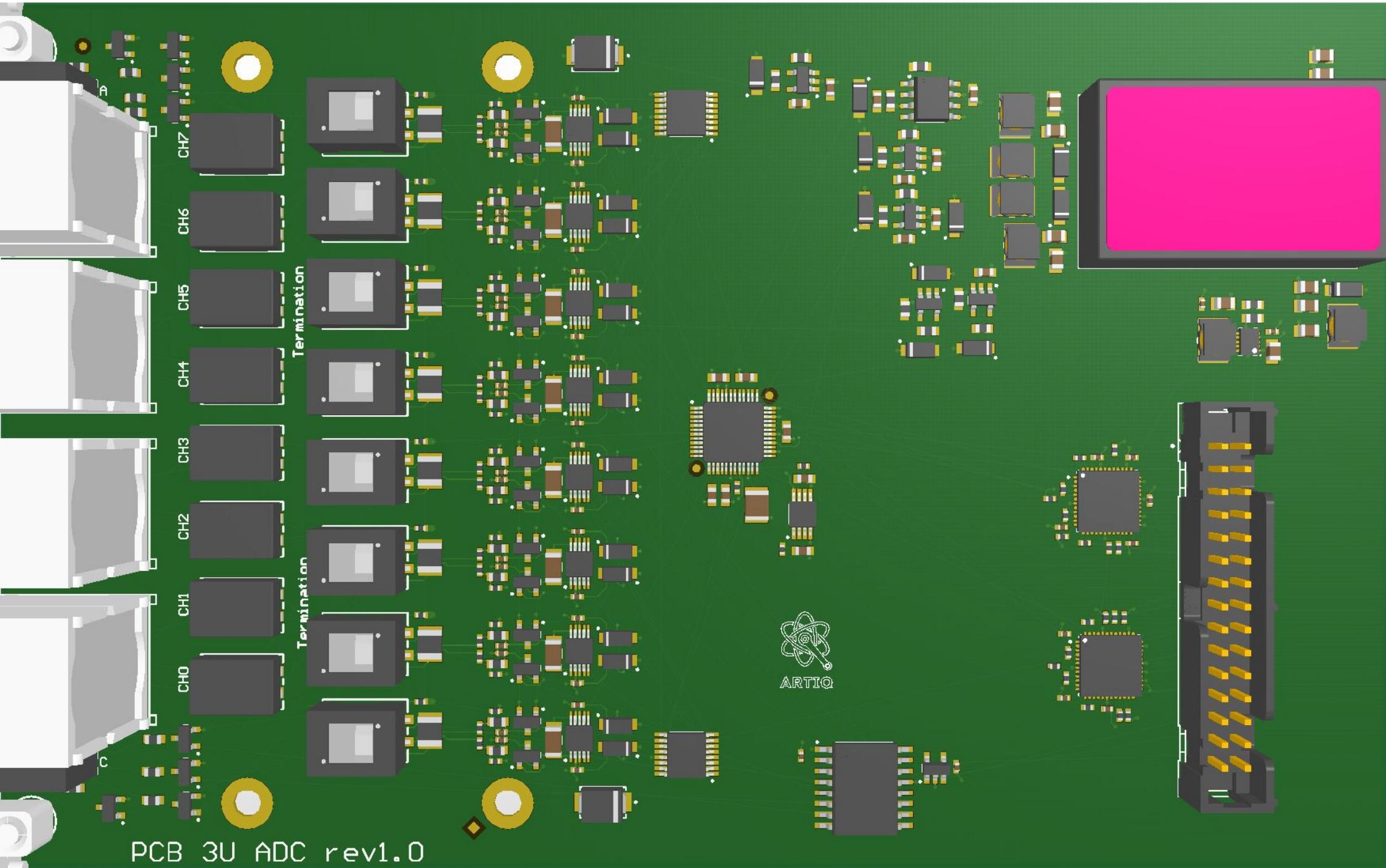
Power budget:
AD8253ARMZ 8*4mA=32mA
LTC2335
I_{VCC} 4.3mA 0-38V
I_{VEE} -5mA -16.5 - 0
I_{VDD} 14.5mA 5V
I_{OVDD} 4.2mA 1.7 - 5.5V

Project/Equipment 3U ADC



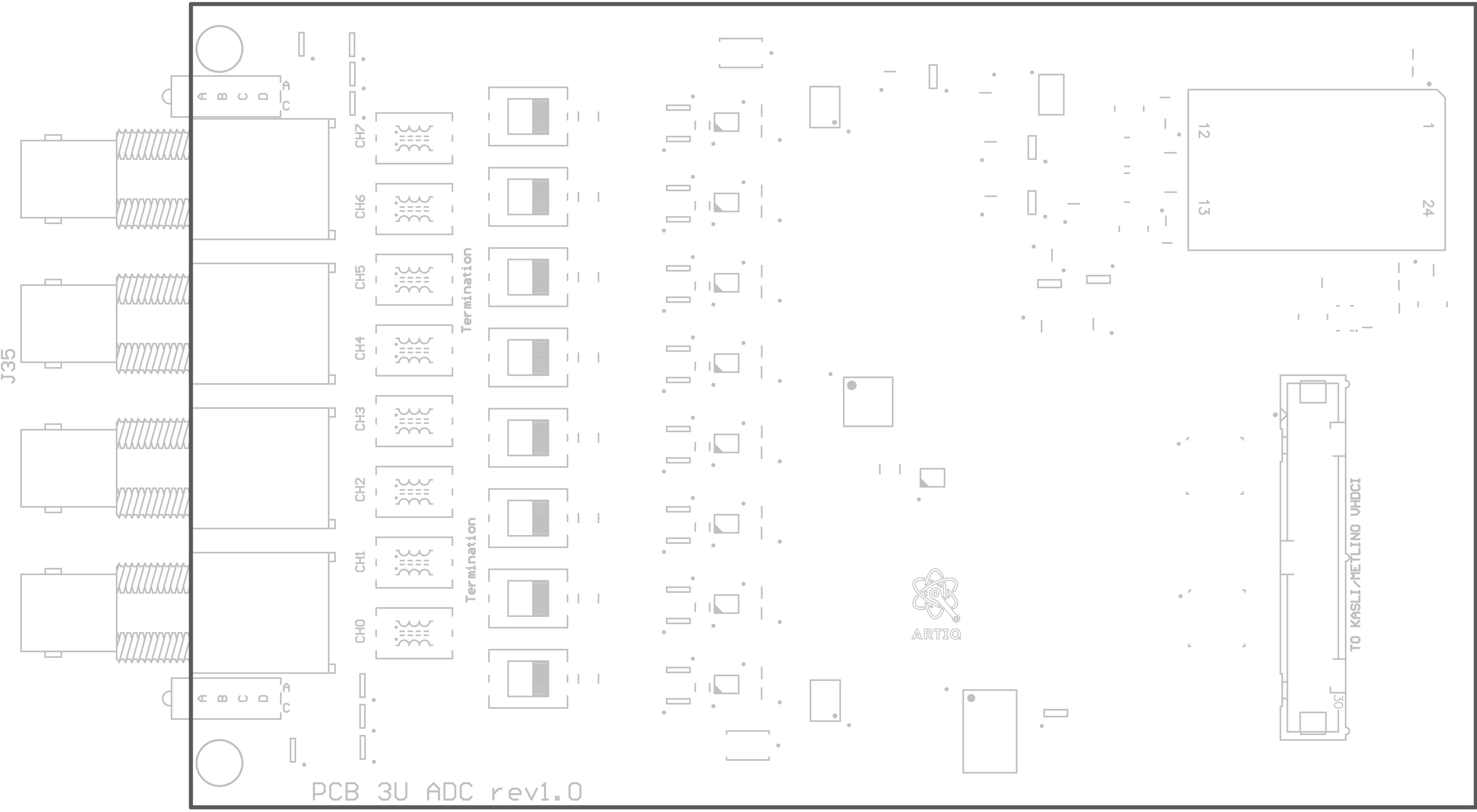
Power Supply converters + LDOs

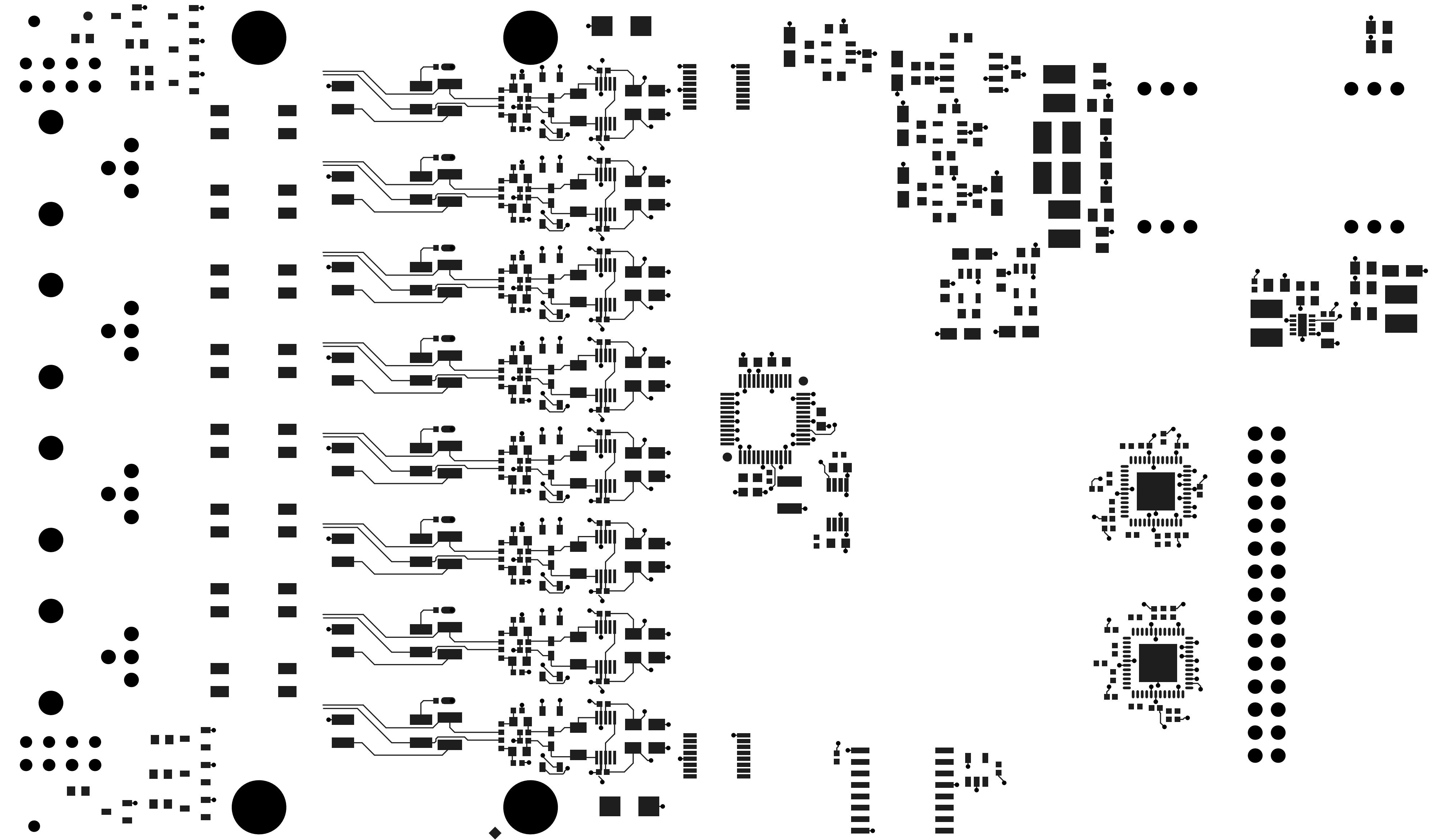
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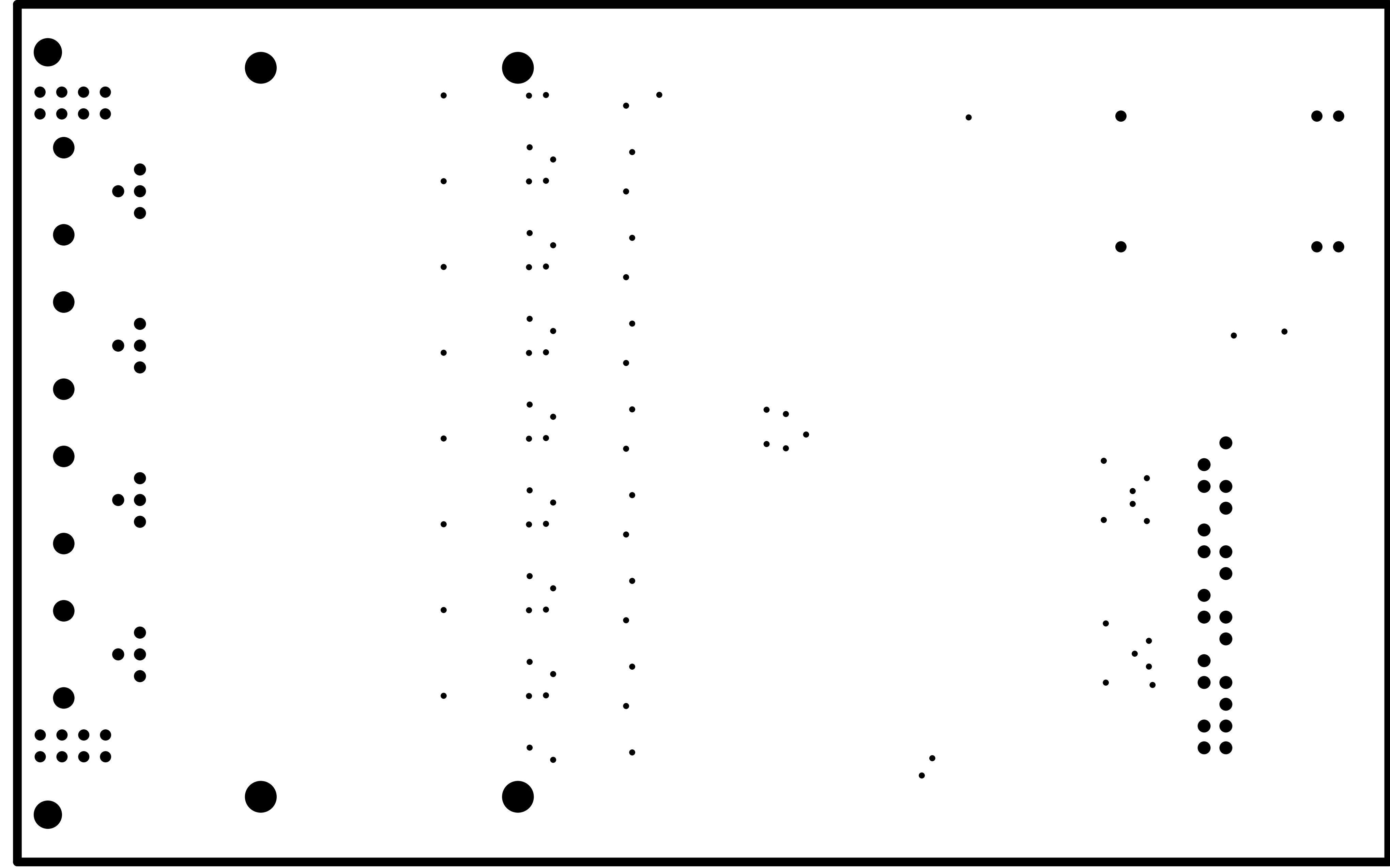


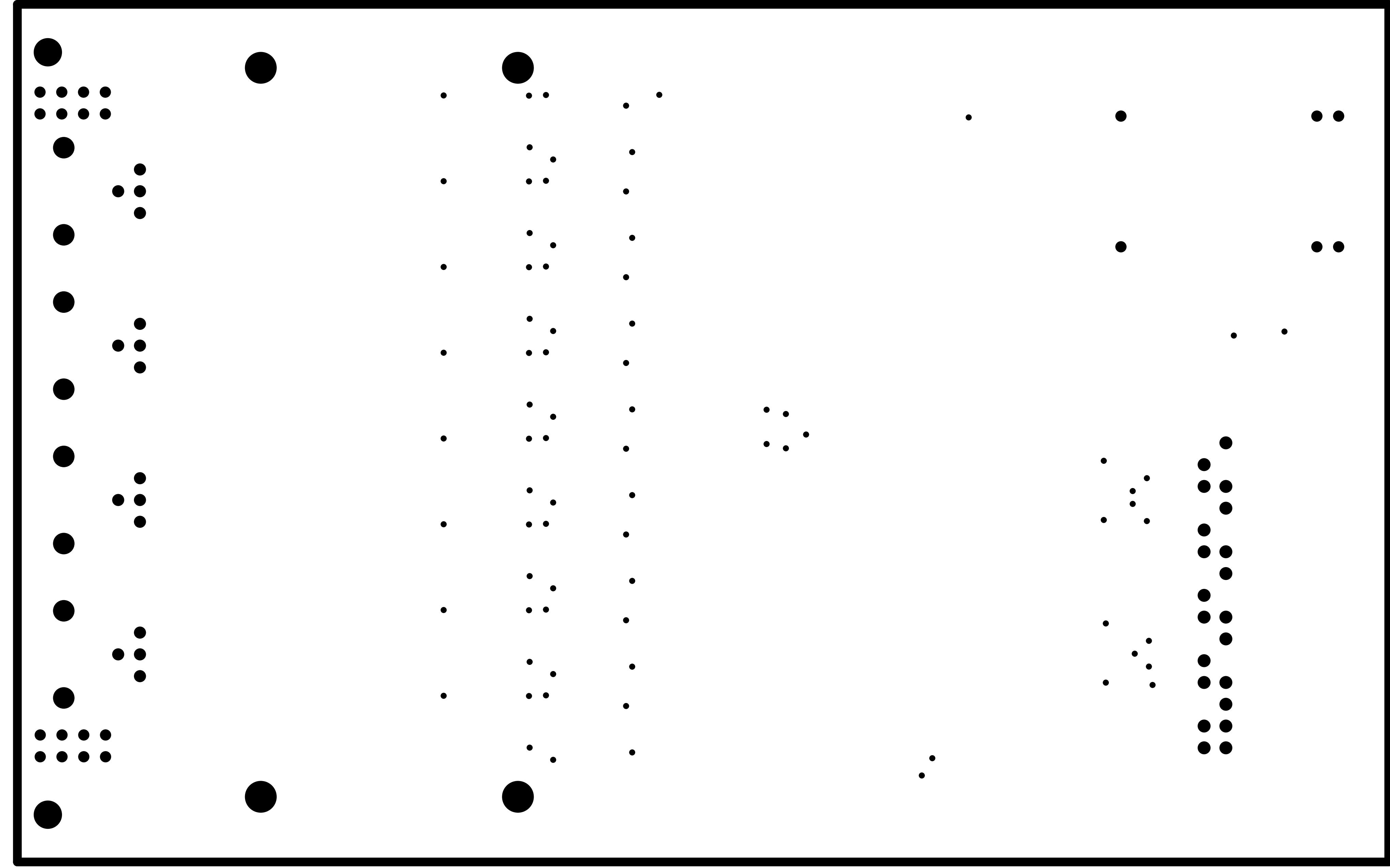


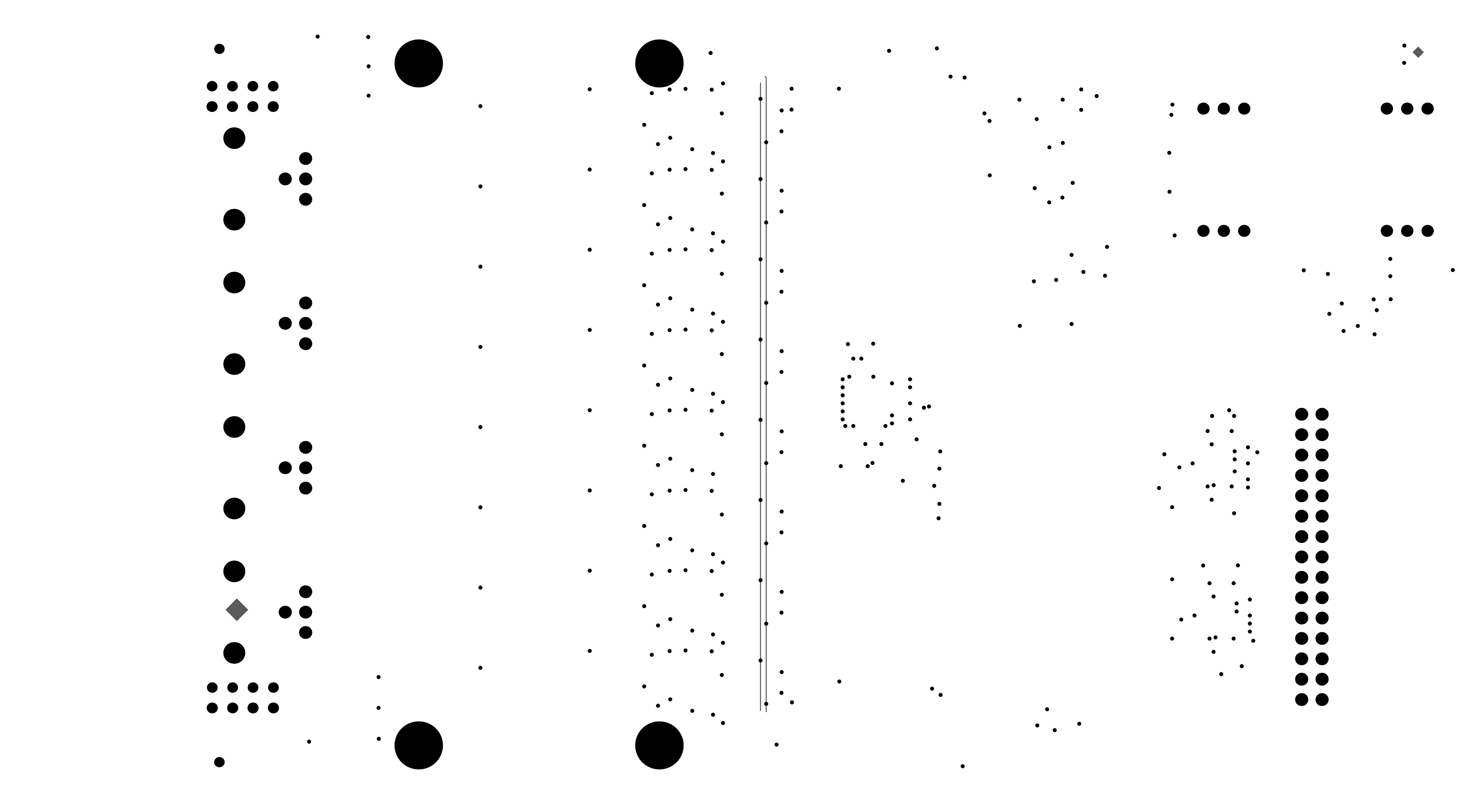
PCB 3U ADC rev1.0













PCB 3U ADC Rev1.0