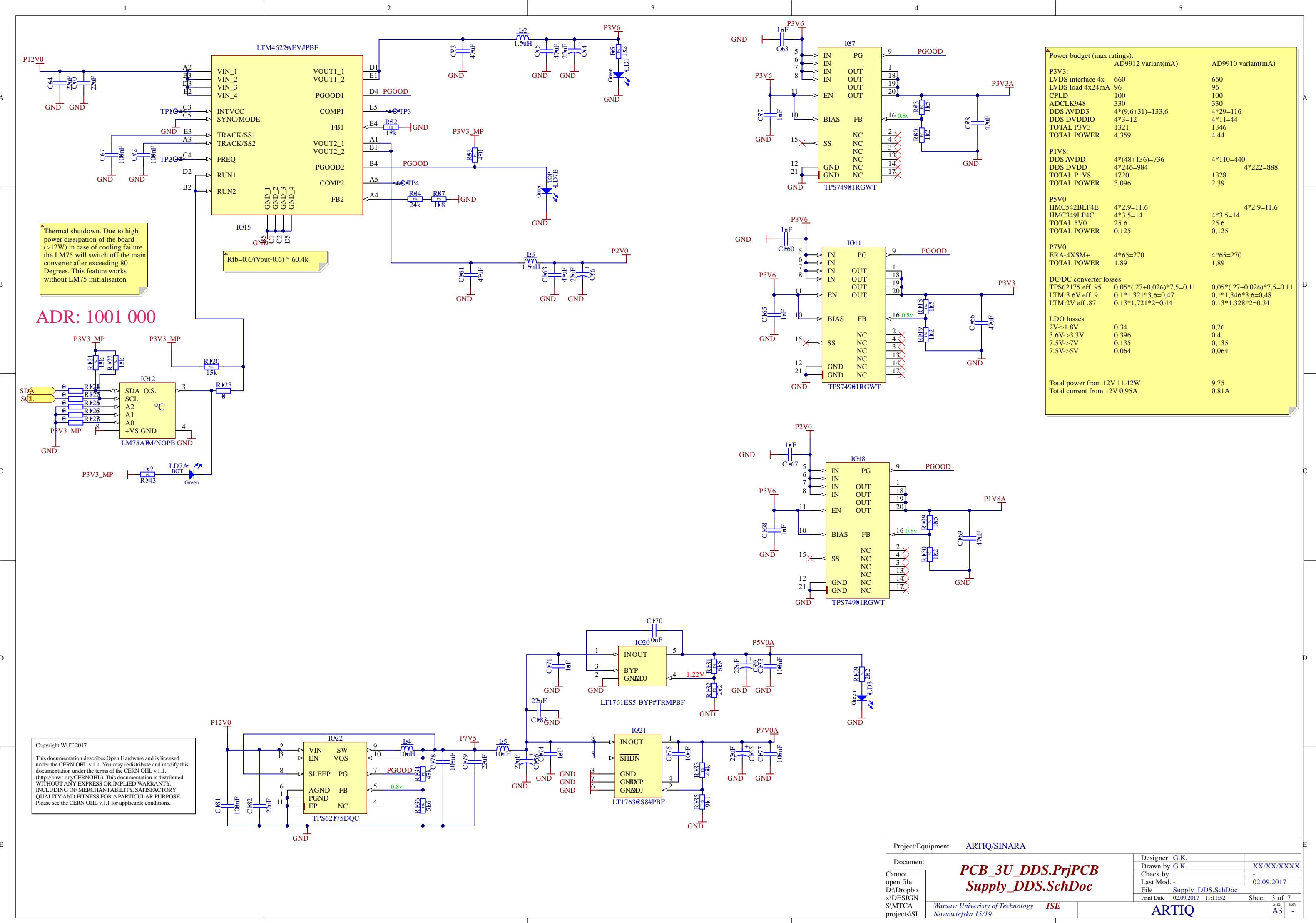
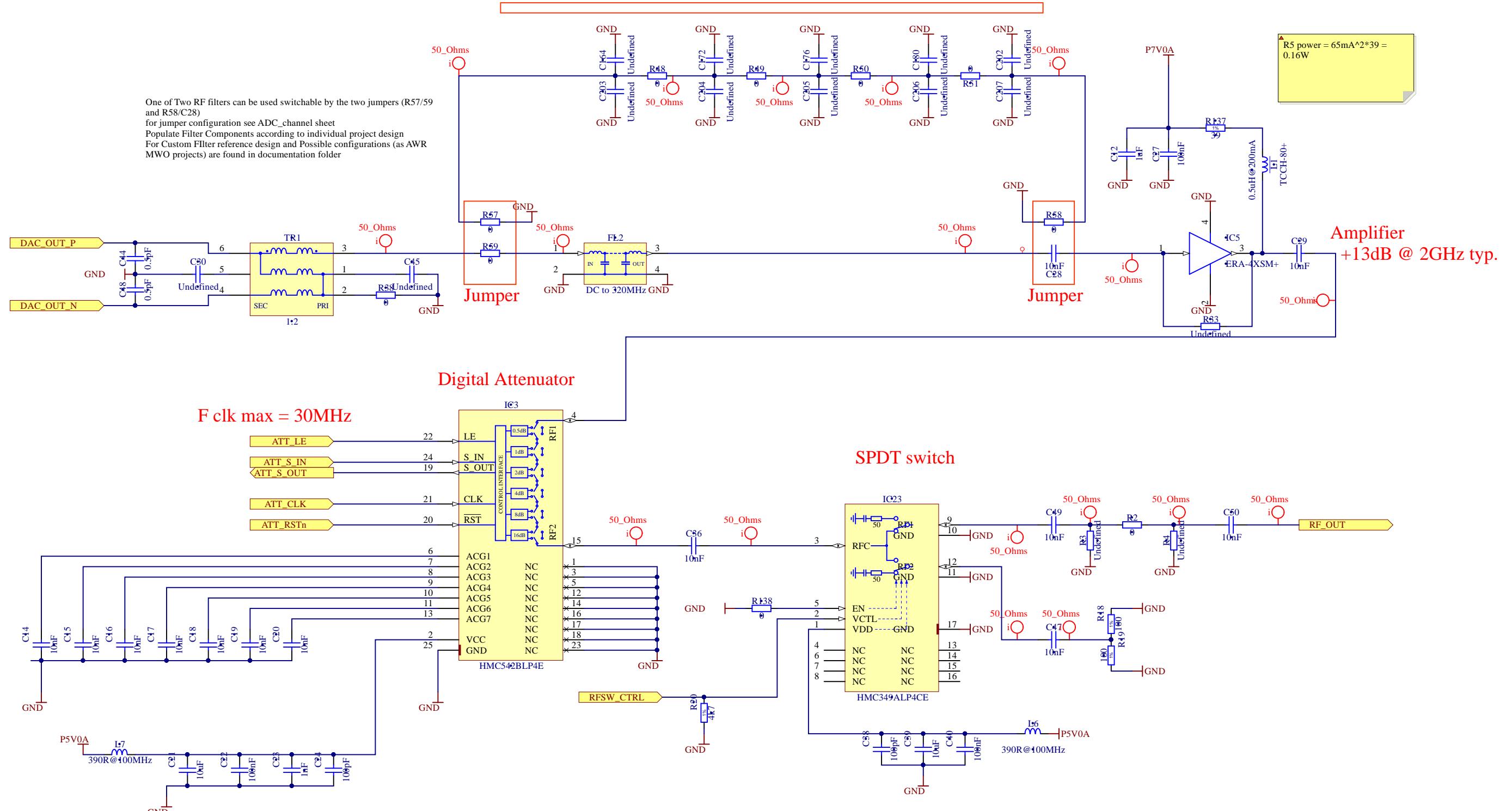


Copyright WUT 2017
This documentation describes Open Hardware and is licensed under the terms of the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING MERCHANTABILITY, SATISFACTORINESS, QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

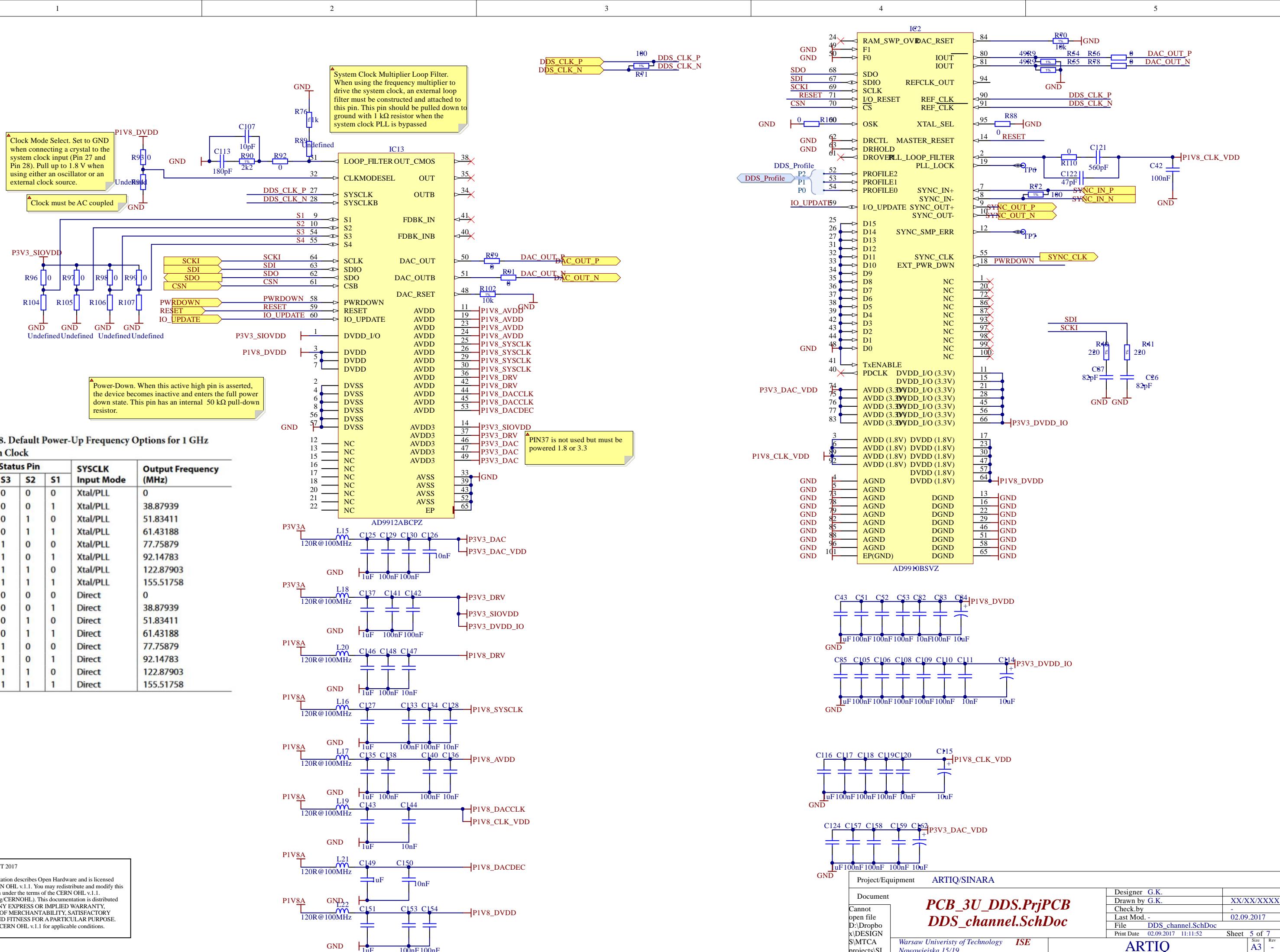


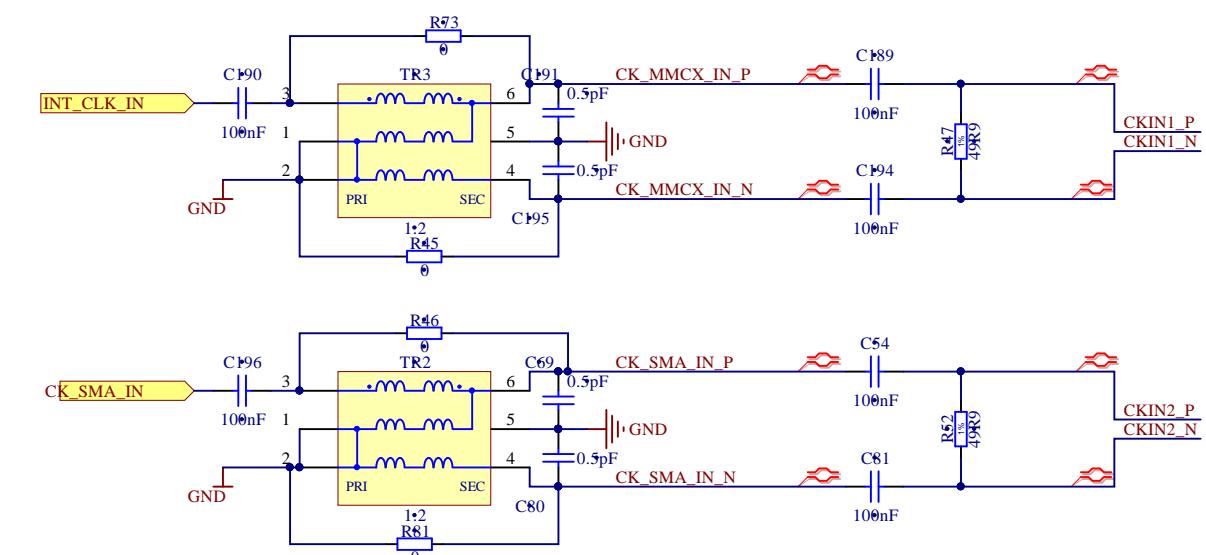


Copyright WUT 2017
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1 for applicable conditions.

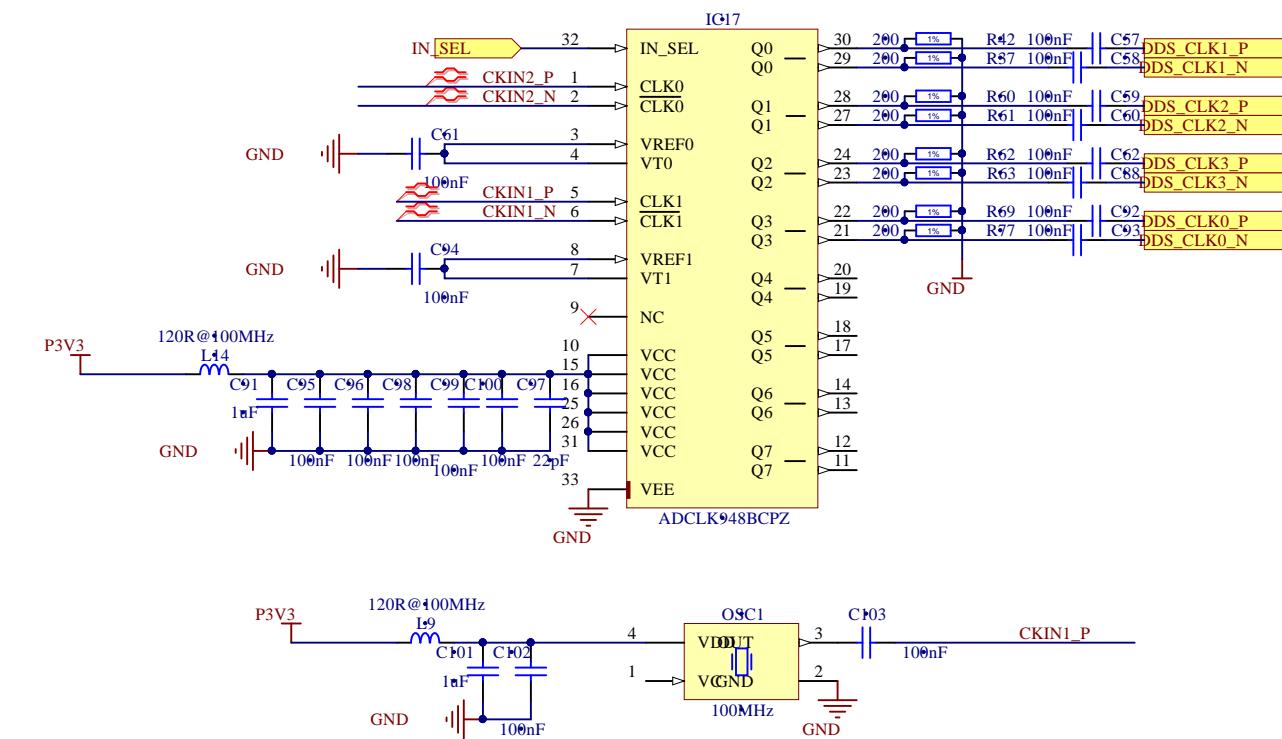
Project/Equipment		ARTIQ/SINARA	
Document	Designer G.K.	Drawn by G.K.	XX/XX/XXXX
Cannot open file D:\Dropbox\DESIGN\SMTCAs\projects\SI	Check by -	Last Mod. -	02.09.2017
File DDS_OUT_channel.SchDoc	Print Date 02.09.2017 11:11:52	Sheet 4 of 7	
	Warsaw University of Technology ISE Nowowiejska 15/19		Size A3 Rev -

PCB_3U_DDS.PrjPCB
DDS_OUT_channel.SchDoc





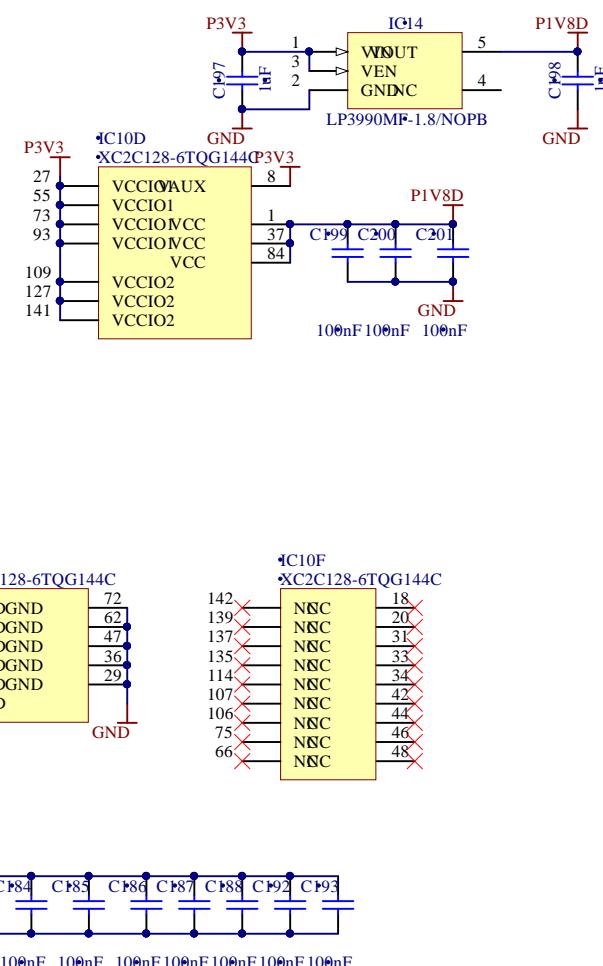
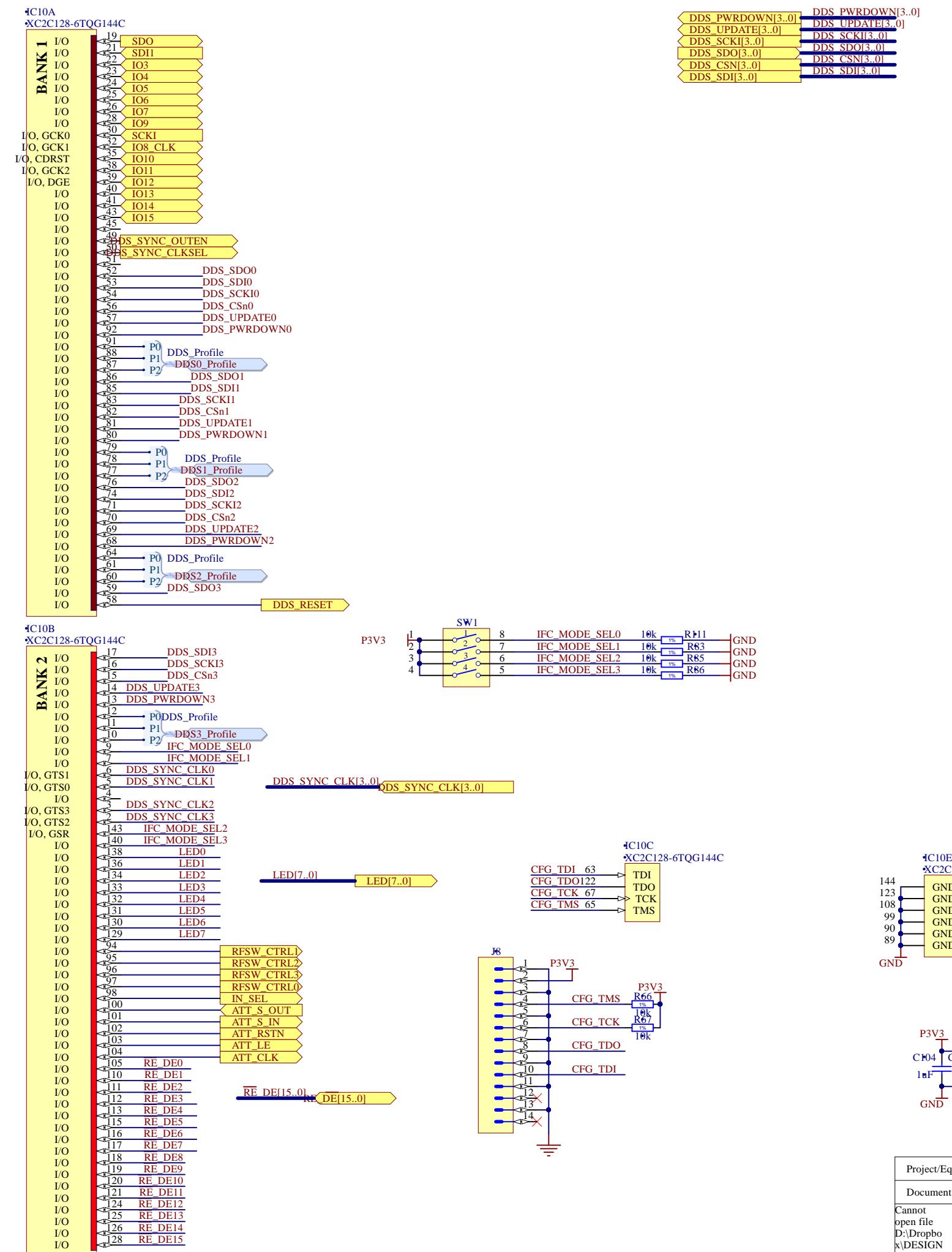
AC-Coupled Input Termination, Such as LVDS and LEVPE



Copyright WUT 2017

This documentation describes Open Hardware and is licensed under the CERN OHL, v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNohl>) This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

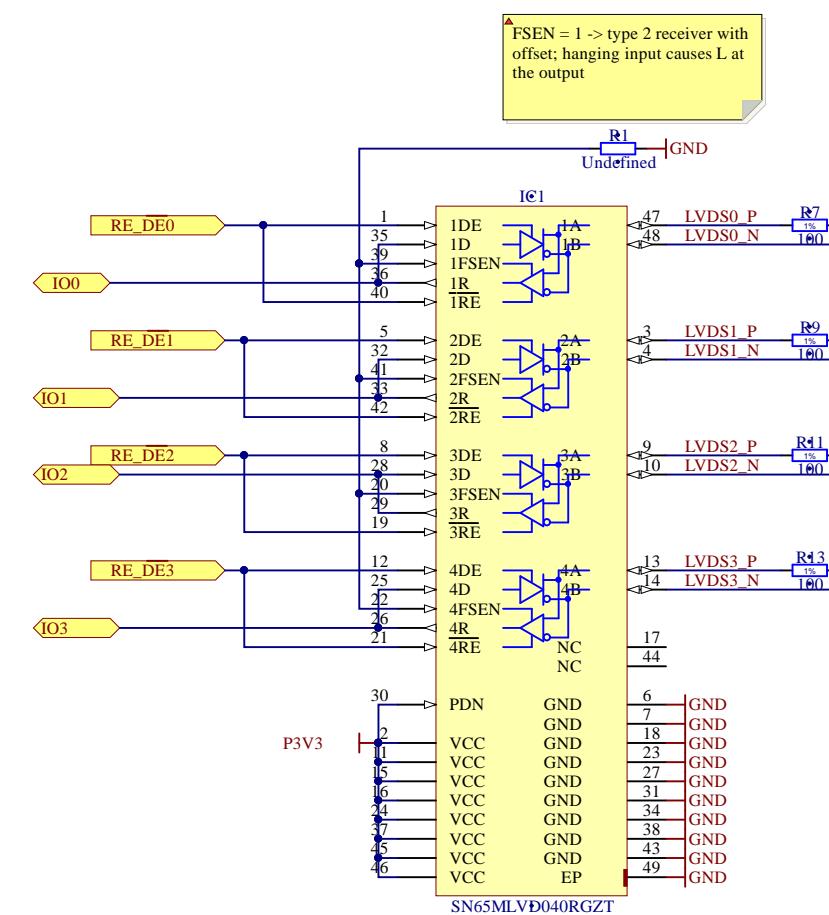
Project/Equipment	ARTIQ/SINARA
Document	<i>PCB_3U_DDS.PrtPCB CLK_INPUT.SchDoc</i>
Cannot open file D:\Dropbox\DESIGN\S\MTCA projects\SI	Designer G.K. Drawn by G.K. XX/XX/XXXX Check by - Last Mod. - 02.09.2017 File CLK_INPUT.SchDoc Print Date 02.09.2017 11:11:53 Sheet - of -
Warsaw University of Technology Nowowiejska 15/19	Size Rev A3 -



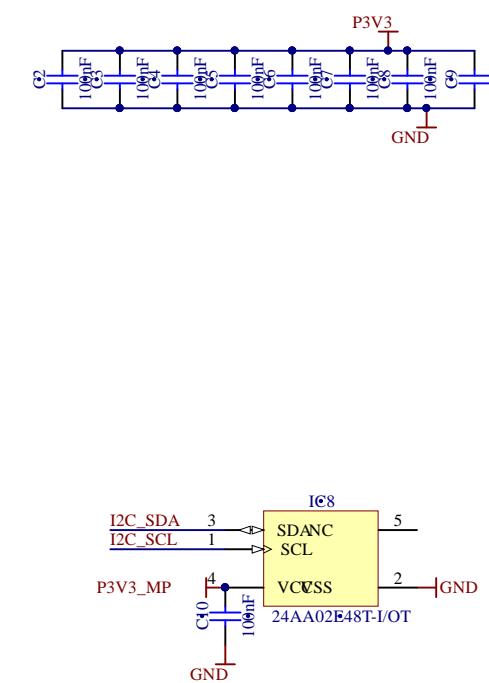
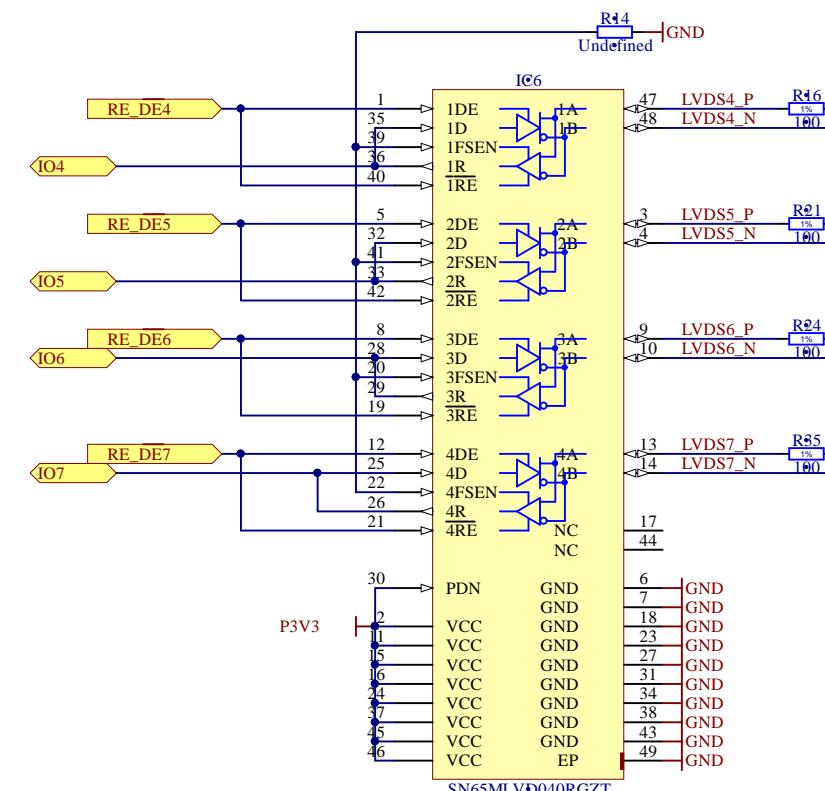
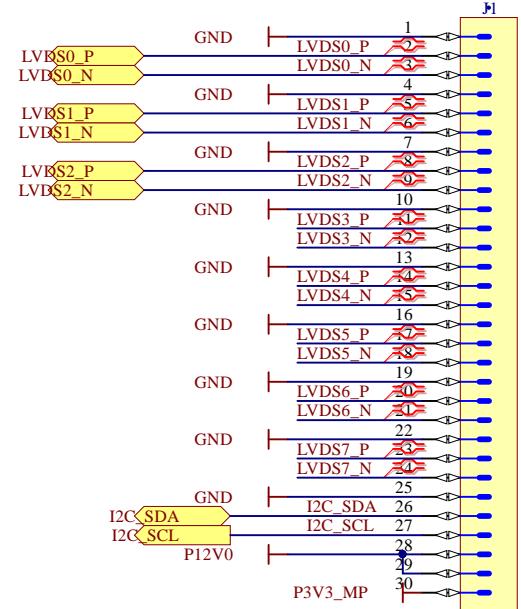
Copyright WUT 2017

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Project/Equipment	ARTIQ/SINARA		
Document		Designer G.K.	
Cannot open file D:\Dropbox\DESIGN\SIMTCA projects\SI	PCB_3U_DDS.PrjPCB CTRL_LOGIC.SchDoc	Drawn by G.K.	XX/XX/XXXX
		Check by -	-
		Last Mod. -	02.09.2017
		File	CTRL_LOGIC.SchDoc
	Warsaw University of Technology Nowowiejska 15/19	Print Date	02.09.2017 11:11:53
	ISE	Sheet	- of -
		Size	Rev
		A3	-
		ARTIQ	



This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I_C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 500mA



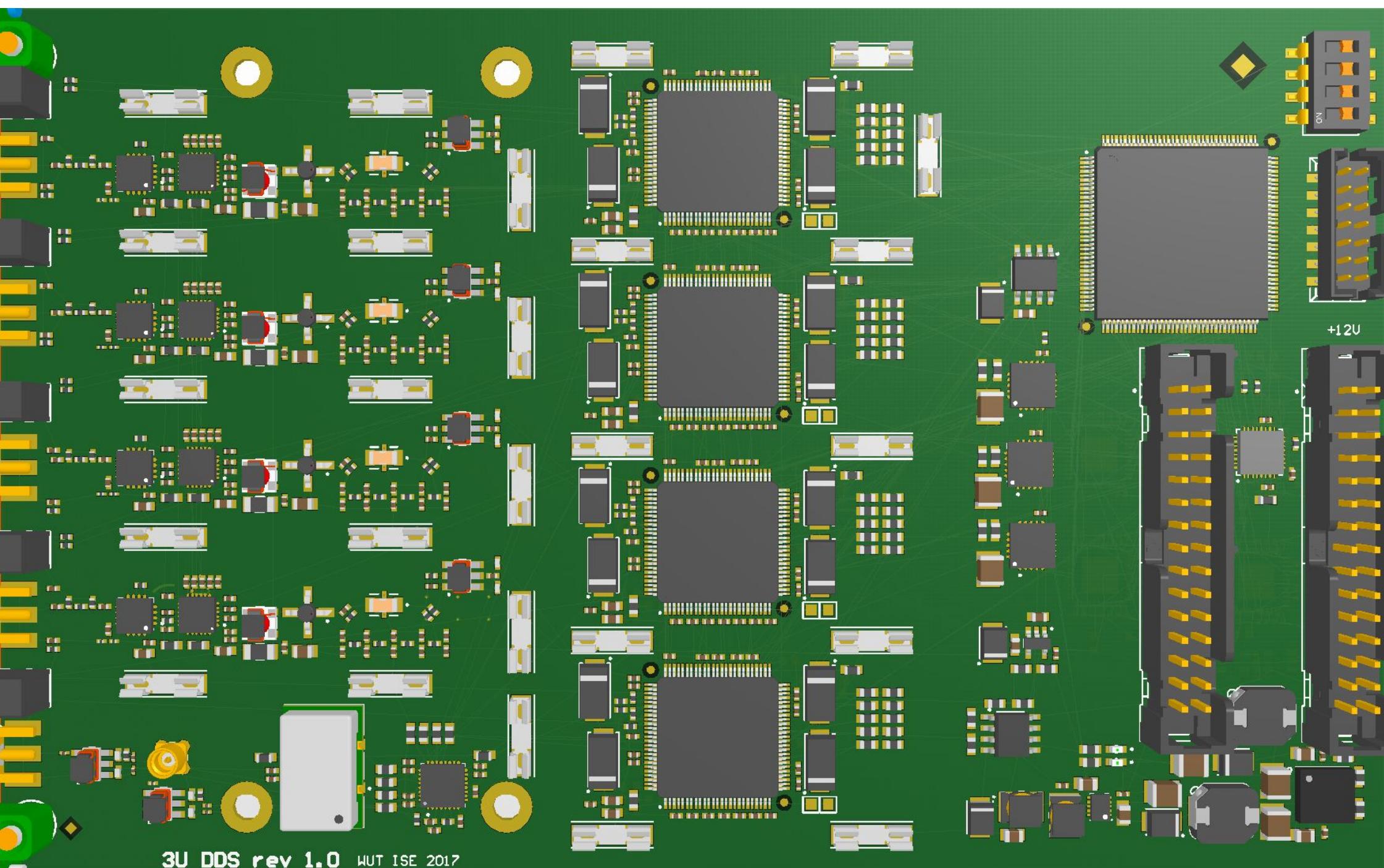
Copyright WUT 2017

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Project Team: APTIO/SINARA

PCB_3U_DDS.PrjPCB
LVDS IFC DDS.SchDoc

Designer	G.K.	
Drawn by	G.K.	XX/XX/XXXX
Check by	-	
Last Mod.	-	02.09.2017
File	LVDS_IFC_DDS.SchDoc	
Print Date	02.09.2017 11:11:53	Sheet _____ of _____
		Size Rev



3U DDS rev 1.0 WUT ISE 2017

