

ARTIQ Sayma

Sayma_AMC

SIZE	DWG NO
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G.K

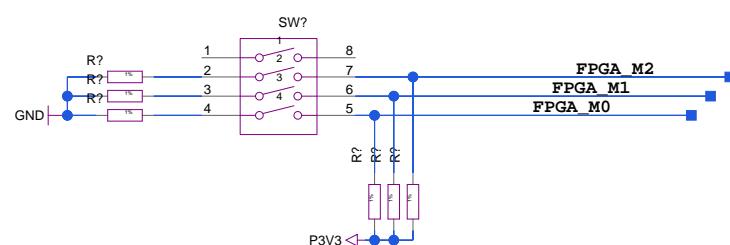
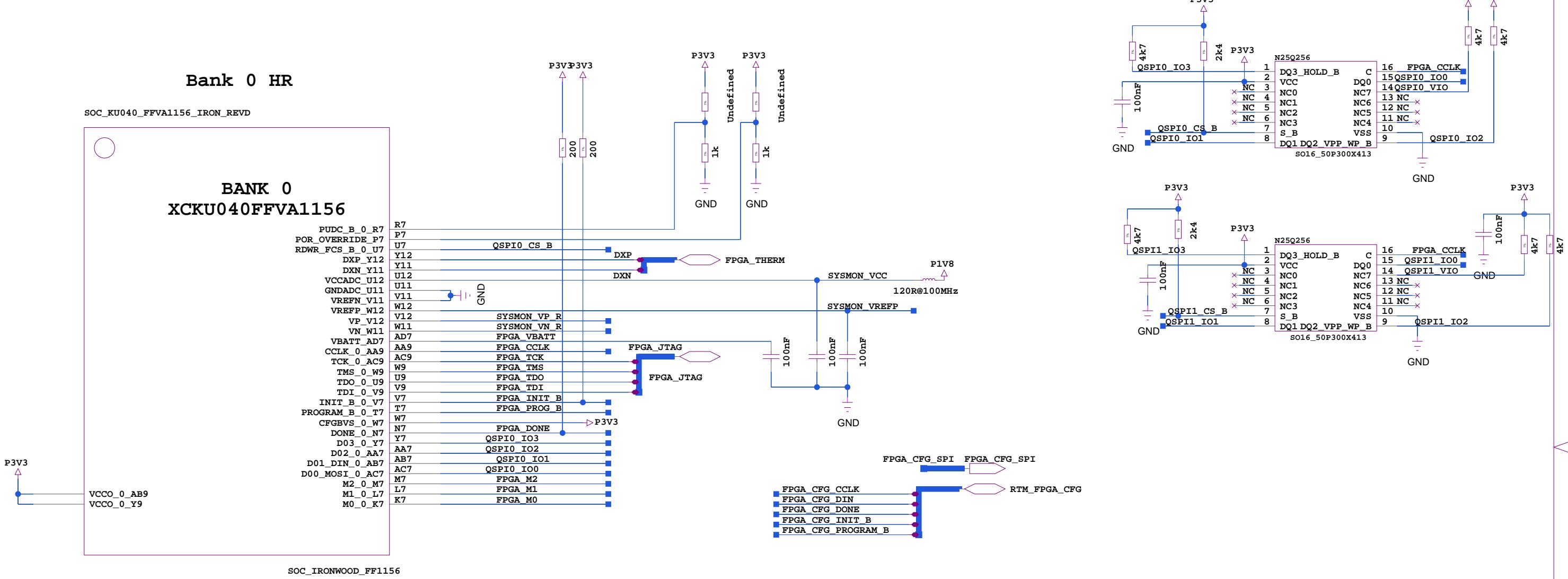
1 2

1

v0.9

2016/11/03:23:35:38

TODO: RIM CONFIG



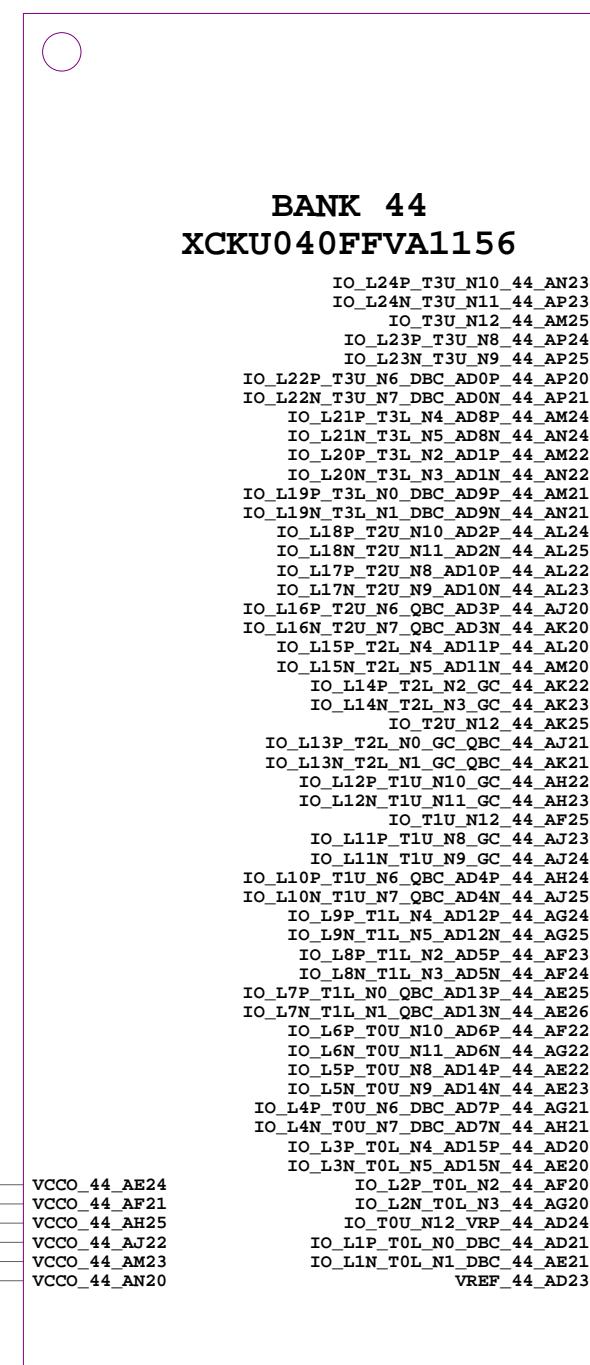
FPGA_XCKU040FFVA1156

ARTIQ Sayma

FPGA Bank 0 CFG

Bank 44 HP

SOC_KU040_FFVA1156_IRON_REV0



U1

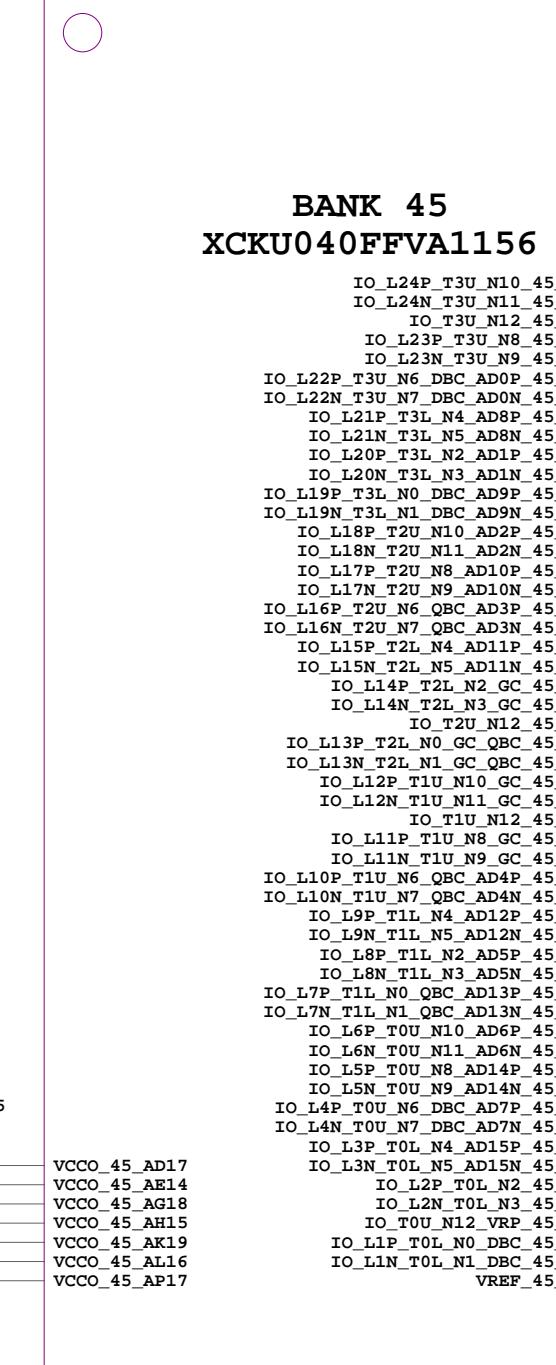
SOC_IRONWOOD_FF1156

SDRAM_DDR3_64

240 100nF
GND GND

Bank 45 HP

SOC_KU040_FFVA1156_IRON_REV0



U1

SOC_IRONWOOD_FF1156

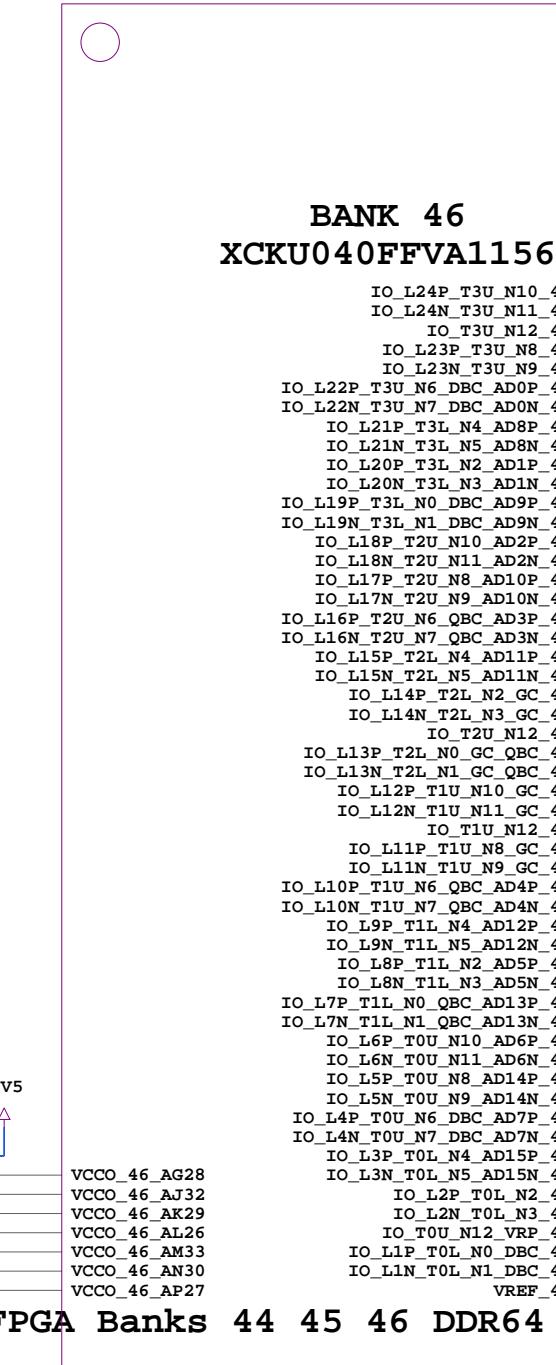
SDRAM_DDR3_x64

240 100nF
GND GND

FAT_PIPE1_AT_PIPE2

Bank 46 HP

SOC_KU040_FFVA1156_IRON_REV0



U1

SOC_IRONWOOD_FF1156

240 100nF
GND GND

FPGA Banks 44 45 46 DDR64

FPGA_XCKU040FFVA1156



ARTIQ Sayma

FPGA Banks 44 45 46 DDR64

SIZE A3

DWG NO.

REV v0.9

DRAWN BY G.K.

SHEET 3 of 29

2016/11/03:23:13:54

BANK 47
XCKU040FFVA1156

IO_L24P_T3U_N10_47_V26
IO_L24N_T3U_N11_47_W26
IO_T3U_N12_47_U29
IO_L23P_T3U_N8_47_V29
IO_L23N_T3U_N9_47_W29
IO_L22P_T3U_N6_DBC_AD0P_47_U26
IO_L22N_T3U_N7_DBC_AD0N_47_U27
IO_L21P_T3L_N4_AD8P_47_W28
IO_L21N_T3L_N5_AD8N_47_Y28
IO_L20P_T3L_N2_AD1P_47_U24
IO_L20N_T3L_N3_AD1N_47_U25
IO_L19P_T3L_N0_DBC_AD9P_47_V27
IO_L19N_T3L_N1_DBC_AD9N_47_V28
IO_L18P_T2U_N10_AD2P_47_V21
IO_L18N_T2U_N11_AD2N_47_W21
IO_L17P_T2U_N8_AD10P_47_T22
IO_L17N_T2U_N9_AD10N_47_T23
IO_L16P_T2U_N6_QBC_AD3P_47_V22
IO_L16N_T2U_N7_QBC_AD3N_47_V23
IO_L15P_T2L_N4_AD11P_47_U21
IO_L15N_T2L_N5_AD11N_47_U22
IO_L14P_T2L_N2_GC_47_W25
IO_L14N_T2L_N3_GC_47_Y25
IO_T2U_N12_47_Y21
IO_L13P_T2L_N0_GC_QBC_47_W23
IO_L13N_T2L_N1_GC_QBC_47_W24
IO_L12P_T1U_N10_GC_47_AA24
IO_L12N_T1U_N11_GC_47_AA25
IO_T1U_N12_47_Y22
IO_L11P_T1U_N11_GC_47_Y23
IO_L11N_T1U_N9_GC_47_AA23
IO_L10P_T1U_N6_QBC_AD4P_47_AB21
IO_L10N_T1U_N7_QBC_AD4N_47_AC21
IO_L9P_T1L_N4_AD12P_47_AA20
IO_L9N_T1L_N5_AD12N_47_AB20
IO_L8P_T1L_N2_AD5P_47_AC22
IO_L8N_T1L_N3_AD5N_47_AC23
IO_L7P_T1L_N0_QBC_AD13P_47_AA22
IO_L7N_T1L_N1_QBC_AD13N_47_AB22
IO_L6P_TOU_N10_AD6P_47_AB25
IO_L6N_TOU_N11_AD6N_47_AB26
IO_L5P_TOU_N8_AD14P_47_AA27
IO_L5N_TOU_N9_AD14N_47_AB27
IO_L4P_TOU_N6_DBC_AD7P_47_AC26
IO_L4N_TOU_N7_DBC_AD7N_47_AC27
IO_L3P_T0L_N4_AD15P_47_AB24
IO_L3N_T0L_N5_AD15N_47_AC24
IO_L2P_T0L_N2_47_AB25
IO_L2N_T0L_N3_47_AB26
IO_TOU_N12_VRP_47_AA28
IO_L1P_T0L_N0_DBC_47_Y26
IO_L1N_T0L_N1_DBC_47_Y27
VREF_47_V24

V26 FMC1_LA09_P
W26 FMC1_LA09_N
U29 FMC1_LA06_P
V29 FMC1_LA06_N
U26 FMC1_LA04_P
W27 FMC1_LA04_N
Y28 FMC1_LA03_P
U24 FMC1_LA08_P
U25 FMC1_LA08_N
V27 FMC1_LA05_P
V28 FMC1_LA05_N
V21 FMC1_LA11_P
W21 FMC1_LA11_N
T22 FMC1_LA10_P
T23 FMC1_LA10_N
V22 FMC1_LA07_P
V23 FMC1_LA07_N
U21 FMC1_LA14_P
U22 FMC1_LA14_N
W25 FMC1_LA01_CC_P
Y25 FMC1_LA01_CC_N
Y21 FMC1_LA00_CC_N
W23 FMC1_LA00_CC_P
W24 FMC1_LA00_CC_N
AA24 FMC1_CLK0_M2C_P
AA25 FMC1_CLK0_M2C_N
Y22 NC

FMC1_LA16_P

FMC1_LA16_N

FMC1_LA13_P

FMC1_LA13_N

FMC1_LA12_P

FMC1_LA12_N

FMC1_LA02_P

FMC1_LA02_N

FMC1_LA15_P

FMC1_LA15_N

RX12_P

RX12_N

AC26

TX12_P

TX12_N

AC27

RX13_P

RX13_N

AC24

TX13_P

TX13_N

AD25

TX13_P

TX13_N

AD26

TX13_N

AA28

VRP_47

Y26 NC

Y27 NC

V24 FMC1_VREF_A_M2C

VREF_47_V24

VCCO_47_T21
VCCO_47_U28
VCCO_47_V25
VCCO_47_W22
VCCO_47_AA26
VCCO_47_AB23
VCCO_47_AC20

U1

SOC_IRONWOOD_FF1156

FMC1_VREF
FMC1_CLK
FMC1_CLK

240 100nF
GND GND

P1V8

VCCO_48_W32
VCCO_48_Y29
VCCO_48_AB33
VCCO_48_AC30
VCCO_48_AD27
VCCO_48_AE34
VCCO_48_AF31

U1

SOC_IRONWOOD_FF1156

FMC1_LA

AMC_P2P

FPGA_XCKU040FFVA1156



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FPGA Banks 47 48 HP FM

SIZE DWG NO

A3

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G.K.

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of

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29

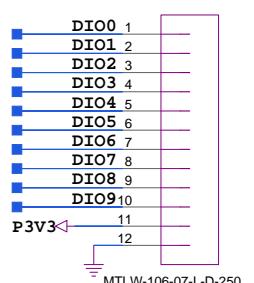
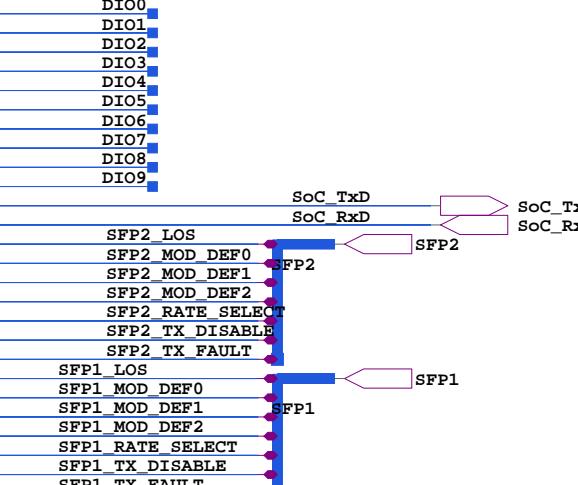
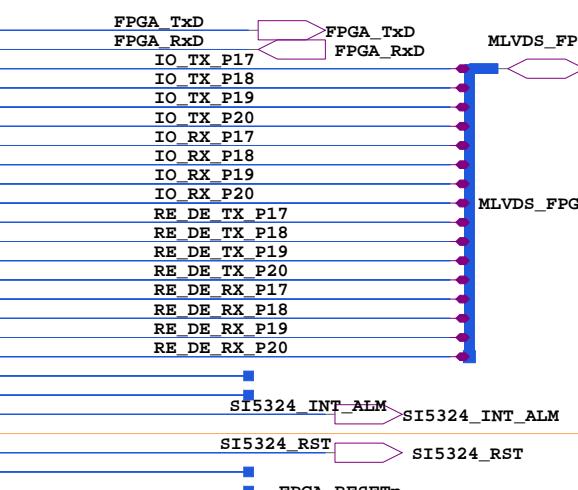
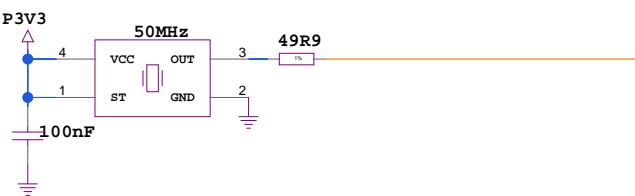
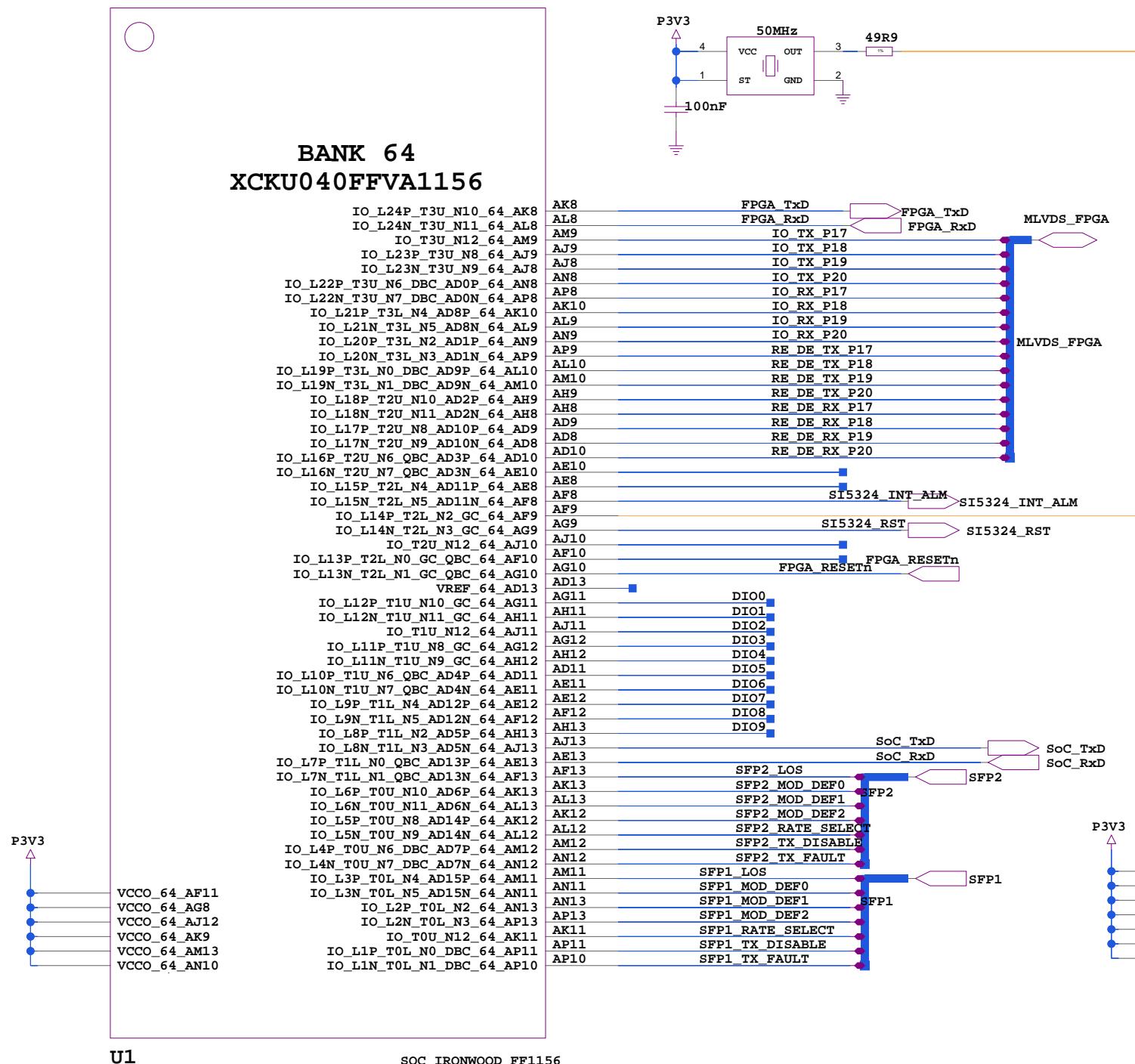
REV

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Bank 64 HR

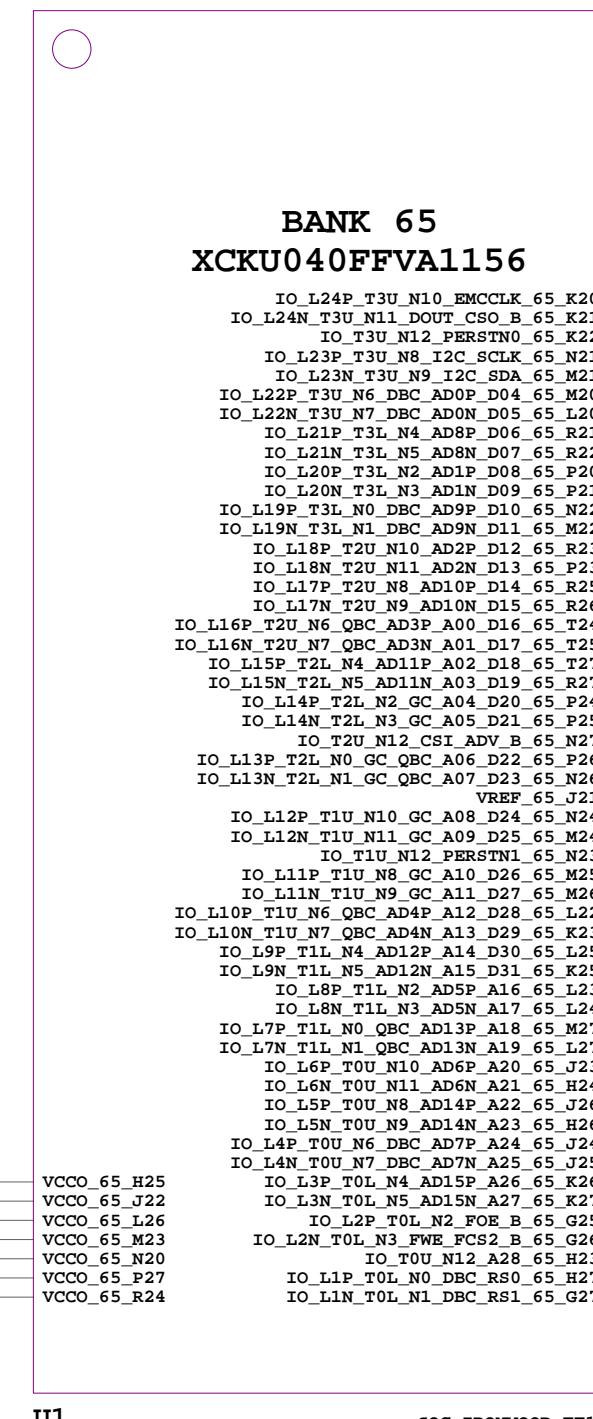
SOC_KU040_FFVA1156_IRON_REV0



MTLW-106-07-L-D-250

Bank 65 HR

SOC_KU040_FFVA1156_IRON_REV0



TITLE

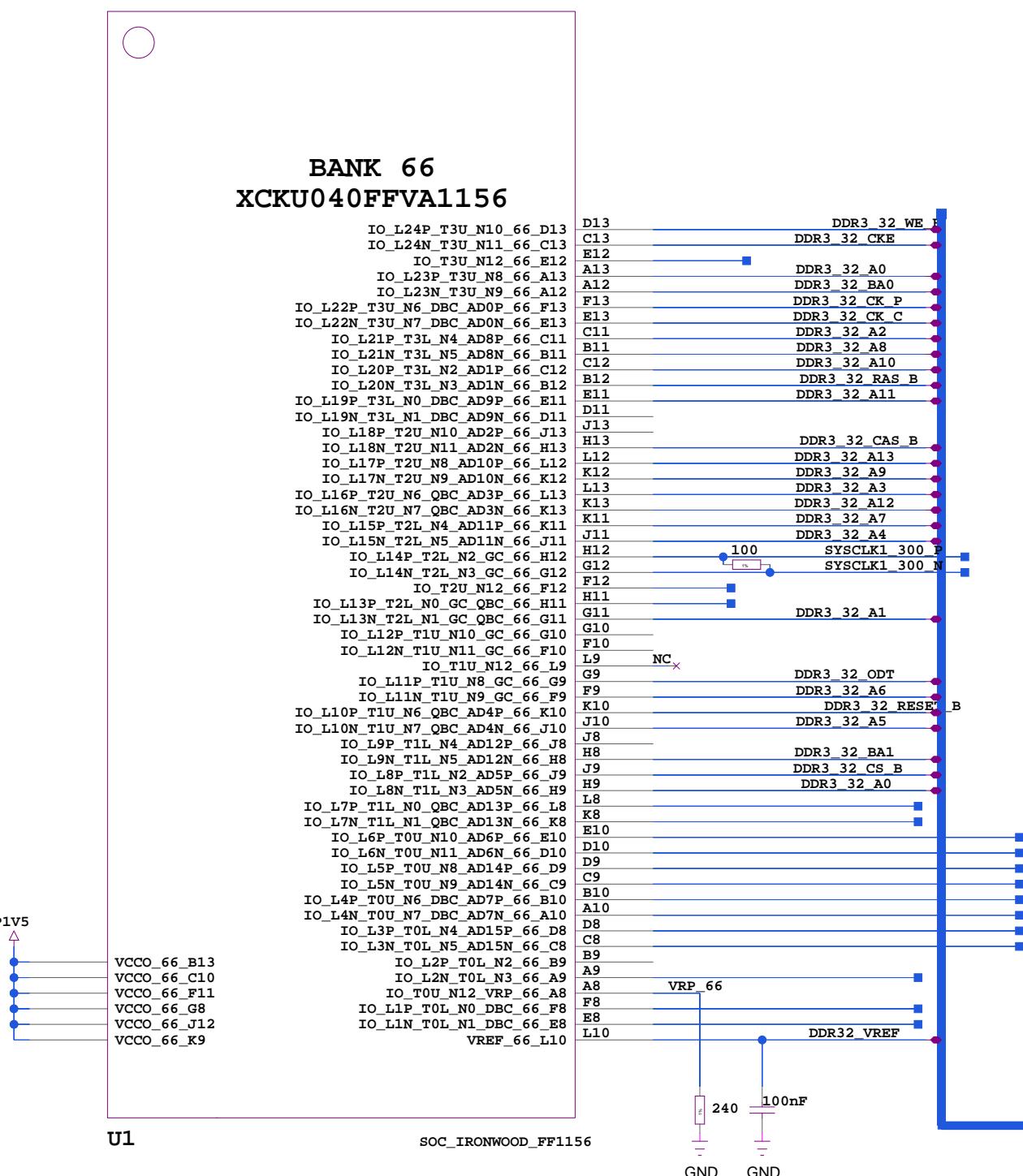


ARTIQ Sayma

Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

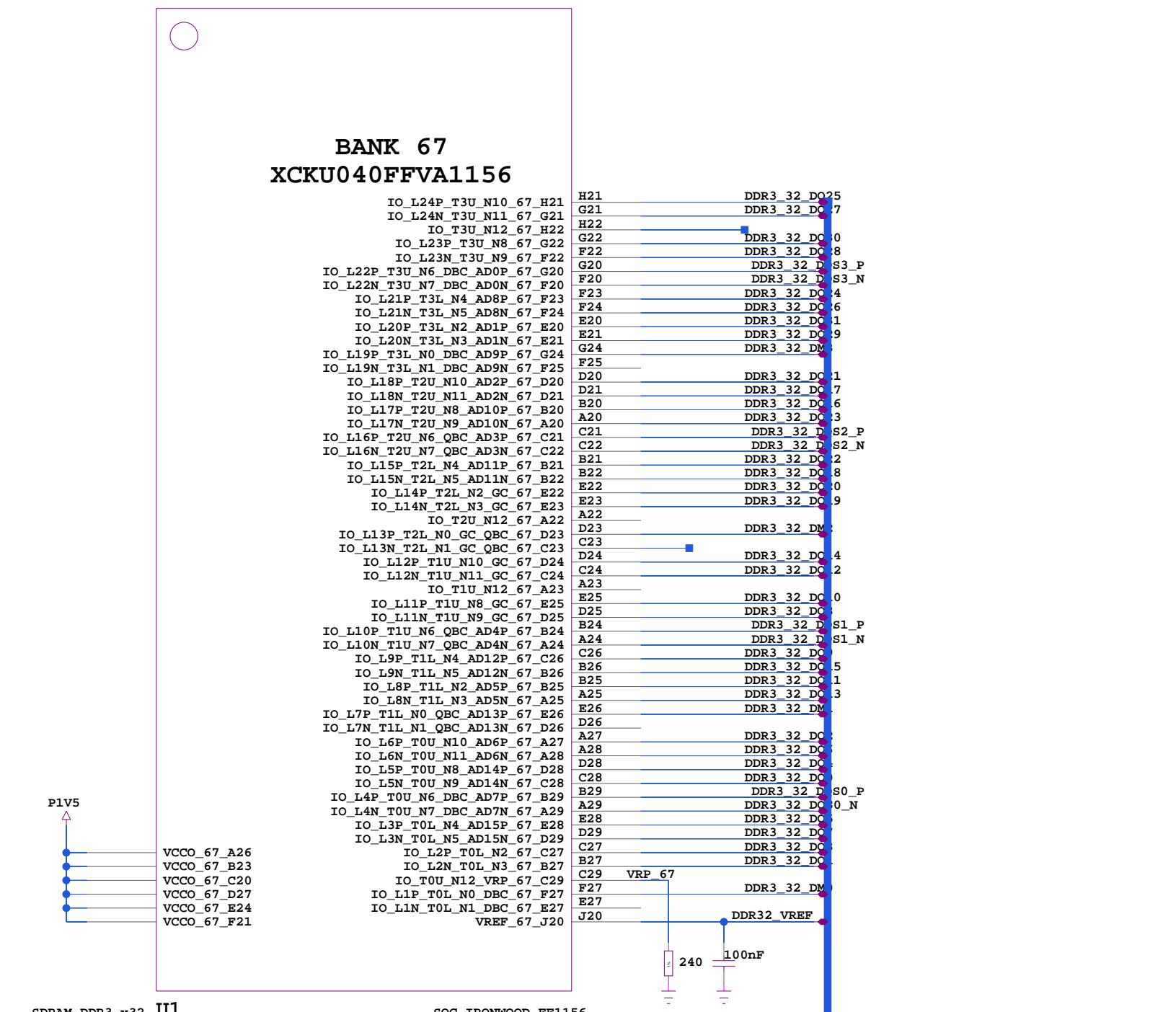
Bank 66 HP

SOC_KU040_FFVA1156_IRON_REV0



Bank 67 HP

SOC_KU040_FFVA1156_IRON_REV0



FPGA Banks 66 67 DDR32

FPGA_XCKU040FFVA1156



ARTIQ Sayma

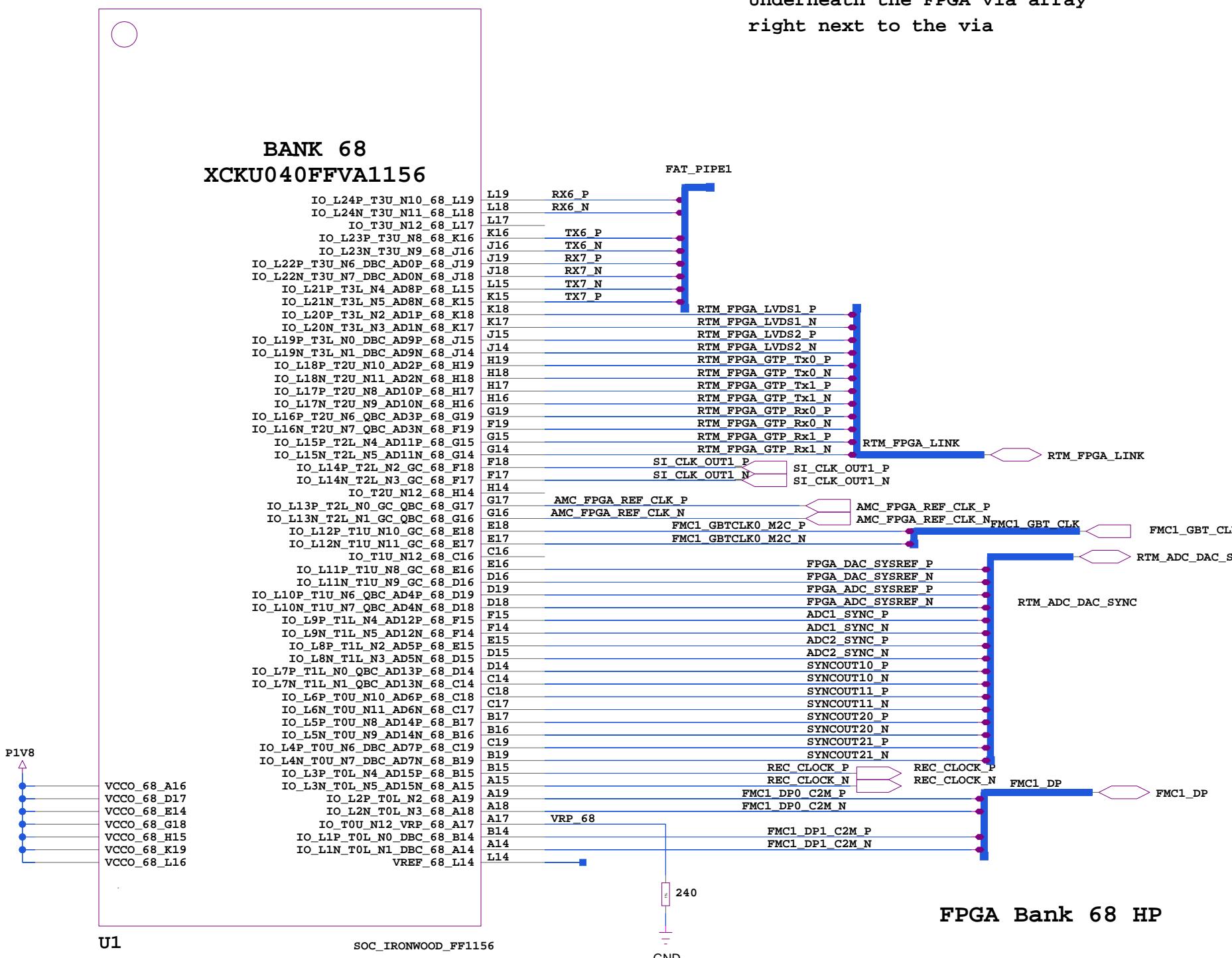
FPGA Banks 66 67 DDR32

SIZE	DWG NO	REV	
A3			v0.9
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G.K.		6	29

2016/11/03:23:13:55

Bank 68 HP

SOC_KU040_FFVA1156_IRON_REV0



Layout: Place resistor and capacitor for VREF

Underneath the FPGA via array
right next to the via

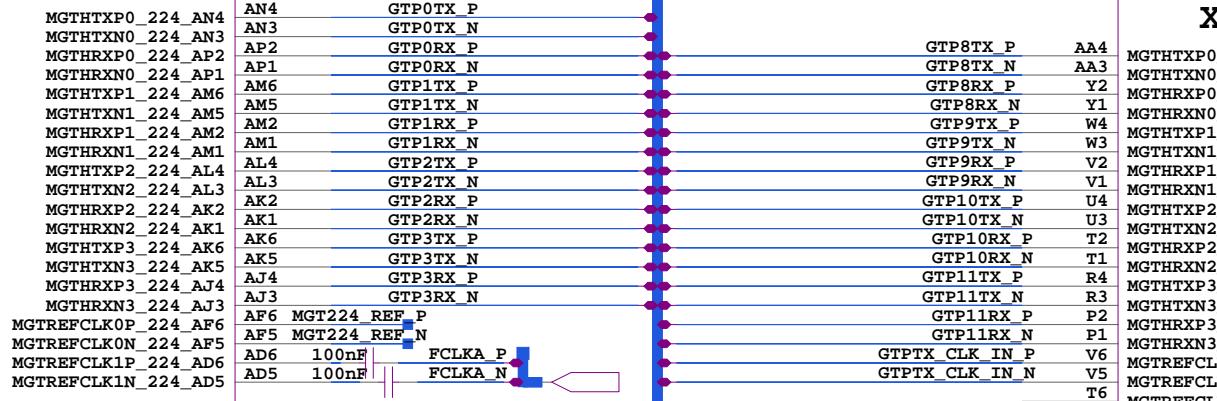
FPGA_XCKU040FFVA1156



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FPGA Bank 68 HP

BANK 224
XCKU040FFVA1156

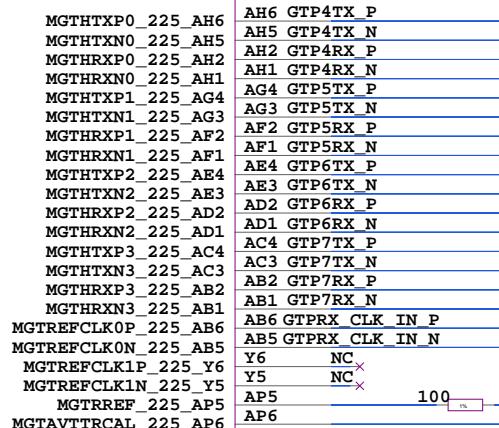


U1

SOC_IRONWOOD_FF1156

SOC_KU040_FFVA1156_IRON_REV0

BANK 225
XCKU040FFVA1156

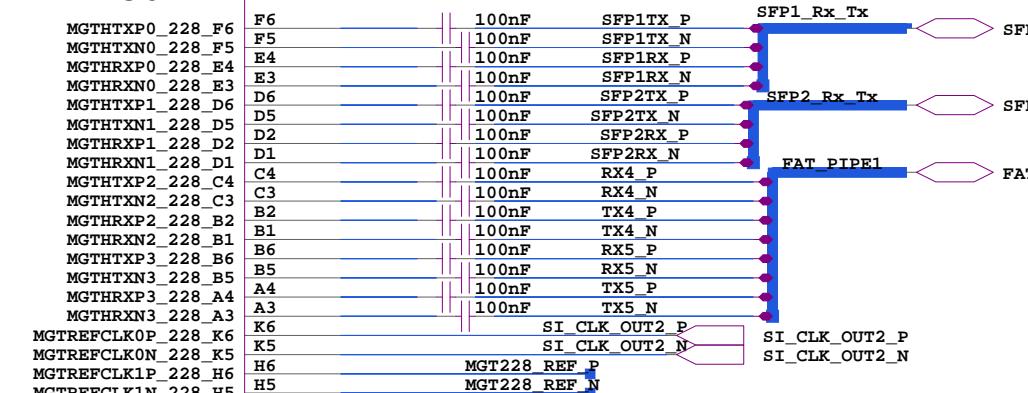


U1

SOC_IRONWOOD_FF1156

SOC_KU040_FFVA1156_IRON_REV0

BANK 228
XCKU040FFVA1156

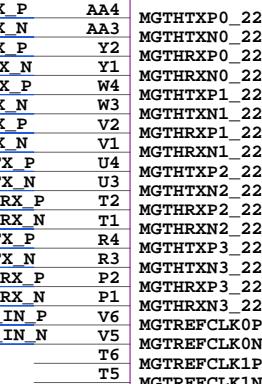


U1

SOC_IRONWOOD_FF1156

SOC_KU040_FFVA1156_IRON_REV0

BANK 226
XCKU040FFVA1156

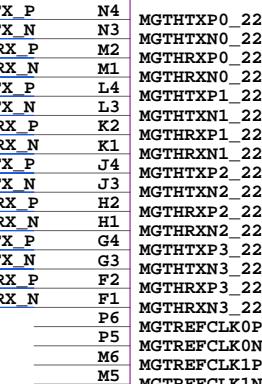


U1

SOC_IRONWOOD_FF1156

SOC_KU040_FFVA1156_IRON_REV0

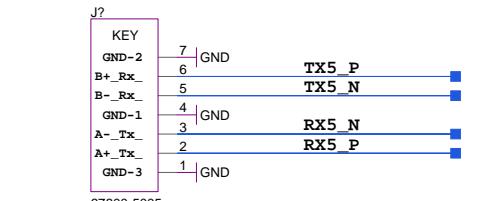
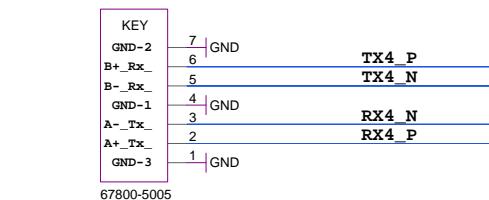
BANK 227
XCKU040FFVA1156



U1

SOC_IRONWOOD_FF1156

SOC_KU040_FFVA1156_IRON_REV0



FPGA_XCKU040FFVA1156



ARTIQ Sayma

FPGA Banks 224 225 226 227 228

SIZE DWG NO
A3
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G.K. 8 29
REV v0.9

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SOC_KU040_FFVA1156_IRON_REV0

SOC_KU040_FFVA1156_IRON_REV0

SOC_KU040_FFVA1156_IRON_REV0

SOC_KU040_FFVA1156_IRON_REV0

BANK MGTAVCC_R
XCKU040FFVA1156

MGTAVCC
AN6
AL6
AJ6
AG6
AE6
AC6
W6
MGTA
R_W6
MGTA
R_U6
MGTA
R_N6
MGTA
R_L6
MGTA
R_J6
G6
MGTA
R_G6
MGTA
R_E6
C6
MGTA
R_C6

U1

SOC_IRONWOOD_FF1156

SOC_KU040_FFVA1156_IRON_REV0

BANK MGTAVTT_R
XCKU040FFVA1156

MGTAVTT
AM3
AL2
AH3
AG2
AD3
AC2
Y3
MGTA
R_Y3
MGTA
R_W2
MGTA
R_T3
R2
M3
L2
H3
G2
D3
C2
MGTA
R_C2

U1

SOC_IRONWOOD_FF1156

SOC_KU040_FFVA1156_IRON_REV0

BANK MGTVCCAUX_R
XCKU040FFVA1156

MGTVCCAUX
AA6
R6

U1

SOC_IRONWOOD_FF1156

BANK MGTAVCC_L
XCKU040FFVA1156

MGTAVCC_L_P29
N31
J31
H29
F30
E31

U1

SOC_IRONWOOD_FF1156

BANK MGTAVTT_L
XCKU040FFVA1156

R32
P33
L32
K33
H33
G32
D33
C32

U1

SOC_IRONWOOD_FF1156

BANK MGTVCCAUX_L
XCKU040FFVA1156

MGTVCCAUX_L_M29
K29

U1

SOC_IRONWOOD_FF1156

BANK VCCAUX
XCKU040FFVA1156

VCCAUX_AC8
VCCAUX_AA8
VCCAUX_W8
VCCAUX_U8

U1

SOC_IRONWOOD_FF1156

BANK VCCAUX_IO
XCKU040FFVA1156

VCCAUX_IO_AC18
AB19
Y19
W20
V19
U20
T19
R20
P19
M19
N18

U1

SOC_IRONWOOD_FF1156

BANK VCCBRAM
XCKU040FFVA1156

VCCBRAM_AA18
AB17
Y17
V17

U1

SOC_IRONWOOD_FF1156

BANK VCCINT
XCKU040FFVA1156

VCCINT_AA16
W16
U16
VCCINT_W16
VCCINT_U16
VCCINT_R16
VCCINT_N16
VCCINT_R8
VCCINT_N8
VCCINT_T17
VCCINT_AC16
VCCINT_AC14
VCCINT_AC12
VCCINT_AC10
VCCINT_AB15
VCCINT_AB13
VCCINT_AB11
VCCINT_AA14
VCCINT_AA12
VCCINT_AA10
VCCINT_Y15
VCCINT_Y13
VCCINT_W14
VCCINT_W10
VCCINT_V15
VCCINT_V13
VCCINT_V1
VCCINT_U14
VCCINT_U10
VCCINT_T15
VCCINT_T13
VCCINT_T11
VCCINT_T9
VCCINT_R14
VCCINT_R12
VCCINT_R10
P15
VCCINT_P15
VCCINT_P13
VCCINT_P11
VCCINT_P1
P9
VCCINT_P9
VCCINT_N14
N12
VCCINT_N12
VCCINT_N10
VCCINT_M15
VCCINT_M13
VCCINT_M11
VCCINT_M9
U1
SOC_KU040_FFVA1156_IRON_REV0

SOC_IRONWOOD_FF1156

BANK VCCINT_IO
XCKU040FFVA1156

VCCINT_IO_W18
U18
R18
P17
M17
U1
SOC_KU040_FFVA1156_IRON_REV0

SOC_IRONWOOD_FF1156

FPGA Power



ARTIQ Sayma

FPGA Power

SIZE DWG NO

A3

DRAWN BY

G.K.

SHEET

of

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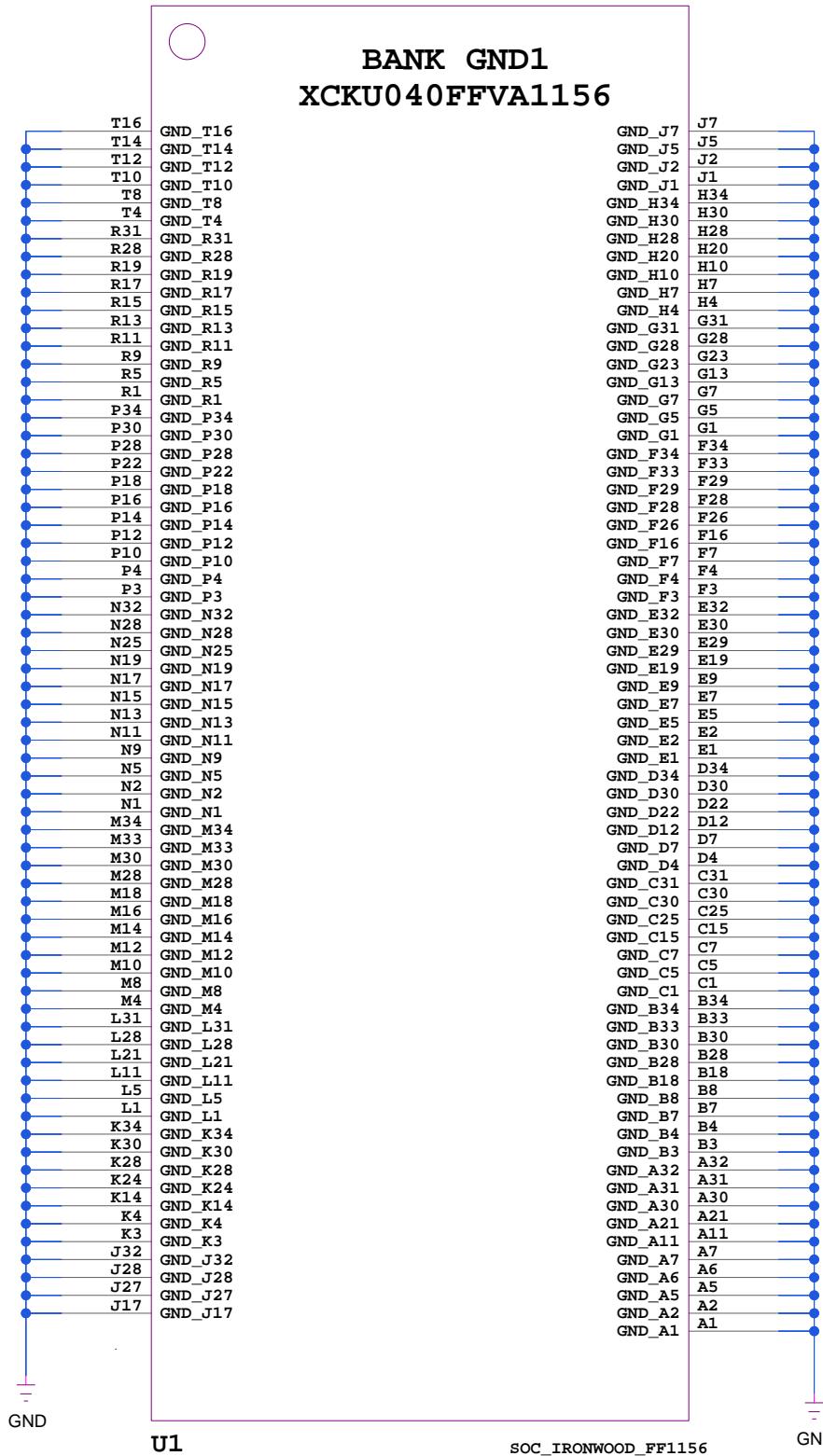
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REV

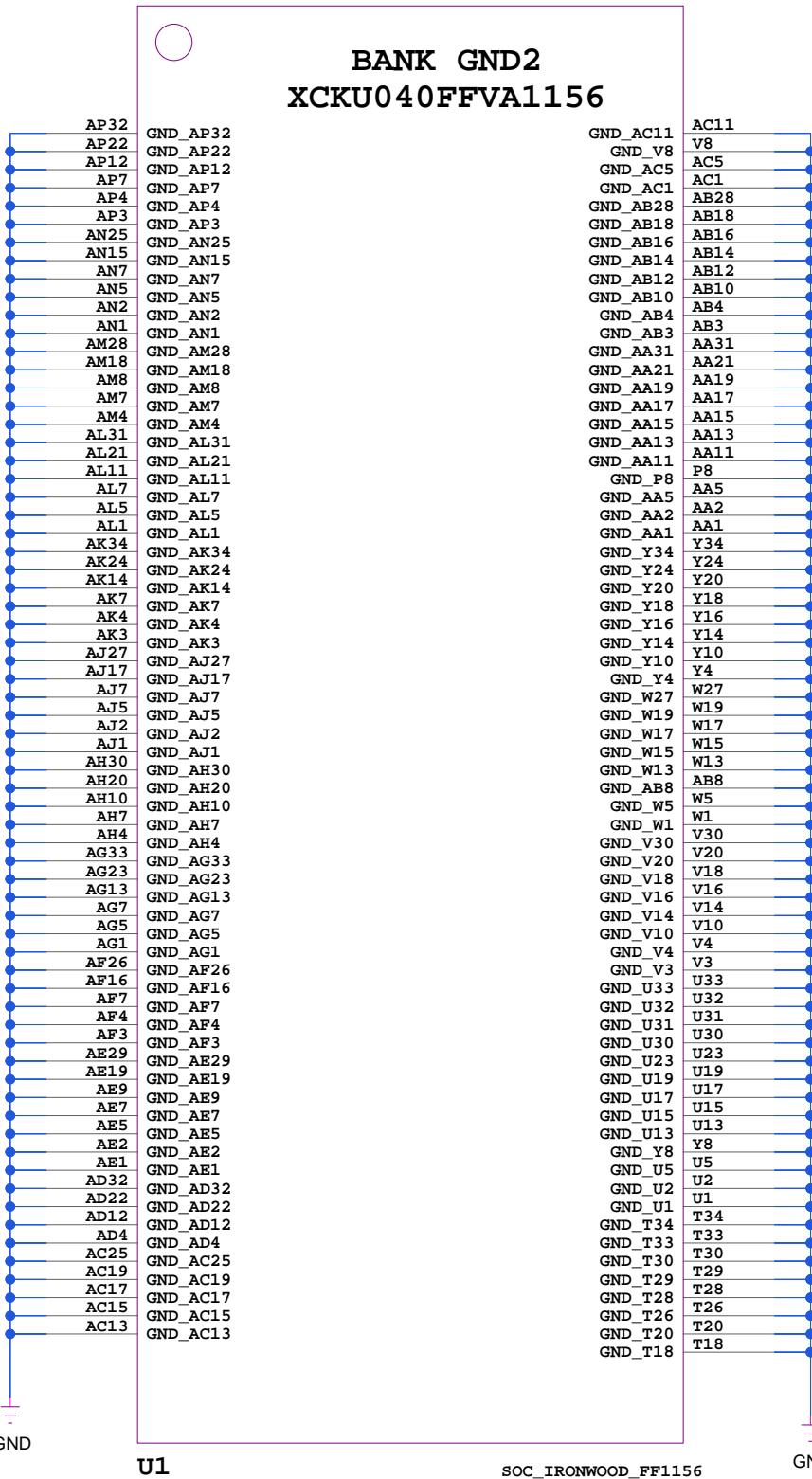
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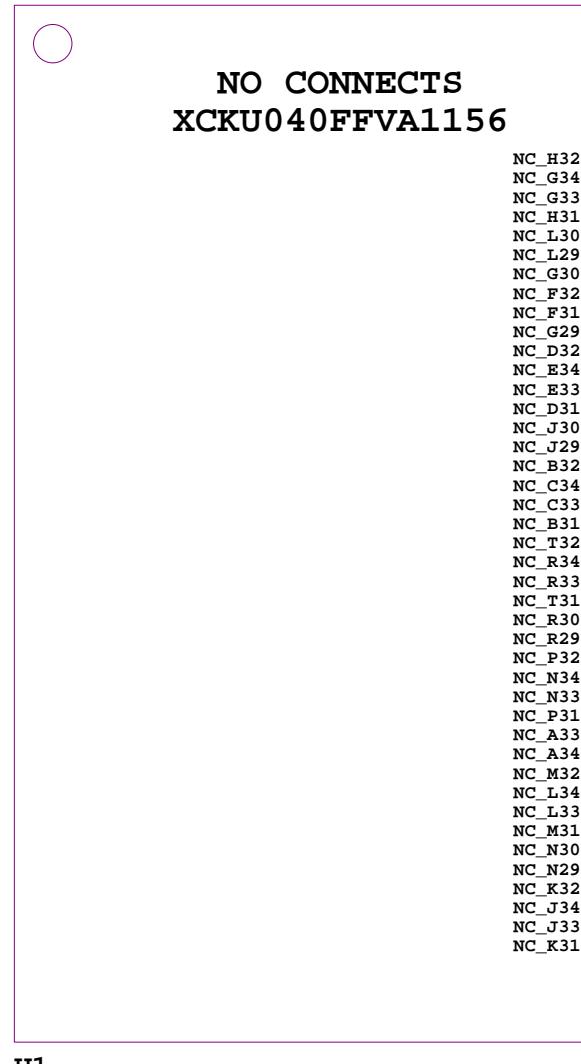
SOC_KU040_FFVA1156_IRON_REV0



SOC_KU040_FFVA1156_IRON_REV0



SOC_KU040_FFVA1156_IRON_REV0



NC_H32	NC
NC_G34	NC
NC_G33	NC
NC_H31	NC
NC_L30	NC
NC_L29	NC
NC_G30	NC
NC_F32	NC
NC_F31	NC
NC_G29	NC
NC_D32	NC
NC_E34	NC
NC_E33	NC
NC_D31	NC
NC_J30	NC
NC_J29	NC
NC_B32	NC
NC_C34	NC
NC_C33	NC
NC_B31	NC
NC_T32	NC
NC_R34	NC
NC_R33	NC
NC_T31	NC
NC_R30	NC
NC_R29	NC
NC_P32	NC
NC_N34	NC
NC_N33	NC
NC_P31	NC
NC_A33	NC
NC_A34	NC
NC_M32	NC
NC_L34	NC
NC_L33	NC
NC_M31	NC
NC_N30	NC
NC_N29	NC
NC_K32	NC
NC_J34	NC
NC_J33	NC
NC_K31	NC



ARTIQ Sayma

FPGA_XCKU040FFVA1156 FPGA GND NC

SIZE DWG NO

A3

DRAWN BY

G.K.

SHEET

of

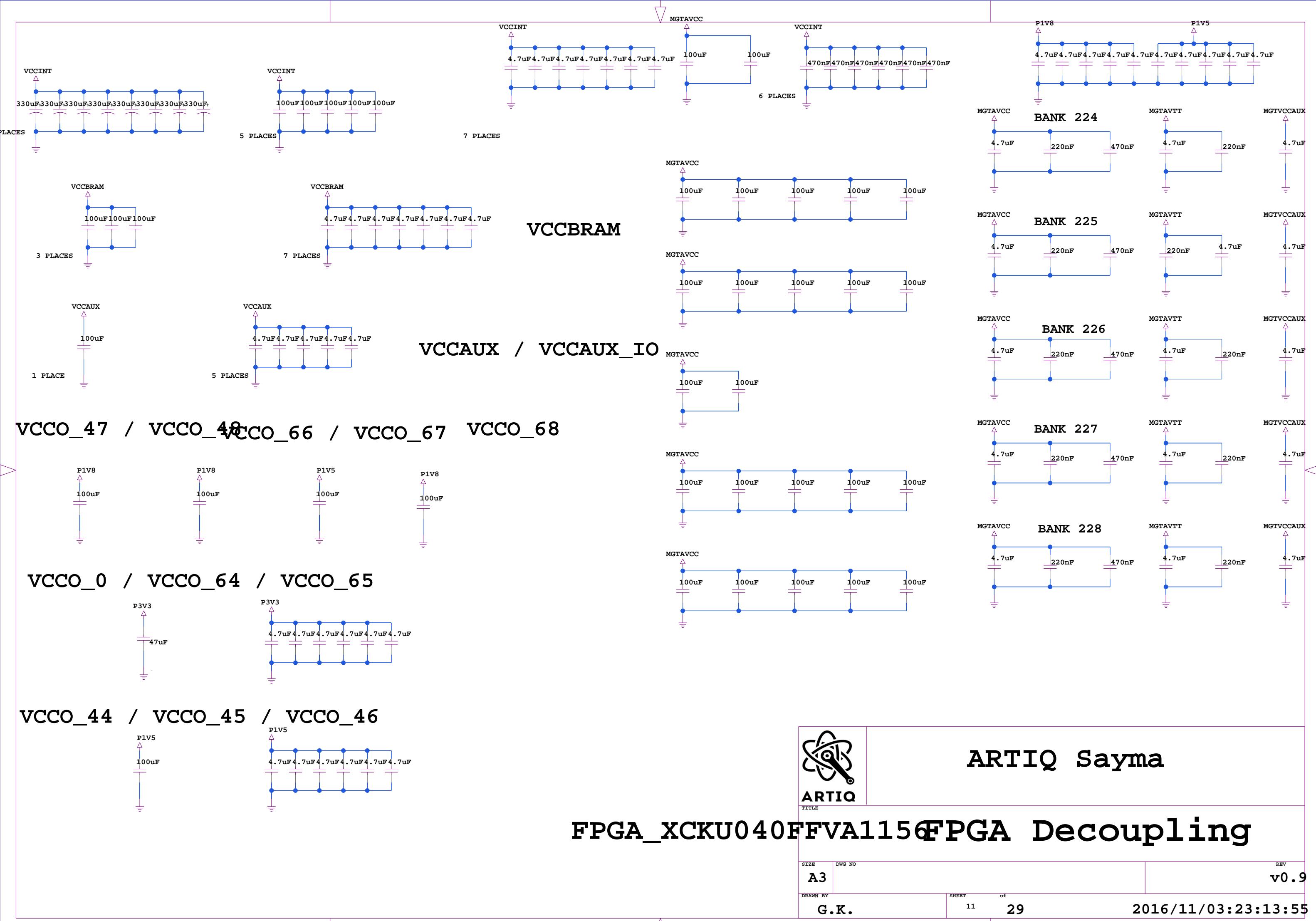
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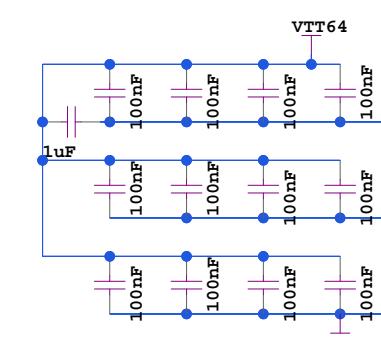
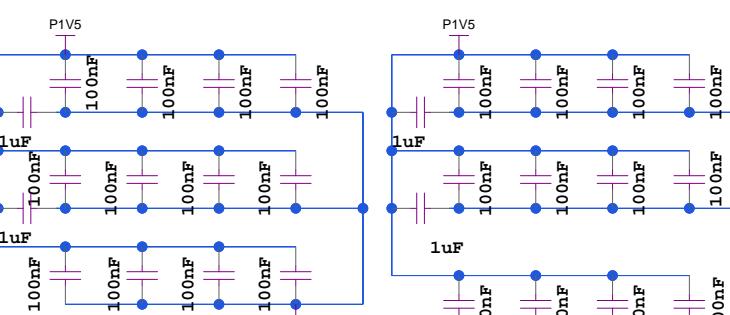
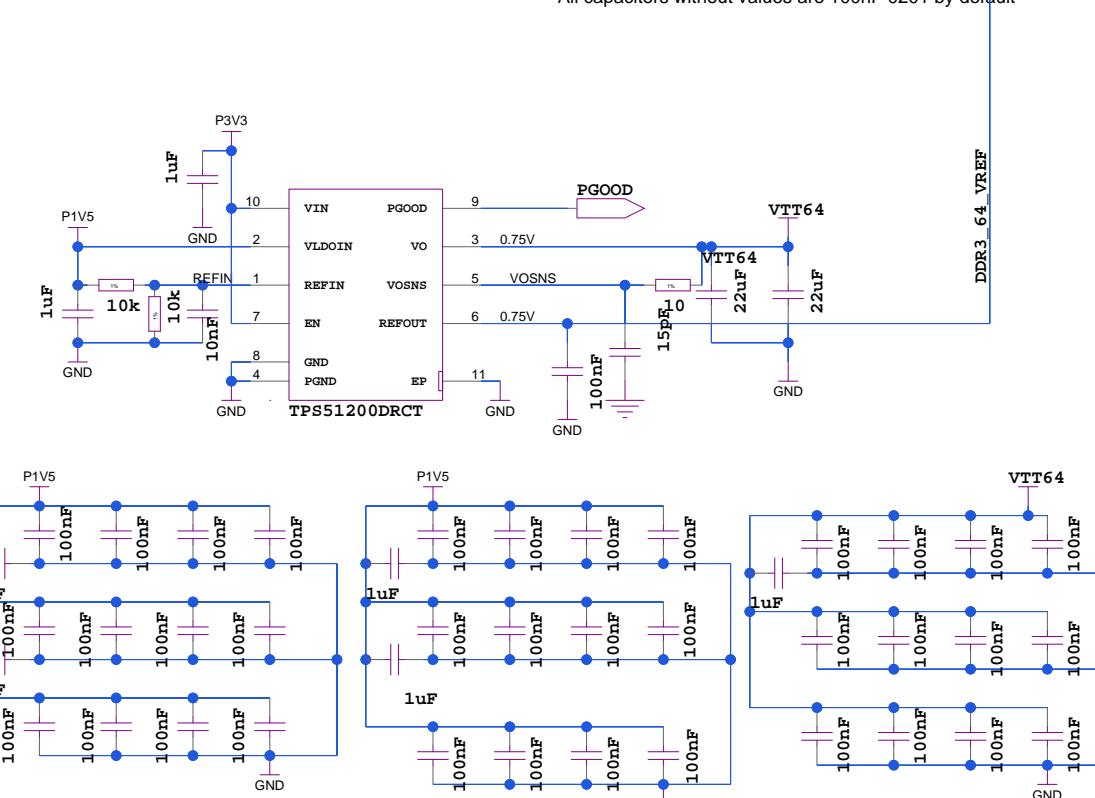
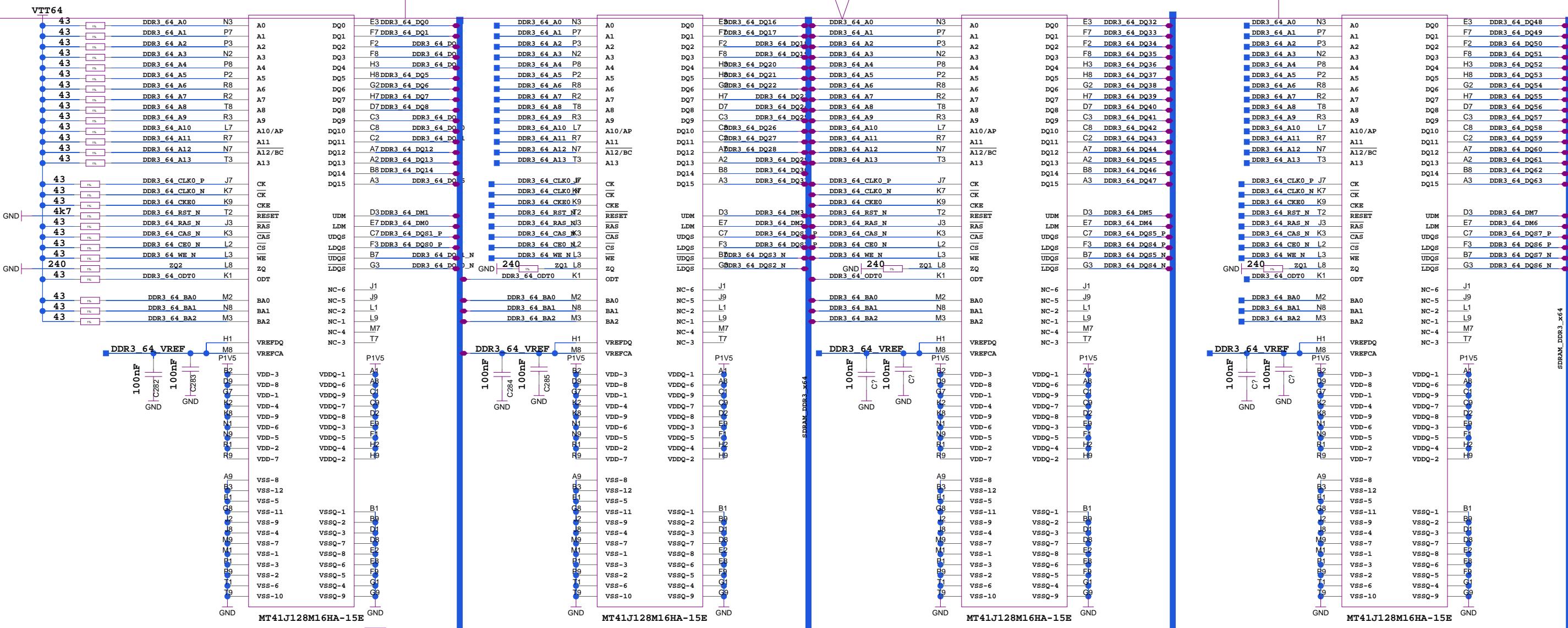
REV

v0.9

10

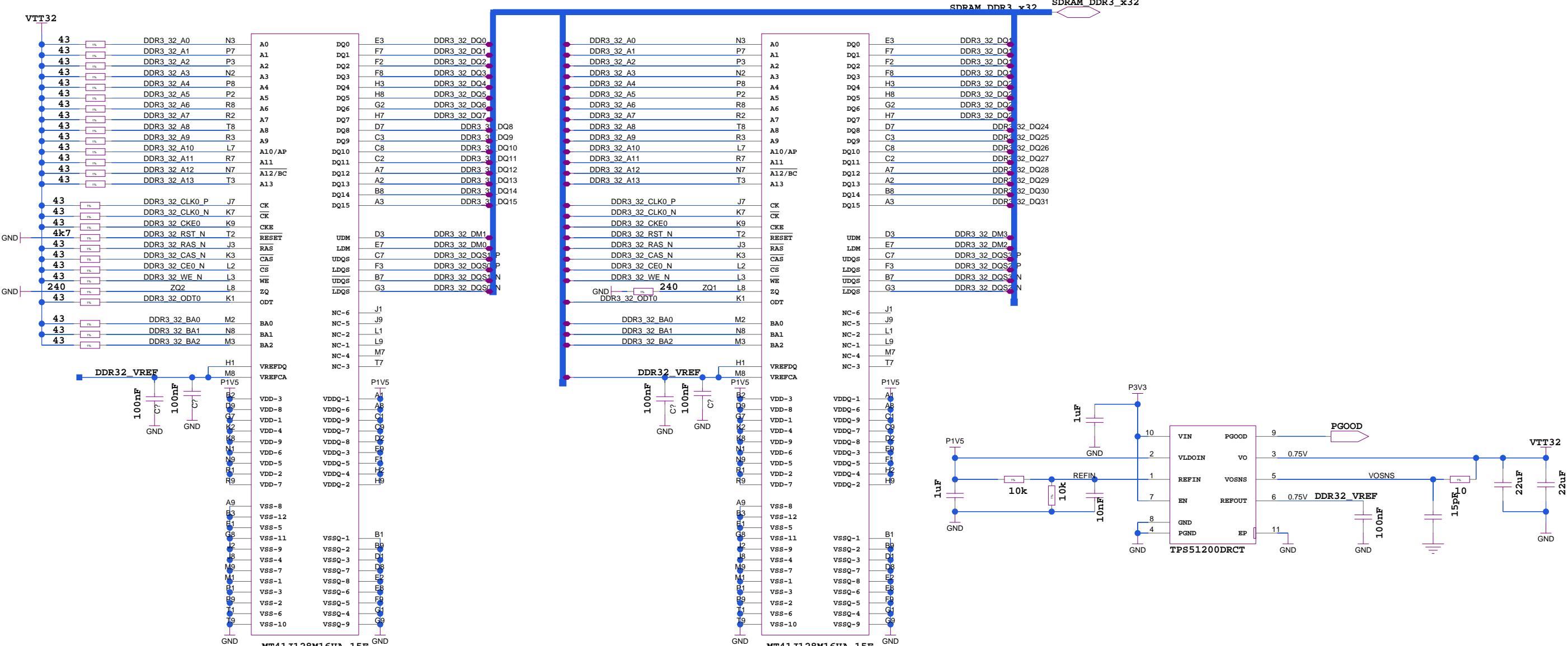
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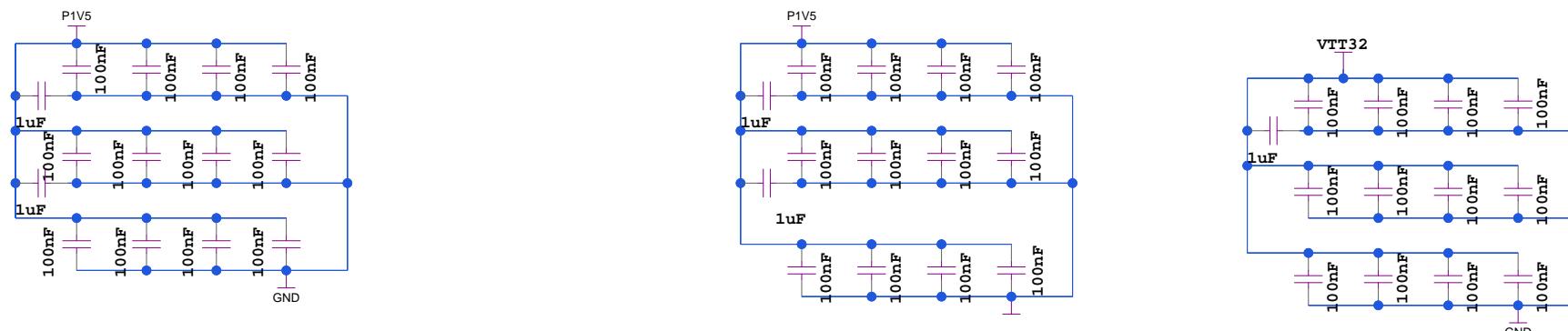


ARTIQ Sayma

SDRAM_DDR3_4x16



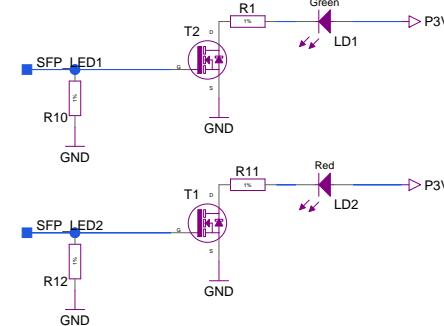
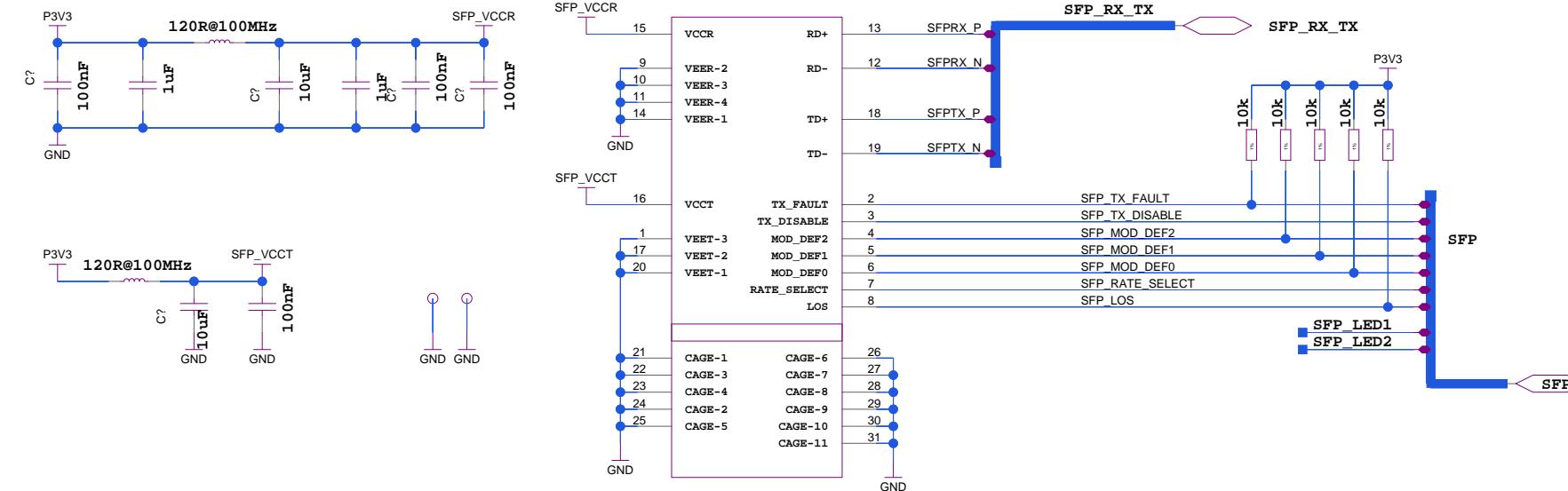
All capacitors without values are 100nF 0201 by default



ARTIQ Sayma

SDRAM DDR3 2x16

SIZE	DWG NO
A3	
DRAWN BY	
G.K.	

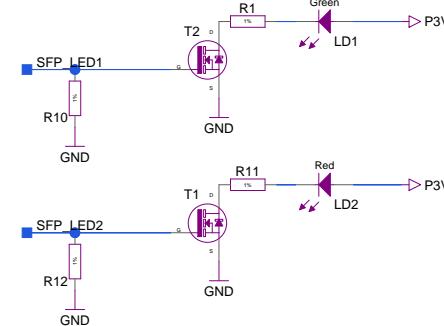
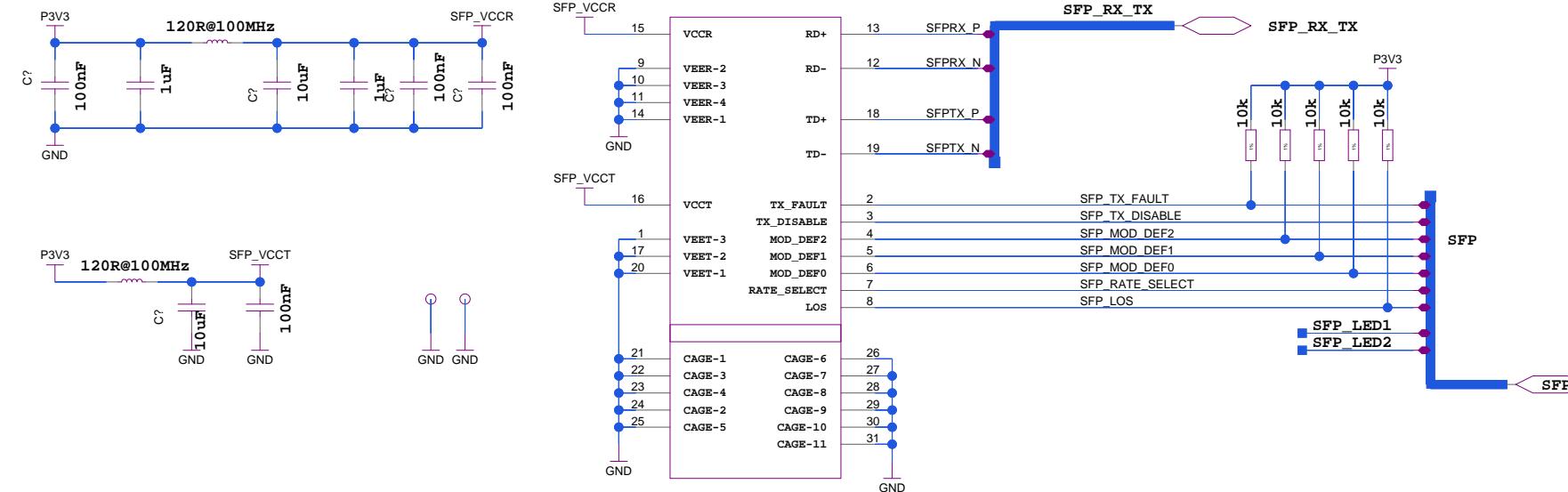


ARTIQ Sayma

SFP

SIZE	DWG NO	REV
A3	SFP	v0.9
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G.K.	14	29

2016/11/03:23:14:00

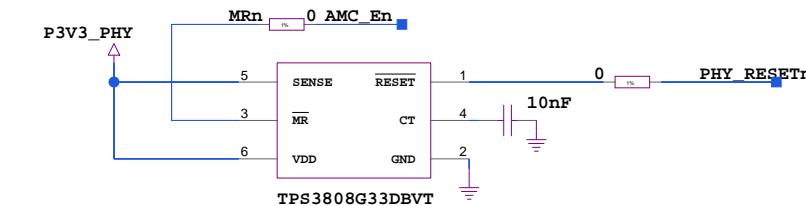


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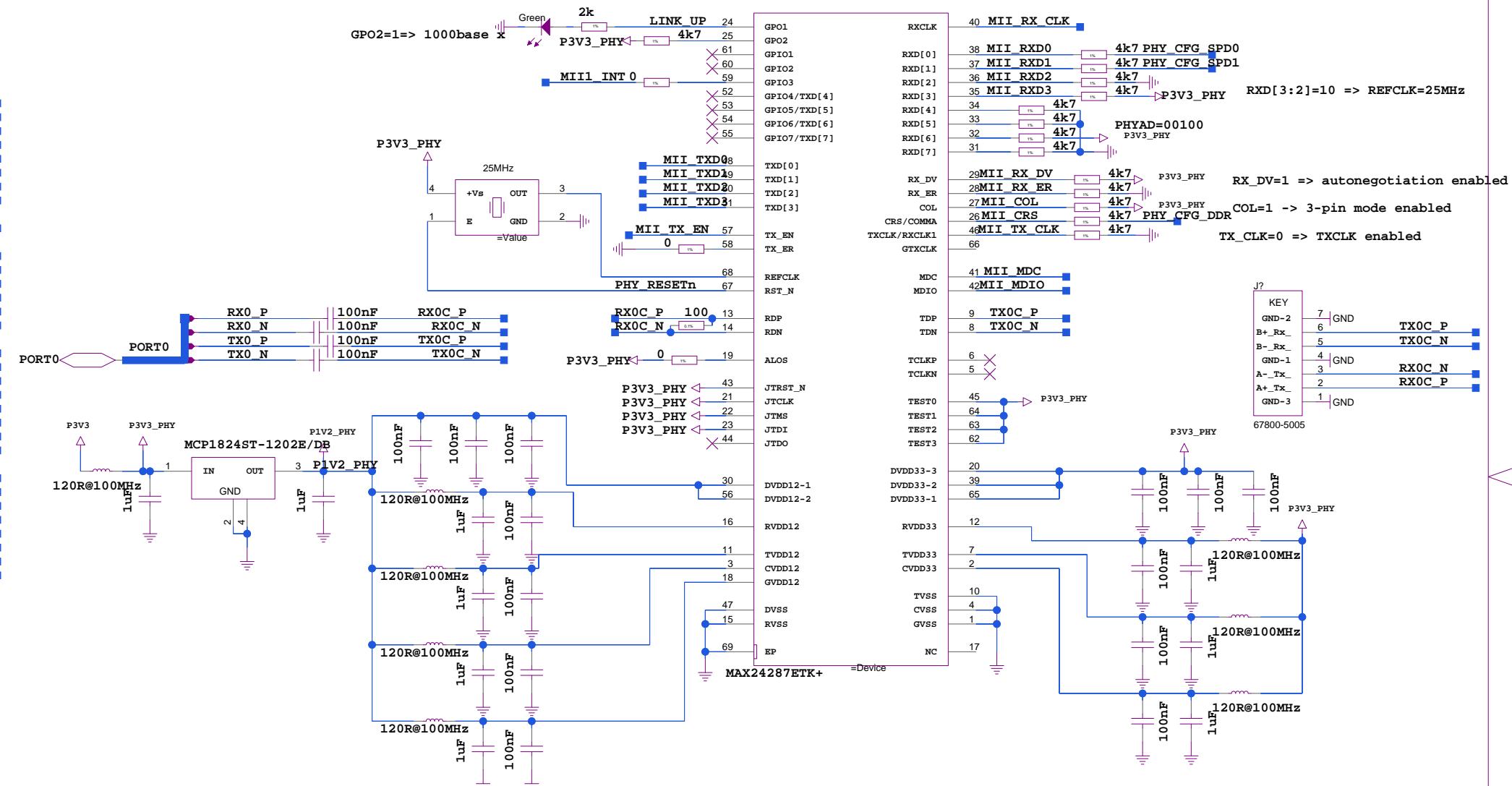
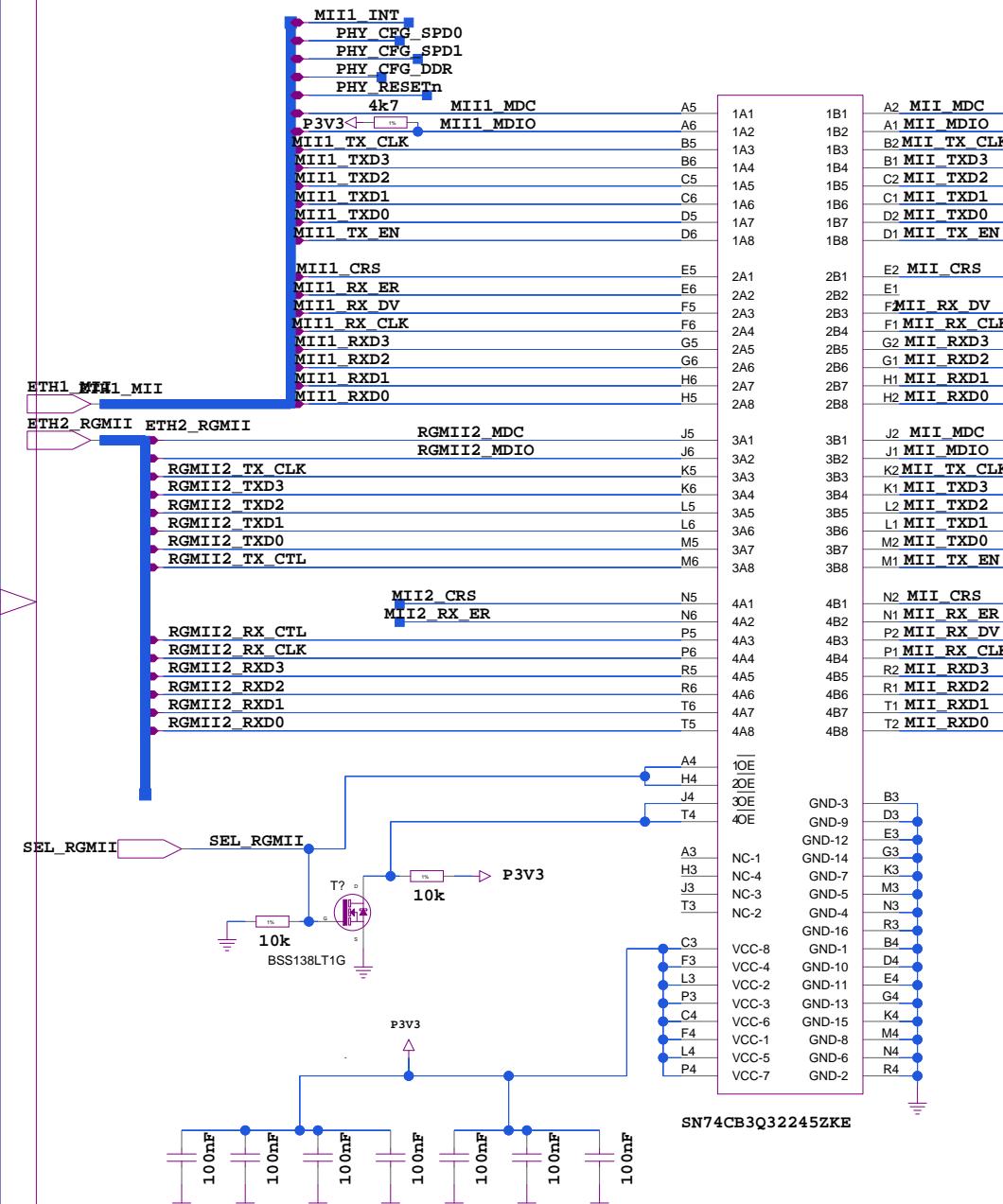
SFP

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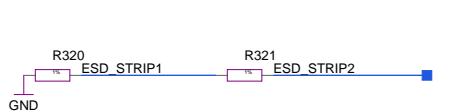
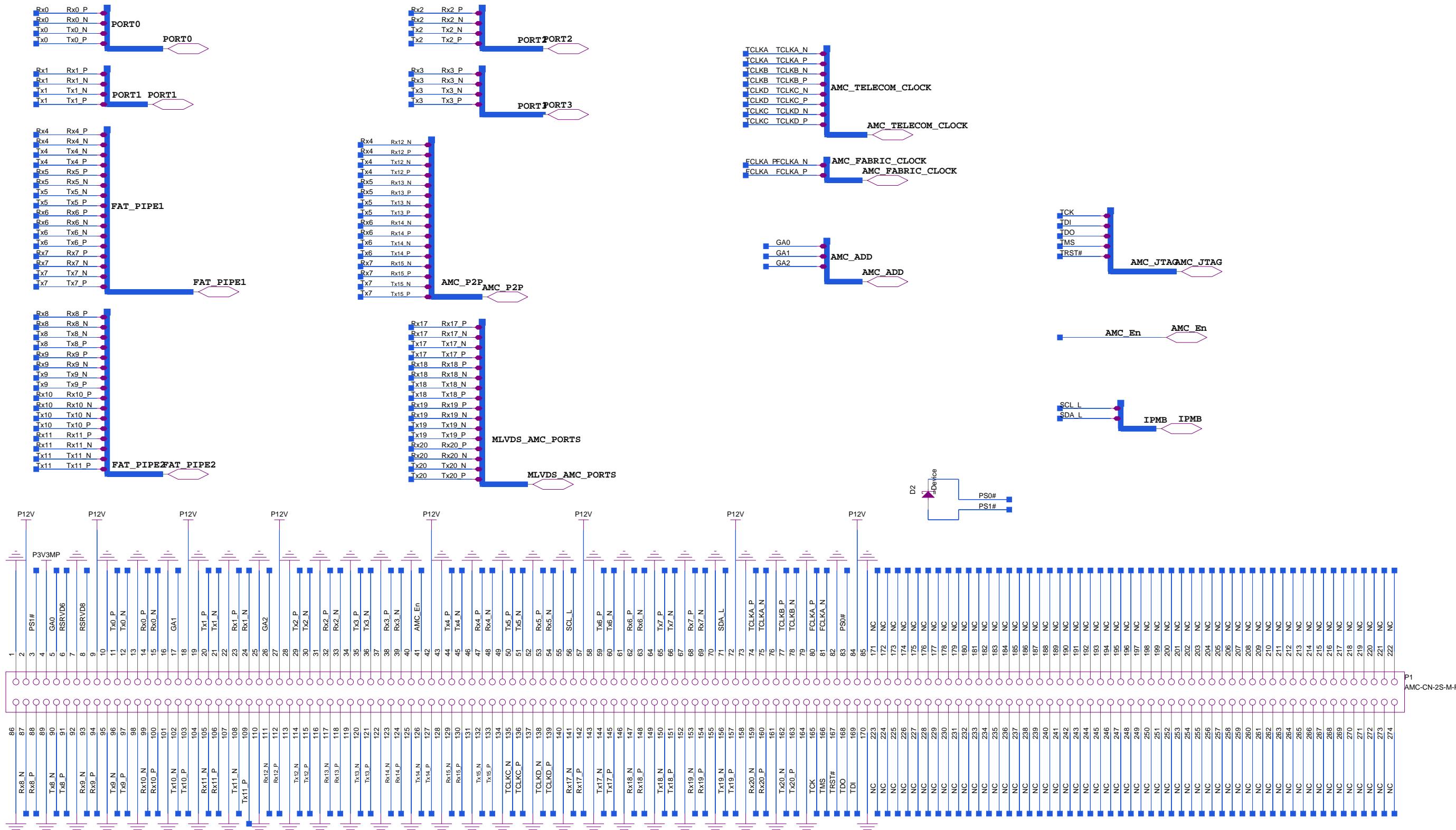
We want to have:
 SPD[1:0] DDR
 01 0 in MII
 10 1 in RGMII-1000



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ETH_PHY_RMII_MII

SIZE	DWG NO	REV
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DRAWN BY	SHEET of	
G.K.	16	29



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AMC_Connector

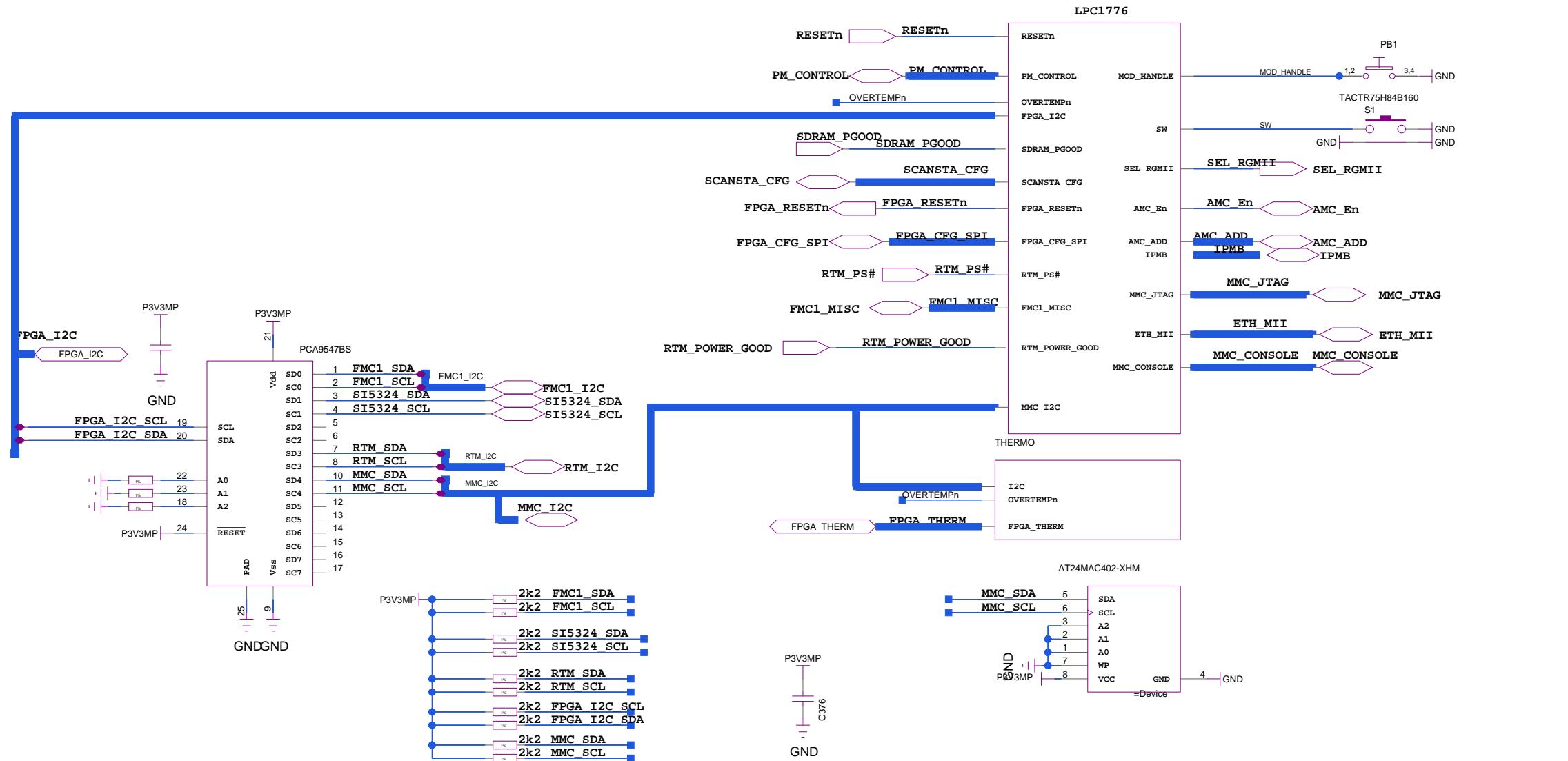
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<http://ohwr.org/CERNOHL>. This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

- Dimensions are in MM, nominal values used
- Component height rule derived from AMC Base Specification.PDF, Page 62
- The two corners of outline near the edge-connector are approximated, see AMC Base Specification.PDF, Page 59
- Stackup is not specified in AMC Base Specification.PDF or implemented in this template.

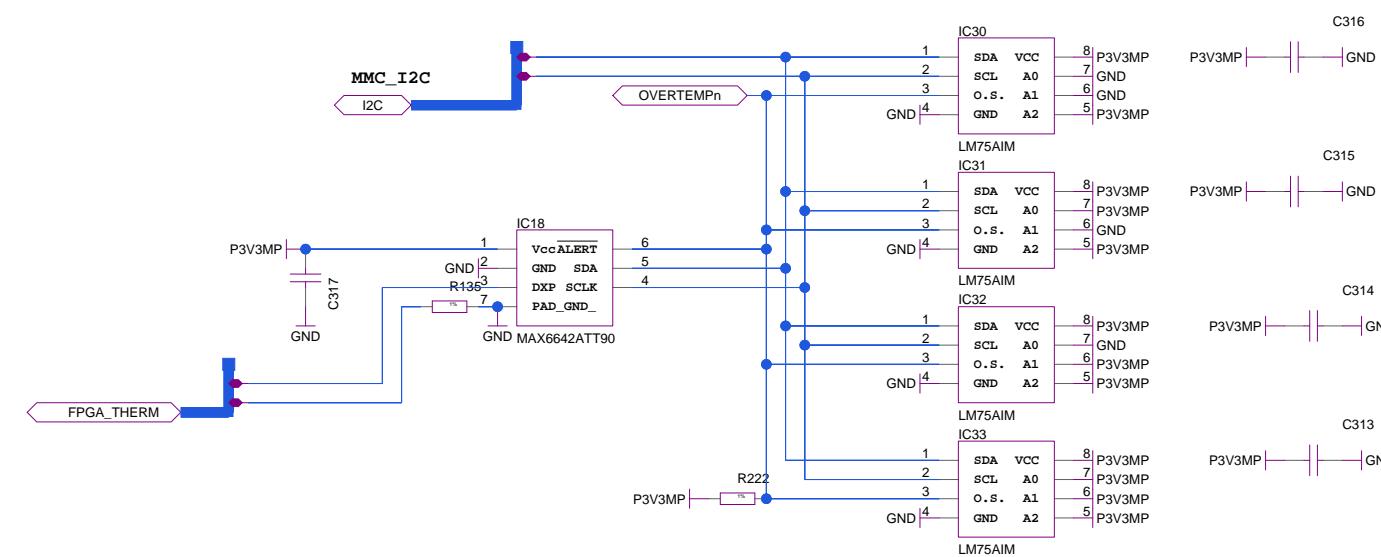
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IPMI

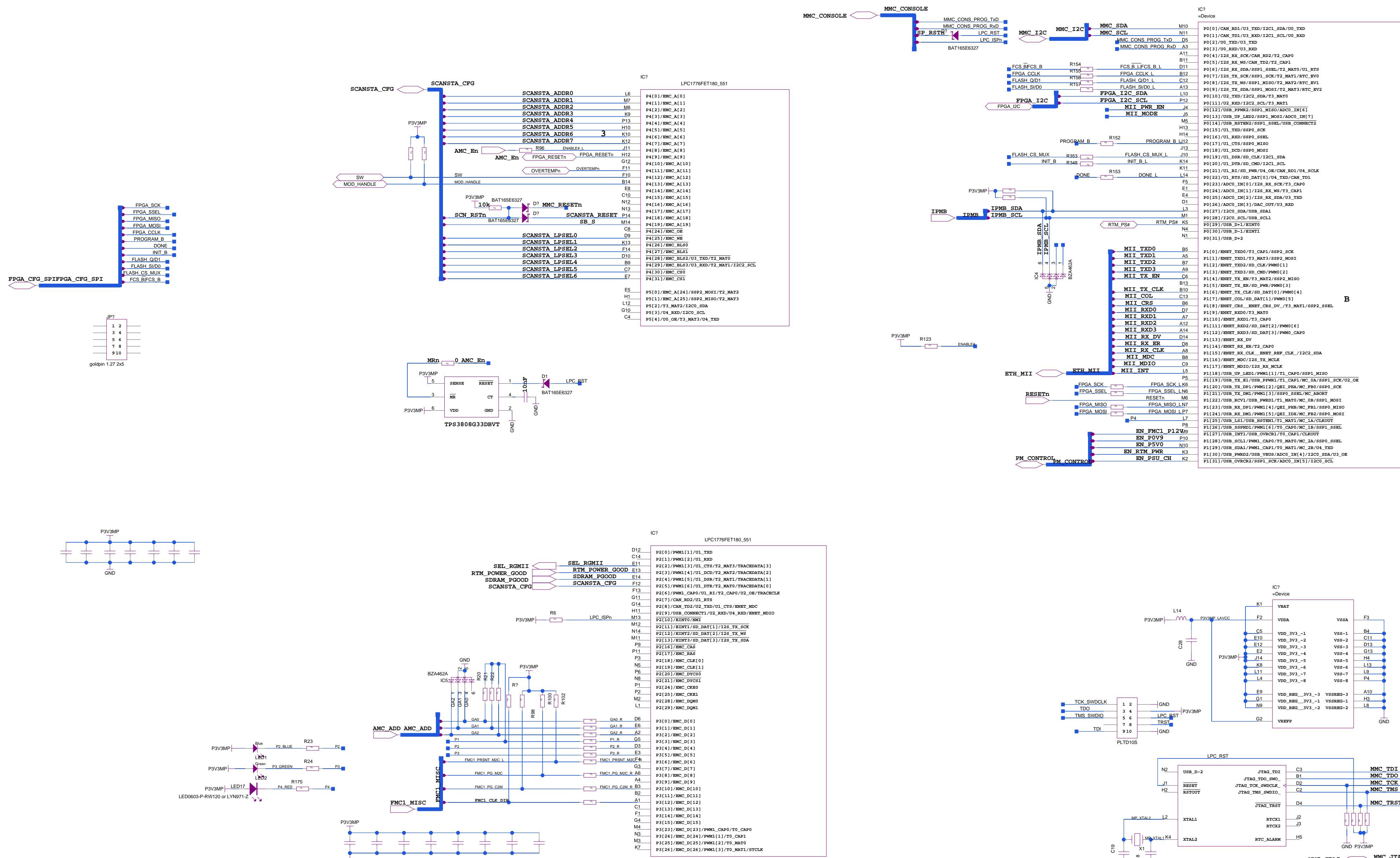
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DRAWN BY	G.K.	SHEET	18	29	OF
					2016/11/03:23:13:55



ARTIQ Sayma

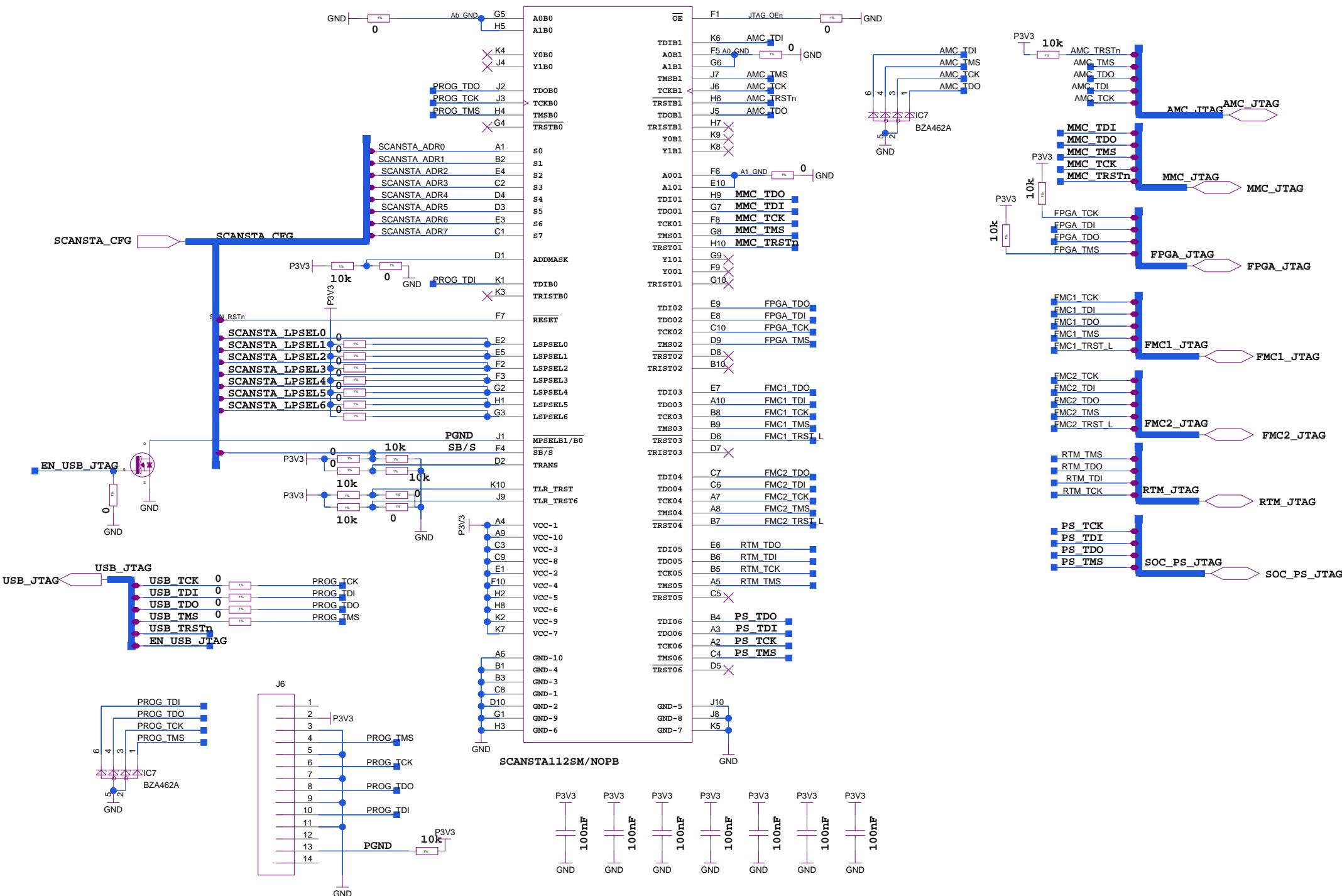
Thermometers

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2016/11/03:23:13:56		



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CPU_LPC1776



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JTAG_Configuration

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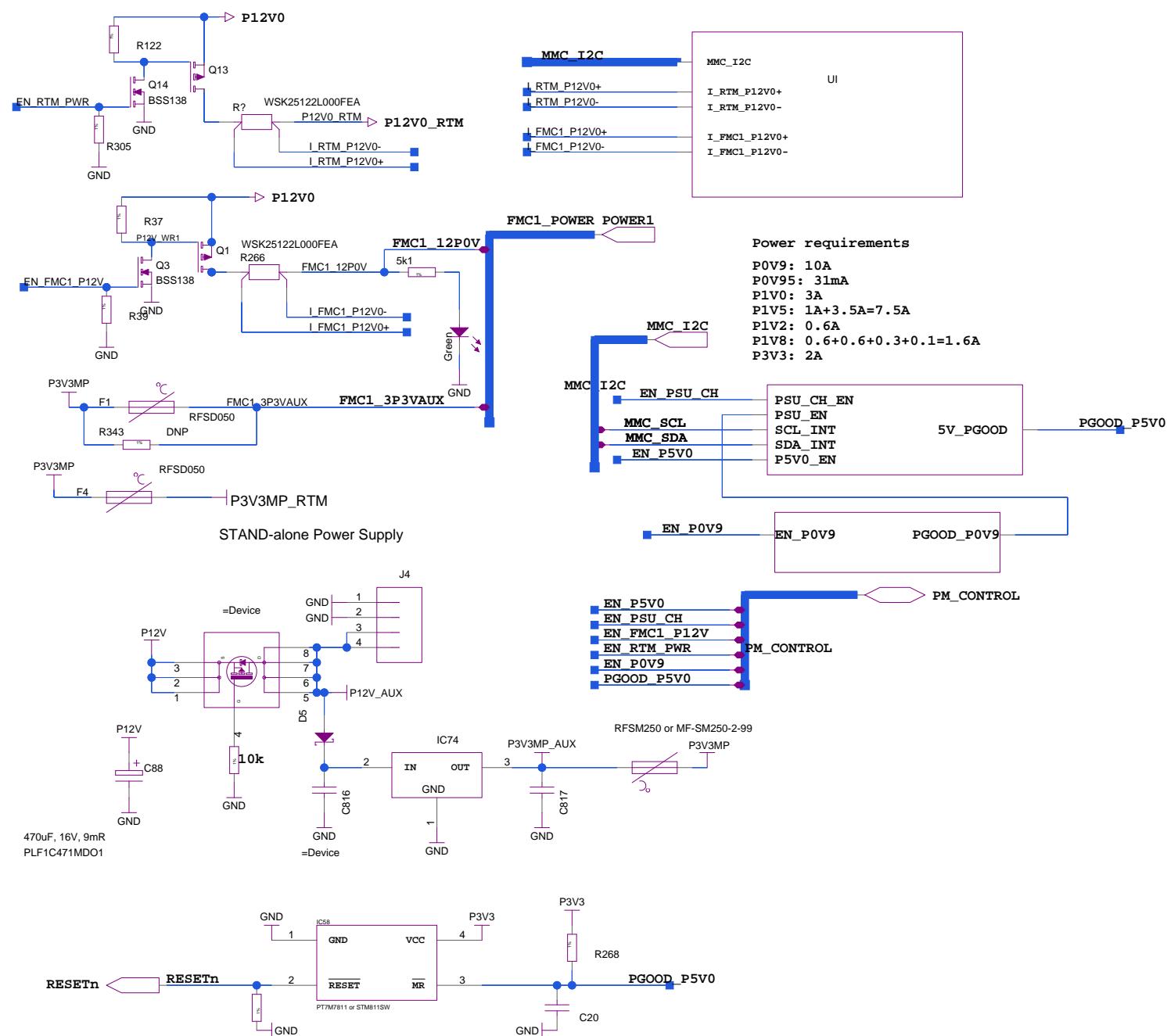


Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V _{CCINT}	Internal supply voltage	0.922	0.950	0.979	V
V _{CCINT}	For -1L (0.90V) devices: internal supply voltage	0.880	0.900	0.920	V
V _{CCINT}	For -3 (1.0V only) devices: internal supply voltage	0.970	1.000	1.030	V
V _{CCBRAM}	Internal supply voltage for the I/O banks	0.922	0.950	0.979	V
V _{CCBRAM}	For -1L (0.90V) devices: internal supply voltage for the I/O banks	0.880	0.900	0.920	V
V _{CCCAUX}	Block RAM supply voltage	0.922	0.950	0.979	V
V _{CCCAUX}	For -1L (0.90V) devices: block RAM supply voltage	0.970	1.000	1.030	V
V _{CCO}	Auxiliary supply voltage	1.746	1.800	1.854	V
V _{CCO}	Supply voltage for HR I/O banks	1.140	-	3.400	V
V _{CCO}	Supply voltage for HP I/O banks	0.950	-	1.890	V
V _{CCO}	Auxiliary I/O supply voltage	1.746	1.800	1.854	V
V _{IN}	I/O input voltage	-0.200	-	V _{CCO} + 0.200	V
V _{IN}	I/O input voltage when V _{CCO} = 3.3V for V _{REF} and differential I/O standards except TMDS_33 ⁽³⁾	-	0.400	2.625	V
I _H	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	-	-	10.000	mA
V _{BATT}	Battery voltage	1.000	-	1.890	V
GTH and GTY Transceivers					
V _{MGTAVCC}	Analog supply voltage for the GTH and GTY transceivers ⁽¹⁰⁾	0.970	1.000	1.030	V
V _{MGTAVTT}	Analog supply voltage for the GTH and GTY transmitter and receiver termination circuits	1.170	1.200	1.230	V
V _{MGTVAUX}	Auxiliary analog QPLL voltage supply for the transceivers	1.750	1.800	1.850	V

Power-On/Off Power Supply Sequencing

The recommended power on sequence is V_{CCINT}/V_{CCINT}_IO/V_{CCBRAM}/V_{CCAU}/V_{CCAU}_IO and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-state at power-on. The recommended power-off sequence is V_{CCO}/V_{CCAU}/V_{CCAU}_IO/V_{CCINT}/V_{CCINT}_IO. If the I/Os are 3-state during power-on, they can be powered by the same supply and ramped simultaneously. V_{CCINT}_IO must be connected to V_{CCINT}. If V_{CCAU}/V_{CCAU}_IO and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAU} and V_{CCAU}_IO must be connected together. When the current minimums are met, the device powers up after V_{CCINT}/V_{CCINT}_IO/V_{CCAU}/V_{CCAU}_IO and V_{CCO} supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied.

V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing recommendations. The recommended power on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, V_{MGTAVCC}, V_{MGTAVTT} OR V_{MGTAVCC}, V_{CCINT}, V_{MGTAVTT}. There is no recommended sequencing for V_{CCADC} and V_{REF}. The recommended power off sequence is V_{CCO}/V_{CCAU}/V_{CCAU}_IO/V_{CCINT}/V_{CCINT}_IO. The recommended power off sequence is the reverse of the power on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from V_{MGTAVTT} can be higher than specifications during power-up and power-down.

Power Supply			
Source	Voltage	Total (A)	
V _{CCINT}	0,900	9,165	
V _{CCINT} _IO	0,900	0,620	
V _{CCBRAM}	0,950	0,031	
V _{CCAU}	1,800	0,660	
V _{CCAU} _IO	1,800	0,546	
V _{CCO} 3.3V	3,300	0,000	
V _{CCO} 2.5V	2,500		
V _{CCO} 1.8V	1,800	0,380	
V _{CCO} 1.5V	1,500	0,936	
V _{CCO} 1.35V	1,350		
V _{CCO} 1.2V	1,200		
V _{CCO} 1.0V	1,000		
MGT _V _{CCAU}	1,800	0,081	
MGT _V _{CC}	1,000	3,038	
MGT _V _{TT}	1,200	0,592	
-	-		
-	-		
-	-		
V _{CCADC}	1,800	0,014	

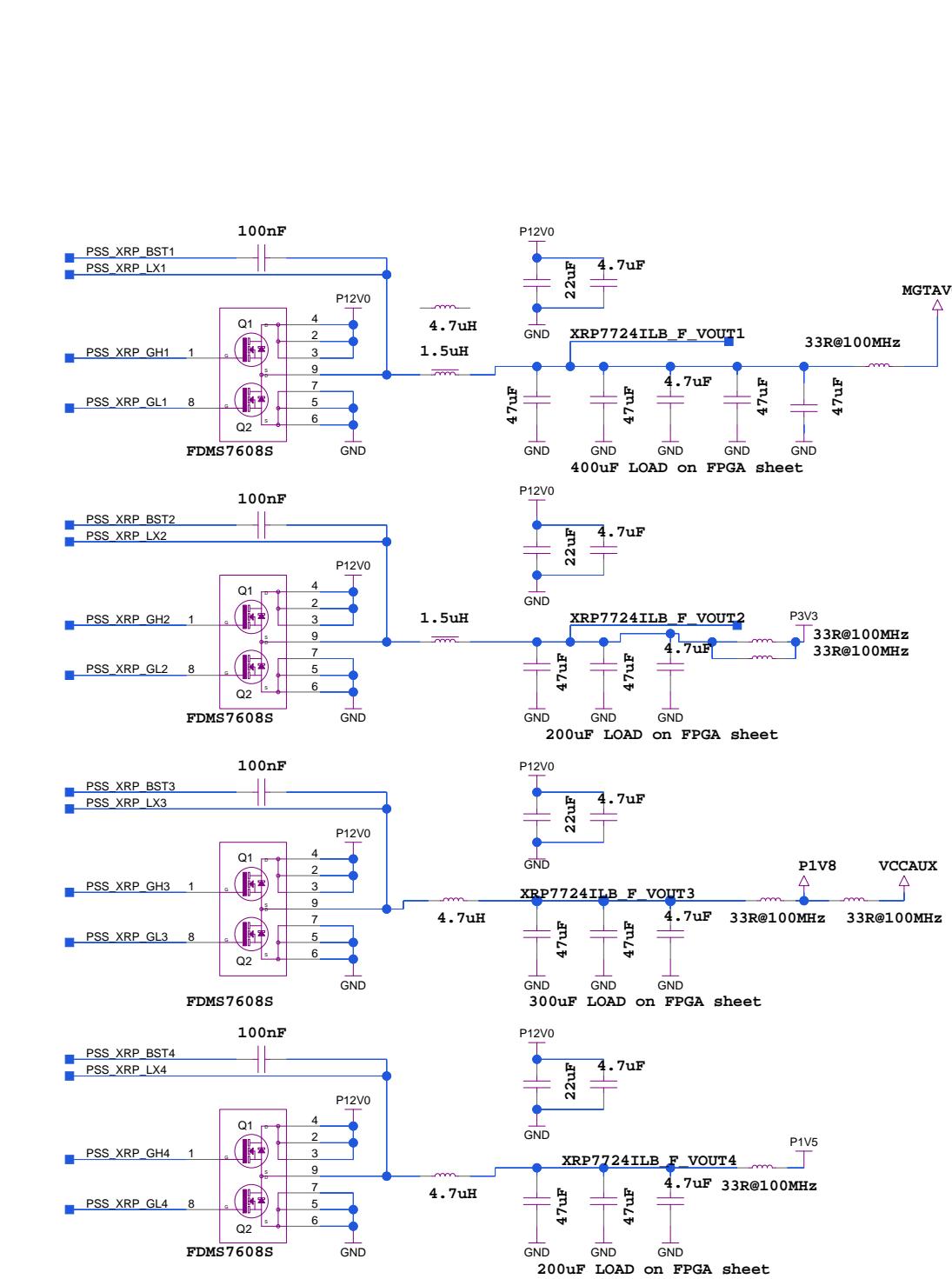
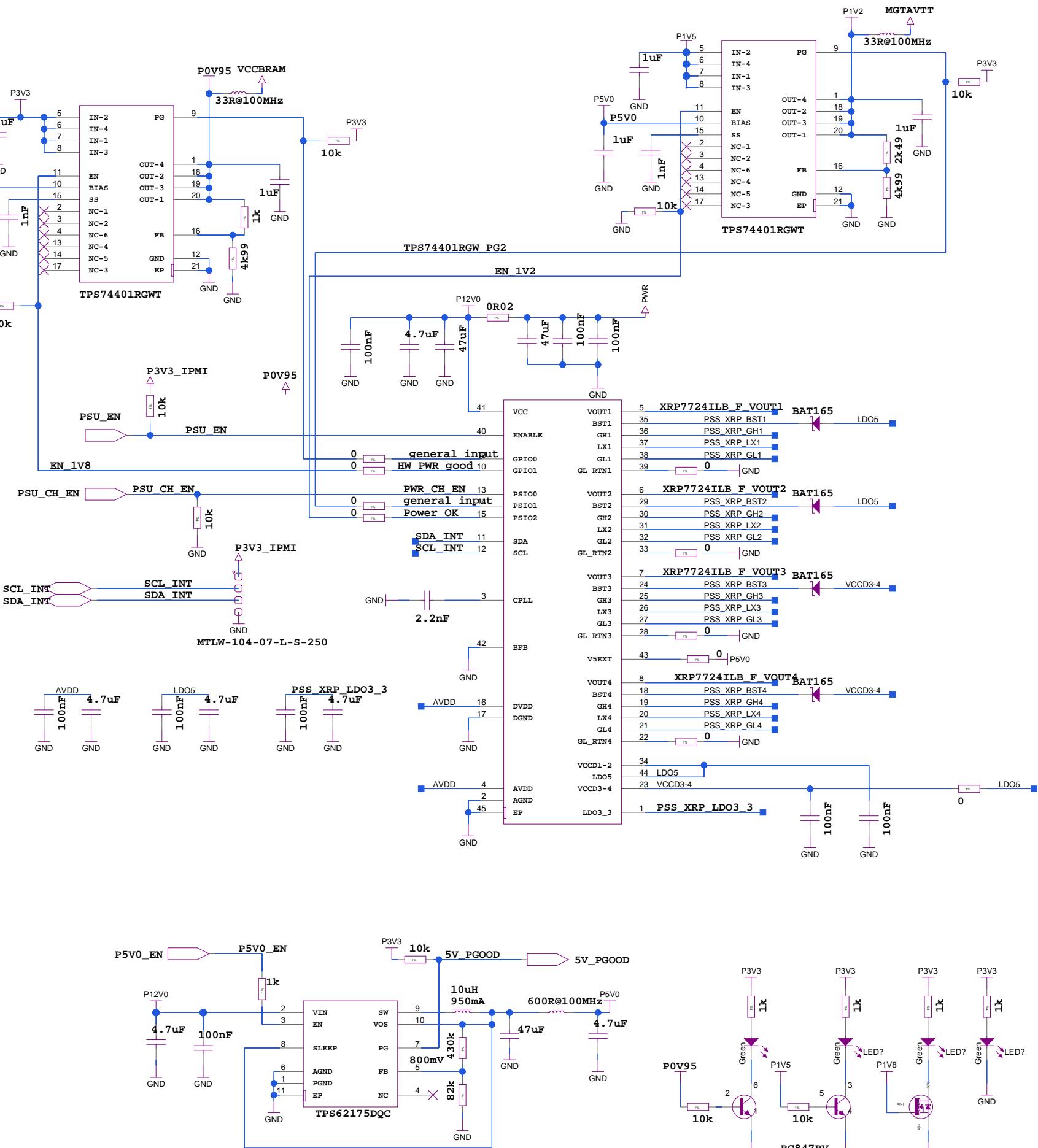


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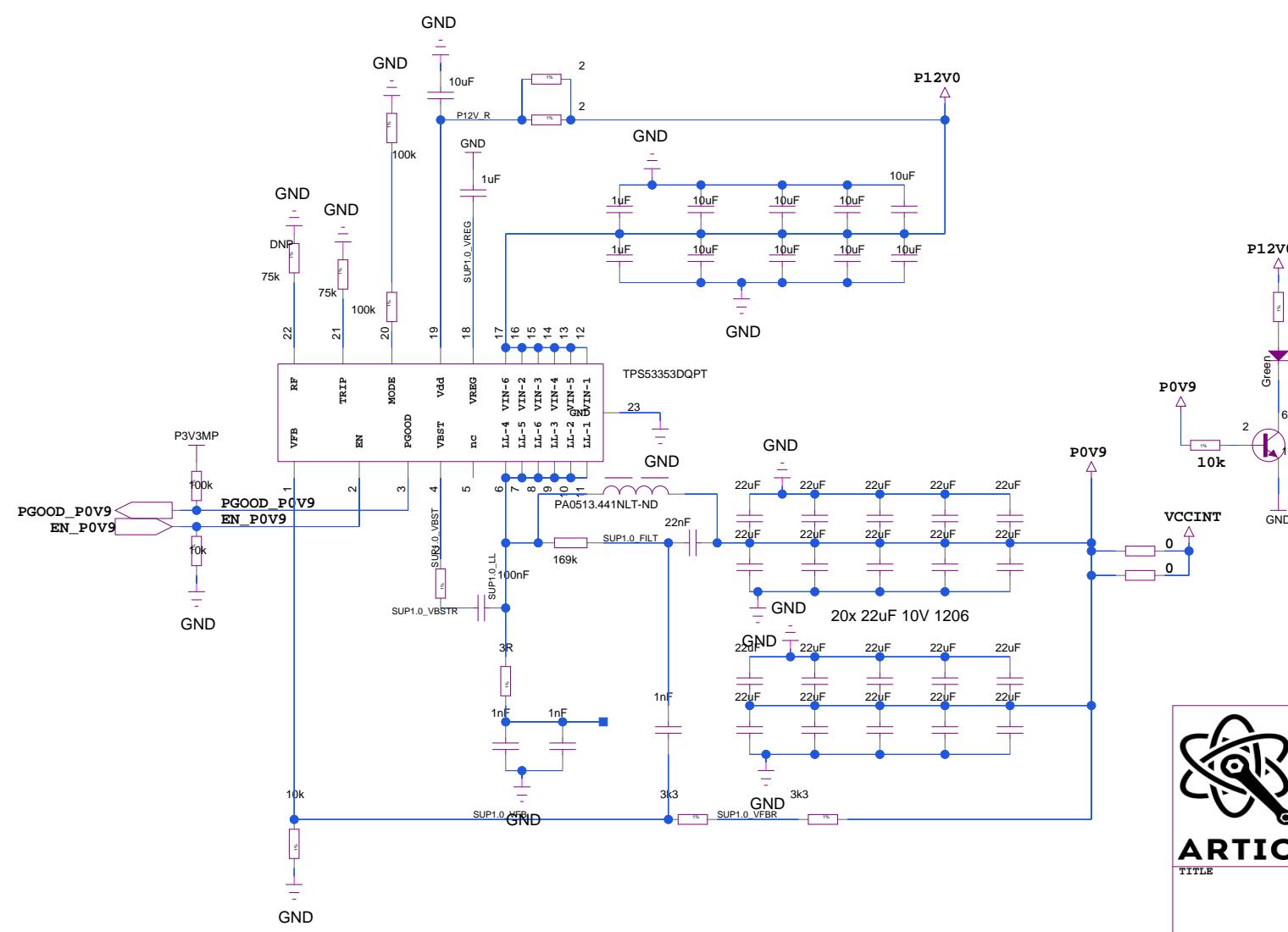
POWER_Management

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DRAWN BY	SHEET	of	
G.K.	22	29	2016/11/03:23:13:53



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PWR_DC_DC_EXAR



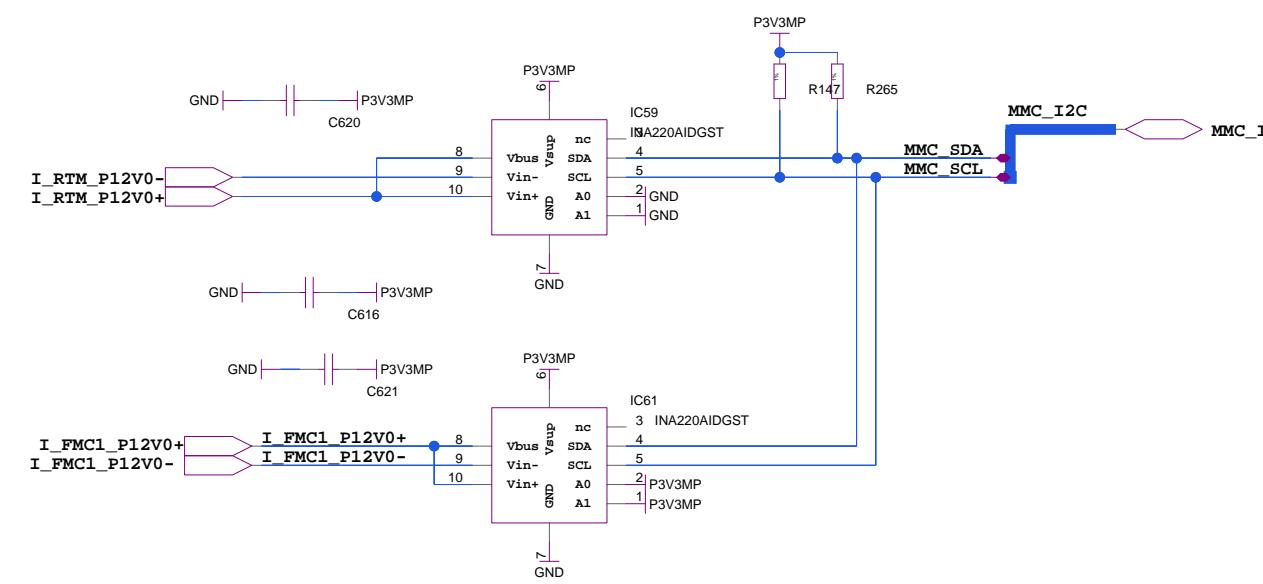
TITLE

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PWR_0V9

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DRAWN BY	SHEET	of
G.K.	24	29

2016/11/03:23:13:53

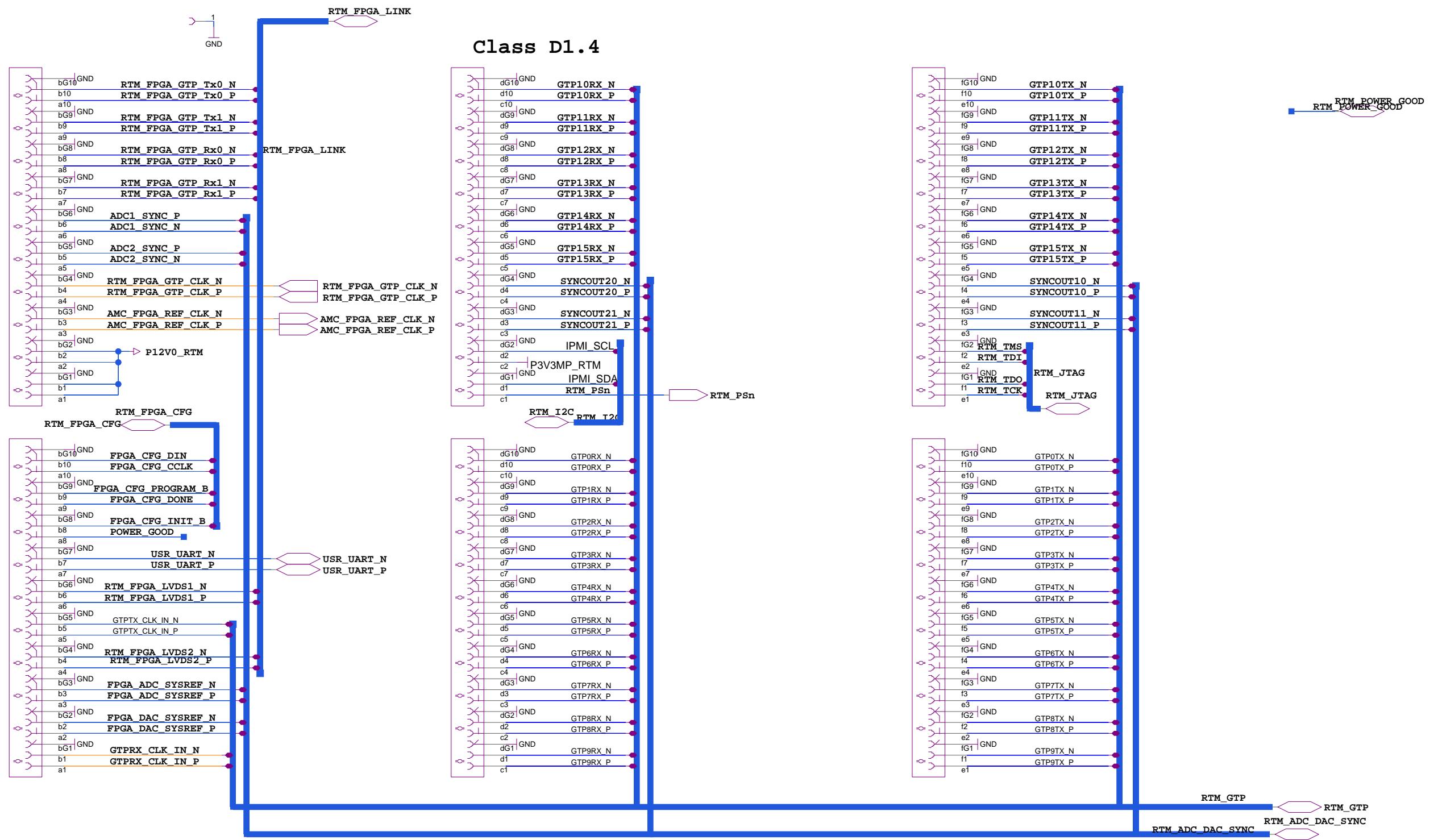


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UI_mon

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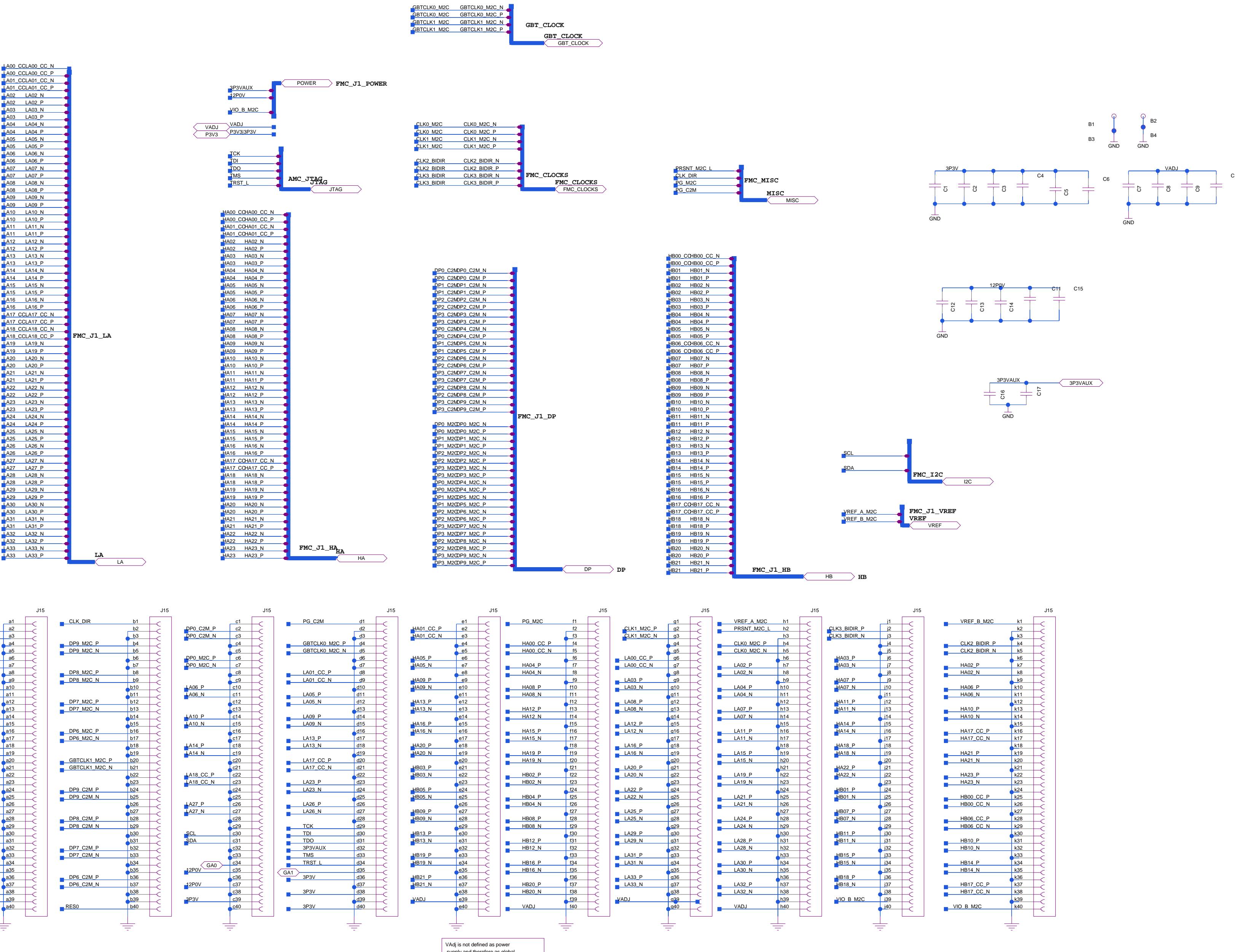
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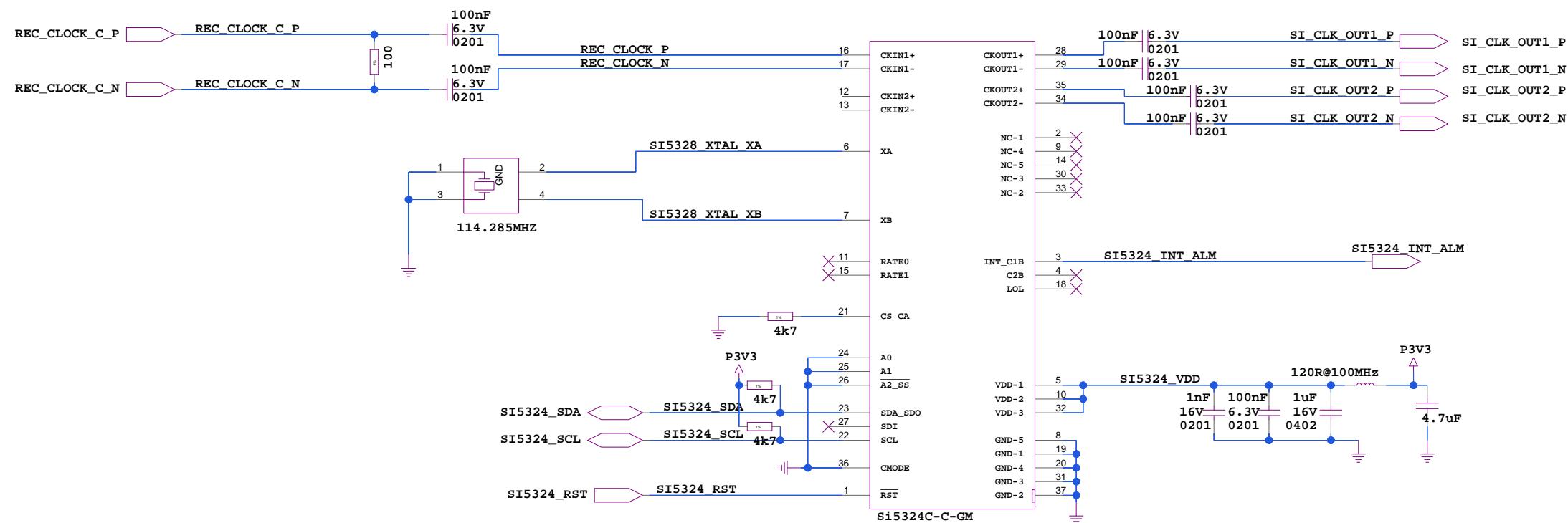
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DRAWN BY	SHEET	26	29
G.K.	of	2016/11/03:23:28:00	



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FMC_connector

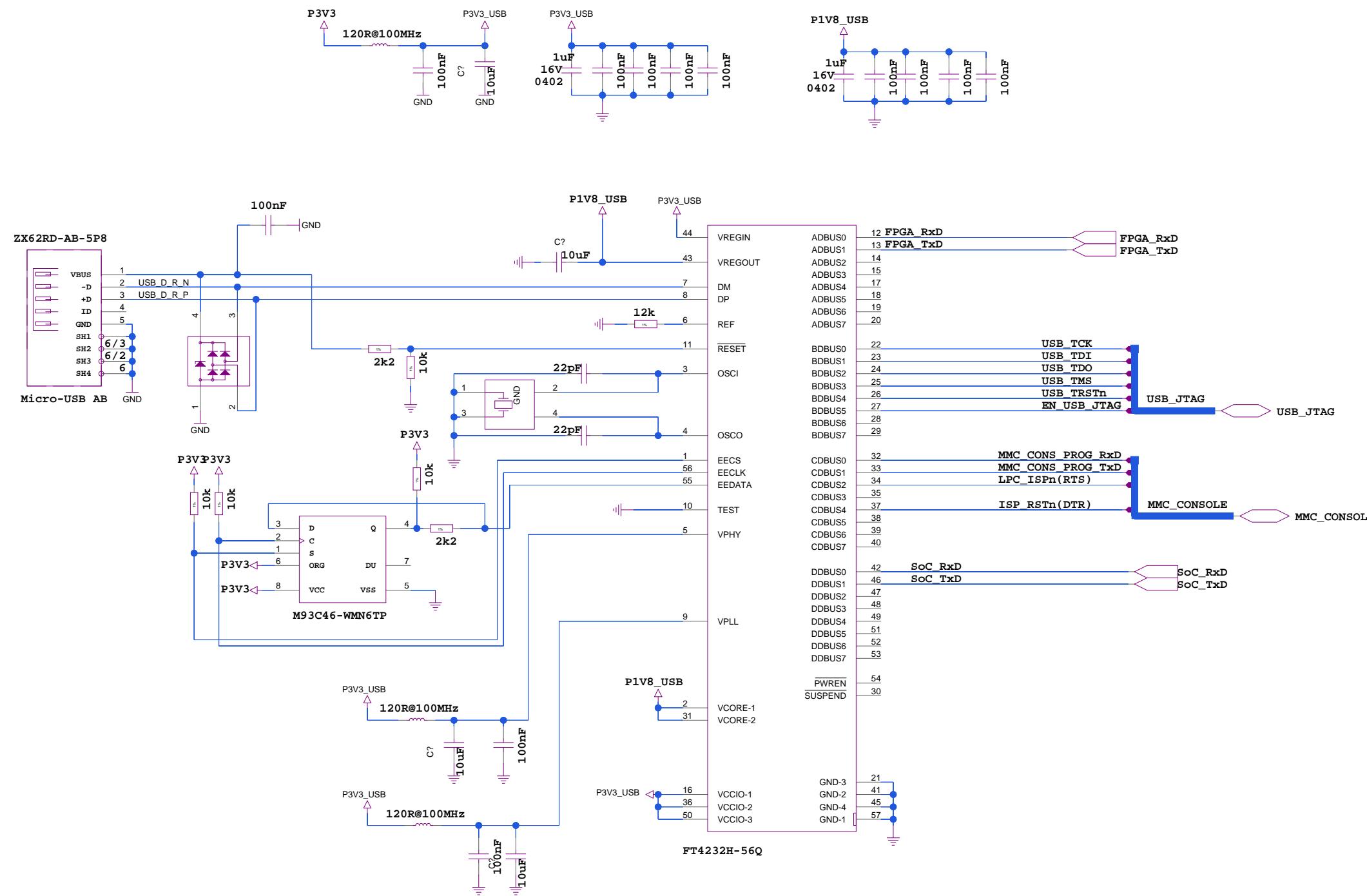


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SI5324_CLK_RECOVERY

SIZE	DWG NO	REV
A3		v0.9
DRAWN BY	SHEET of	
G.K.	28	29

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supply from USB to enable MMC at 3.3V MP



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USB_SERIAL_QUAD