

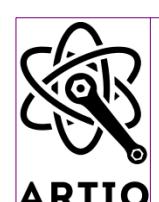
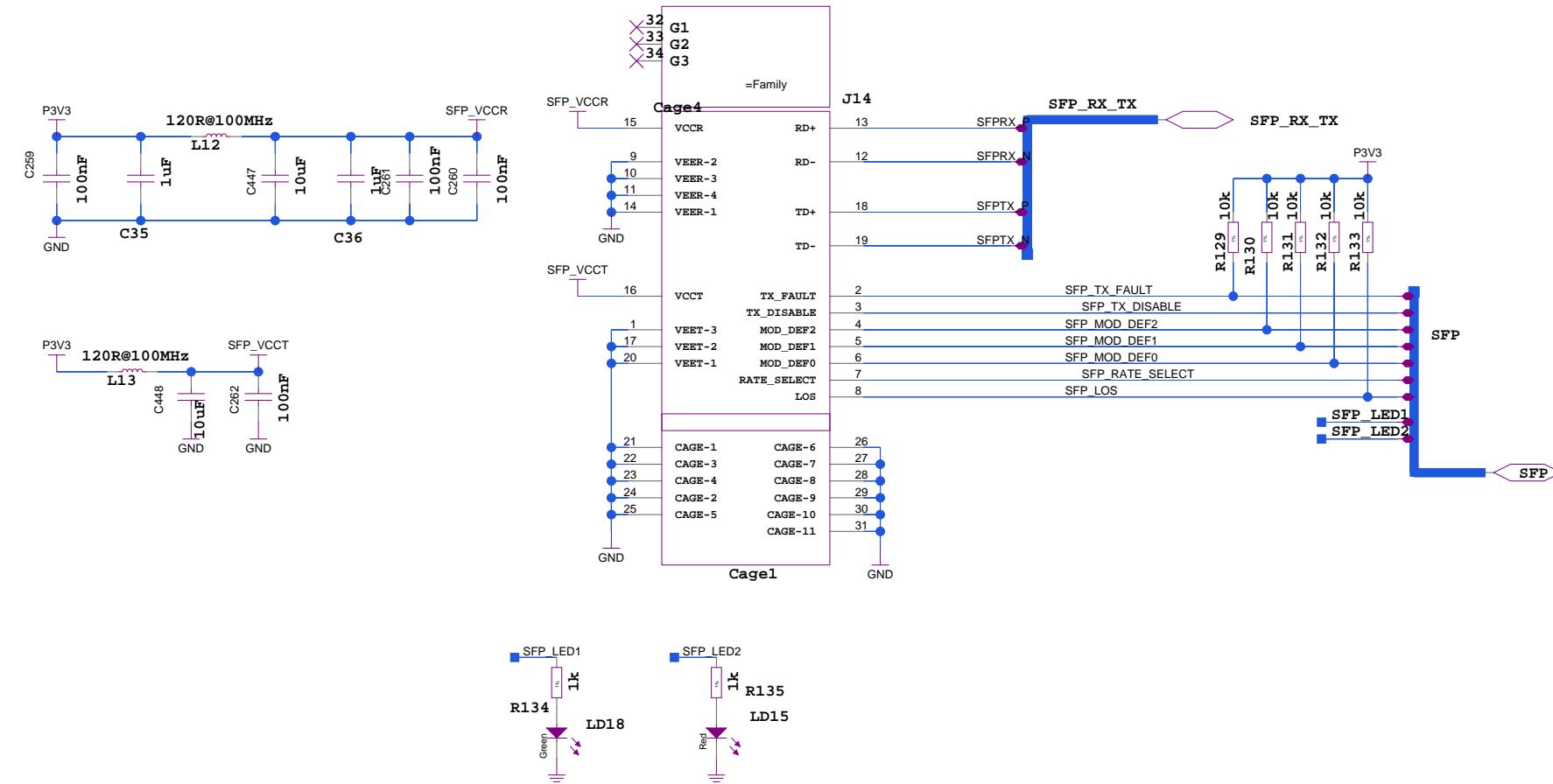
Metlino_MCH

ARTIQ Sinara

Copyright ISE WUT 2016.
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2.
(<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.2 for applicable conditions.

1M
R1 ESDSTRIP1 1M
R2 ESDSTRIP2

SIZE DWG NO
A3
DRAWN BY G.K.
1 28 REV v0.95
08/12/2016:00:00



ARTIQ Sinara

SFP

SIZE DWG NO

A3

REV

v0.95

DRAWN BY

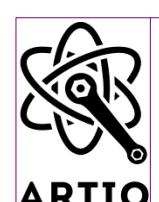
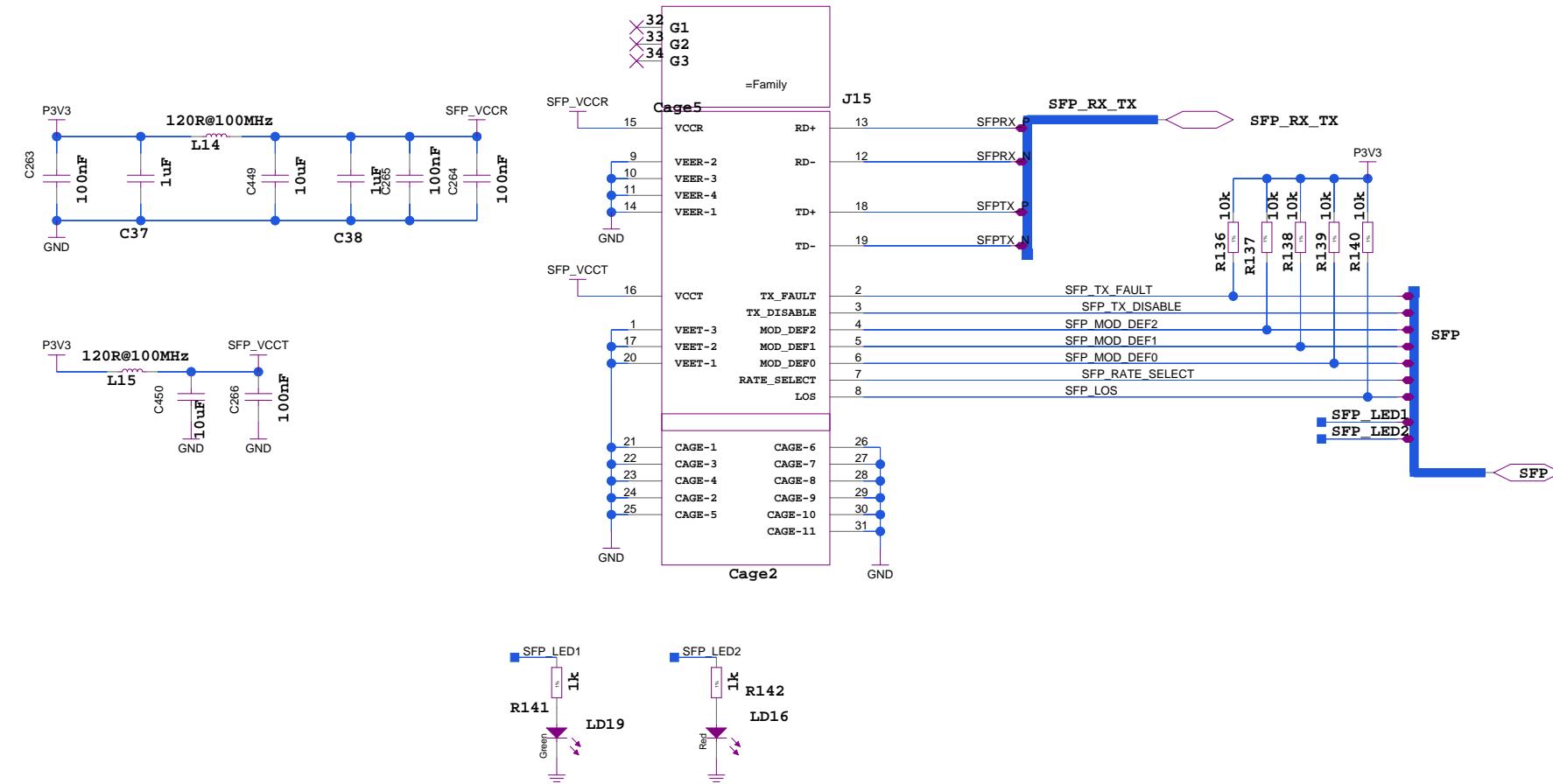
G.K.

SHEET OF

3 28

06/12/2016:16:44

Copyright ISE WUT 2016.
This documentation describes Open Hardware and is
licensed under the CERN OHL v.1.2. You may
redistribute and modify this documentation under the
terms of the CERN OHL v.1.2.
(<http://ohwr.org/CERNOHL>). This documentation is
distributed WITHOUT ANY EXPRESS OR IMPLIED
WARRANTY, INCLUDING OF
MERCHANTABILITY, SATISFACTORY QUALITY
AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.2 for applicable
conditions.



ARTIQ Sinara

SFP

SIZE DWG NO

A3

REV

v0.95

DRAWN BY

G.K.

SHEET

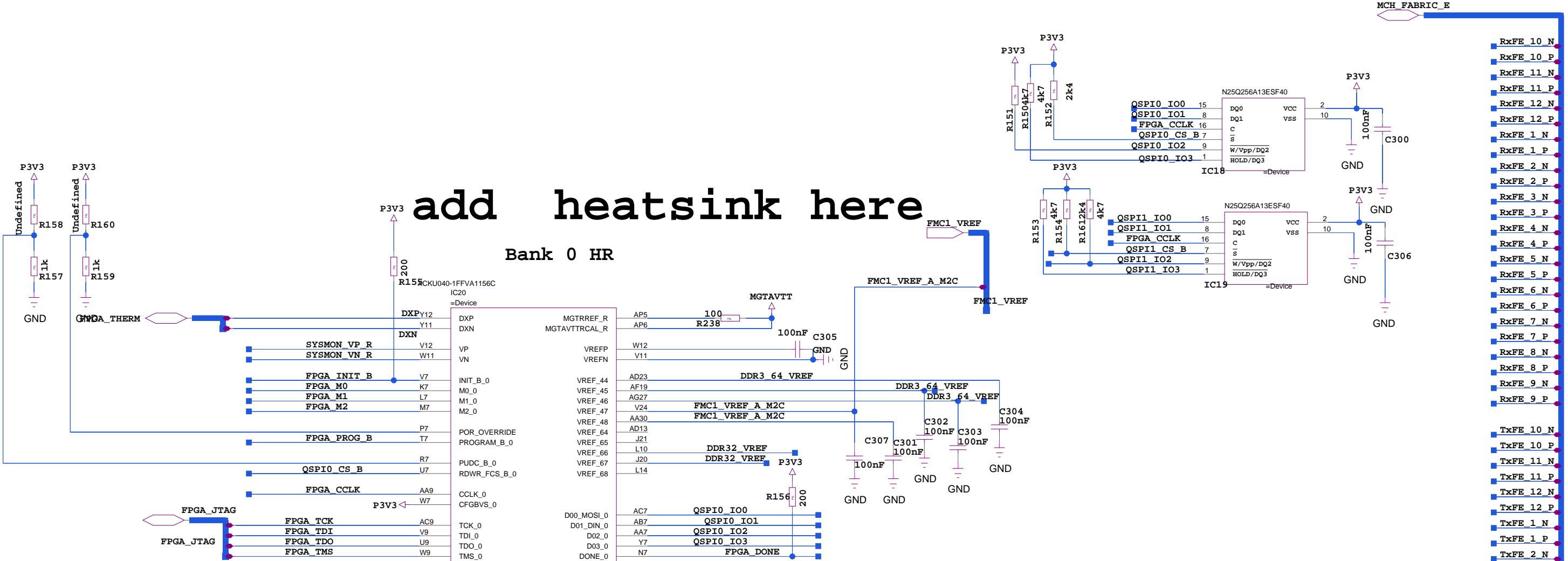
of

4

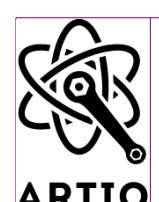
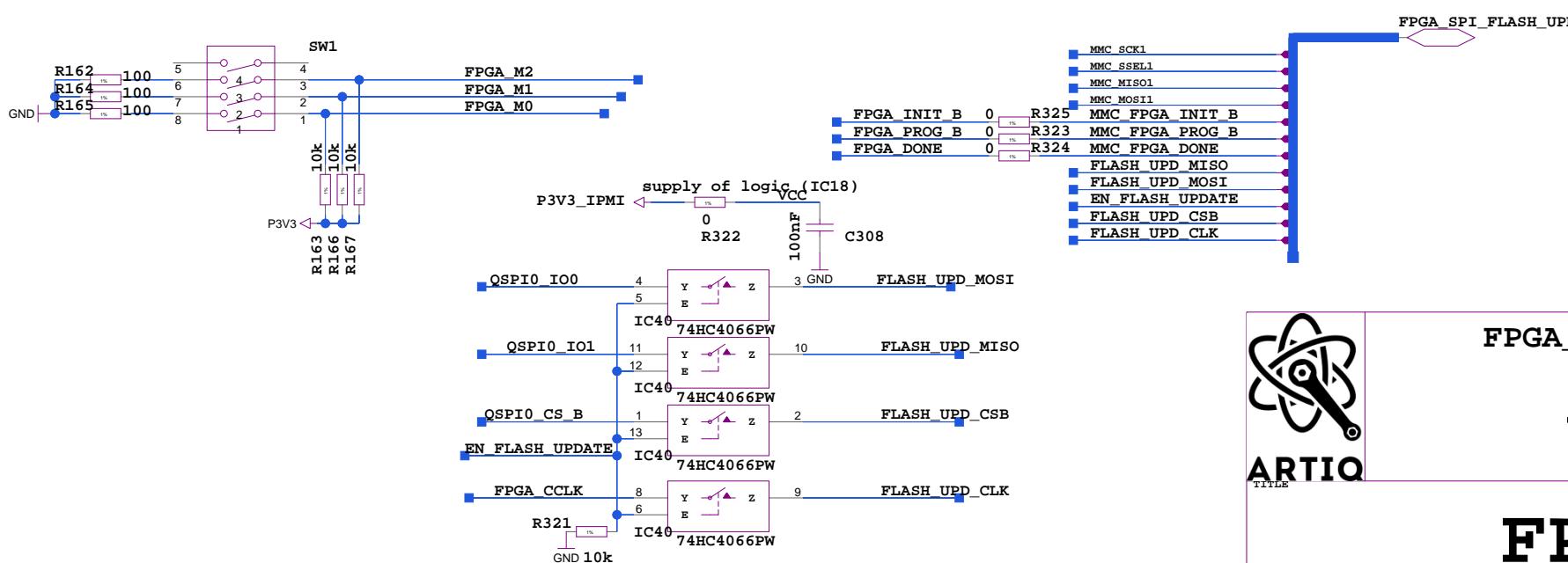
28

06/12/2016:16:44

Copyright ISE WUT 2016.
This documentation describes Open Hardware and is
licensed under the CERN OHL v.1.2. You may
redistribute and modify this documentation under the
terms of the CERN OHL v.1.2.
(<http://ohwr.org/CERNOLH>). This documentation is
distributed WITHOUT ANY EXPRESS OR IMPLIED
WARRANTY, INCLUDING OF
MERCHANTABILITY, SATISFACTORY QUALITY
AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.2 for applicable
conditions.



Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via



FPGA_XCKU040FFVA1156_MCH

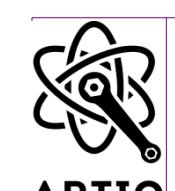
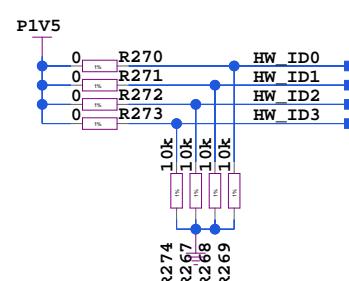
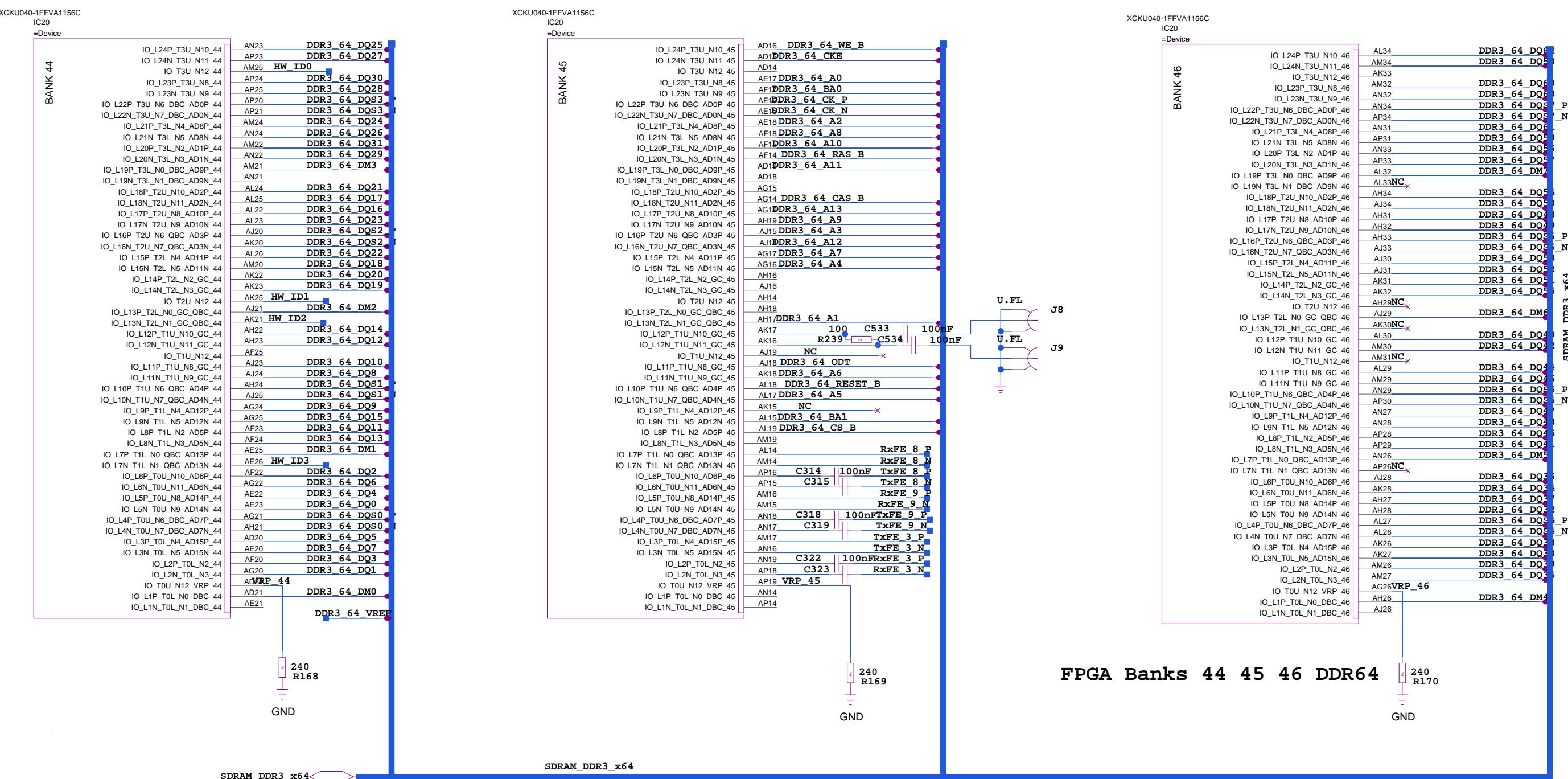
FPGA Bank 0 CFG

Copyright ISE WUT 2016.
This documentation describes Open Hardware and is
licensed under the CERN OHL v.1.2. You may
redistribute and modify this documentation under the
terms of the CERN OHL v.1.2.
(http://ohwr.org/CERNOHL). This documentation is
distributed WITHOUT ANY EXPRESS OR IMPLIED
WARRANTY, INCLUDING OF
MERCHANTABILITY, SATISFACTORY QUALITY
AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.2 for applicable
conditions.

Bank 44 HP

Bank 45 HF

Bank 46 HP

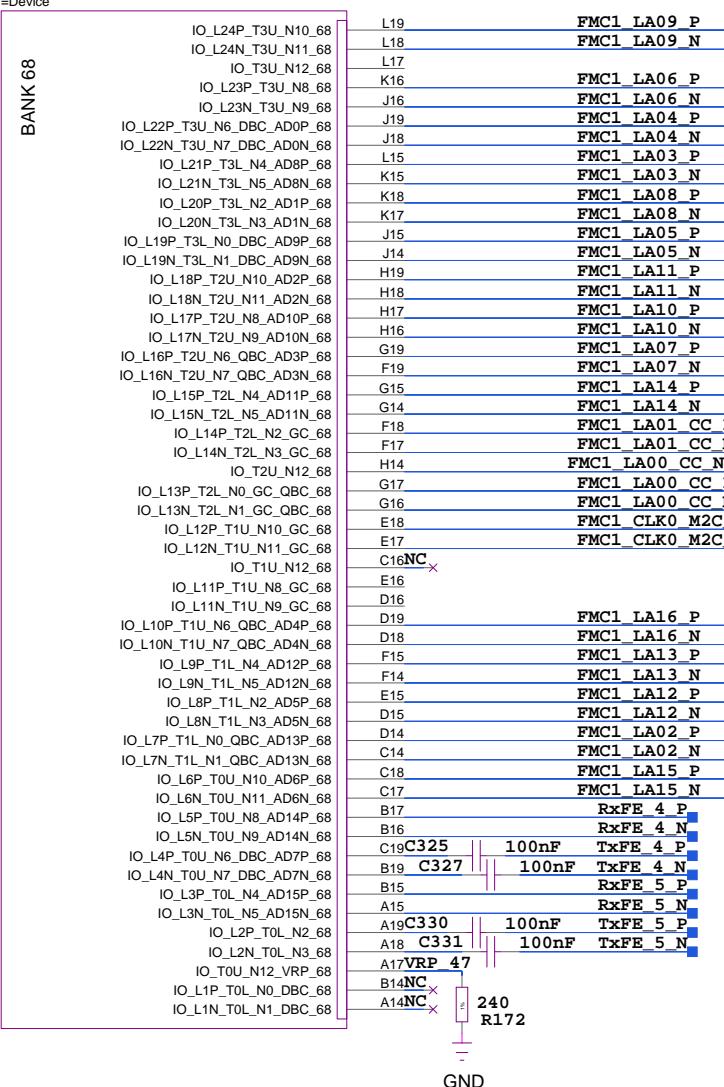


ARTIQ Sinara

FPGA Banks 44 45 46 DDR

XCKU040-1FFVA1156C
IC20
=Device

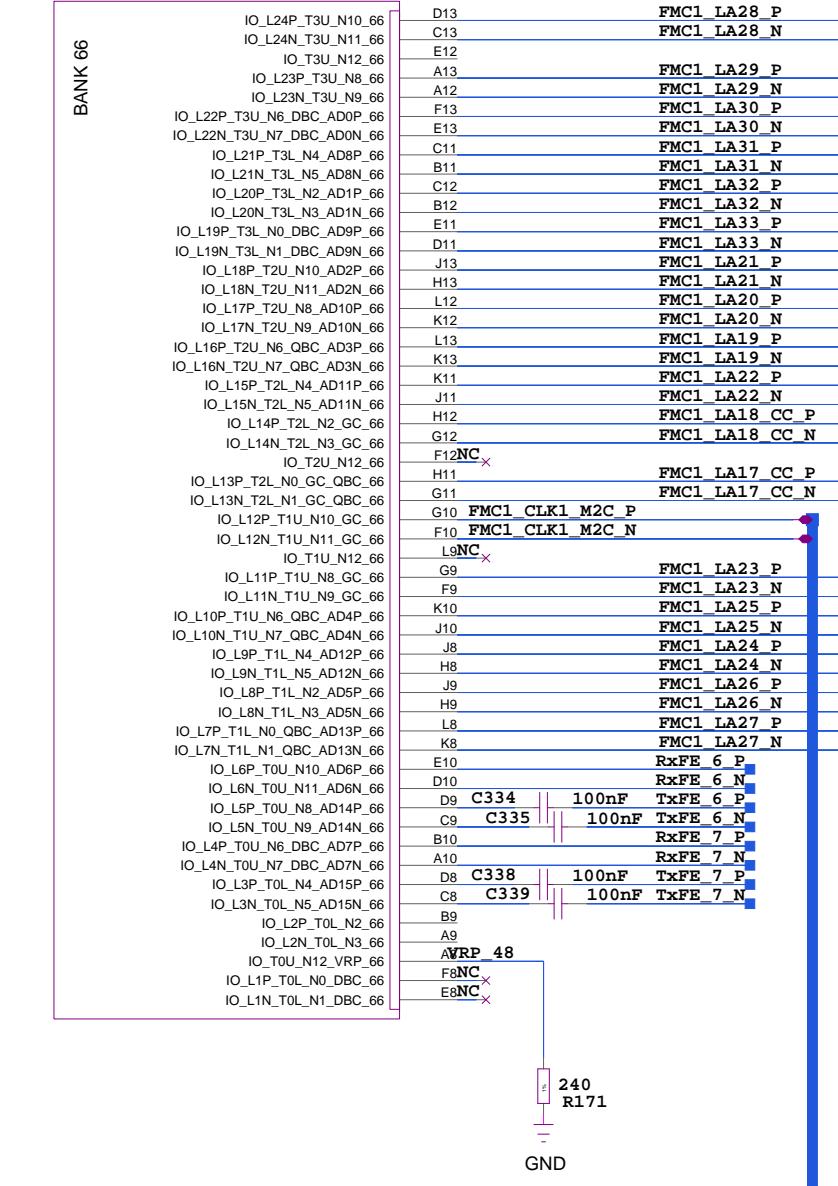
Bank 68 HP



FMC1_CLK FMC1_CLK

IC20
=Device

Bank 66 HP



FMC1_LA

FPGA_XCKU040FFVA1156_MCH



ARTIQ Sinara

FPGA Banks 47 48 HP FM

Copyright ISE WUT 2016.
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2.
Please see the CERN OHL v.1.2 for applicable conditions.

SIZE DWG NO

A3

REV

v0.95

DRAWN BY

G.K.

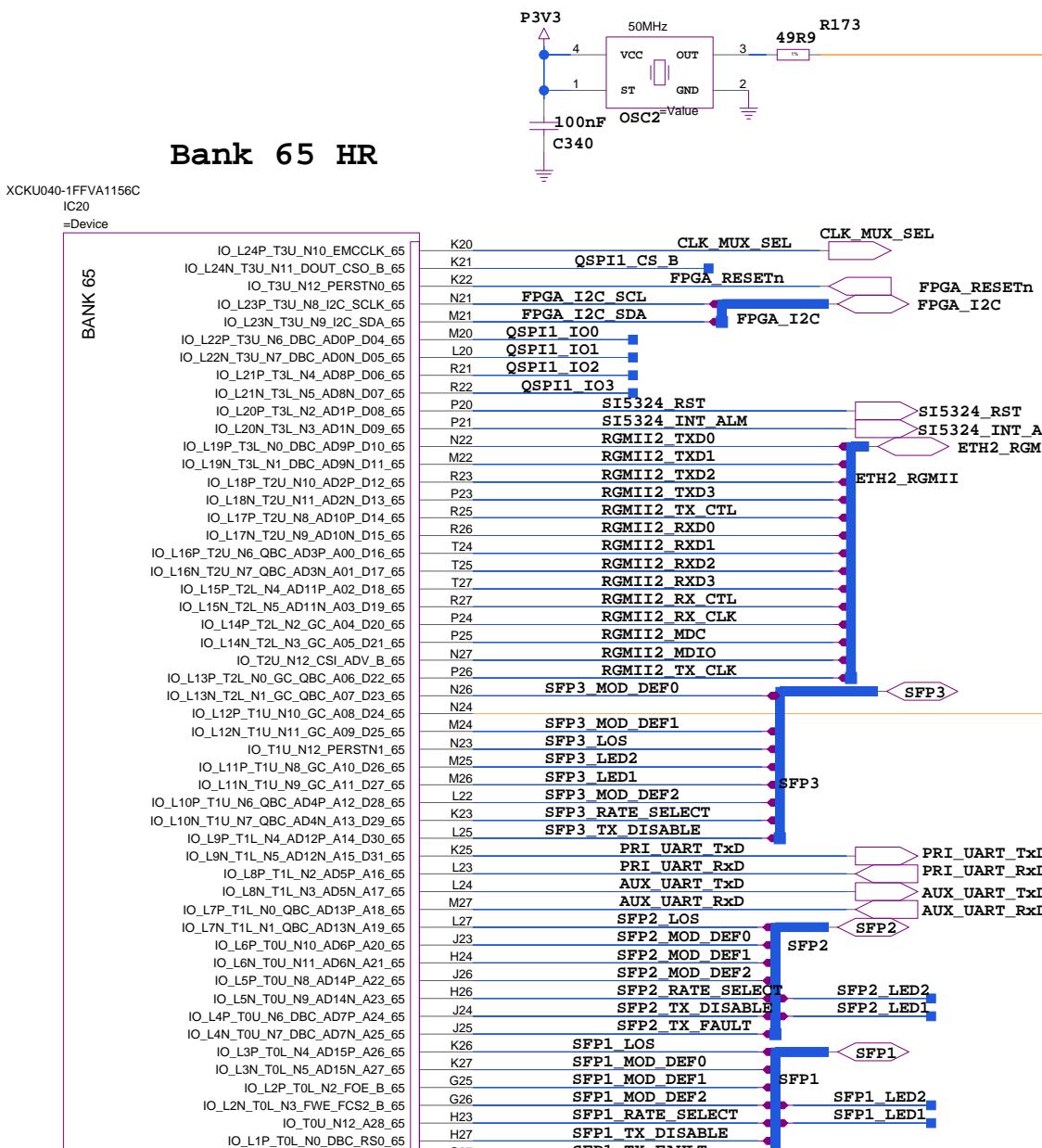
SHEET

of

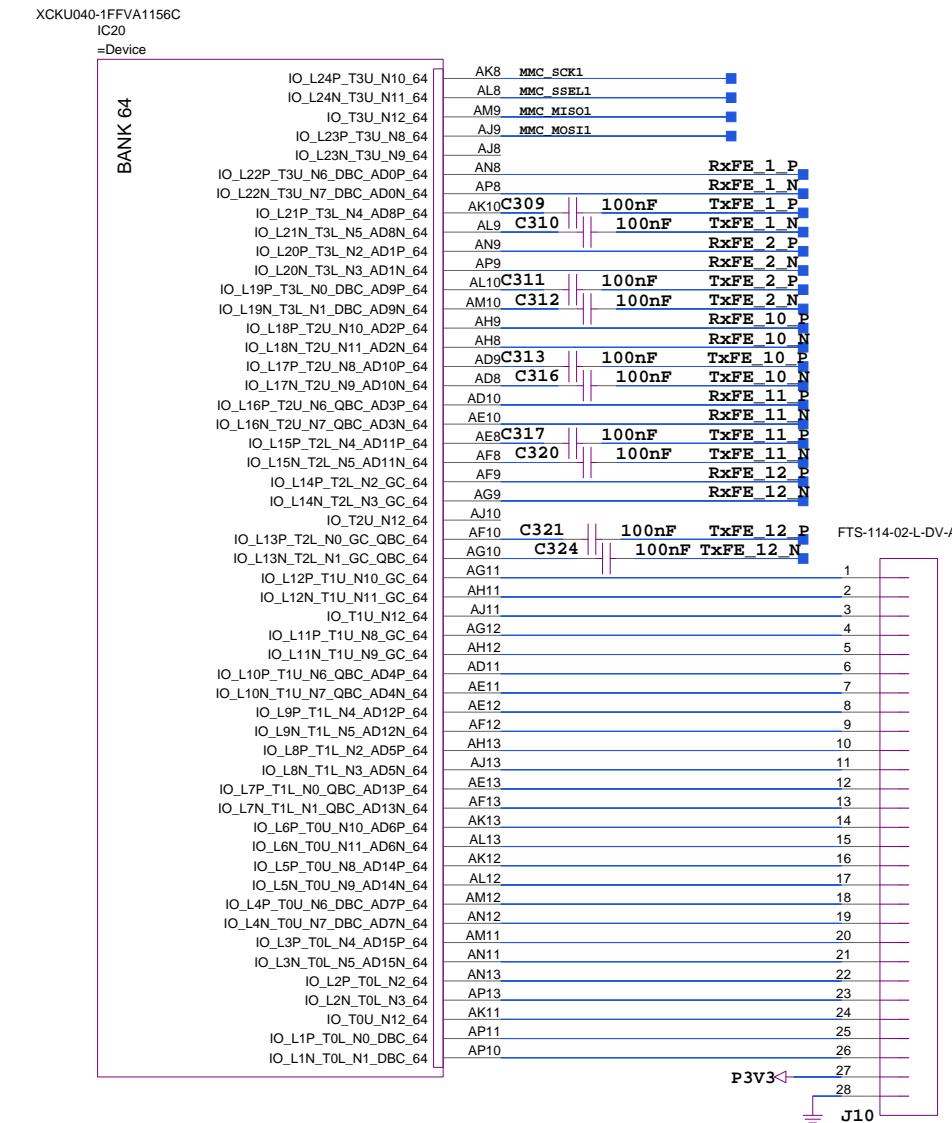
7

28

01/12/2016:18:22



Bank 64 HR



FPGA_XCKU040FFVA1156_MCH

ARTIQ Sinara

FPGA Banks 64 65 HR

SIZE DWG NO

A3

REV

v0.95

DRAWN BY

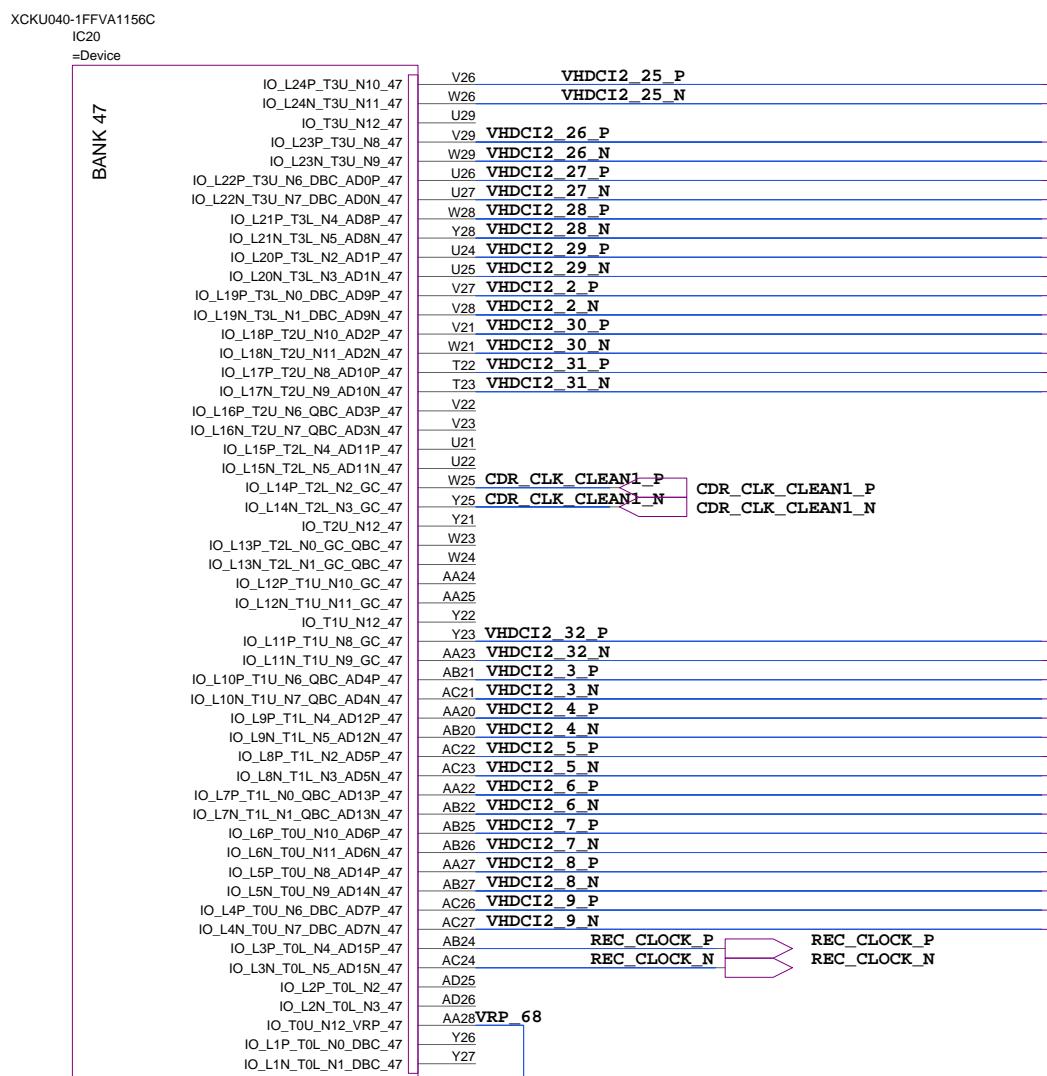
G.K.

8

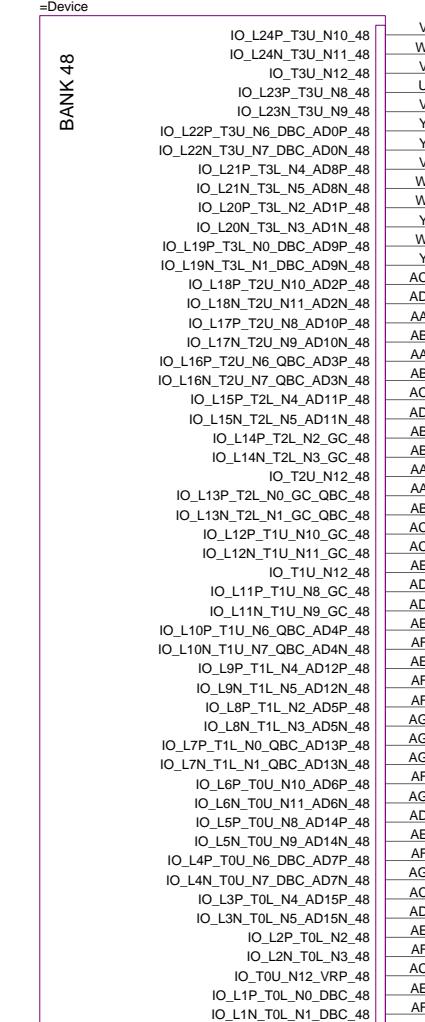
28

01/12/2016:18:22

Bank 47 HP



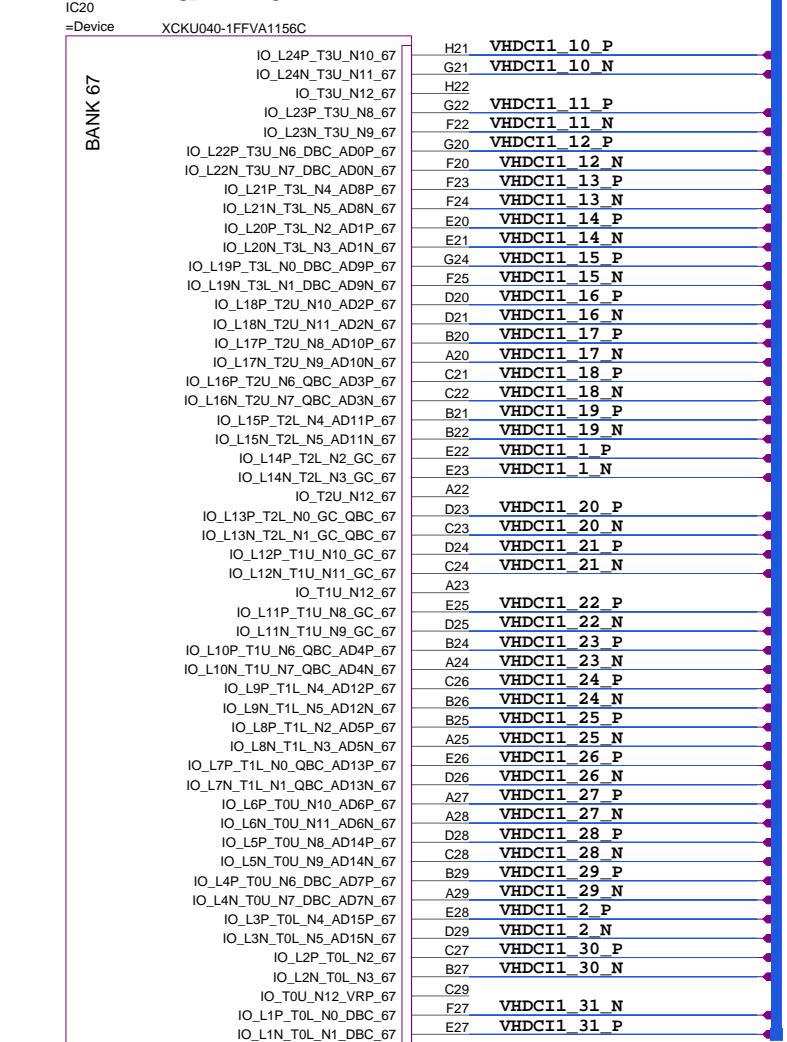
Bank 48 HP



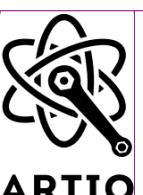
FPGA_XCKU040FFVA1156_MCH

FPGA Bank 60 67 68 HP VHDCI

Bank 67 HP

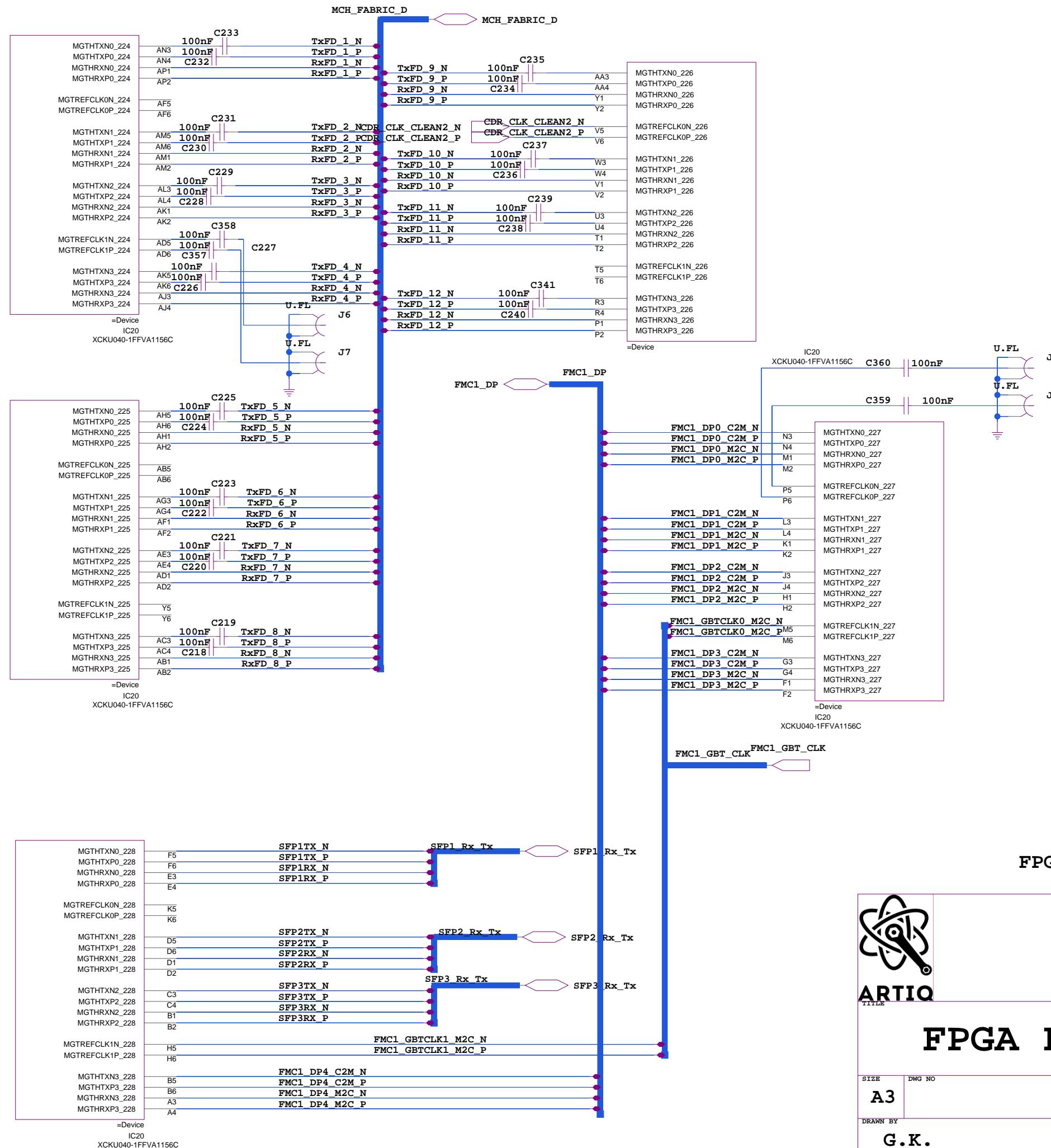


VHDCI1



ARTIQ Sinara

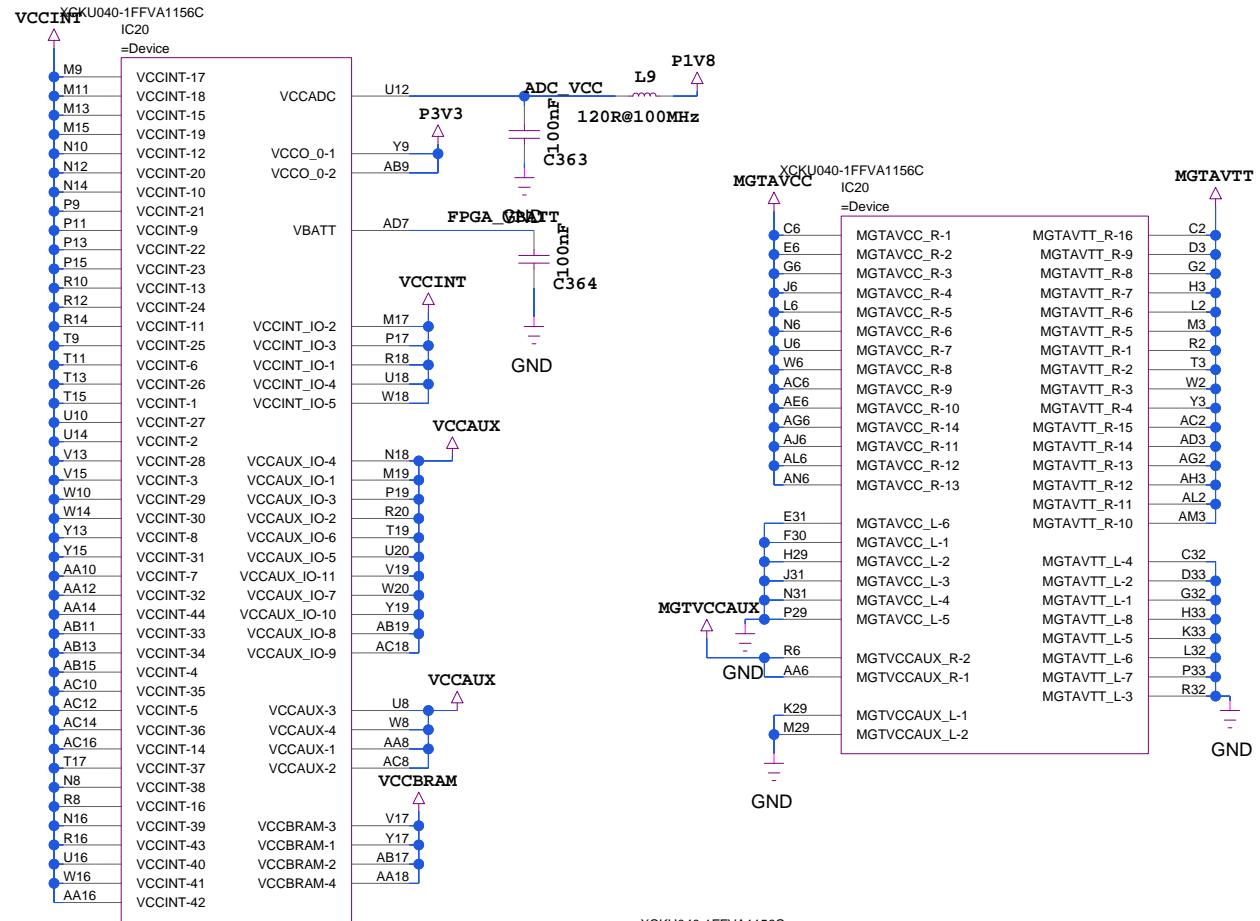
FPGA Bank 66 67 68

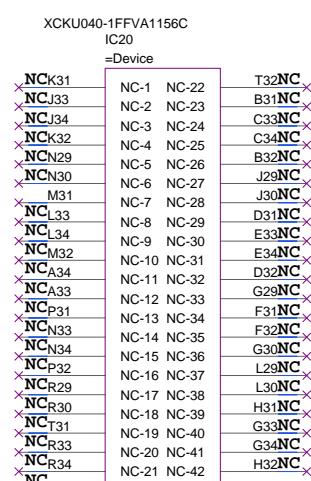
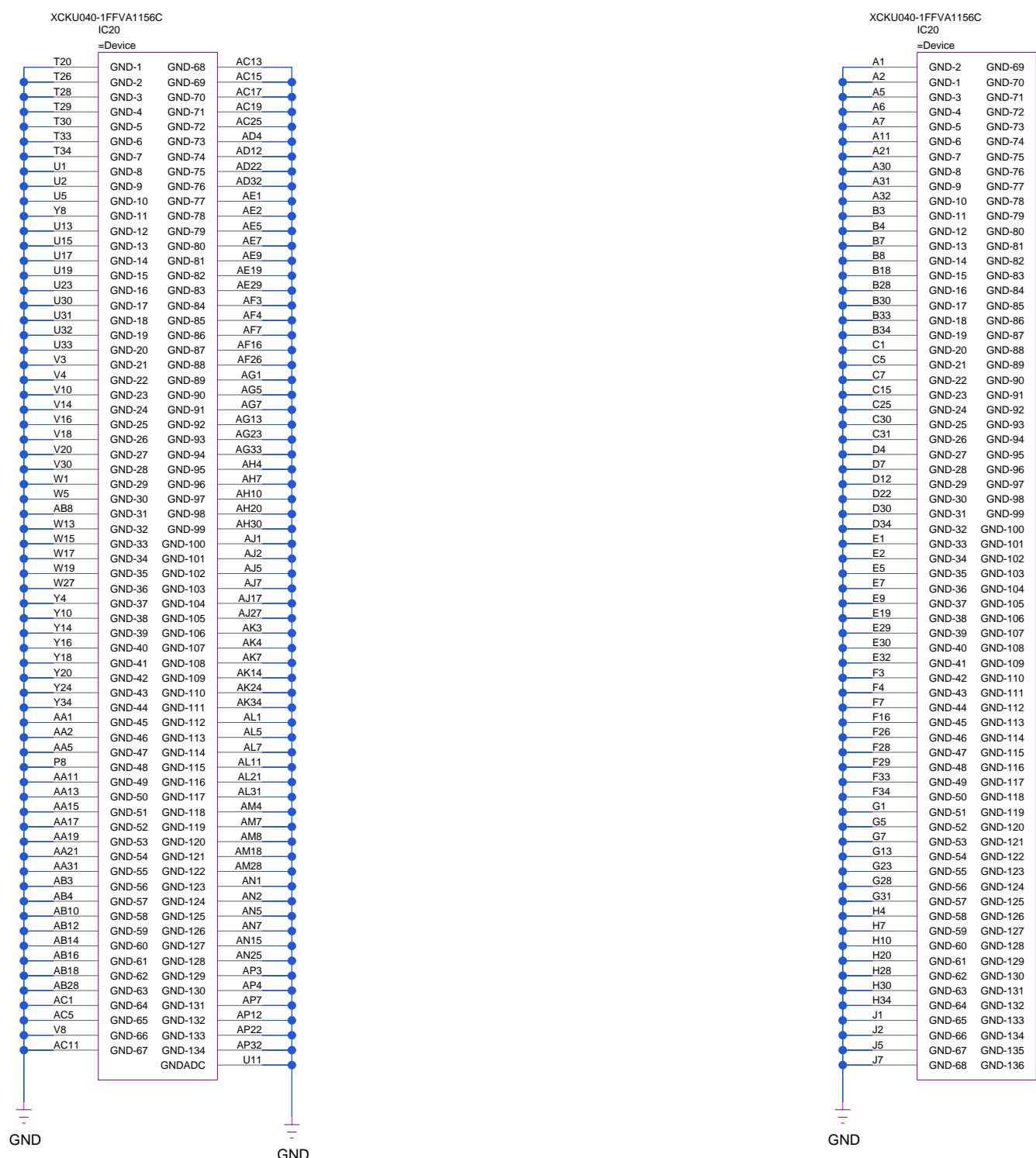


FPGA_XCKU040FFVA1156_MCH

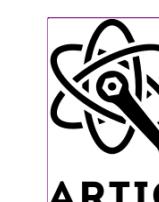


ARTIQ Sinara





FPGA XCKU040FFVA1156 MCH



ARTIQ Sinaran

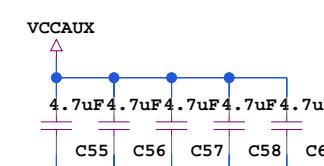
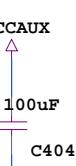
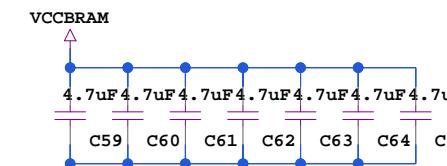
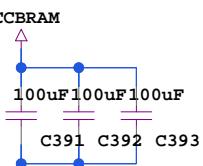
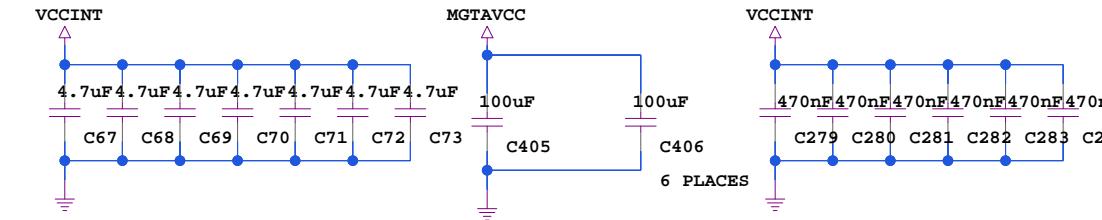
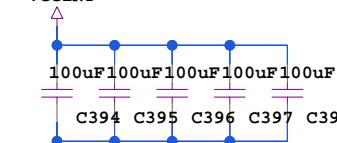
FPGA GND NC

Figure 1. A schematic diagram of the experimental setup.

A3

v0.95

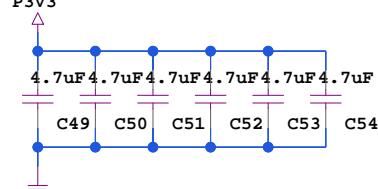
Copyright ISE WUT 2016.
This documentation describes Open Hardware and is
licensed under the CERN OHL v.1.2. You may
redistribute and modify this documentation under the
terms of the CERN OHL v.1.2.
<http://ohwr.org/CERN OHL>. This documentation is
distributed WITHOUT ANY EXPRESS OR IMPLIED
WARRANTY, INCLUDING OF
MERCHANTABILITY, SATISFACTORY QUALITY
AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.2 for applicable
conditions.



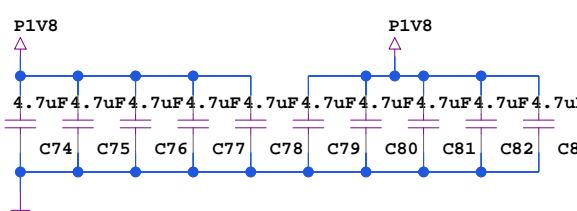
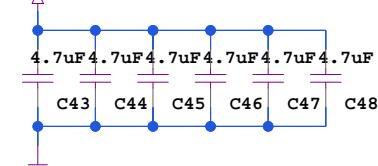
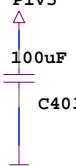
VCCO_47 / VCCO_48 VCCO_66 / VCCO_67 VCCO_68



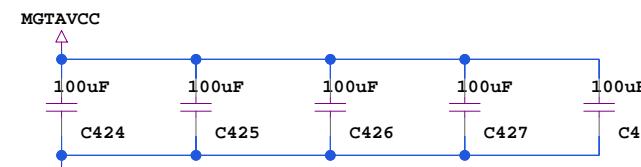
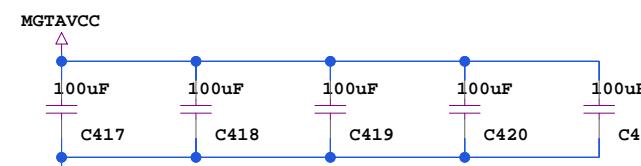
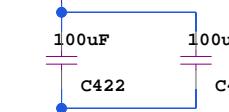
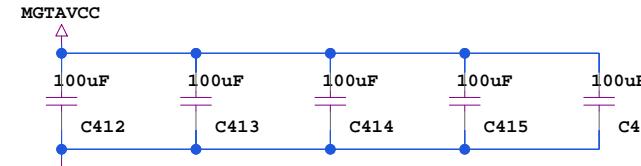
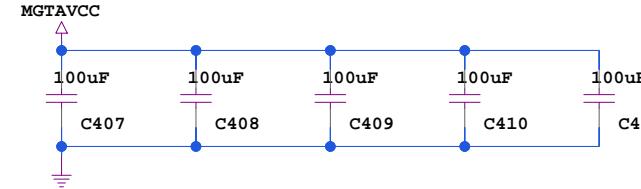
VCCO_0 / VCCO_64 / VCCO_65



VCCO_44 / VCCO_45 / VCCO_46



VCCBRAM



VCCAUX / VCCAUX_IO

FPGA_XCKU040FFVA1156_MCH



ARTIQ Sinara

FPGA Decoupling

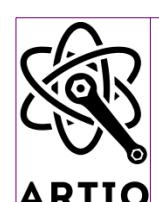
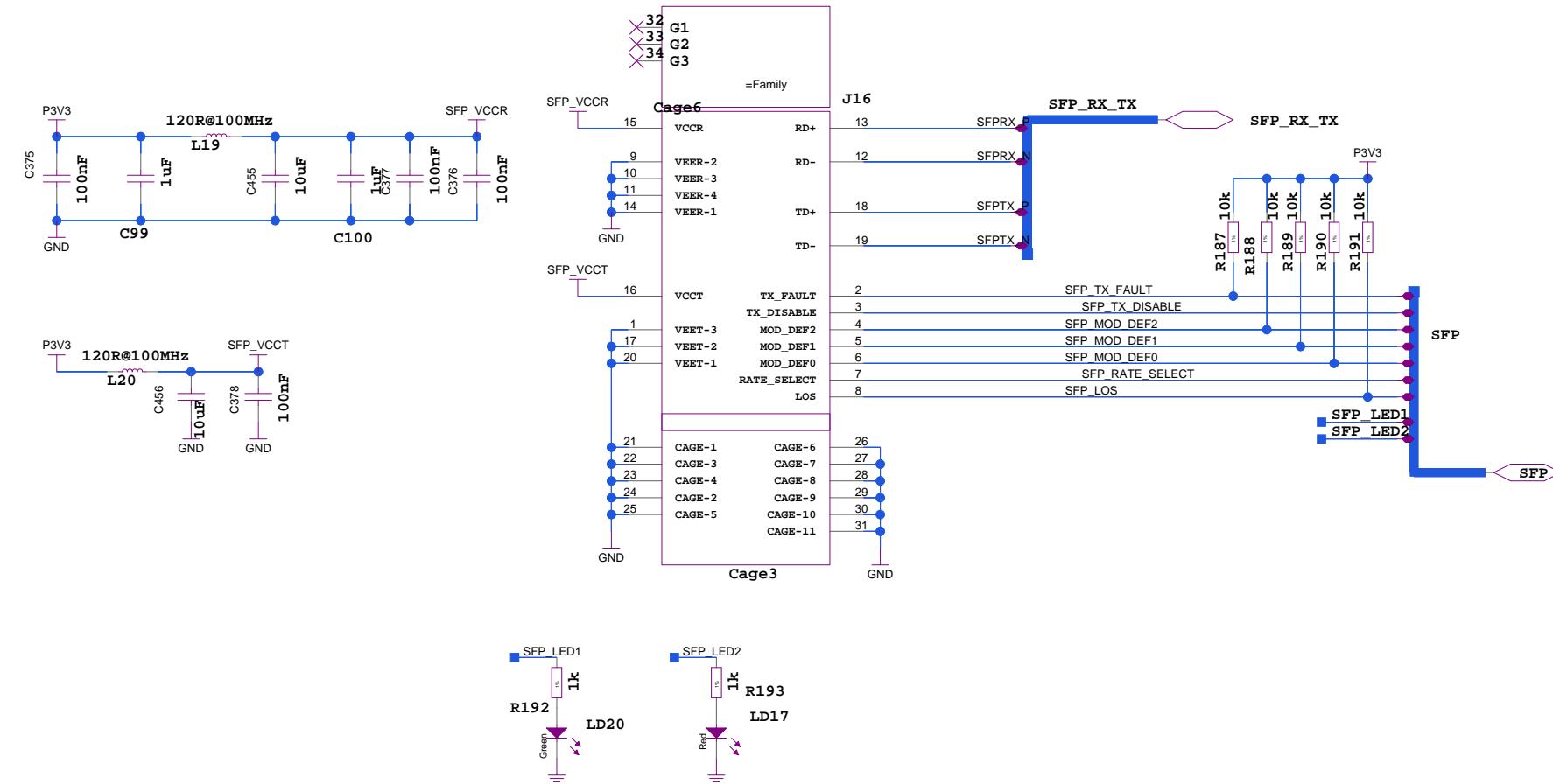
Copyright ISE WUT 2016.
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2.
Please see the CERN OHL v.1.2 for applicable conditions.

SIZE DWG NO
A3

DRAWN BY SHEET OF
G.K. 13 28

REV v0.95

01/12/2016:18:22



ARTIQ Sinara

SFP

SIZE DWG NO

A3

REV

v0.95

DRAWN BY

G.K.

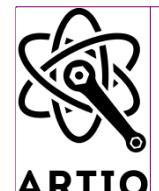
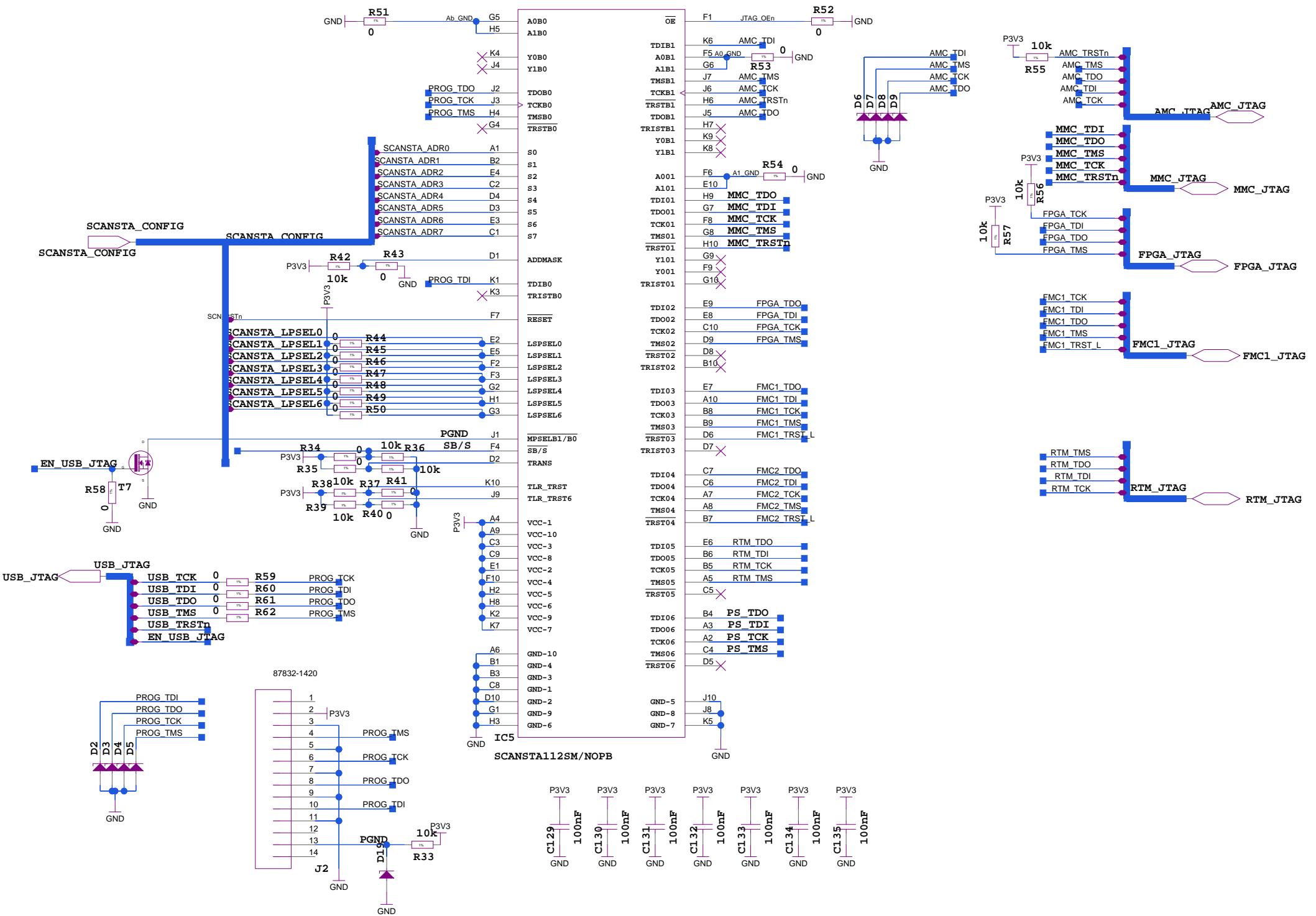
SHEET

of

14 28

06/12/2016:16:44

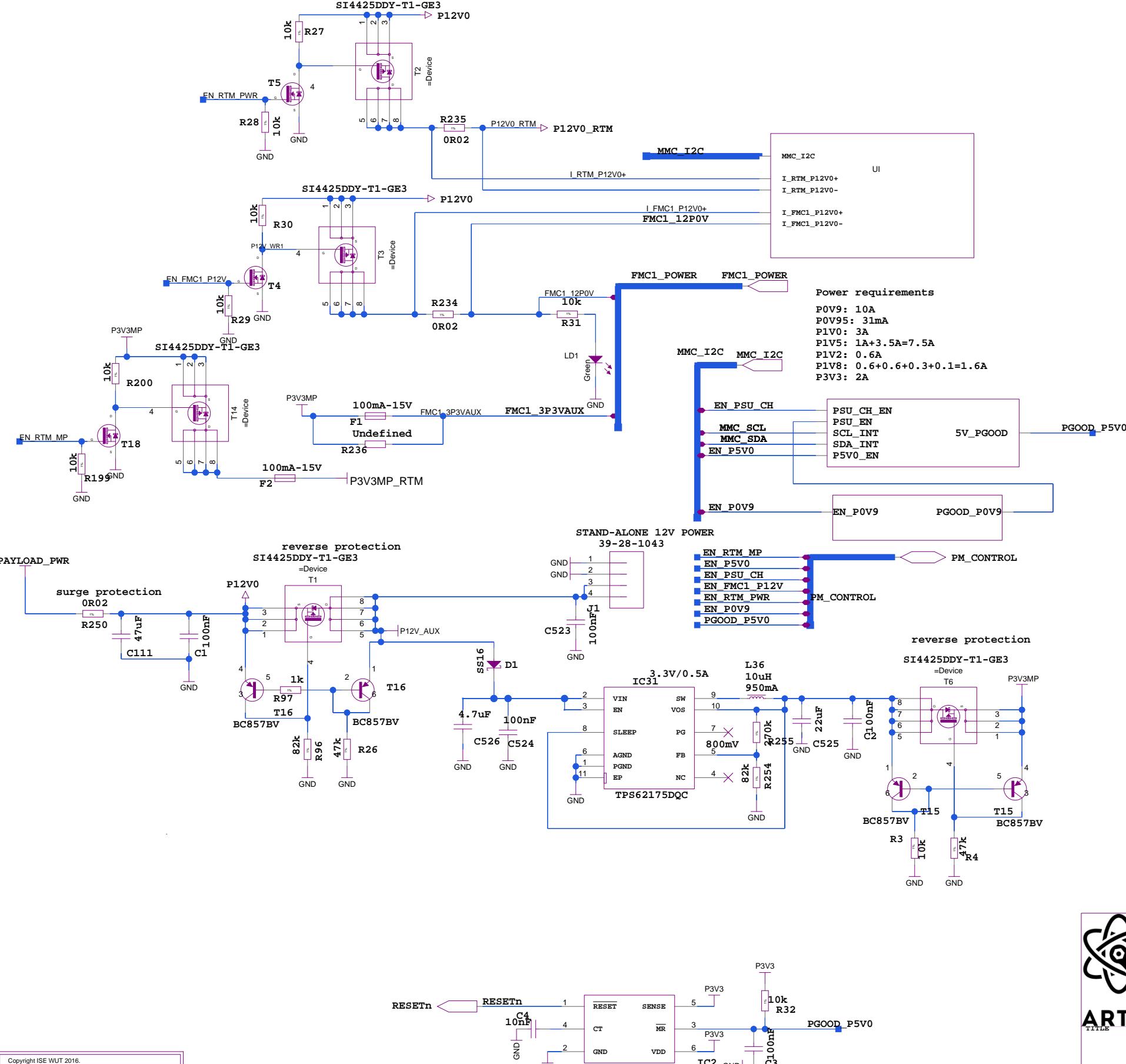
Copyright ISE WUT 2016.
This documentation describes Open Hardware and is
licensed under the CERN OHL v.1.2. You may
redistribute and modify this documentation under the
terms of the CERN OHL v.1.2.
(<http://ohwr.org/CERNOHL>). This documentation is
distributed WITHOUT ANY EXPRESS OR IMPLIED
WARRANTY, INCLUDING OF
MERCHANTABILITY, SATISFACTORY QUALITY
AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.2 for applicable
conditions.



ARTIQ Sinara

JTAG_Configuration

SIZE	DWG NO	REV
A3		v0.95
DRAWN BY	SHEET of	
G.K.	15	28



Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V _{CCINT}	Internal supply voltage	0.922	0.950	0.979	V
V _{CCINT}	For -1L (0.90V) devices: internal supply voltage	0.880	0.900	0.920	V
V _{CCINT}	For -3 (1.0V only) devices: internal supply voltage	0.970	1.000	1.030	V
V _{CCINT}	Internal supply voltage for the I/O banks	0.922	0.950	0.979	V
V _{CCINT}	For -1L (0.90V) devices: internal supply voltage for the I/O banks	0.880	0.900	0.920	V
V _{CCBRAM}	Block RAM supply voltage	0.922	0.950	0.979	V
V _{CCCAUX}	For -3 (1.0V only) devices: block RAM supply voltage	0.970	1.000	1.030	V
V _{CCO}	Auxiliary supply voltage	1.746	1.800	1.854	V
V _{CCO}	Supply voltage for HP I/O banks	1.140	-	3.400	V
V _{CCO}	Supply voltage for HP I/O banks	0.950	-	1.890	V
V _{CCO}	Auxiliary I/O supply voltage	1.746	1.800	1.854	V
V _{IN}	I/O input voltage	-0.200	-	V _{CCO} + 0.200	V
V _{IN}	I/O input voltage when V _{CCO} = 3.3V for V _{REF} and differential I/O standards except TMDS_33 ⁽⁸⁾	-	0.400	2.625	V
I _H	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	-	-	10.000	mA
V _{BATT}	Battery voltage	1.000	-	1.890	V
GTH and GTY Transceivers					
V _{MGTAVCC} ⁽¹¹⁾	Analog supply voltage for the GTH and GTY transceivers ⁽¹⁰⁾	0.970	1.000	1.030	V
V _{MGTAVTT} ⁽¹¹⁾	Analog supply voltage for the GTH and GTY transmitter and receiver termination circuits	1.170	1.200	1.230	V
V _{MGTVCVCAU} ⁽¹¹⁾	Auxiliary analog QPLL voltage supply for the transceivers	1.750	1.800	1.850	V
Temperature					
V _{TEMPMON} ⁽¹¹⁾	Analog supply voltage for the resistor calibration circuit of the GTH and GTY transceiver columns	1.170	1.200	1.230	V
V _{CACD}	SYMON supply relative to GNDADC	1.746	1.800	1.854	V
V _{REF}	Externally supplied reference voltage	1.200	1.250	1.300	V
T _J	Junction temperature operating range for commercial (C)	0	-	85	°C
T _J	Junction temperature operating range for extended (E) temperature devices	0	-	100	°C
T _J	Junction temperature operating range for industrial (I)	-40	-	100	°C

Power-On/Off Power Supply Sequencing

The recommended power on sequence is V_{CCINT}/V_{CCINT}_IO/V_{CCBRAM}/V_{CCAU}/V_{CCAU}_IO and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-state at power-on. The recommended power down sequence is V_{CCO}/V_{CCAU}/V_{CCAU}_IO/V_{CCBRAM}/V_{CCINT}/V_{CCINT}_IO. If the same recommended power levels are maintained during power sequencing, the I/Os can be 3-state at power-off. V_{CCINT}_IO must be connected to V_{CCINT}. If V_{CCAU}/V_{CCAU}_IO and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAU} and V_{CCAU}_IO must be connected together. When the current minimums are met, the device powers up after the V_{CCINT}/V_{CCINT}_IO/V_{CCBRAM}/V_{CCAU}/V_{CCAU}_IO and V_{CCO} supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied.

V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing recommendations.

The recommended power on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, V_{MGTAVCC}, V_{MGTAVTT}, OR V_{MGTAVCC}, V_{CCINT}, V_{MGTAVTT}. There is no recommended sequencing for V_{MGTAVCC} and V_{MGTAVTT}. The recommended power off sequence is the reverse of the power on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from V_{MGTAVTT} can be higher than specifications during power-up and power-down.

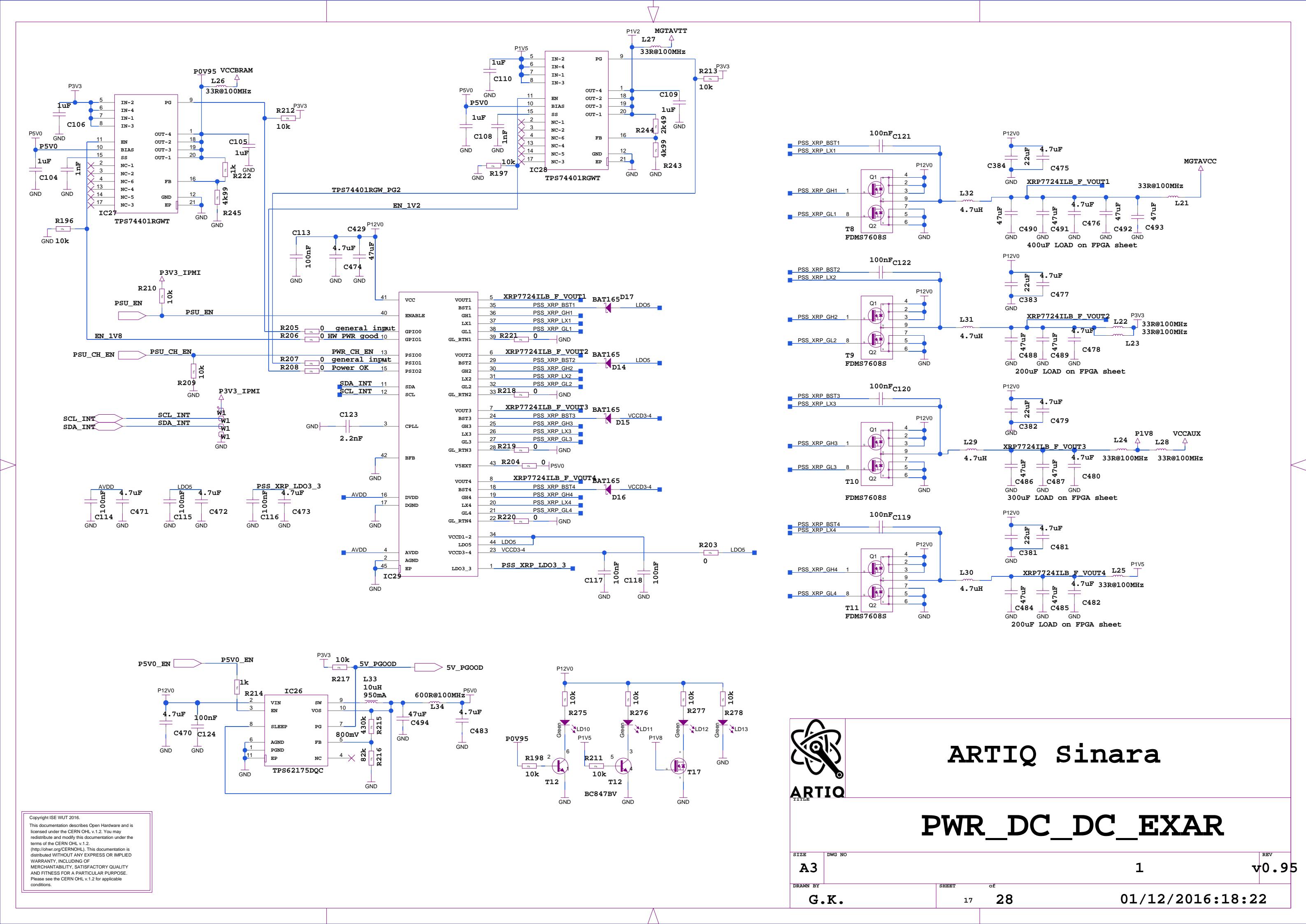
Power Supply			
Source	Voltage	Total (A)	
V _{CCINT}	0,900	9,165	
V _{CCINT} _IO	0,900	0,620	
V _{CCBRAM}	0,950	0,031	
V _{CCAU}	1,800	0,660	
V _{CCAU} _IO	1,800	0,546	
V _{CCO} 3.3V	3,300	0,000	
V _{CCO} 2.5V	2,500		
V _{CCO} 1.8V	1,800	0,380	
V _{CCO} 1.5V	1,500	0,936	
V _{CCO} 1.35V	1,350		
V _{CCO} 1.2V	1,200		
V _{CCO} 1.0V	1,000		
MGT _V CCAU	1,800	0,081	
MGT _V CC	1,000	3,038	
MGT _V TT	1,200	0,592	
-	-	-	
V _{CCADC}	1,800	0,014	

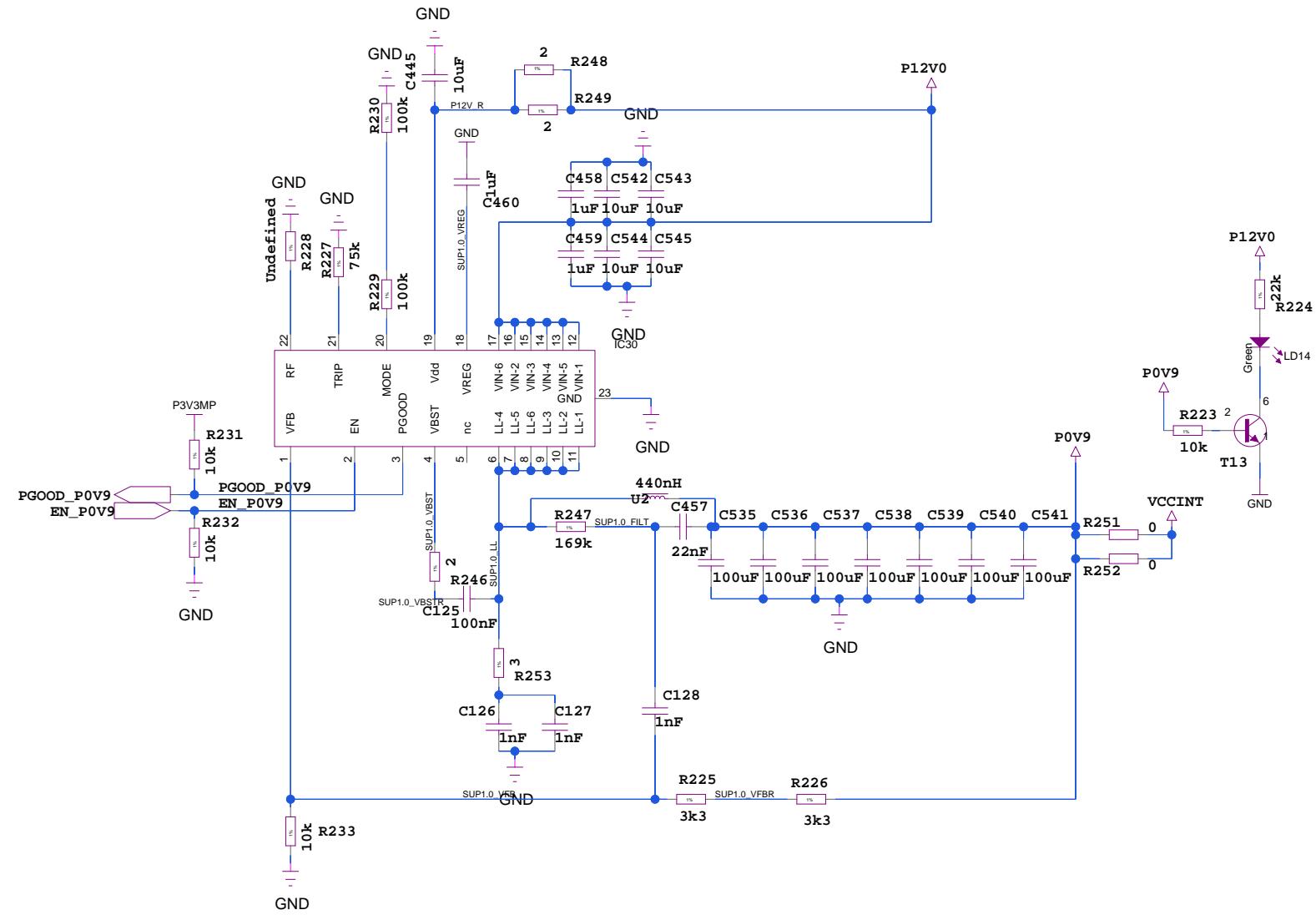


ARTIQ Sinara

POWER Management

Copyright ISE WUT 2016.
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2.
(http://ohwr.org/CERNohl). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions.

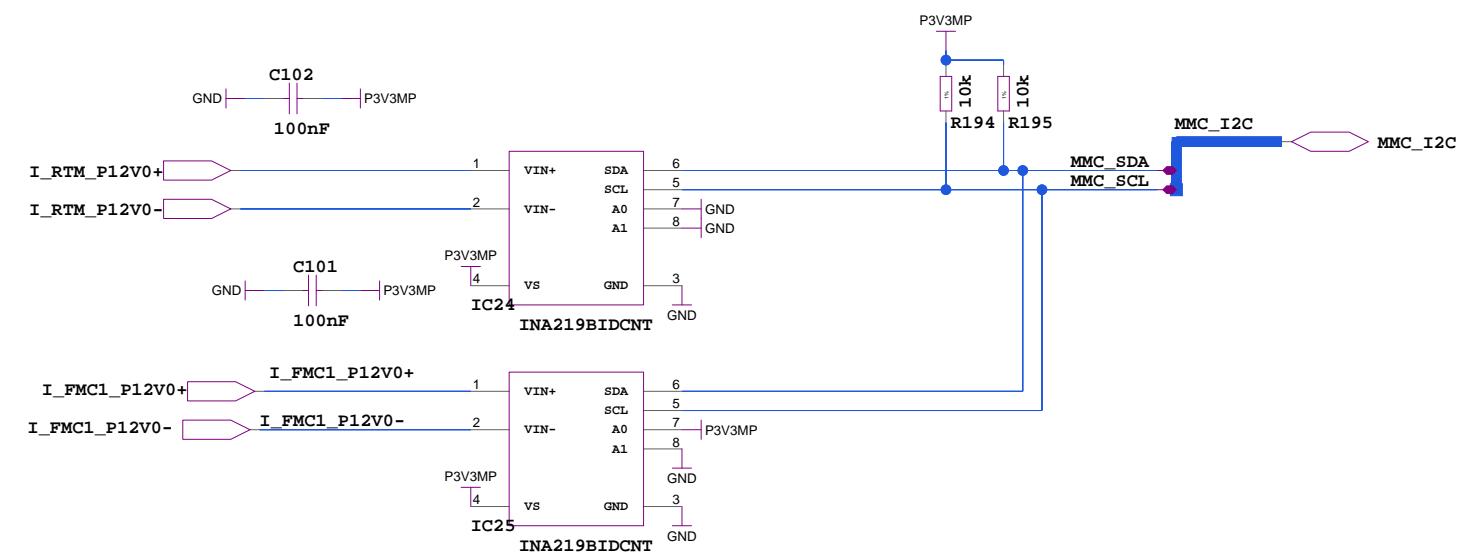




ARTIQ Sinara

PWR_0V9

Copyright ISE WUT 2016.
This documentation describes Open Hardware and is
licensed under the CERN OHL v.1.2. You may
redistribute and modify this documentation under the
terms of the CERN OHL v.1.2.
(<http://ohwr.org/CERNOHL>). This documentation is
distributed WITHOUT ANY EXPRESS OR IMPLIED
WARRANTY, INCLUDING OF
MERCHANTABILITY, SATISFACTORY QUALITY
AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.2 for applicable
conditions.



ARTIQ Sinara

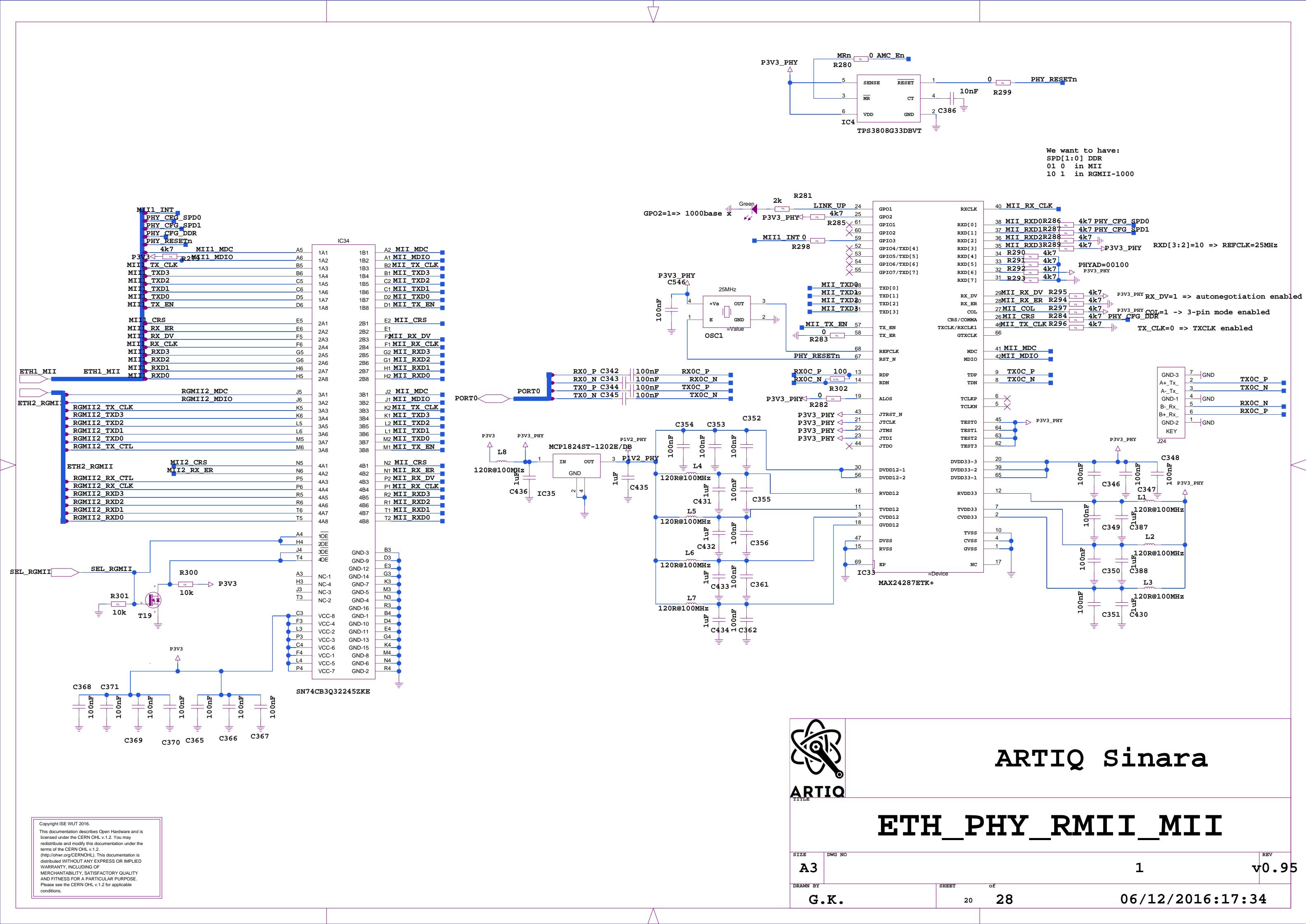
UI_mon

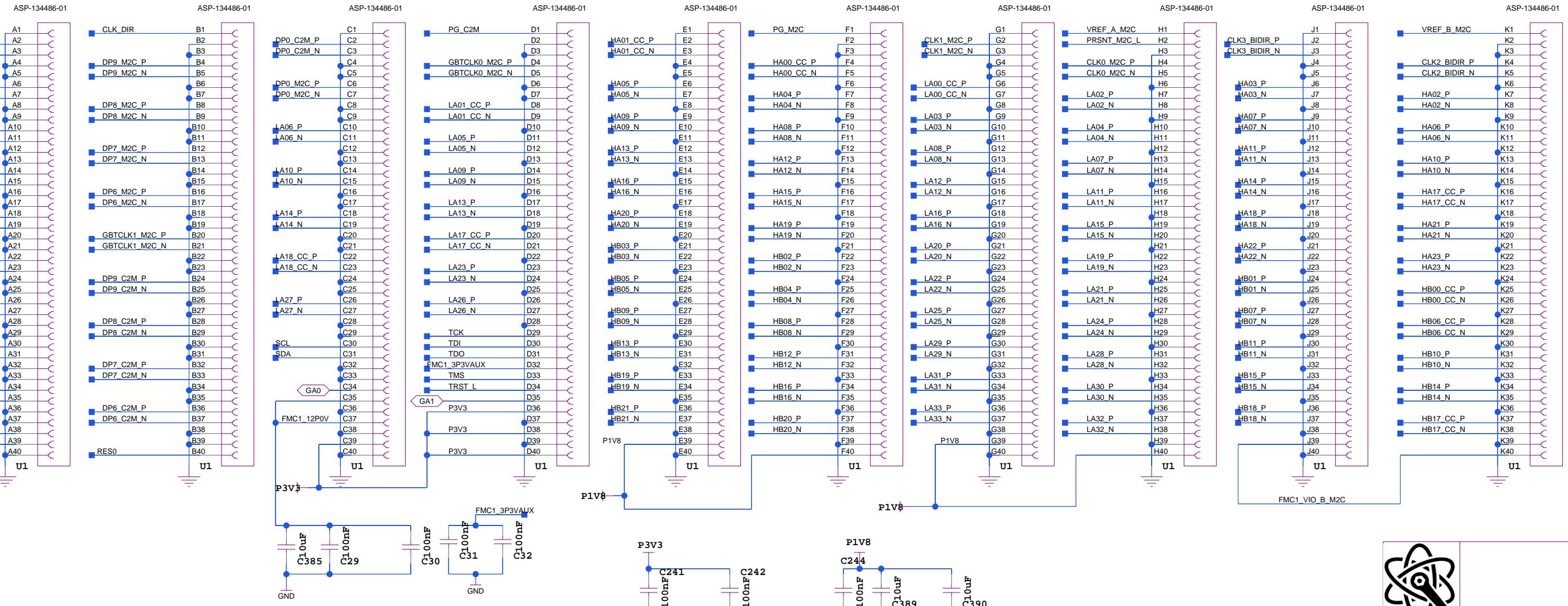
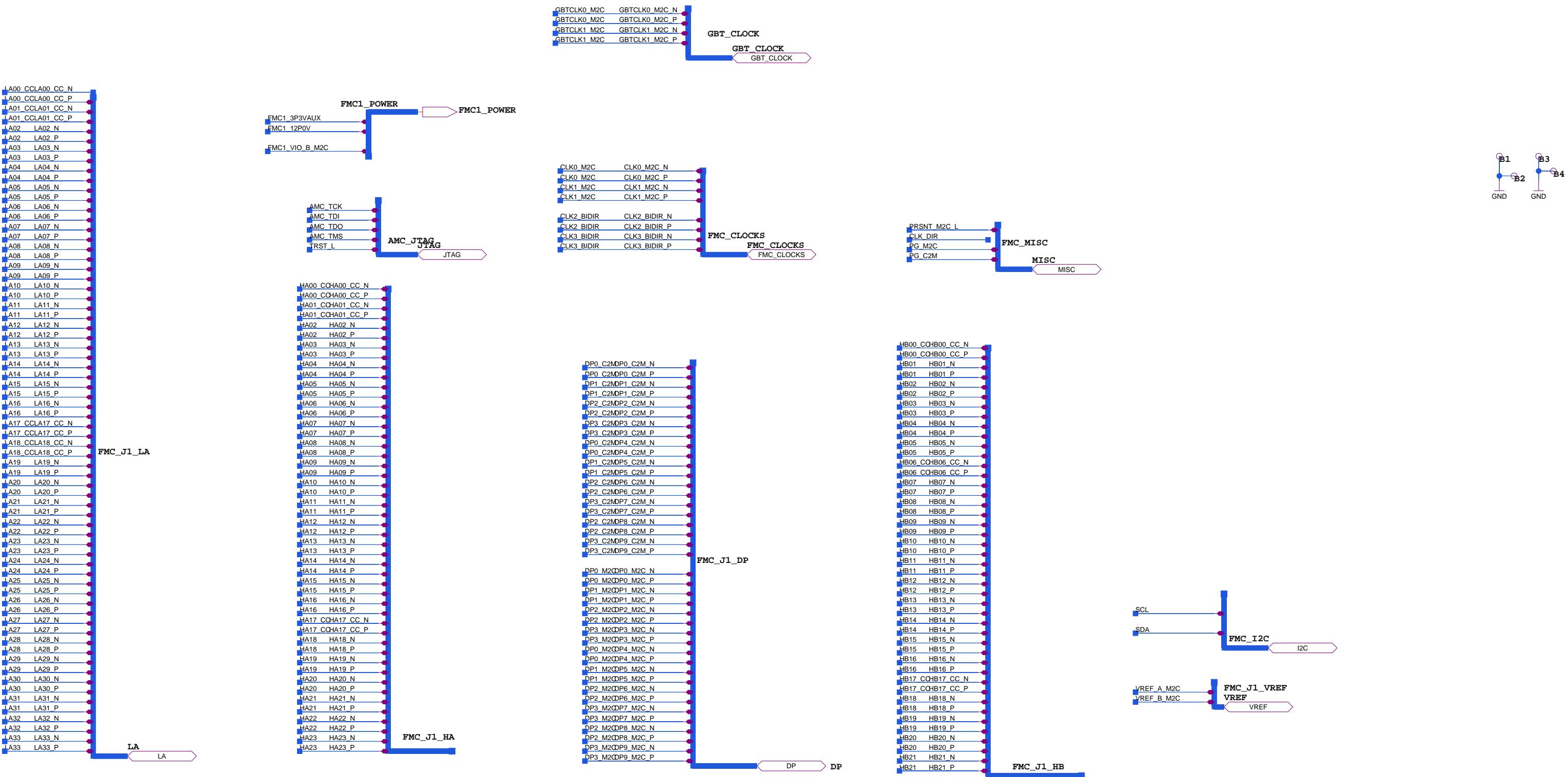
SIZE	DWG NO	REV
A3		v0.95
DRAWN BY	SHEET of	
G.K.	19	28

Copyright ISE WUT 2016.
This documentation describes Open Hardware and is
licensed under the CERN OHL v.1.2. You may
redistribute and modify this documentation under the
terms of the CERN OHL v.1.2.
(<http://ohwr.org/CERNOHL>). This documentation is
distributed WITHOUT ANY EXPRESS OR IMPLIED
WARRANTY, INCLUDING OF
MERCHANTABILITY, SATISFACTORY QUALITY
AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.2 for applicable
conditions.

CERN OHL v.1.2

01/12/2016:18:22



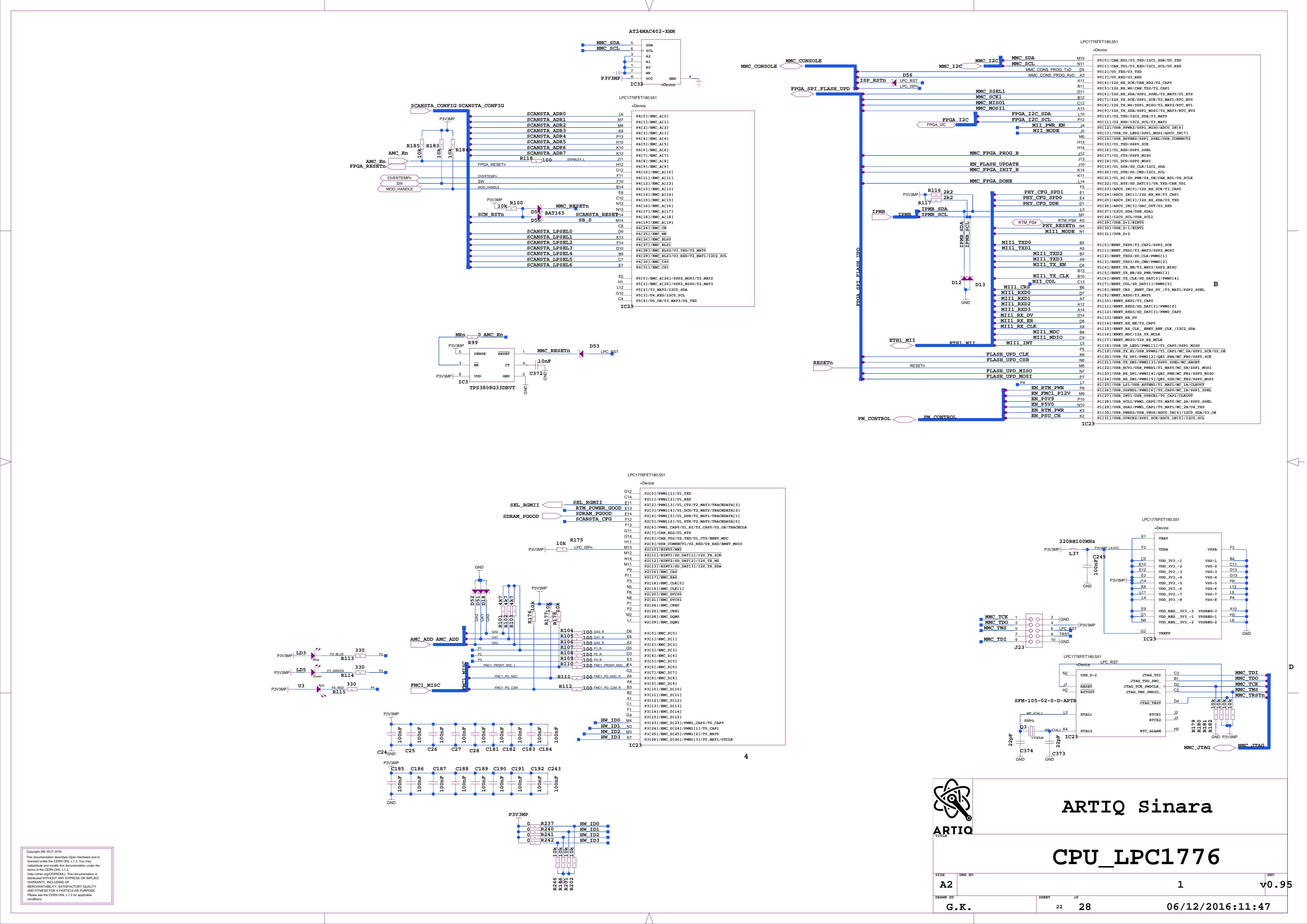


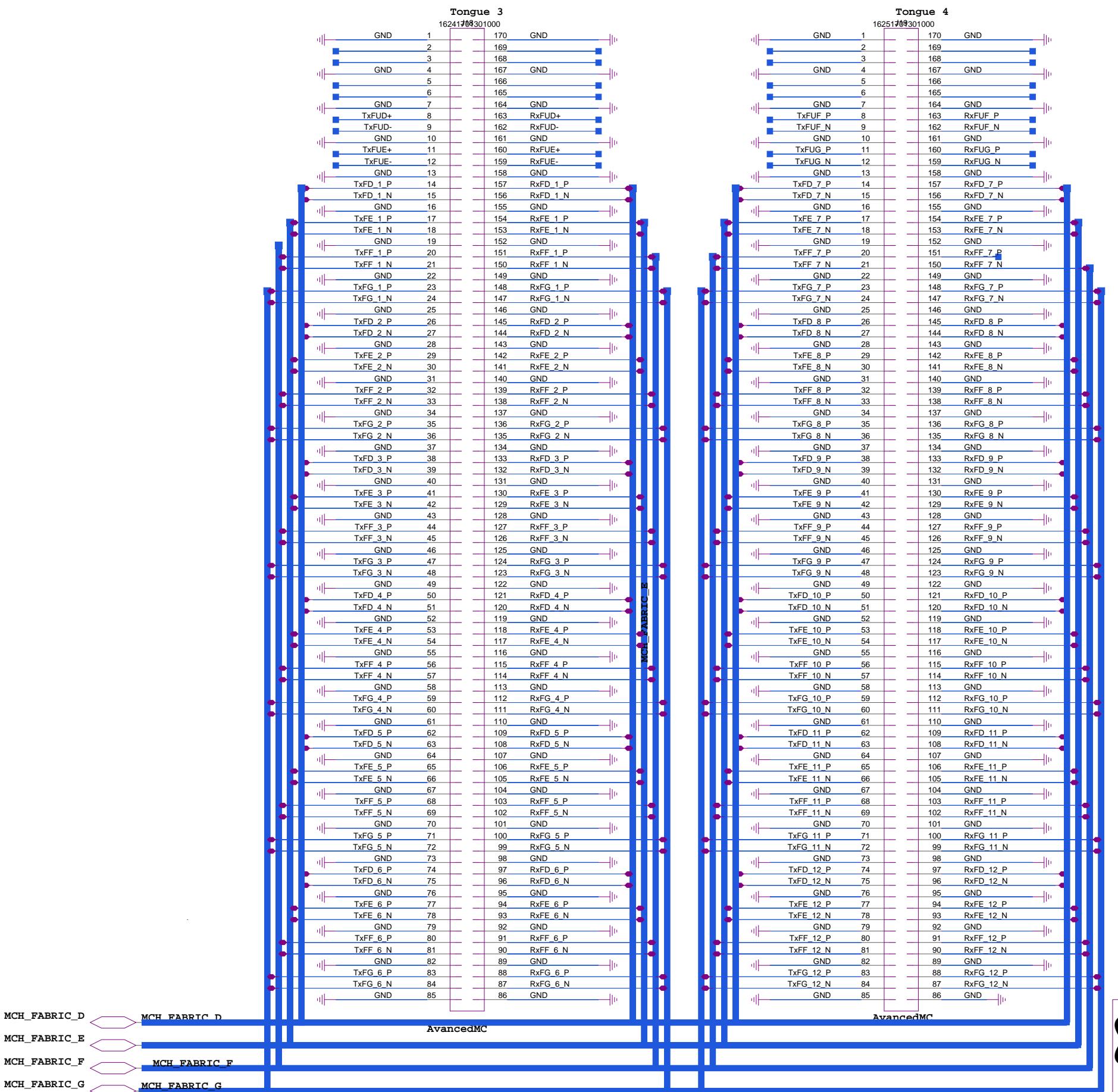
Copyright CERN 2012.
This documentation describes Open Hardware and is
licensed under the CERN OH v.1.1. You may
reproduce and modify this documentation under the
terms of the CERN OH v.1.1 license (available at
<http://cds.cern.ch/record/1300004>). This documentation is
distributed WITHOUT ANY EXPRESS OR IMPLIED
WARRANTY, INCLUDING THE IMPLIED WARRANTY OF
MERCHANTABILITY, SATISFACTORY QUALITY
AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OH v.1.1 for applicable
conditions.



ARTIQ Sinara

FMC_connector





Copyright ISE WUT 2016.
This documentation describes Open Hardware and is
licensed under the CERN OHL v.1.2. You may
reistribute and modify this documentation under the
terms of the CERN OHL v.1.2.
<http://cernohl.readthedocs.io>. This documentation is
described WITHOUT ANY EXPRESS OR IMPLIED
WARRANTY, INCLUDING OF
MERCHANTABILITY, SATISFACTORY QUALITY
AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.2 for applicable
conditions.



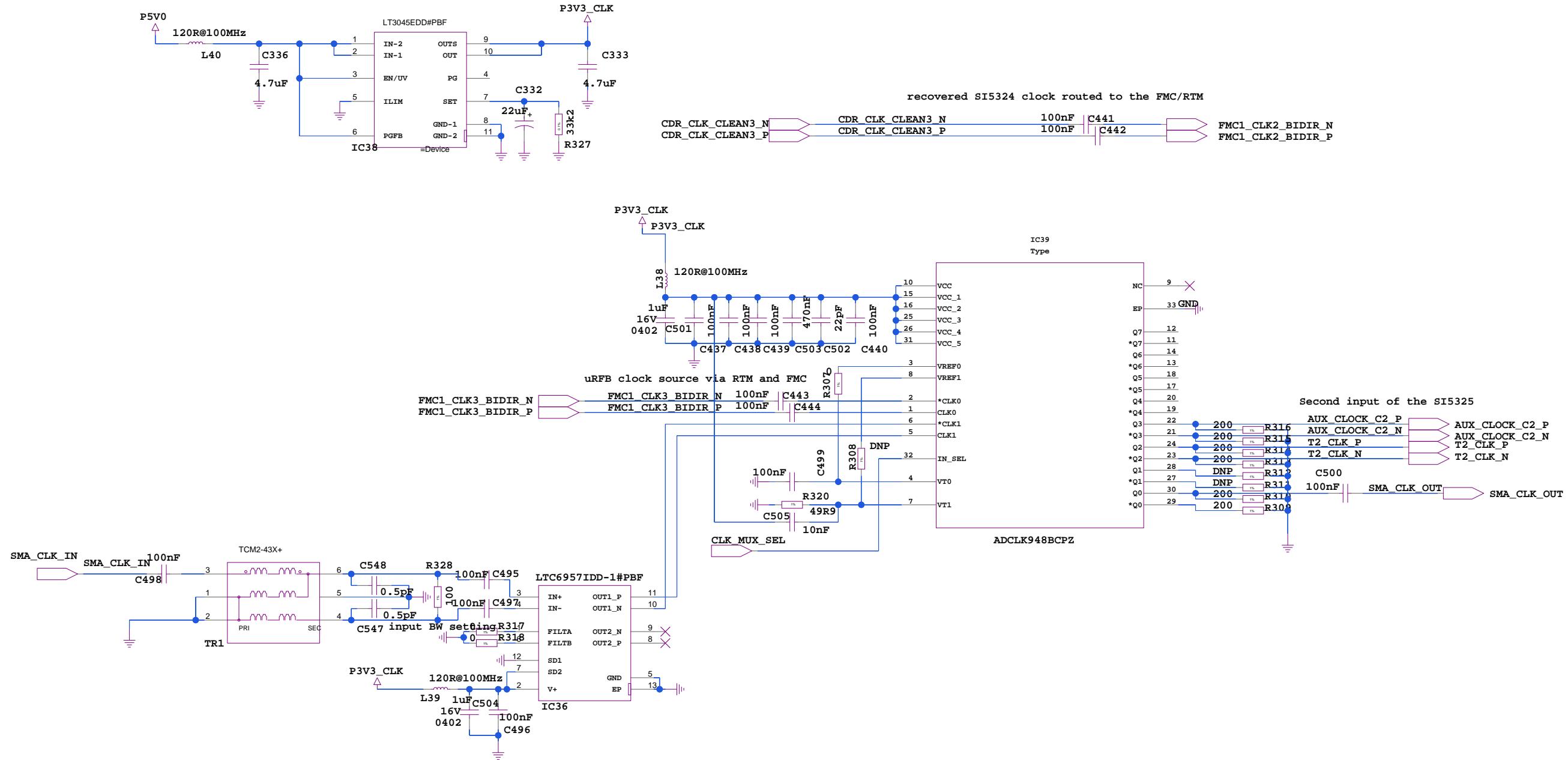
ARTIQ Sinara

MCH_CON

SIZE DWG NO
A3
DRAWN BY G.K.
SHEET 23
of 28
REV v0.95

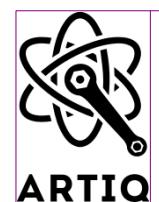
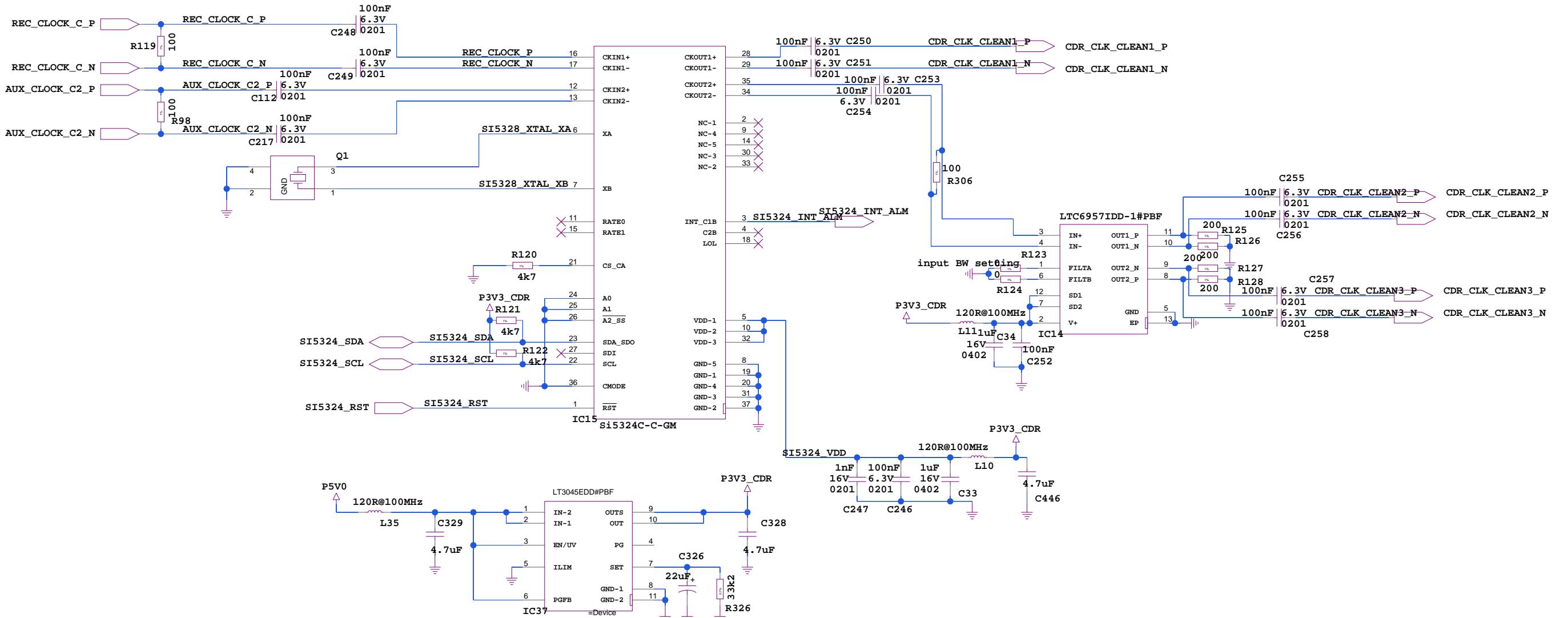
1

01/12/2016:18:22



 MeSi.no_CLK_Distribution
ARTIQ
 TITLE

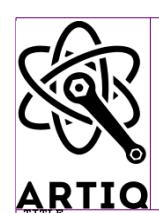
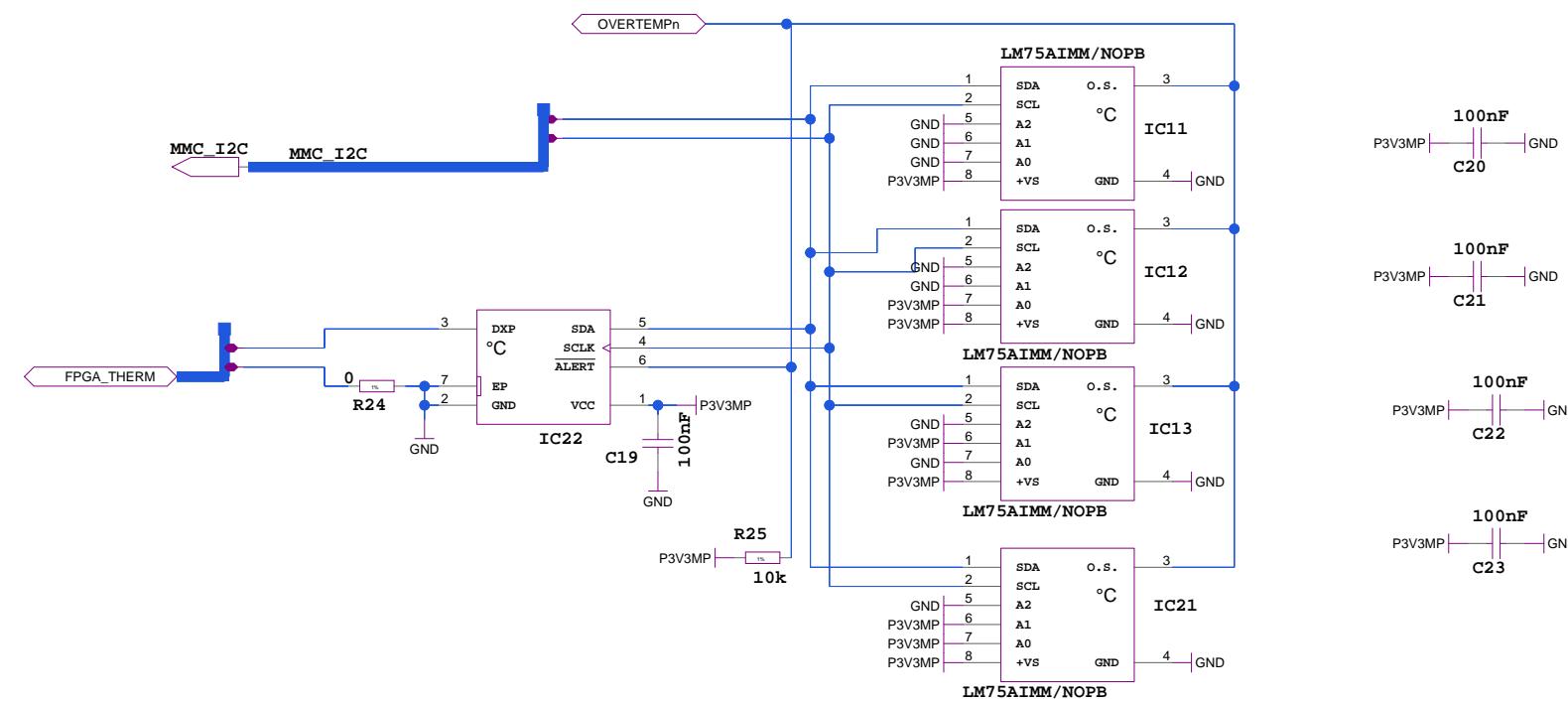
ARTIQ Sinara



ARTIQ Sinara

SI5324_CLK_RECOVERY

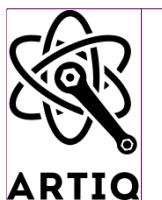
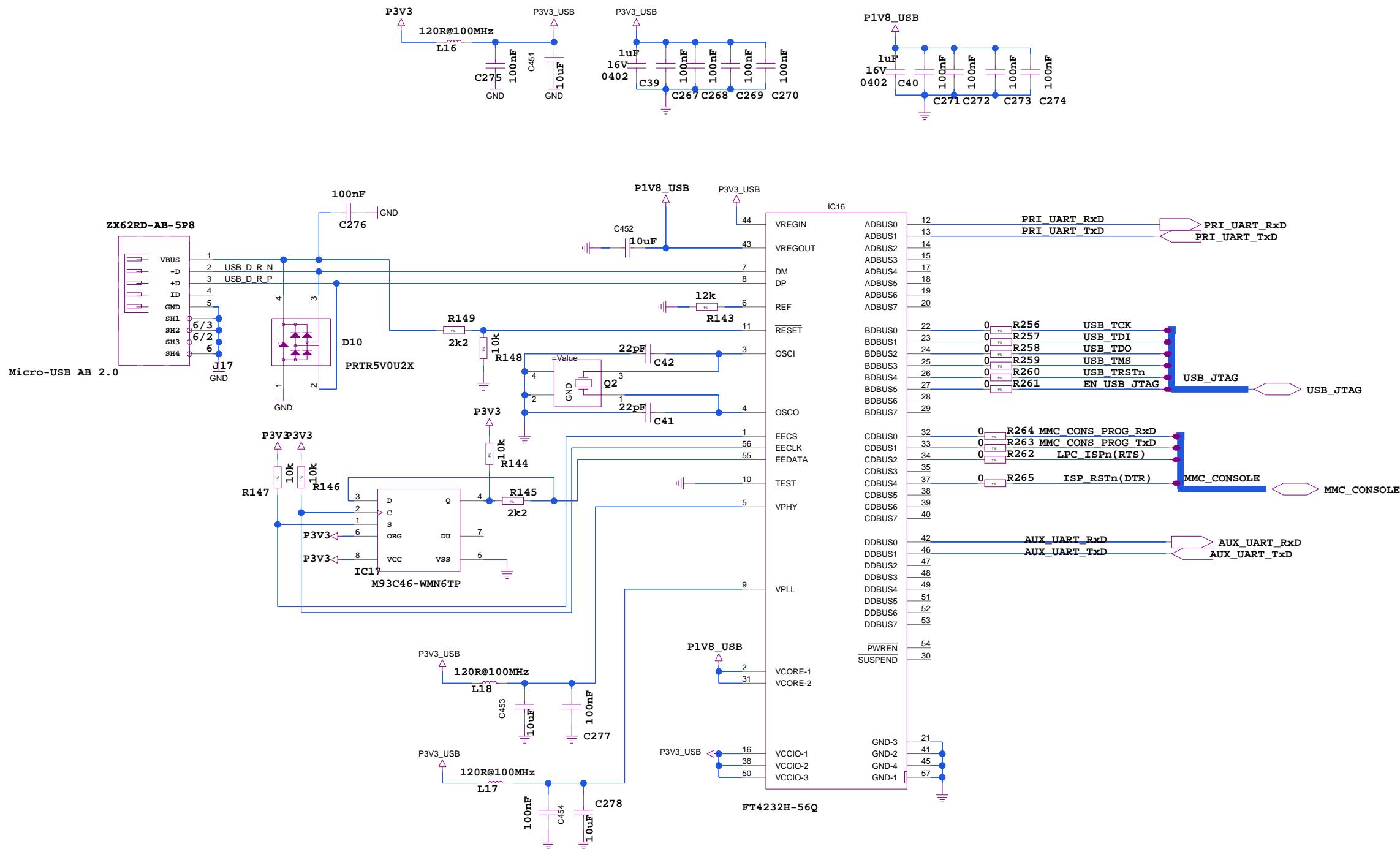
SIZE	DWG NO	REV
A3		v0.95
DRAWN BY	SHEET of	
G.K.	25	28



ARTIQ Sinara

Thermometers

Copyright ISE WUT 2016.
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2.
<http://ohwr.org/CERNOHL>. This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.2 for applicable conditions.



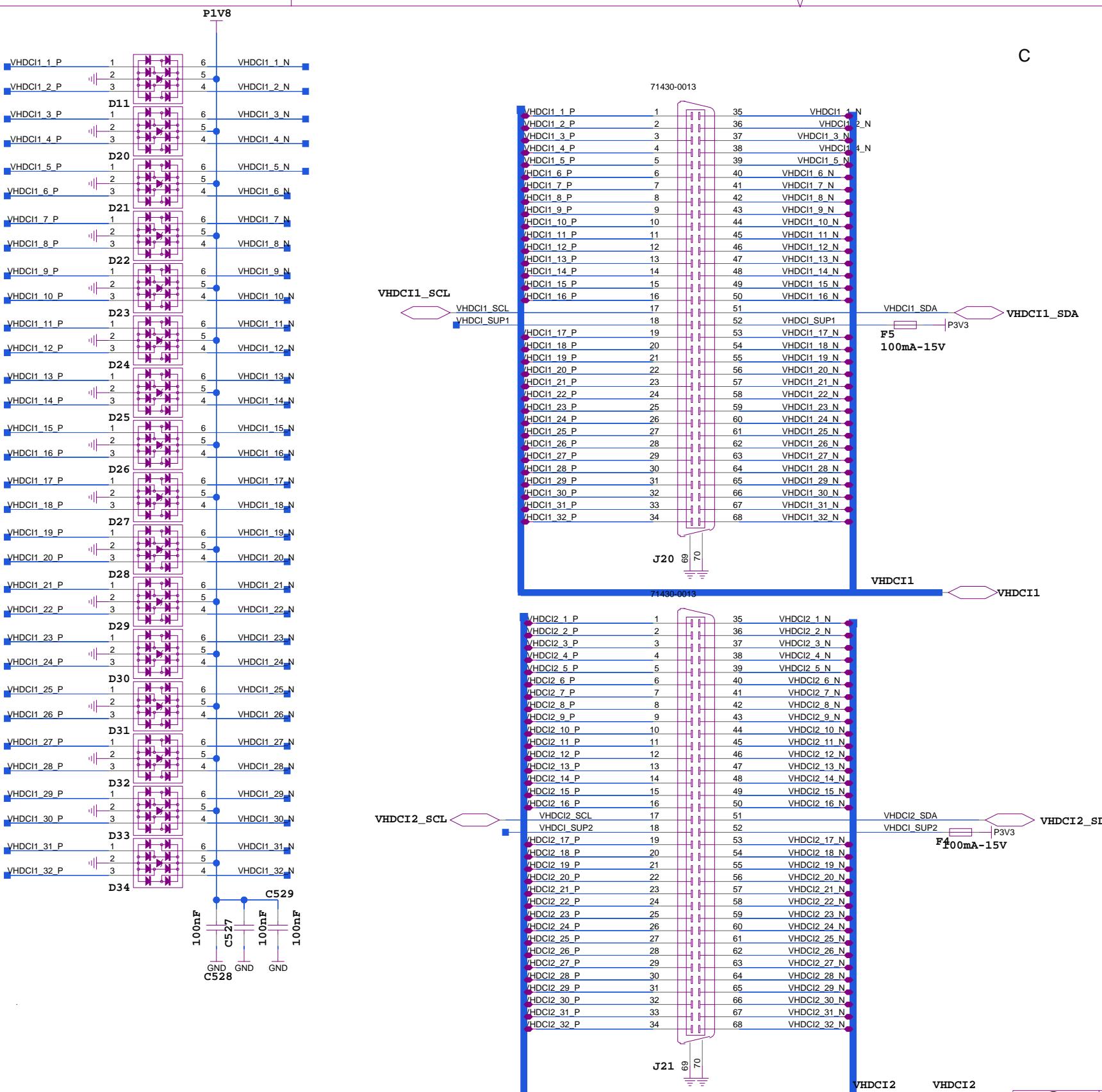
ARTIQ Sinara

USB_SERIAL_QUAD

Copyright ISE WUT 2016.
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2.
(<http://cswr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions.

SIZE	DWG NO	REV
A3		v0.95
DRAWN BY		1
SHEET 28		of 1
03/12/2016:15:08		

C



ARTIQ Sinara

SIZE A3

DWG NO

DRAWN BY G.K.

SHEET 28

OF 28

REV v0.95