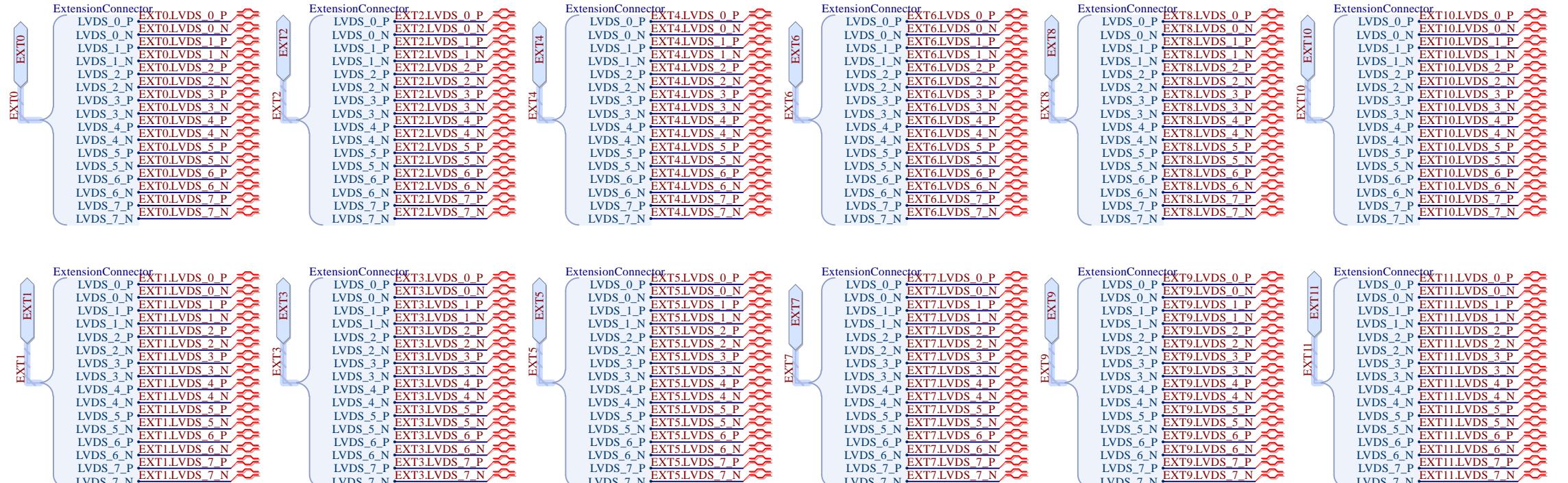
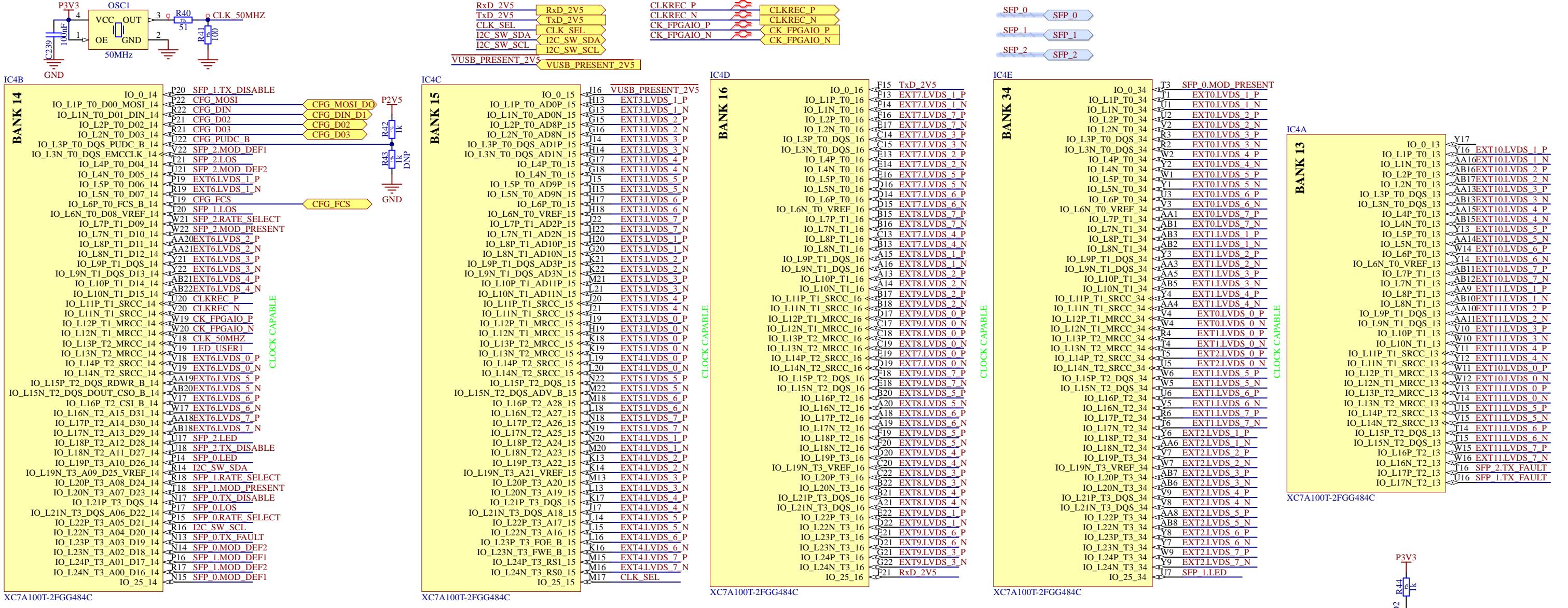


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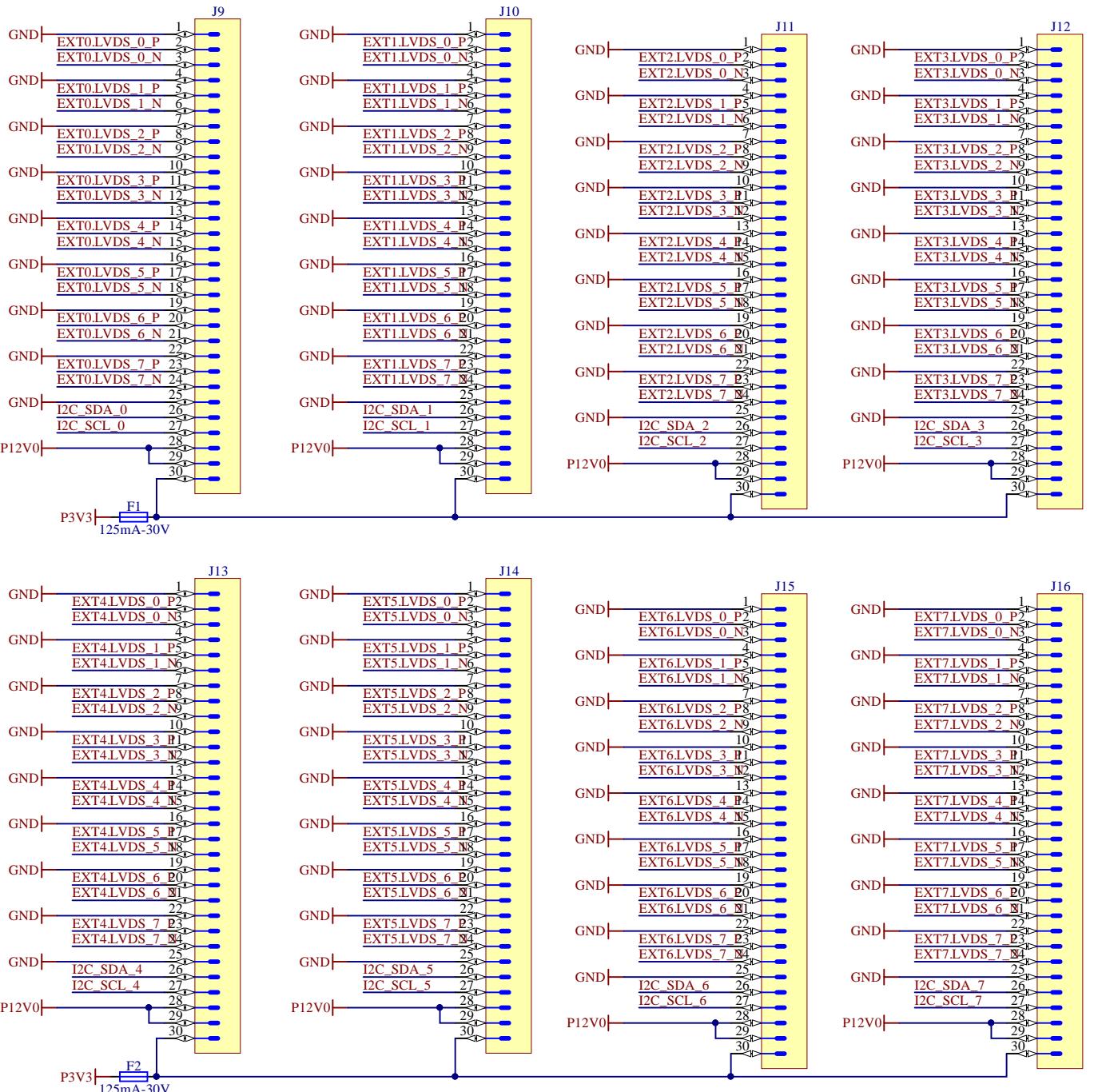
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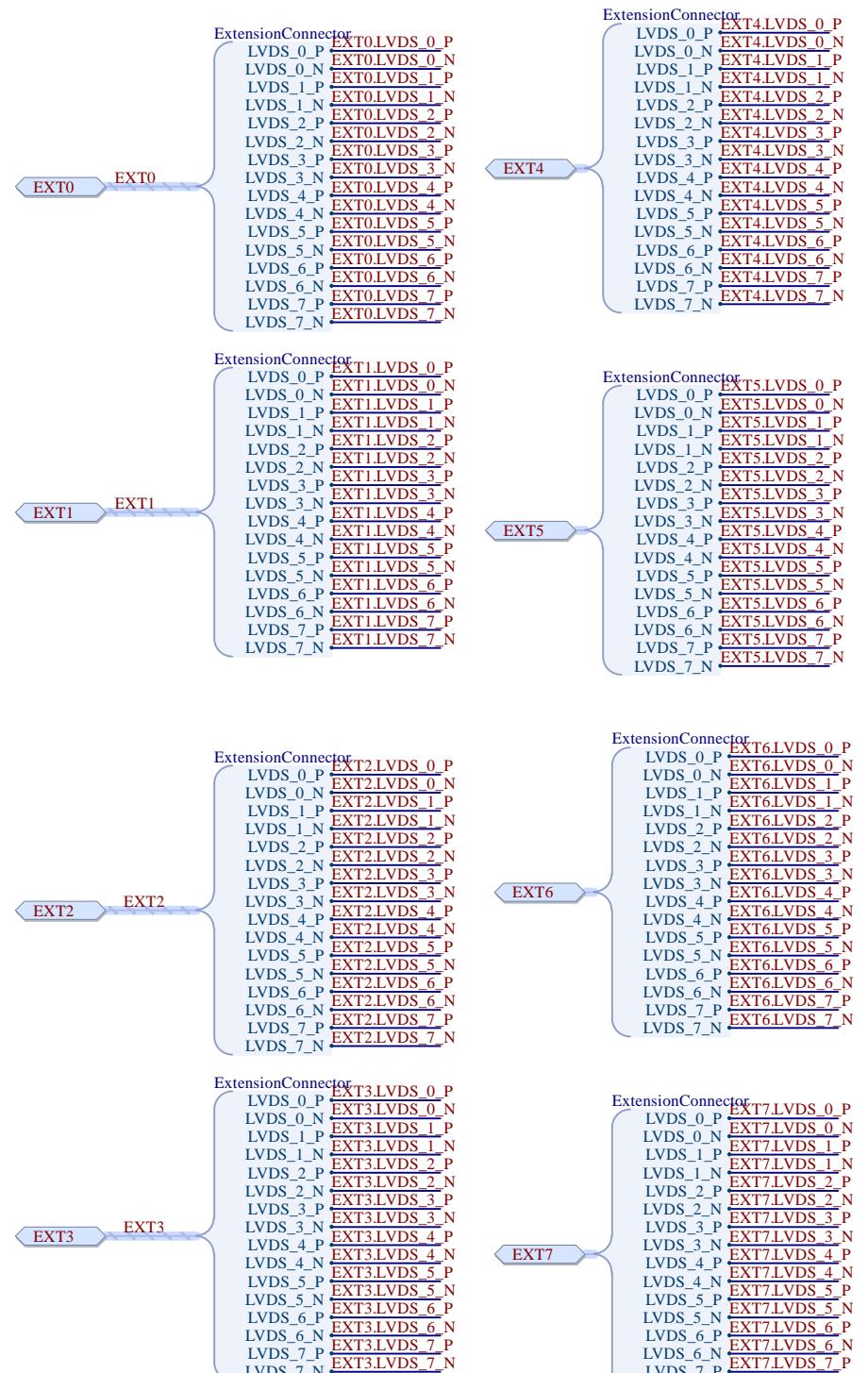
FPGA schdoc

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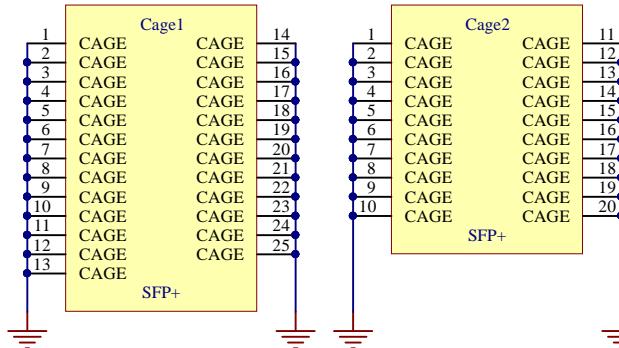
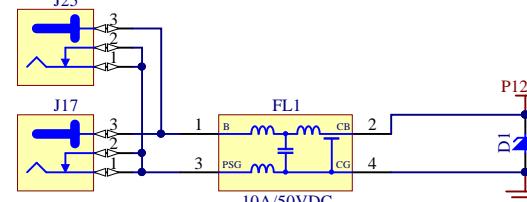


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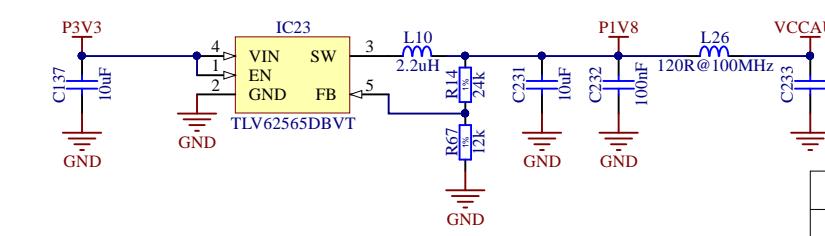
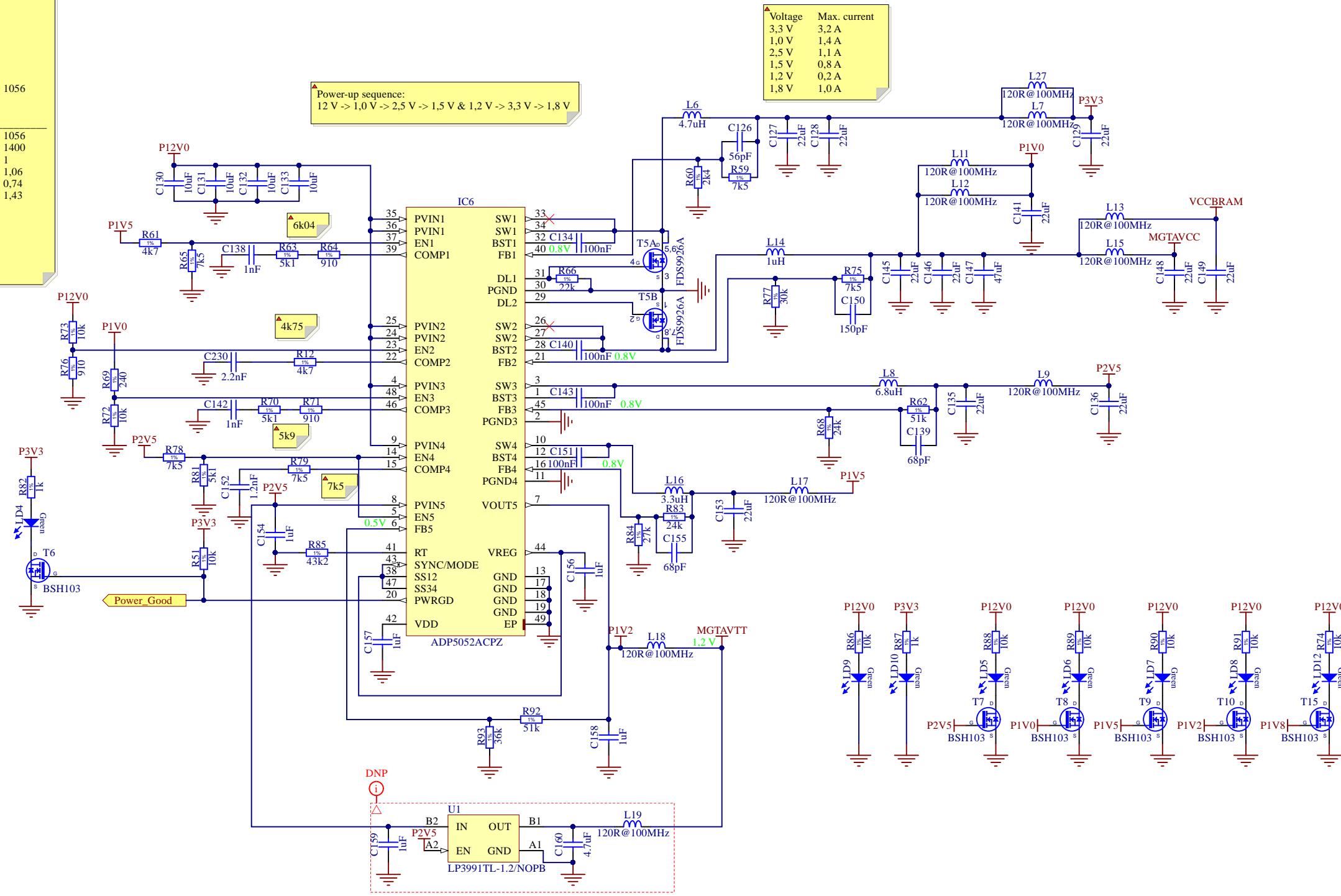
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Warsaw University of Technology ISE Nowowiejska 15/19			
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	P3V3	P2V5	P1V8	LDO P1V5	P1V2	P1V0
LED SFP1-3	27					
LED user1, power good, fpga done, 3V3 LED	12					
Any Frequency Clock Multiplier/						
Jitter Attenuator	Si5324	279				
Clock Fanout Buffer	ADCLK944B	138				
Clock Fanout Buffer	ADCLK948B	330				
Extensions, powered by Kasli (I2C power) x12		240				
DDR Termination Regulator	TPS51200	40				
SFP+ 6.25gb 3x		900				
Level-Shifting I2C Repeater	TCA9517 x4	20				
I2C Switch	TCA9548	80				
Level-Shifting Bus Transceiver	SN74AVC2T245 x9	216				
Temperature Sensor	MAX6642	5				
50 MHz Oscillator	636L3I050M00000	25				
FPGA memory	S25FL128SAGBHIA 100					
RAM x16, rev E	MT41K256M16					
Artix 7 FPGA	XCTA100T					
LDO 1V2						
1V8 buck	TLV62565	332				
SUM [mA]	2911	698	542	429	167	1056
Current available [mA]	3500	1100	1000	800	200	1400
Voltage [V]	3,3	2,5	1,8	1,5	1,2	1
POWER [W]	9,61	1,75	0,98	0,64	0,20	1,06
Efficiency	0,88	0,78	0,89	0,76	1	0,74
POWER [W]	10,92	2,24	1,10	0,85	0,20	1,43
Total power: 16,82 W						
Total P12V0 current: 1,29 A						
Maximum P12V0 current: 5 A						
P12V0 current left for EEMs: 3,71 A						
Maximum P12V0 EEM current via ribbon cable: 1 A						



Power-up sequence:
12 V > 1,0 V > 2,5 V > 1,5 V & 1,2 V > 3,3 V > 1,8 V

Voltage	Max. current
3,3 V	3,2 A
1,0 V	1,4 A
2,5 V	1,1 A
1,5 V	0,8 A
1,2 V	0,2 A
1,8 V	1,0 A



Project/Equipment ARTIQ/SINARA

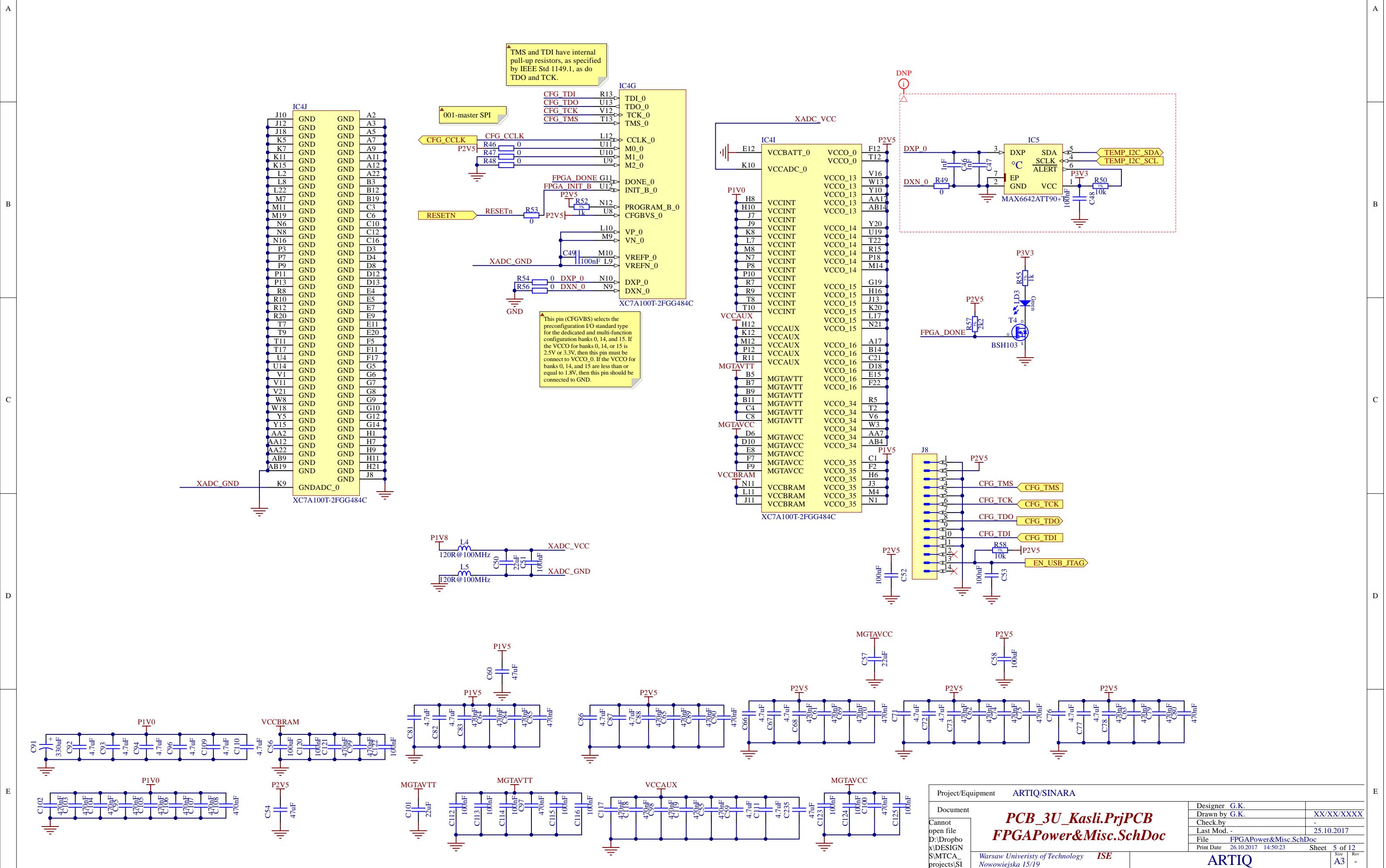
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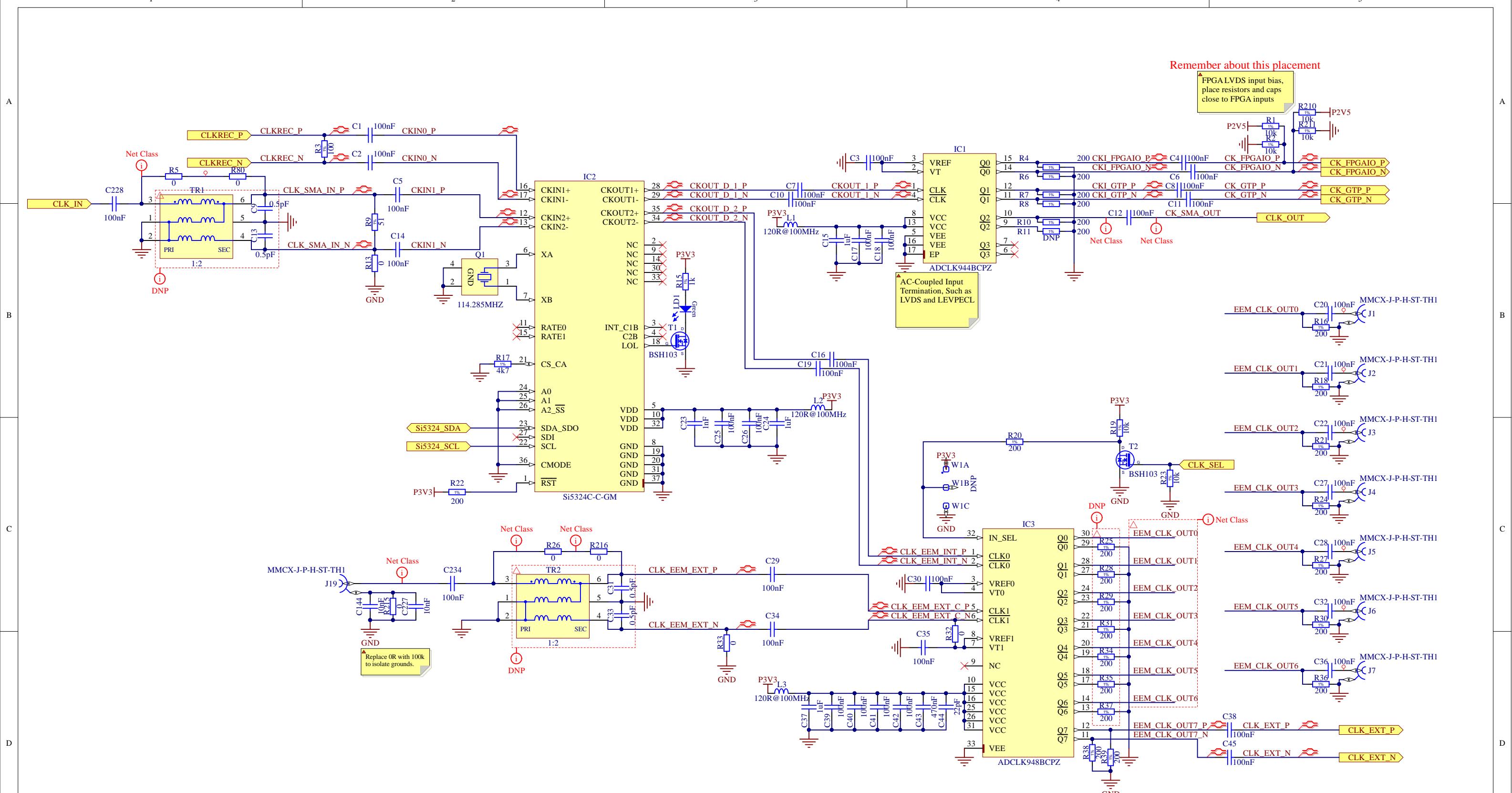
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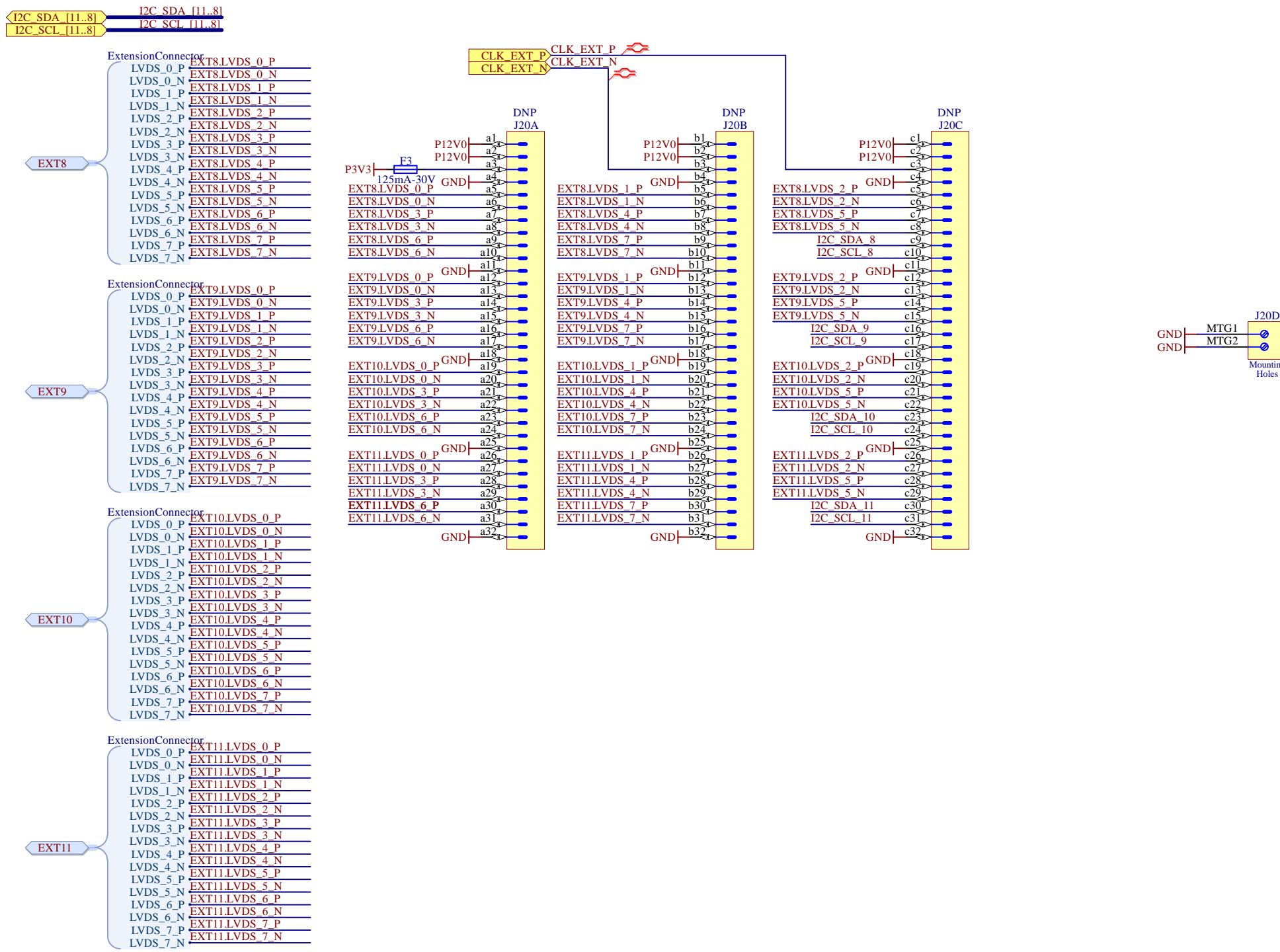
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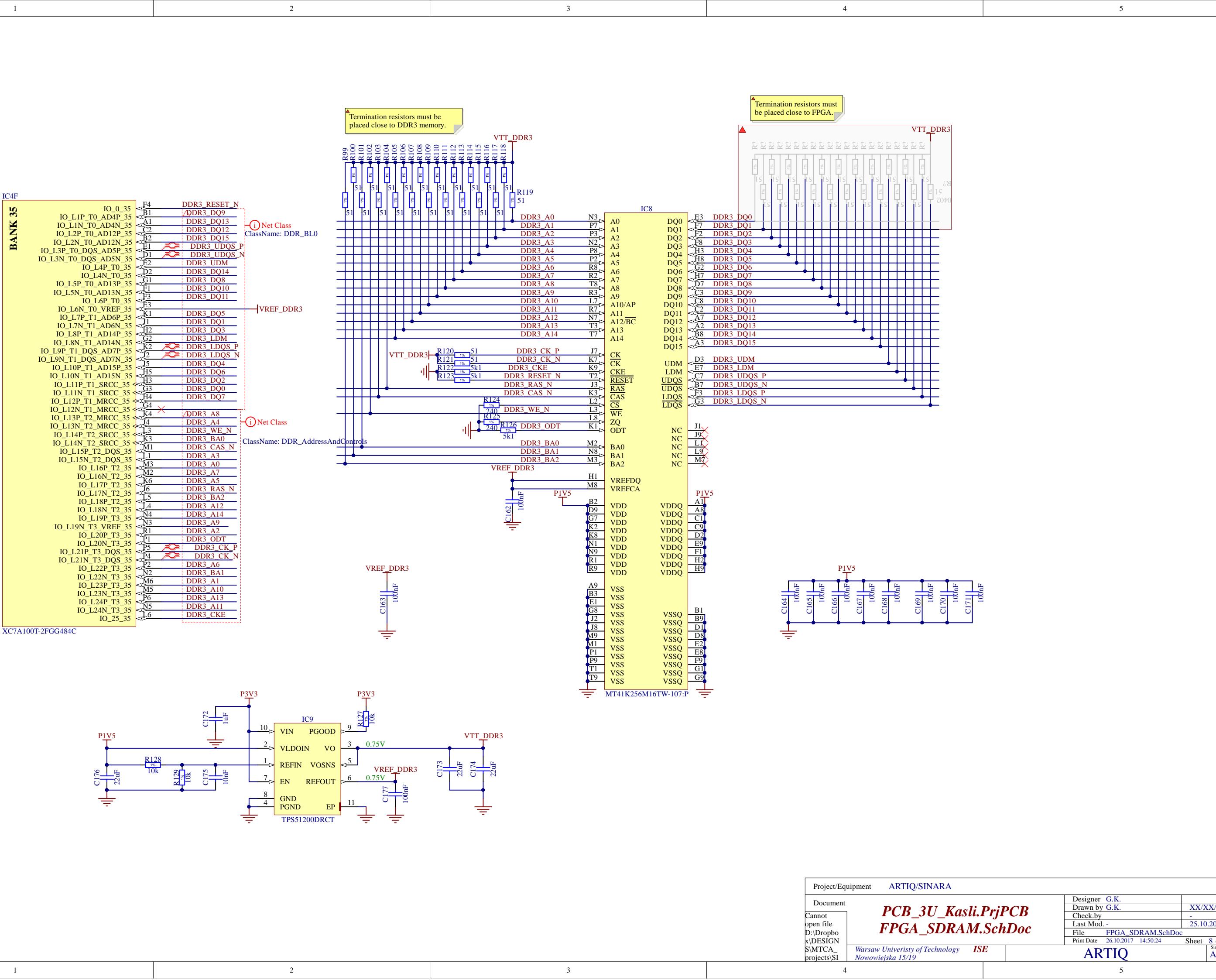


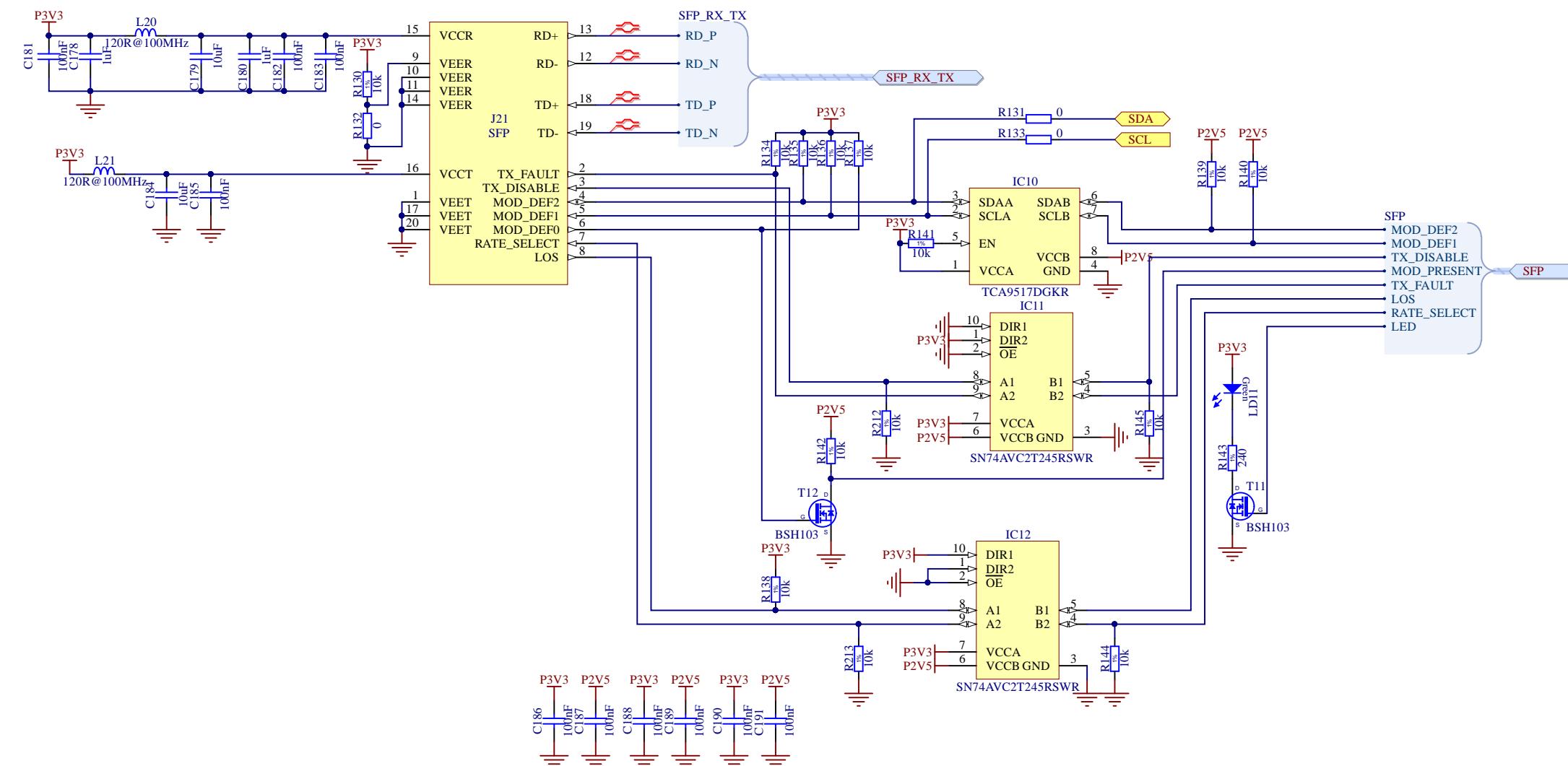


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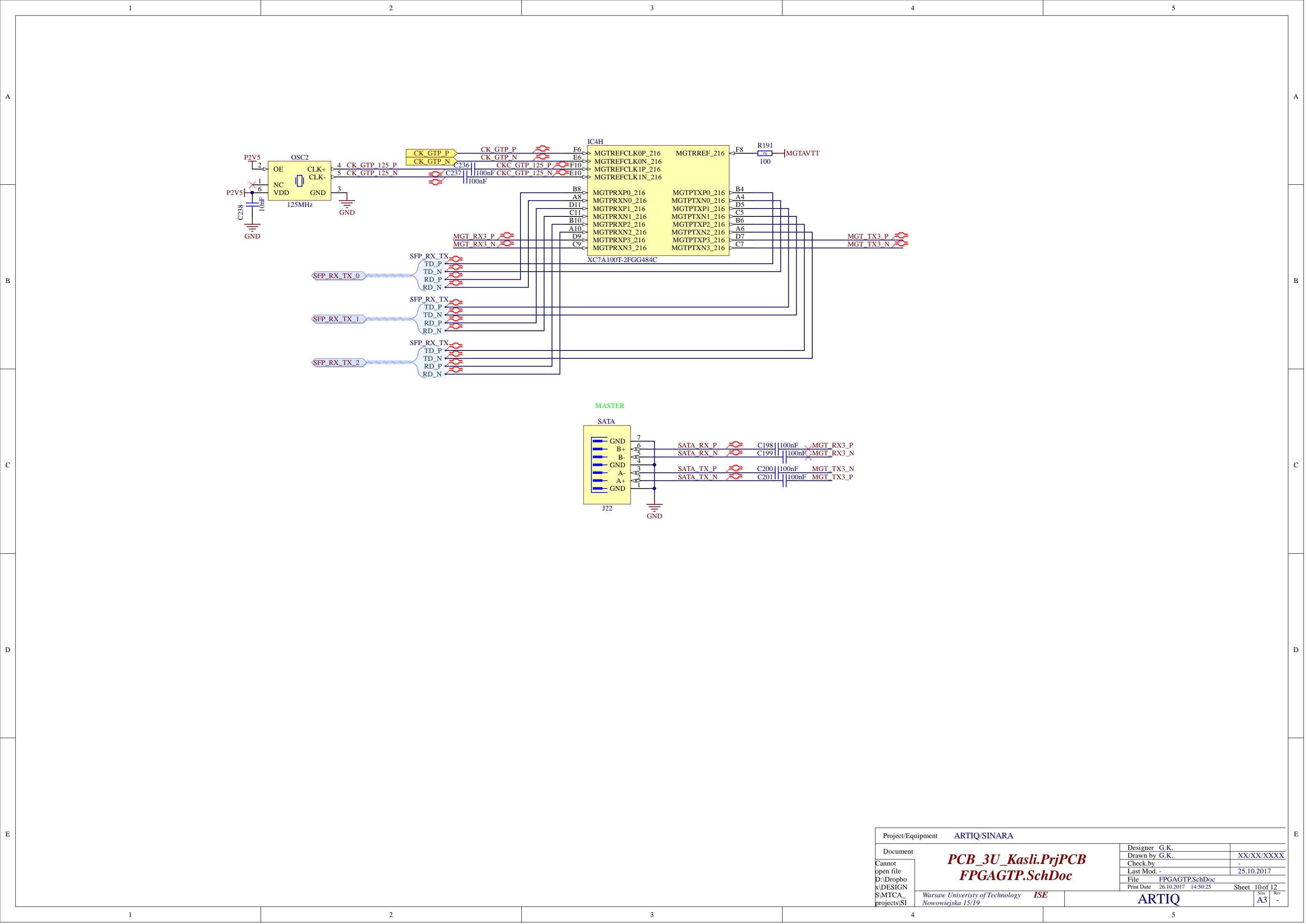


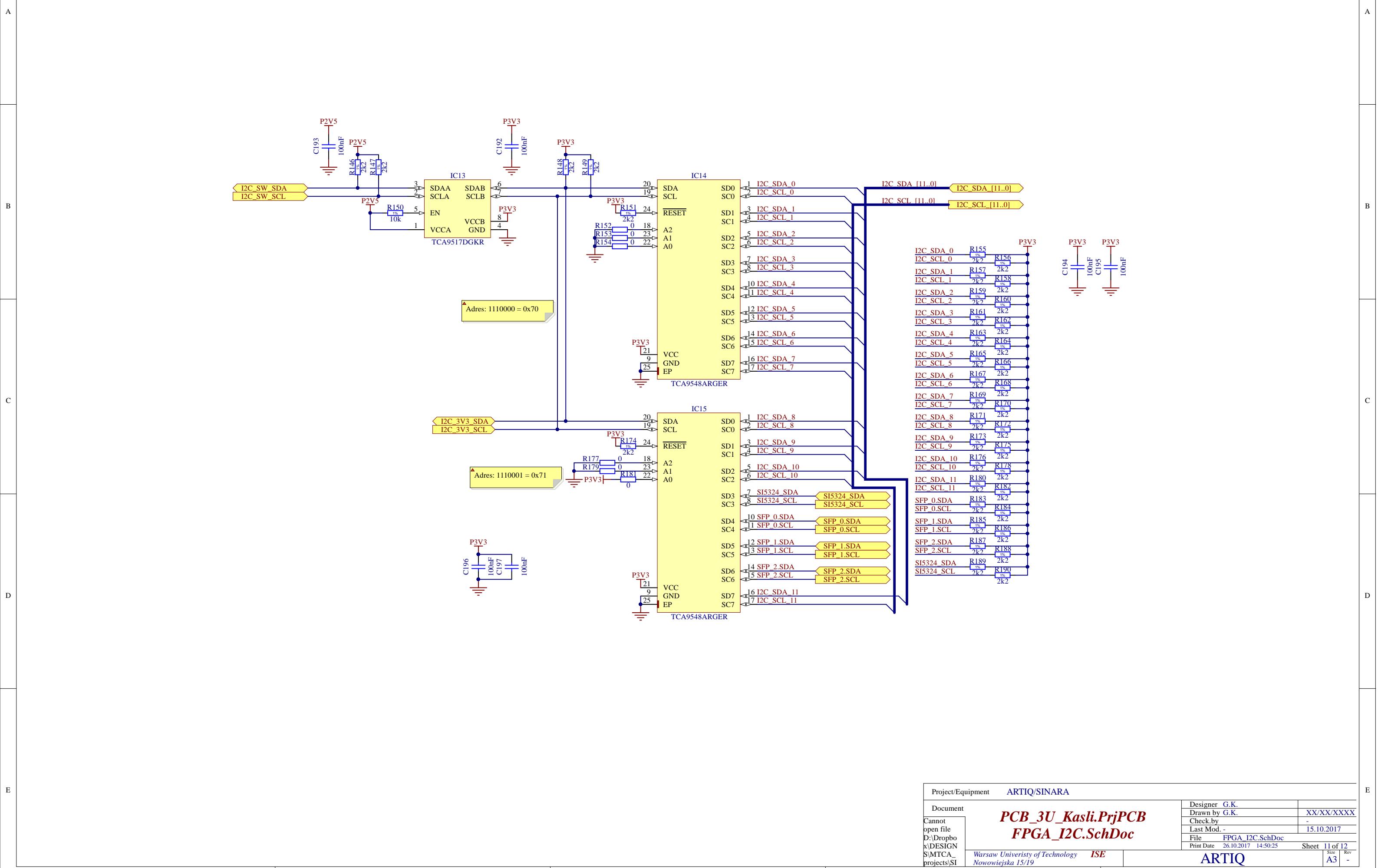
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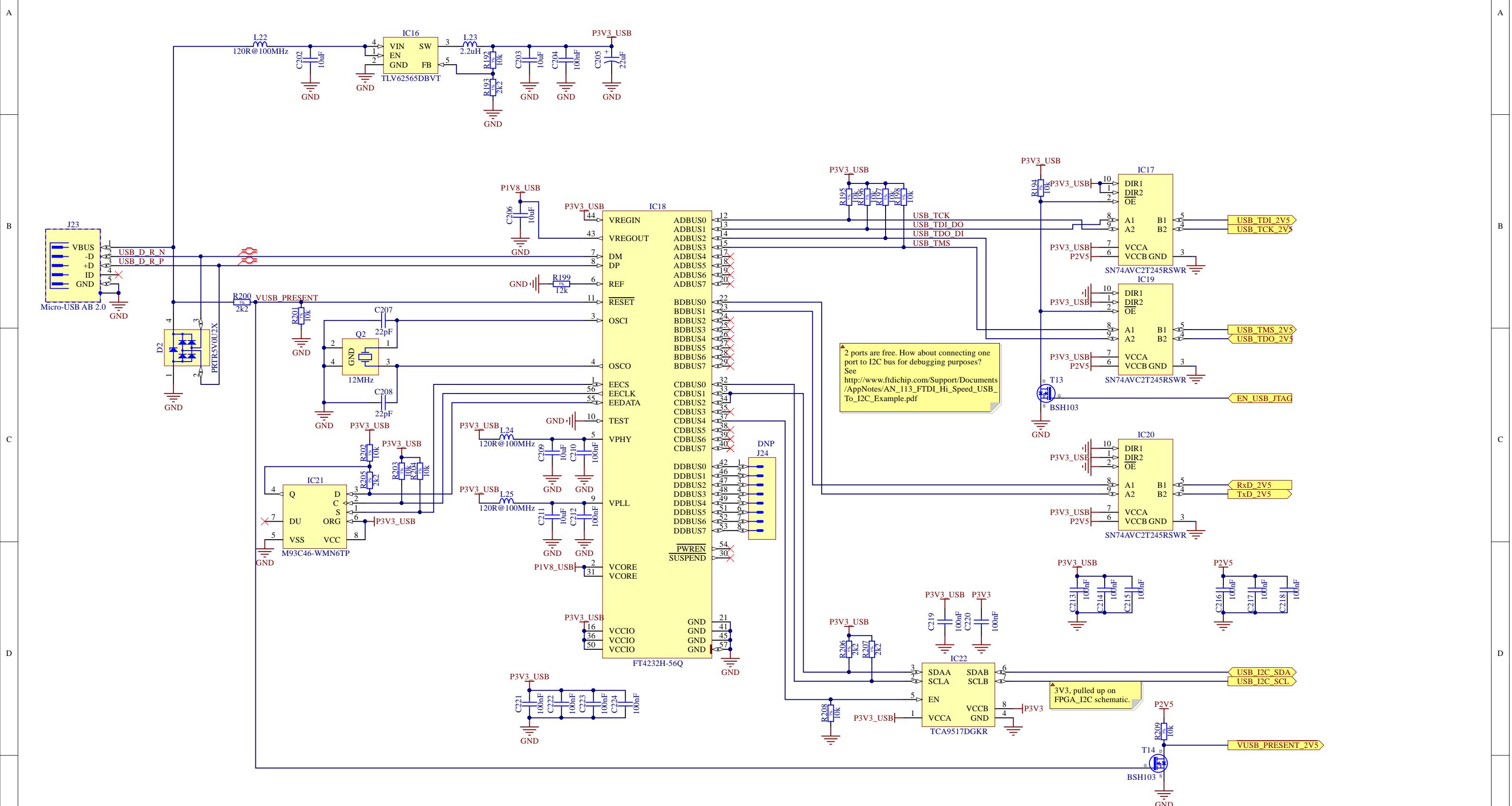


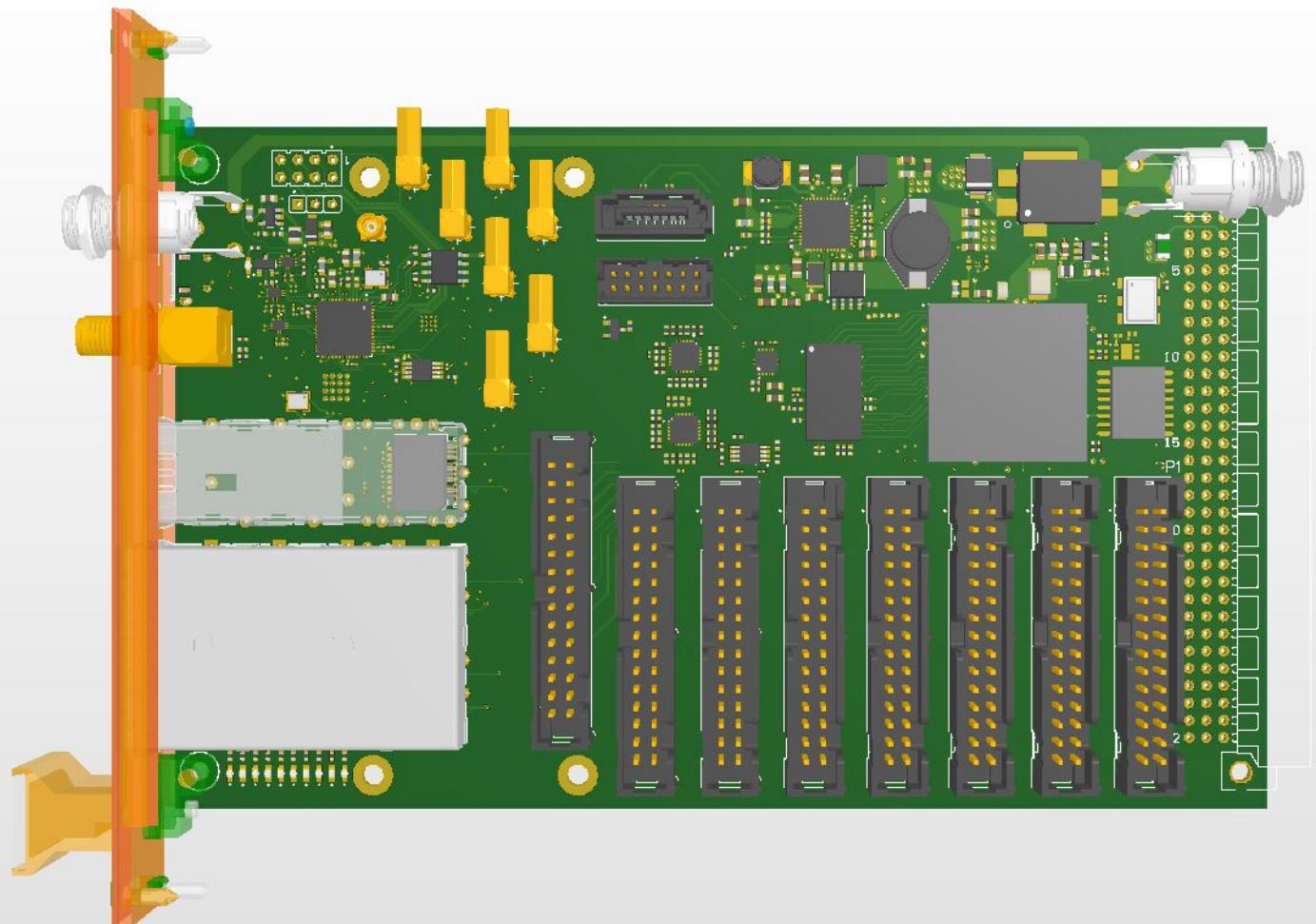


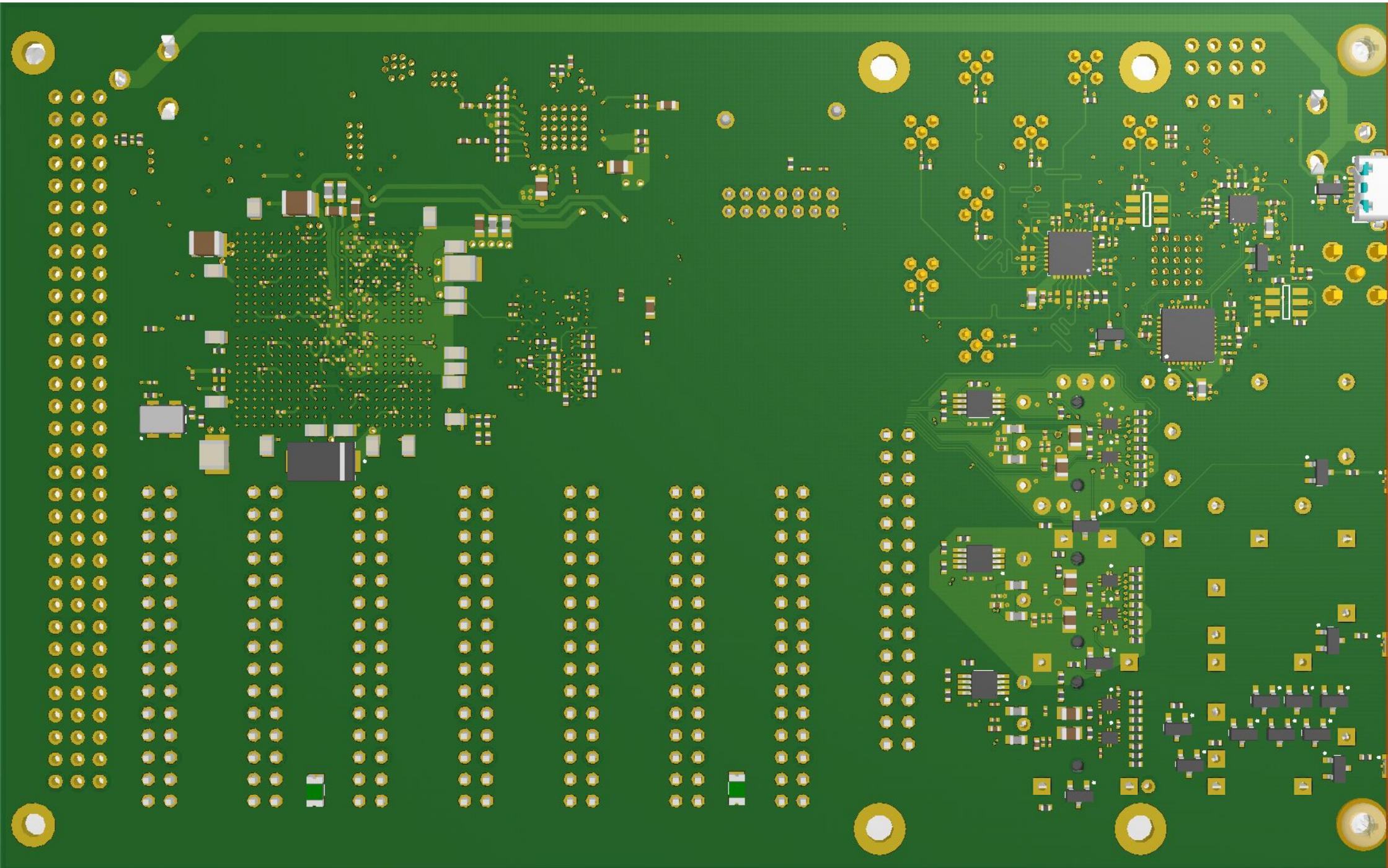
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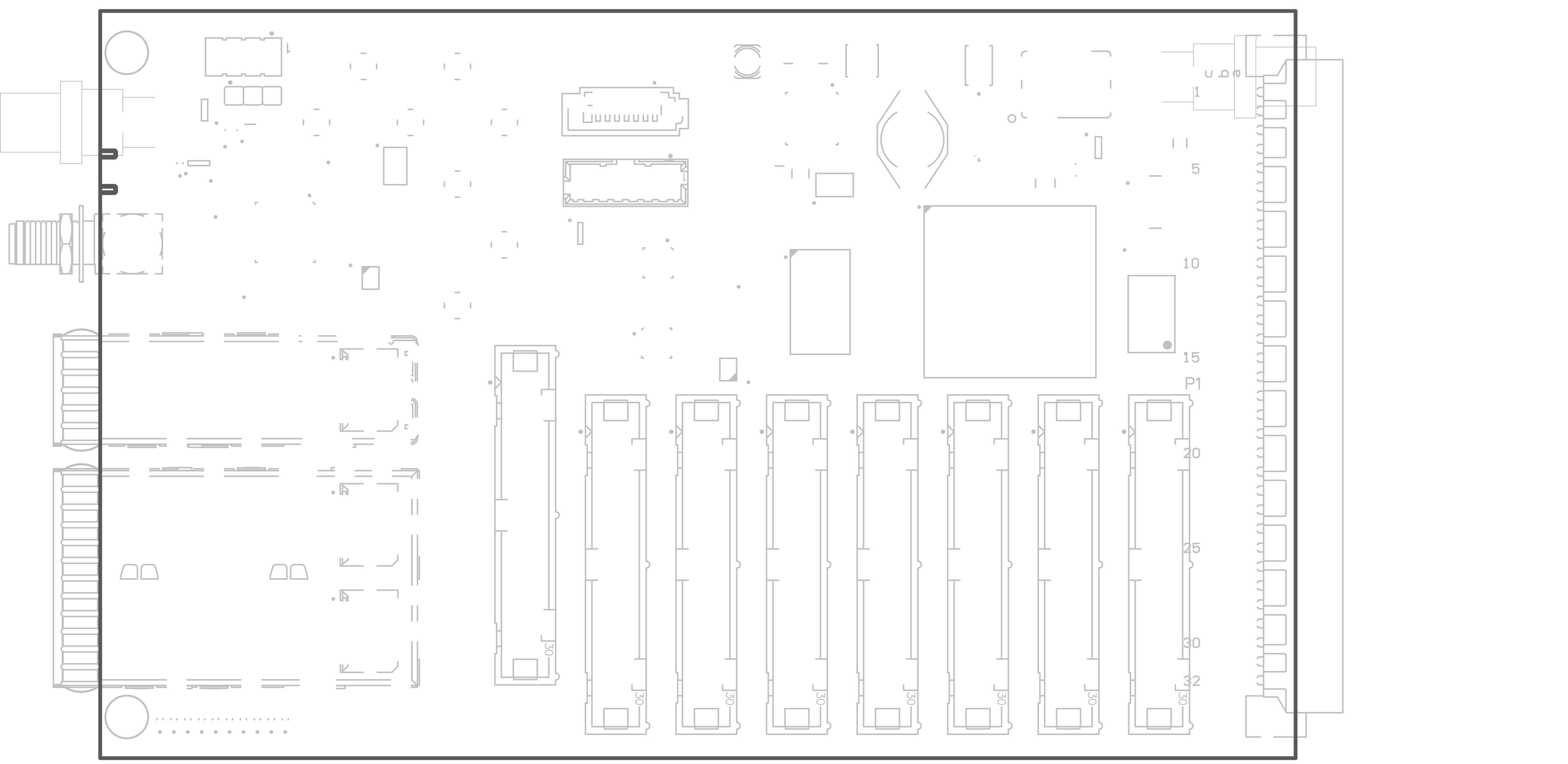


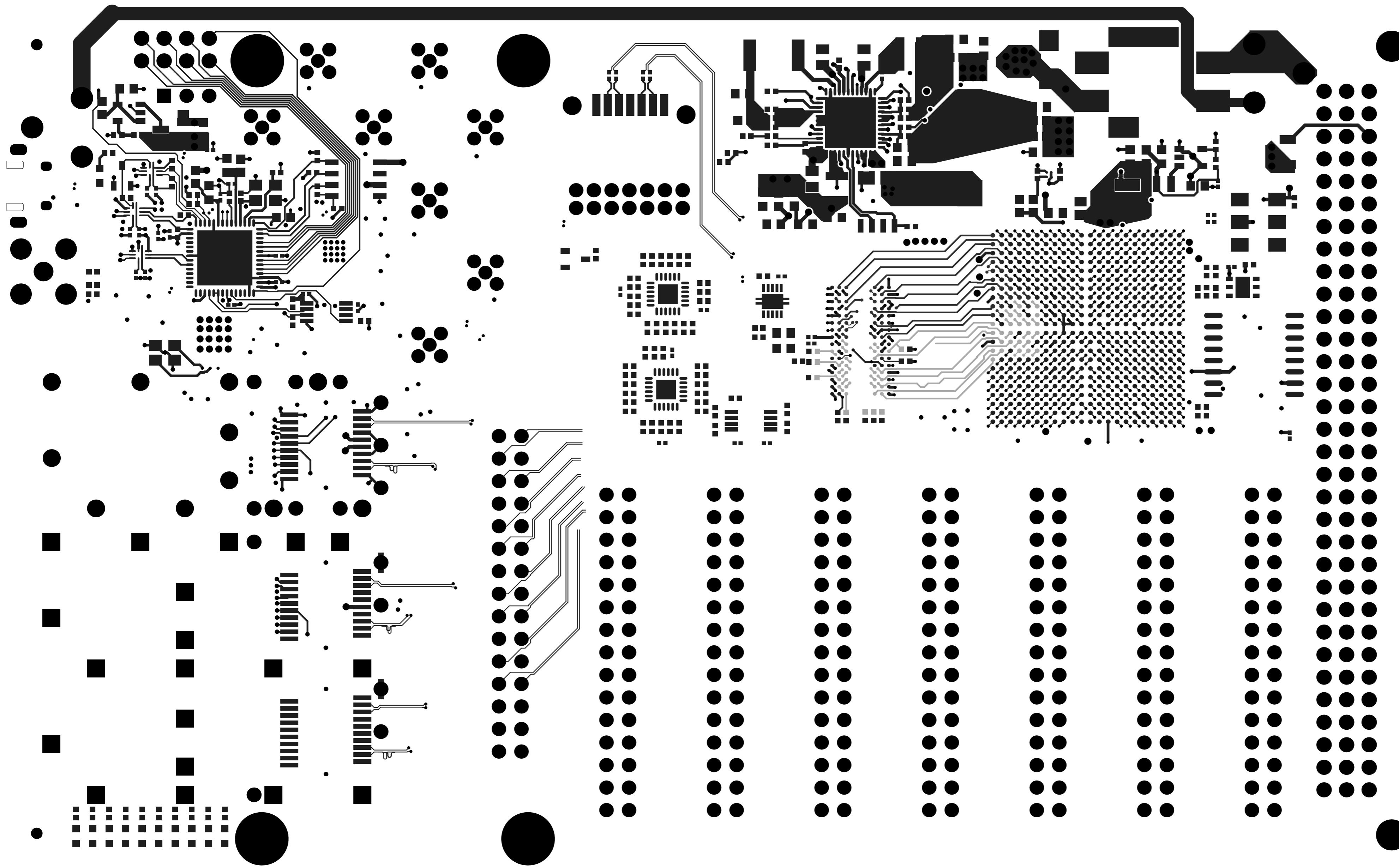


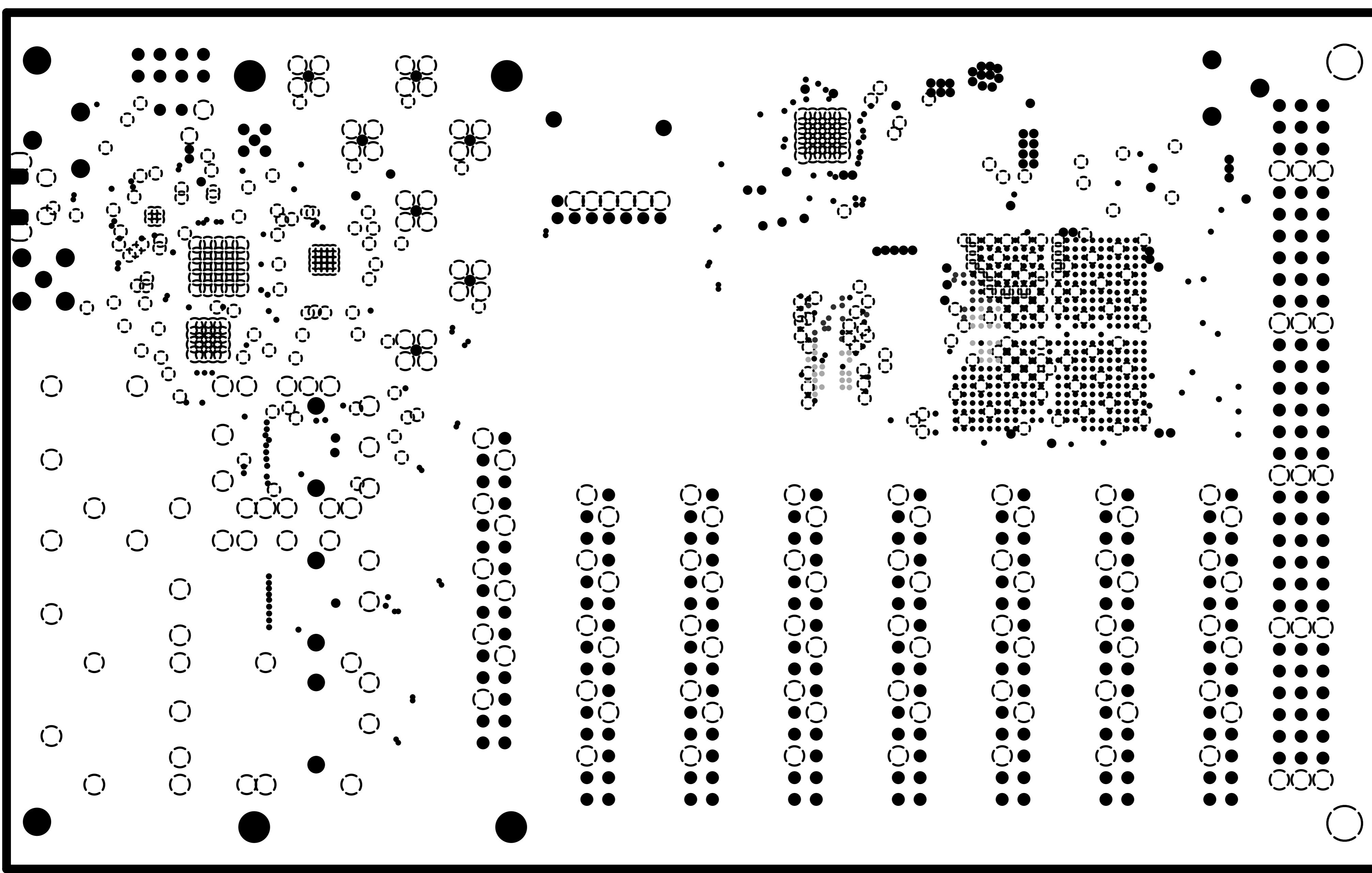












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