

Metlino_MCH

ARTIQ Sinara

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1M ESDSTRIP1 1M ESDSTRIP2

A3

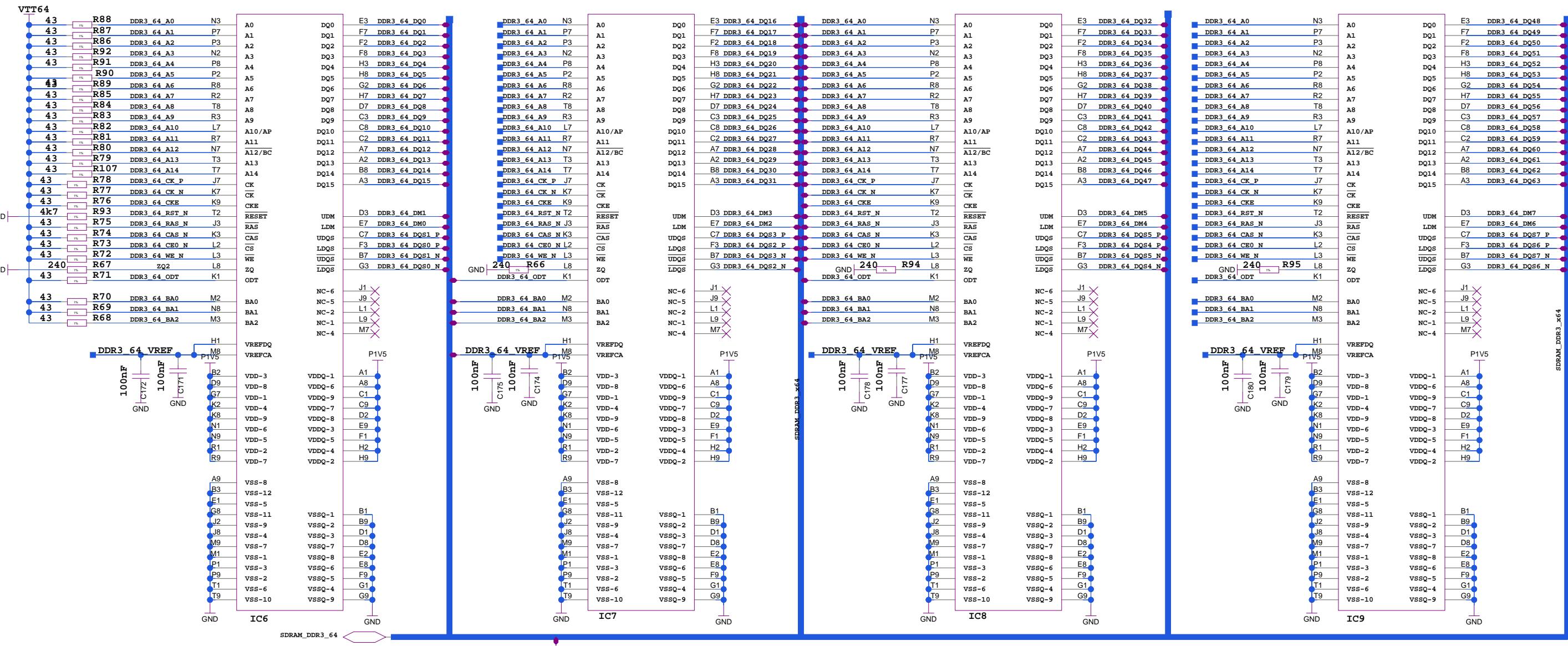
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SHEET 1 of 29

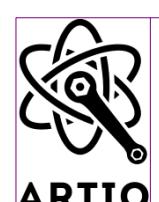
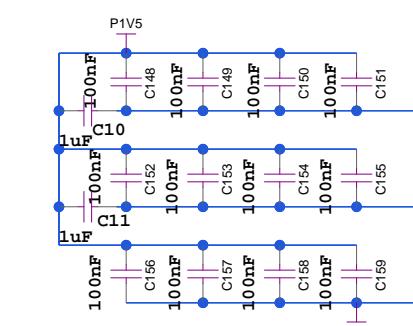
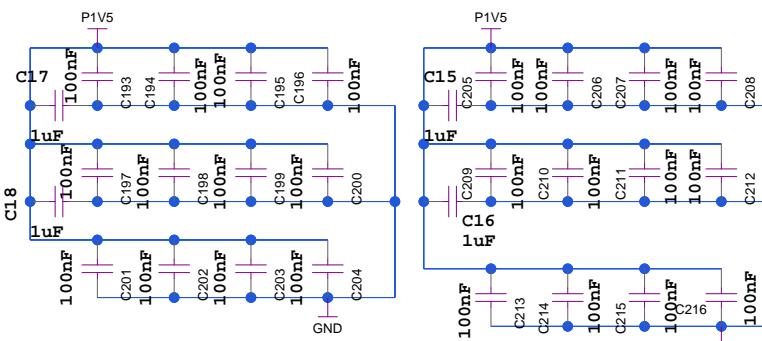
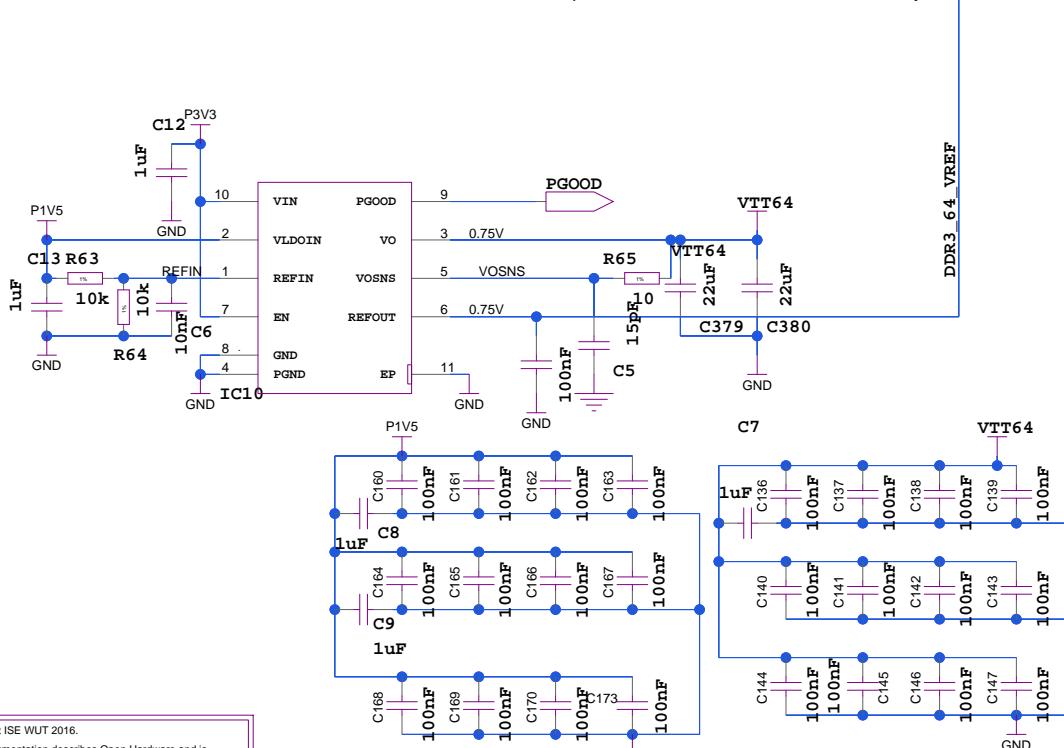
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All capacitors without values are 100nF 0201 by default



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SDRAM_DDR3_4x16

SIZE

A3

DWG NO

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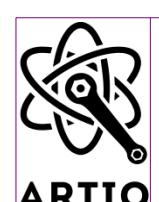
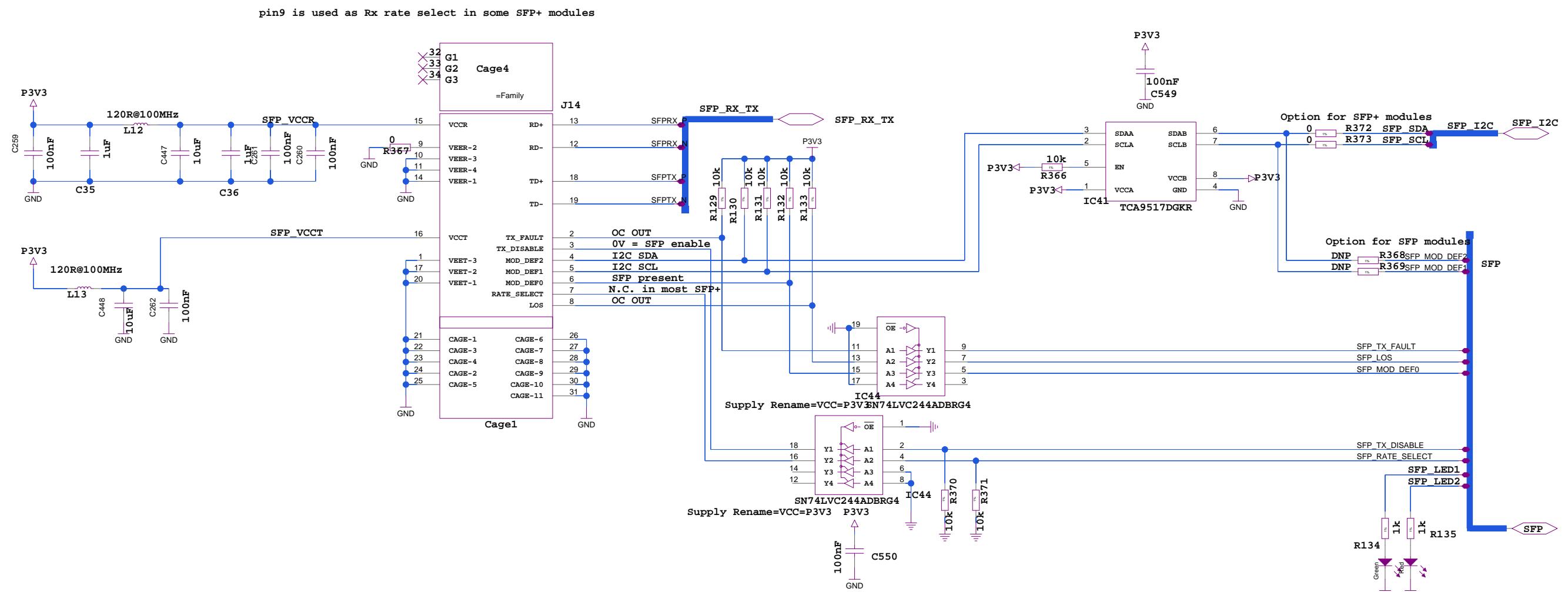
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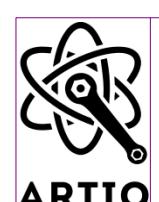
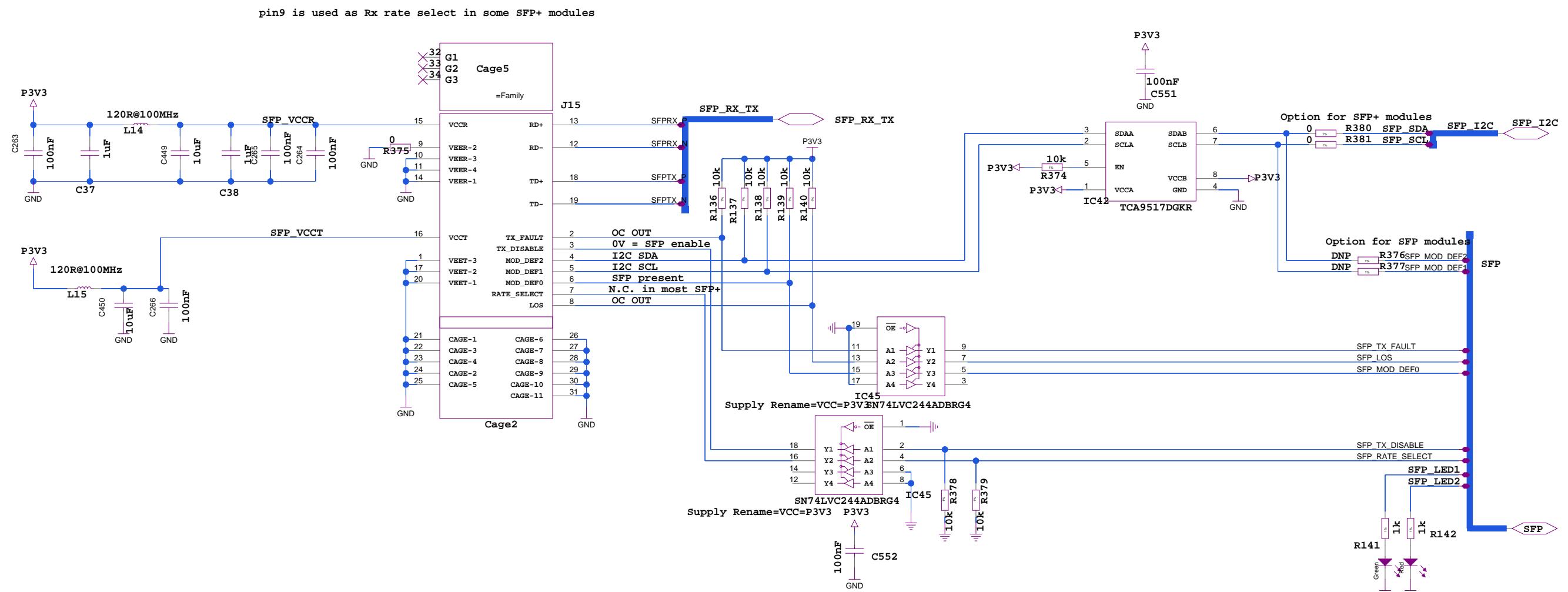
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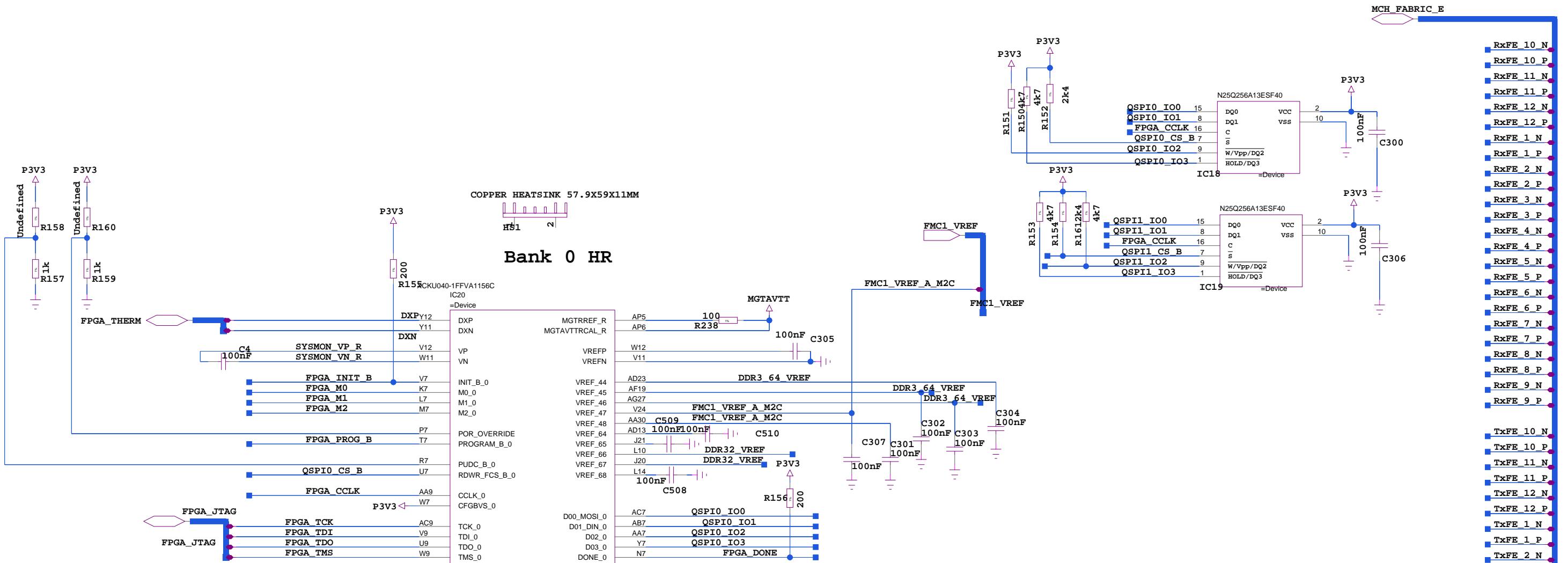
29

REV

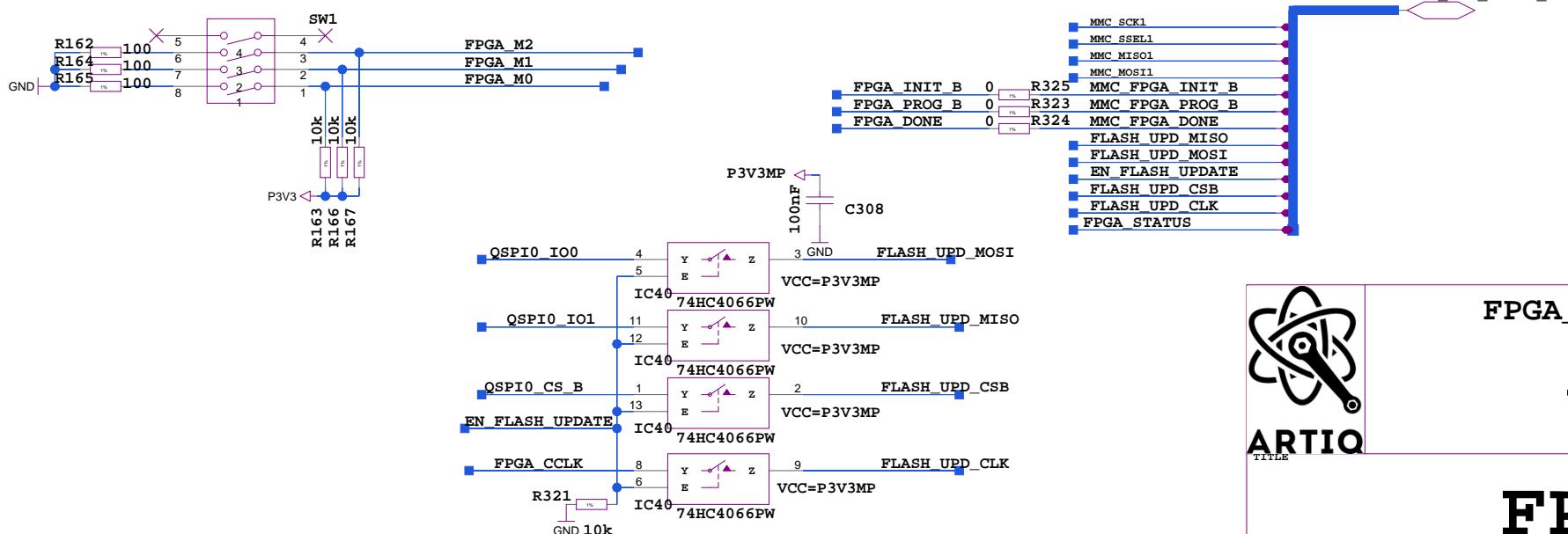
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Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via



FPGA_XCKU040FFVA1156_MCH

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FPGA Bank 0 CFG

SIZE A3

DWG NO

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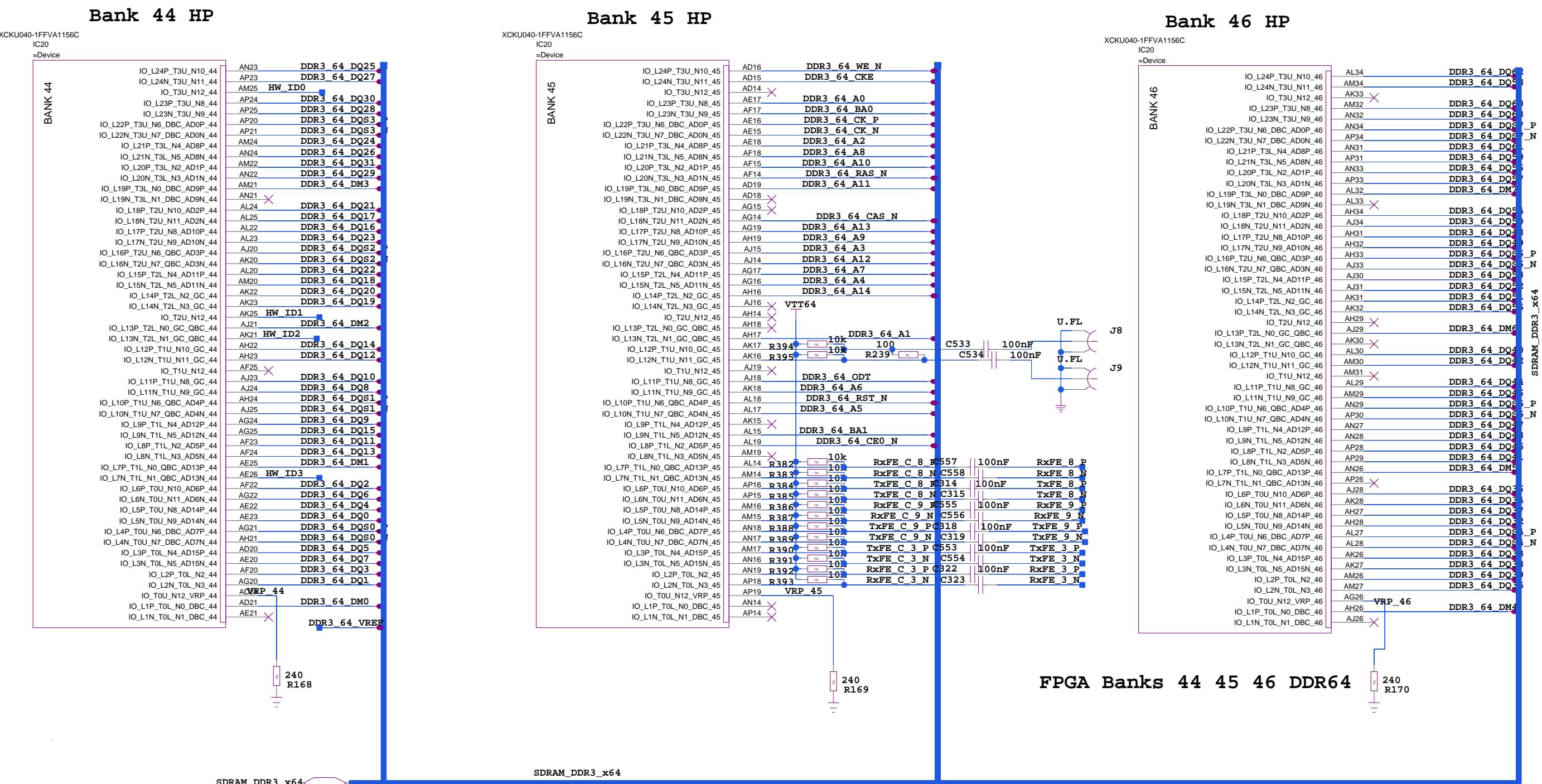
G.K.

SHEET 5 of 29

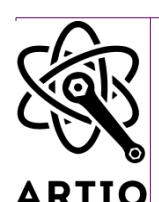
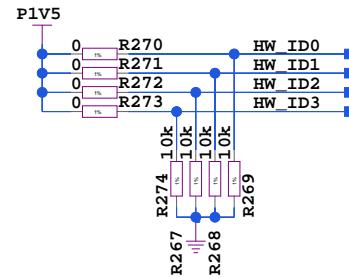
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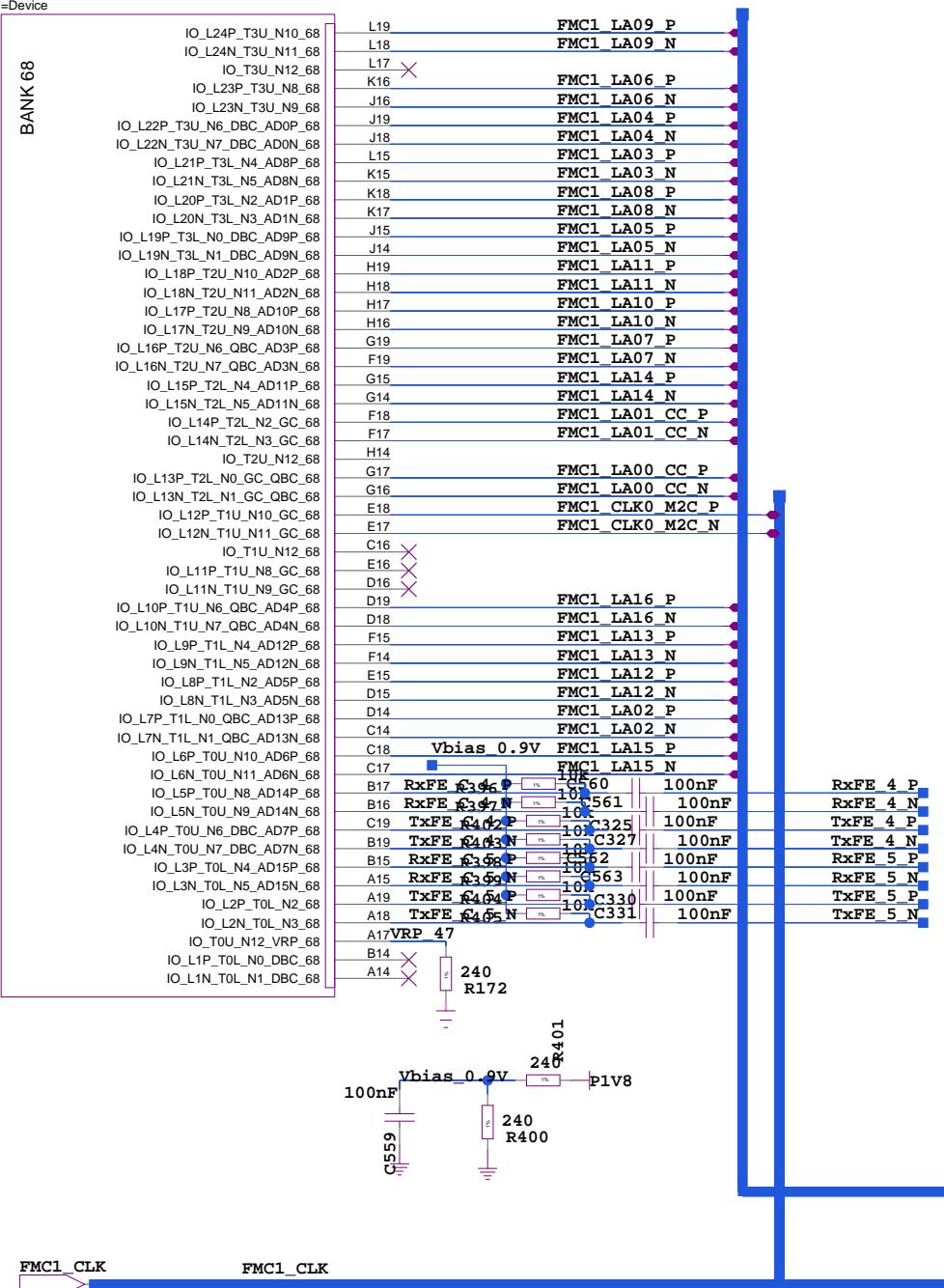


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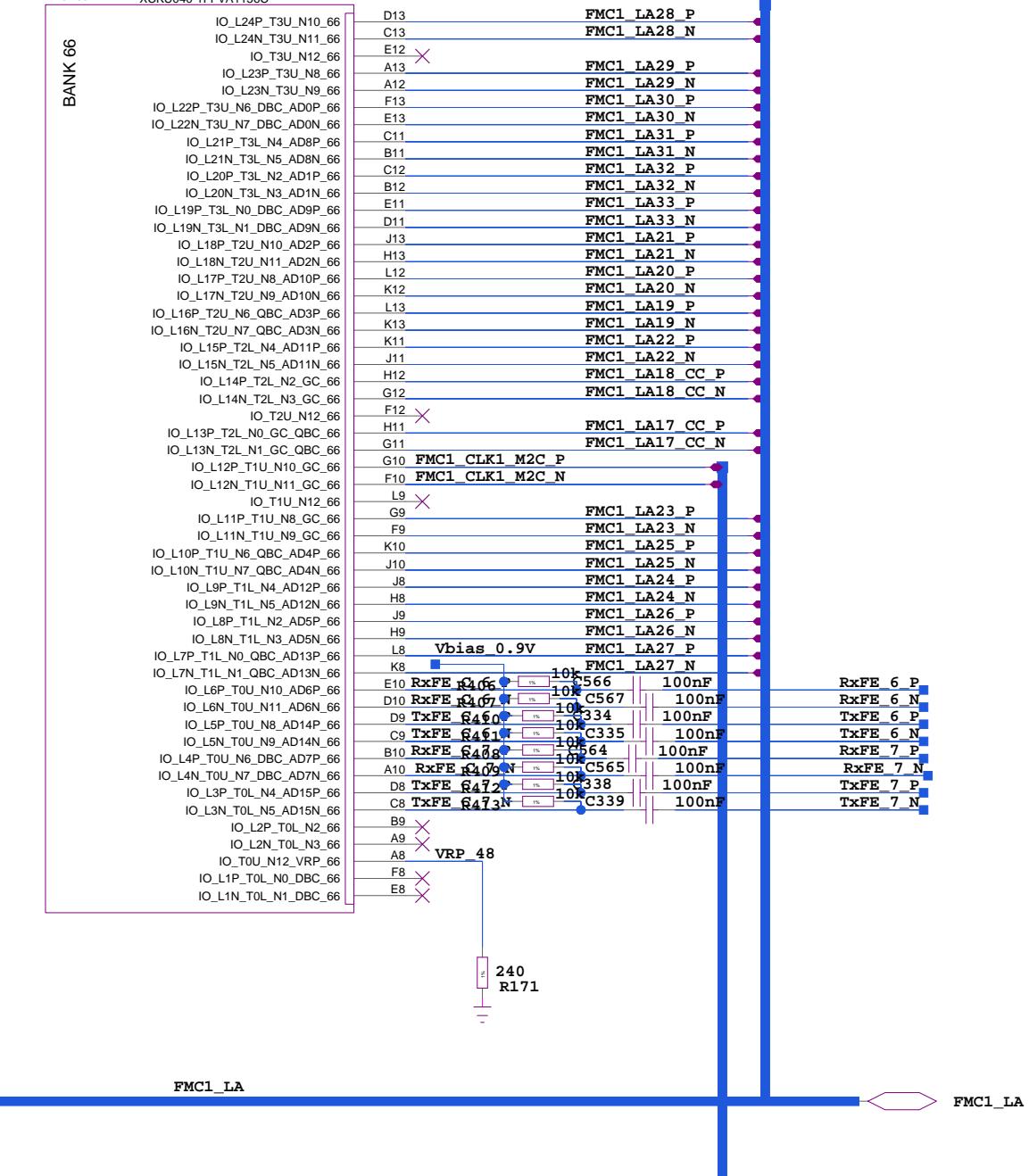
XCKU040-1FFVA1156C
IC20
=Device

Bank 68 HP



IC20
=Device

Bank 66 HP



FPGA_XCKU040FFVA1156_MCH



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FPGA Banks 47 48 HP FM

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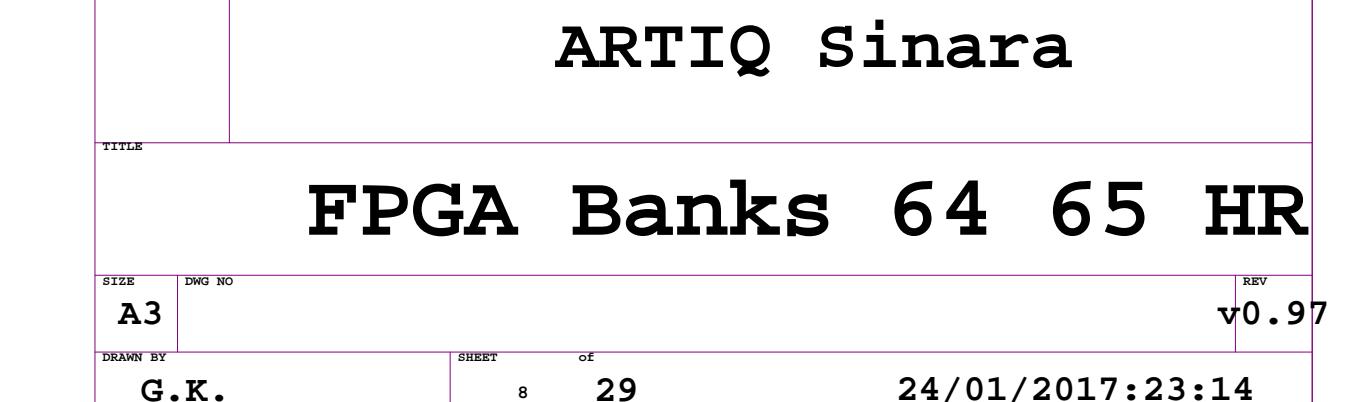
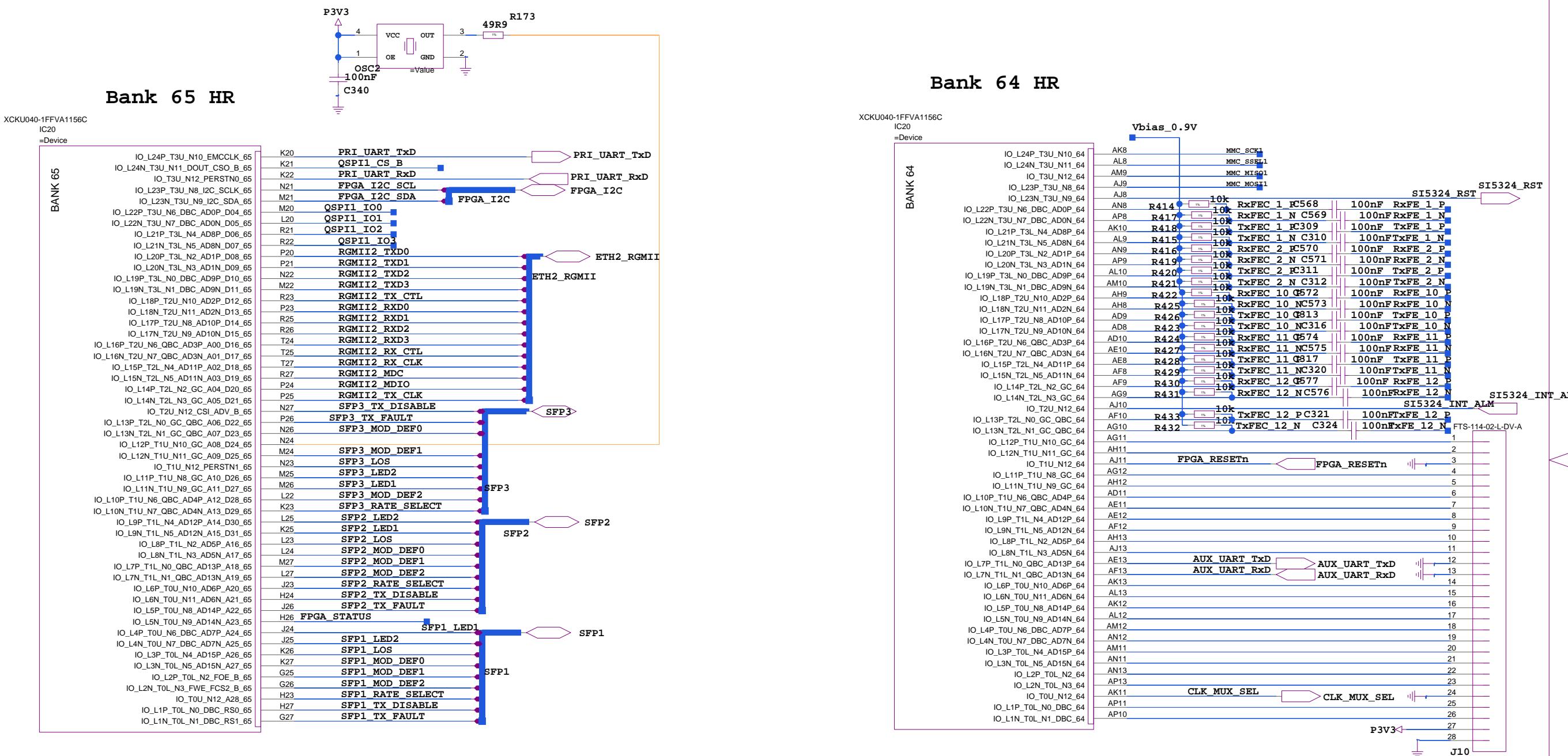
7

29

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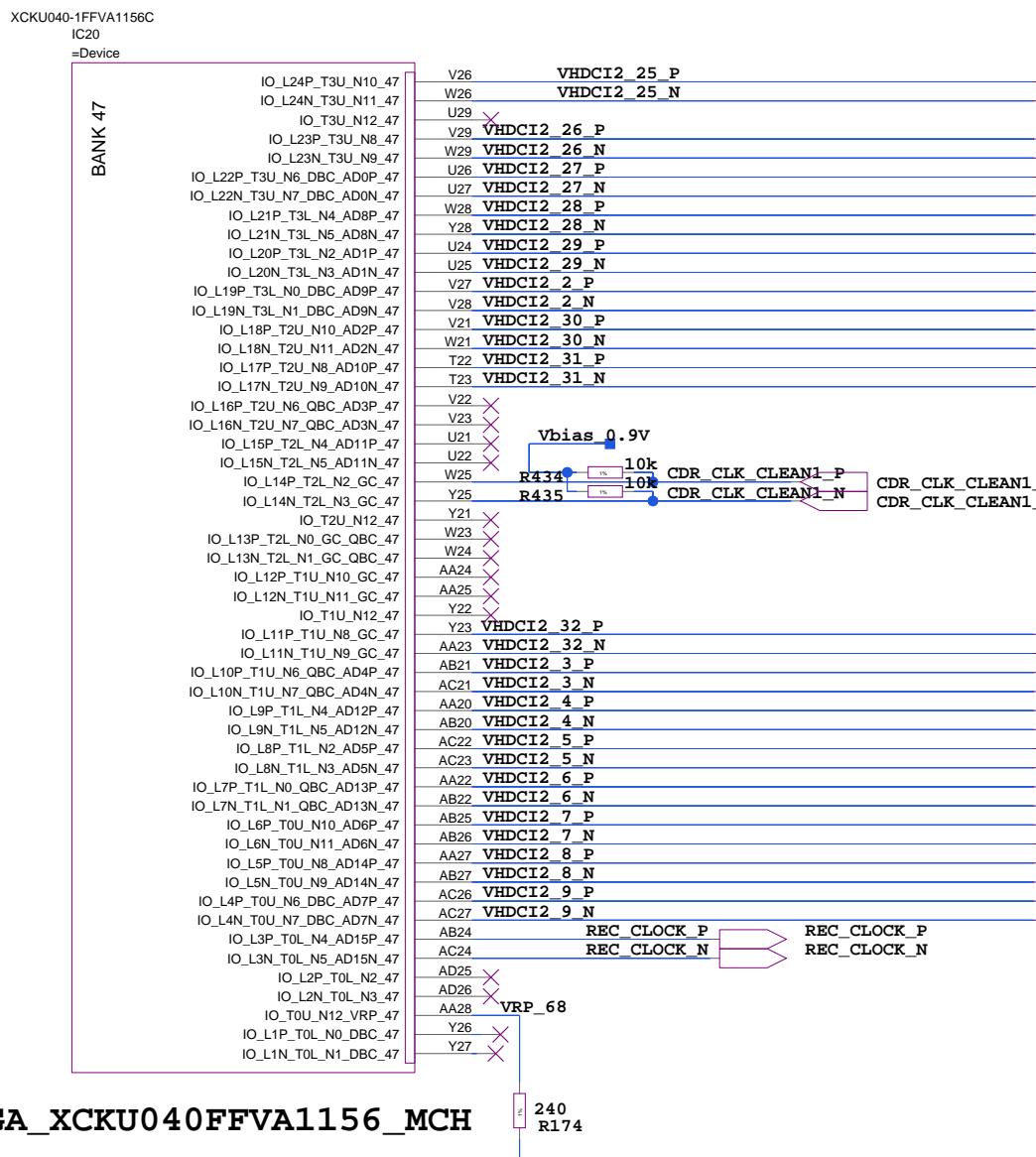
v0.97

24/01/2017:23:14

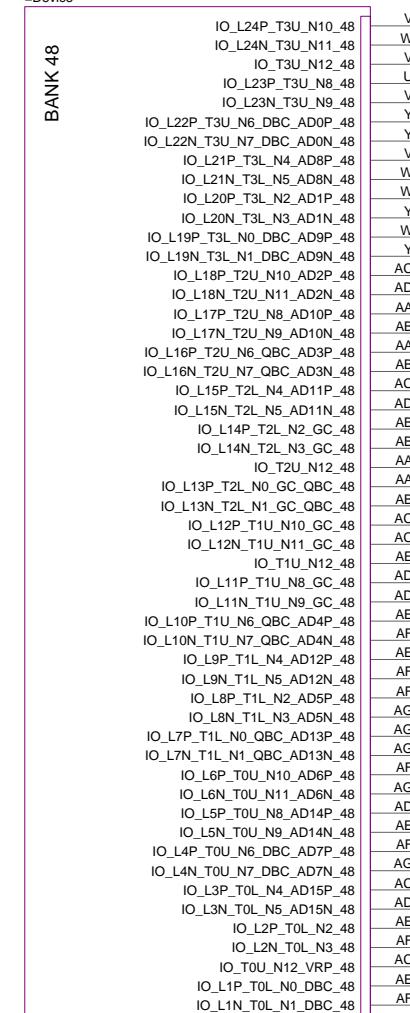


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Bank 47 HP



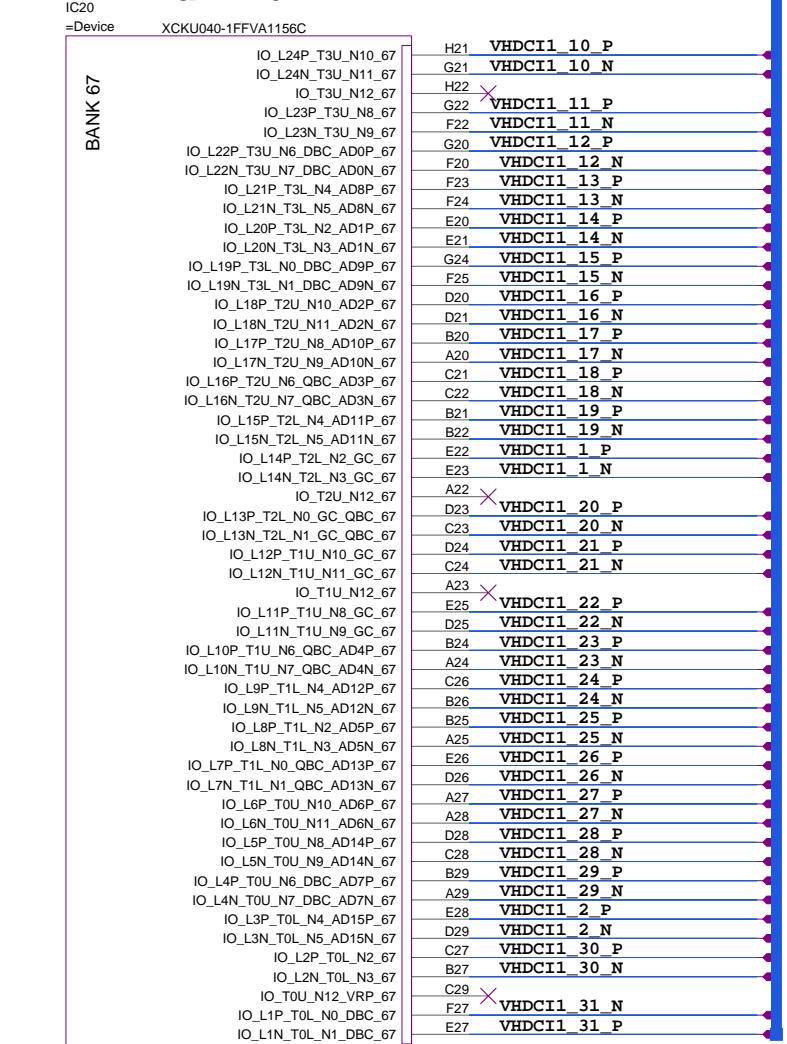
Bank 48 HP



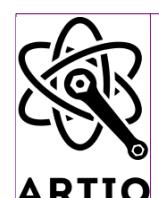
FPGA_XCKU040FFVA1156_MCH

FPGA Bank 60 67 68 HP VHDCI

Bank 67 HP



VHDCI1



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FPGA Bank 66 67 68

SIZE DWG NO

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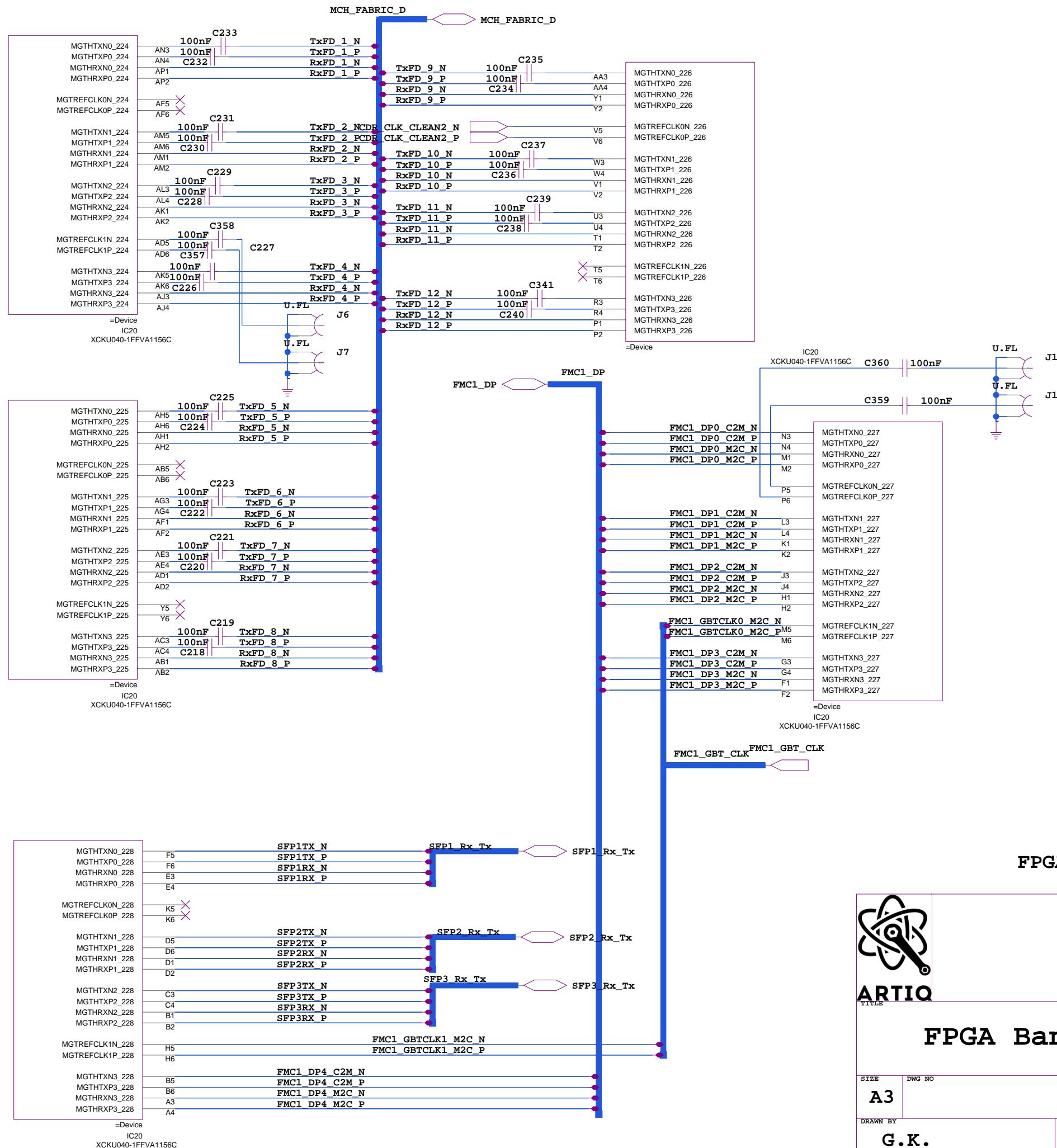
SHEET

of

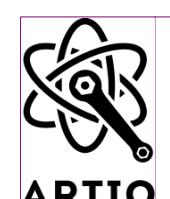
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FPGA_XCKU040FFVA1156_MCH



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FPGA Banks 224 225 226 227 228

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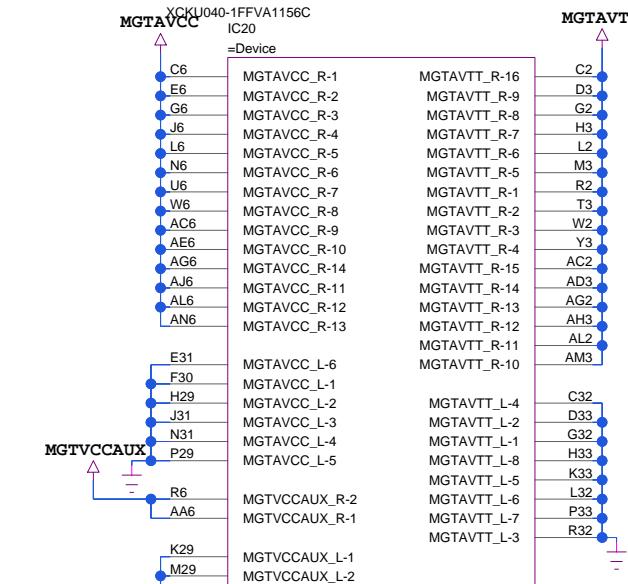
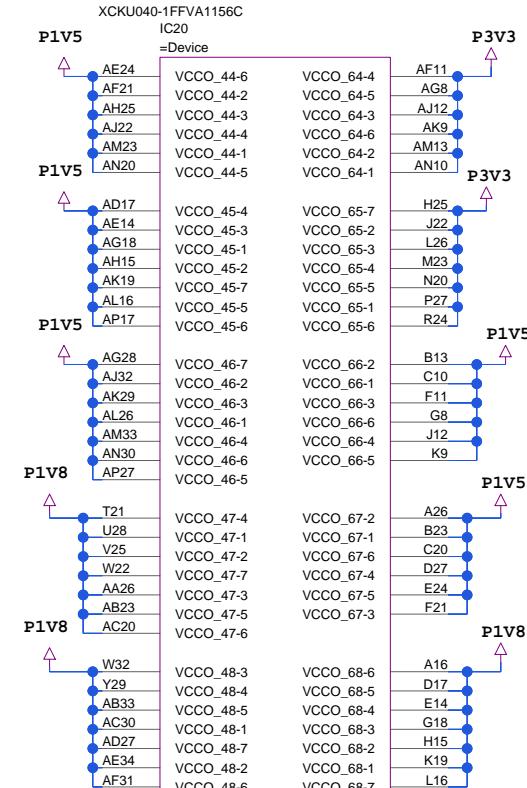
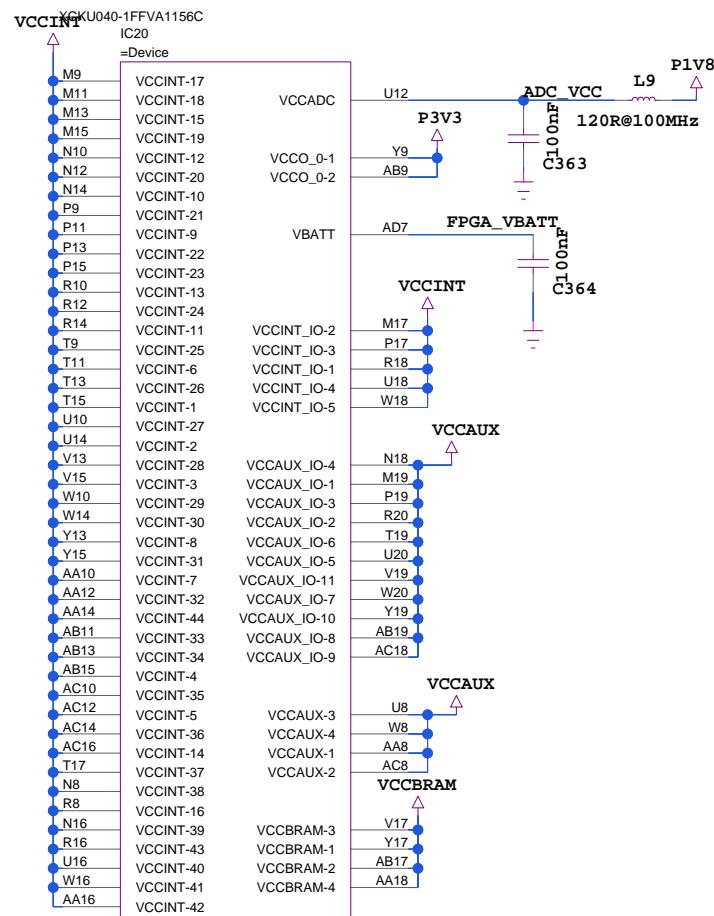
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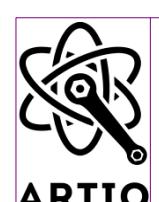
29

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FPGA Power

FPGA_XCKU040FFVA1156_MCH



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FPGA Power

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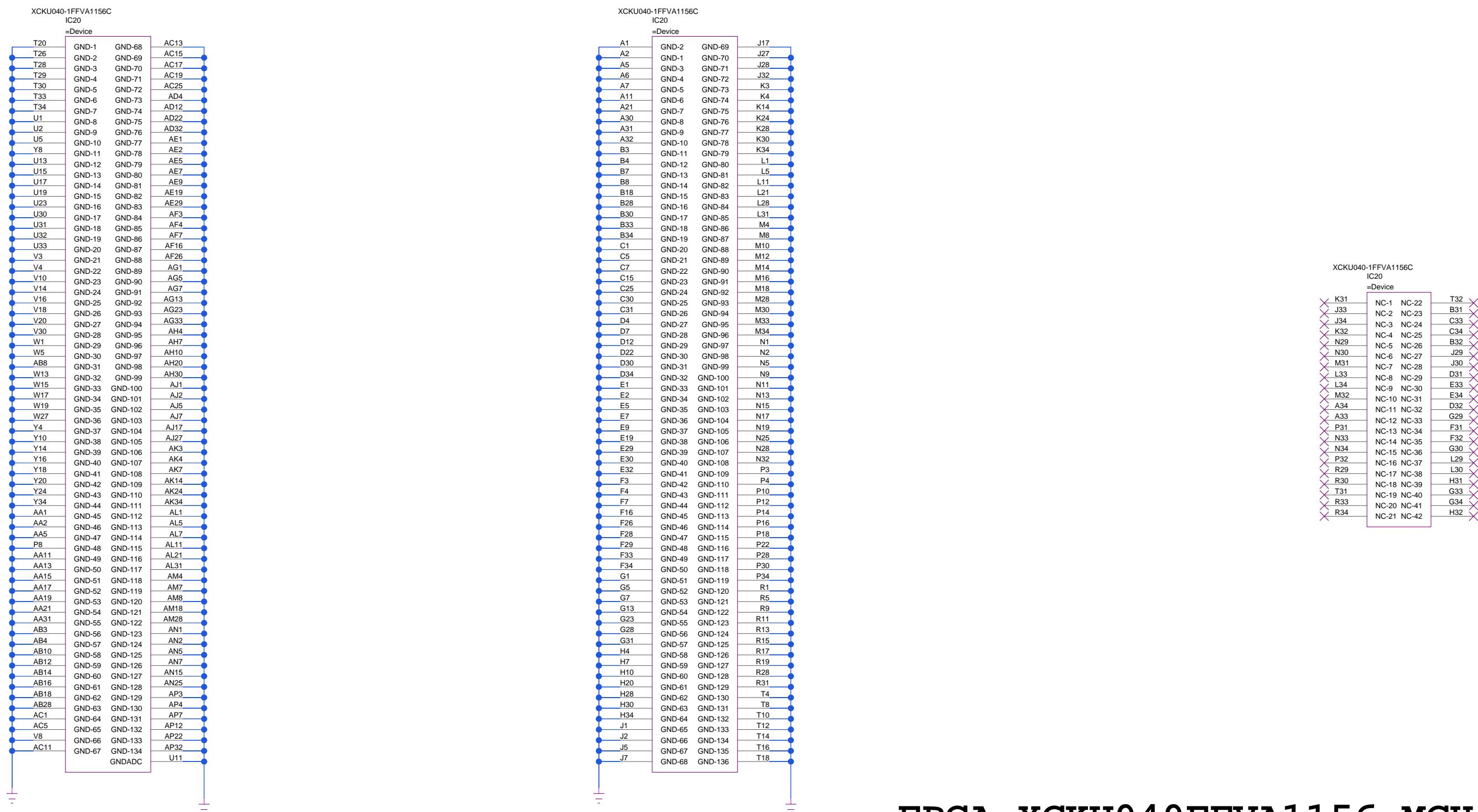
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FPGA GND NC

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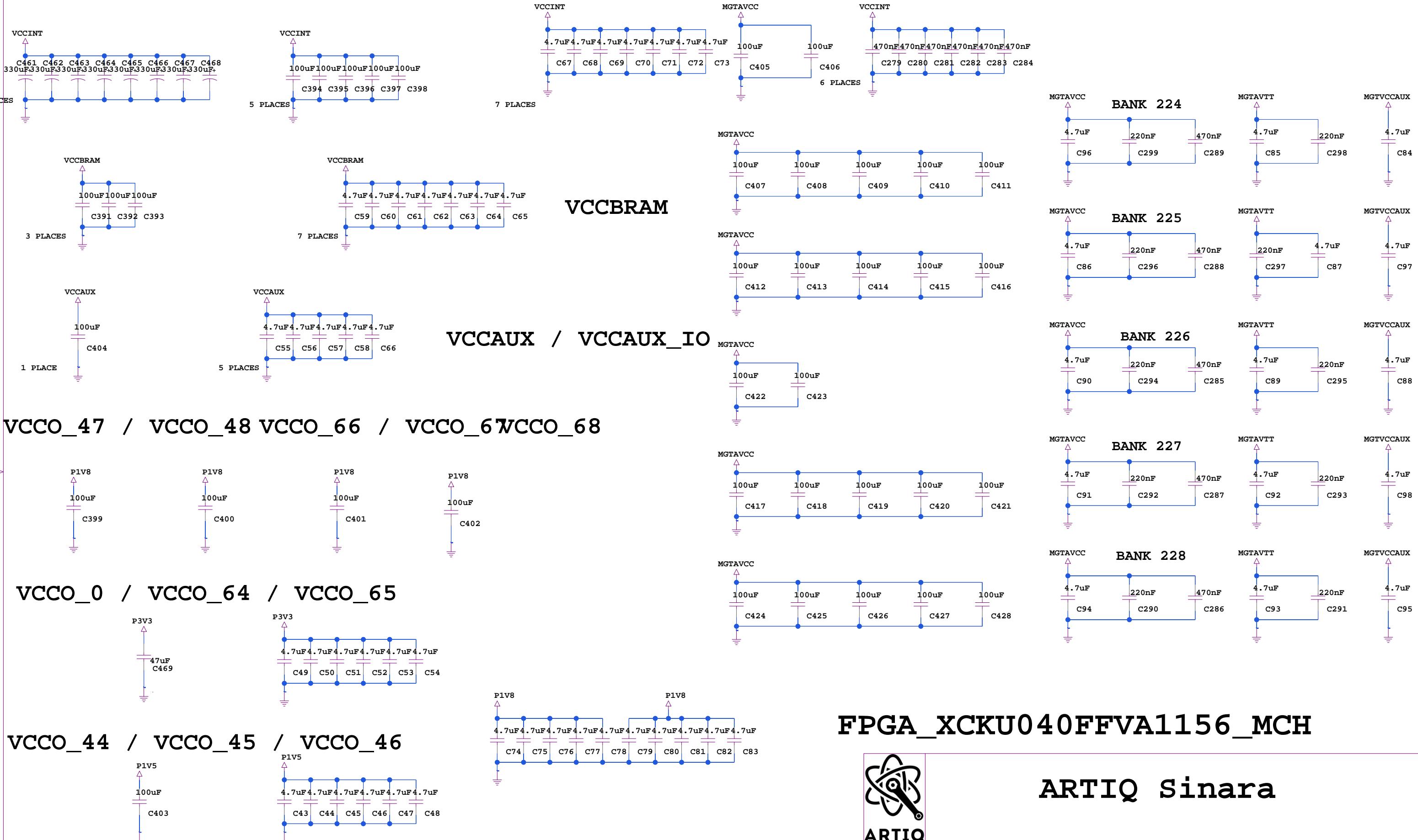
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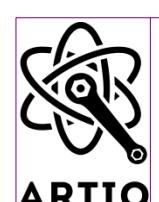
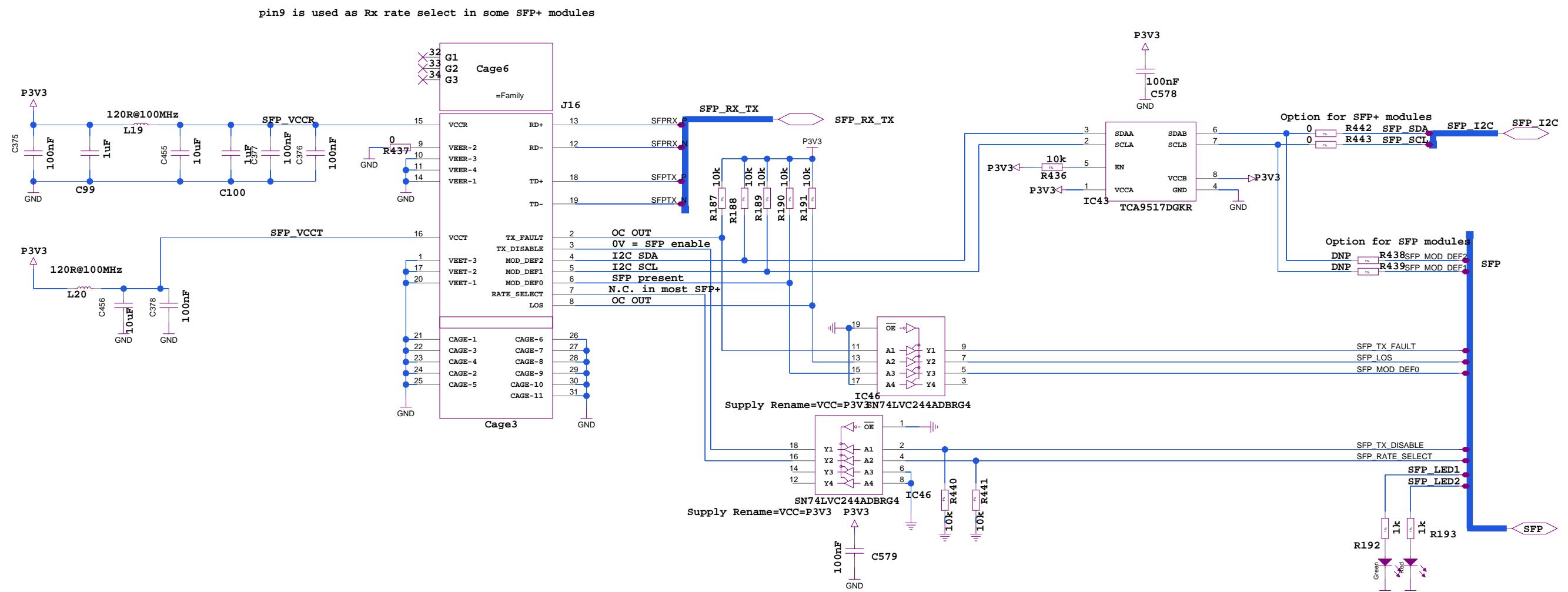
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FPGA Decoupling

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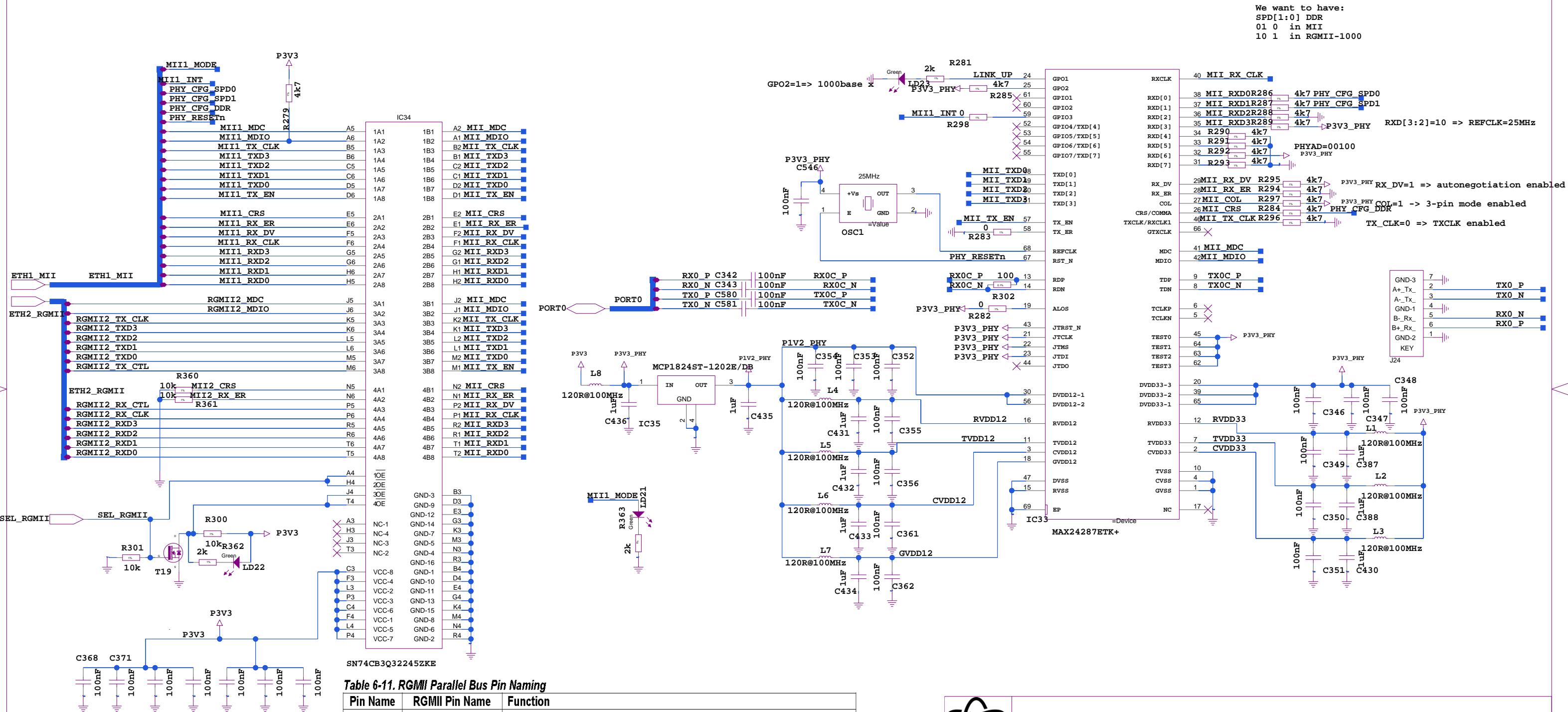
29

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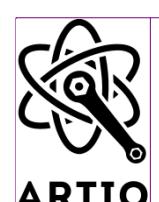
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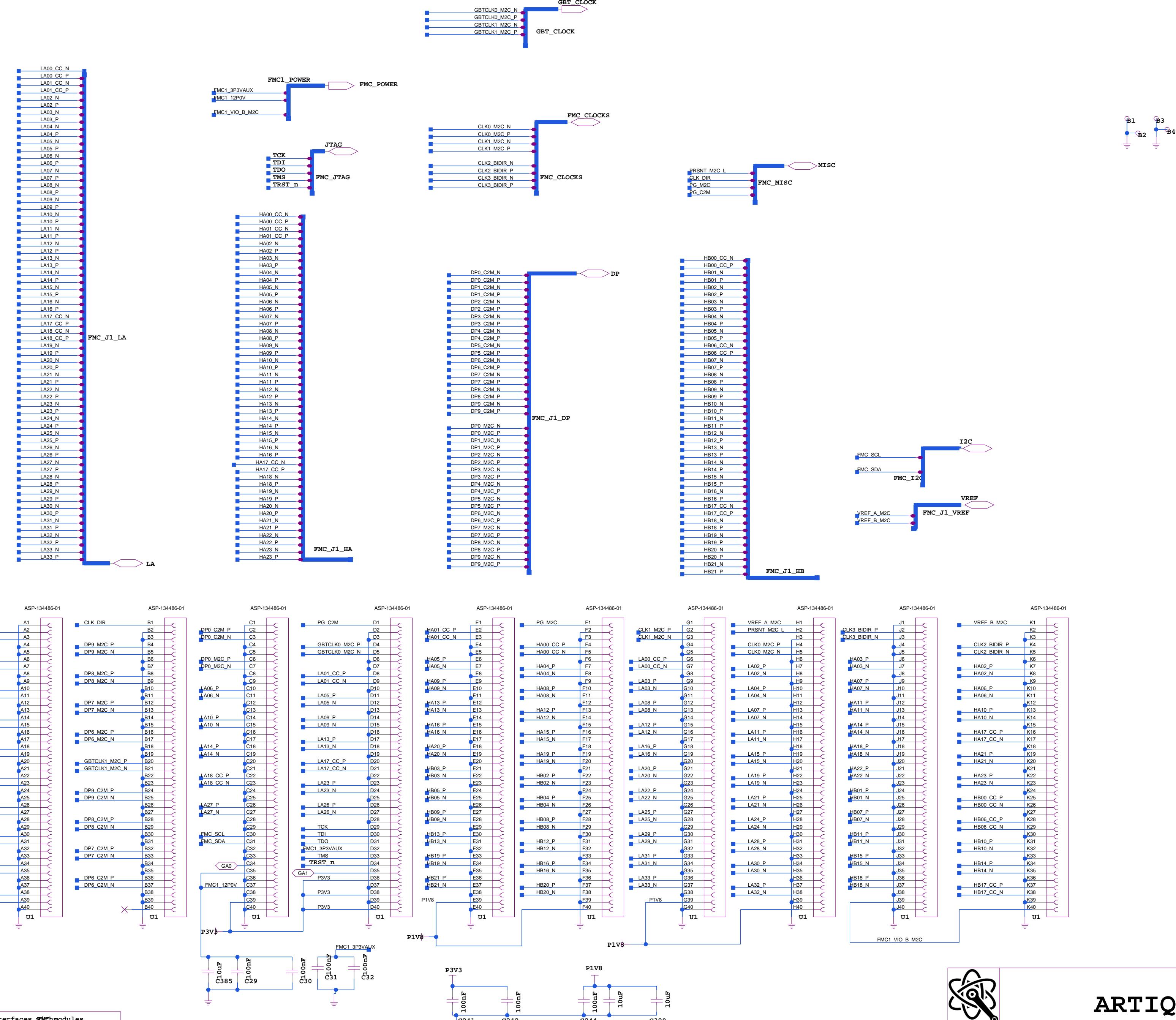


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ETH_PHY_RMII_MII

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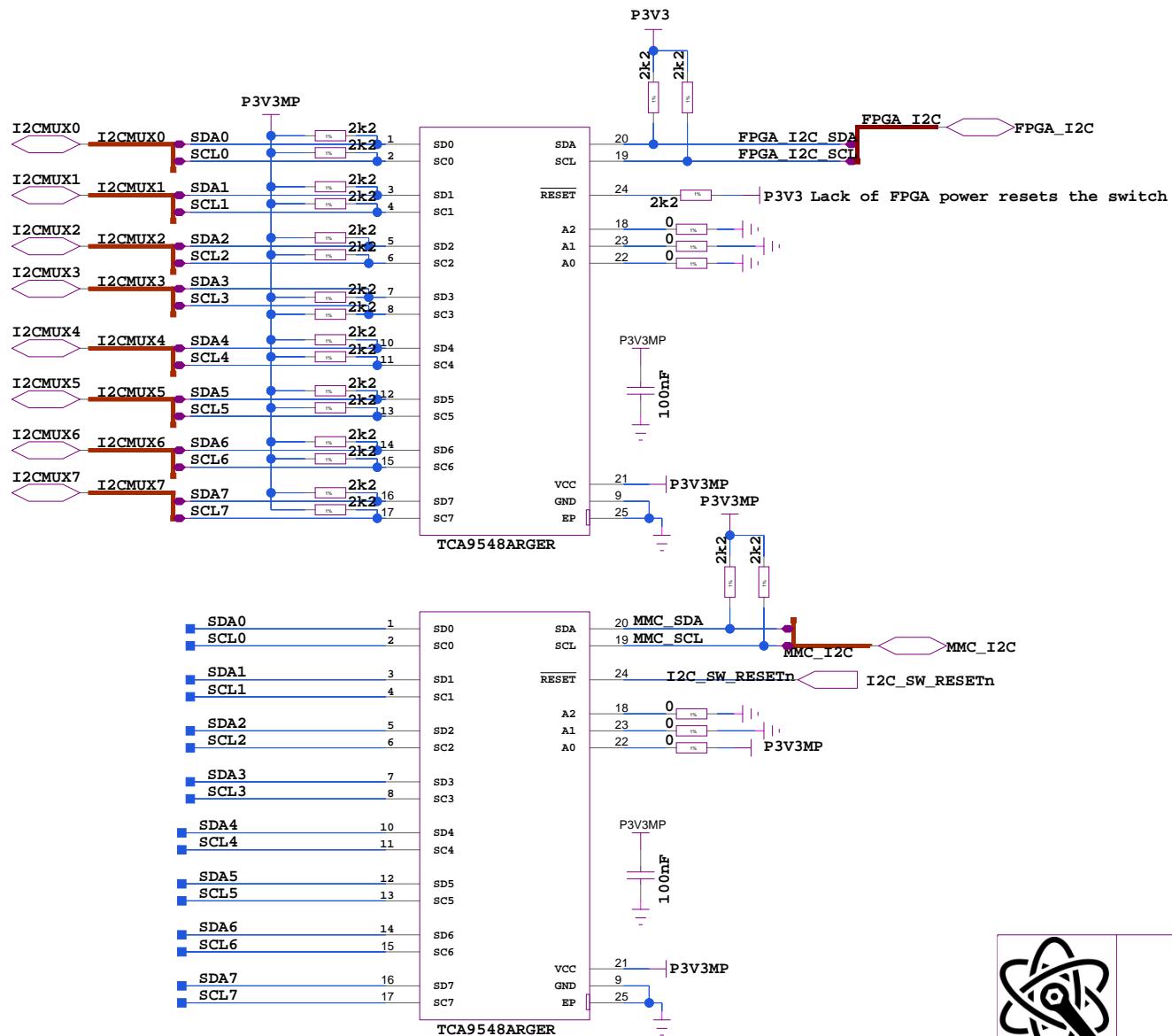
Interfaces with modules
Impedance: 100Ω diff
diff lines: LVDS 2.5V
control signals: 3.3V LVC MOS



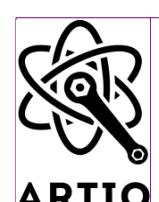
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FMC_connector

I2C switch footprint is compatible with MAX7358 which has interesting anti-lock capabilities



I2C_MUX



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SIZE DWG NO

A3

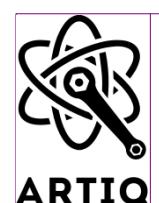
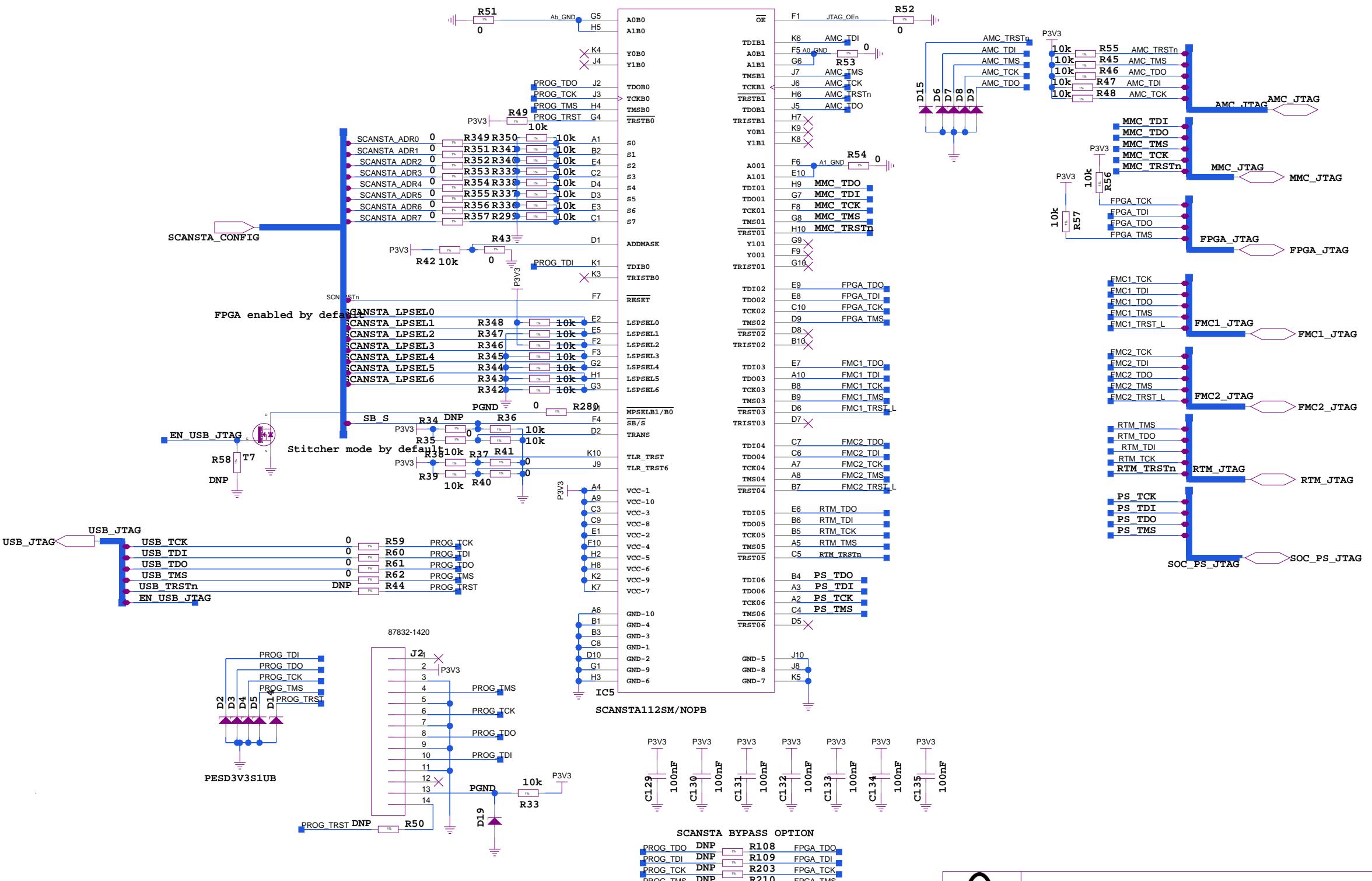
REV
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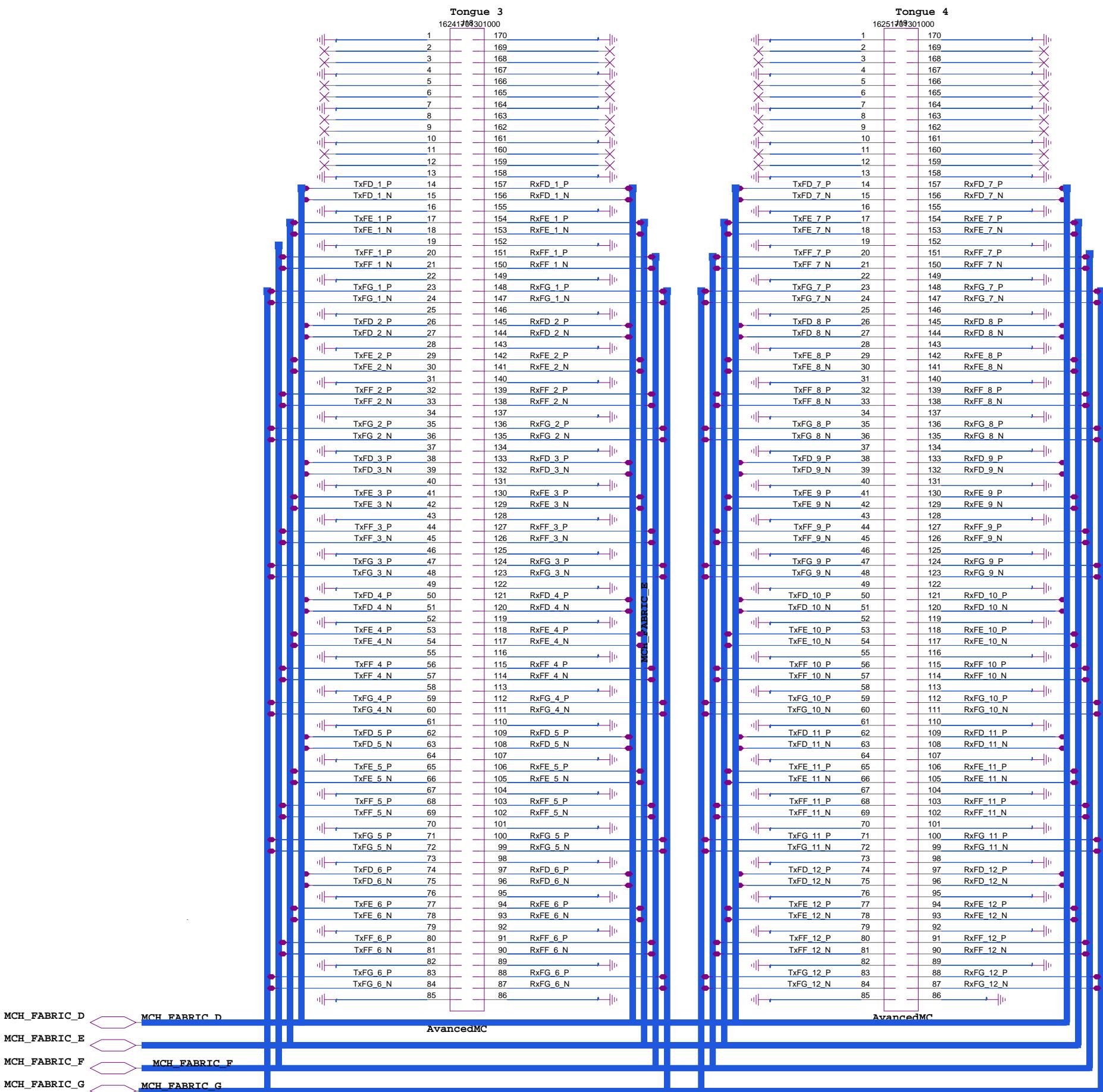
17 29



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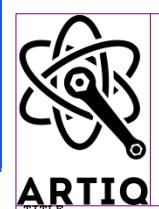
JTAG_Configuration

SIZE	DWG NO	REV
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Interfaces **MFC**: backplane
Impedance: 100Ω diff
control signals: 3.3V LVCMOS



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MCH_CON

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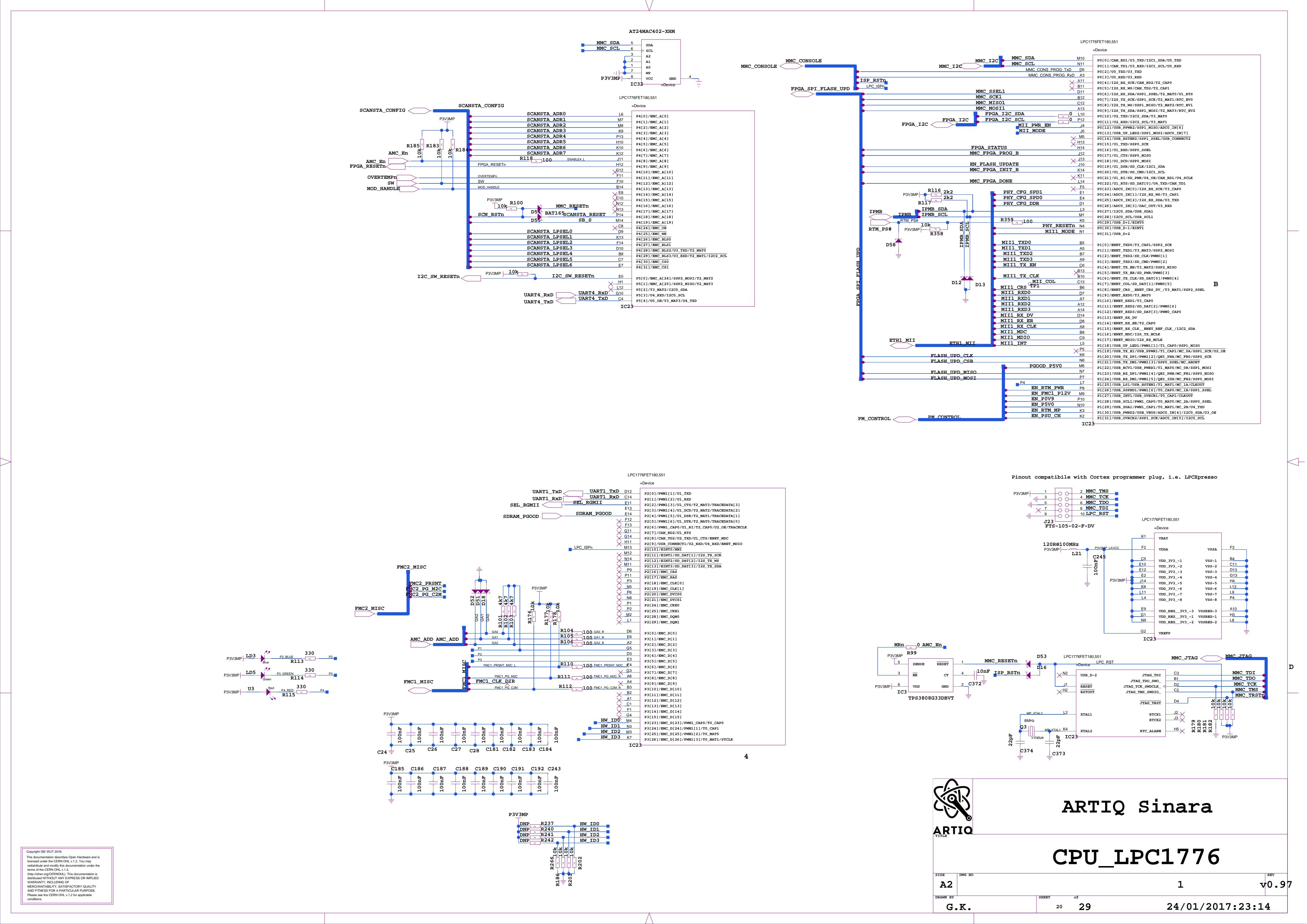
SHEET OF

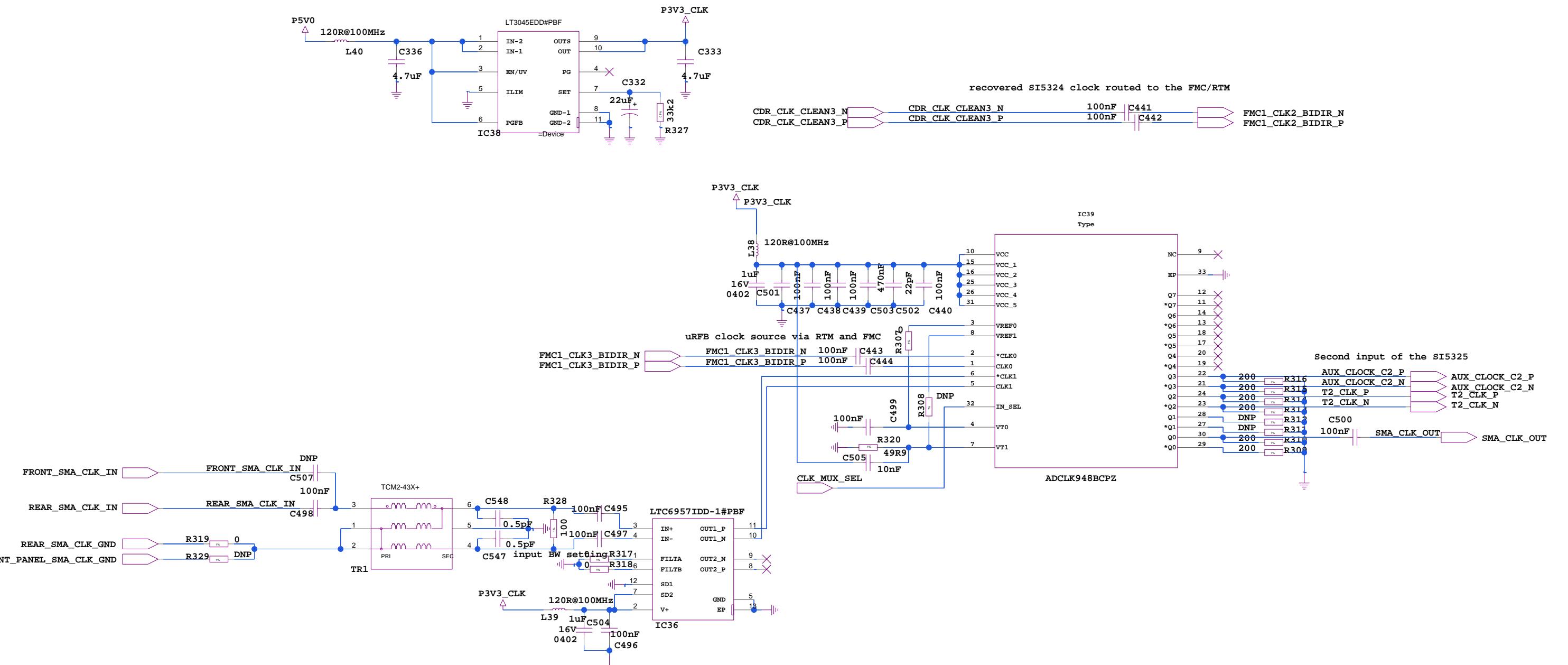
19

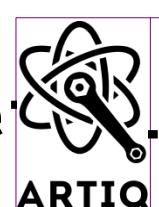
29

1

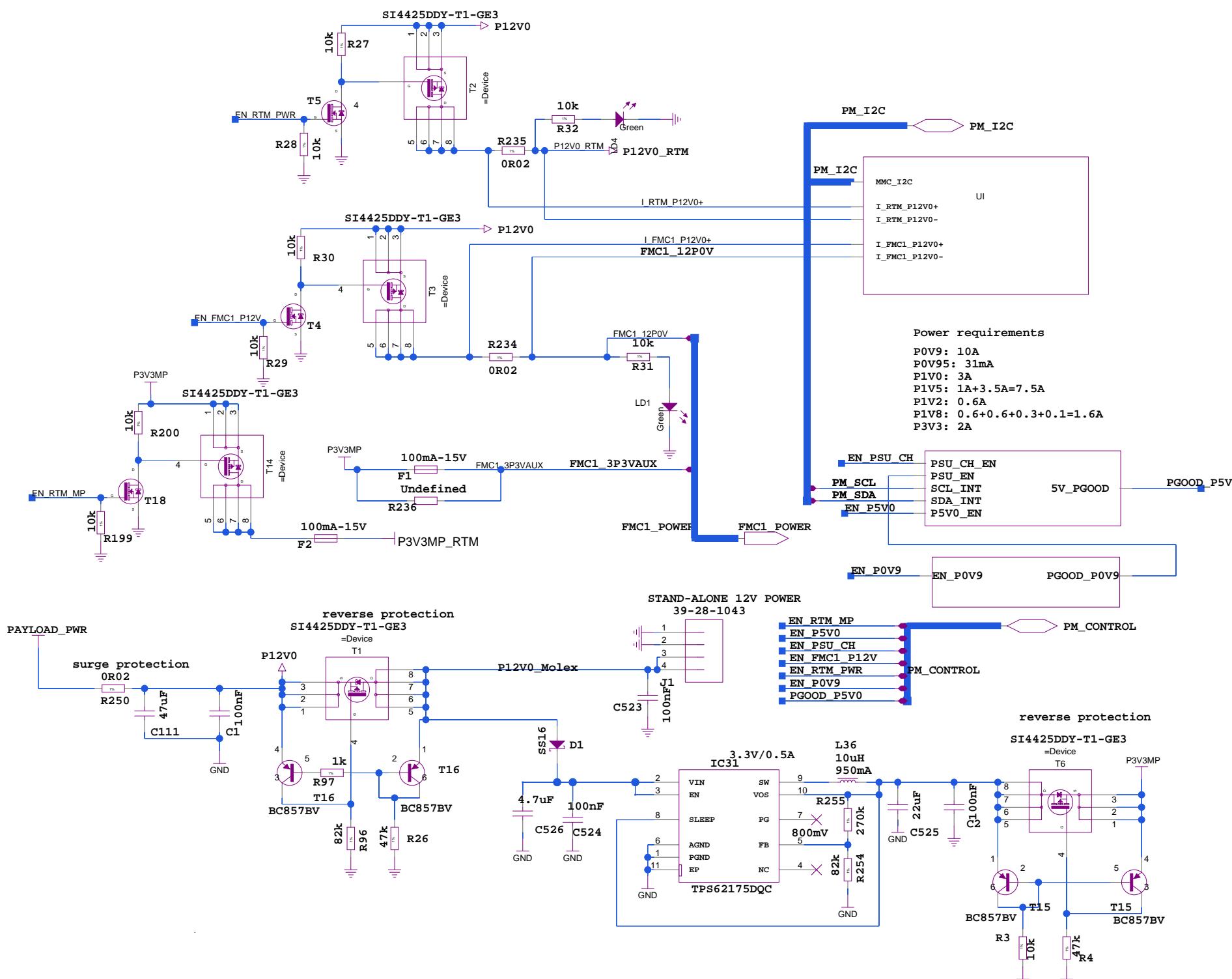
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Me~~no~~.no_CLK_Distribution
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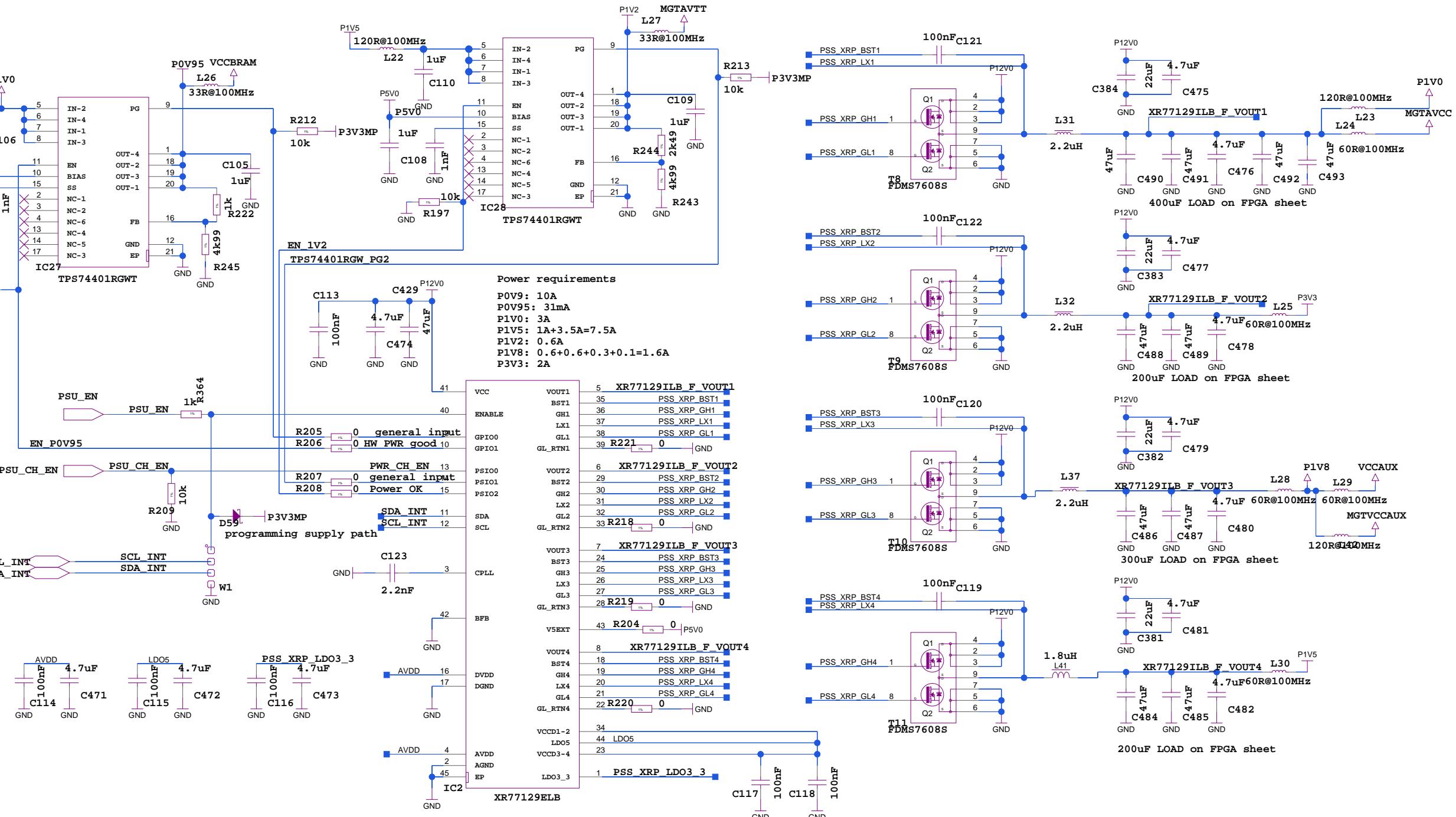
Power Supply		
Source	Voltage	Total (A)
V _{CCINT}	0.900	9.165
V _{CCINT_IO}	0.900	0.620
V _{CCBRAM}	0.950	0.031
V _{CCAUX}	1.800	0.660
V _{CCAUX_IO}	1.800	0.546
V _{CCO 3.3V}	3.300	0.000
V _{CCO 2.5V}	2.500	
V _{CCO 1.8V}	1.800	0.380
V _{CCO 1.5V}	1.500	0.936
V _{CCO 1.35V}	1.350	
V _{CCO 1.2V}	1.200	
V _{CCO 1.0V}	1.000	
MGT _{VCCAUX}	1.800	0.081
MGT _{AV_{CC}}	1.000	3.038
MGT _{AV_{TT}}	1.200	0.592
-	-	
-	-	
V _{CCADC}	1.800	0.014

The recommended power-on sequence is V_{CCINT}/V_{CCINT_IO}, V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the 1/0s are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT}/V_{CCINT_IO} and V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAO} must be connected together. When the current minimums are met, the device powers on after the V_{CCINT}/V_{CCINT_IO}, V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing recommendations. The recommended power-on sequence to achieve minimum current draw for the GTH or GT_T transceivers is V_{CCINT}, VMGTA_{VCC}, VMGTA_{VIT} OR VMGTA_{VCC}, V_{CCINT}, VMGTA_{VTT}. There is no recommended sequencing for VMGTA_{VCC}. Both VMGTA_{VCC} and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from VMGTA_{VTT} can be higher than specifications during power-up and power-down.

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POWER_Management

Power Supply		
Source	Voltage	Total (A)
VCCINT	0.800	9.165
VCCINTIO	0.900	0.620
VCCBRAM	0.950	0.031
VCCAUX	1.800	0.660
VCCAUXIO	1.800	0.546
VCCO 3.3V	3.300	0.000
VCCO 2.5V	2.500	
VCCO 1.8V	1.800	0.380
VCCO 1.5V	1.500	0.936
VCCO 1.35V	1.350	
VCCO 1.2V	1.200	
Vcc 1.0V	1.000	
MGTVCAX	1.800	0.081
MGTAVCC	1.000	3.038
MGTAVTT	1.200	0.592
-	-	
VCCADC	1.800	0.014

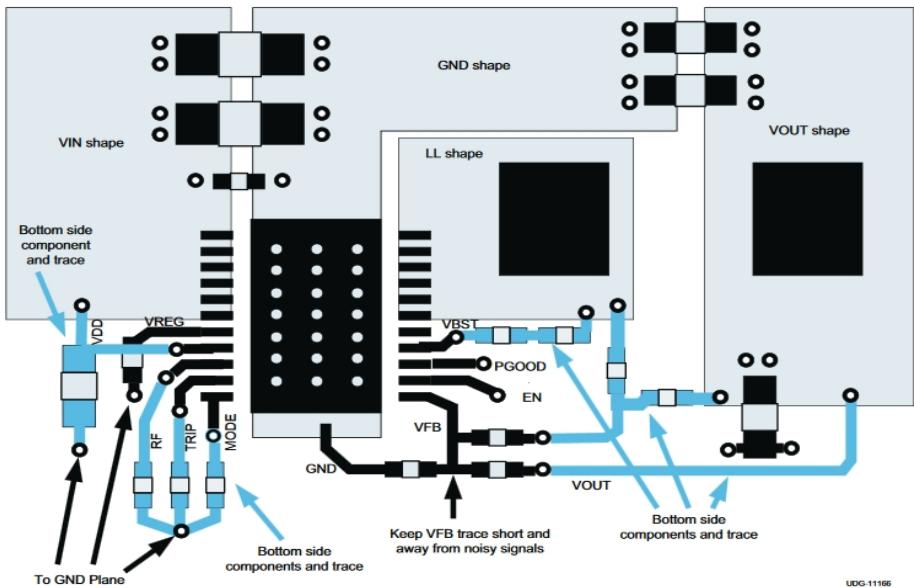


The recommended power-on sequence is VCCINT/VCCINT IO, VCCBRAM, VCCAUX/VCCAO to achieve minimum current draw and ensure that the I/Os are 3-stated at power-up. Sequence is the reverse of the power-on sequence. I/O and VCCAUX have the same recommended voltage levels. They can be powered by the same supply and VCCINT/VCCINT IO must be connected to VCCINT. Both VCCINT/VCCINT IO and VCCAO must be connected together. When the current minimums are met, the device power-up sequence has VCCBRAM, VCCAUX/VCCAO IO, and VCCAO. Power-up sequence threshold voltages should be configured until after VCCINT is applied. VCCAO and VREF can be powered up simultaneously. There is no recommended sequencing for VMGTVCCAO. Both VMGTAVC and VCCIN can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence. The recommended sequencing for the power-down sequence is to active eye minimum current draw and ensure that the I/Os are 3-stated at power-down. There is no recommended sequencing for VMGTVCCAO. Both VMGTAVC and VCCIN can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence. The recommended sequencing for the power-down sequence is to active eye minimum current draw and ensure that the I/Os are 3-stated at power-down.

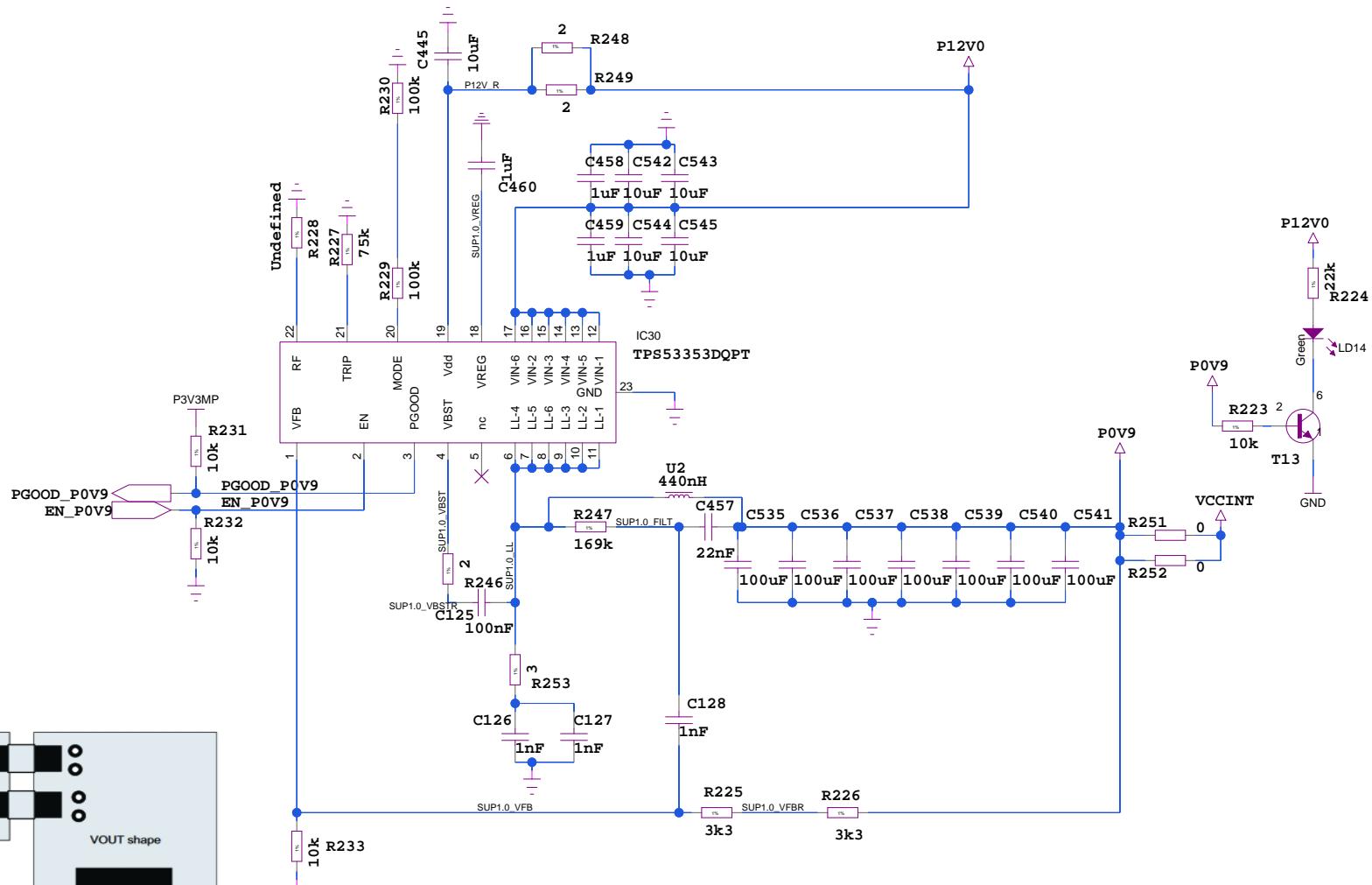
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PWR_DC_DC_EXAR

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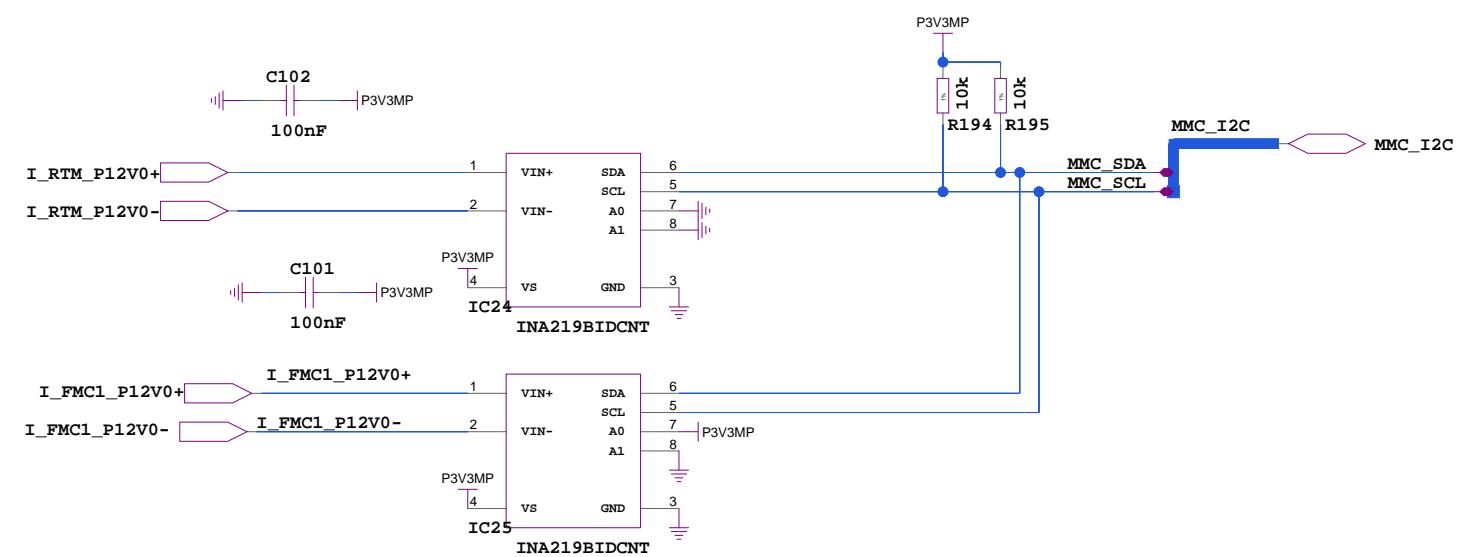
ARTIQ Sinara

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SIZE	DWG NO	REV
A3		
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G.K.	24	29

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UI_mon

SIZE	DWG NO	REV
A3		v0.97
DRAWN BY	SHEET of	
G.K.	25	29

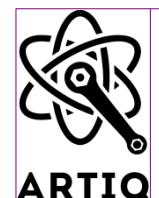
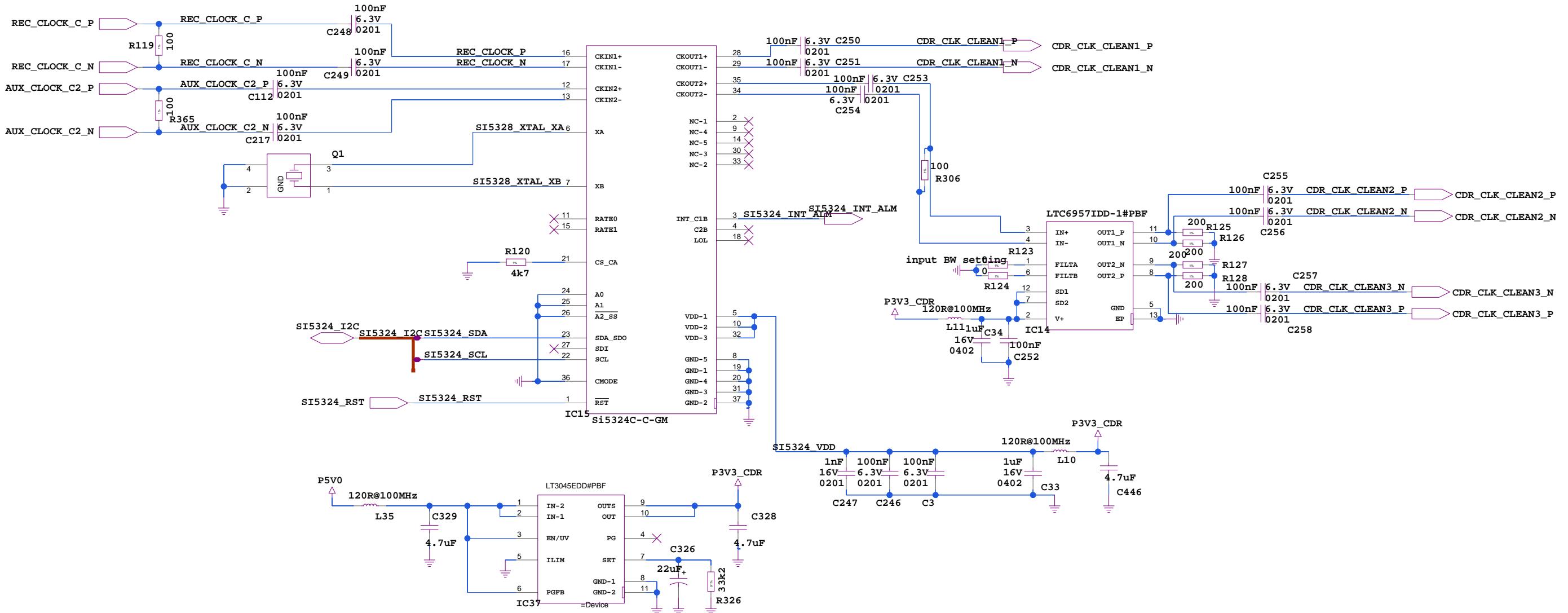
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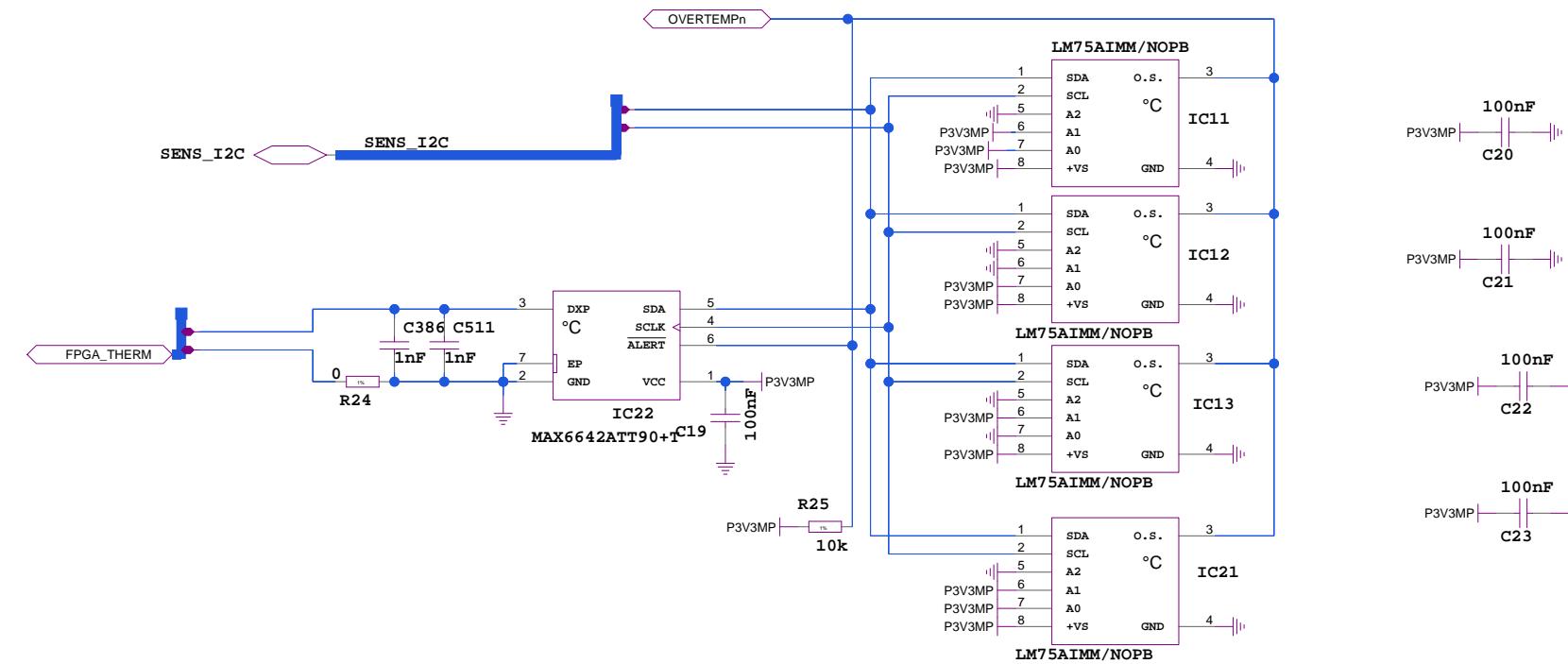


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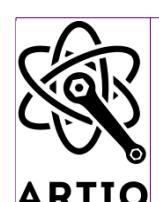
SI5324_CLK_RECOVERY

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SIZE	DWG NO	REV
A3		v0.97
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G.K.	26	29



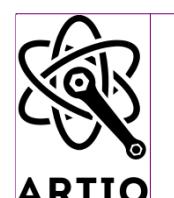
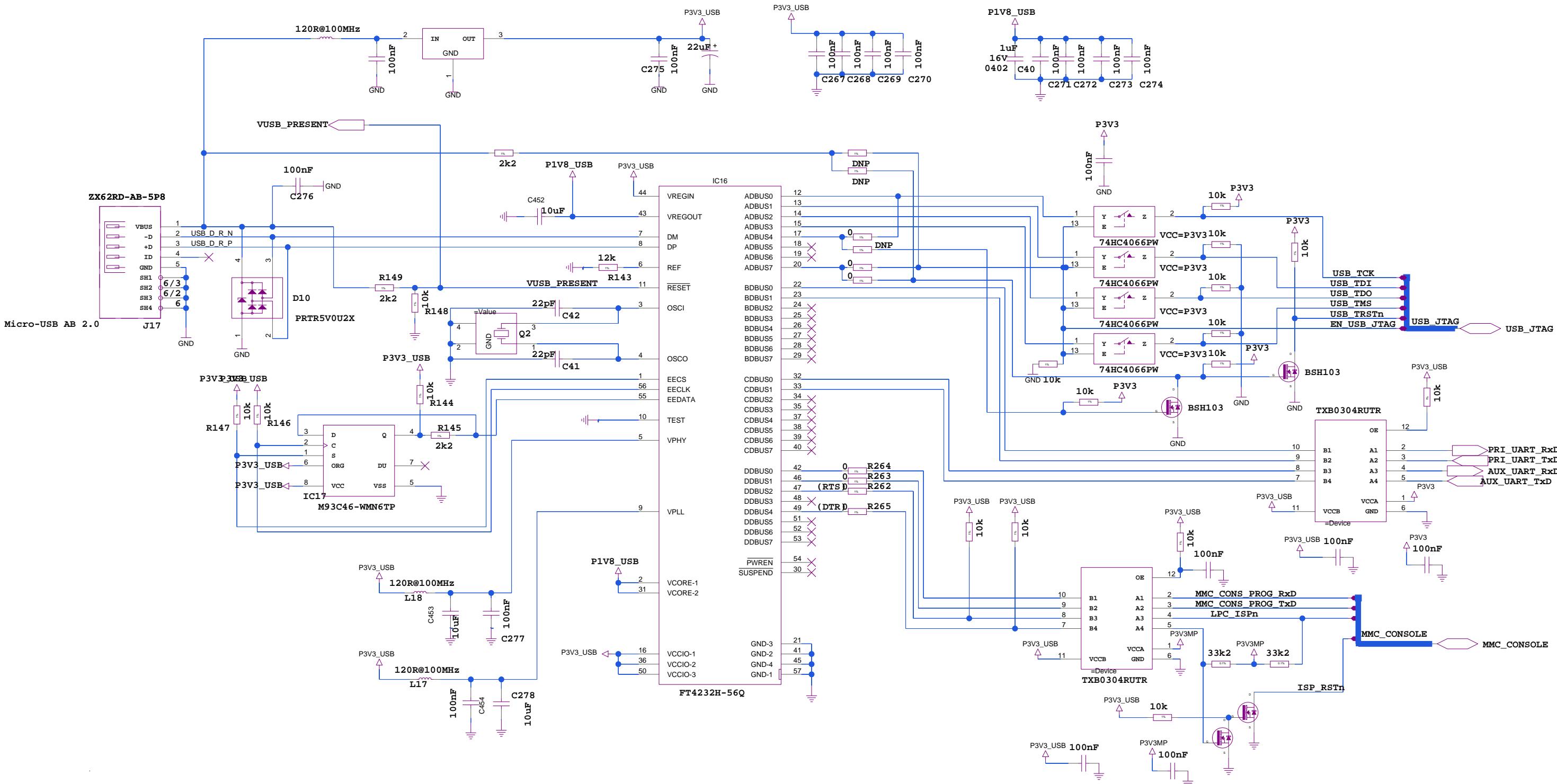
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Thermometers

SIZE	DWG NO	REV
A3		v0.97
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USB_SERIAL_QUAD

SIZE	DWG NO	REV
A3		v0.97
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G.K.	28	29

