

Project/Equipment **ARTIQ/SINARA**

Document **PCB_3U_Kasli.PrjPCB**

Designer **P.K.**

Drawn by **P.K.**

Check by **-**

Last Mod. -

File **FPGA.schdoc**

Print Date **23.11.2017 04:43:13**

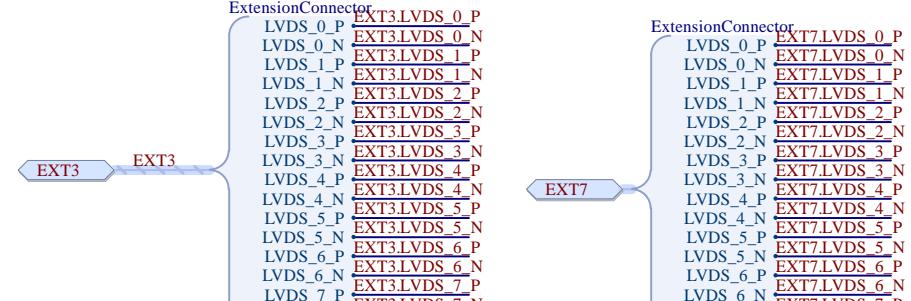
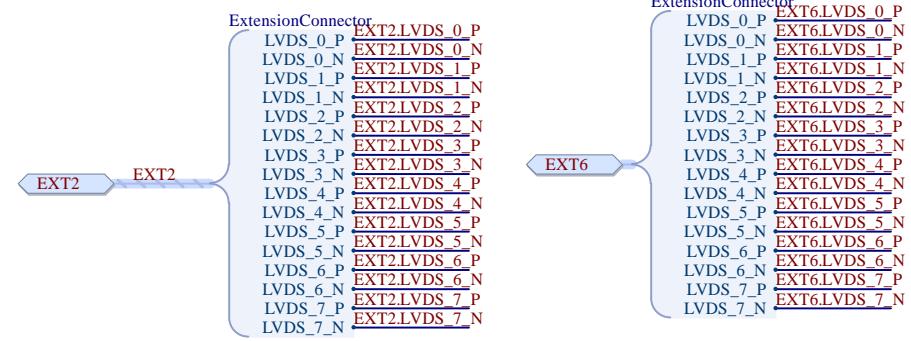
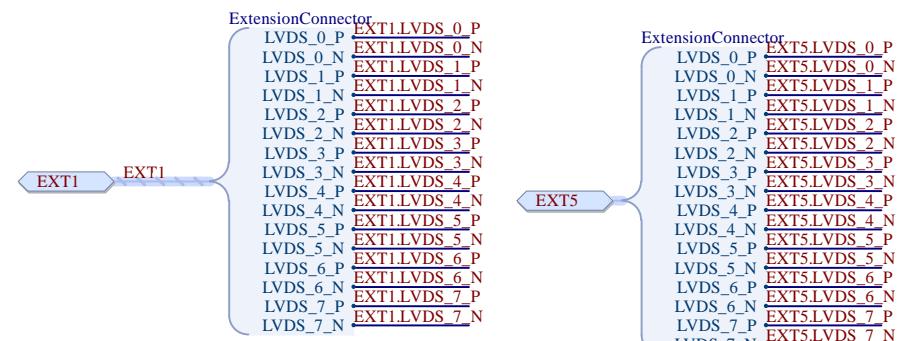
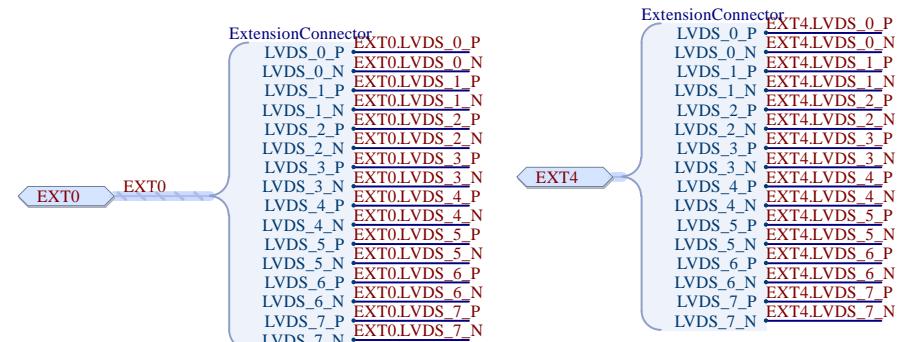
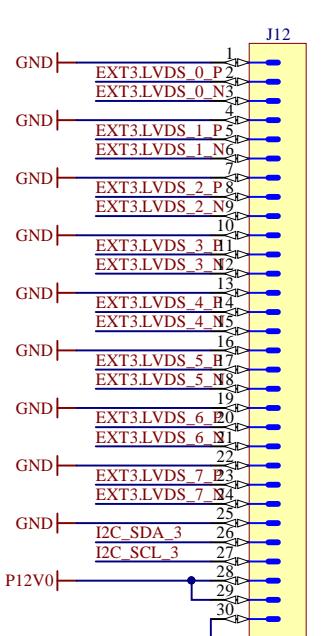
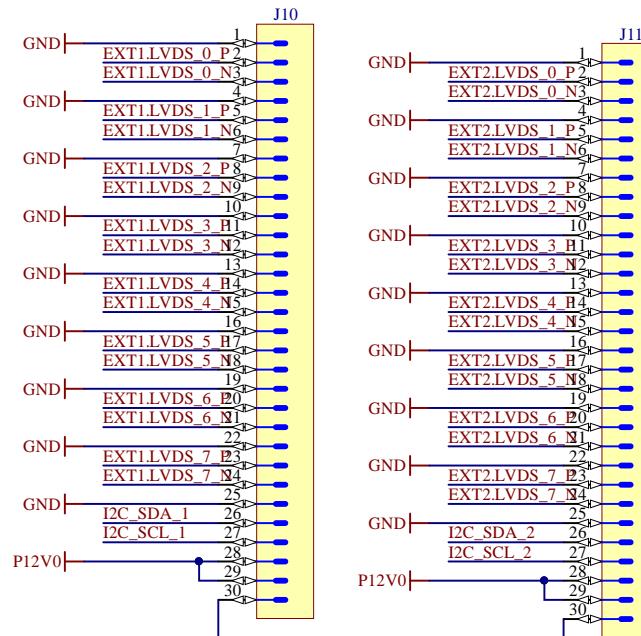
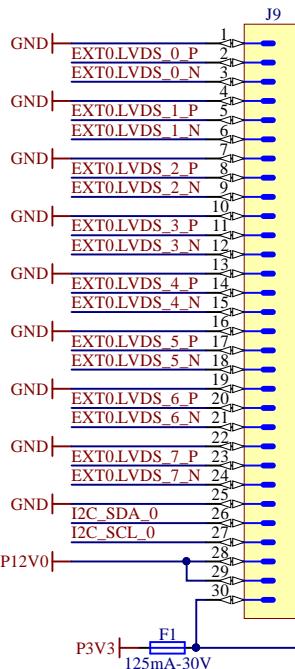
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Size **A3** Rev **1.0**

ARTIQ

Warsaw University of Technology **ISE**

A



E

A

A

B

B

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C

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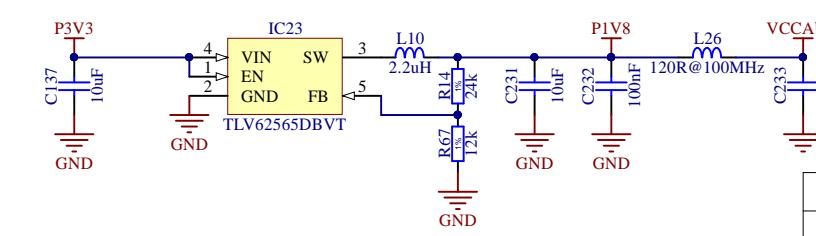
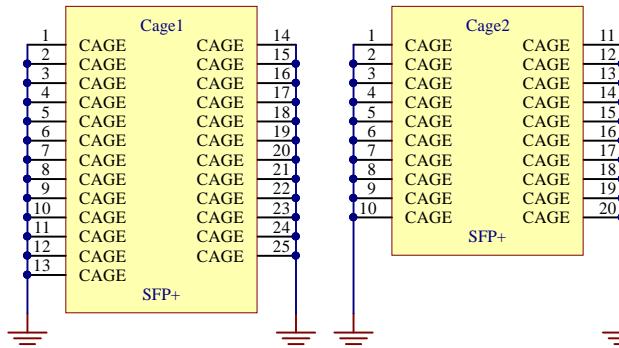
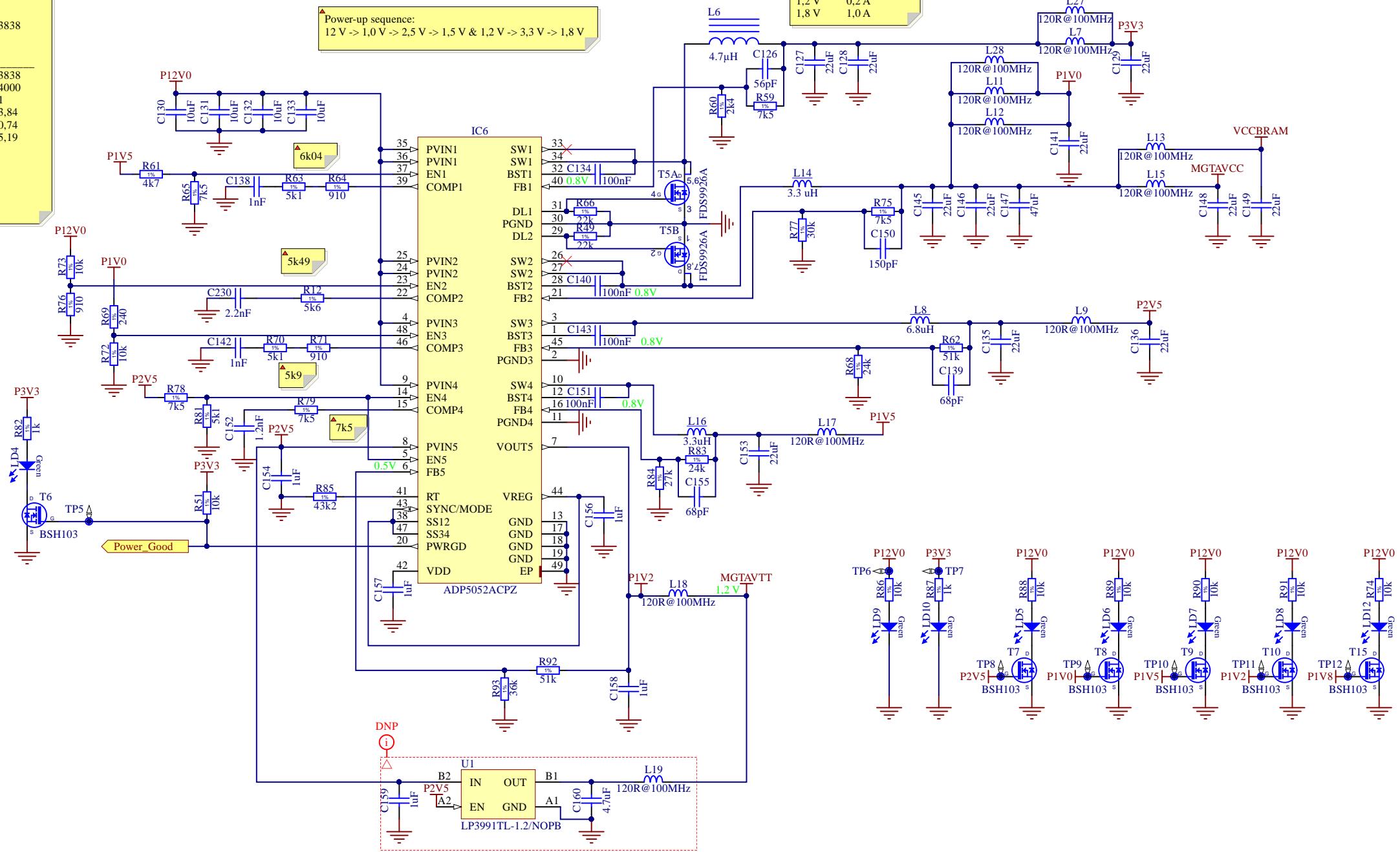
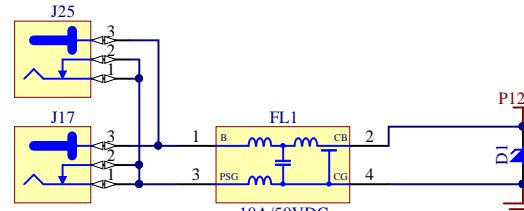
D

E

E

	P3V3	P2V5	P1V8	LDO PIV5	P1V2	P1V0
LED SFP1-3	27					
LED user1, power good, fpga done, 3V3 LED	12					
Any Frequency Clock Multiplier/						
Jitter Attenuator	Si5324	279				
Clock Fanout Buffer	ADCLK944B	138				
Clock Fanout Buffer	ADCLK948B	330				
Extensions, powered by Kasli (I2C power) x12		240				
DDR Termination Regulator	TPS51200	40				
SFP+ 6.25gb 3x		900				
Level-Shifting I2C Repeater	TCA9517 x4	20				
I2C Switch	TCA9548	80				
Level-Shifting Bus Transceiver	SN74AVC2T245 x9	216				
50 MHz Oscillator	636L3I050M00000	25				
FPGA memory	S25FL128SAGBHIA	100				
125 MHz LVDS clock510FBA125M000		23				
RAM x16, rev E	MT41K256M16					
Artix 7 FPGA	XC7A100T					
LDO 1V2						
1V8 buck	TLV62565					
	767	971	274	167	3838	
SUM [mA]	3169	790	971	429	167	3838
Current available [mA]	3500	1100	1000	800	200	4000
Voltage [V]	3,3	2,5	1,8	1,5	1,2	1
POWER [W]	10,46	1,98	1,75	0,64	0,20	3,84
Efficiency	0,88	0,78	0,89	0,76	1	0,74
POWER [W]	11,88	2,53	1,96	0,85	0,20	5,19

Total power: 22,61 W
Total P12V0 current: 1,70 A
Maximum P12V0 current: 5 A
P12V0 current left for EEMs: 3,30 A
Maximum P12V0 EEM current via ribbon cable: 1 A



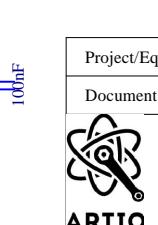
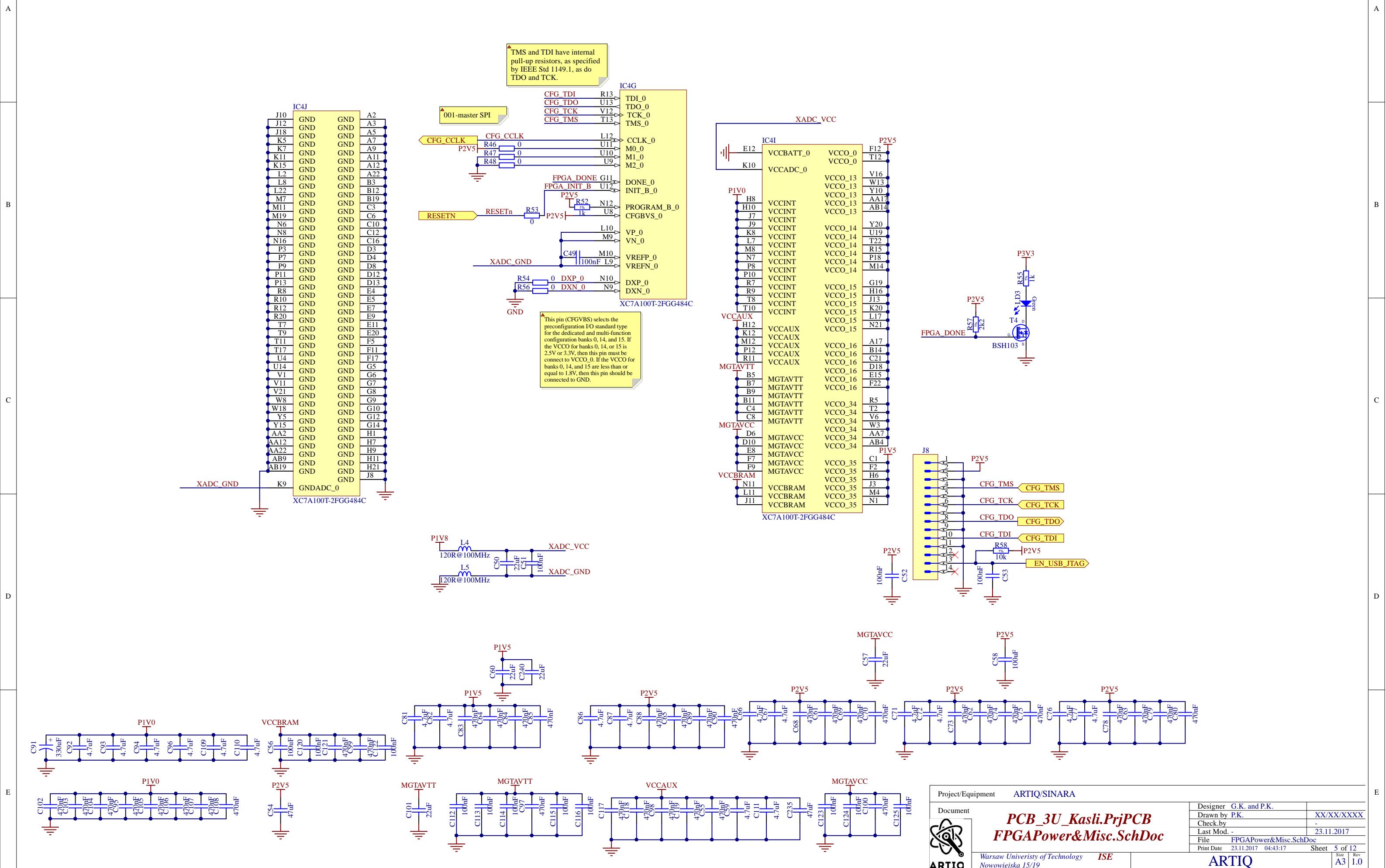
Project/Equipment ARTIQ/SINARA

PCB_3U_Kasli.PjPCB
PowerSupplies.SchDoc

Designer P.K.	
Drawn by P.K.	XX/XX/XXXX
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Last Mod. -	23.11.2017
File PowerSupplies.SchDoc	
Print Date 23.11.2017 04:43:16	
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ARTIQ



Project/Equipment
Document
ARTIQ/SINARA
PCB_3U_Kasli.PrjPCB
FPGAPower&Misc.SchDoc

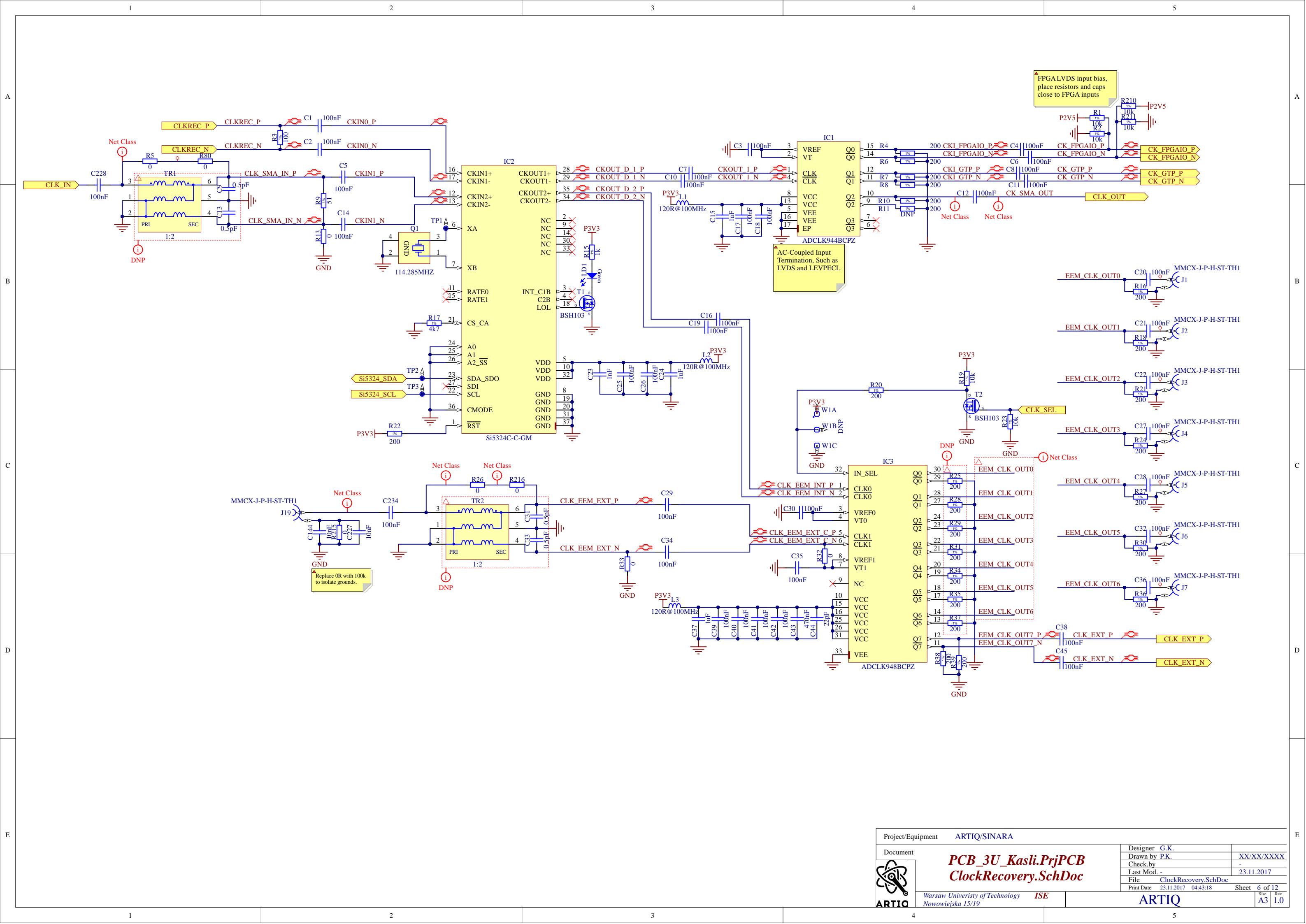
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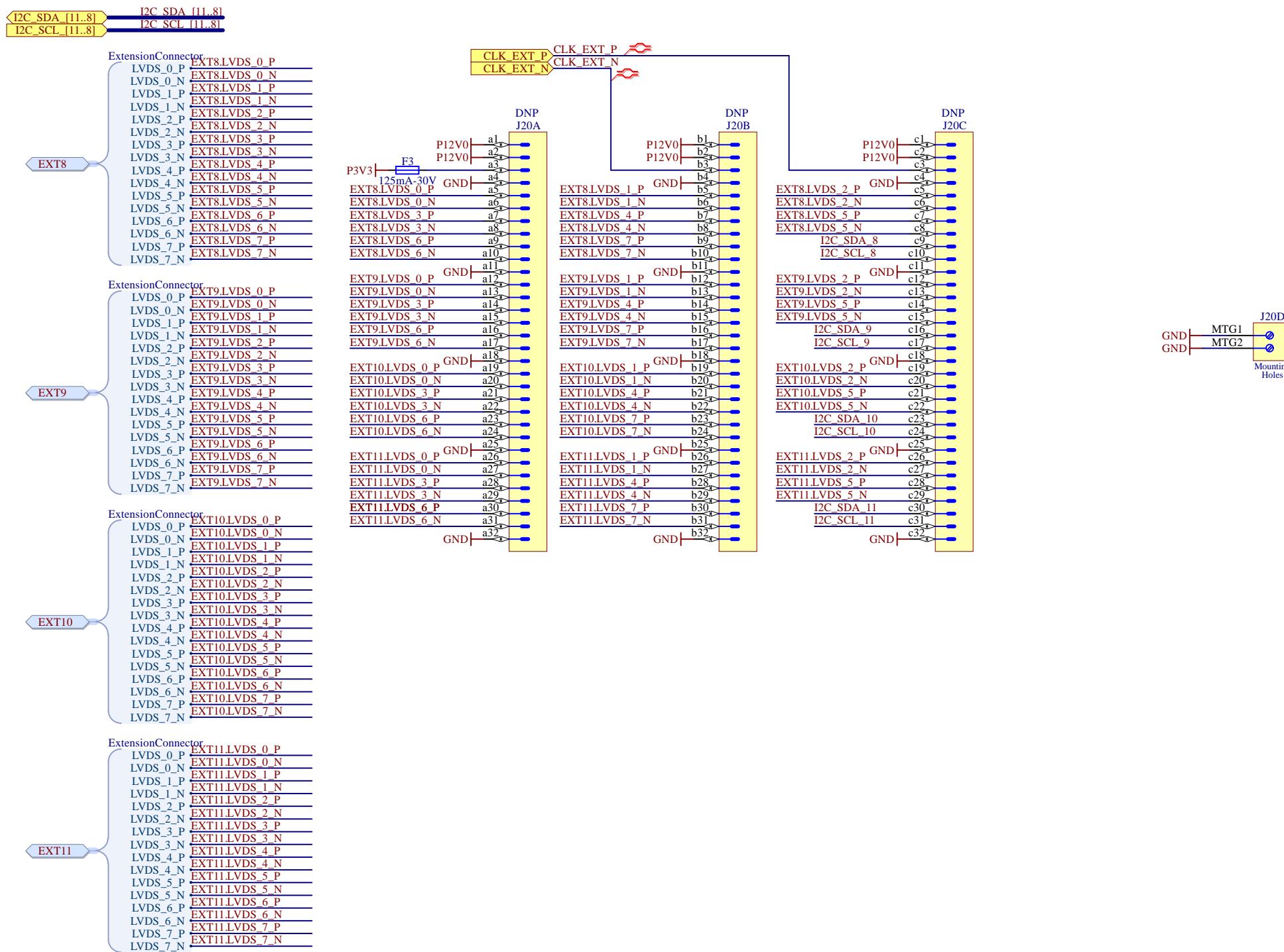
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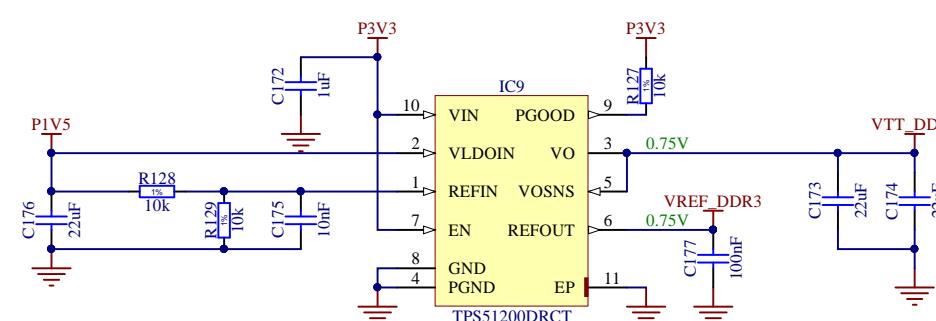
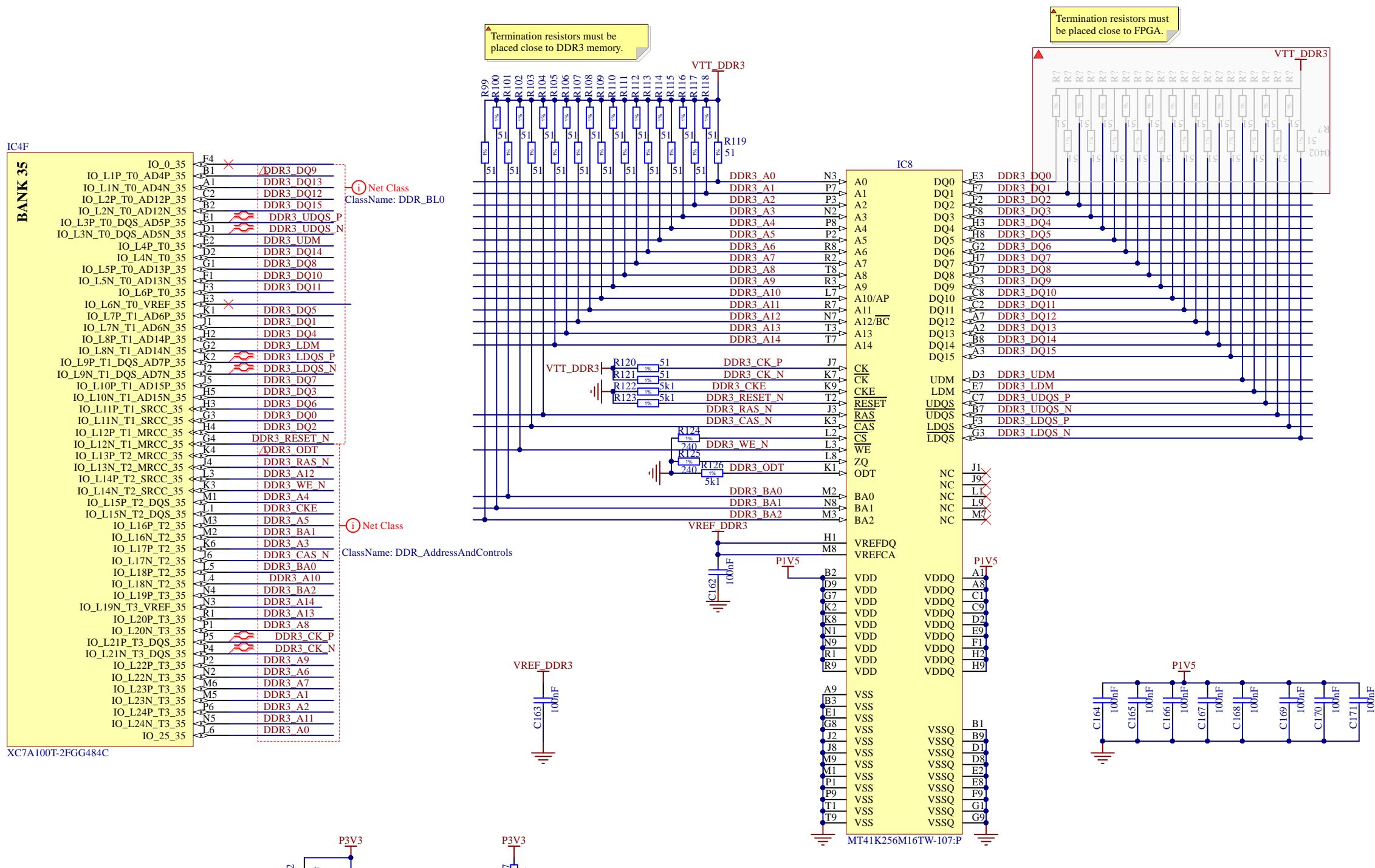
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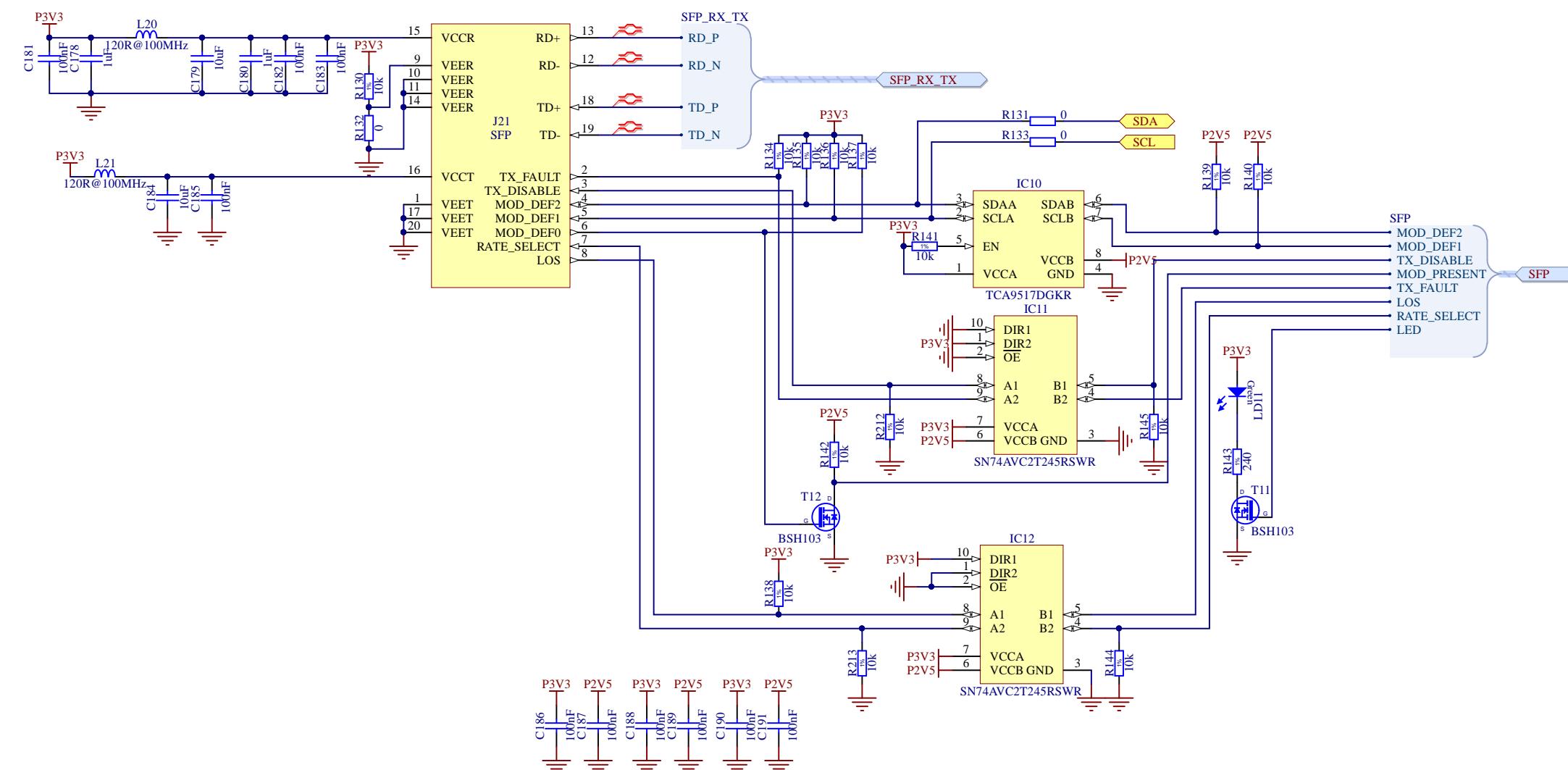
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ARTIQ

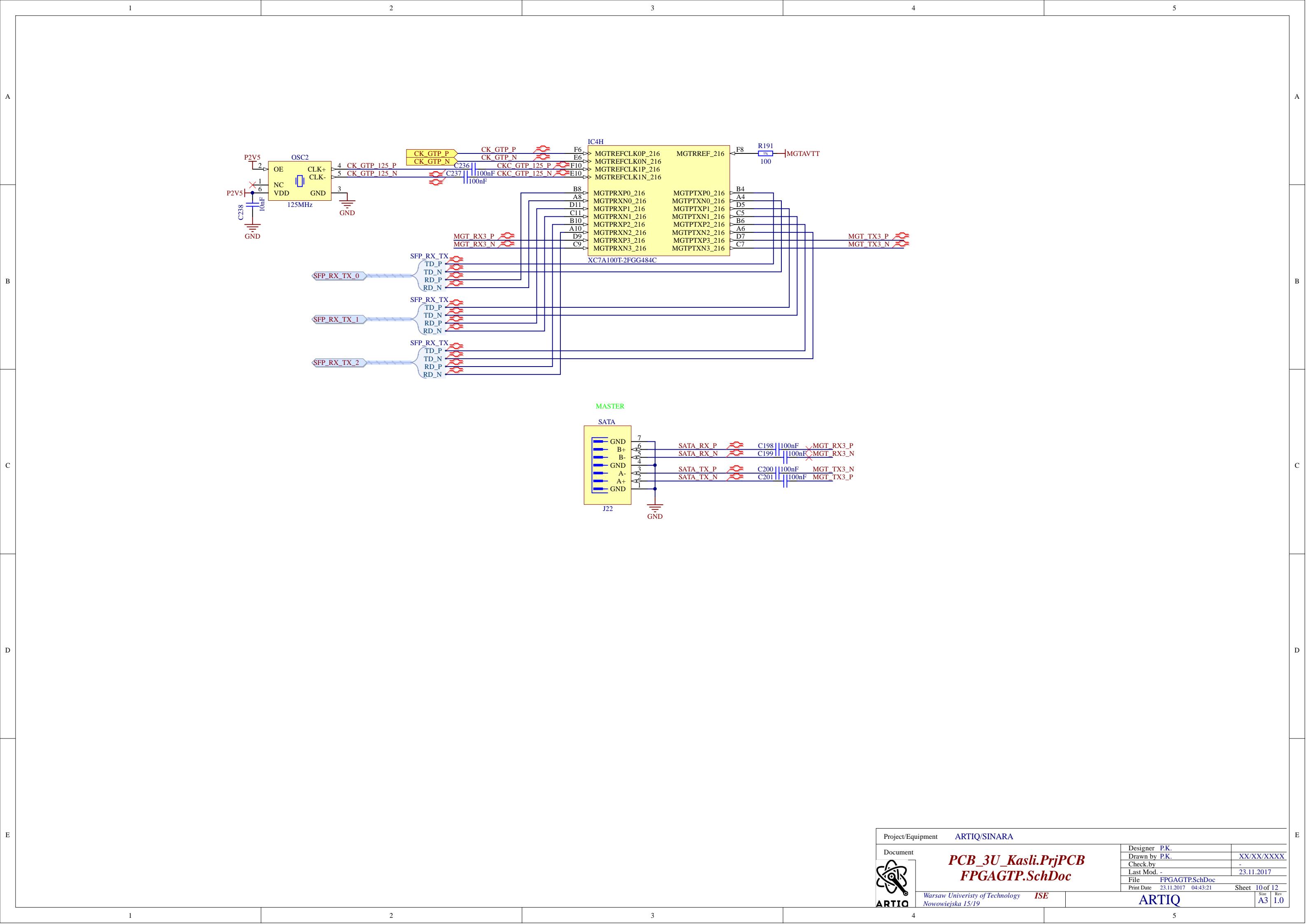








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	Warsaw University of Technology ISE Nowowiejska 15/19	ARTIQ	



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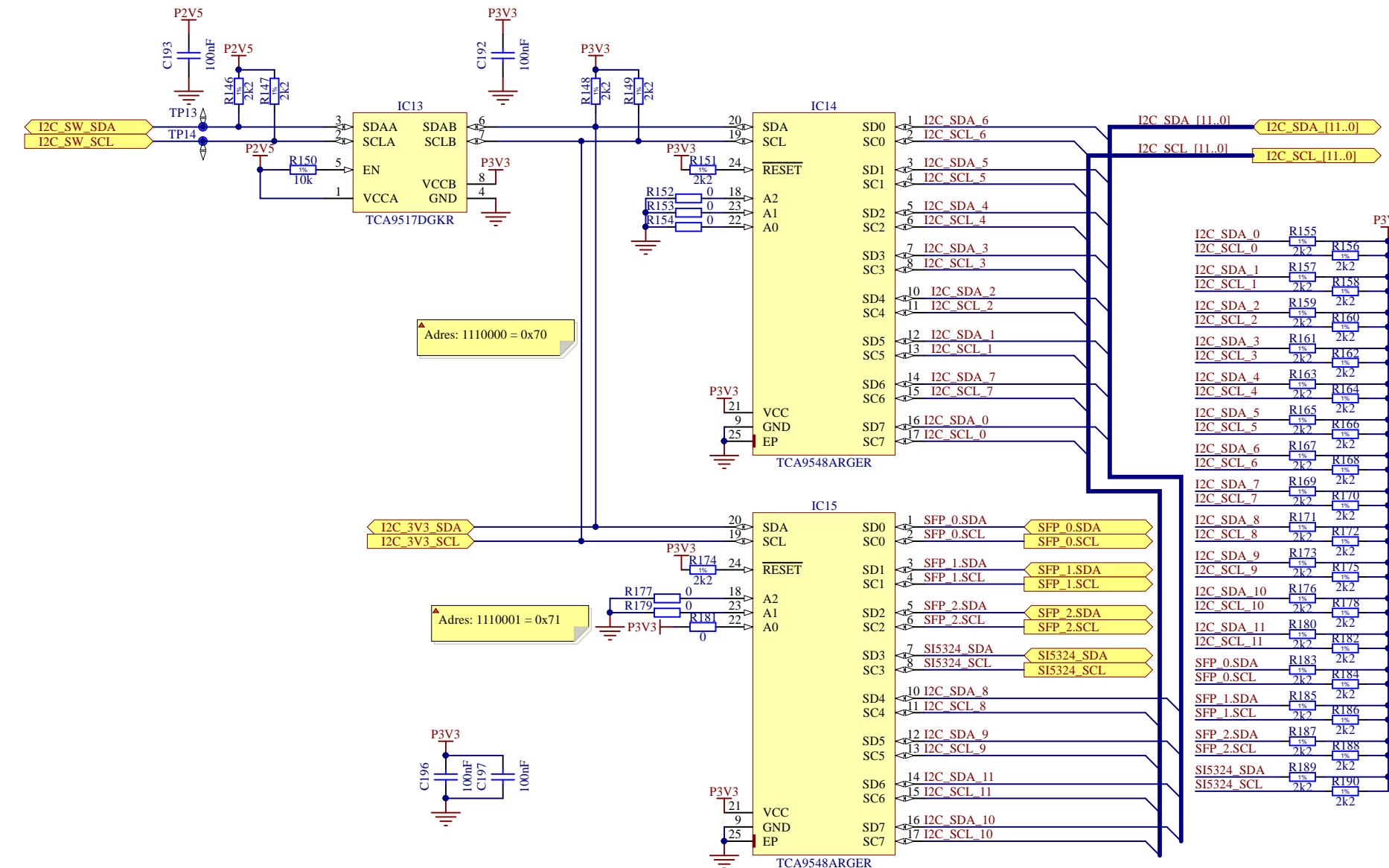
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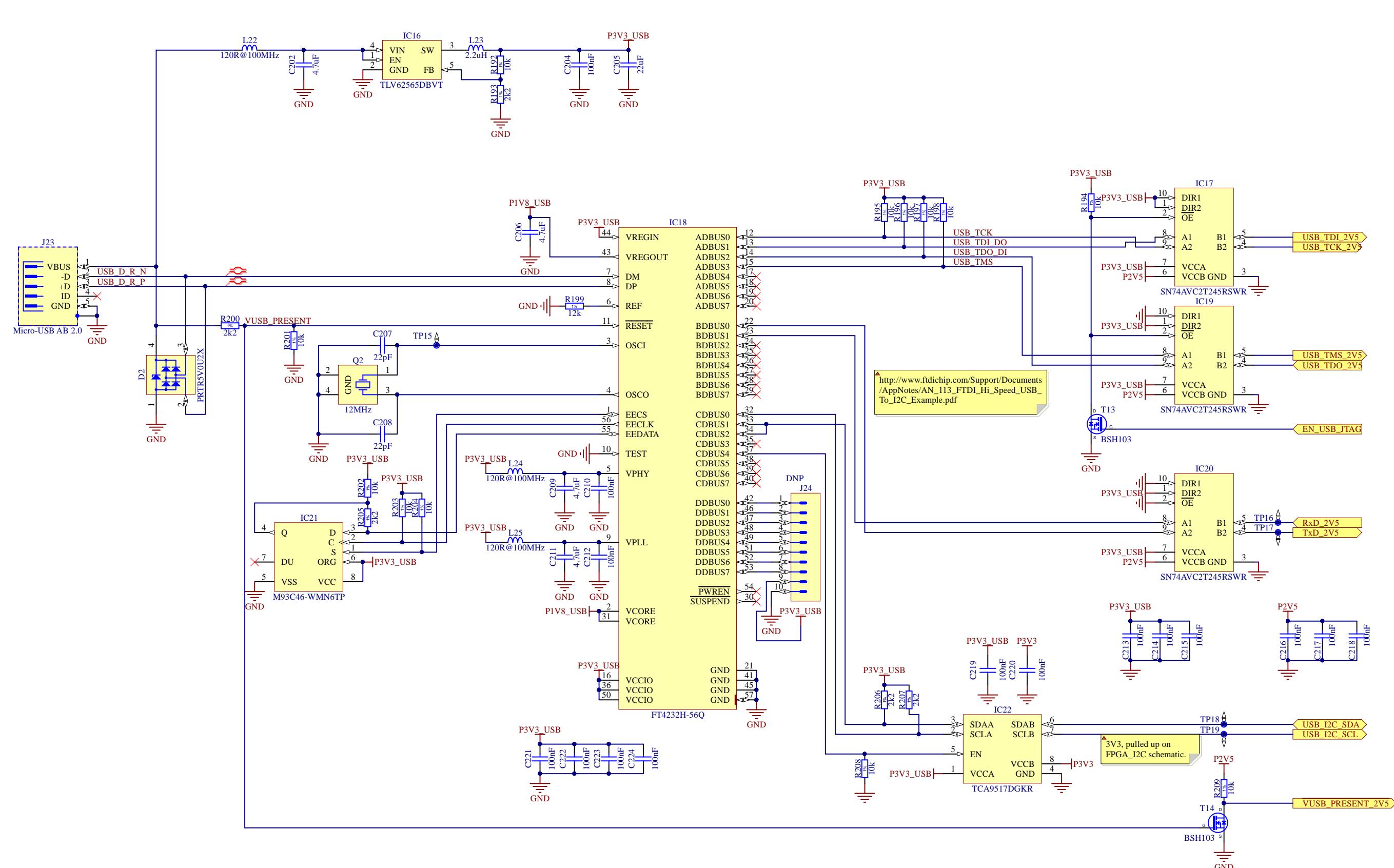
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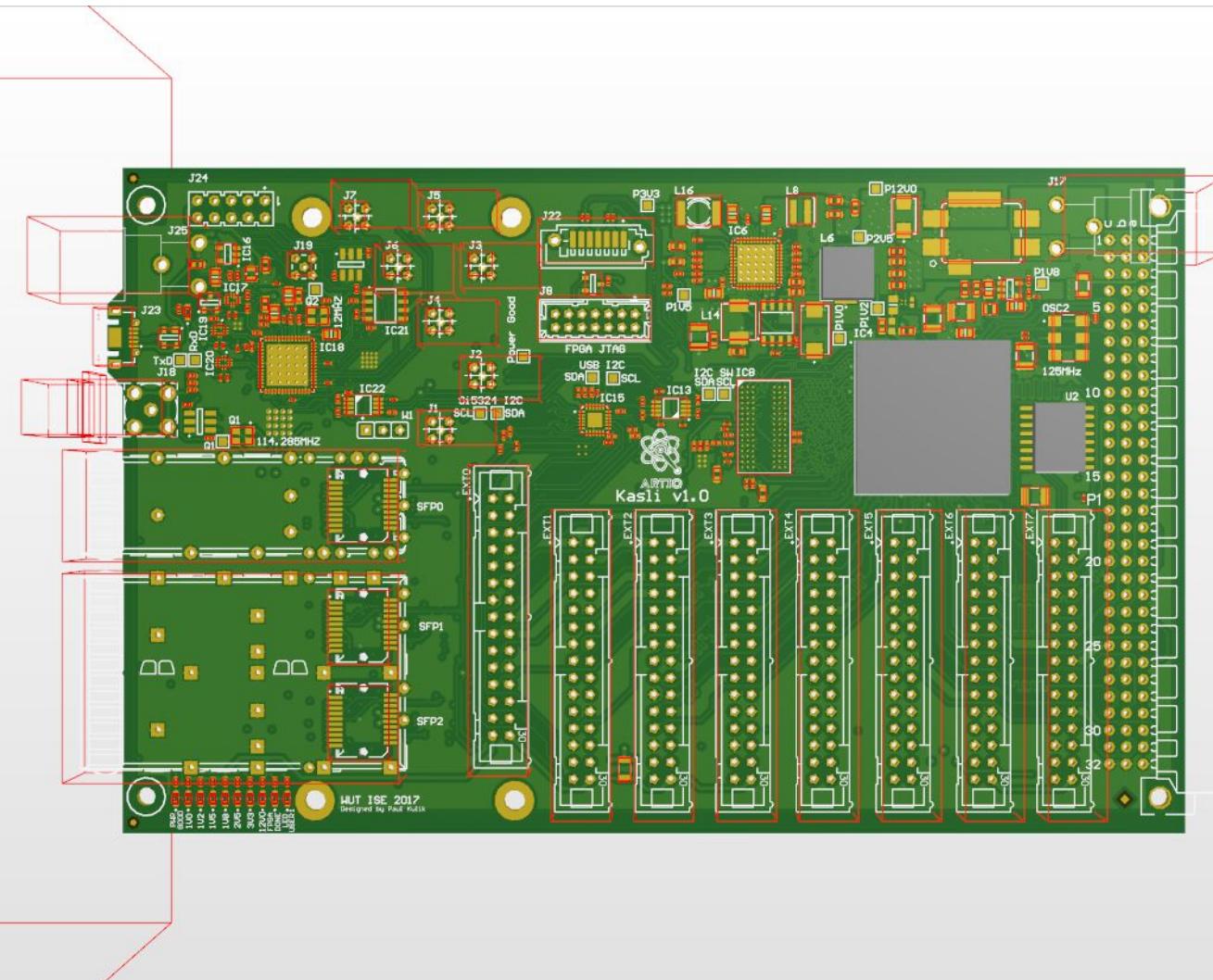
E

E

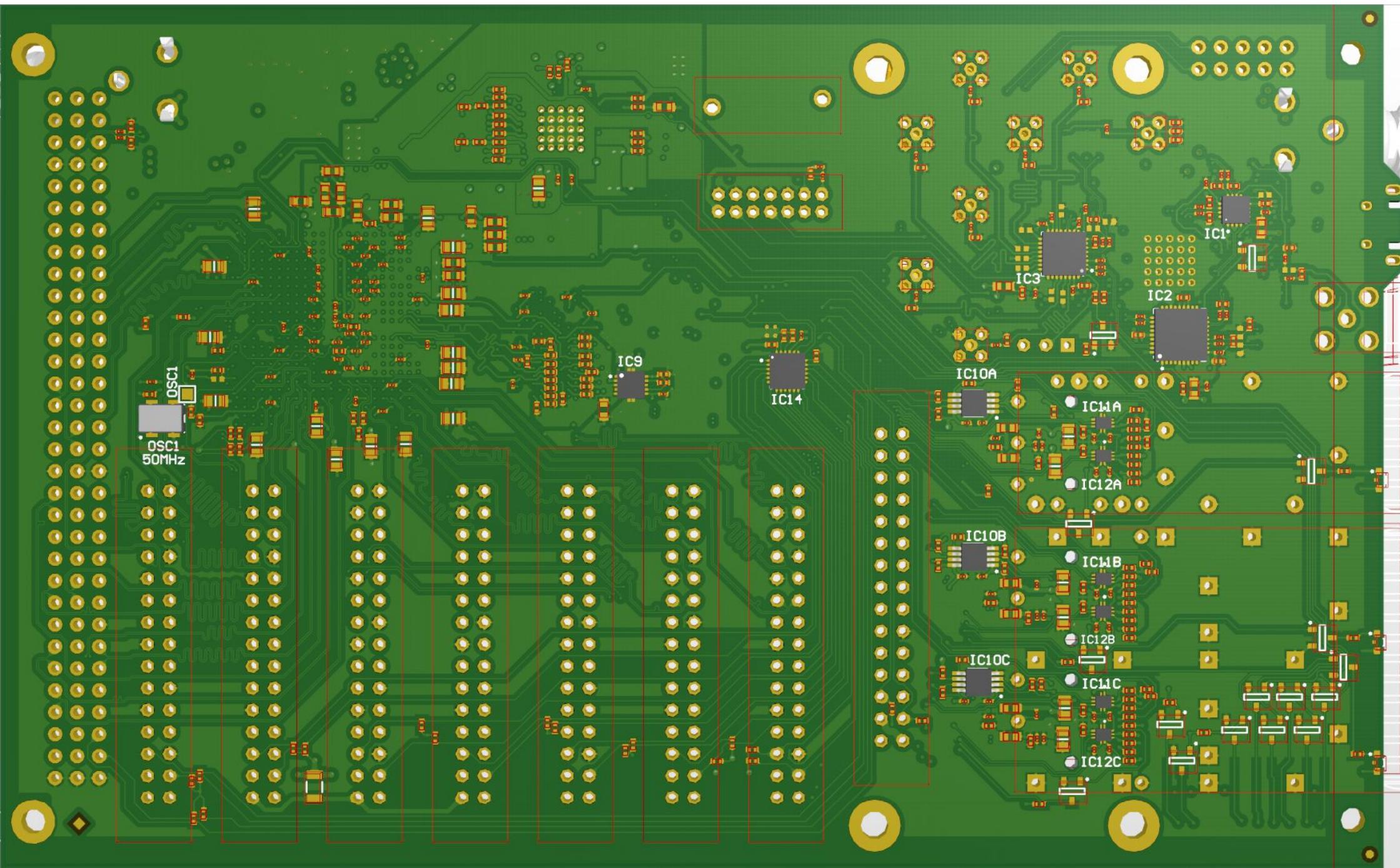


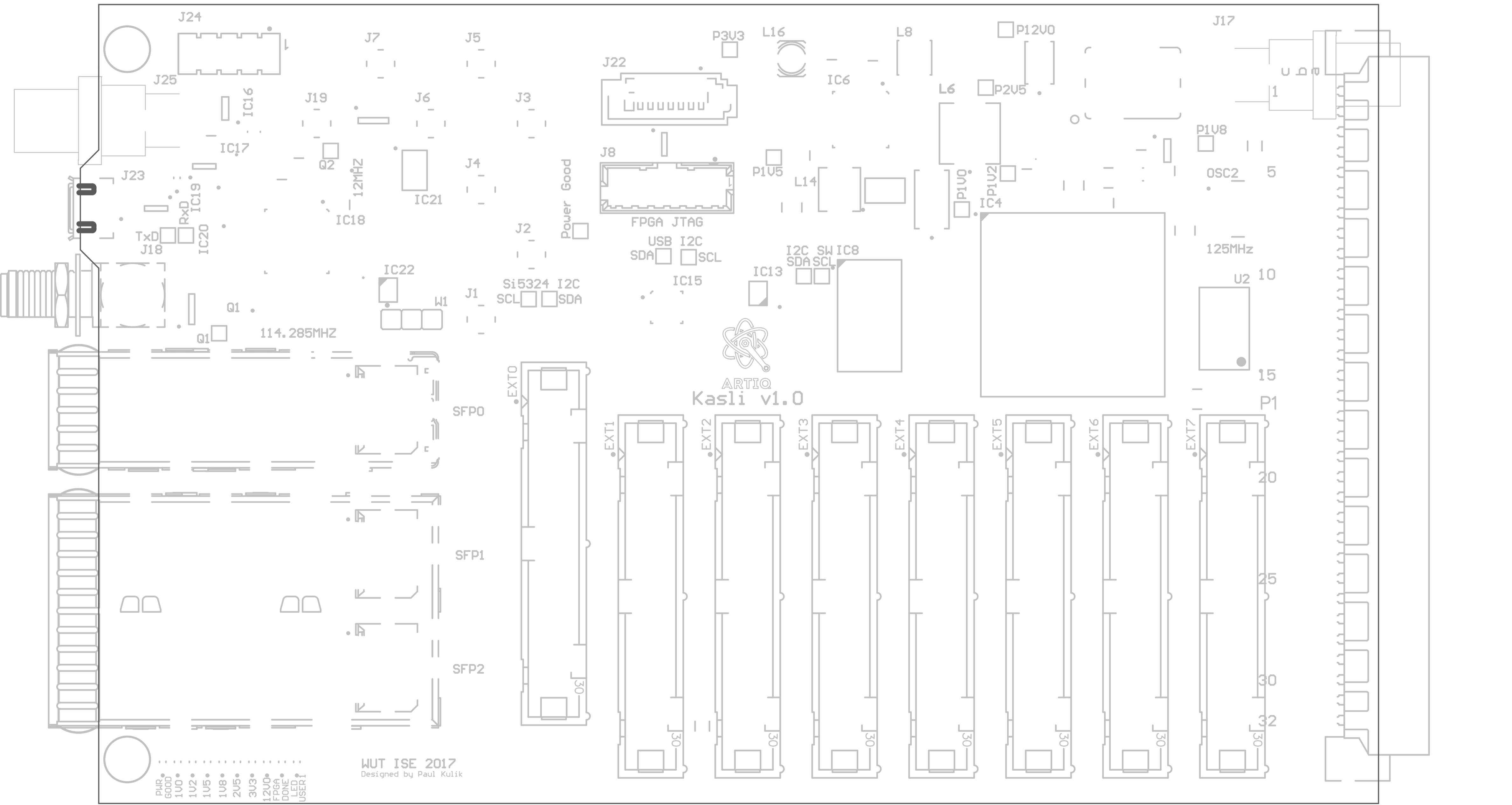
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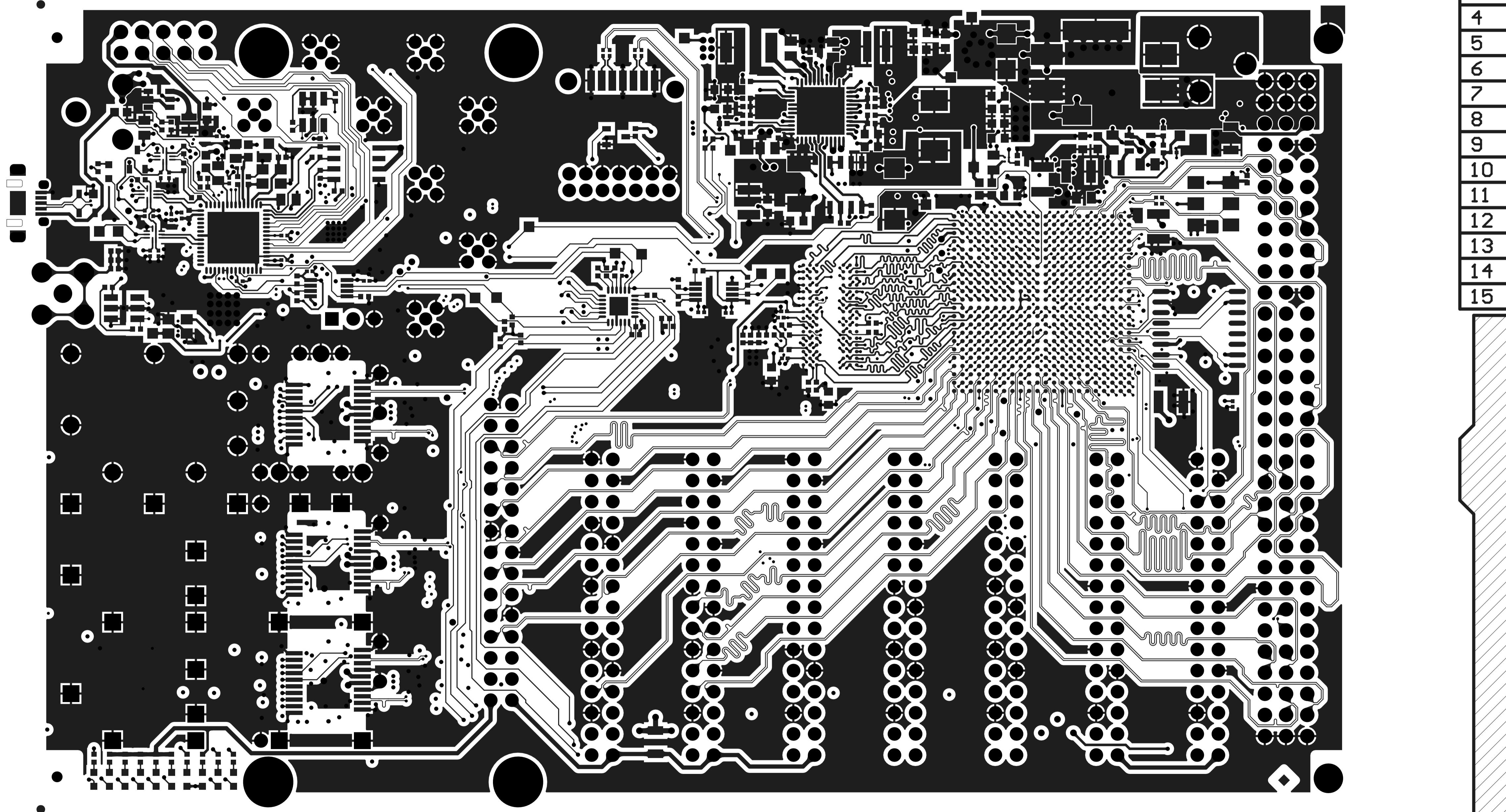




Layer	Name	Material	Thickness
1	TopOverlay		
2	TopSolder	Solder Resist	0,8
3	TopLayer	Copper	2,0
4	Dielectric1	FR-4	4,3
5	MidLayer1	Copper	0,7
6	Dielectric2	FR-4	7,8
7	MidLayer2	Copper	0,7
8	Dielectric3	FR-4	28,
9	SignalLayer1	Copper	0,7
10	Dielectric4	FR-4	7,8
11	Internal Plane 1	Copper	0,7
12	Dielectric5	FR-4	4,3
13	BottomLayer	Copper	2,0
14	BottomSolder	Solder Resist	0,8
15	BottomOverlay		







Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	TopOverlay				
2	TopSolder	Solder Resist	0,89mil	3,5	
3	TopLayer	Copper	2,09mil		
4	Dielectric1	FR-4	4,33mil	4,2	
5	MidLayer1	Copper	0,71mil		
6	Dielectric2	FR-4	7,87mil	4,2	
7	MidLayer2	Copper	0,71mil		
8	Dielectric3	FR-4	28,74mil	4,2	
9	SignalLayer1	Copper	0,71mil		
10	Dielectric4	FR-4	7,87mil	4,2	
11	Internal Plane 1	Copper	0,71mil		
12	Dielectric5	FR-4	4,33mil	4,2	
13	BottomLayer	Copper	2,09mil		
14	BottomSolder	Solder Resist	0,89mil	3,5	
15	BottomOverlay				

