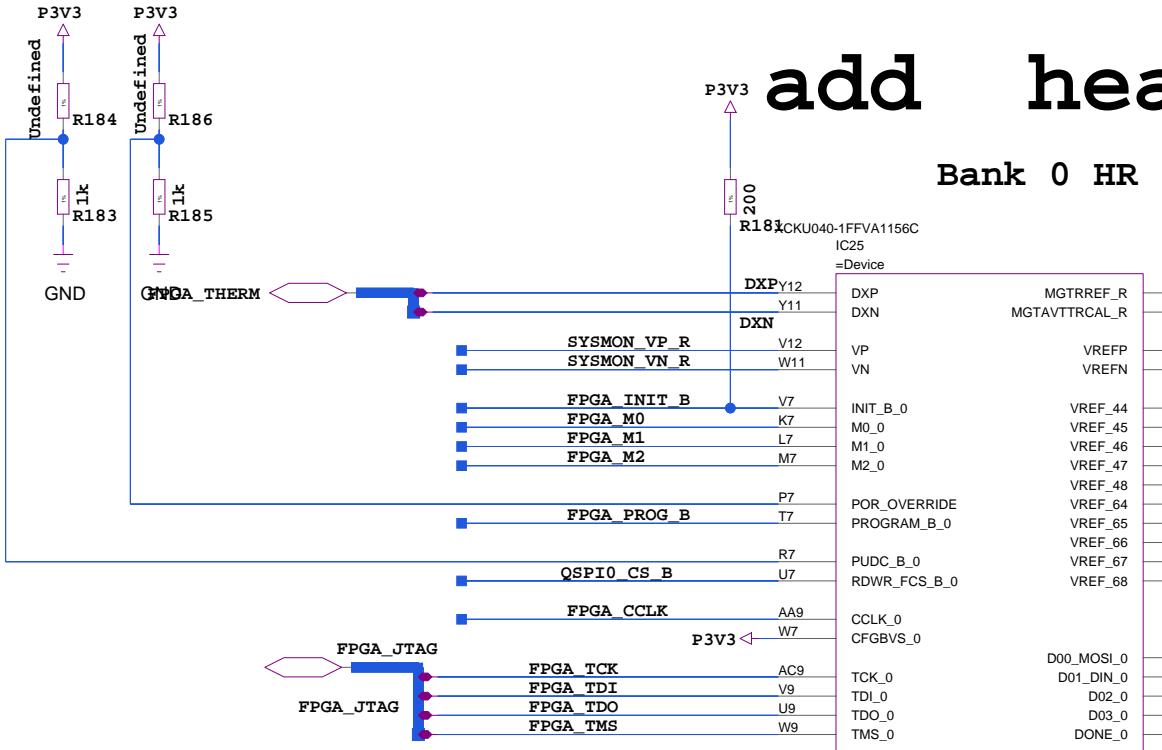


ARTIQ Sinara

Sayma_AMC

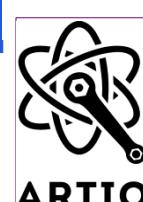
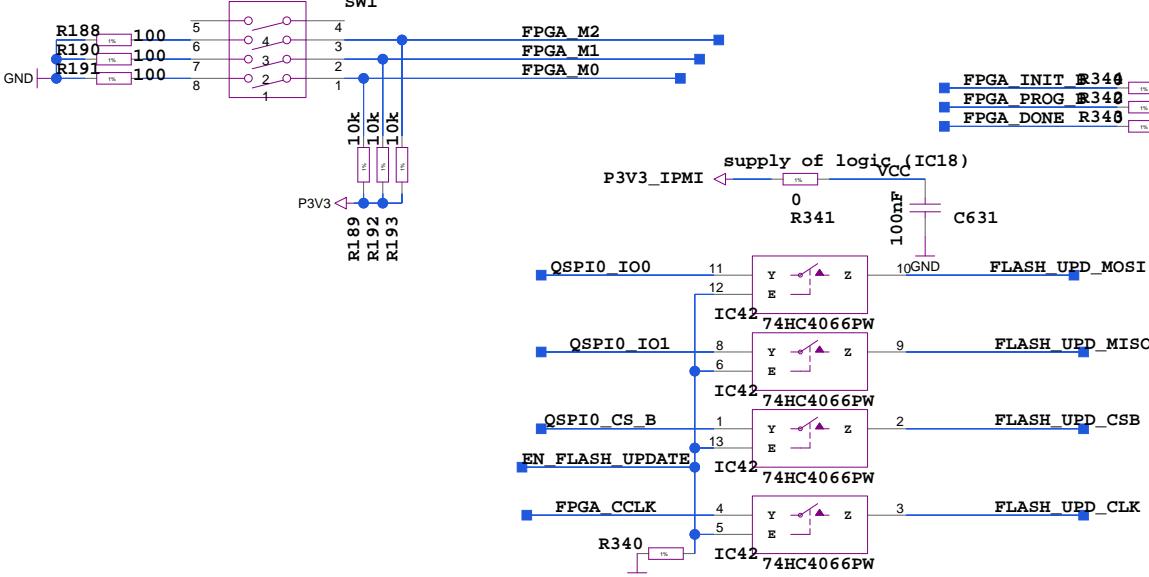
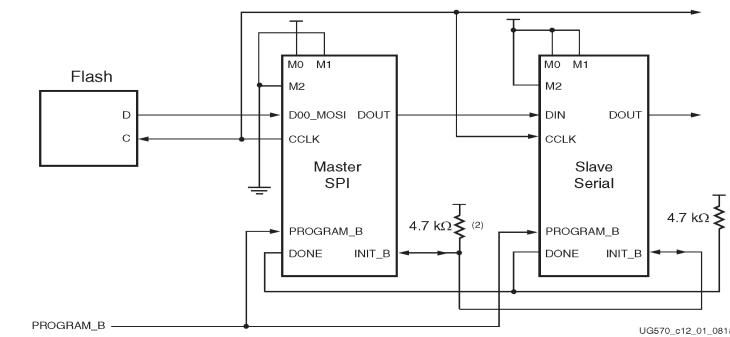
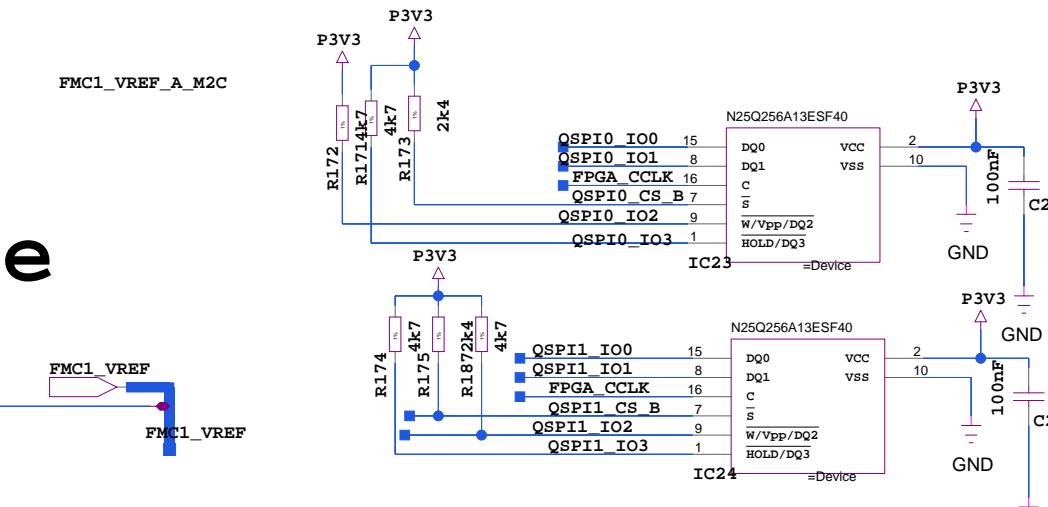
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1M
R1 ESDSTRIP1 1M
R2 ESDSTRIP2



add heatsink here

Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via



FPGA_XCKU040FFVA1156

ARTIQ Sinara

FPGA Bank 0 CFG

A3

G.K.

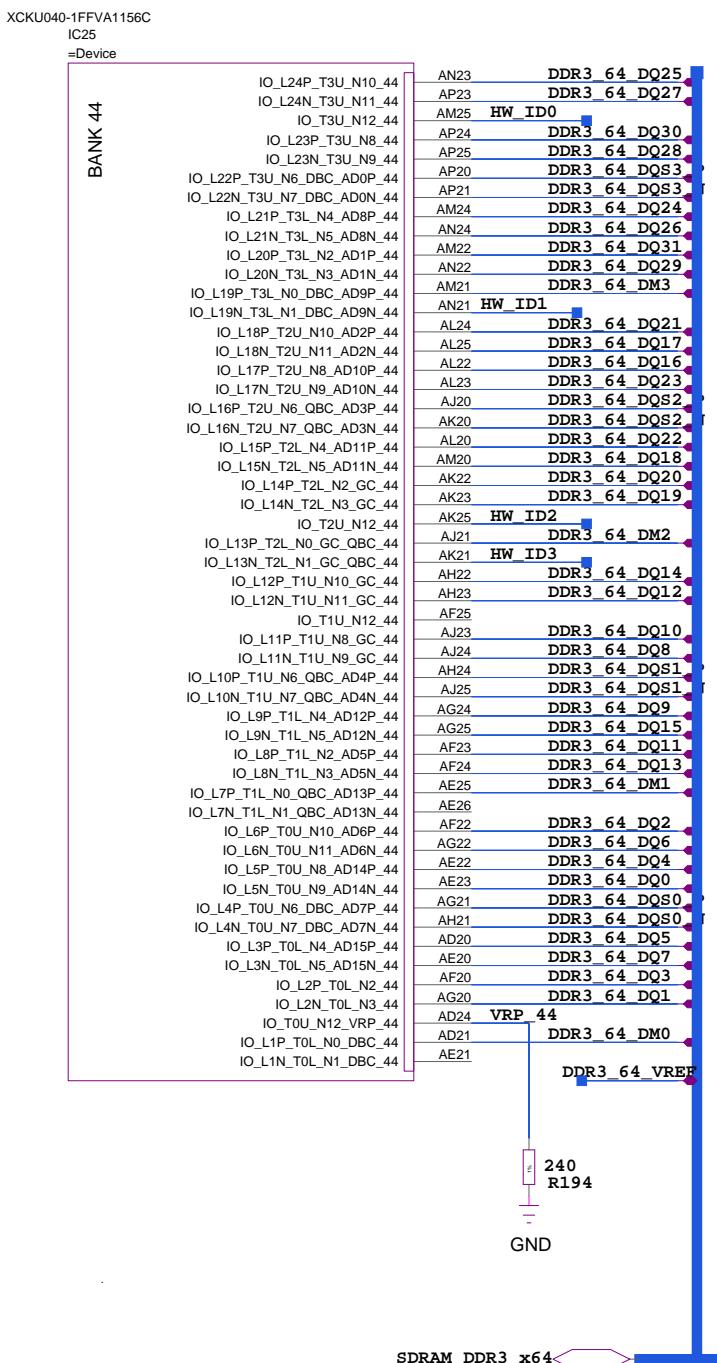
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29

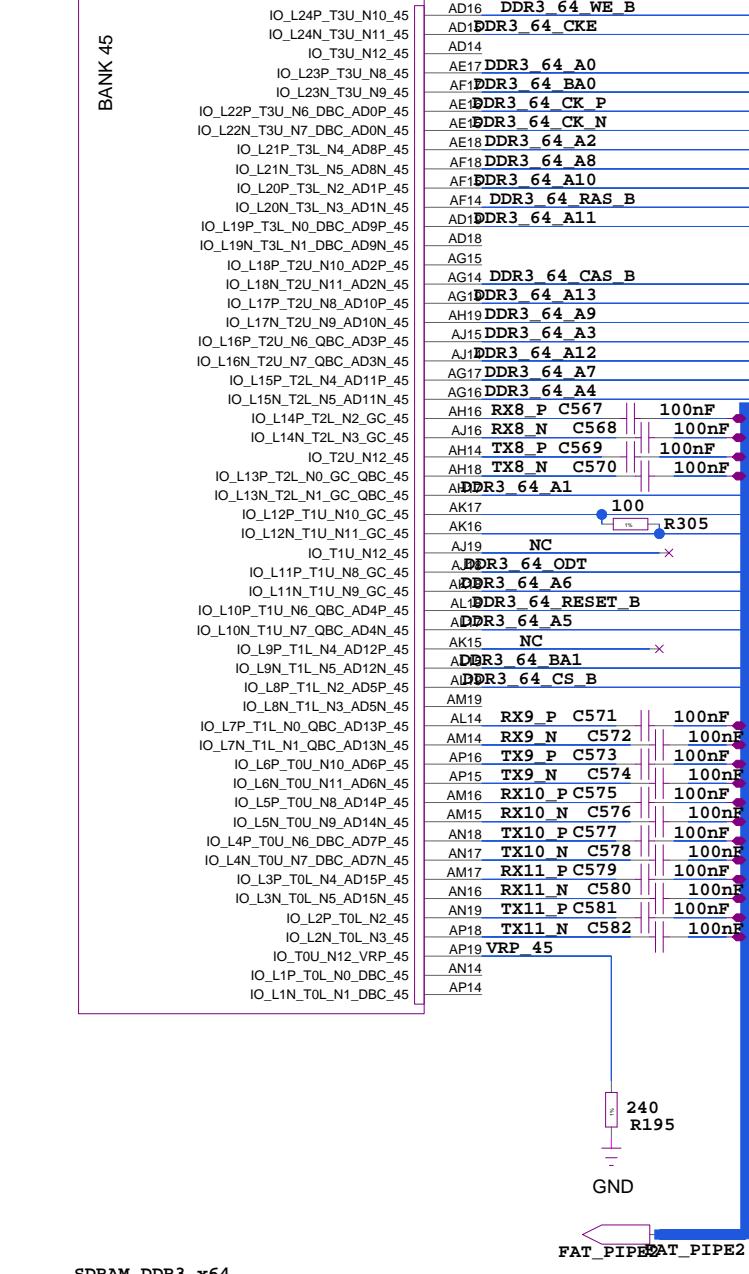
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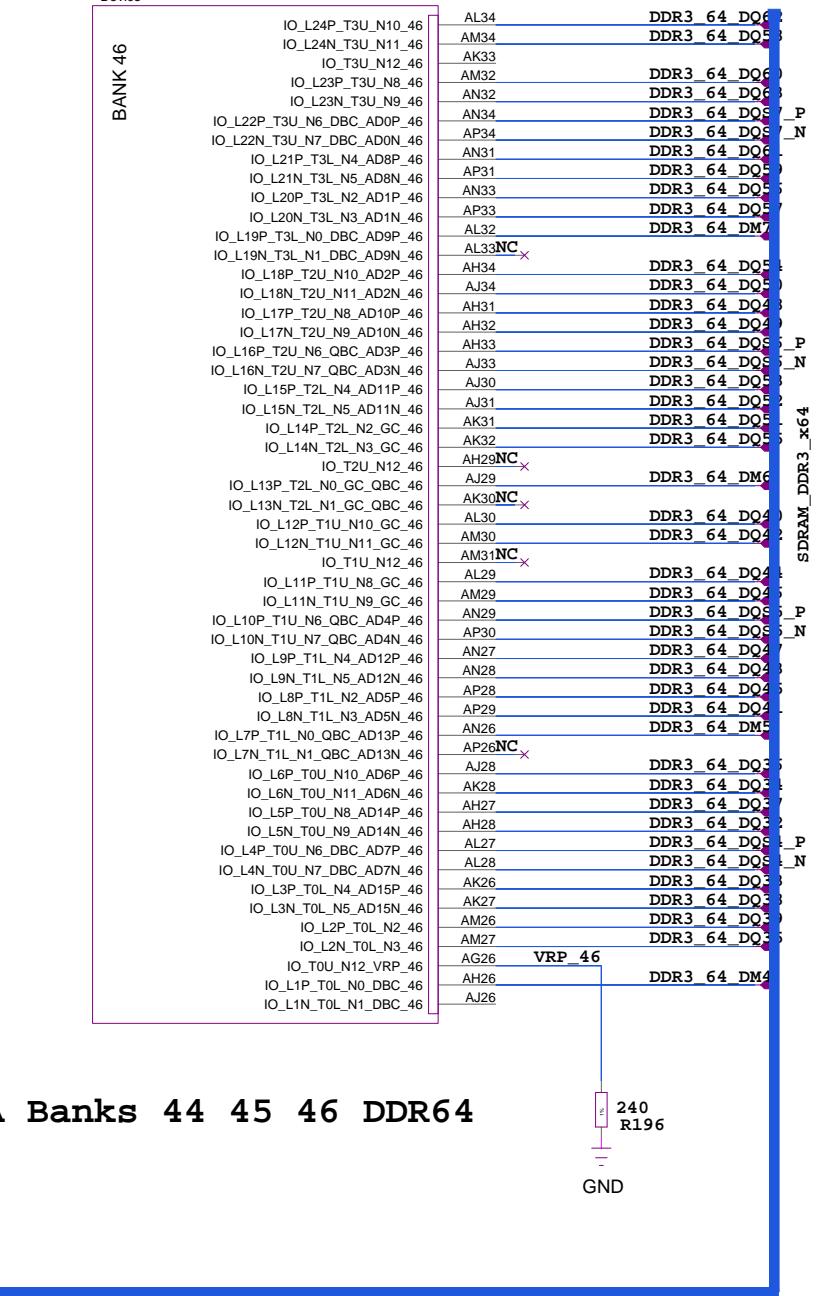
Bank 44 HP



Bank 45 HP

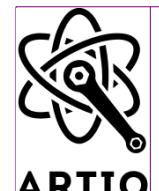


Bank 46 HP



FPGA Banks 44 45 46 DDR64

FPGA_XCKU040FFVA1156



ARTIQ Sinara

FPGA Banks 44 45 46 DDR64

SIZE DWG NO

A3

DRAWN BY

G.K.

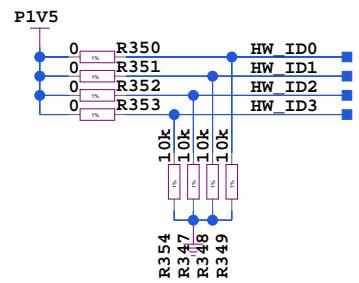
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29

REV

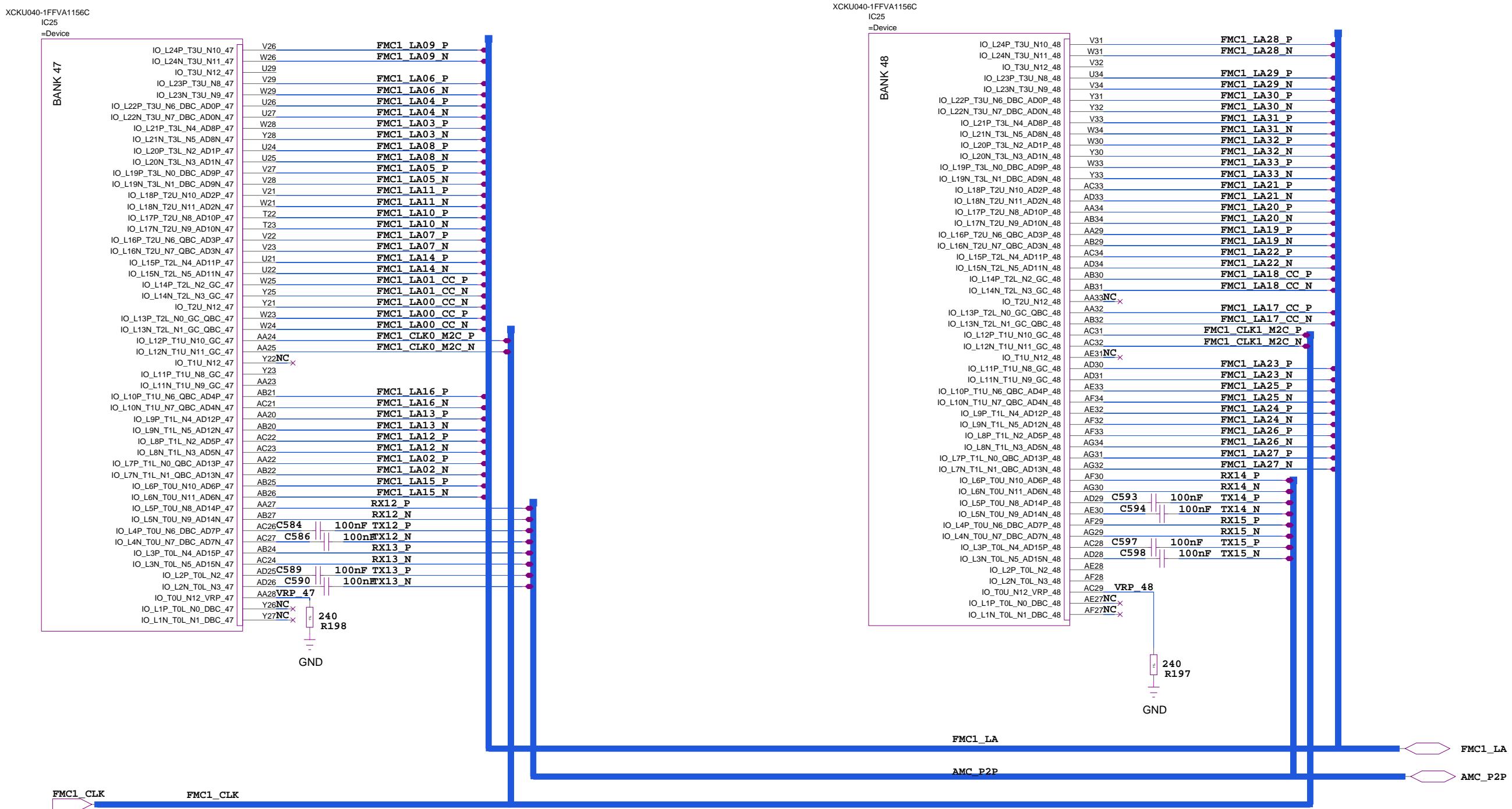
v0.95

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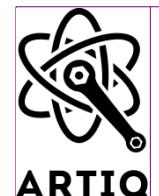


Bank 47 HP

Bank 48 HP



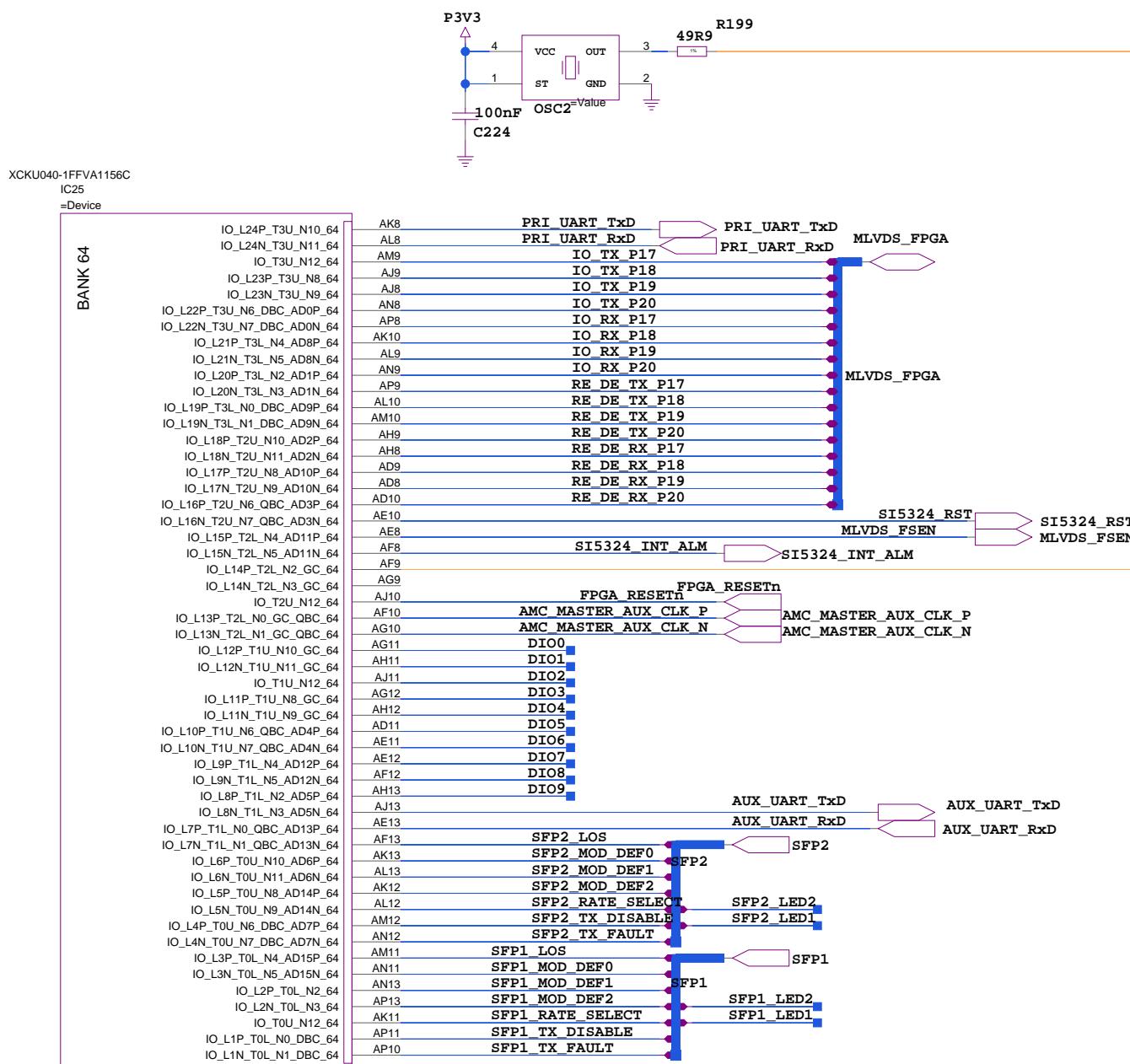
FPGA_XCKU040FFVA1156



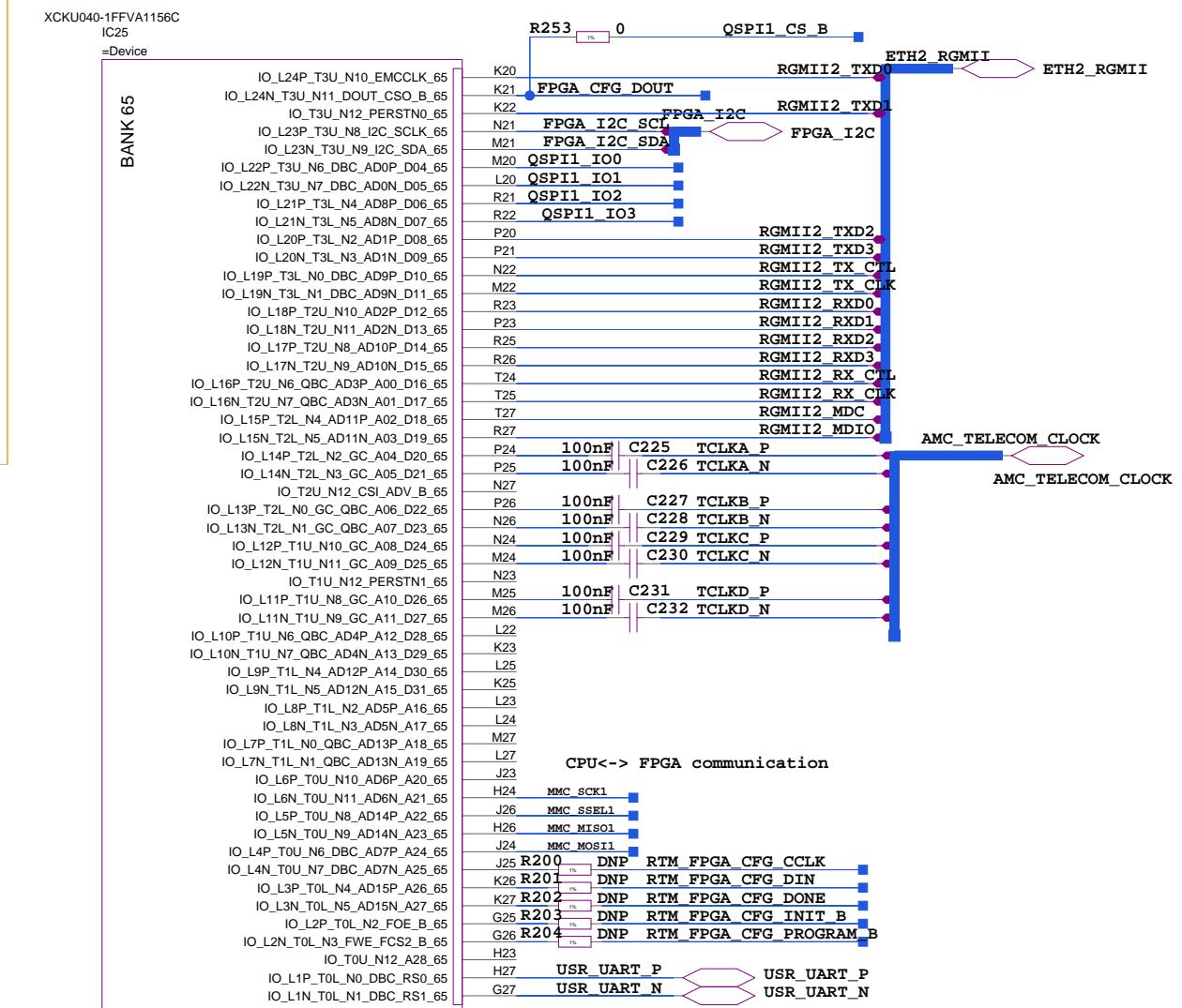
ARTIQ Sinara

FPGA Banks 47 48 HP FM

Bank 64 HR



Bank 65 HR



FPGA_XCKU040FFVA1156



ARTIQ Sinara

FPGA Banks 64 65 HR

SIZE DWG NO

A3

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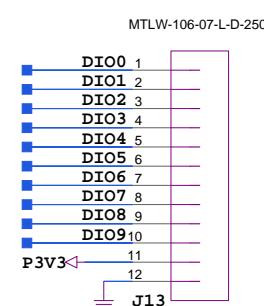
of

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REV

v0.95

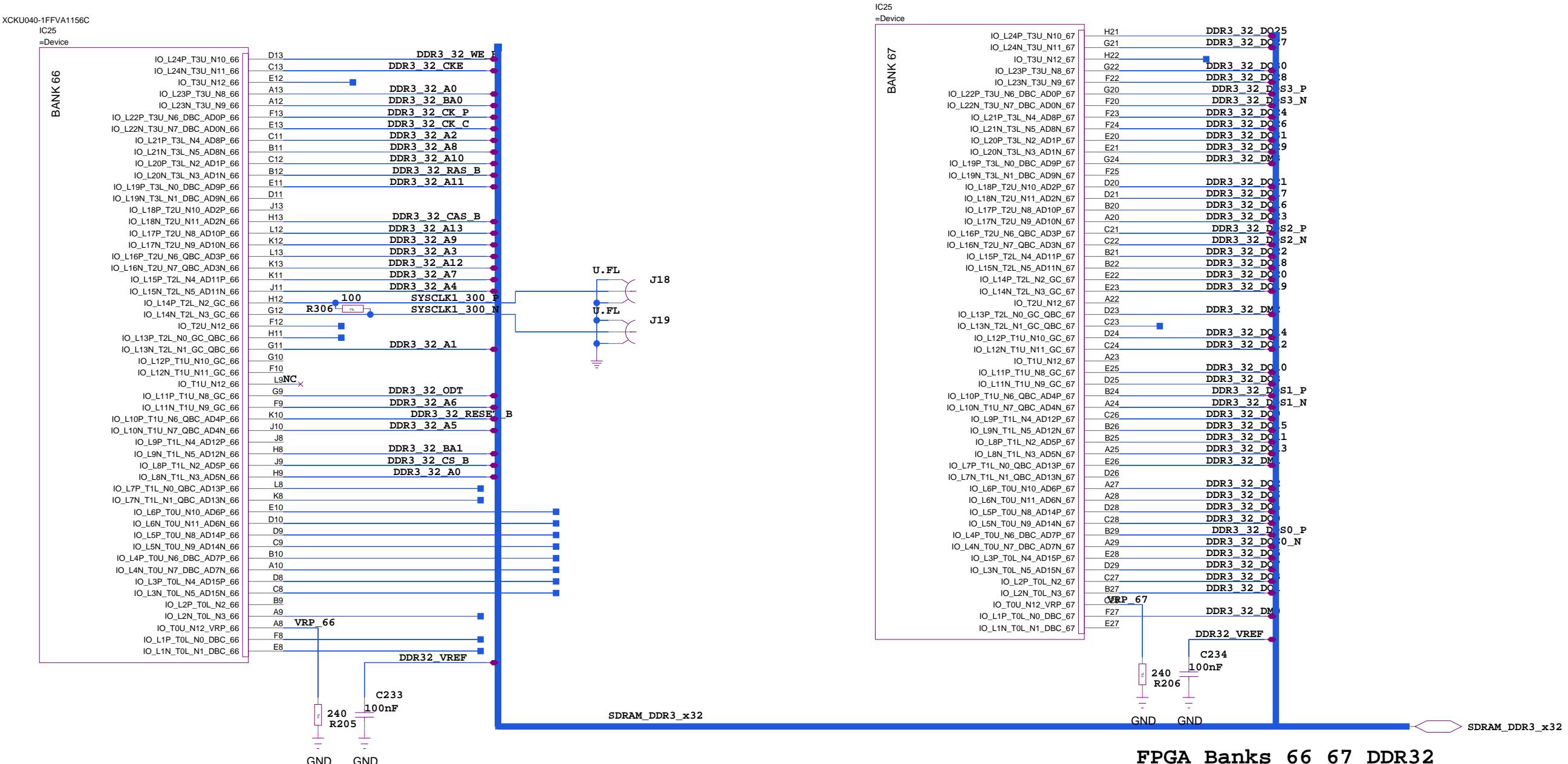
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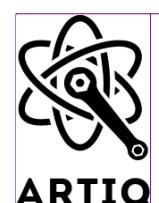
Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

Bank 67 HP

Bank 66 HP



FPGA_XCKU040FFVA1156



ARTIQ Sinara

FPGA Banks 66 67 DDR32

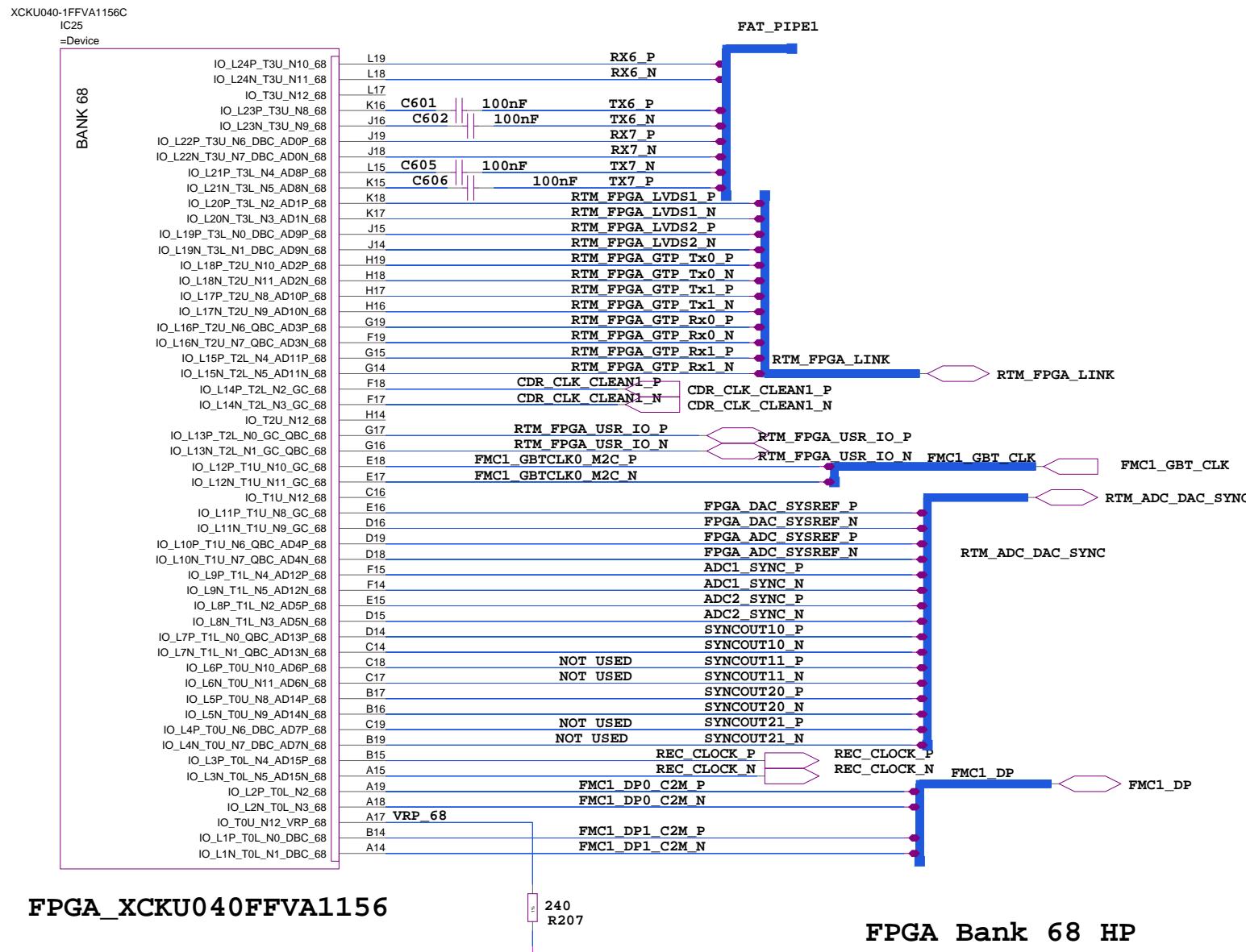
SIZE	DWG NO
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6	29

REV v0.95

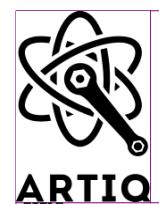
01/12/2016:18:22

Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

Bank 68 HP



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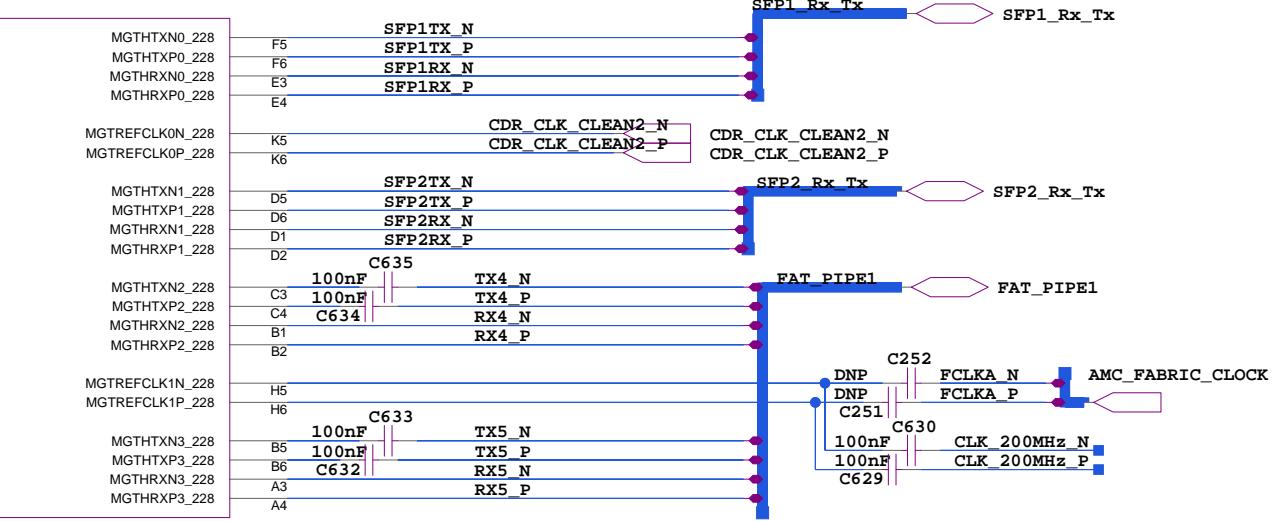
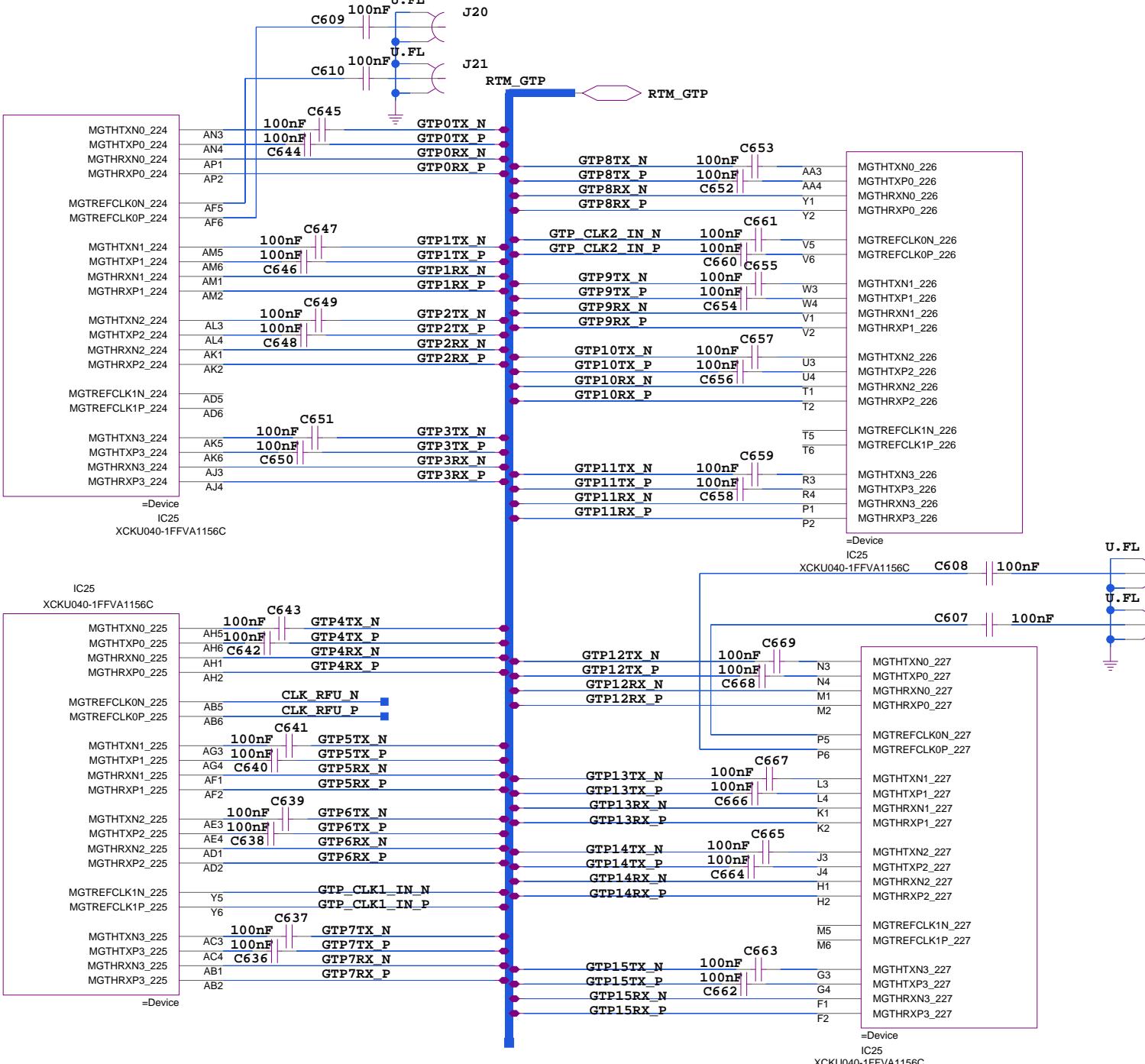


ARTIQ Sinara

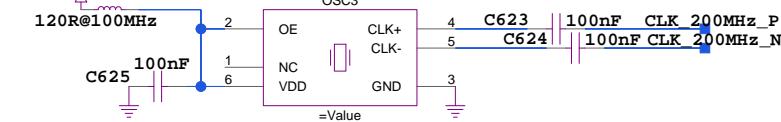
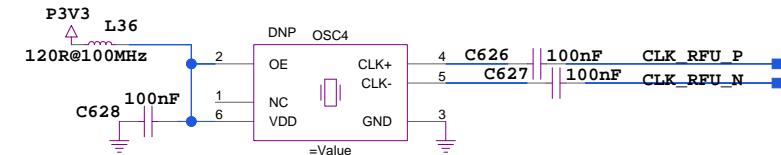
FPGA Bank 68 HP

SIZE	DWG NO	
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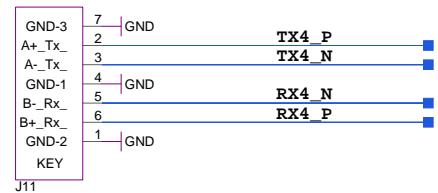
REV v0.95
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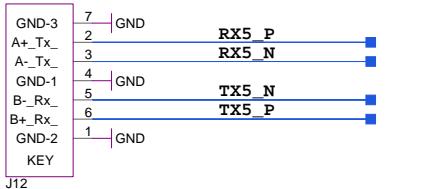
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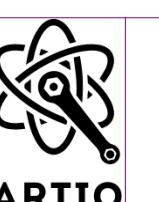
MSTER SATA



SLAVE SATA



FPGA Banks 224 225 226 22



ARTIQ

ARTIQ Sinara

TITLE

SIZE DWG NO

A3

FPGA_XCKU040FFVA1156

REV

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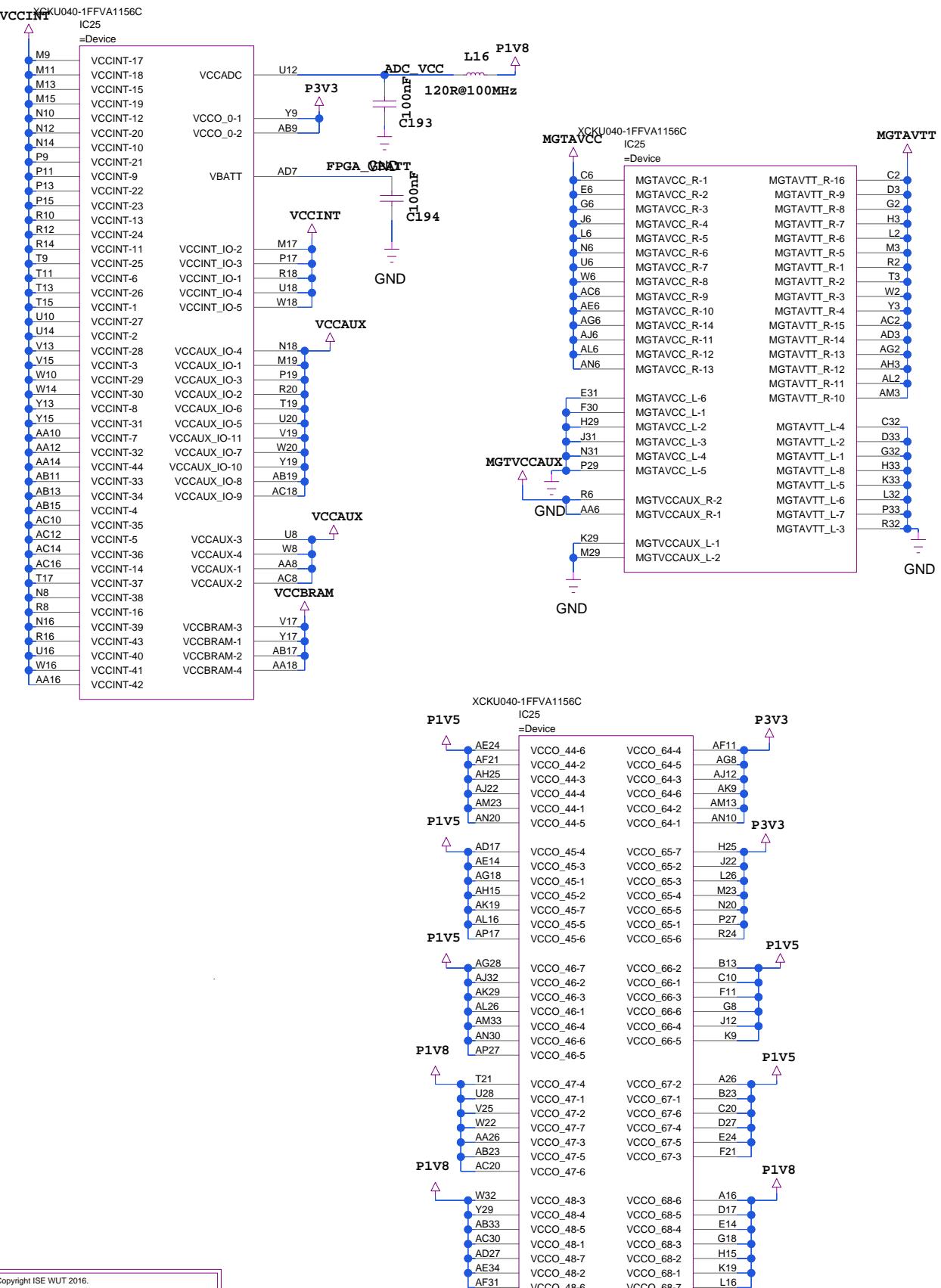
SHEET OF

8 29

03/12/2016:15:08

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V _{CCINT}	Internal supply voltage	0.922	0.950	0.979	V
	For -1L (0.90V) devices: internal supply voltage	0.880	0.900	0.920	V
	For -3 (1.0V only) devices: internal supply voltage	0.970	1.000	1.030	V
V _{CCINT_IO} ⁽³⁾	Internal supply voltage for the I/O banks	0.922	0.950	0.979	V
	For -1L (0.90V) devices: internal supply voltage for the I/O banks	0.880	0.900	0.920	V
	For -3 (1.0V only) devices: internal supply voltage for the I/O banks	0.970	1.000	1.030	V
V _{CCBRAM}	Block RAM supply voltage	0.922	0.950	0.979	V
	For -3 (1.0V only) devices: block RAM supply voltage	0.970	1.000	1.030	V
V _{CCAUX}	Auxiliary supply voltage	1.746	1.800	1.854	V
V _{CCO} ⁽⁴⁾⁽⁵⁾	Supply voltage for HR I/O banks	1.140	-	3.400	V
	Supply voltage for HP I/O banks	0.950	-	1.890	V
V _{CCAUX_IO} ⁽⁶⁾	Auxiliary I/O supply voltage	1.746	1.800	1.854	V
V _{IN} ⁽⁷⁾	I/O input voltage	-0.200	-	V _{CCO} + 0.200	V
	I/O input voltage (when V _{CCO} = 3.3V) for V _{REF} and differential I/O standards except TMDS_33 ⁽⁸⁾ .	-	0.400	2.625	V
I _{IN} ⁽⁹⁾	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	-	-	10.000	mA
V _{BATT} ⁽¹⁰⁾	Battery voltage	1.000	-	1.890	V
GTH and GTY Transceivers					
V _{MGTAVCC} ⁽¹¹⁾	Analog supply voltage for the GTH and GTY transceivers ⁽¹⁰⁾	0.970	1.000	1.030	V
V _{MGTAVTT} ⁽¹¹⁾	Analog supply voltage for the GTH and GTY transmitter and receiver termination circuits	1.170	1.200	1.230	V
V _{MGTCCAUX} ⁽¹¹⁾	Auxiliary analog QPLL voltage supply for the transceivers	1.750	1.800	1.850	V



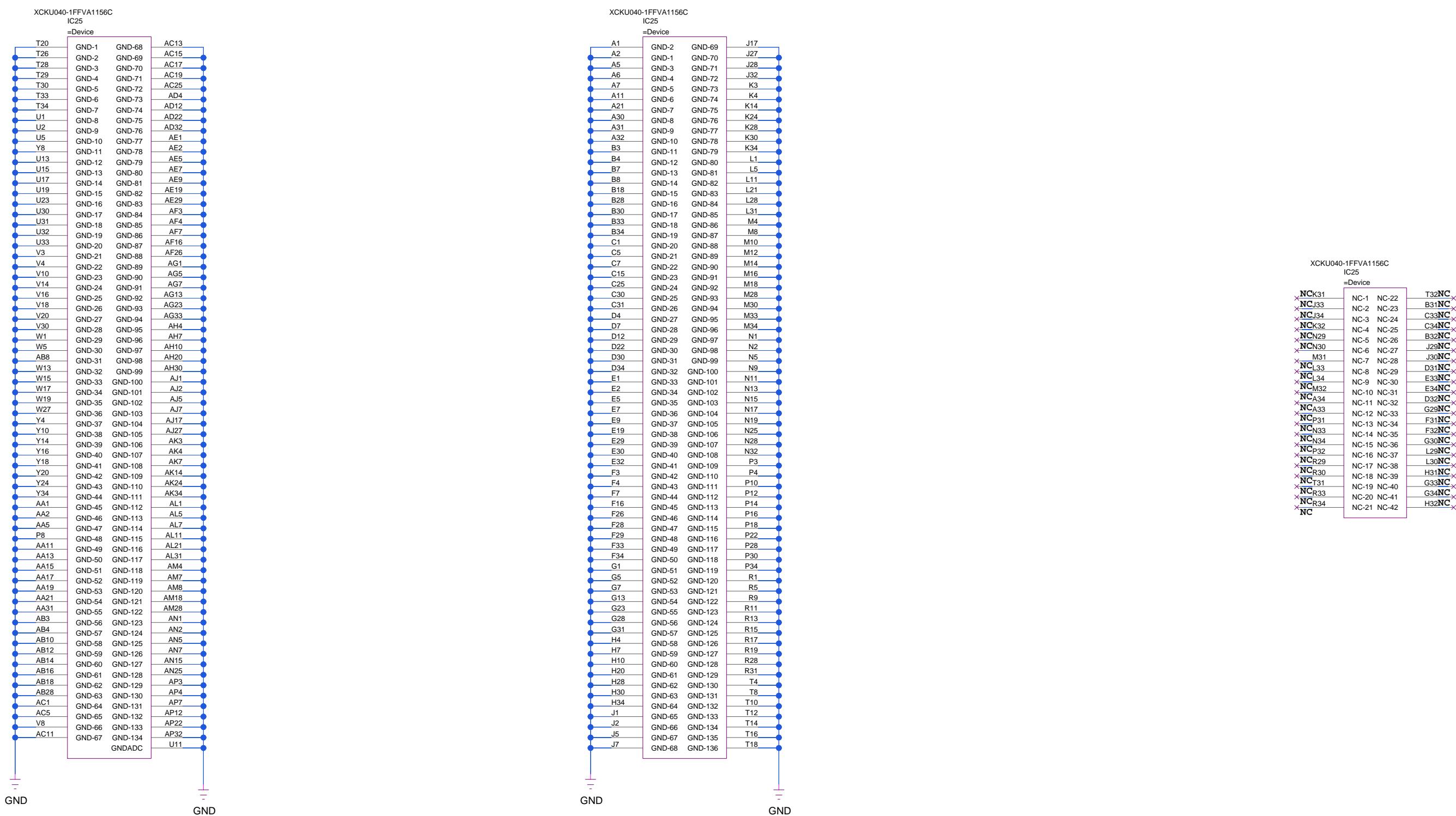
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FPGA_XCKU040FFVA1156

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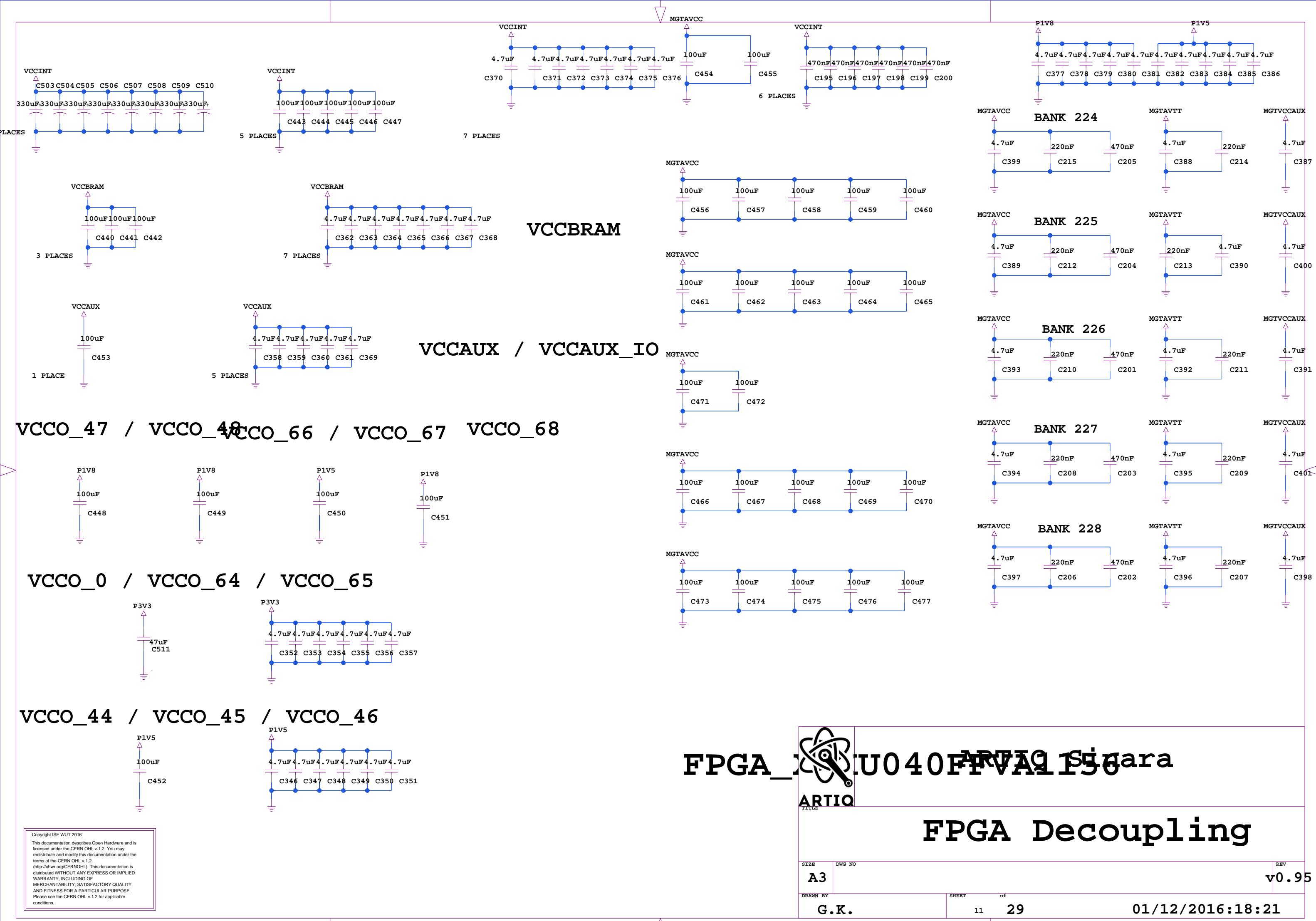
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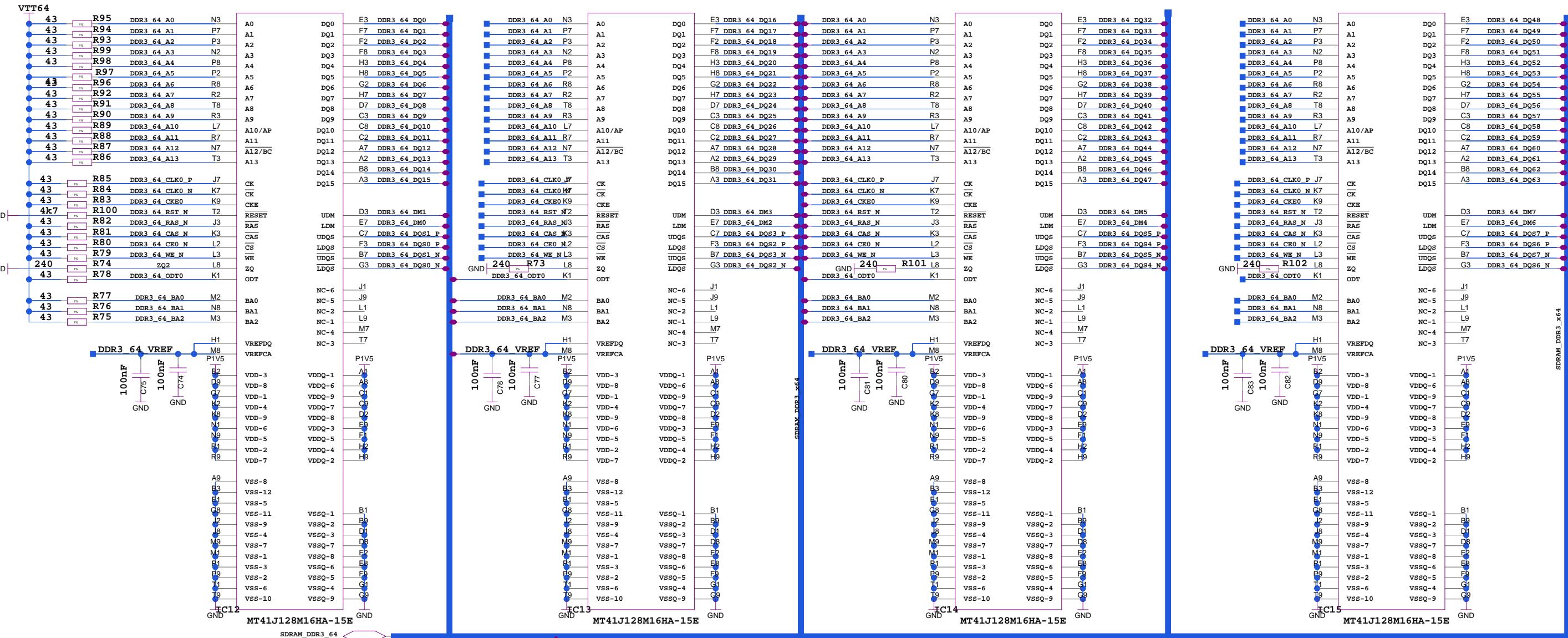


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ARTIQ

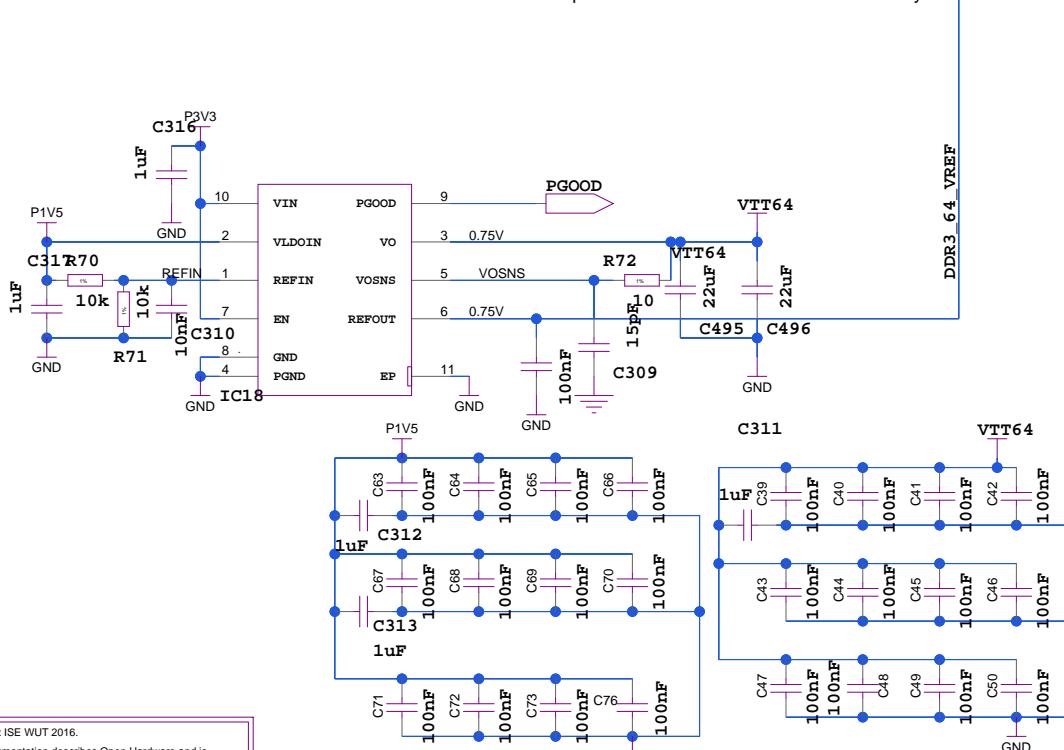
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SIZE	DWG NO	REV
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G.K.		10 29
01/12/2016:18:21		

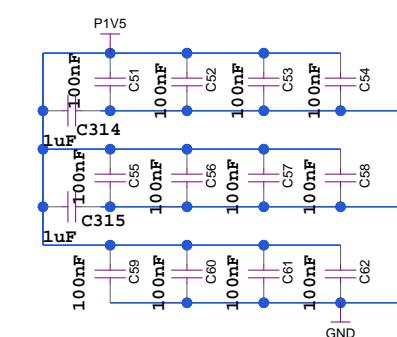
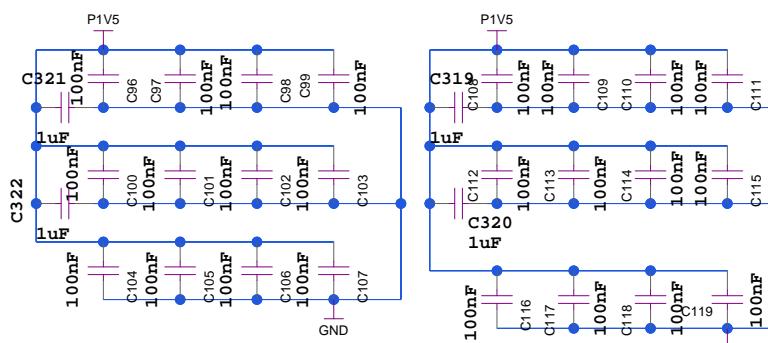




All capacitors without values are 100nF 0201 by default



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ARTIQ Sinara

SDRAM_DDR3_4x16

A3

G.K.

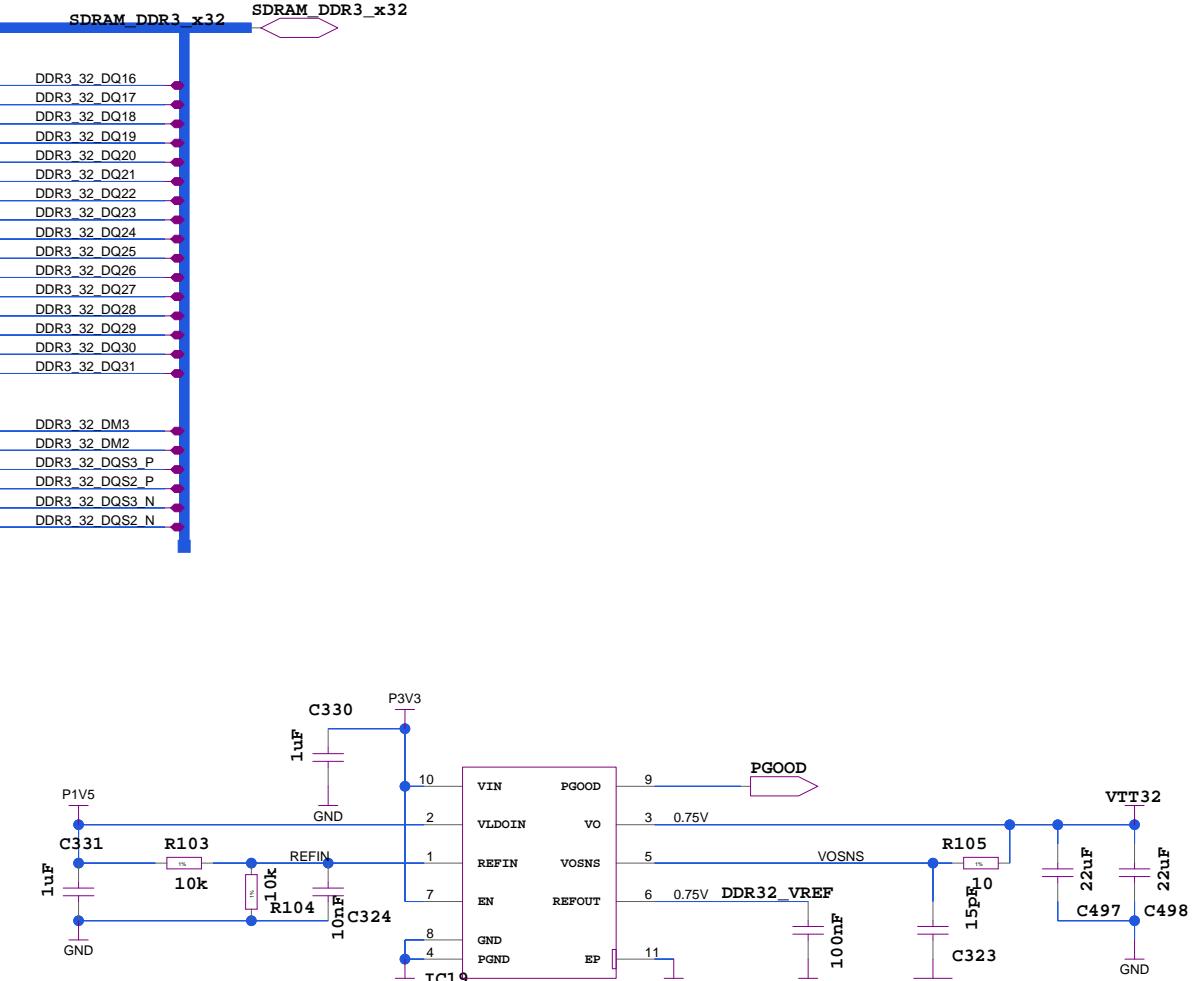
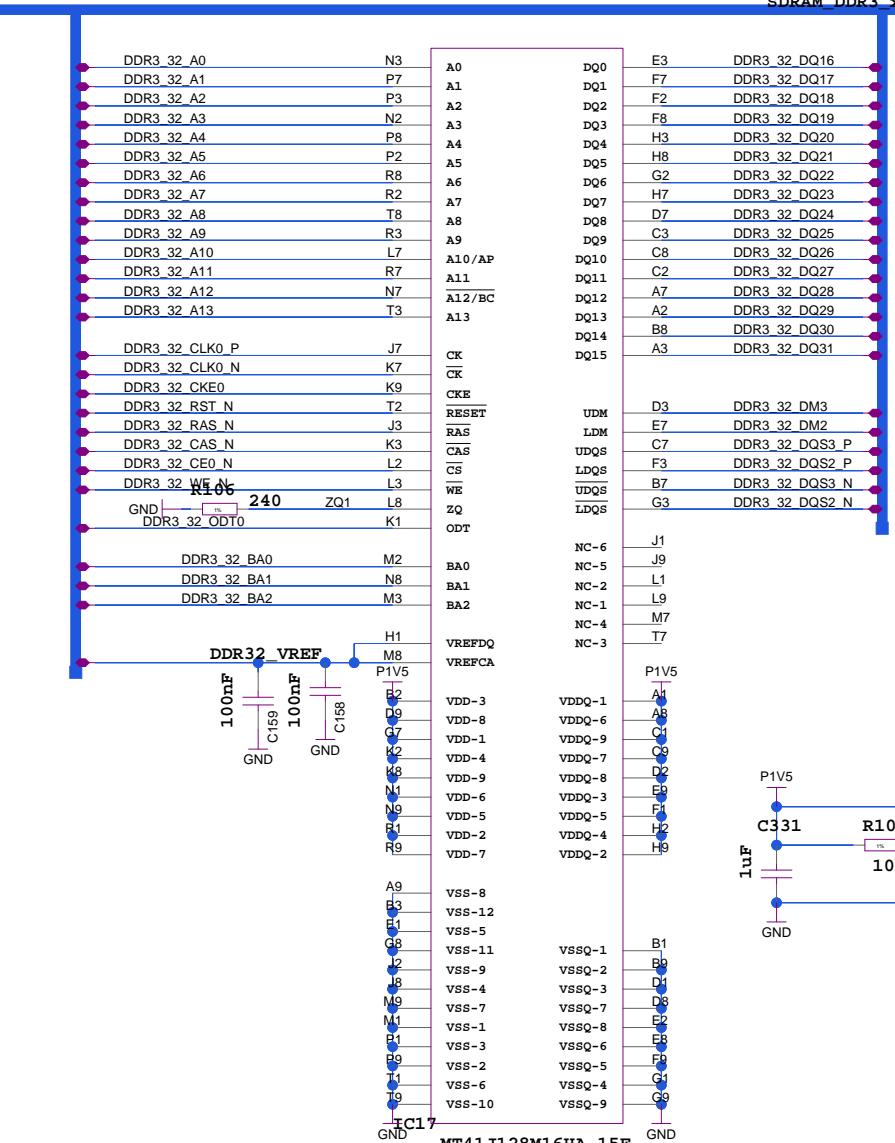
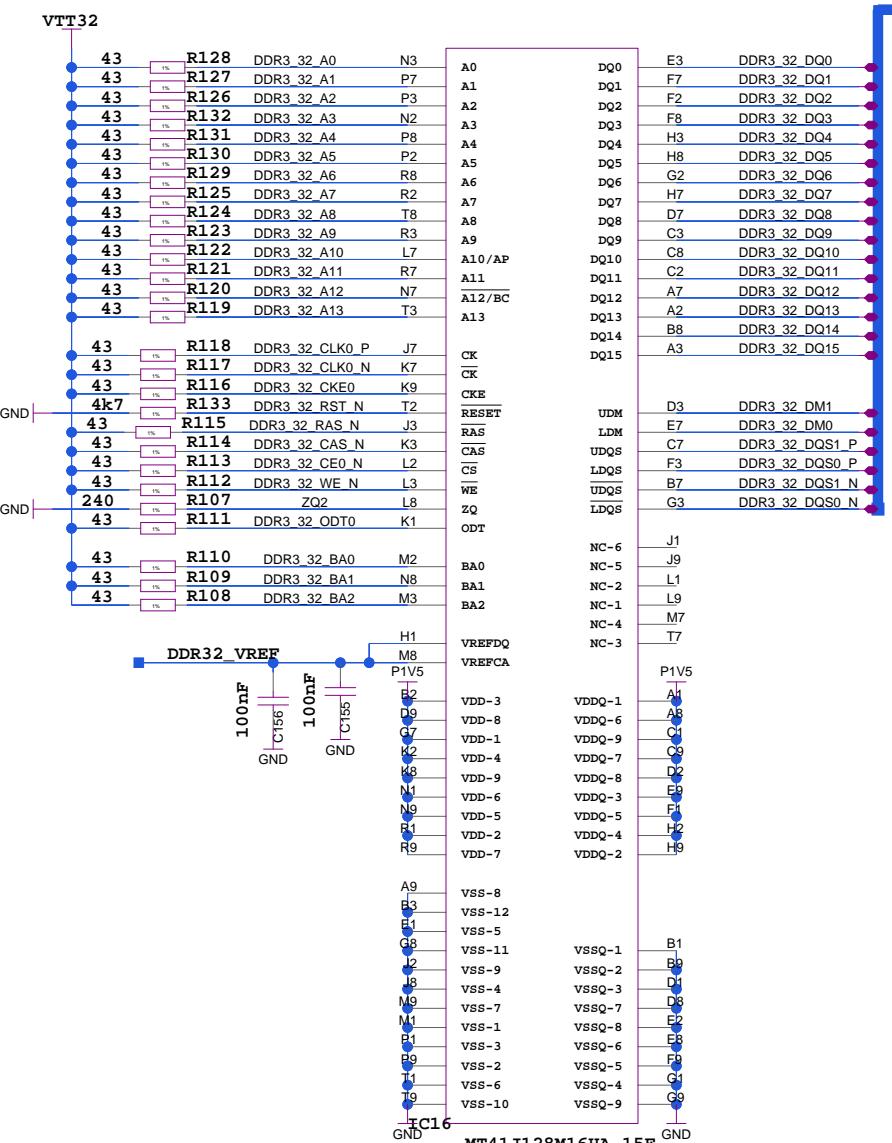
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v0.95

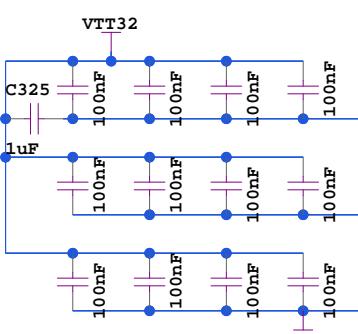
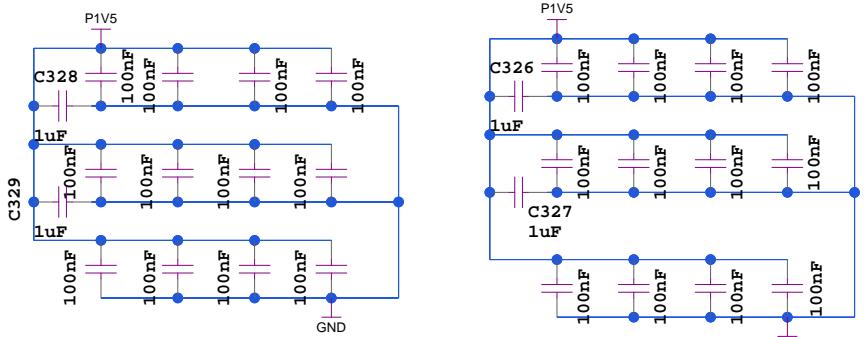
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All capacitors without values are 100nF 0201 by default



ARTIQ Sinara

SDRAM_DDR3_2x16

A3

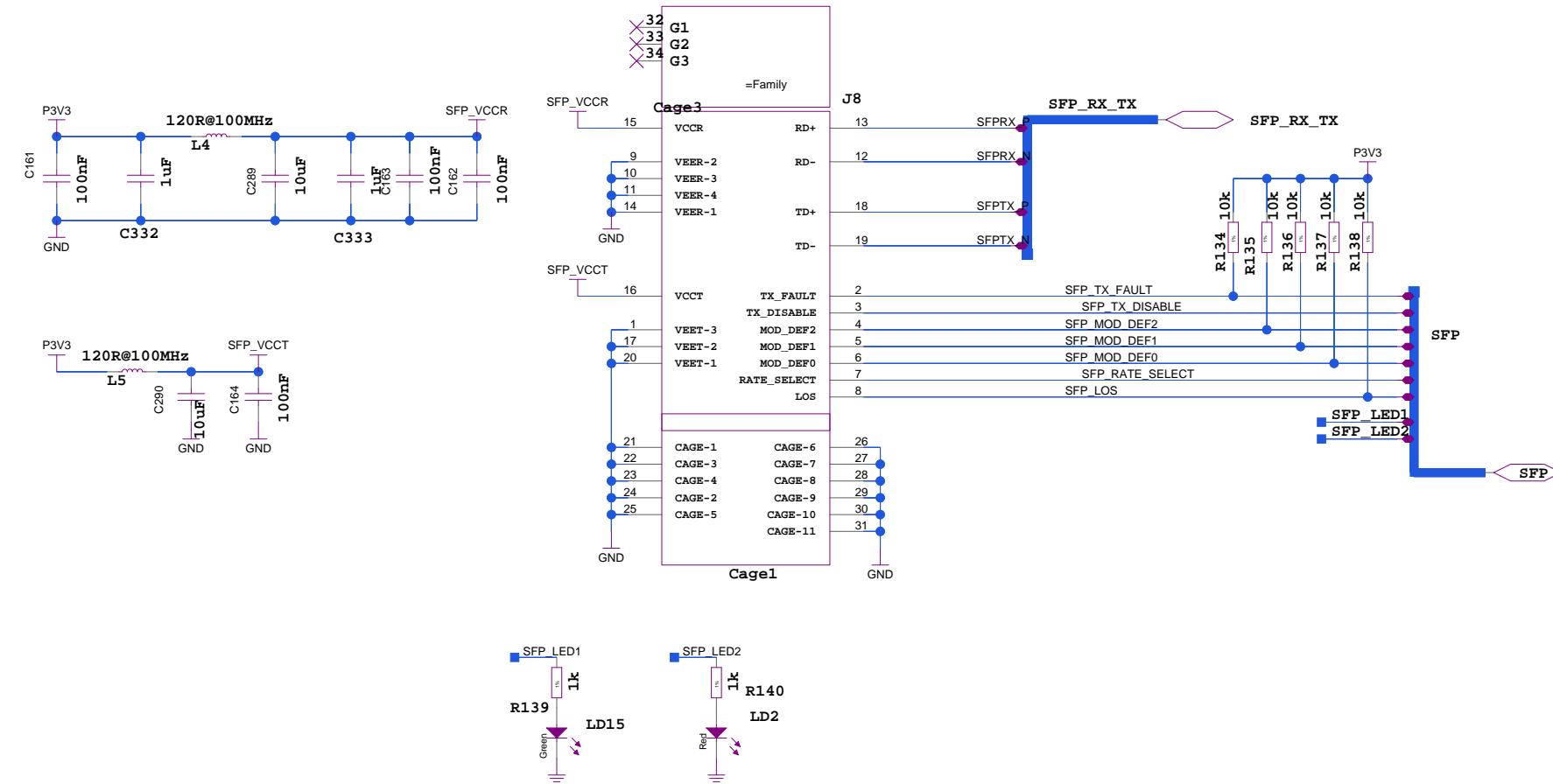
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v0.95

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SFP

SIZE DWG NO

A3

REV

v0.95

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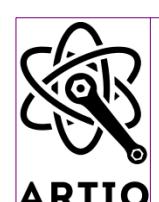
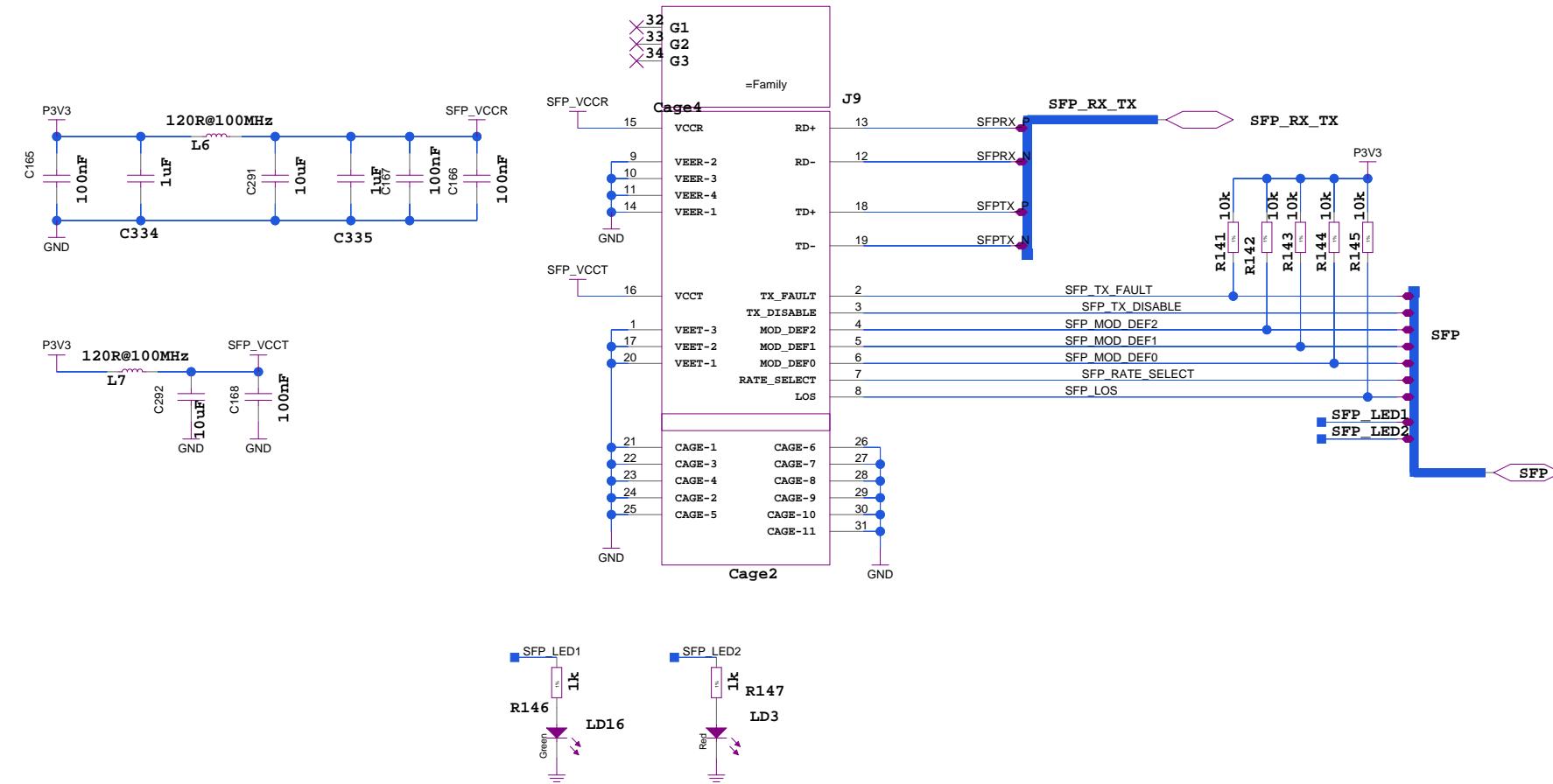
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29

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SFP

SIZE DWG NO

A3

REV

v0.95

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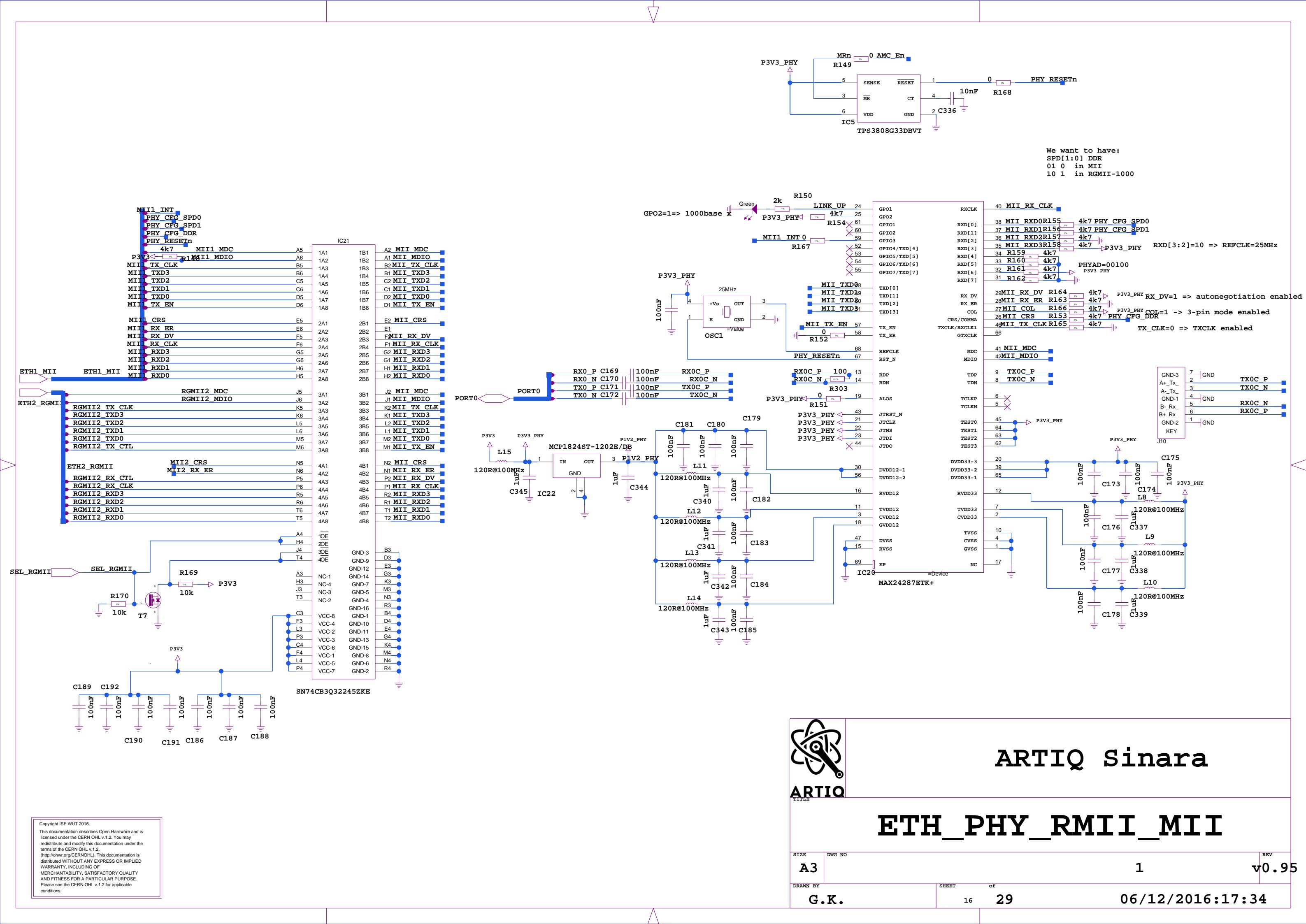
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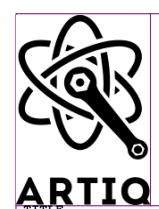
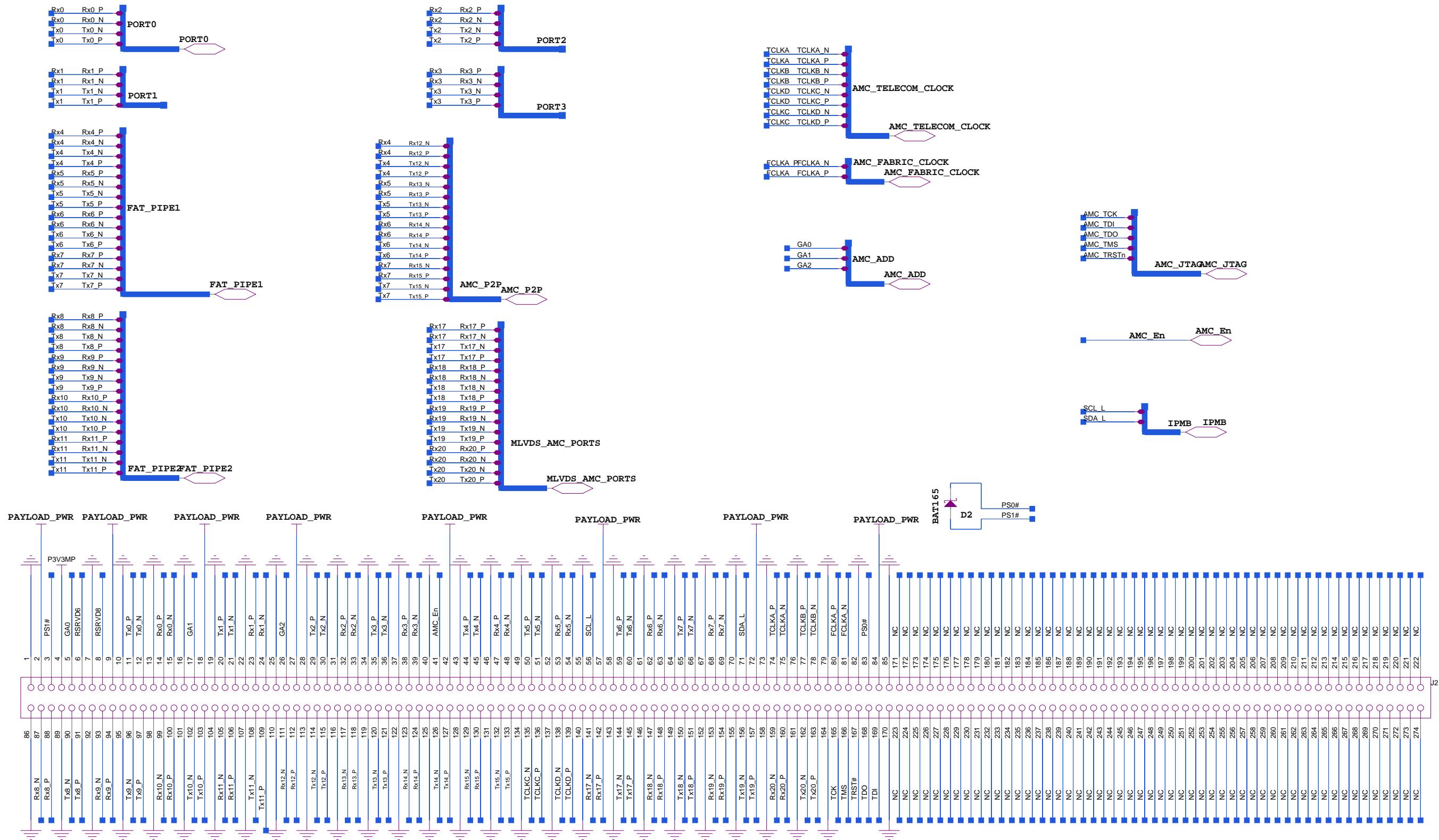
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1

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AMC_Connector

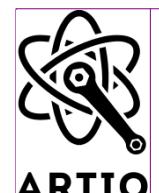
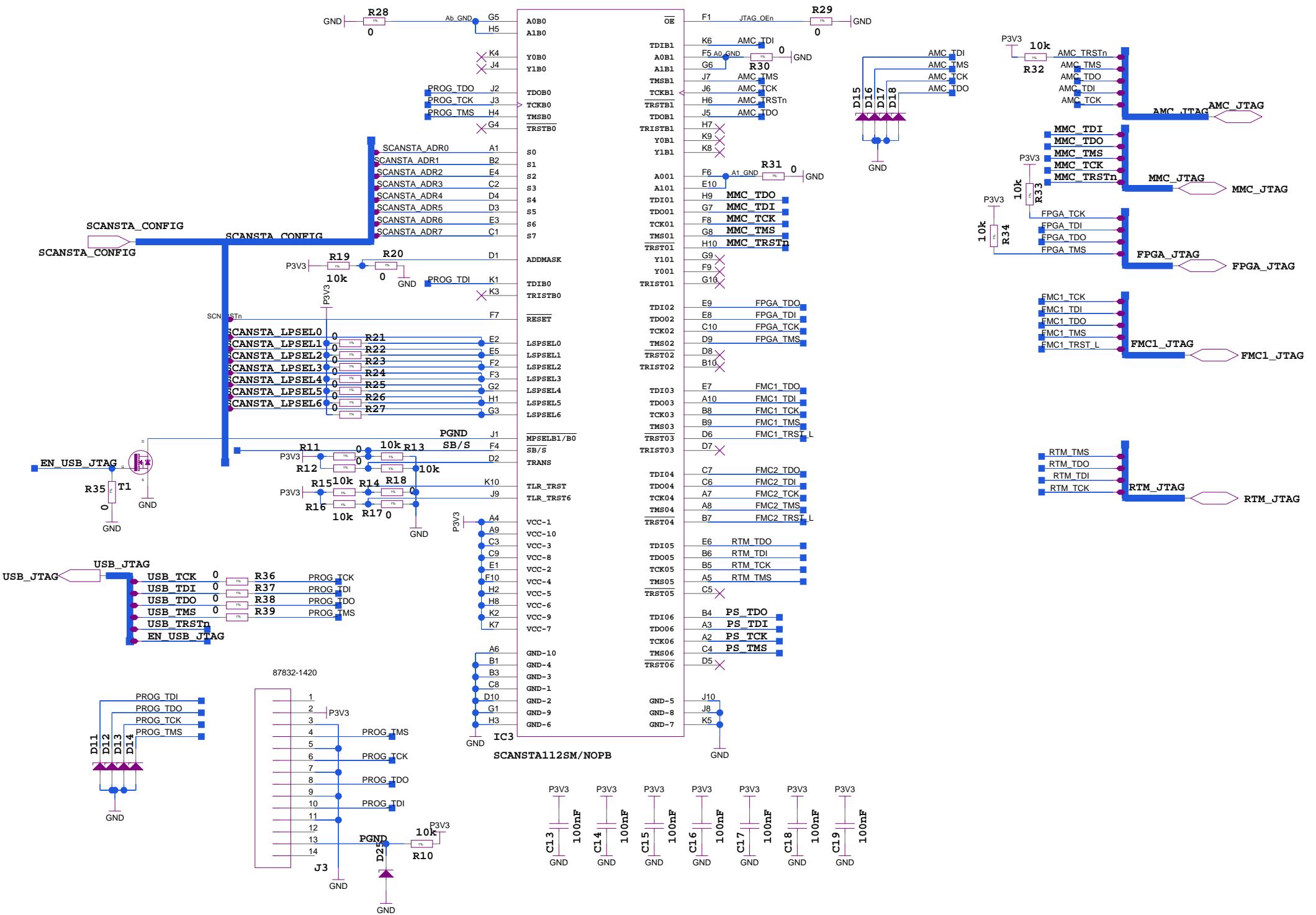
SIZE	DWG NO	REV
A3		v0.95
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G.K.	17	29

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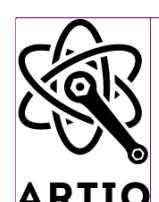
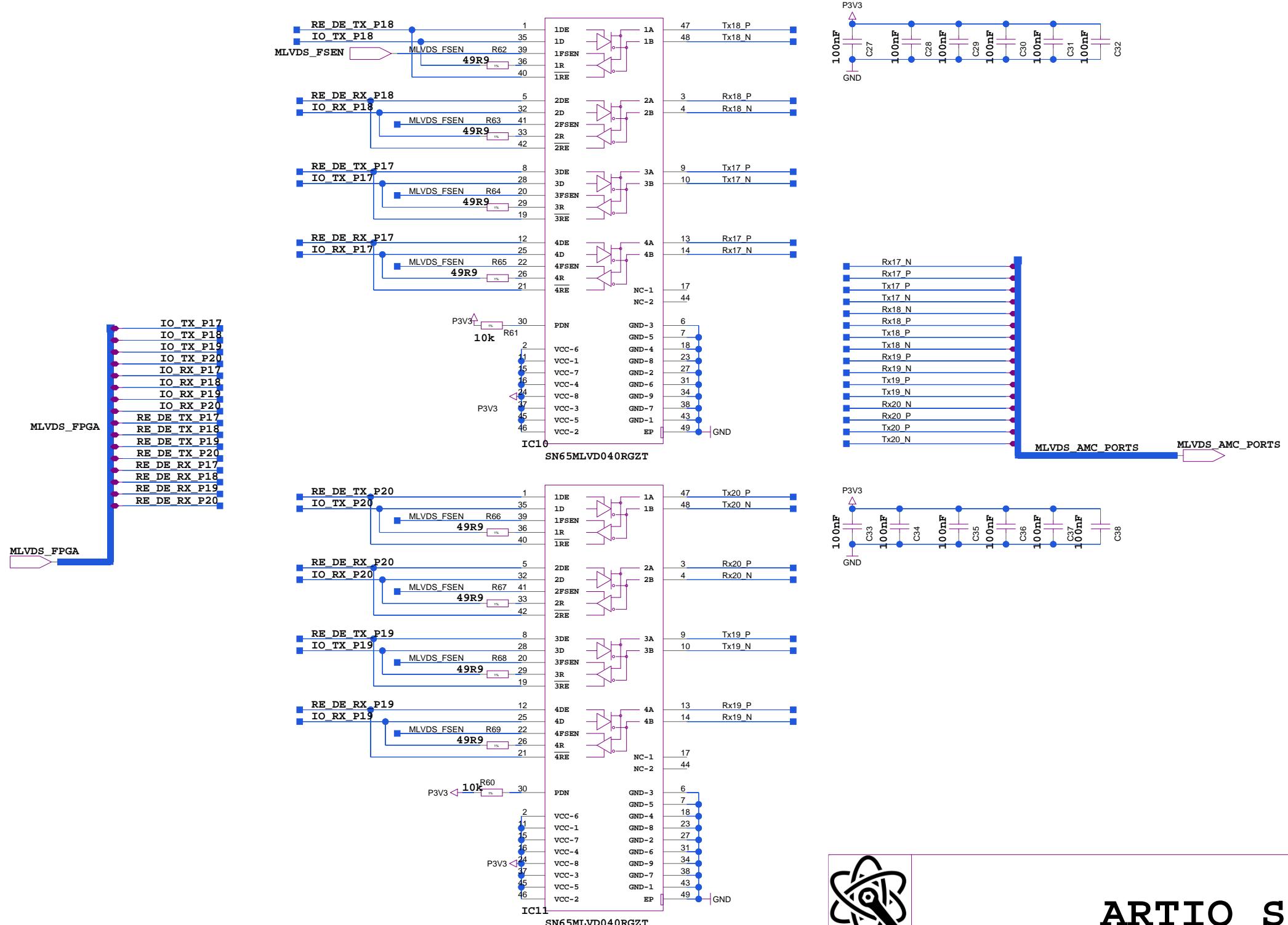
- Dimensions are in MM, nominal values used
- Component height rule derived from AMC Base Specification.PDF, Page 62
- The two corners of outline near the edge-connector are approximated, see AMC Base Specification.PDF, Page 59
- Stackup is not specified in AMC Base Specification.PDF or implemented in this template.



ARTIQ Sinara

JTAG_Configuration

SIZE	DWG NO	REV
A3		v0.95
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G.K.	18	29



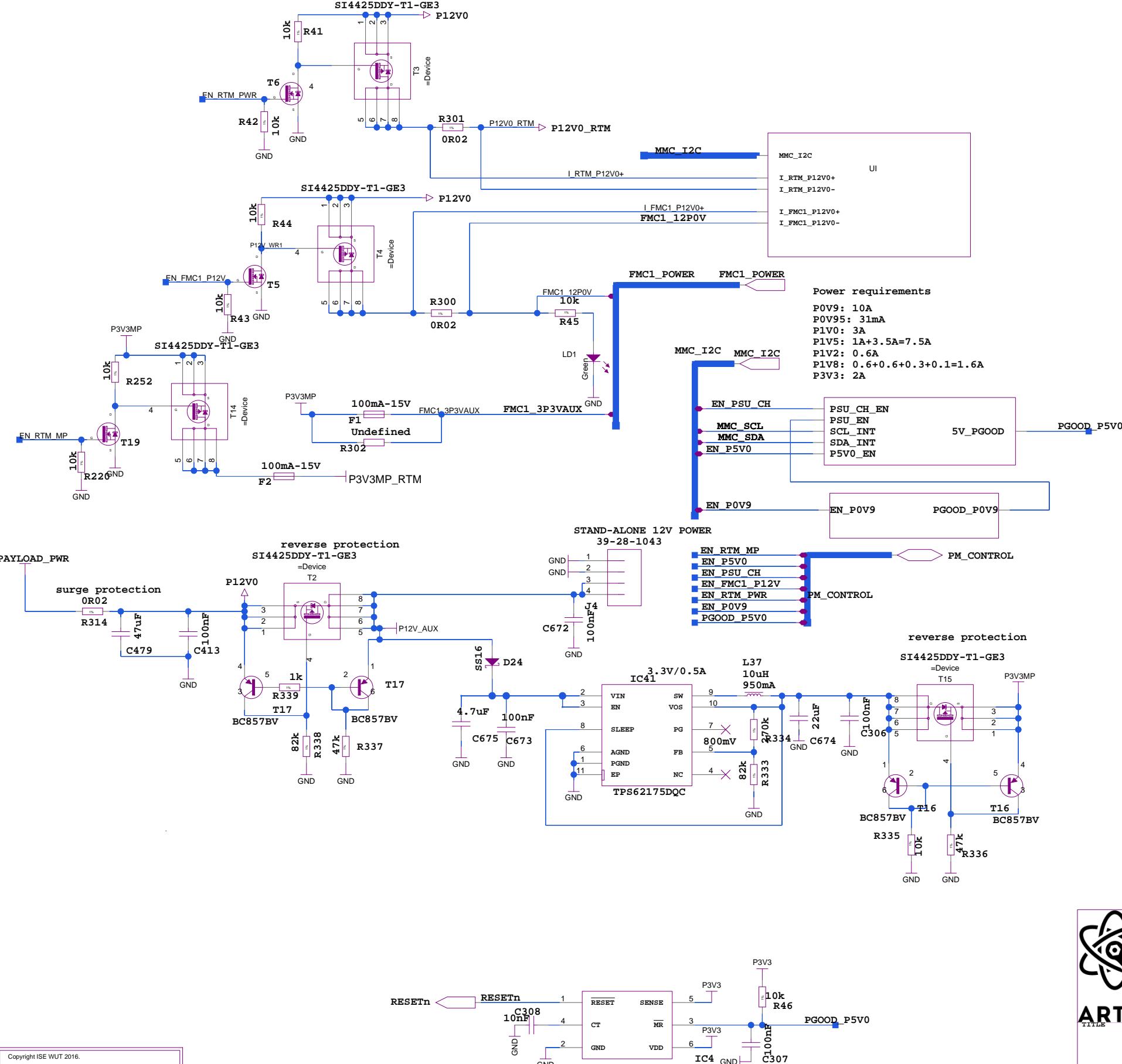
ARTIQ Sinara

M-LVDS_PHY

SIZE	DWG NO	REV
A3		
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G.K.	19	29

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Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V _{CCINT}	Internal supply voltage	0.922	0.950	0.979	V
V _{CCINT}	For -1L (0.90V) devices: internal supply voltage	0.880	0.900	0.920	V
V _{CCINT}	For -3 (1.0V only) devices: internal supply voltage	0.970	1.000	1.030	V
V _{CCINT}	Internal supply voltage for the I/O banks	0.922	0.950	0.979	V
V _{CCINT}	For -1L (0.90V) devices: internal supply voltage for the I/O banks	0.880	0.900	0.920	V
V _{CCRAM}	Block RAM supply voltage	0.970	1.000	1.030	V
V _{CCRAM}	For -3 (1.0V only) devices: block RAM supply voltage	0.922	0.950	0.979	V
V _{CCAUX}	Auxiliary supply voltage	1.746	1.800	1.854	V
V _{CCO} ⁽⁴⁾⁽⁵⁾	Supply voltage for HR I/O banks	1.140	-	3.400	V
V _{CCO} ⁽⁴⁾⁽⁵⁾	Supply voltage for HP I/O banks	0.950	-	1.890	V
V _{CCAUX}	Auxiliary I/O supply voltage	1.746	1.800	1.854	V
V _{IN} ⁽⁷⁾	I/O input voltage	-0.200	-	V _{CCO} + 0.200	V
V _{IN} ⁽⁷⁾	I/O input voltage when V _{CCO} = 3.3V for V _{GEF} and differential I/O standards except TMDS_33 ⁽⁸⁾	-	0.400	2.625	V
I _H ⁽⁹⁾	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	-	-	10.000	mA
V _{BATT} ⁽¹⁰⁾	Battery voltage	1.000	-	1.890	V
GTH and GTY Transceivers					
V _{MGTAVCC} ⁽¹¹⁾	Analog supply voltage for the GTH and GTY transceivers ⁽¹²⁾	0.970	1.000	1.030	V
V _{MGTAVTT} ⁽¹¹⁾	Analog supply voltage for the GTH and GTY transmitter and receiver termination circuits	1.170	1.200	1.230	V
V _{MGTVCVAU} ⁽¹¹⁾	Auxiliary analog QPLL voltage supply for the transceivers	1.750	1.800	1.850	V
Temperature					
V _{TEMP}	Analog supply voltage for the resistor calibration circuit of the GTH and GTY transceiver columns	1.170	1.200	1.230	V
V _{SYSMON}	SYSDAC supply relative to GNDADC	1.746	1.800	1.854	V
V _{REFP}	Externally supplied reference voltage	1.200	1.250	1.300	V
T _J	Junction temperature operating range for commercial (C) Junction temperature operating range for extended (E) Junction temperature operating range for industrial (I)	0	-	85	°C
		0	-	100	°C
		-40	-	100	°C

Power-On/Off Power Supply Sequencing

The recommended power on sequence is V_{CCINT}/V_{CCINT}_IO/V_{CCRAM}/V_{CCAUX}/V_{CCAUX}_IO and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-state at power-on. The recommended power down sequence is V_{CCO}/V_{CCAUX}/V_{CCAUX}_IO/V_{CCRAM}/V_{CCINT}/V_{CCINT}_IO. If the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT}_IO must be connected to V_{CCINT}. If V_{CCAU}/V_{CCAUX}_IO and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAU} and V_{CCAUX} must be connected together. When the current minimums are met, the device powers up after the V_{CCINT}/V_{CCINT}_IO/V_{CCRAM}/V_{CCAUX}/V_{CCAUX}_IO and V_{CCO} supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied.

V_{CADC} and V_{REF} can be powered at any time and have no power-up sequencing recommendations.

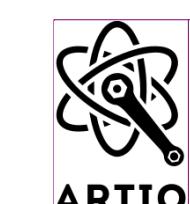
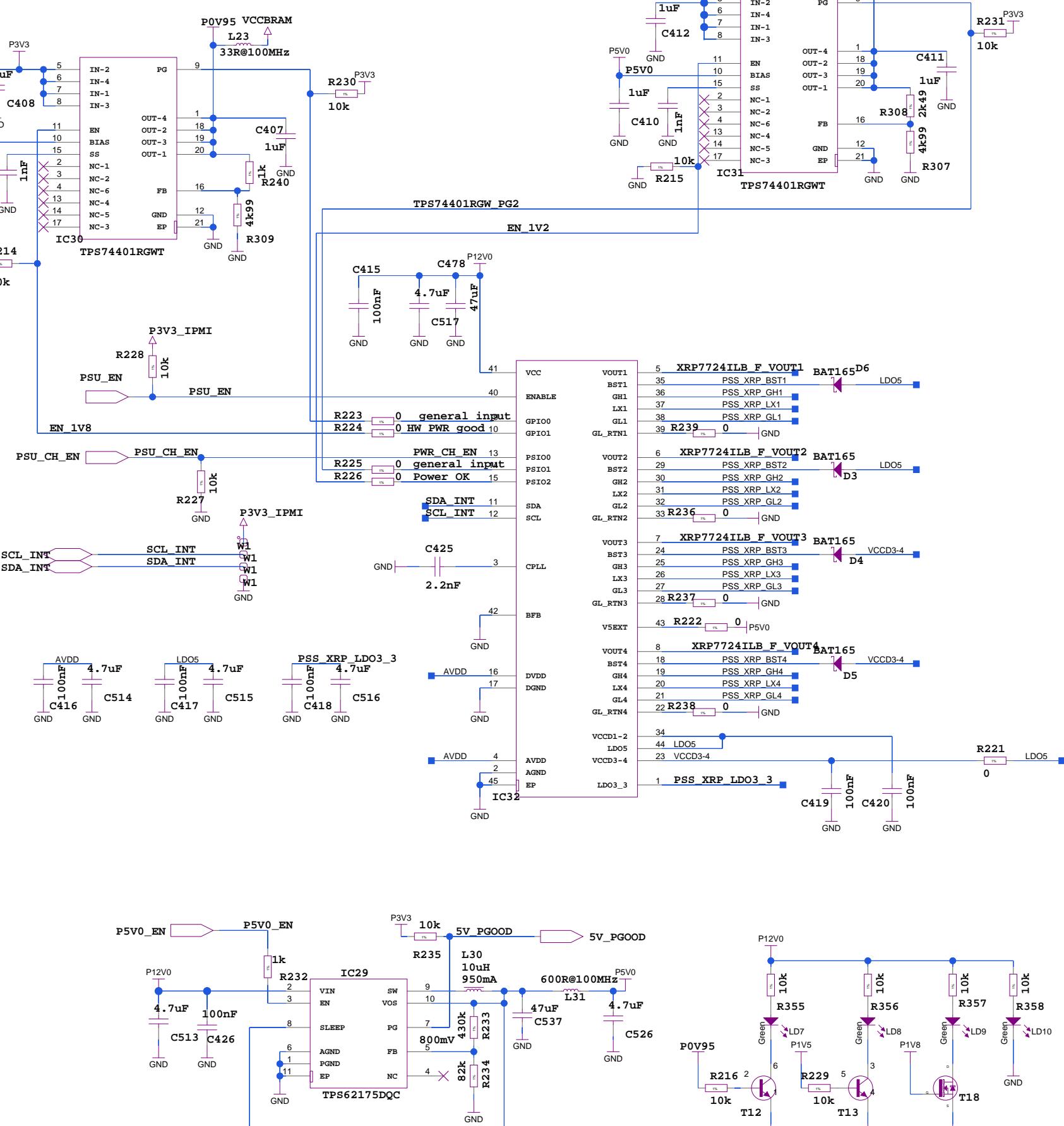
The recommended power on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, V_{MGTAVCC}, V_{MGTAVTT} OR V_{MGTAVCC}, V_{MGTAVTT}, V_{MGTAVTT}. There is no recommended sequencing for V_{MGTAVCC}, V_{MGTAVTT} OR V_{MGTAVCC}, V_{MGTAVTT}. The recommended sequencing for power off sequence is the reverse of the power on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from V_{MGTAVTT} can be higher than specifications during power up and power down.

Power Supply			
Source	Voltage	Total (A)	
V _{CCINT}	0,900	9,165	
V _{CCINT} _IO	0,900	0,620	
V _{CCRAM}	0,950	0,031	
V _{CCAUX}	1,800	0,660	
V _{CCAUX} _IO	1,800	0,546	
V _{CCO} 3.3V	3,300	0,000	
V _{CCO} 2.5V	2,500		
V _{CCO} 1.8V	1,800	0,380	
V _{CCO} 1.5V	1,500	0,936	
V _{CCO} 1.35V	1,350		
V _{CCO} 1.2V	1,200		
V _{CCO} 1.0V	1,000		
MGT _V CCAUX	1,800	0,081	
MGT _A V _{CC}	1,000	3,038	
MGT _A V _{TT}	1,200	0,592	
-	-	-	
V _{CCADC}	1,800	0,014	



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POWER_Management



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PWR_DC_DC_EXAR

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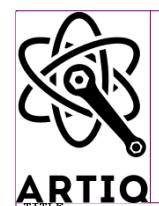
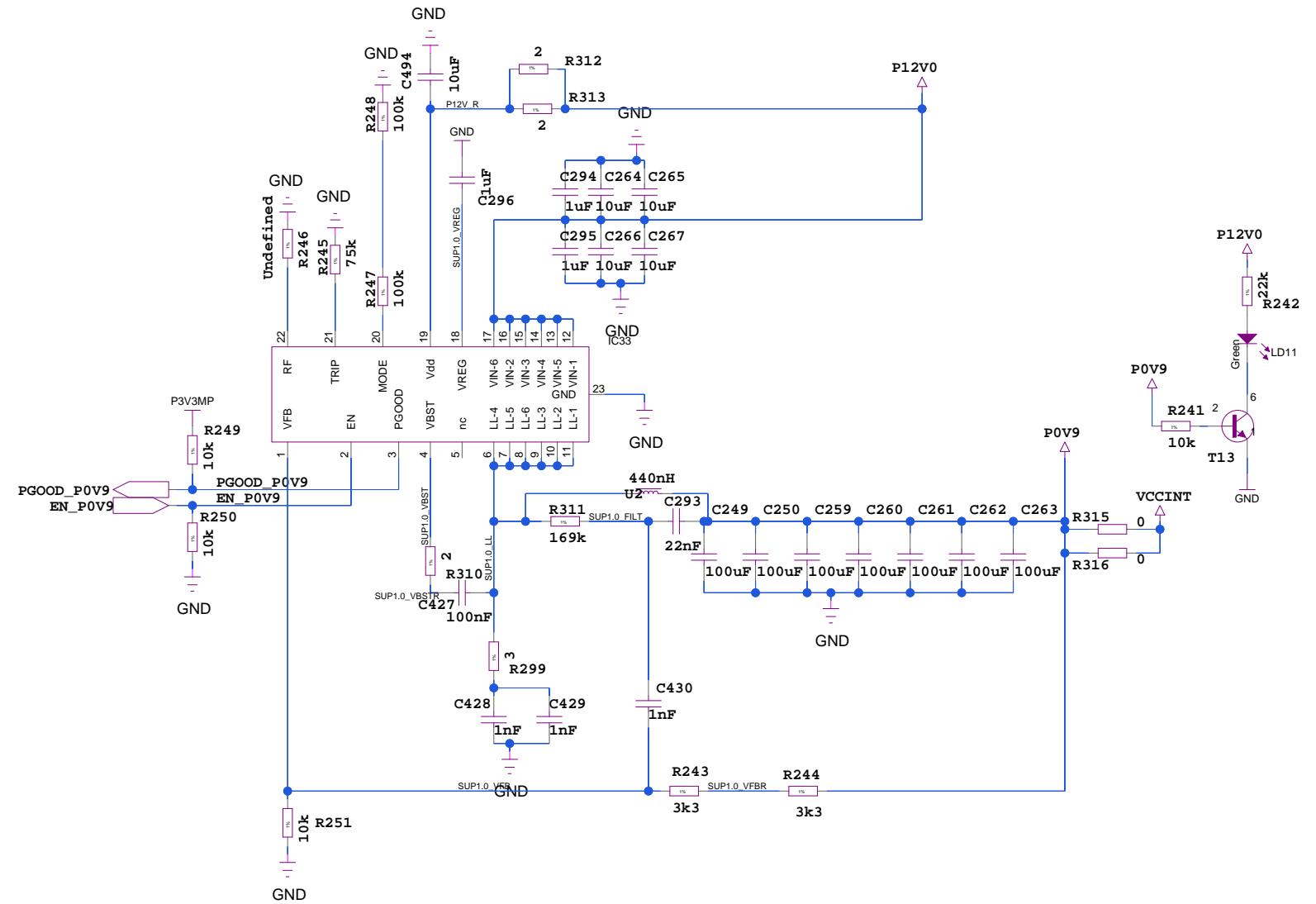
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29

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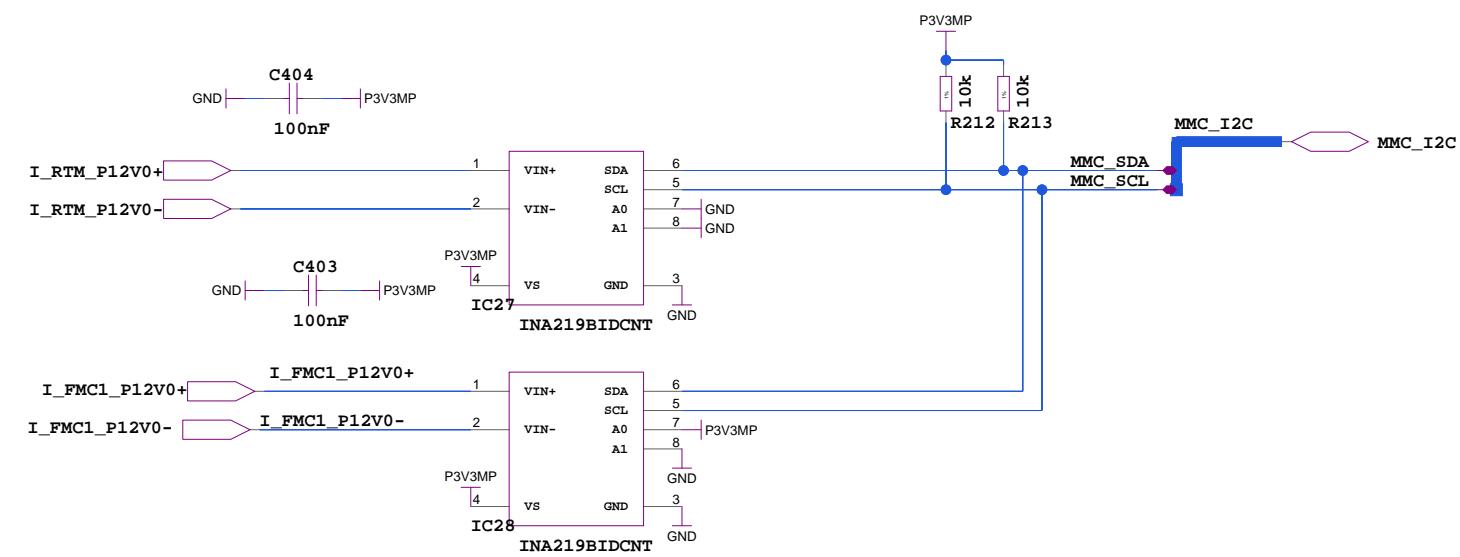
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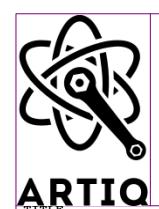
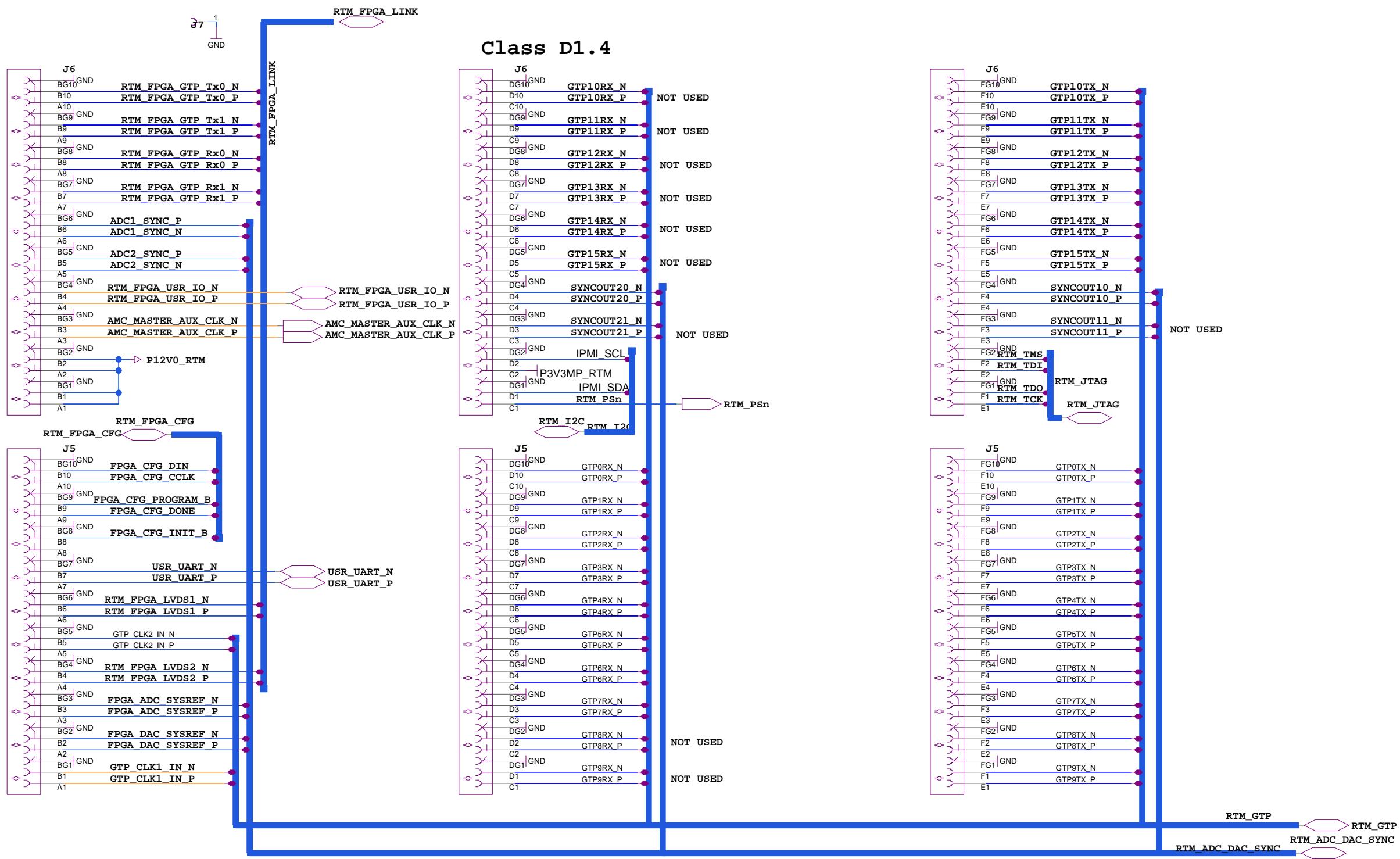


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UI_mon

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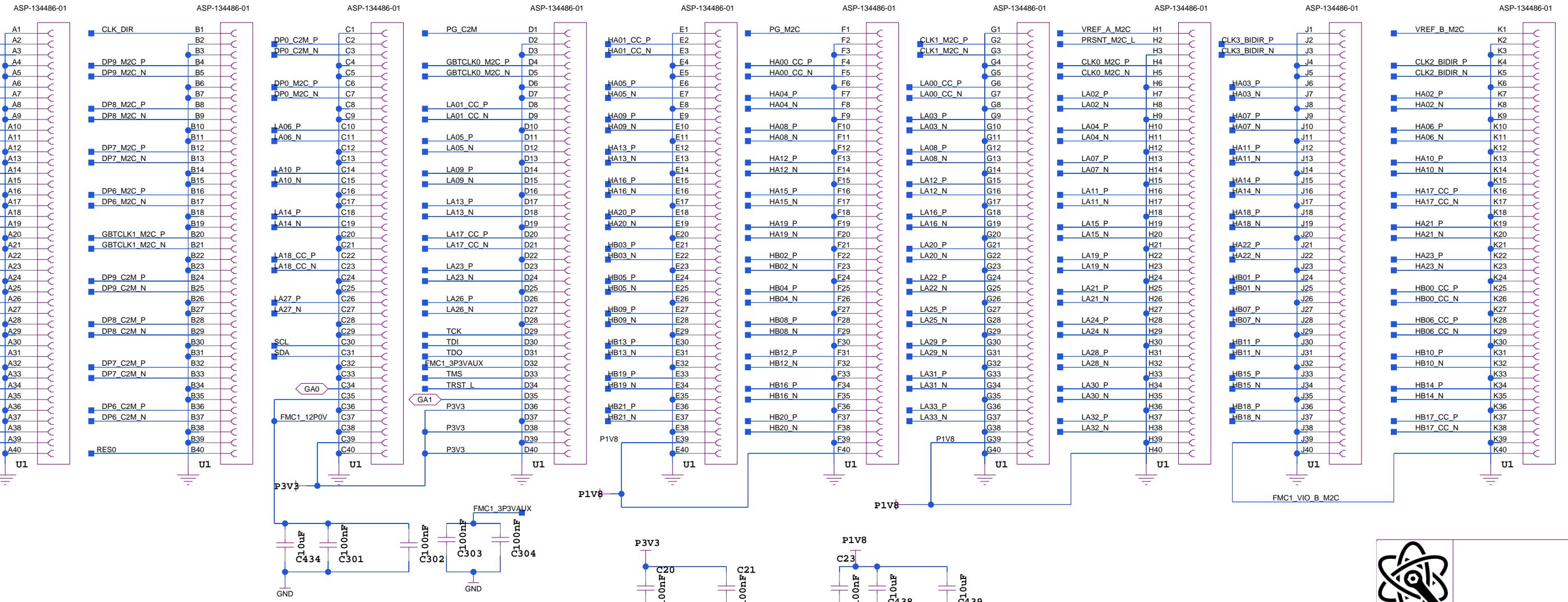
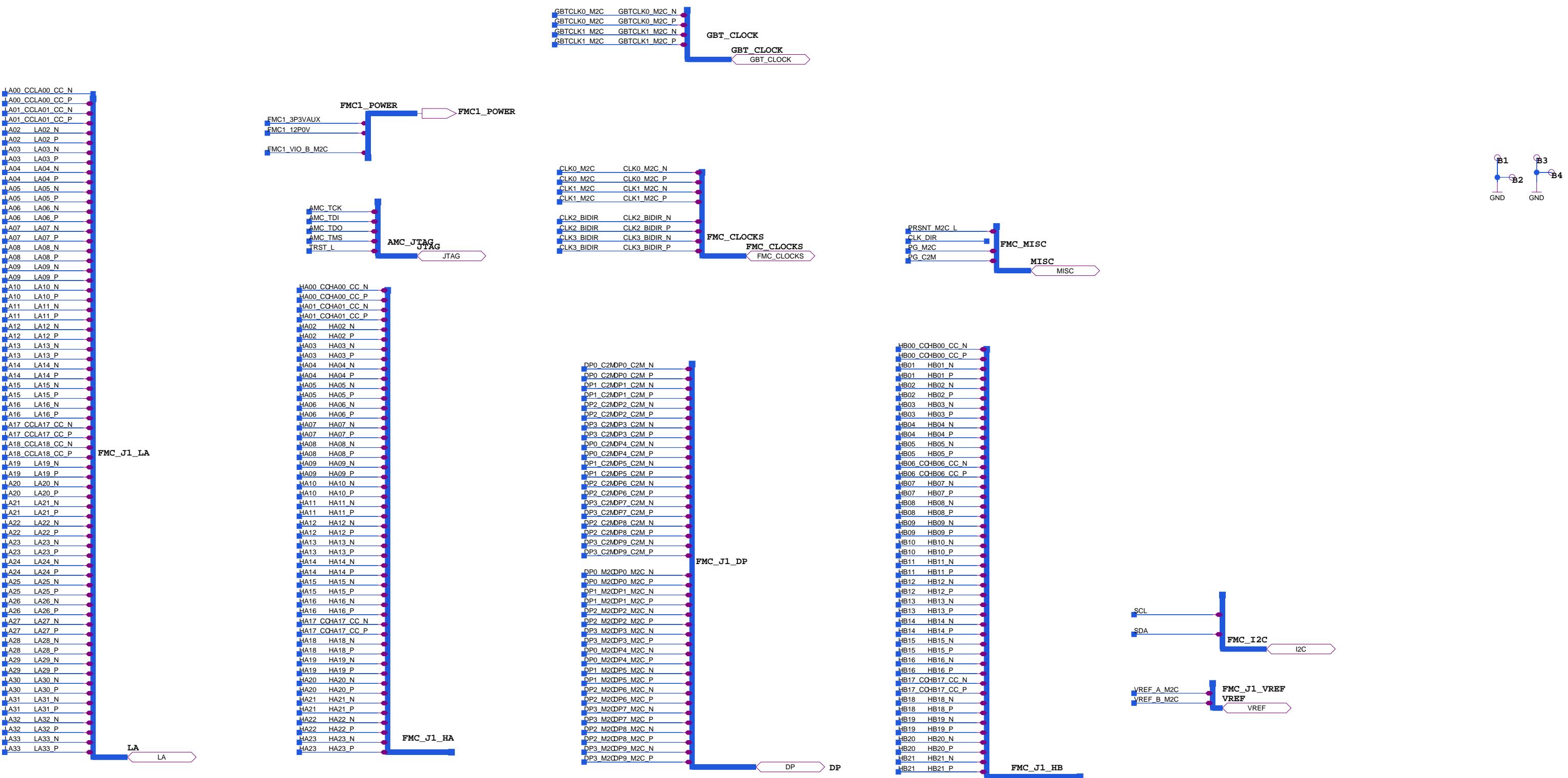
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RTM_CON

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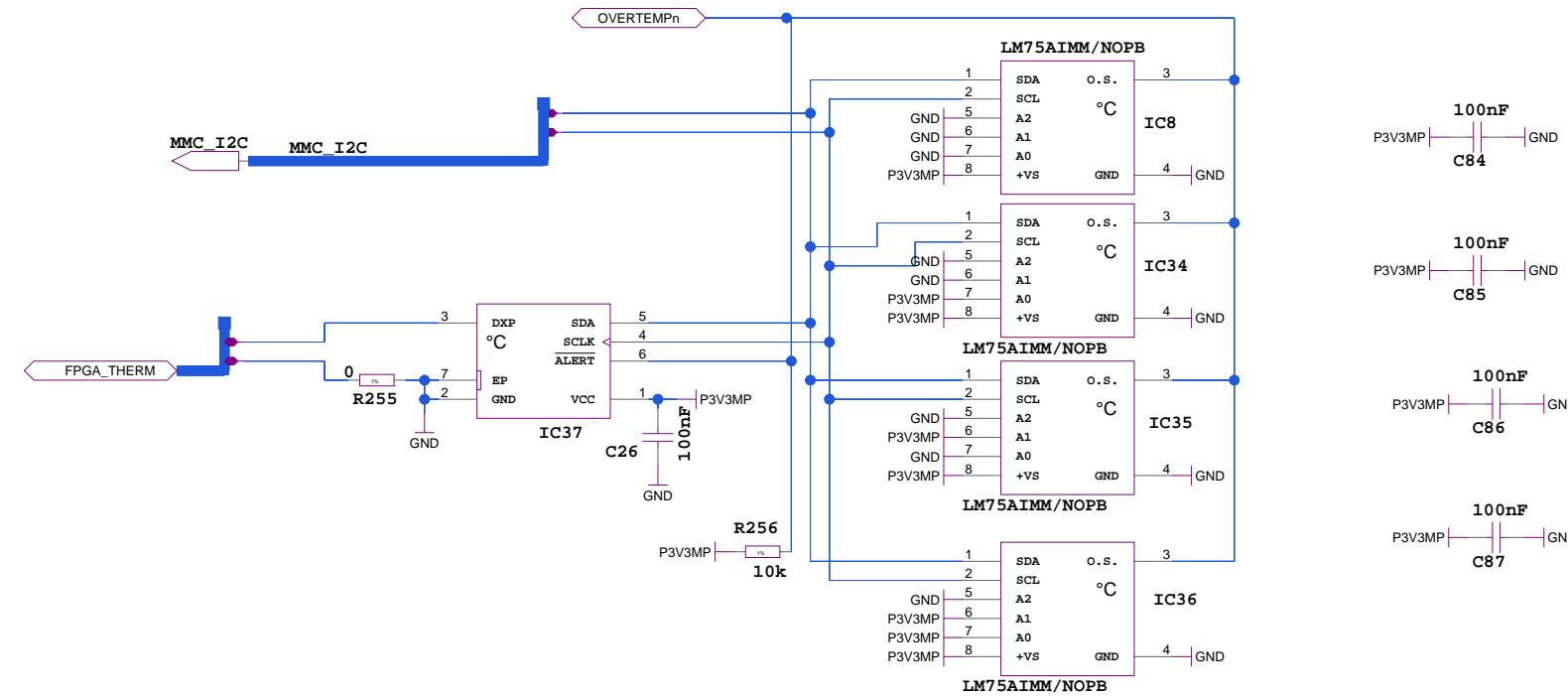


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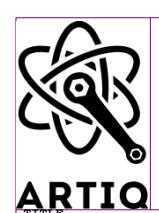


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FMC_connector



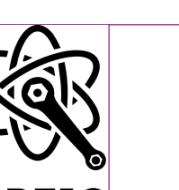
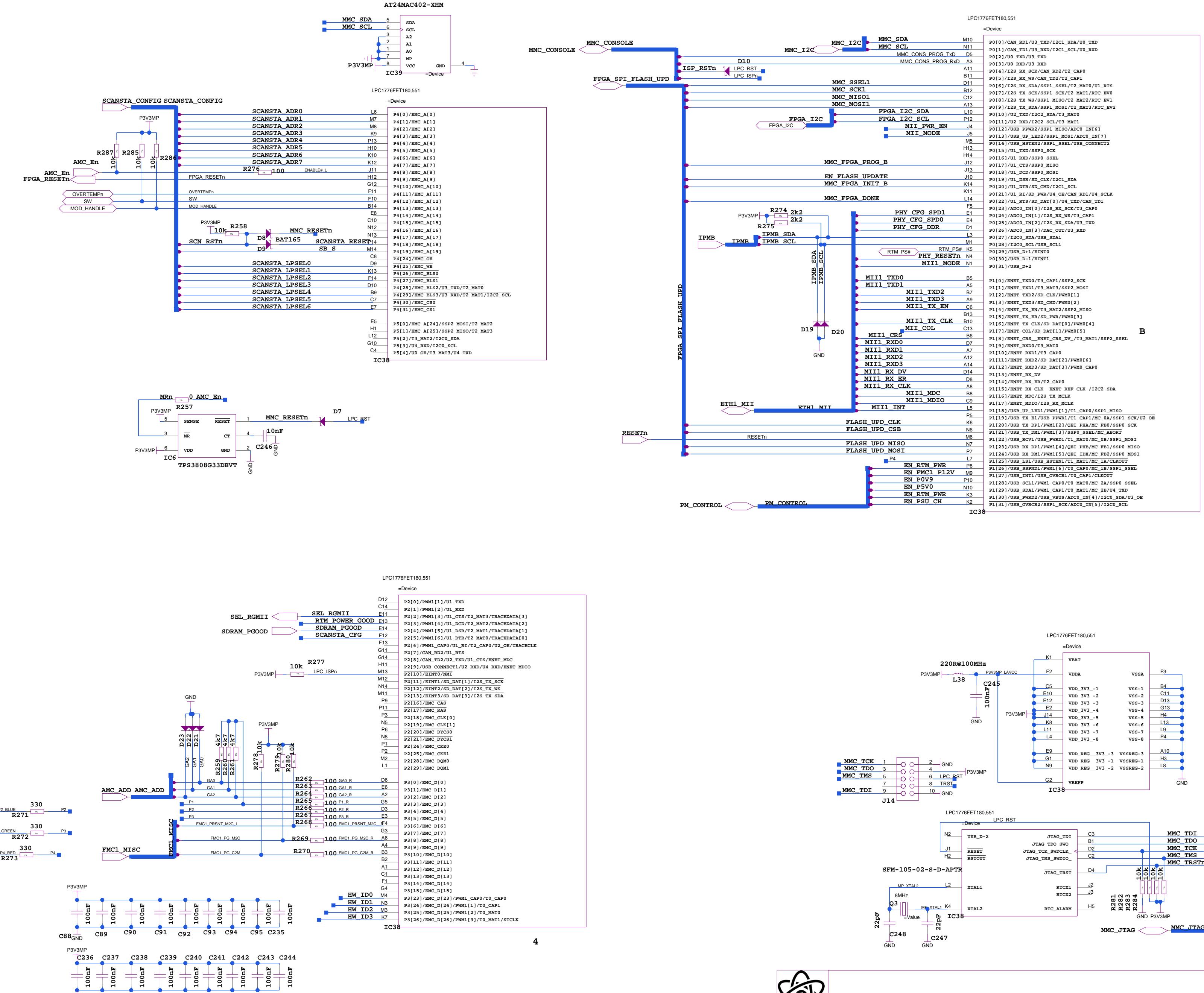
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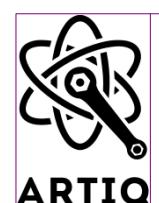
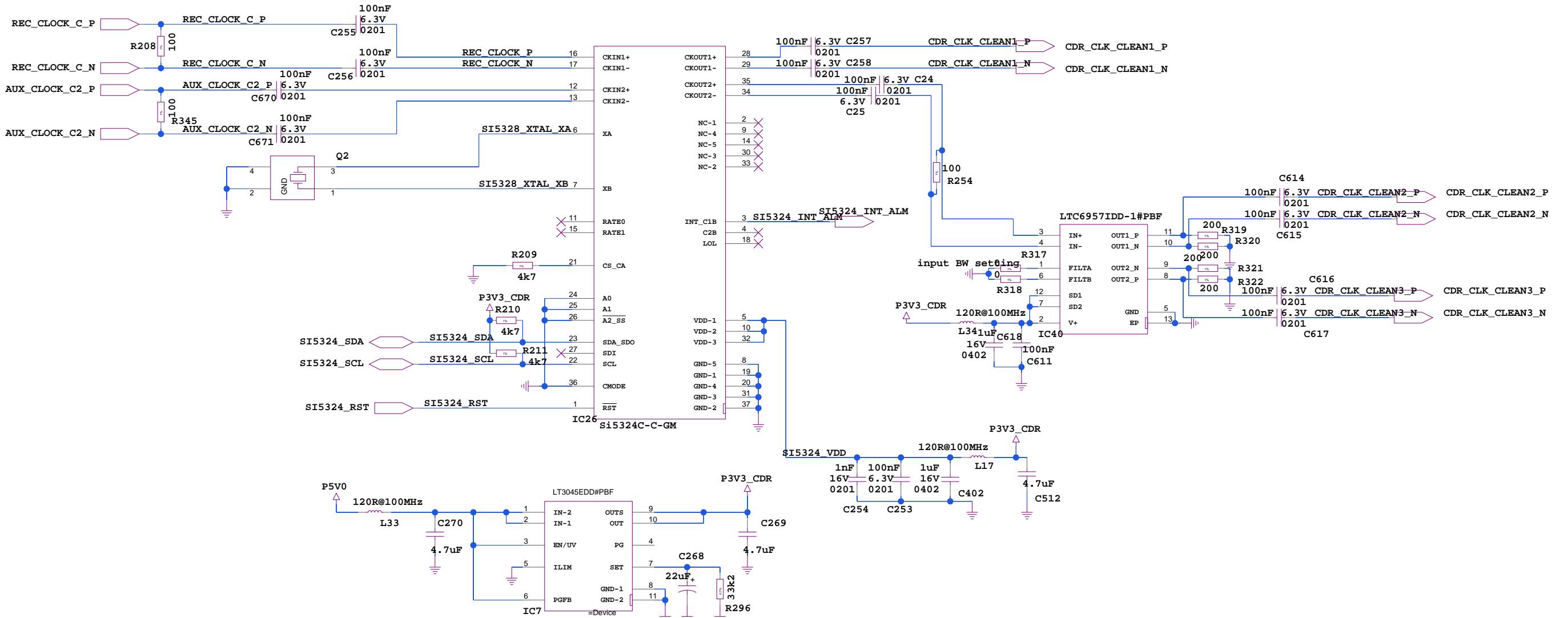
Thermometers

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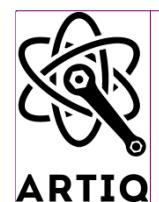
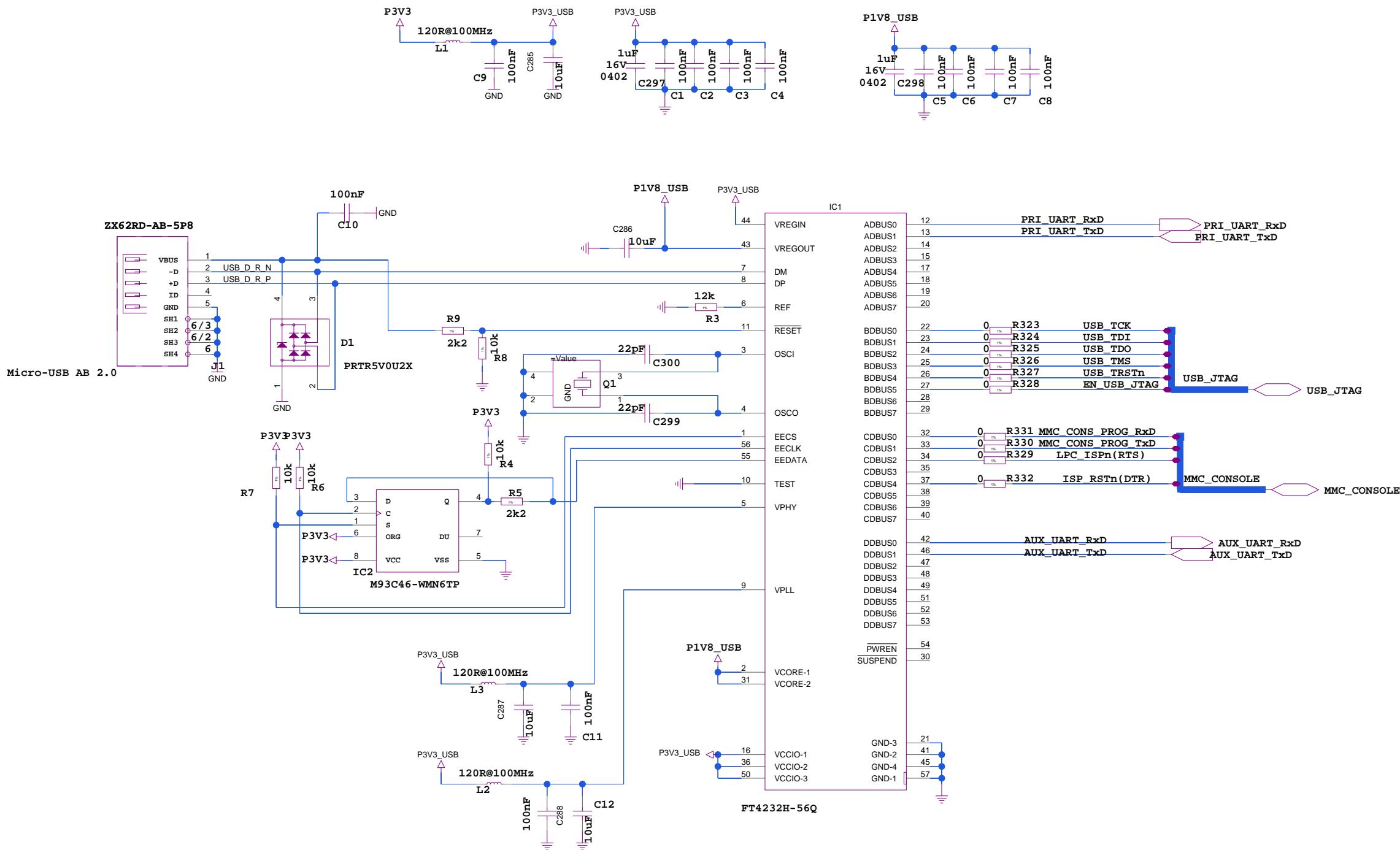
CPU LPC1776



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SI5324_CLK_RECOVERY

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USB_SERIAL_QUAD

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