

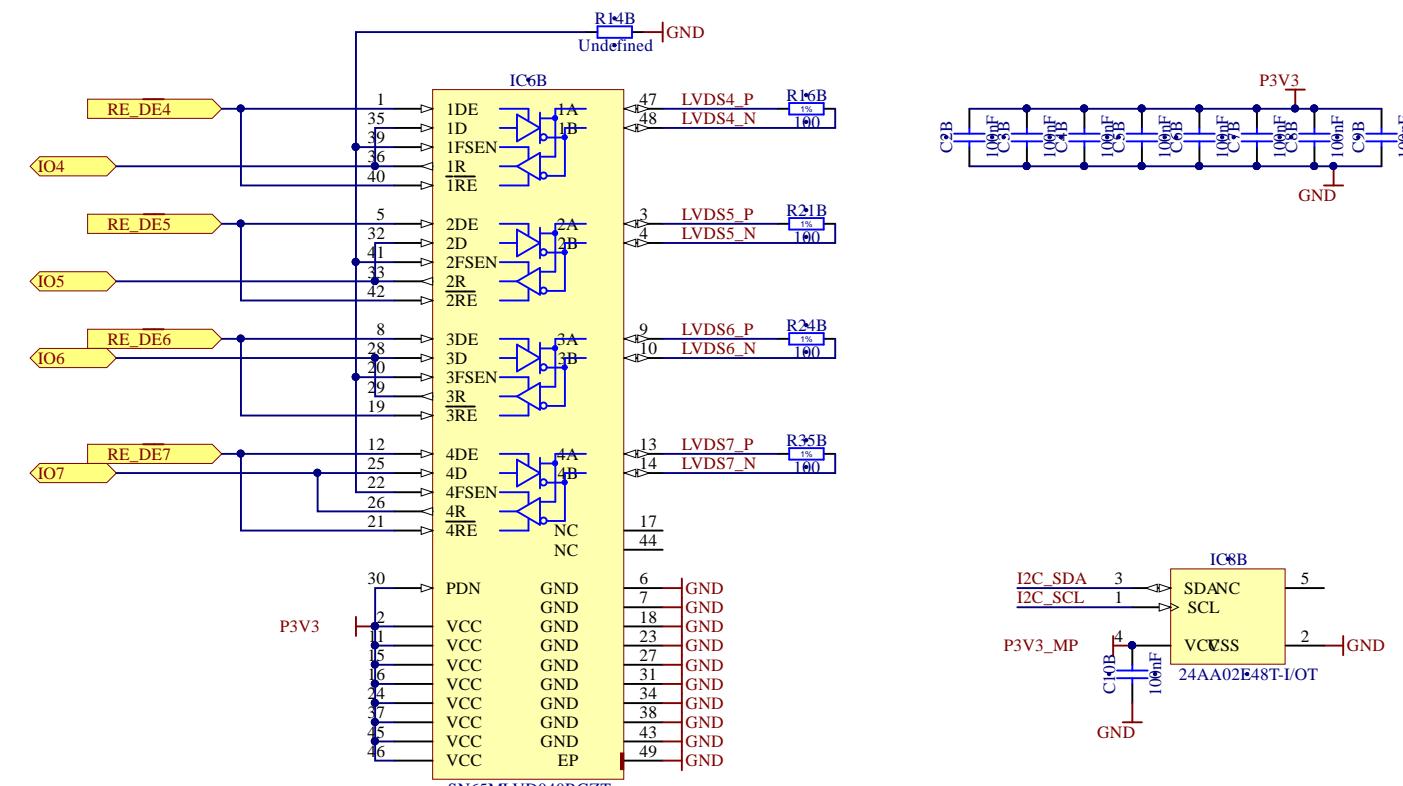
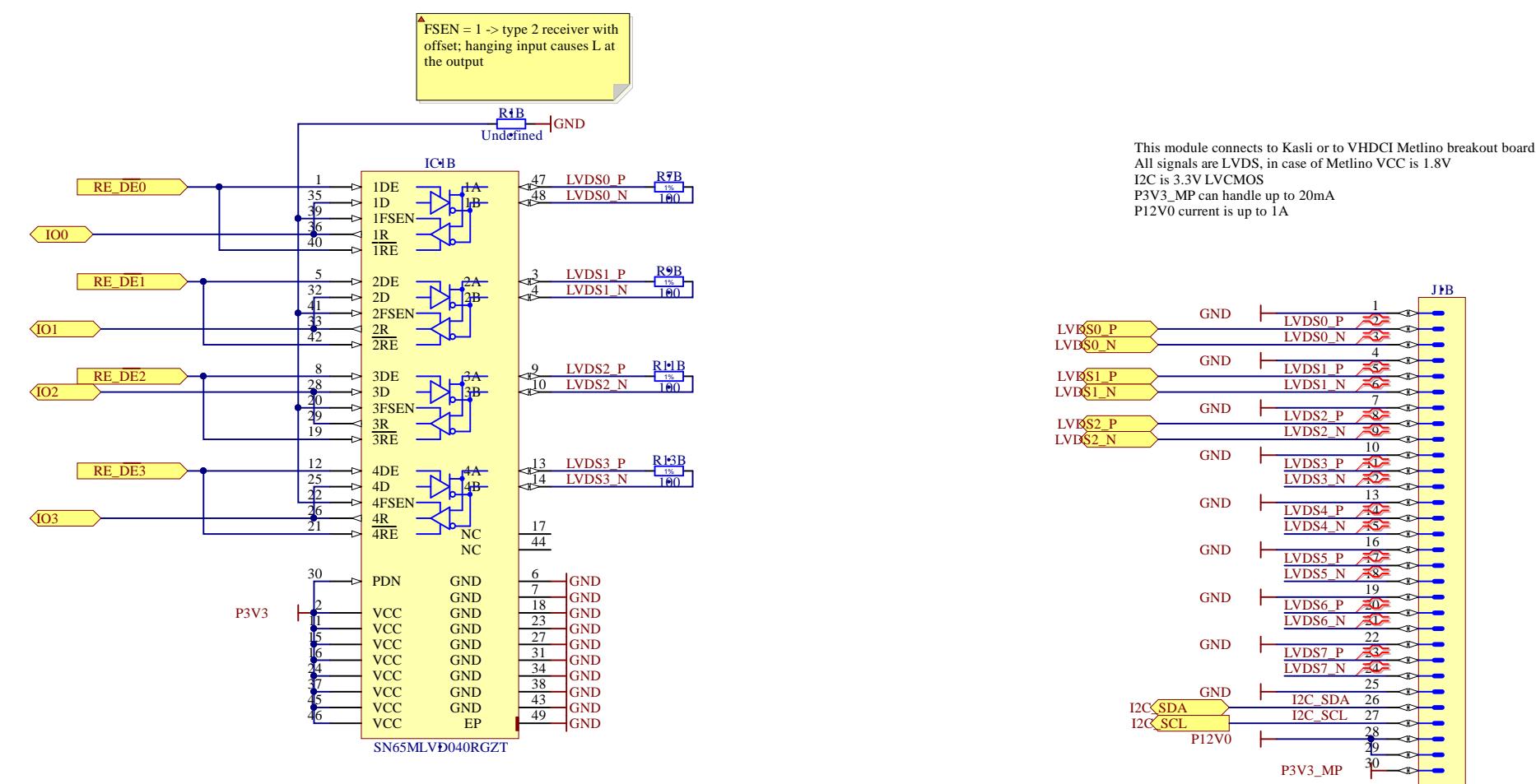
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For more information about the study, please contact Dr. John Smith at (555) 123-4567 or via email at [john.smith@researchinstitute.org](mailto:john.smith@researchinstitute.org).

*PCB\_3U\_DDS.PrjPCB  
LVDS IFC DDS.SchDoc*

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Project/Equipment ARTIQ/SINARA

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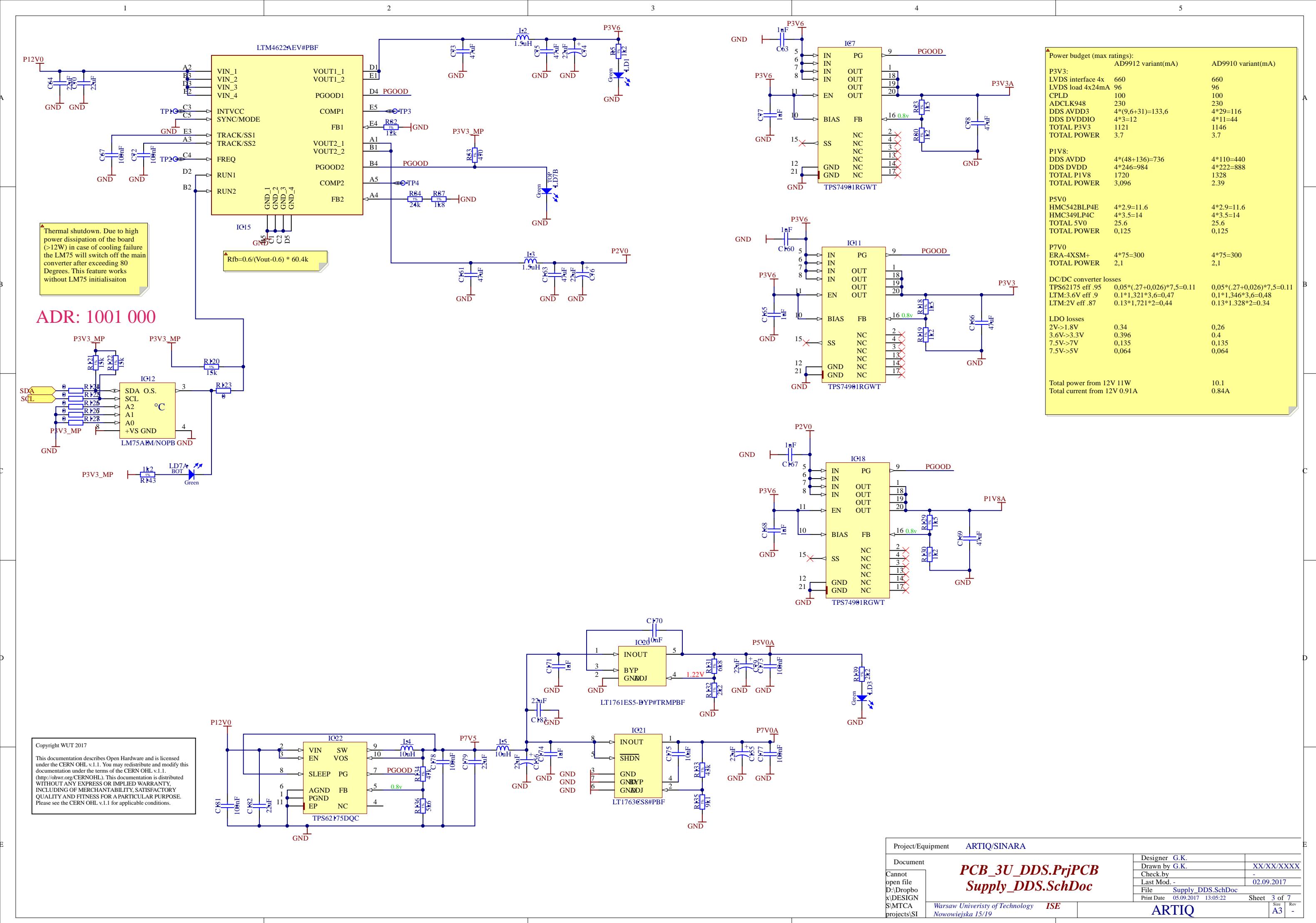
**PCB\_3U\_DDS.PjPCB**  
**LVDS\_IFC\_DDS.SchDoc**

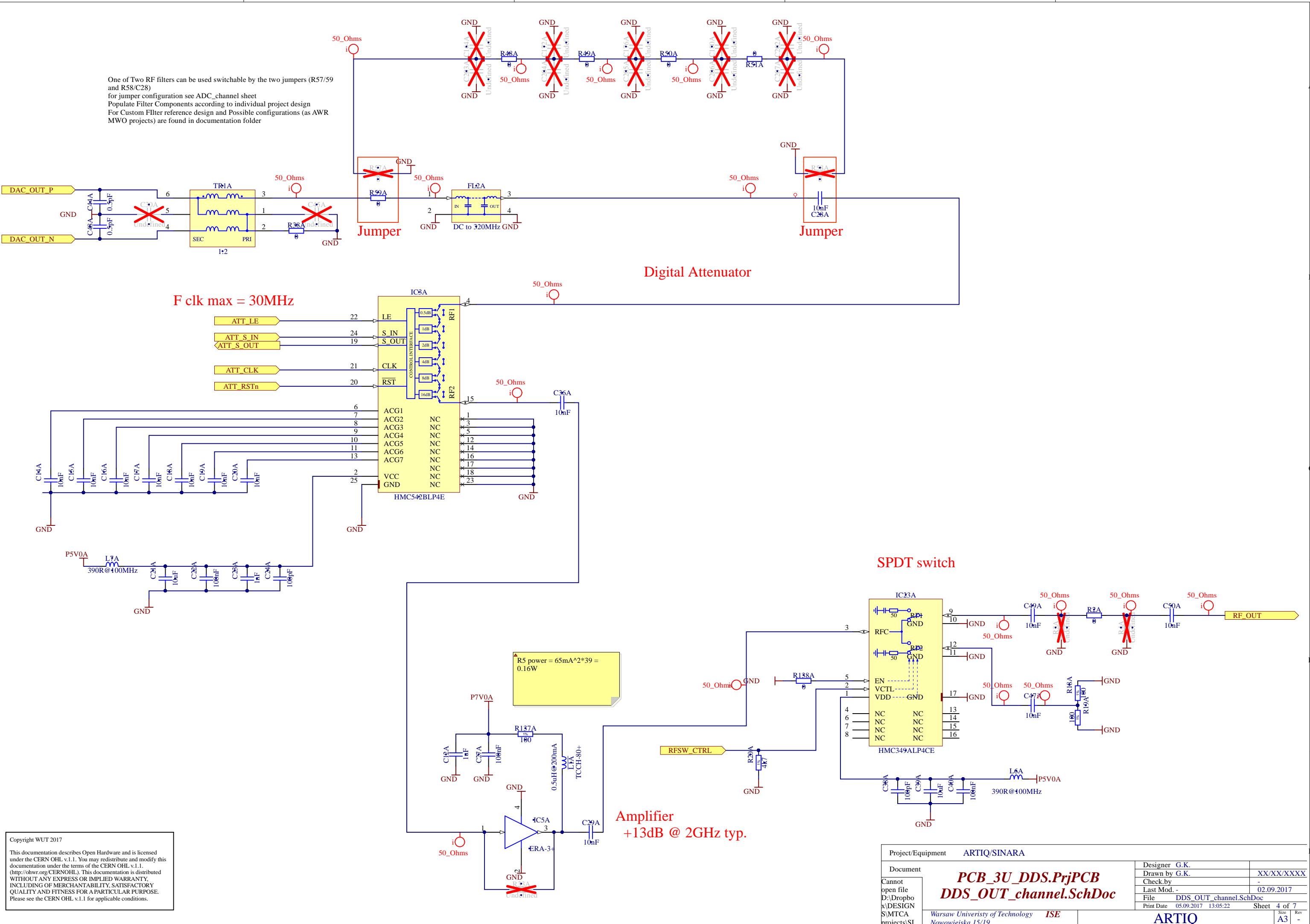
Designer G.K.	Drawn by G.K.	XX/XX/XXXX
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Last Mod.	-	02.09.2017
File	LVDS_IFC_DDS.SchDoc	
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ARTIQ

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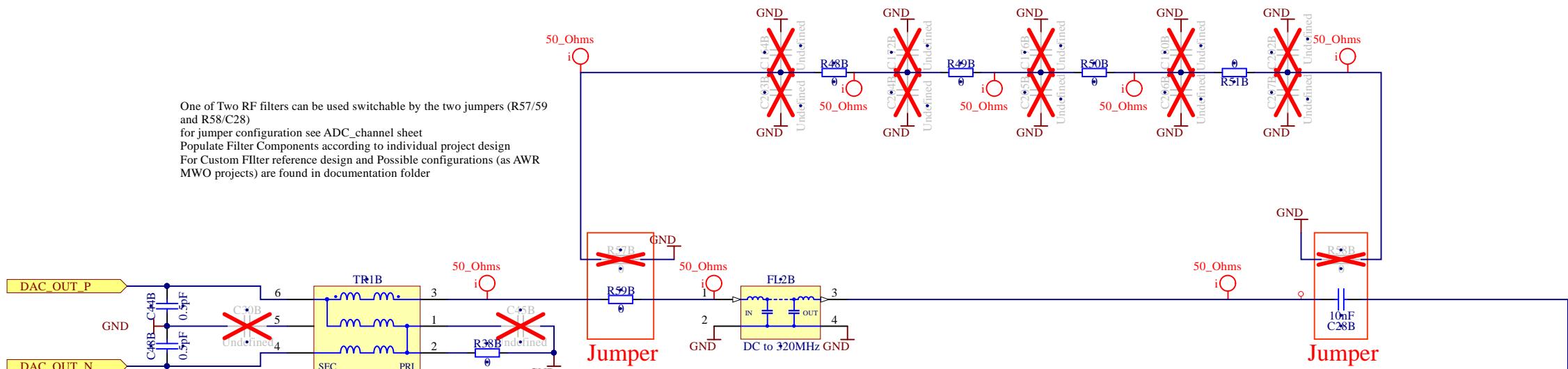




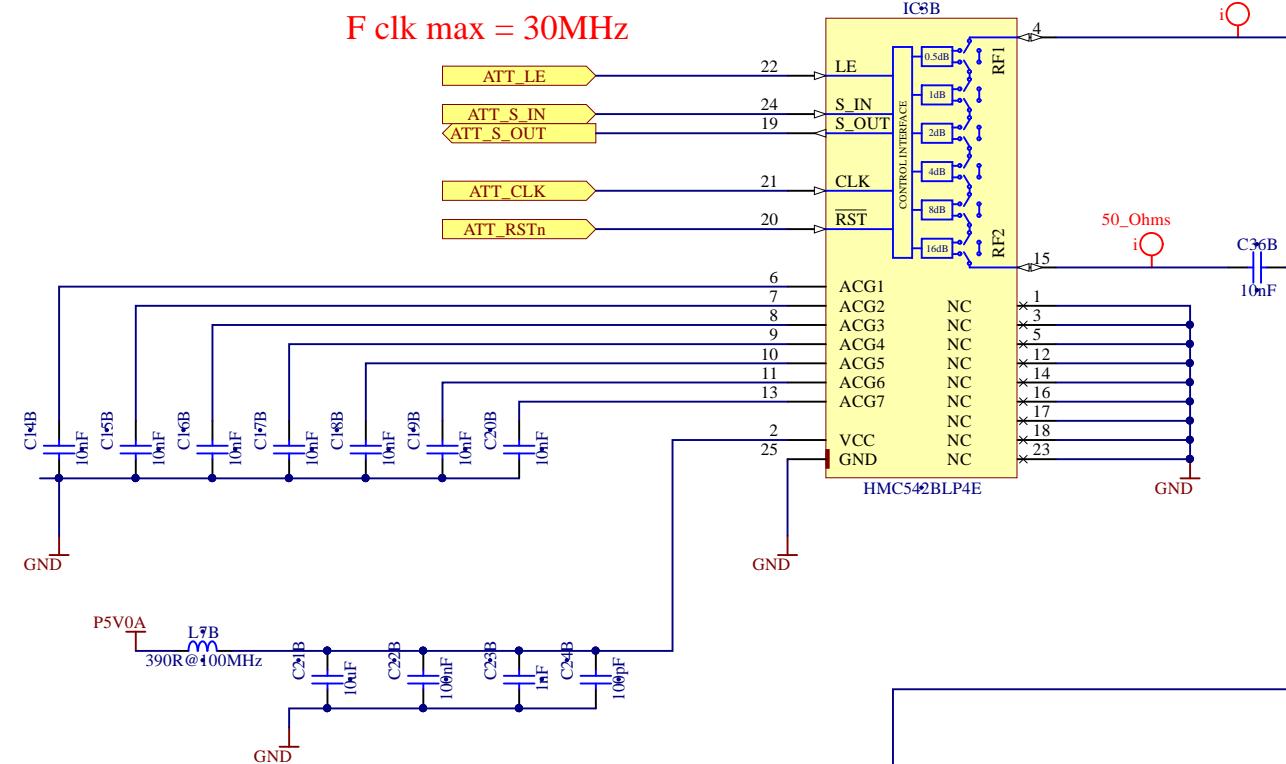
1 2 3 4 5

A A

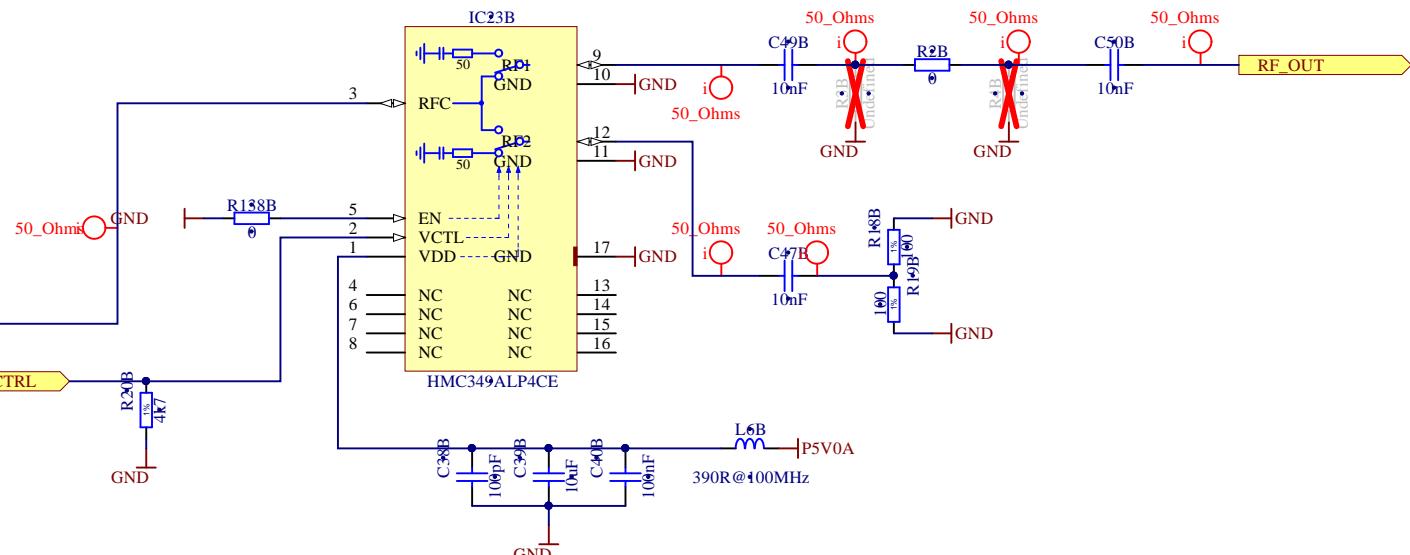
One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)  
for jumper configuration see ADC\_channel sheet  
Populate Filter Components according to individual project design  
For Custom Filter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder



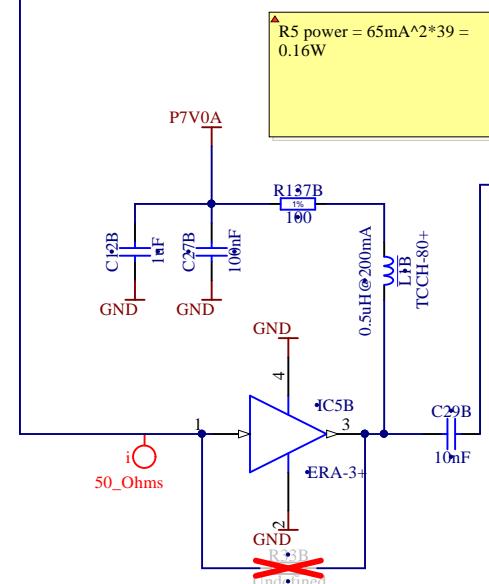
### Digital Attenuator



### SPDT switch



### Amplifier +13dB @ 2GHz typ.



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**PCB\_3U\_DDS.PrjPCB**  
**DDS\_OUT\_channel.SchDoc**

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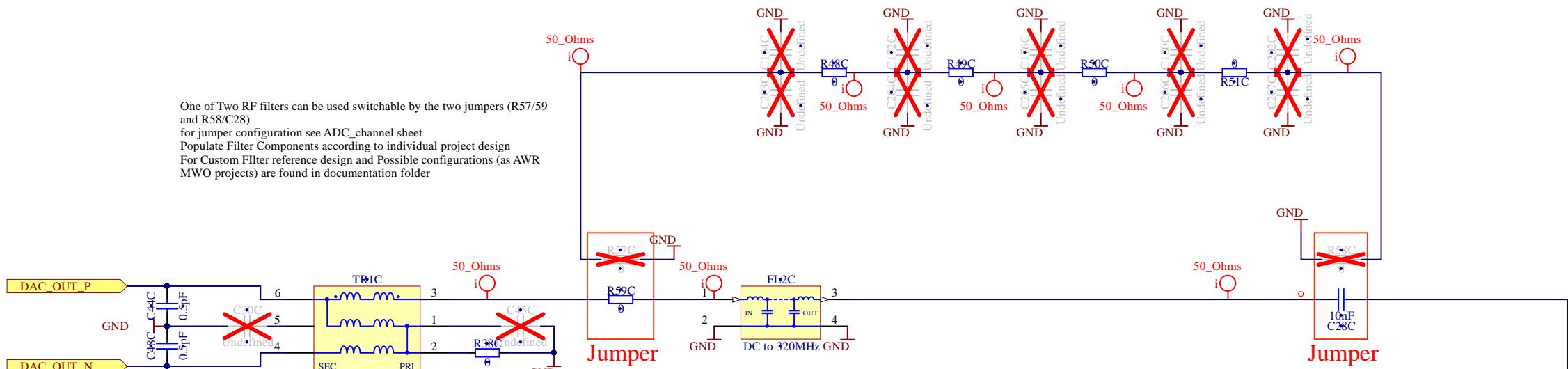
ARTIQ

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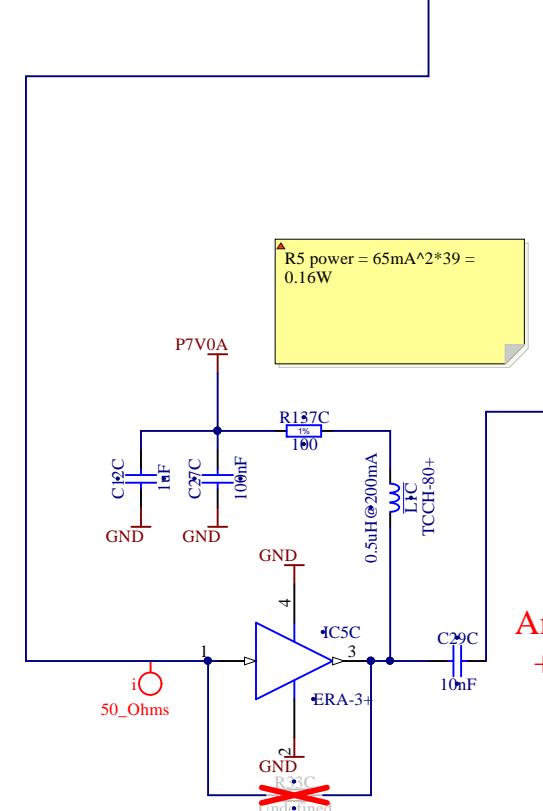
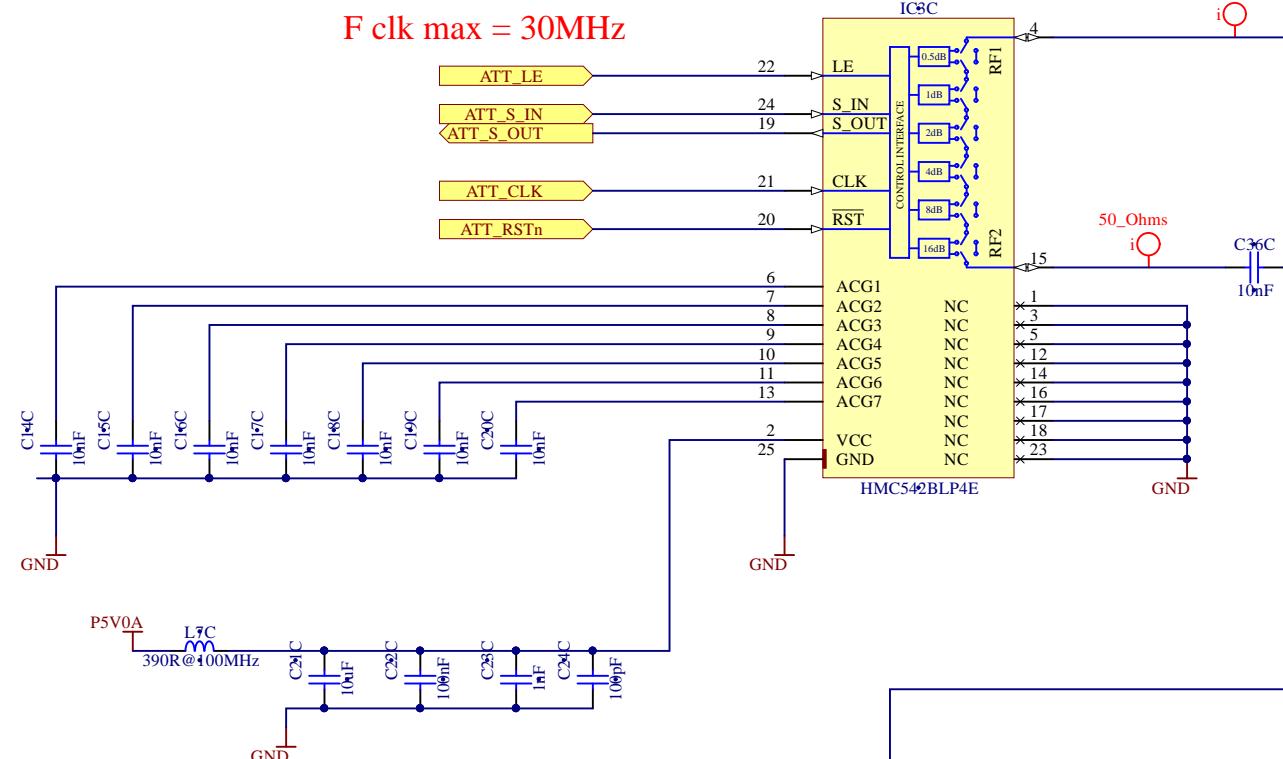
1 2 3 4 5

A A

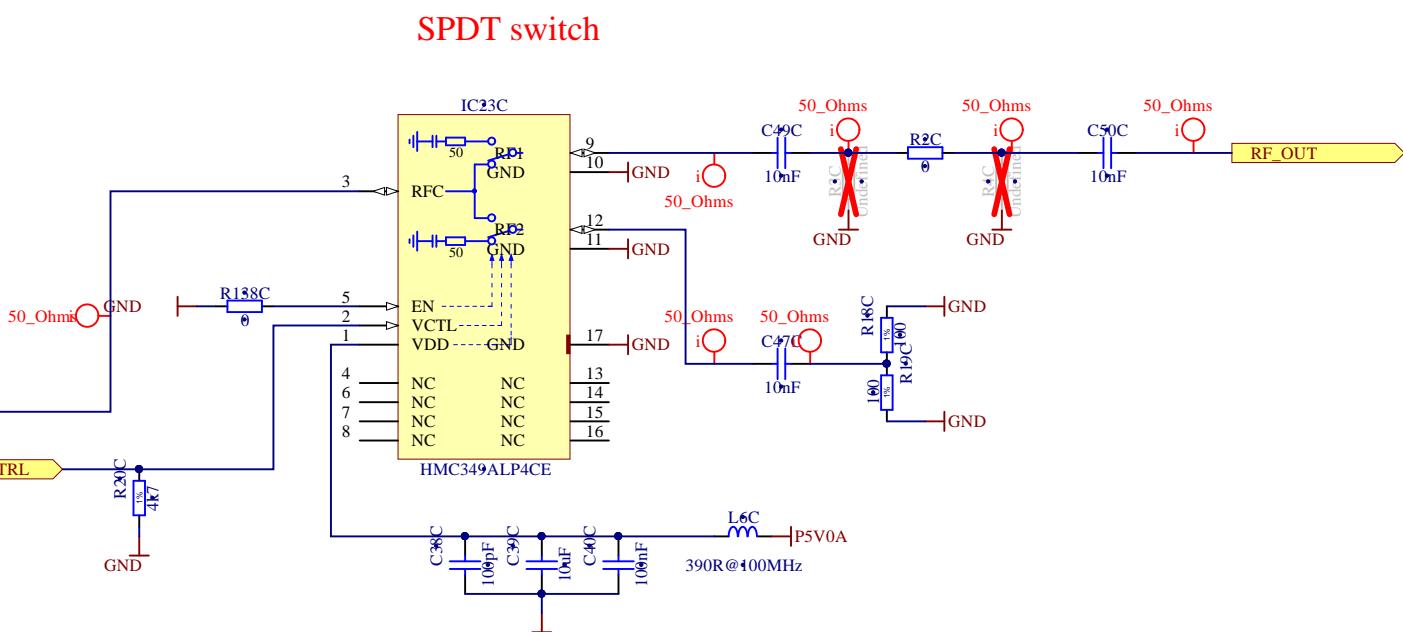
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### Digital Attenuator



Amplifier  
+13dB @ 2GHz typ.



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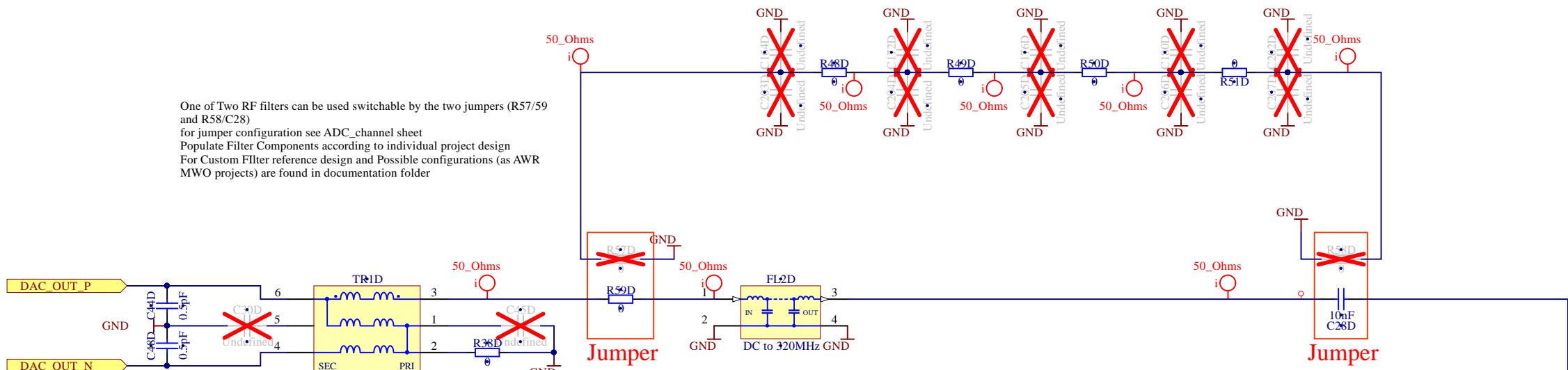
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ARTIQ Size A3 Rev -

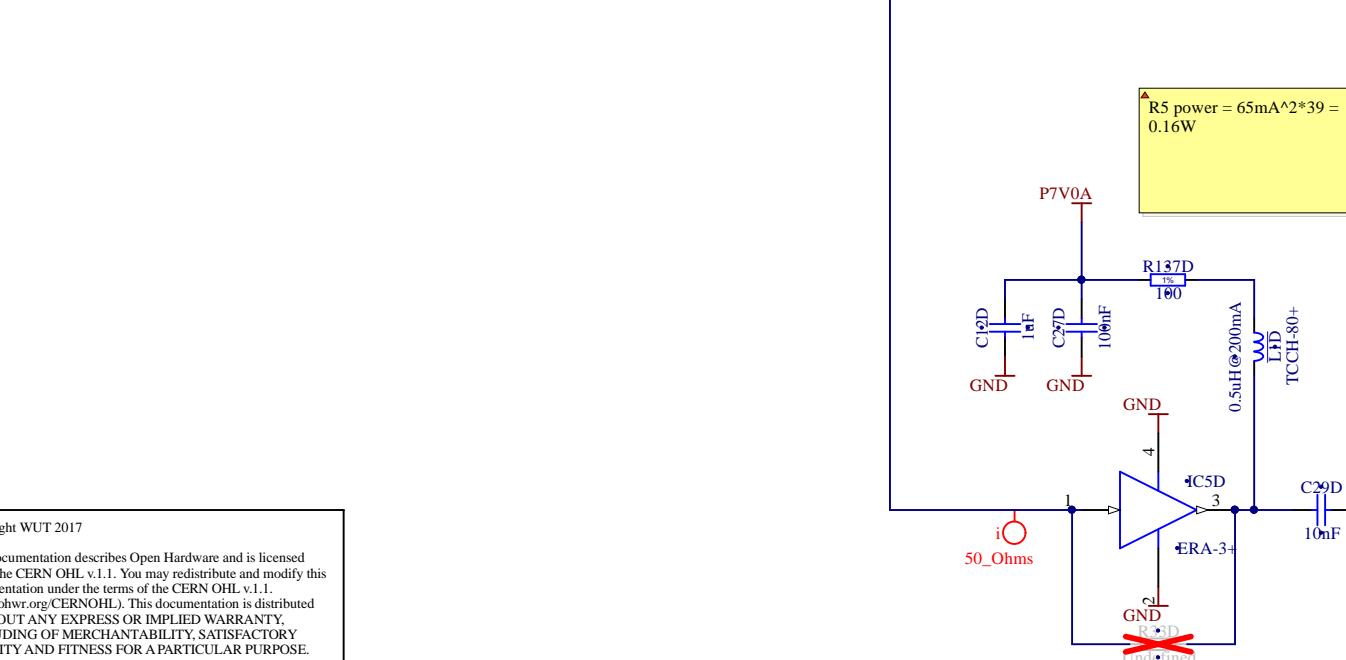
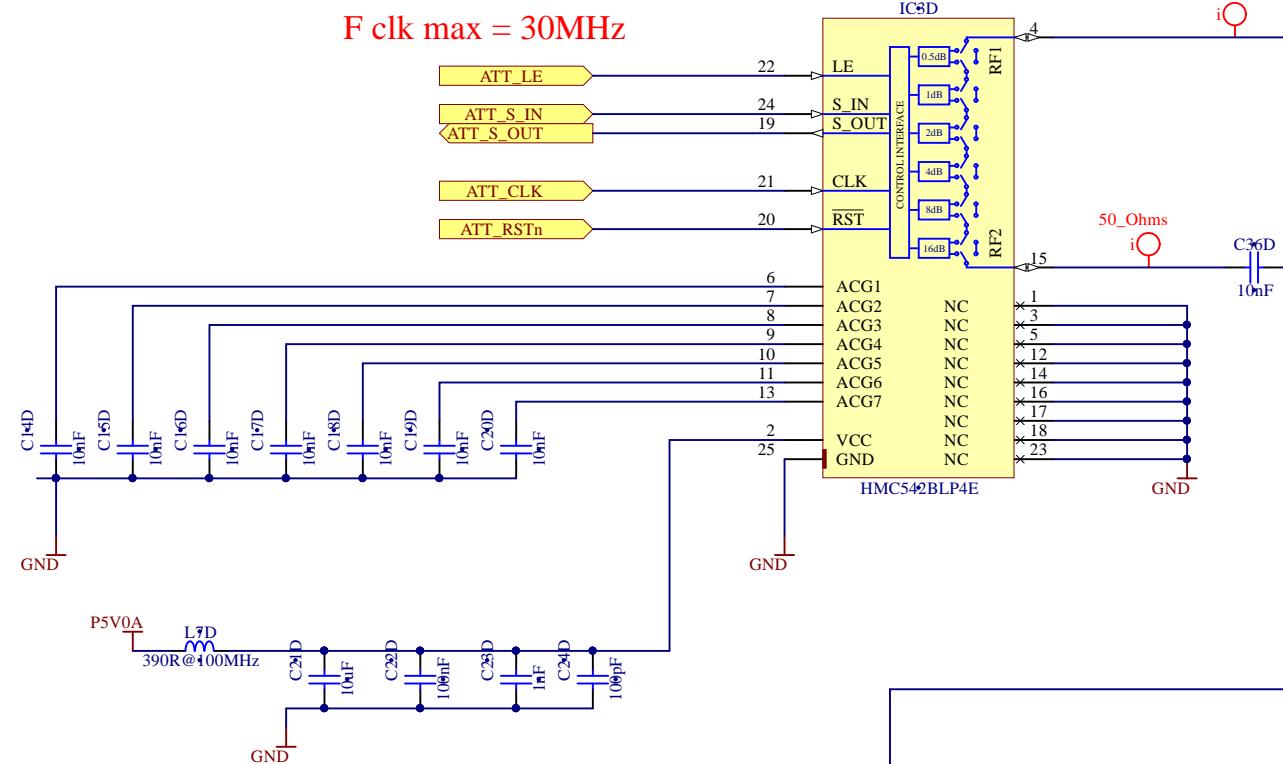
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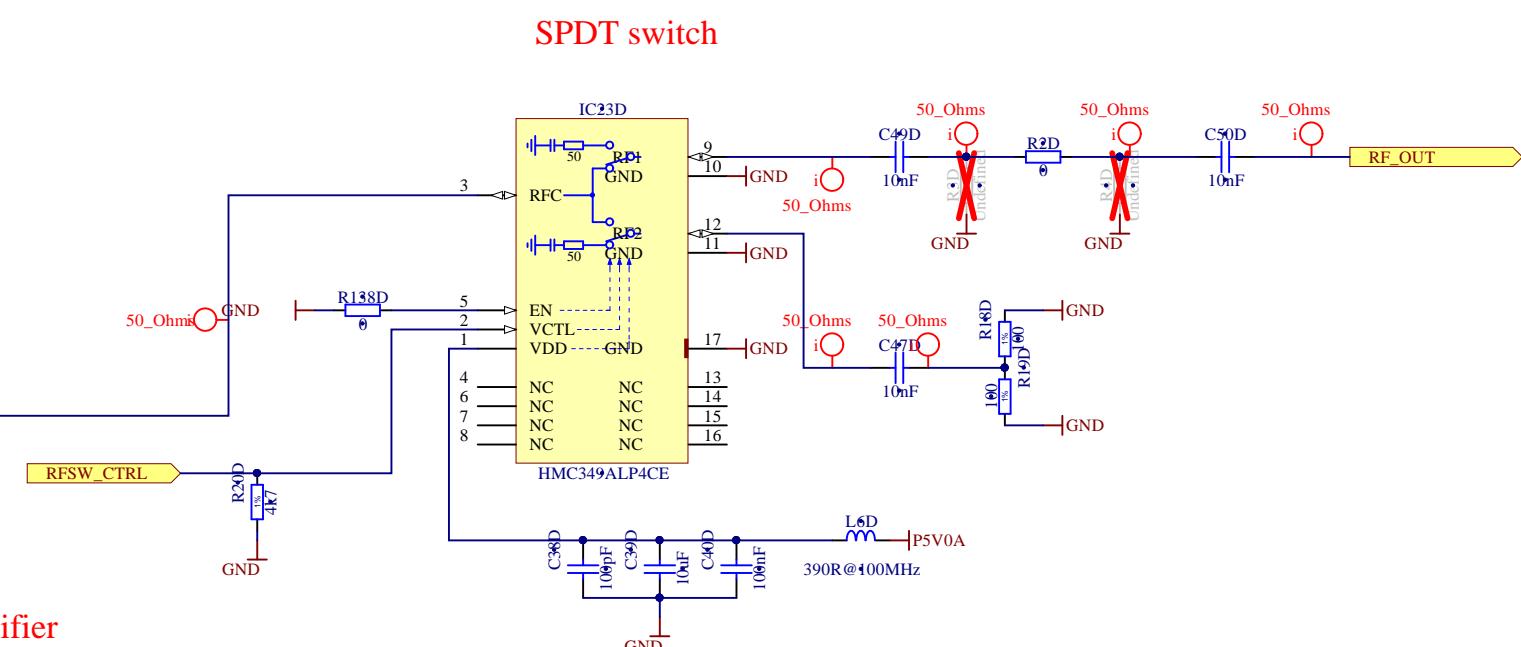
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### Digital Attenuator



**Amplifier**  
**+13dB @ 2GHz typ.**



Project/Equipment ARTIQ/SINARA

**PCB\_3U\_DDS.PrjPCB**  
**DDS\_OUT\_channel.SchDoc**

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Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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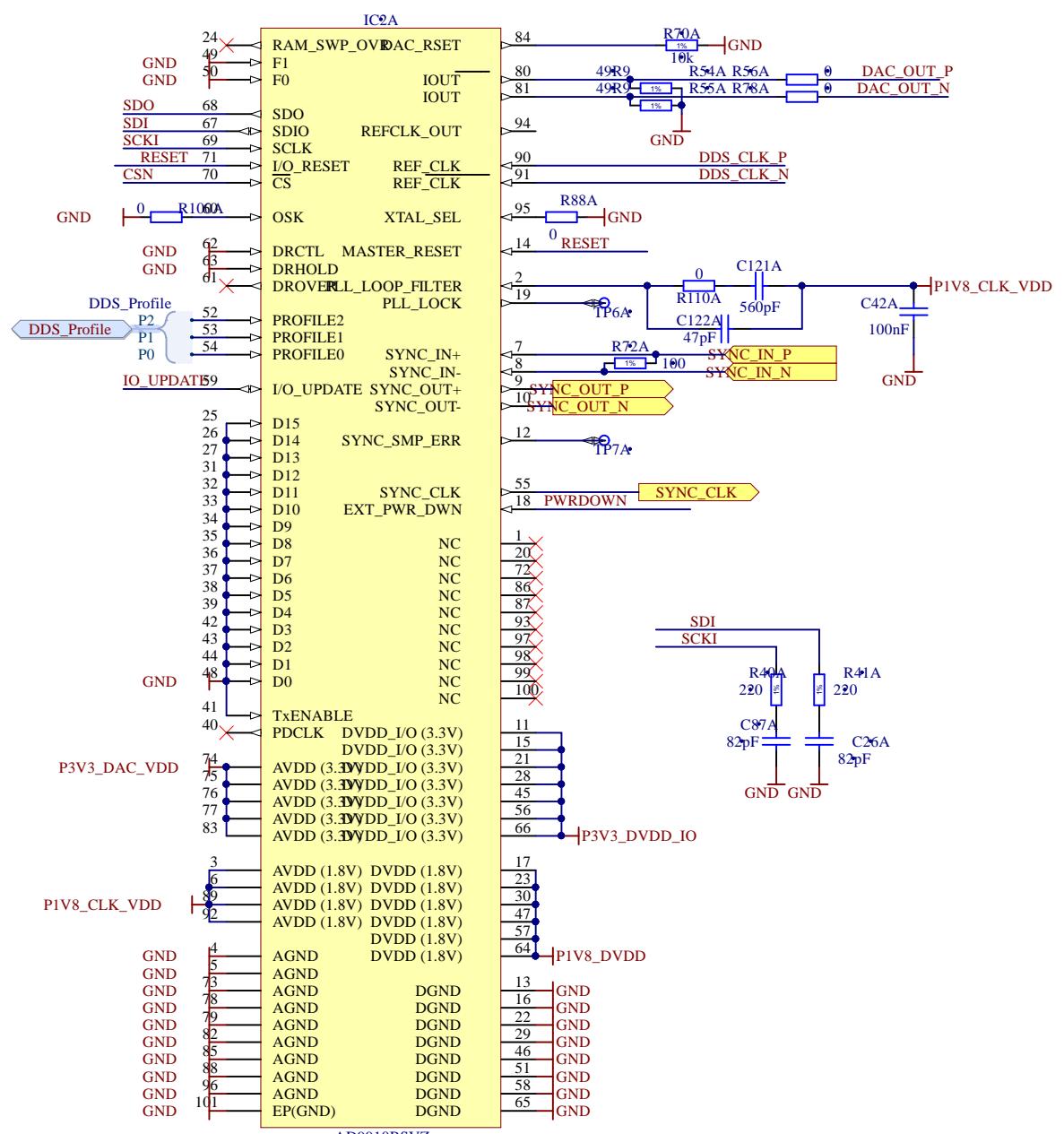
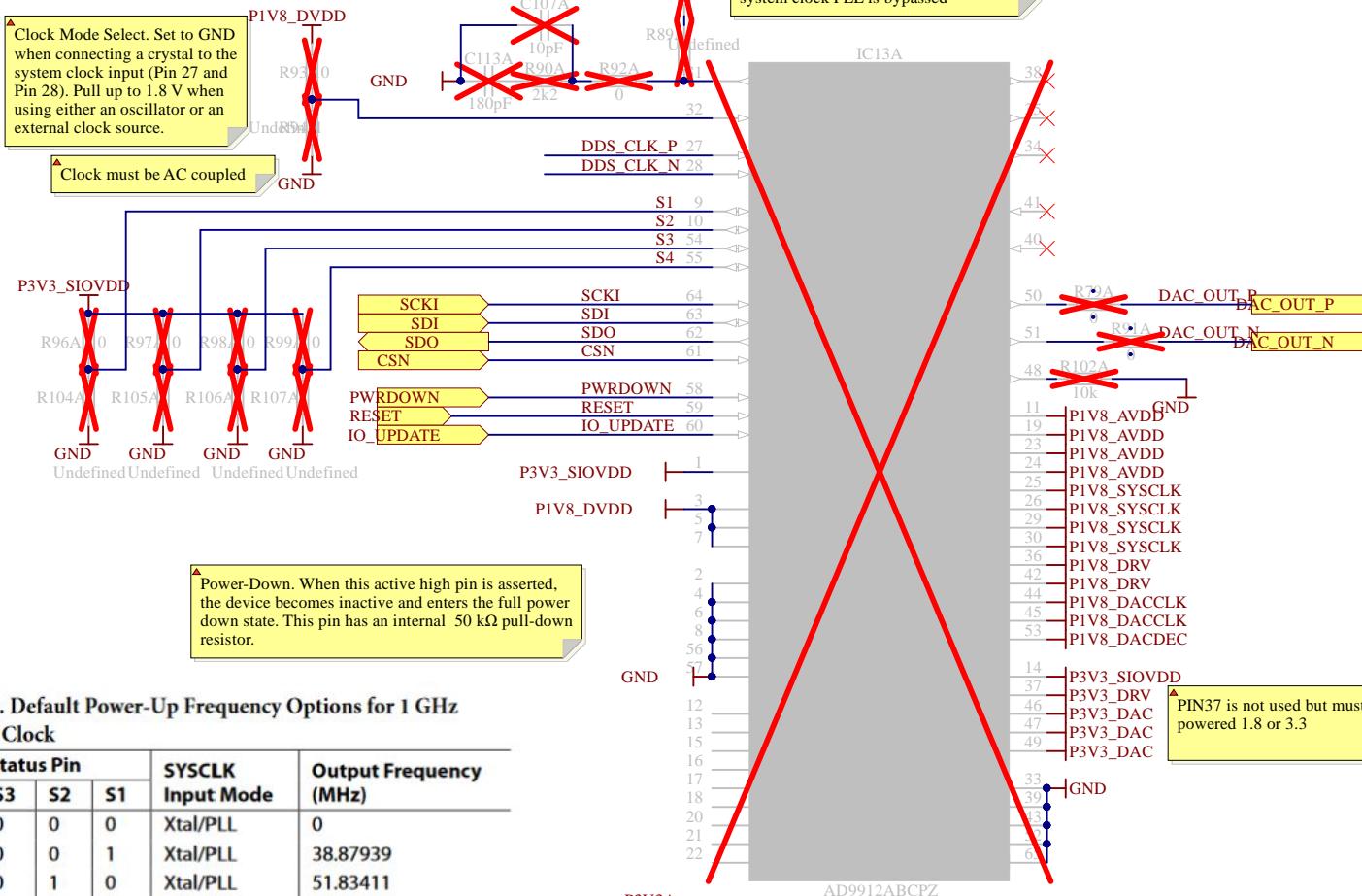
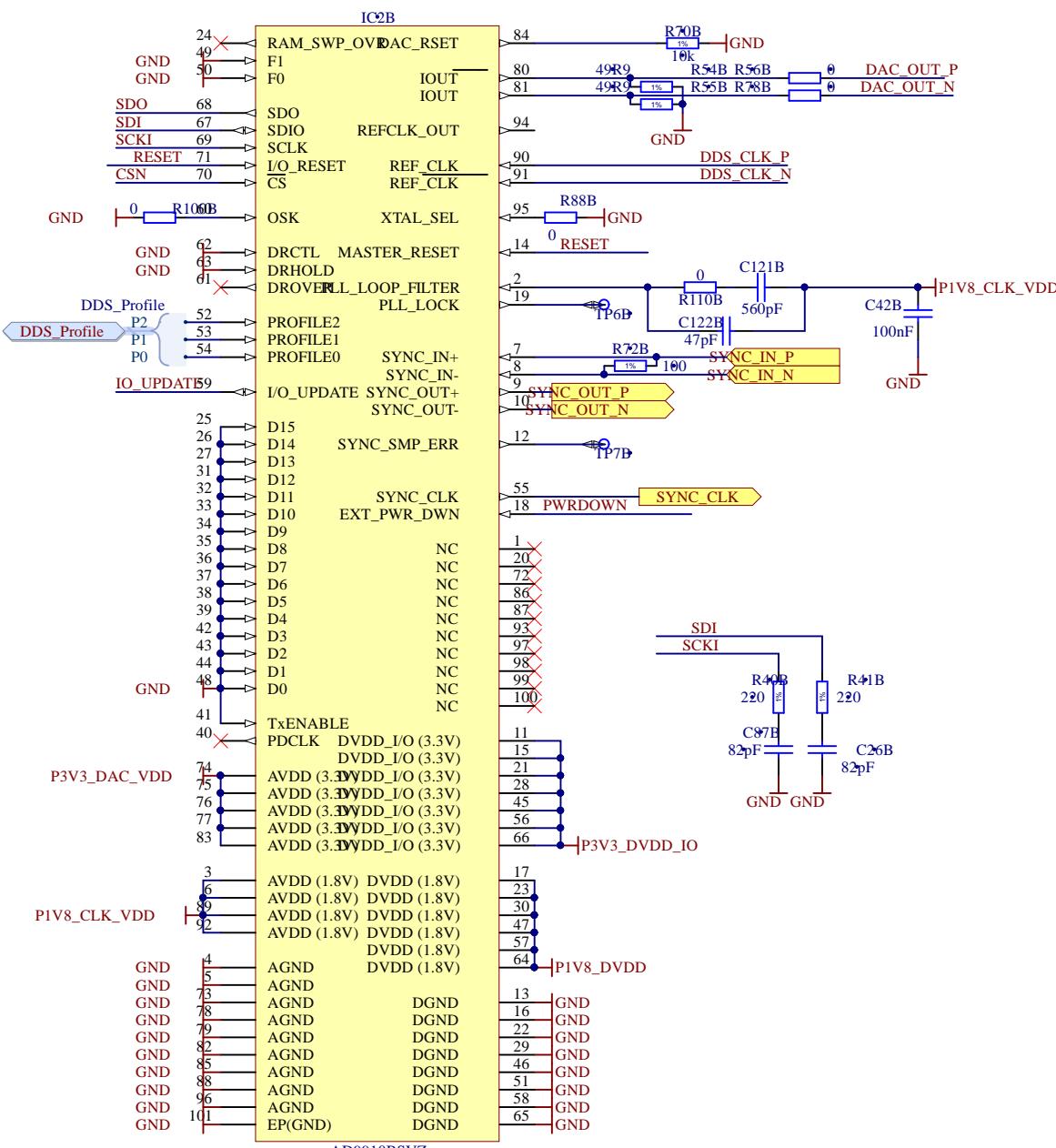
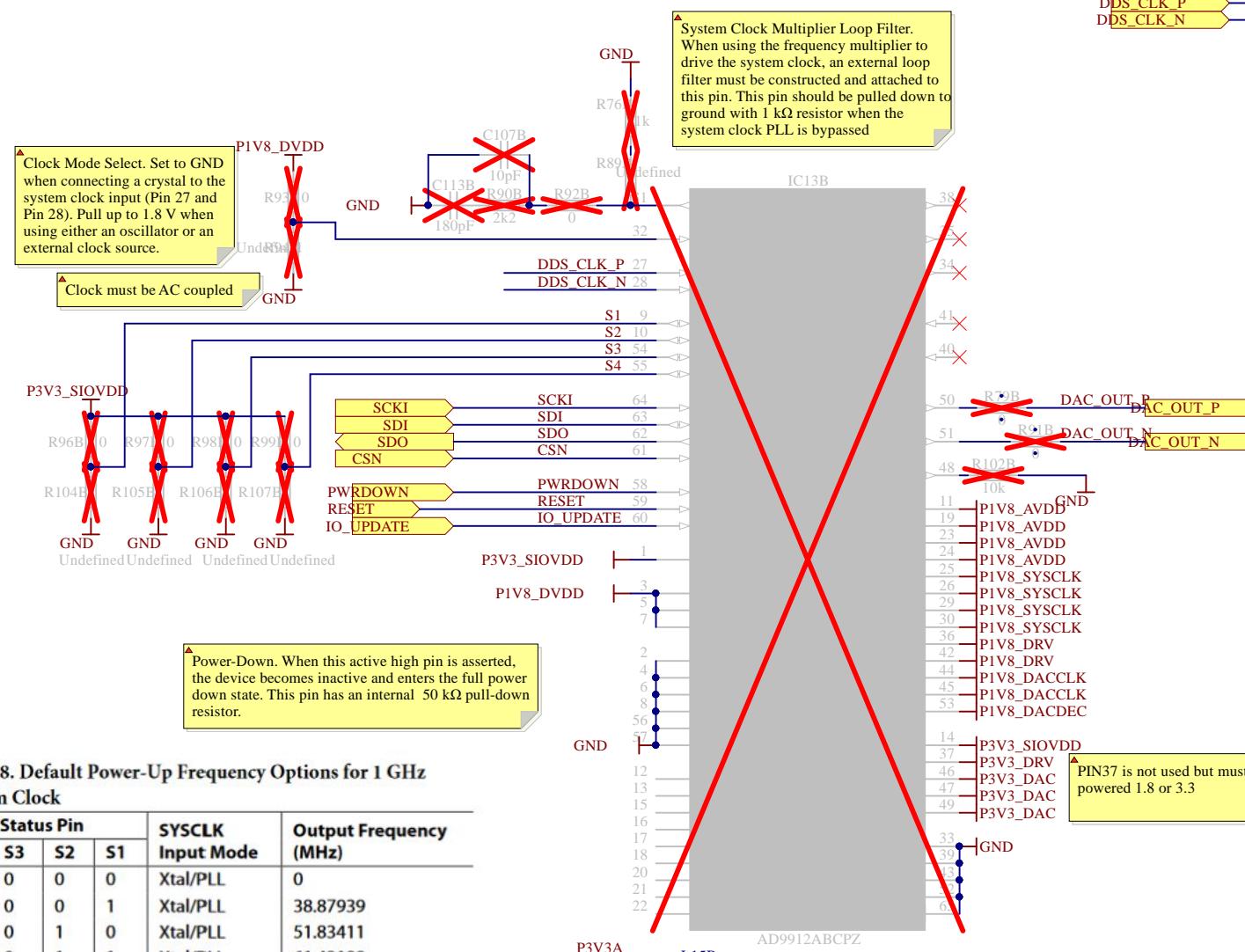


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
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0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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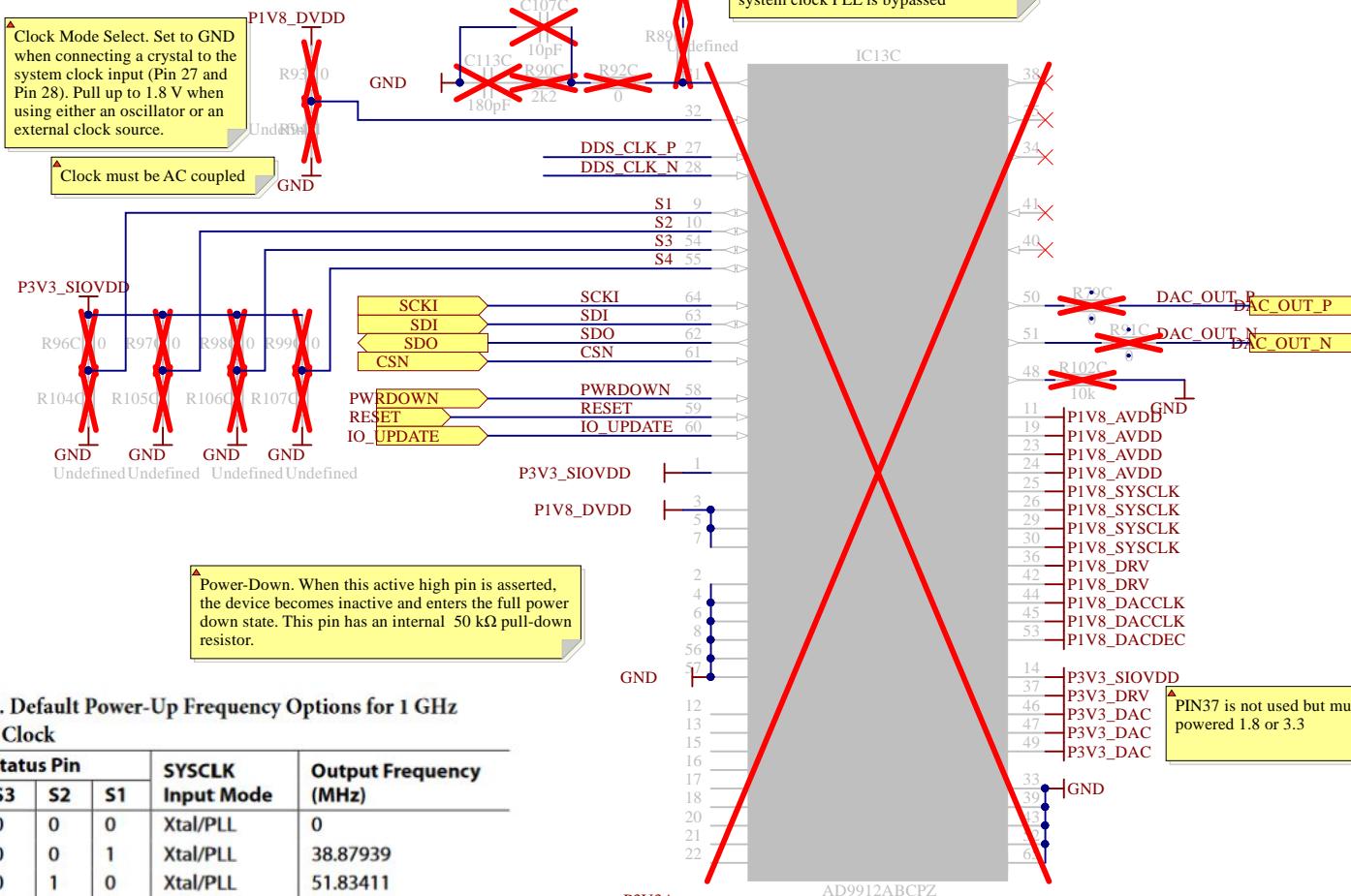
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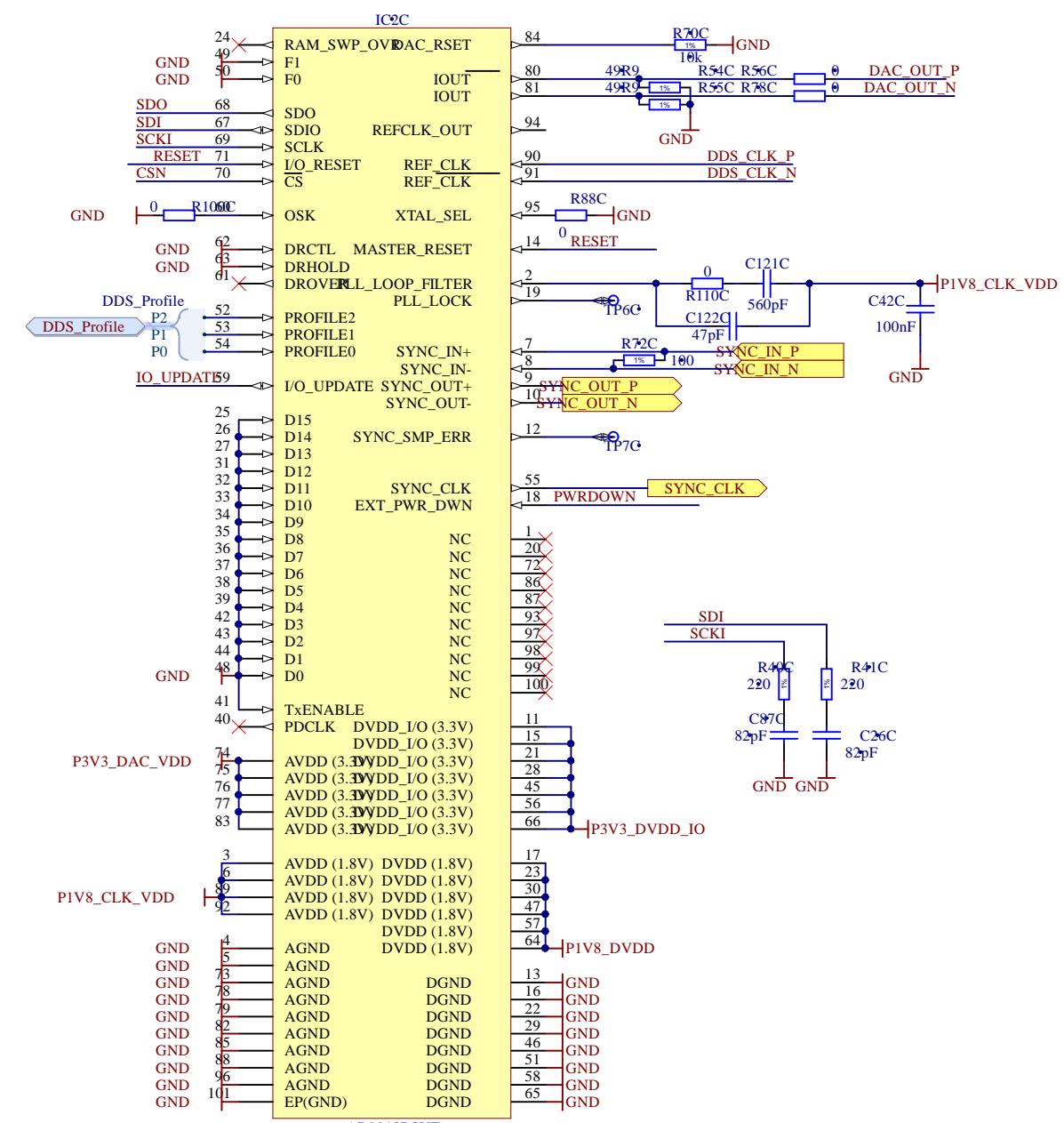
Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

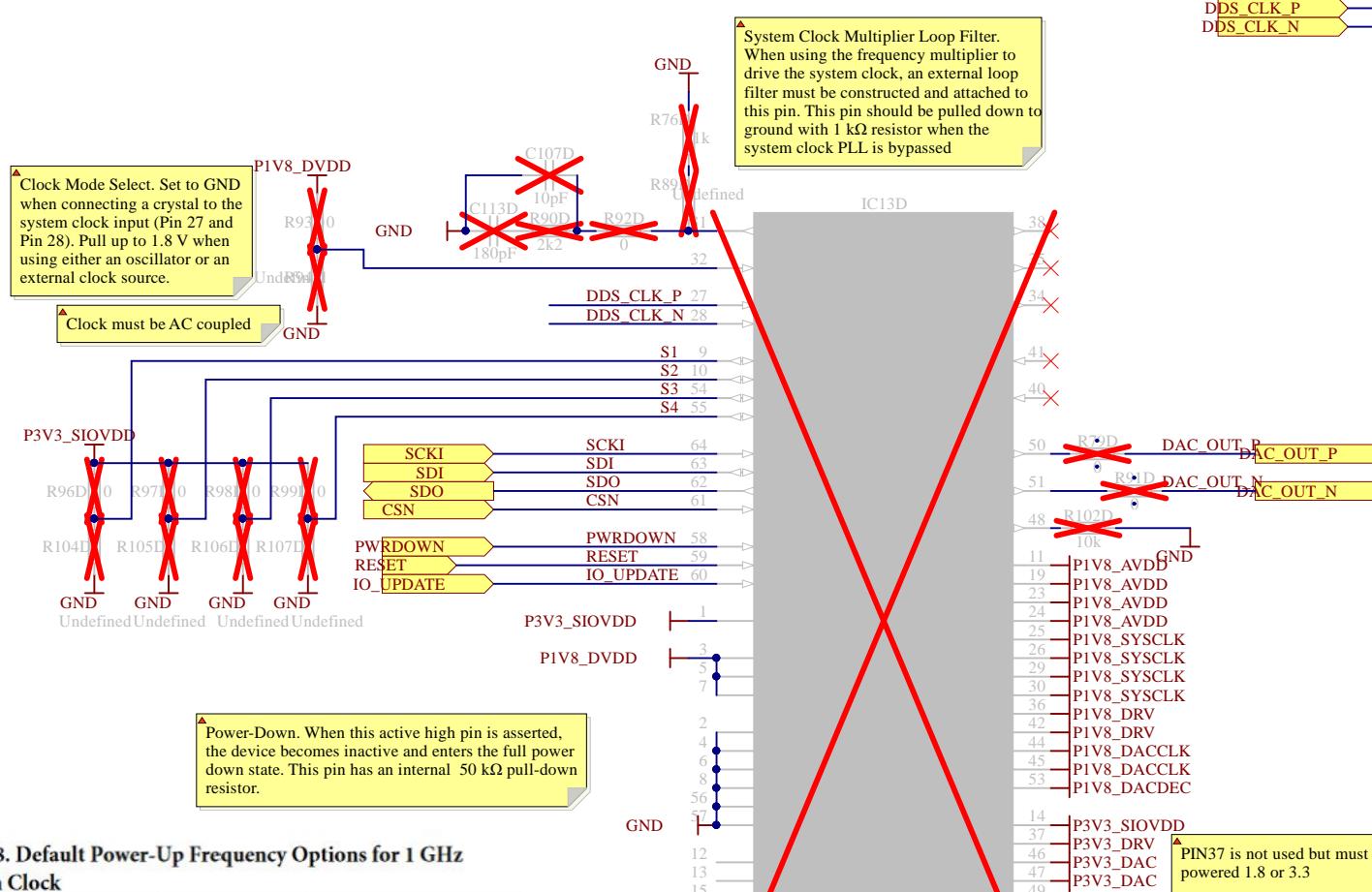
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0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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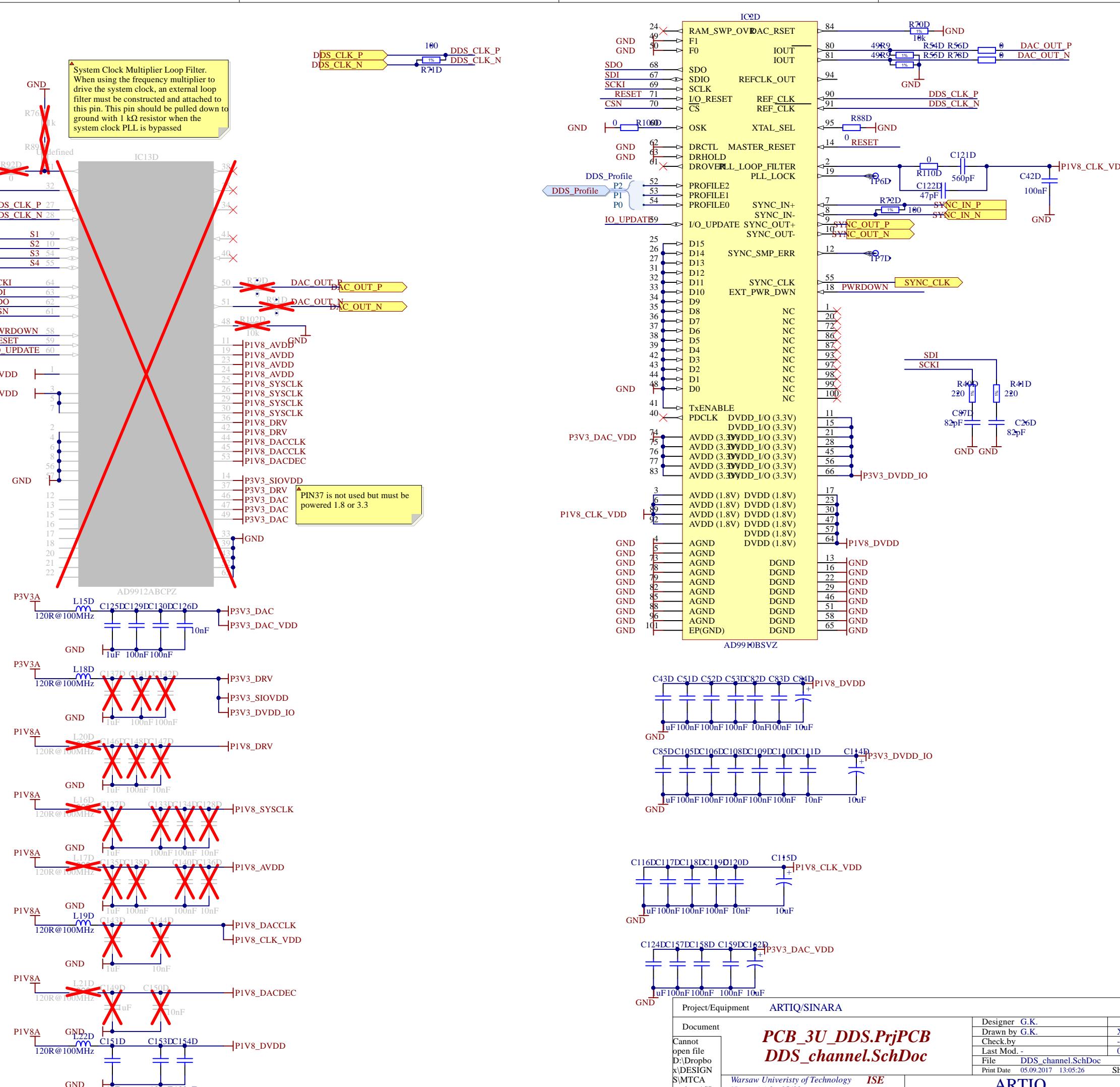
System Clock Multiplier Loop Filter.  
When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed.

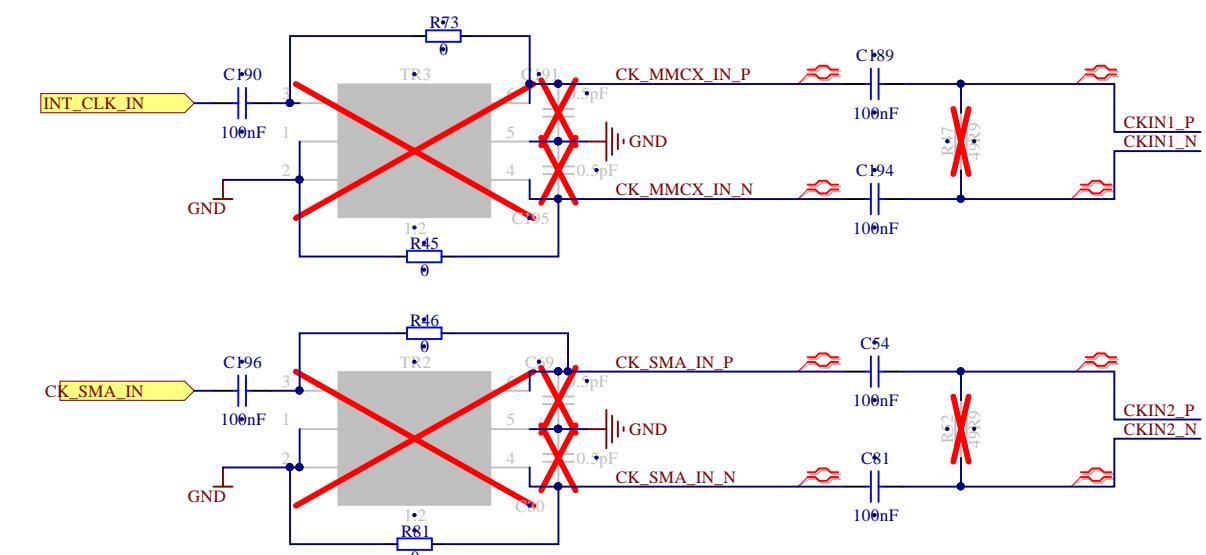




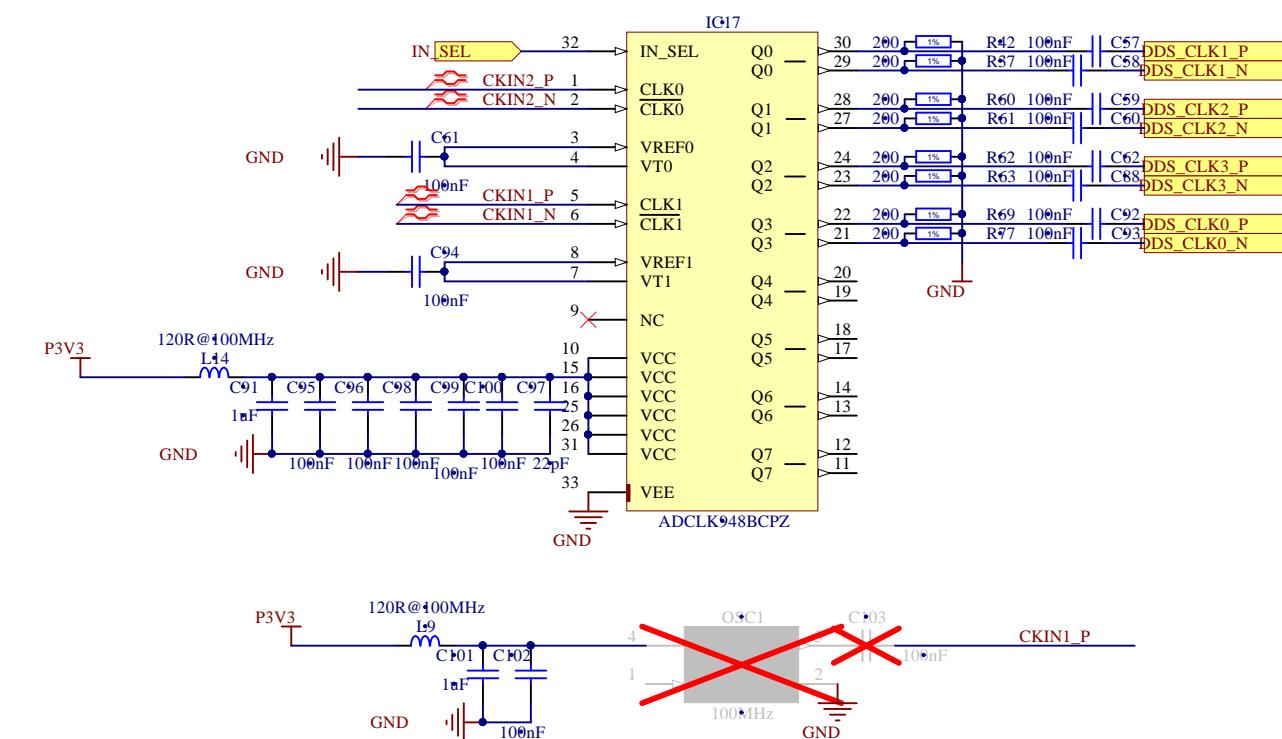
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0	1	1	0	Xtal/PLL	122.87903
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1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758



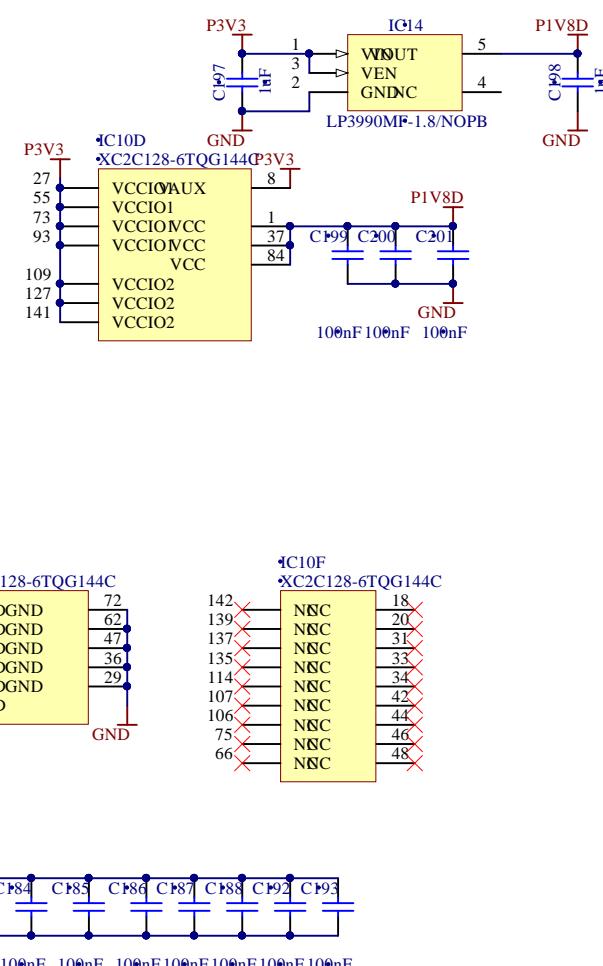
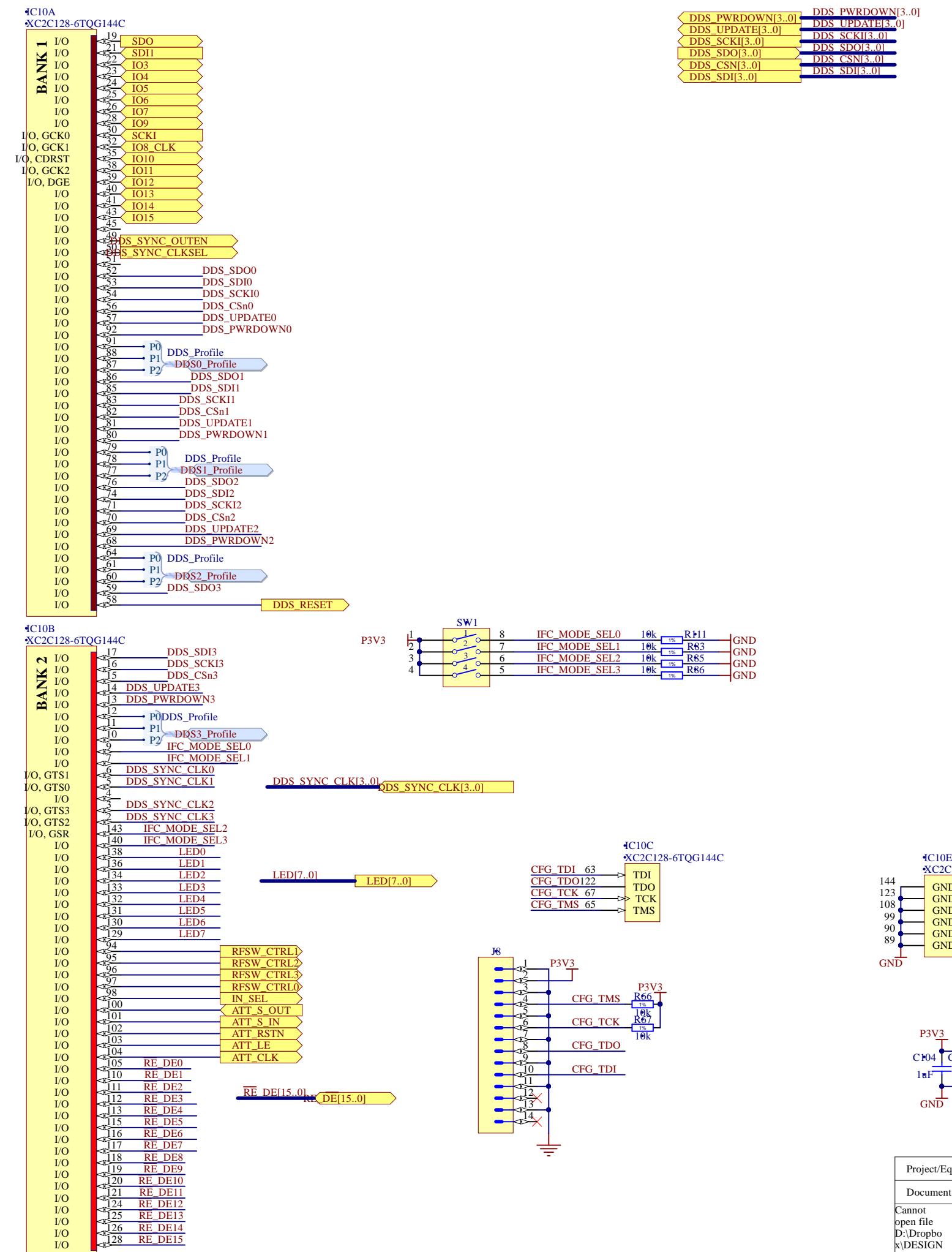


AC-Coupled Input  
Termination, Such as  
LVDS and LEVPEC

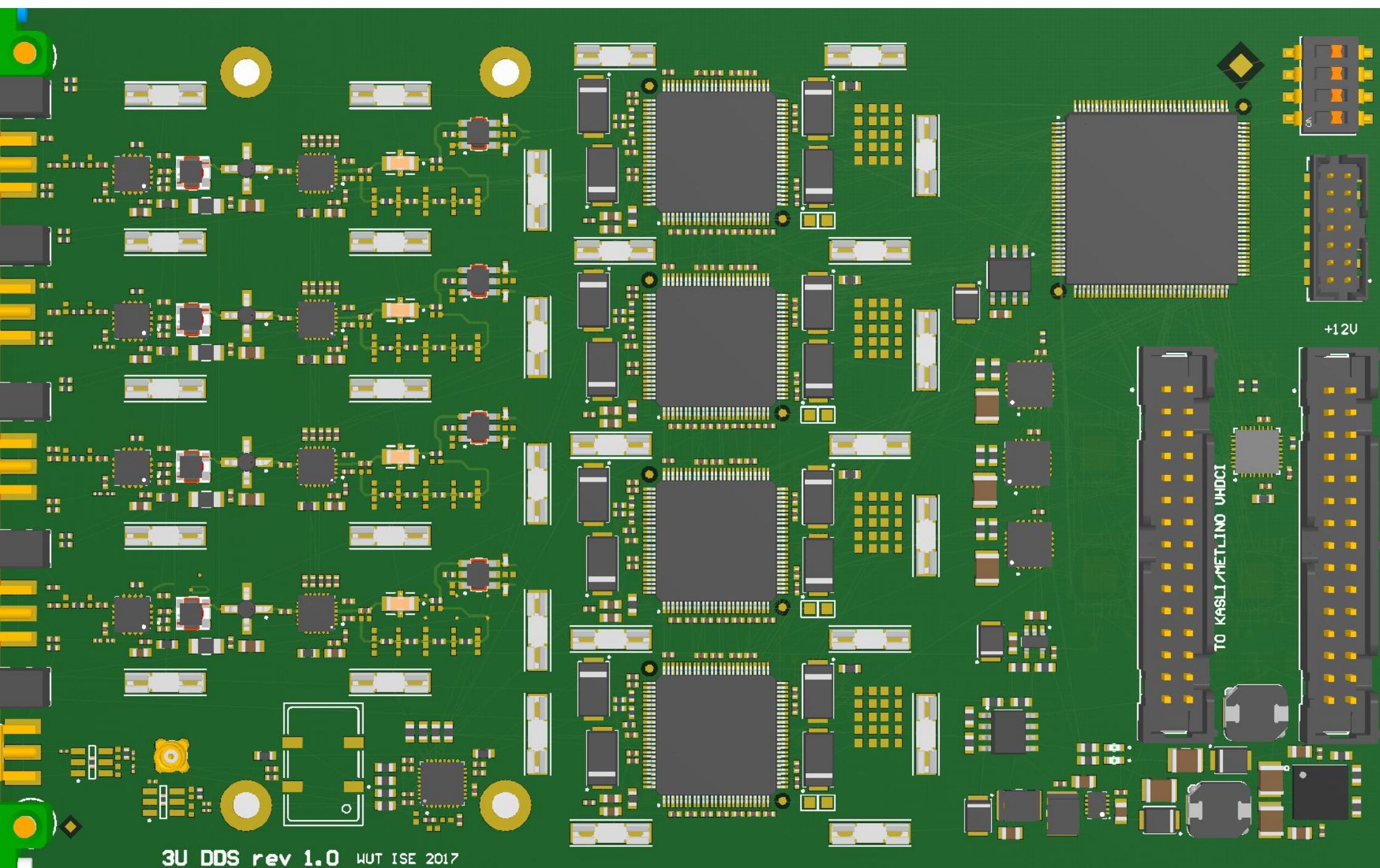


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Project/Equipment		ARTIQ/SINARA	
Document		Designer	G.K.
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	File	CTRL_LOGIC.SchDoc	
	Print Date	05.09.2017 13:05:26	Sheet 7 of 7
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