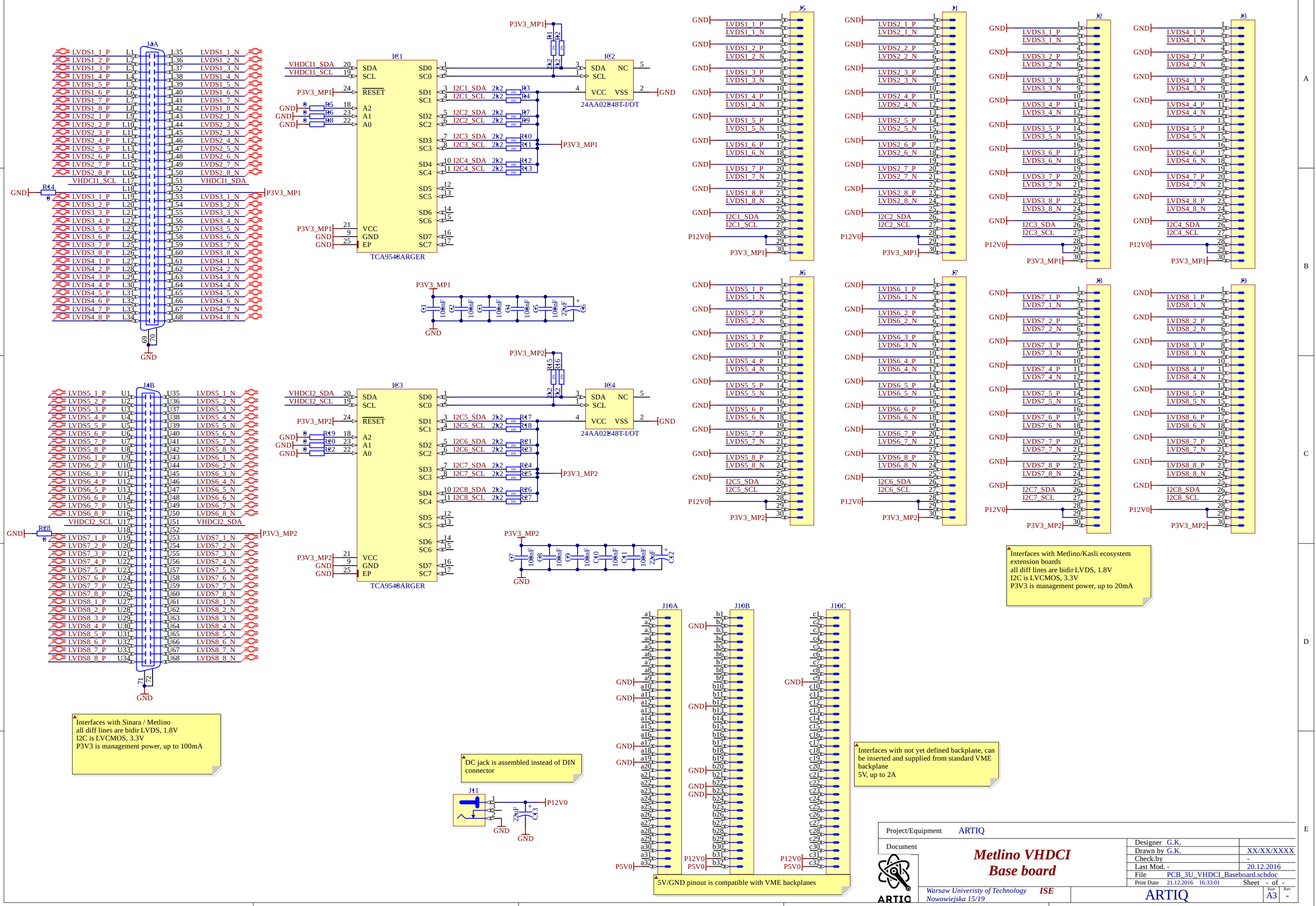
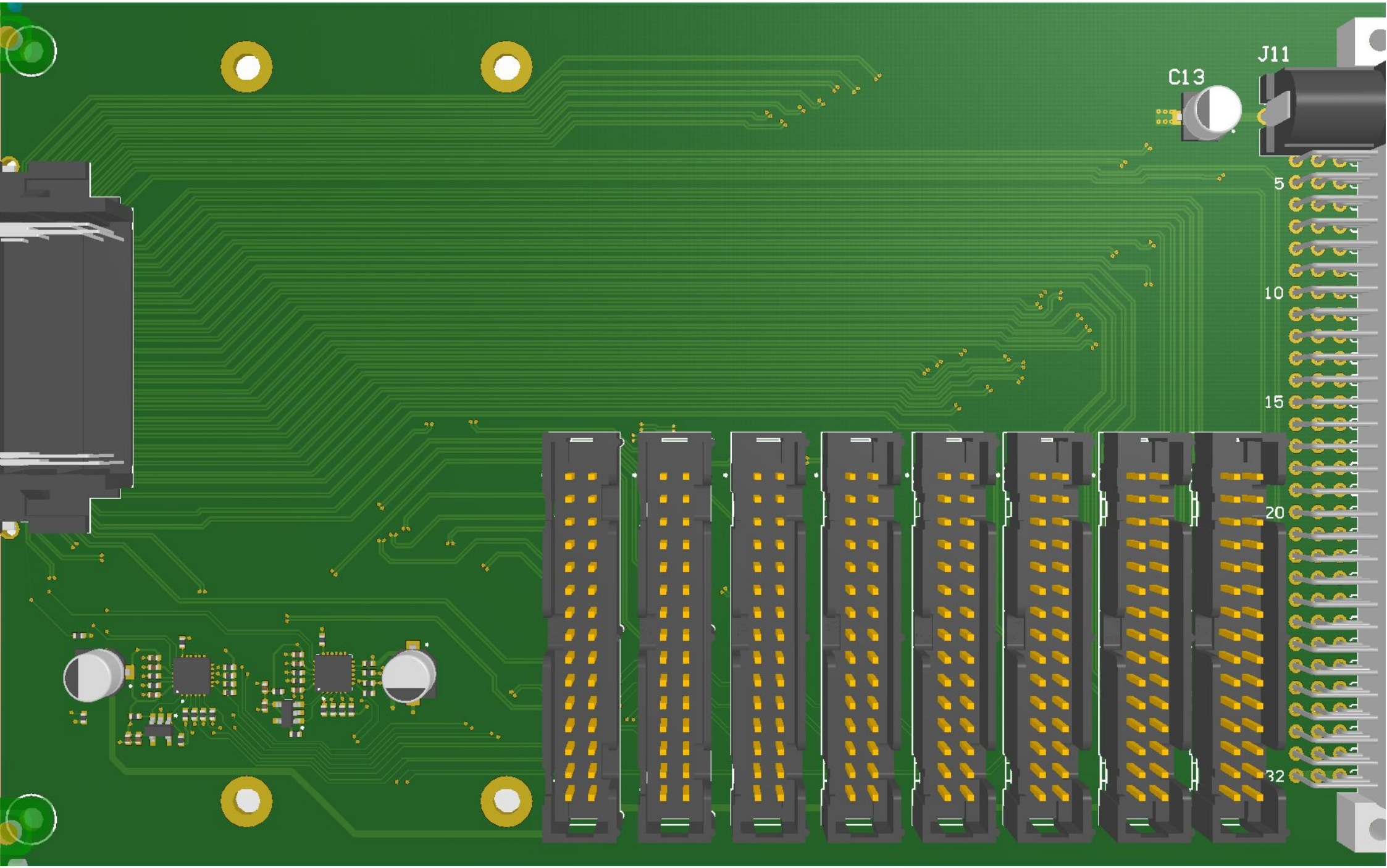
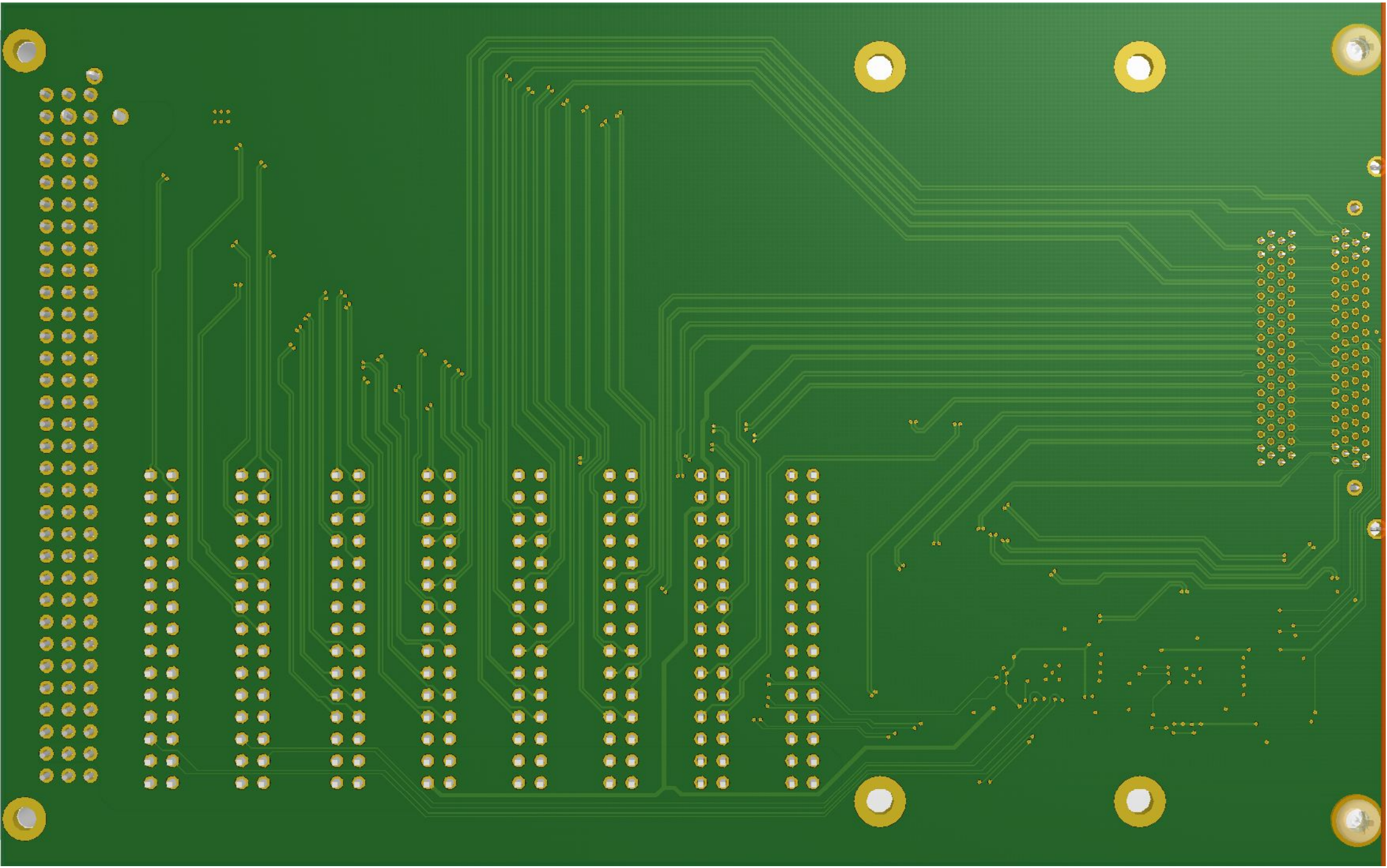
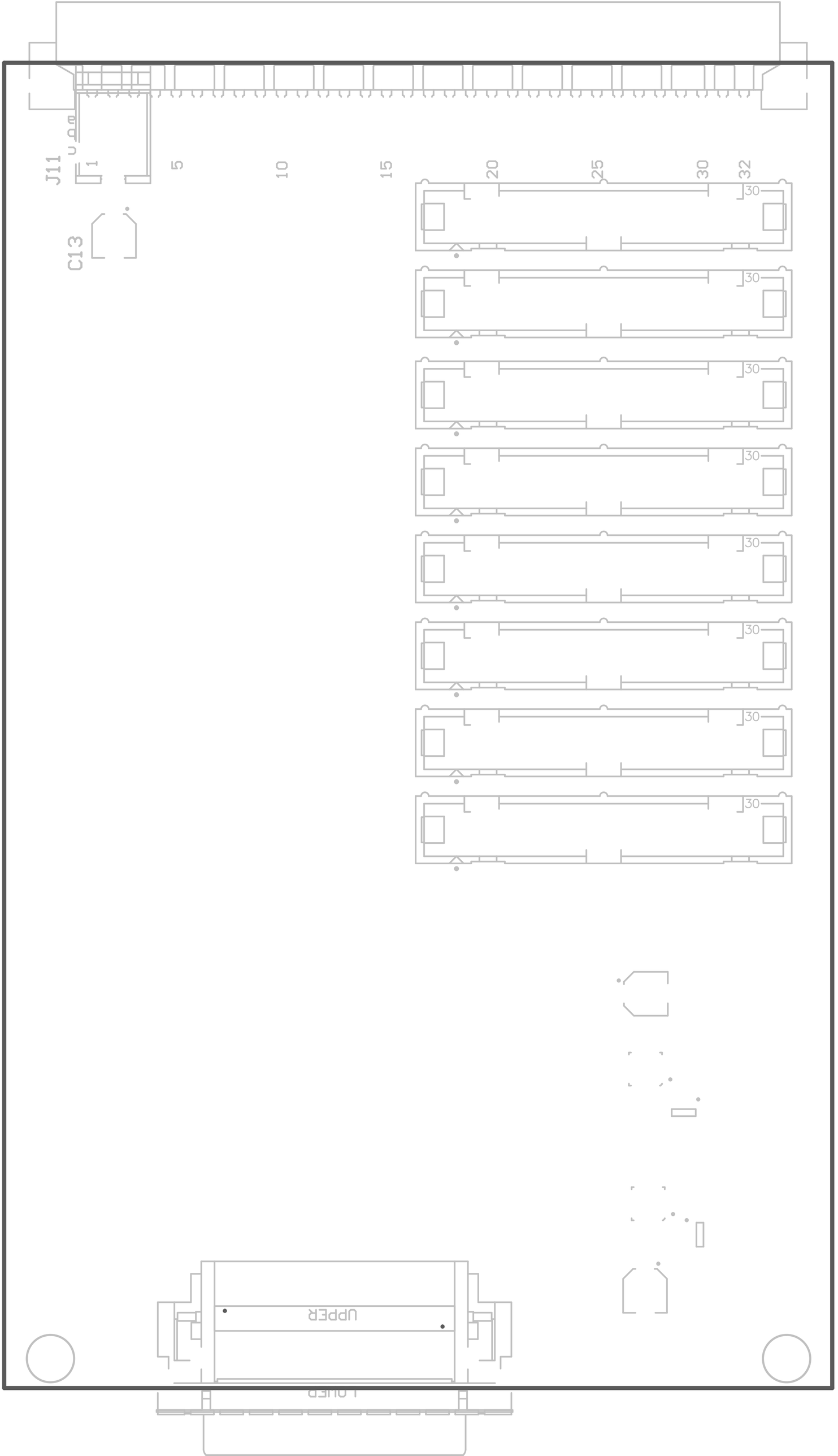

J4A
LVDS1_1_P L1 L35 LVDS1_1_N
LVDS1_2_P L2 L36 LVDS1_2_N
LVDS1_3_P L3 L37 LVDS1_3_N
LVDS1_4_P L4 L38 LVDS1_4_N
LVDS1_5_P L5 L39 LVDS1_5_N
LVDS1_6_P L6 L40 LVDS1_6_N
LVDS1_7_P L7 L41 LVDS1_7_N
LVDS1_8_P L8 L42 LVDS1_8_N
LVDS2_1_P L9 L43 LVDS2_1_N
LVDS2_2_P L10 L44 LVDS2_2_N
LVDS2_3_P L11 L45 LVDS2_3_N
LVDS2_4_P L12 L46 LVDS2_4_N
LVDS2_5_P L13 L47 LVDS2_5_N
LVDS2_6_P L14 L48 LVDS2_6_N
LVDS2_7_P L15 L49 LVDS2_7_N
LVDS2_8_P L16 L50 LVDS2_8_N
VHDCI1_SCL L17 L51 VHDCI1_SDA
L18 L52
LVDS3_1_P L19 L53 LVDS3_1_N
LVDS3_2_P L20 L54 LVDS3_2_N
LVDS3_3_P L21 L55 LVDS3_3_N
LVDS3_4_P L22 L56 LVDS3_4_N
LVDS3_5_P L23 L57 LVDS3_5_N
LVDS3_6_P L24 L58 LVDS3_6_N
LVDS3_7_P L25 L59 LVDS3_7_N
LVDS3_8_P L26 L60 LVDS3_8_N
LVDS4_1_P L27 L61 LVDS4_1_N
LVDS4_2_P L28 L62 LVDS4_2_N
LVDS4_3_P L29 L63 LVDS4_3_N
LVDS4_4_P L30 L64 LVDS4_4_N
LVDS4_5_P L31 L65 LVDS4_5_N
LVDS4_6_P L32 L66 LVDS4_6_N
LVDS4_7_P L33 L67 LVDS4_7_N
LVDS4_8_P L34 L68 LVDS4_8_N
69 70
GND
R44 0
GND
P3V3_MP1
IC1
VHDCI1_SDA 20
VHDCI1_SCL 19
SDA
SCL
RESET 24
A2 18
A1 23
A0 22
SD0 1
SC0 2
SD1 3
SC1 4
SD2 5
SC2 6
SD3 7
SC3 8
SD4 10
SC4 11
SD5 12
SC5 13
SD6 14
SC6 15
SD7 16
SC7 17
VCC 21
GND 9
EP 25
TCA9546ARGER
P3V3_MP1 R1 2k2 R2 2k2
R5 0 R6 0 R8 0
GND
I2C1_SDA 2k2 R3 1%
I2C1_SCL 2k2 R4 1%
I2C2_SDA 2k2 R7 1%
I2C2_SCL 2k2 R9 1%
I2C3_SDA 2k2 R10 1%
I2C3_SCL 2k2 R11 1%
I2C4_SDA 2k2 R12 1%
I2C4_SCL 2k2 R13 1%
P3V3_MP1
IC2
SDA NC 5
SCL
VCC VSS 2
GND
24AA02E48T-I/OT
P3V3_MP1
C1 100nF C2 100nF C3 100nF C4 100nF C5 100nF C6 22uF
GND
J5
J1
J2
J3
J6
J7
J8
J9
GND
P12V0
P3V3_MP1
LVDS1_1_P LVDS1_1_N LVDS1_2_P LVDS1_2_N LVDS1_3_P LVDS1_3_N LVDS1_4_P LVDS1_4_N LVDS1_5_P LVDS1_5_N LVDS1_6_P LVDS1_6_N LVDS1_7_P LVDS1_7_N LVDS1_8_P LVDS1_8_N I2C1_SDA I2C1_SCL
LVDS2_1_P LVDS2_1_N LVDS2_2_P LVDS2_2_N LVDS2_3_P LVDS2_3_N LVDS2_4_P LVDS2_4_N LVDS2_5_P LVDS2_5_N LVDS2_6_P LVDS2_6_N LVDS2_7_P LVDS2_7_N LVDS2_8_P LVDS2_8_N I2C2_SDA I2C2_SCL
LVDS3_1_P LVDS3_1_N LVDS3_2_P LVDS3_2_N LVDS3_3_P LVDS3_3_N LVDS3_4_P LVDS3_4_N LVDS3_5_P LVDS3_5_N LVDS3_6_P LVDS3_6_N LVDS3_7_P LVDS3_7_N LVDS3_8_P LVDS3_8_N I2C3_SDA I2C3_SCL
LVDS4_1_P LVDS4_1_N LVDS4_2_P LVDS4_2_N LVDS4_3_P LVDS4_3_N LVDS4_4_P LVDS4_4_N LVDS4_5_P LVDS4_5_N LVDS4_6_P LVDS4_6_N LVDS4_7_P LVDS4_7_N LVDS4_8_P LVDS4_8_N I2C4_SDA I2C4_SCL
Interfaces with Metlino/Kasli ecosystem extension boards
all diff lines are bidir LVDS, 1.8V
I2C is LVCMOS, 3.3V
P3V3 is management power, up to 20mA
J4B
LVDS5_1_P U1 U35 LVDS5_1_N
LVDS5_2_P U2 U36 LVDS5_2_N
LVDS5_3_P U3 U37 LVDS5_3_N
LVDS5_4_P U4 U38 LVDS5_4_N
LVDS5_5_P U5 U39 LVDS5_5_N
LVDS5_6_P U6 U40 LVDS5_6_N
LVDS5_7_P U7 U41 LVDS5_7_N
LVDS5_8_P U8 U42 LVDS5_8_N
LVDS6_1_P U9 U43 LVDS6_1_N
LVDS6_2_P U10 U44 LVDS6_2_N
LVDS6_3_P U11 U45 LVDS6_3_N
LVDS6_4_P U12 U46 LVDS6_4_N
LVDS6_5_P U13 U47 LVDS6_5_N
LVDS6_6_P U14 U48 LVDS6_6_N
LVDS6_7_P U15 U49 LVDS6_7_N
LVDS6_8_P U16 U50 LVDS6_8_N
VHDCI2_SCL U17 U51 VHDCI2_SDA
U18 U52
LVDS7_1_P U19 U53 LVDS7_1_N
LVDS7_2_P U20 U54 LVDS7_2_N
LVDS7_3_P U21 U55 LVDS7_3_N
LVDS7_4_P U22 U56 LVDS7_4_N
LVDS7_5_P U23 U57 LVDS7_5_N
LVDS7_6_P U24 U58 LVDS7_6_N
LVDS7_7_P U25 U59 LVDS7_7_N
LVDS7_8_P U26 U60 LVDS7_8_N
LVDS8_1_P U27 U61 LVDS8_1_N
LVDS8_2_P U28 U62 LVDS8_2_N
LVDS8_3_P U29 U63 LVDS8_3_N
LVDS8_4_P U30 U64 LVDS8_4_N
LVDS8_5_P U31 U65 LVDS8_5_N
LVDS8_6_P U32 U66 LVDS8_6_N
LVDS8_7_P U33 U67 LVDS8_7_N
LVDS8_8_P U34 U68 LVDS8_8_N
71 72
GND
R28 0
P3V3_MP2
IC3
VHDCI2_SDA 20
VHDCI2_SCL 19
SDA
SCL
RESET 24
A2 18
A1 23
A0 22
SD0 1
SC0 2
SD1 3
SC1 4
SD2 5
SC2 6
SD3 7
SC3 8
SD4 10
SC4 11
SD5 12
SC5 13
SD6 14
SC6 15
SD7 16
SC7 17
VCC 21
GND 9
EP 25
TCA9546ARGER
P3V3_MP2 R45 2k2 R46 2k2
R49 0 R50 0 R22 0
GND
I2C5_SDA 2k2 R47 1%
I2C5_SCL 2k2 R48 1%
I2C6_SDA 2k2 R21 1%
I2C6_SCL 2k2 R23 1%
I2C7_SDA 2k2 R24 1%
I2C7_SCL 2k2 R25 1%
I2C8_SDA 2k2 R26 1%
I2C8_SCL 2k2 R27 1%
P3V3_MP2
IC4
SDA NC 5
SCL
VCC VSS 2
GND
24AA02E48T-I/OT
P3V3_MP2
C7 100nF C8 100nF C9 100nF C40 100nF C41 100nF C42 22uF
GND
J10A
J10B
J10C
GND
P12V0
P5V0
5V/GND pinout is compatible with VME backplanes
Interfaces with not yet defined backplane, can be inserted and supplied from standard VME backplane
5V, up to 2A
Interfaces with Sinara / Metlino
all diff lines are bidir LVDS, 1.8V
I2C is LVCMOS, 3.3V
P3V3 is management power, up to 100mA
DC jack is assembled instead of DIN connector
J11
P12V0
C43 22nF
GND
Project/Equipment ARTIQ
Document
Metlino VHDCI Base board
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 20.12.2016
File PCB_3U_VHDCI_Baseboard.schdoc
Print Date 21.12.2016 16:33:01 Sheet - of -
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19
ARTIQ
Size A3 Rev -


C13
J11
5
10
15
20
32




J11
1
5
10
15
20
25
30
32
C13
30
30
30
30
30
30
30
30
UPPER
LOWER