

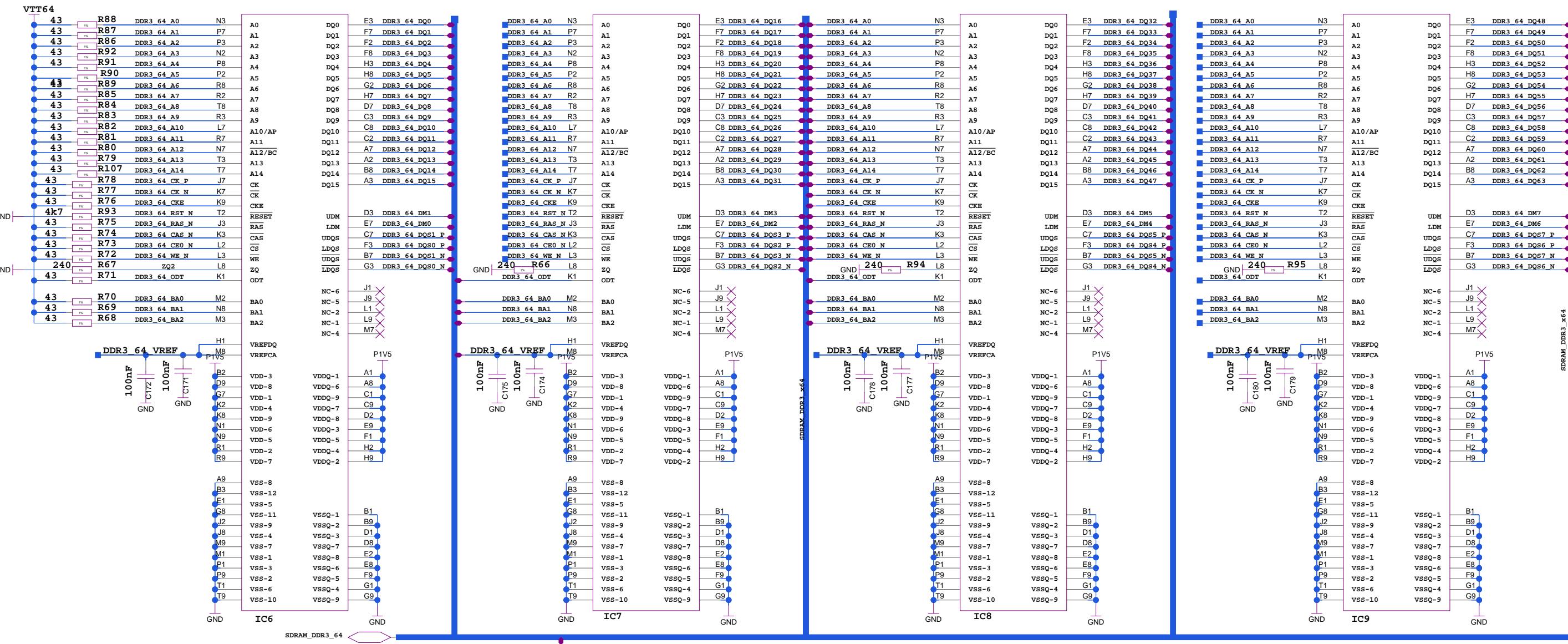
Metlino_MCH

ARTIQ Sinara

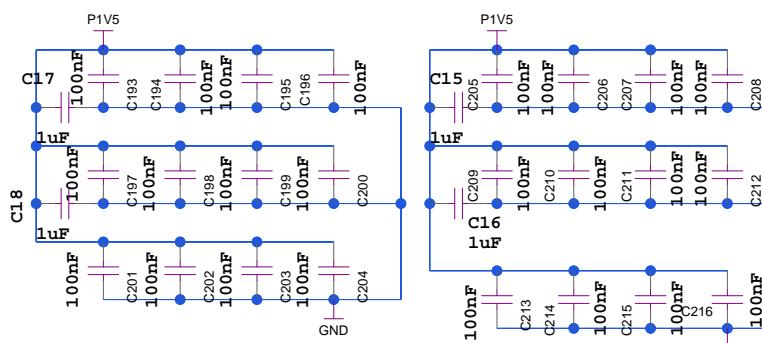
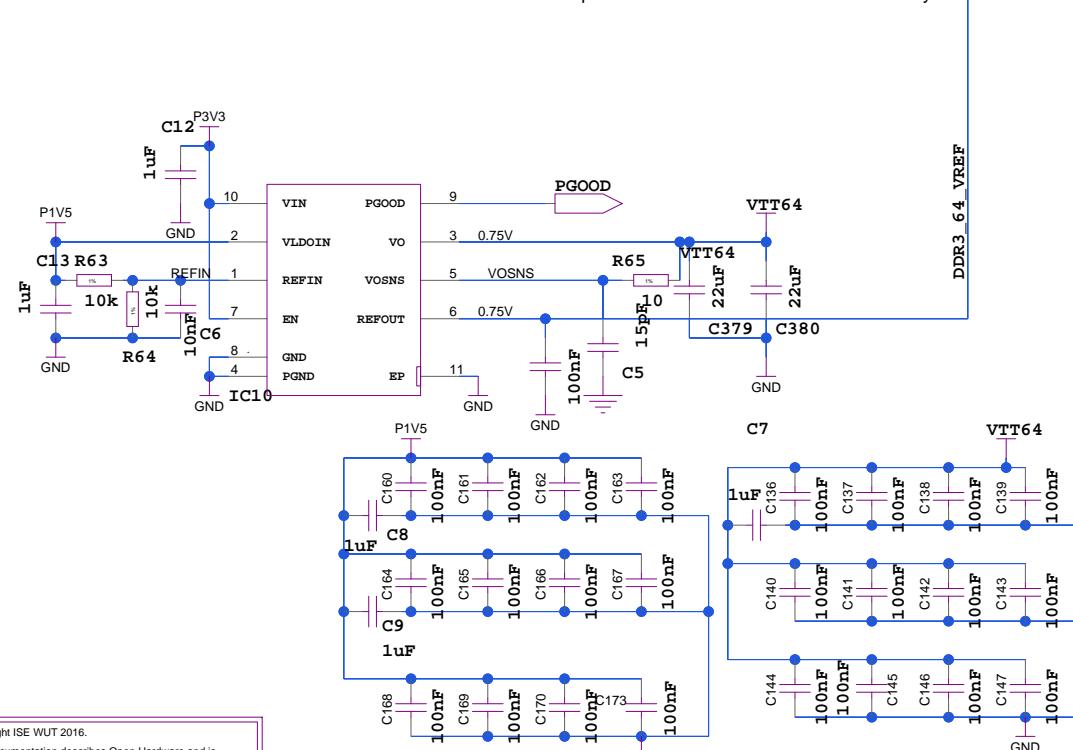
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1M ESDSTRIP1 1M ESDSTRIP2

TITLE
SIZE DWG NO
A3 1 REV v0.95
DRAWN BY G.K. SHEET 1 of 28
07/01/2017:17:07



All capacitors without values are 100nF 0201 by default



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SDRAM DDR3 4x16

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G

SIZE

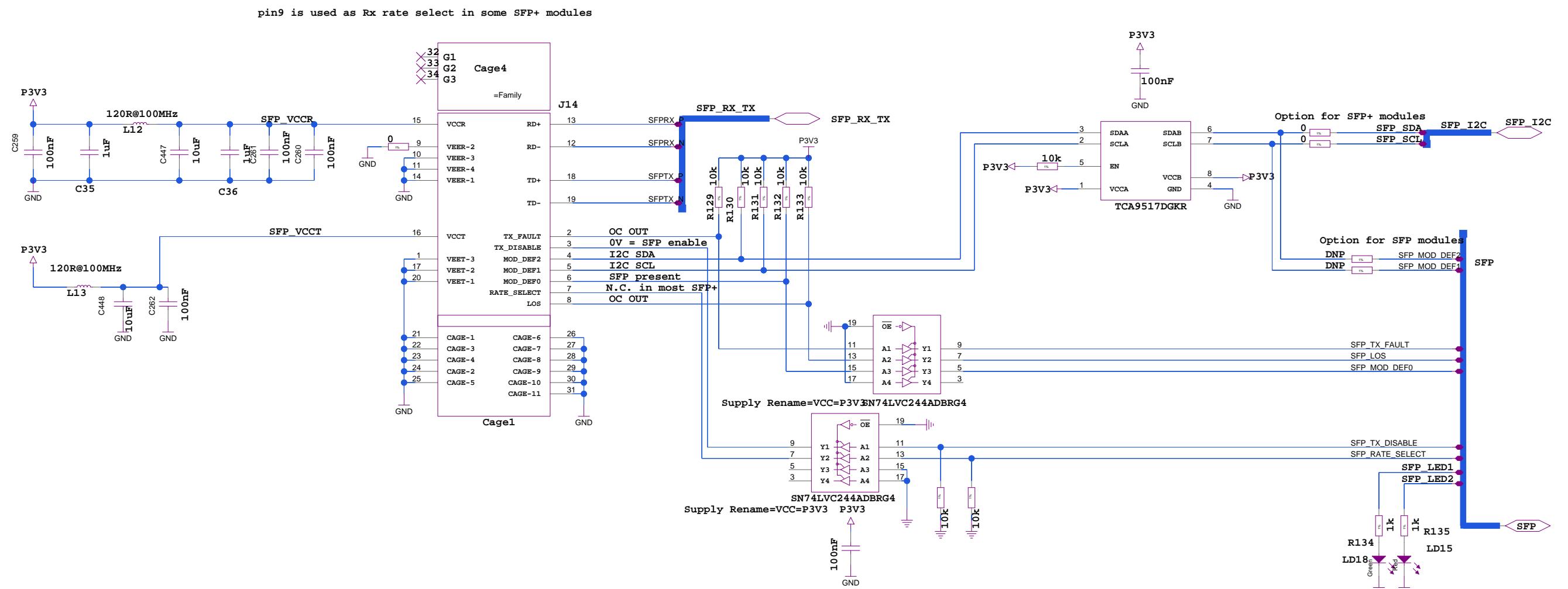
DRAWN BY

REV

8

5-12

20/12/2010.10.15

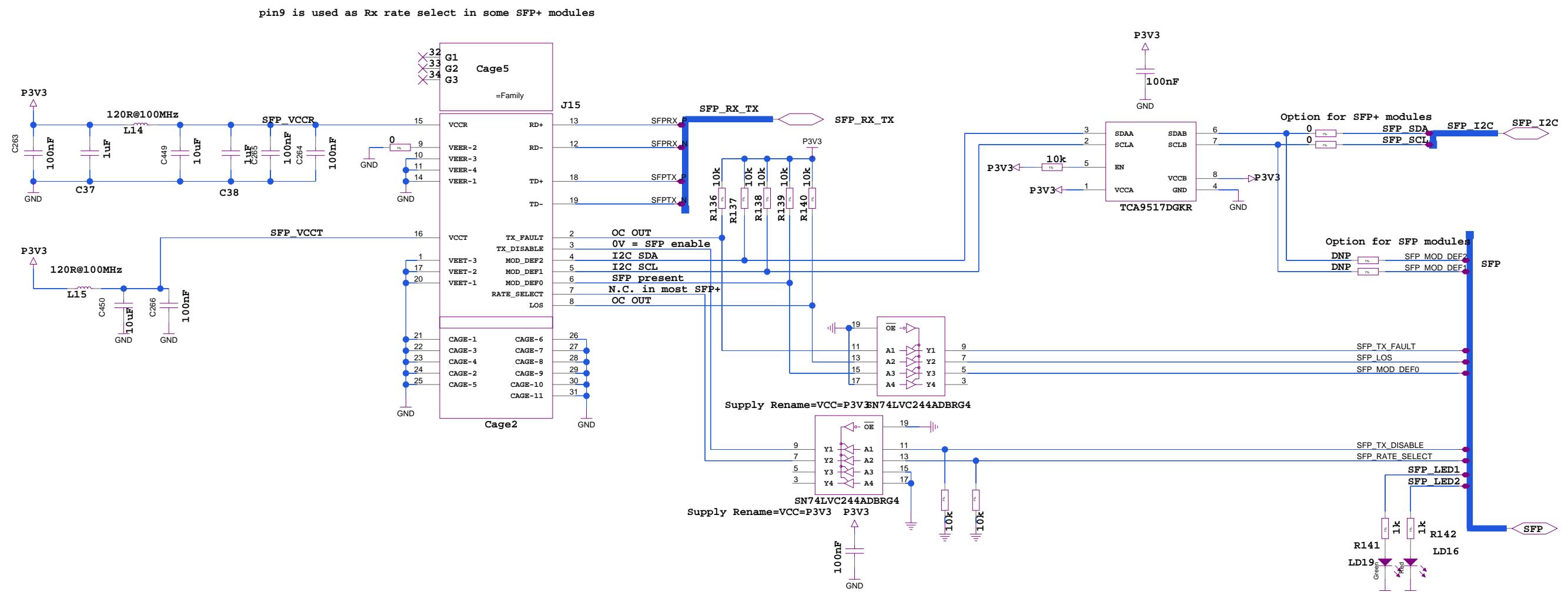


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SFP

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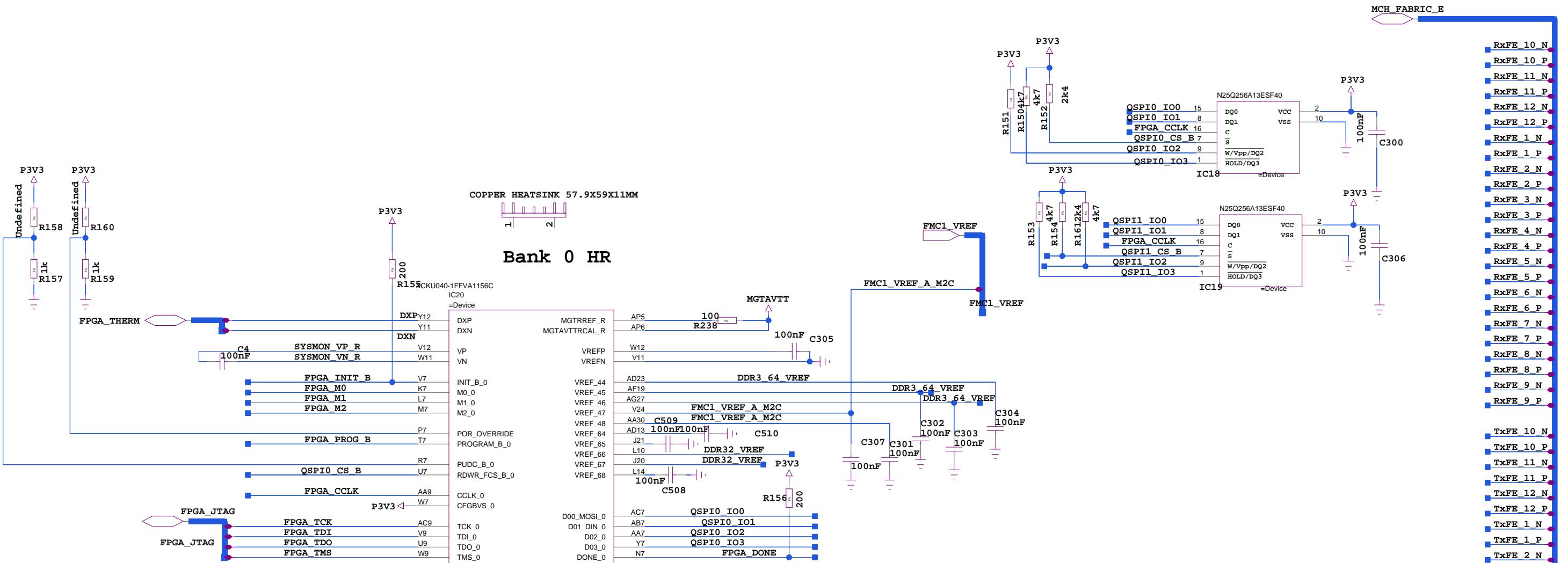
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SFP				
SIZE	DWG NO	SFP		REV
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G.K.		3	28	



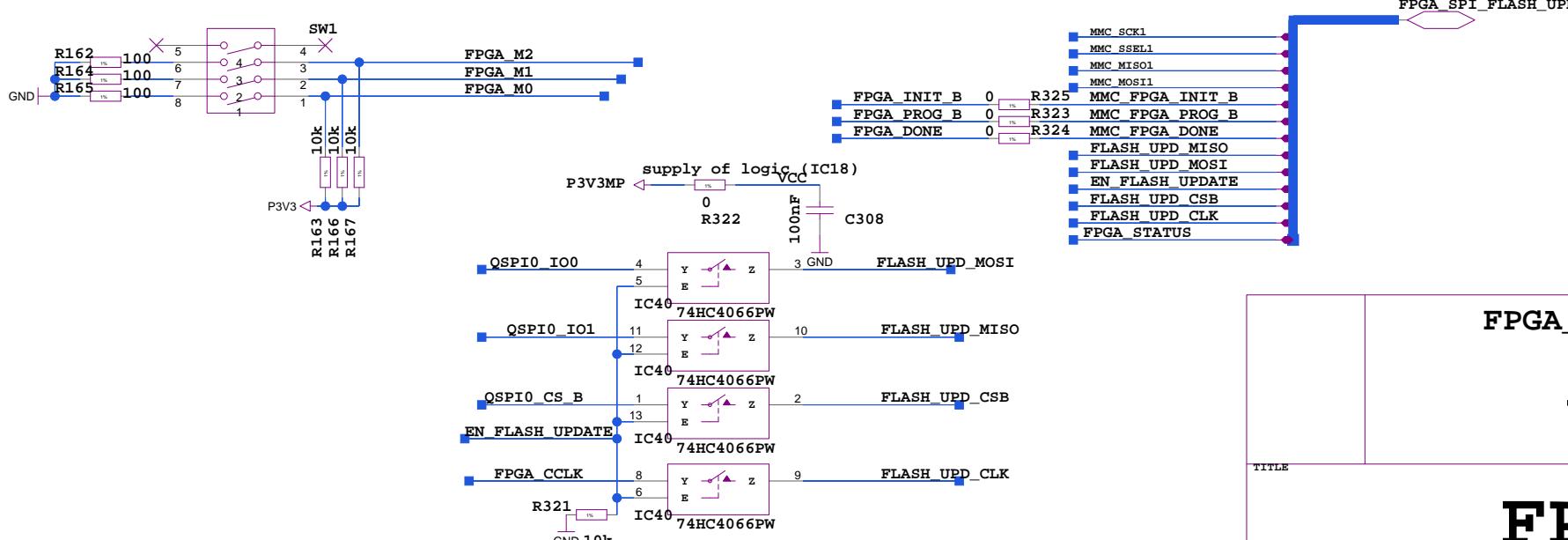
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SIZE A3 DWG NO _____
DRAWN BY G.K. SHEET 4 of 28 REV v0.95
SFP 08/01/2017:00:18



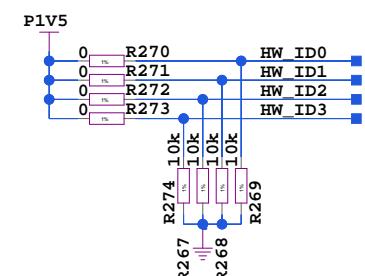
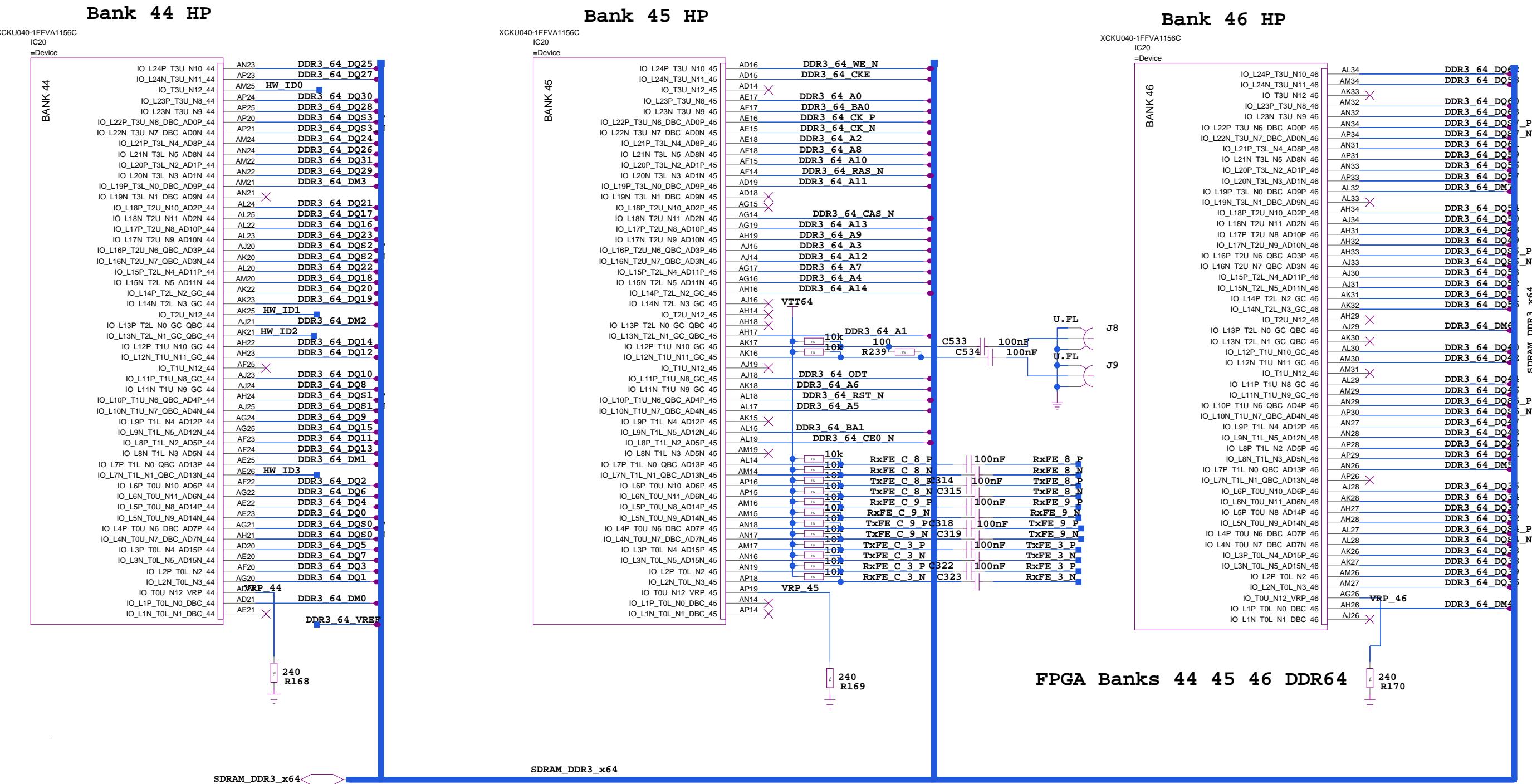
Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via



FPGA_XCKU040FFVA1156_MCH ARTIQ Sinara

FPGA Bank 0 CFG

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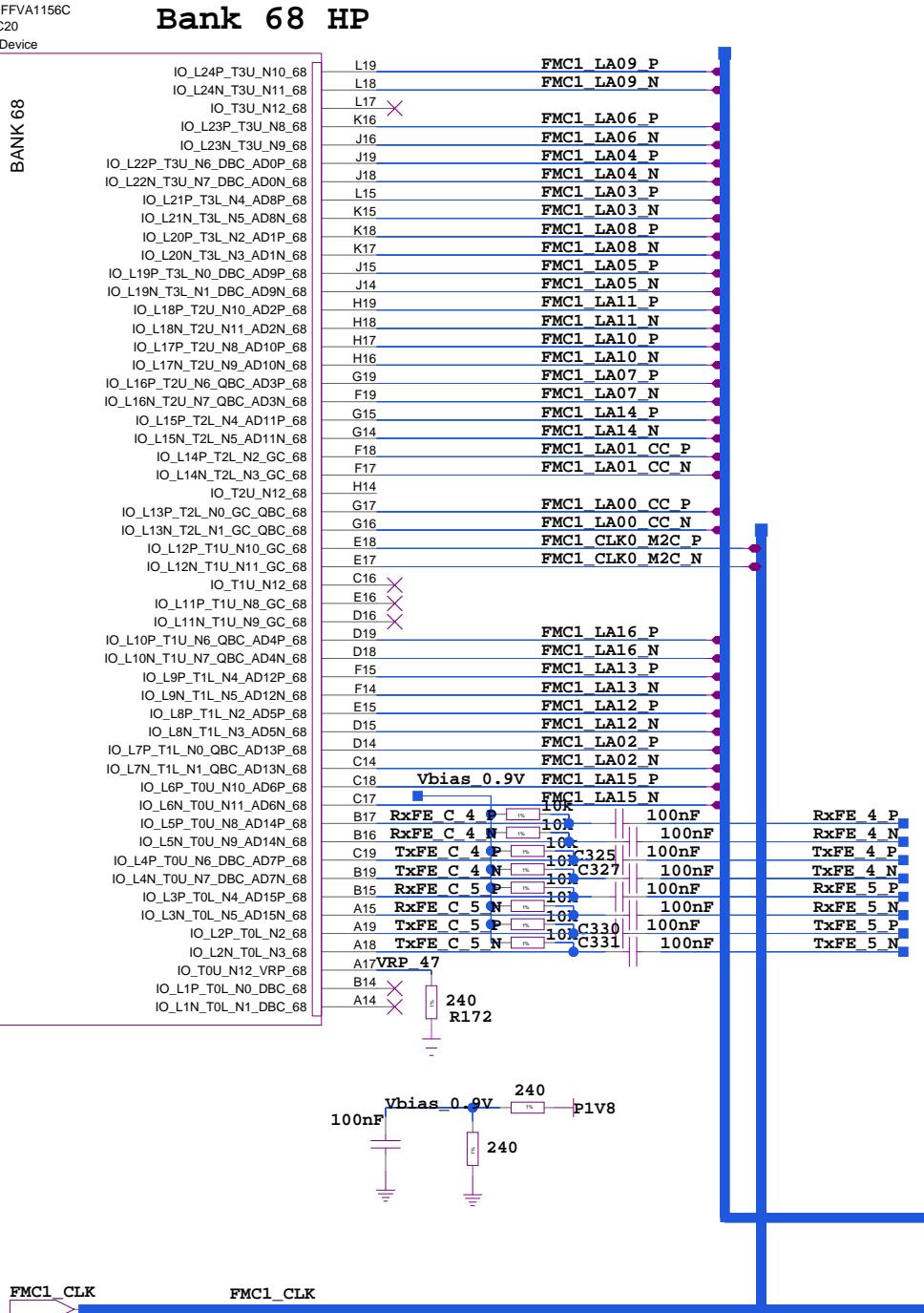


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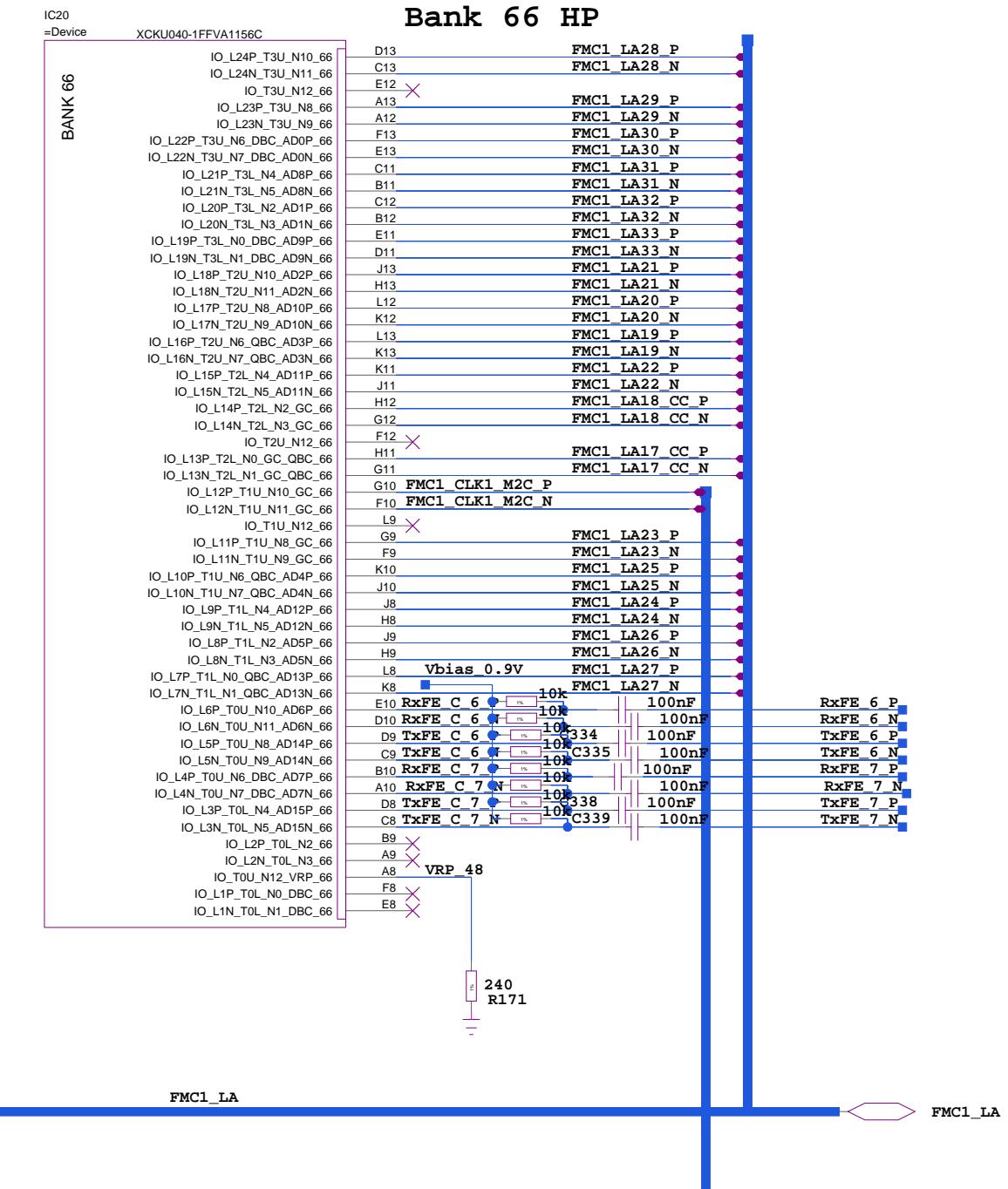
ARTIQ Sinara

A Banks 44 45 46 DDR

XCKU040-1FFVA1156C
IC20
=Device



XCKU040-1FFVA1156C
IC20
=Device

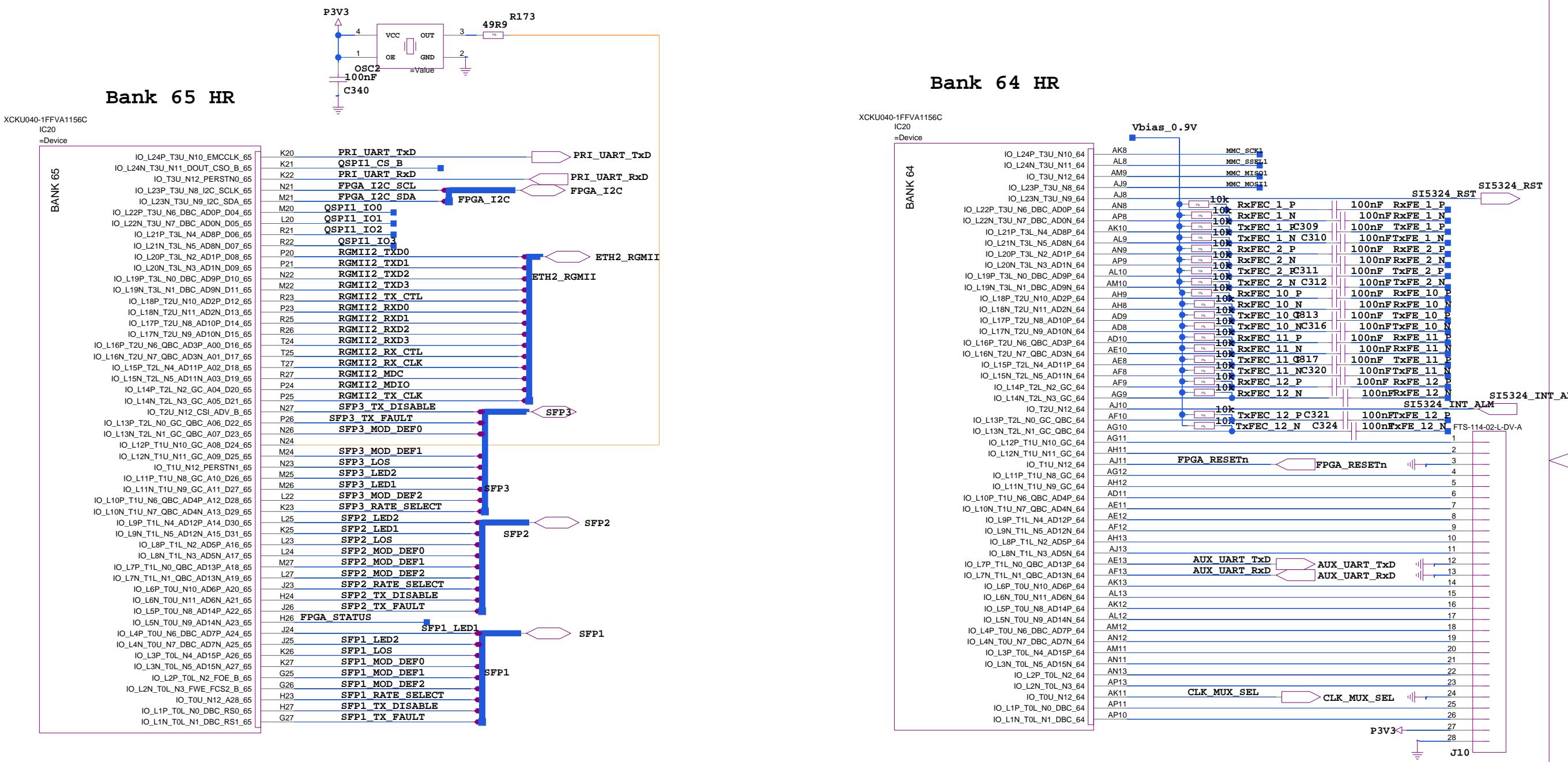


FPGA_XCKU040FFVA1156_MCH

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ARTIQ Sinara
FPGA Banks 47 48 HP FM
A3
G.K. 7 28 06/01/2017:12:48
v0.95



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FPGA Banks 64 65 HR

SIZE A3

DWG NO

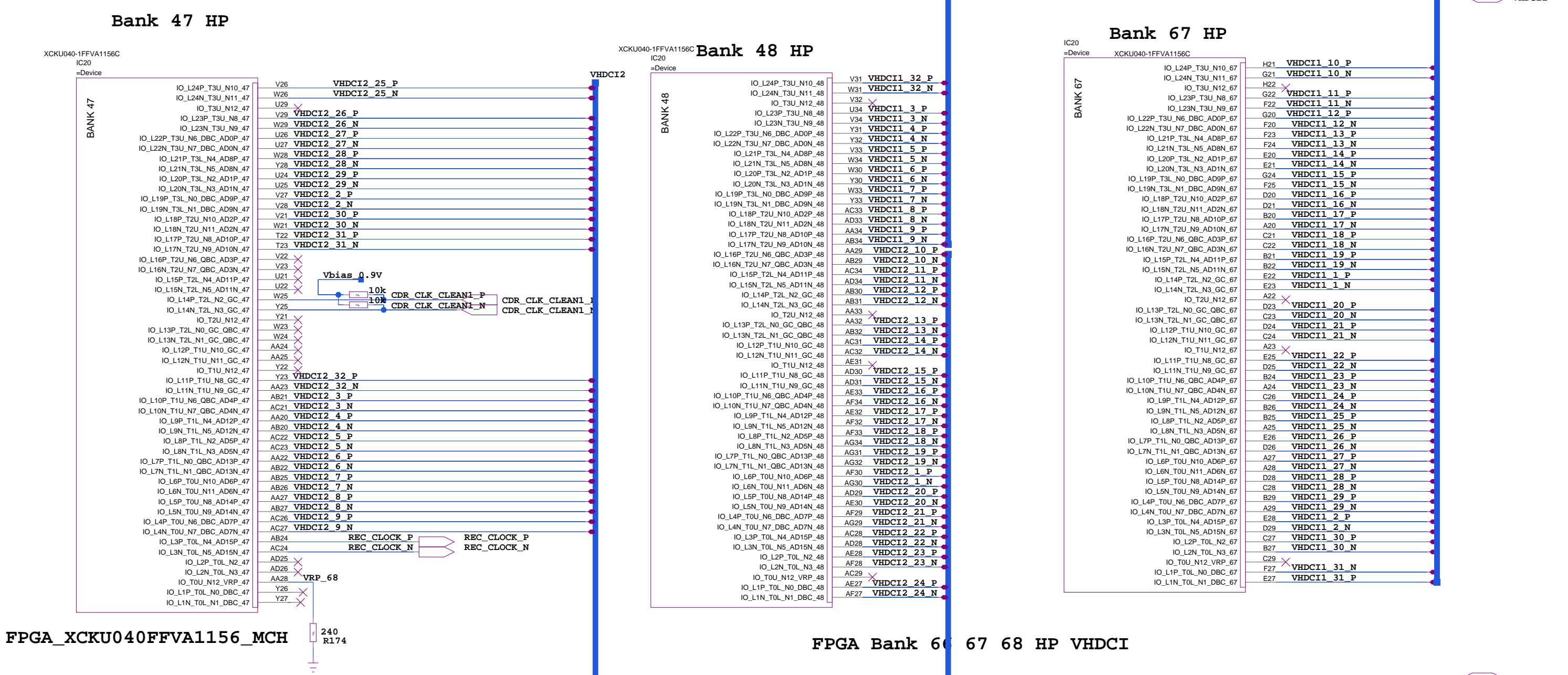
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DRAWN BY G.K.

SHEET 8

of 28

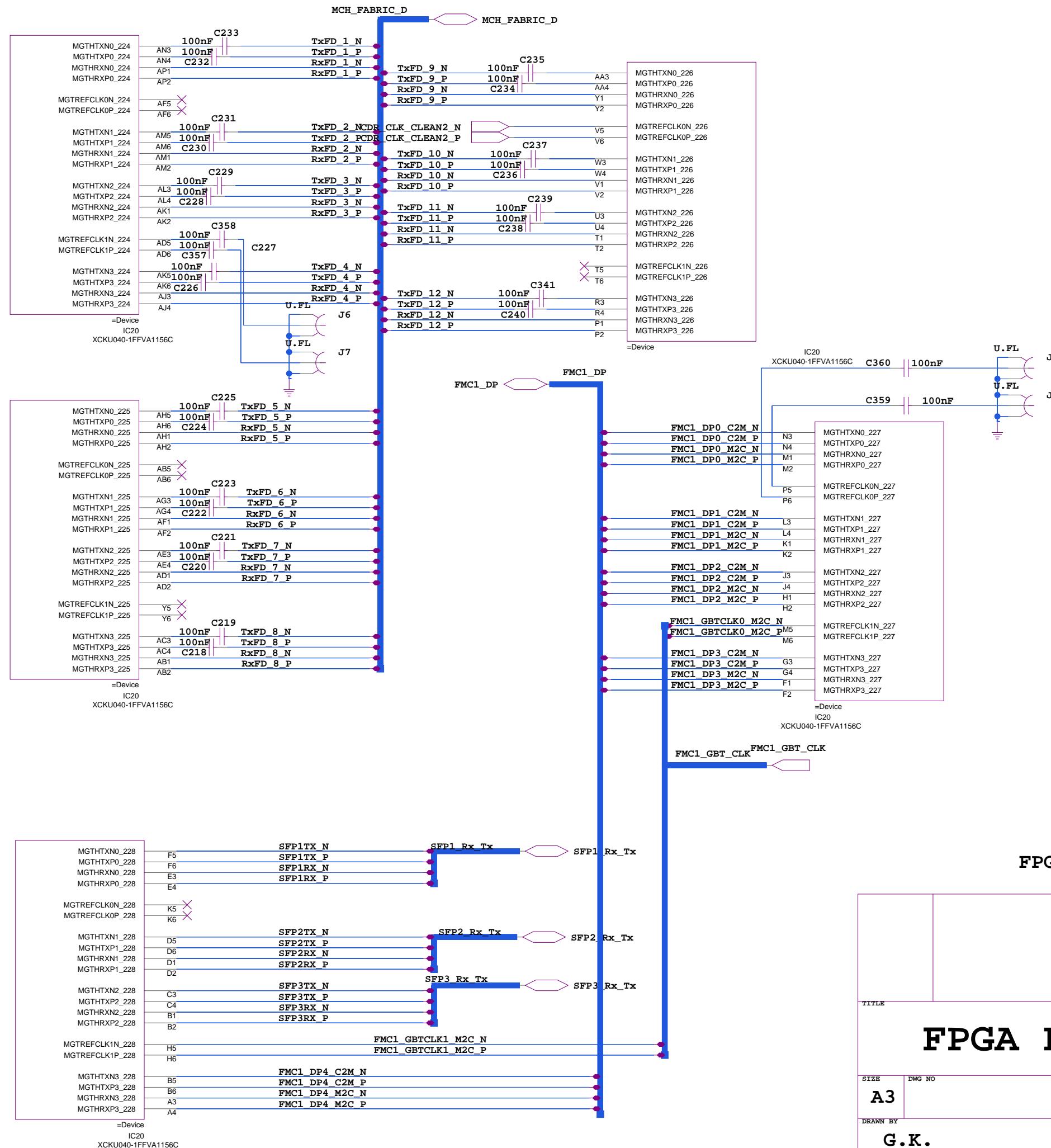
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FPGA Bank 66 67 68

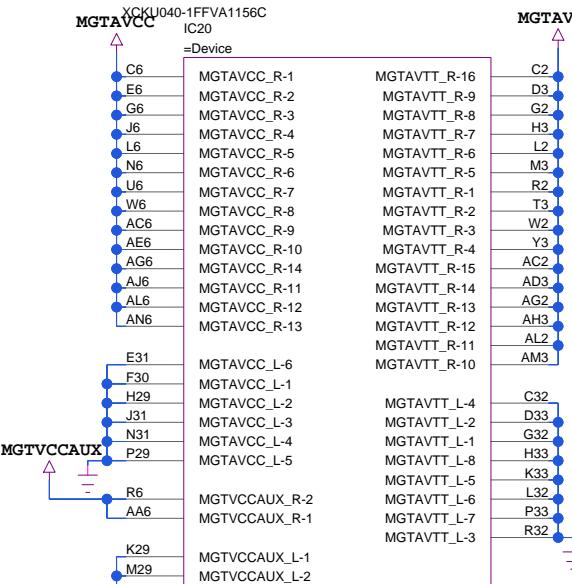
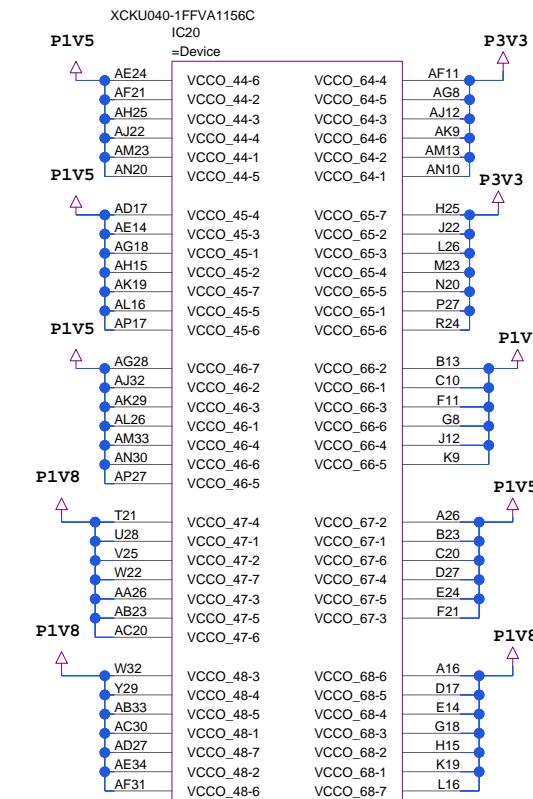
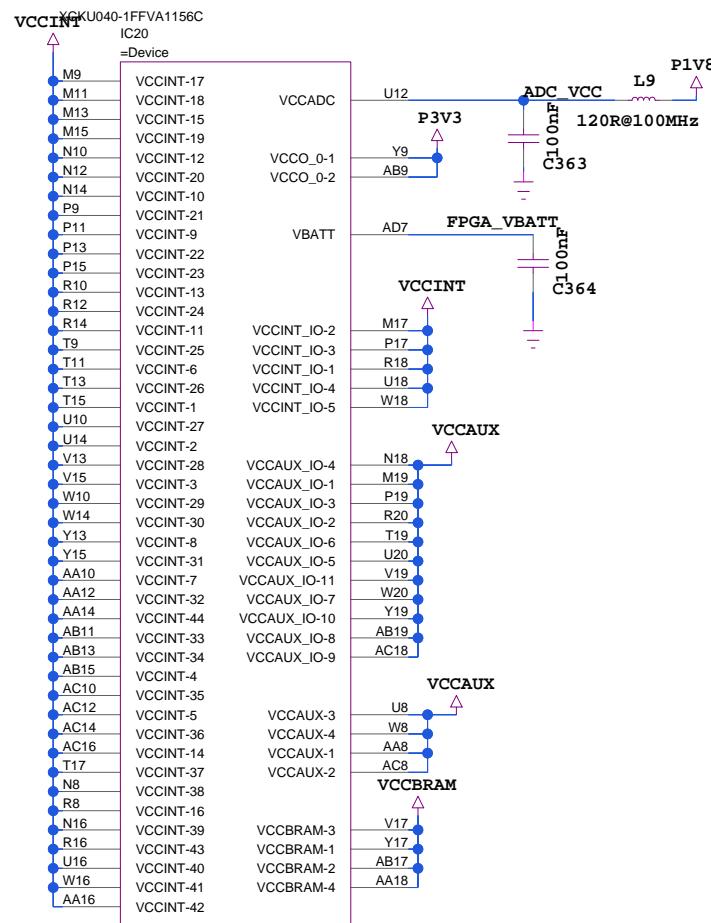
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FPGA_XCKU040FFVA1156_MCH

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TITLE	
SIZE	DWG NO
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SHEET 10 of 28	
21/12/2016:23:49	



FPGA Power

FPGA_XCKU040FFVA1156_MCH

ARTIQ Sinara

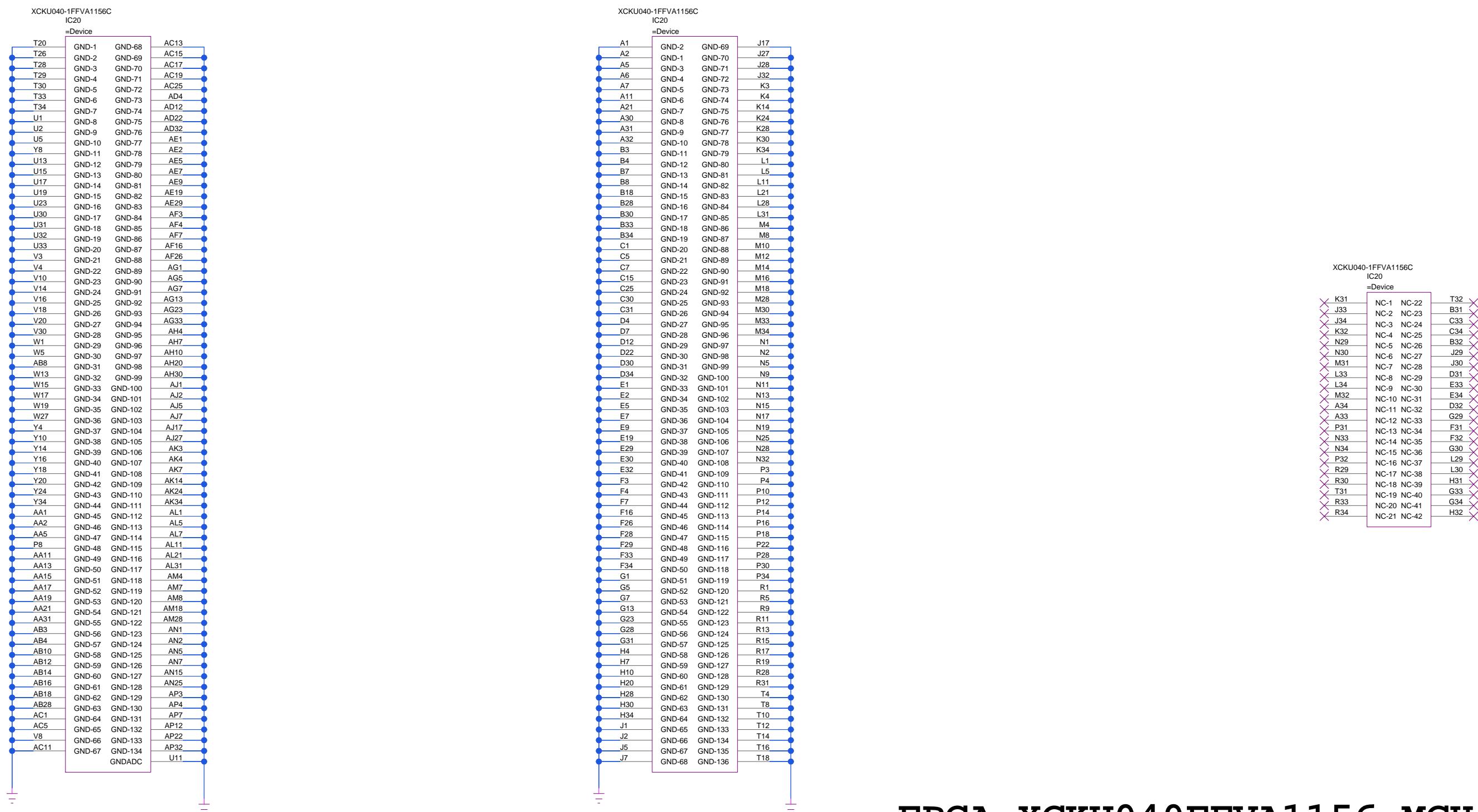
FPGA Power

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REV v0.95

22/12/2016:21:57



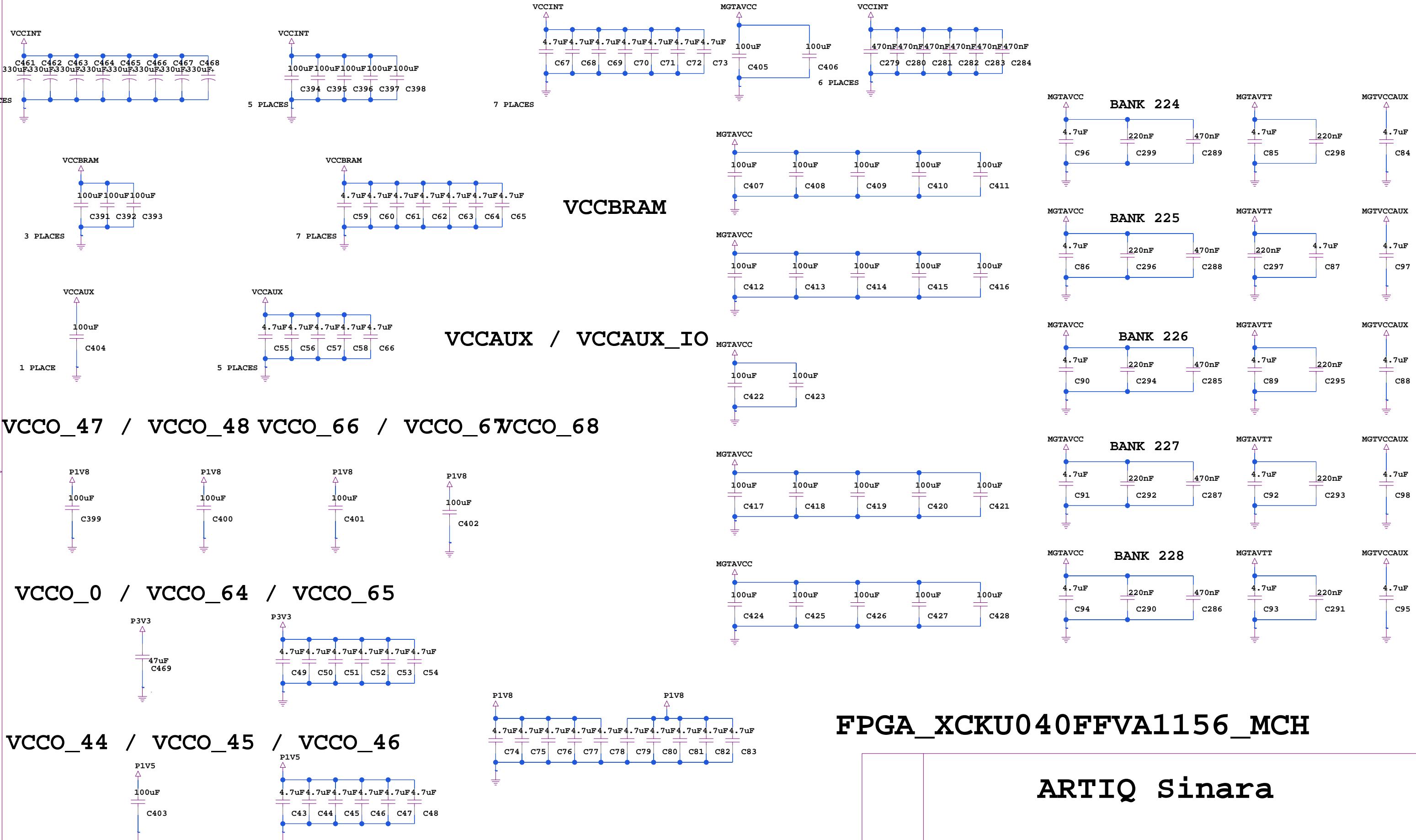
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ARTIQ Sinara

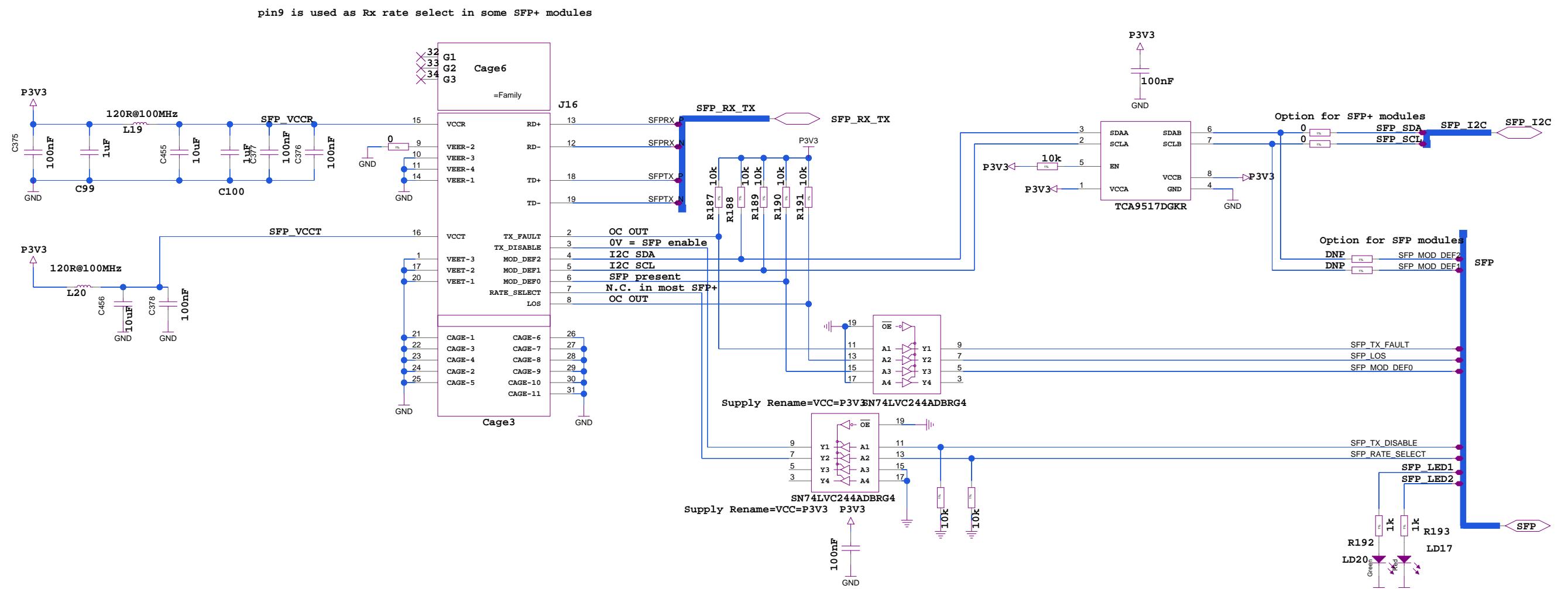
FPGA GND NC

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G.K.		12	28
REV v0.95			
21/12/2016:23:35			

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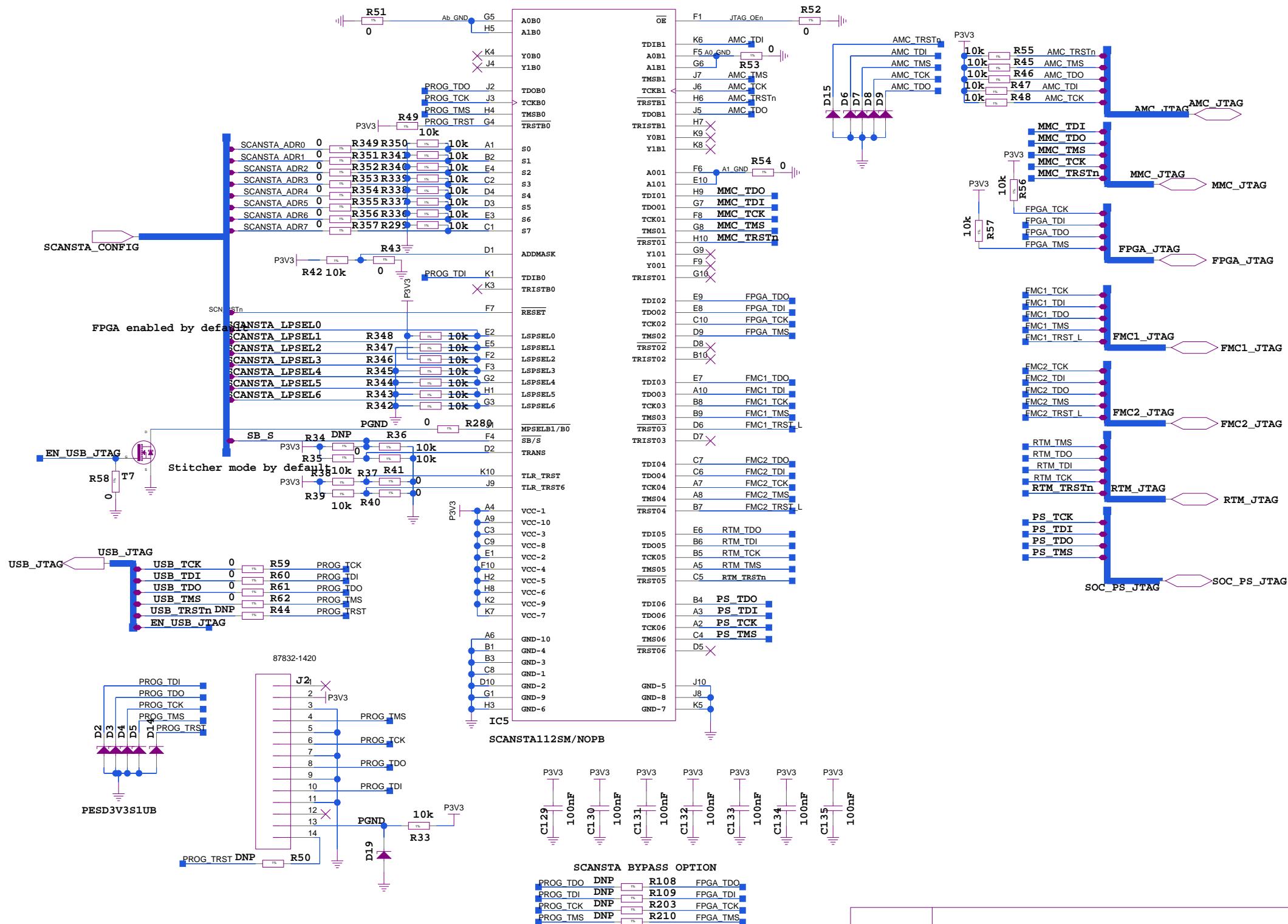


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SFP

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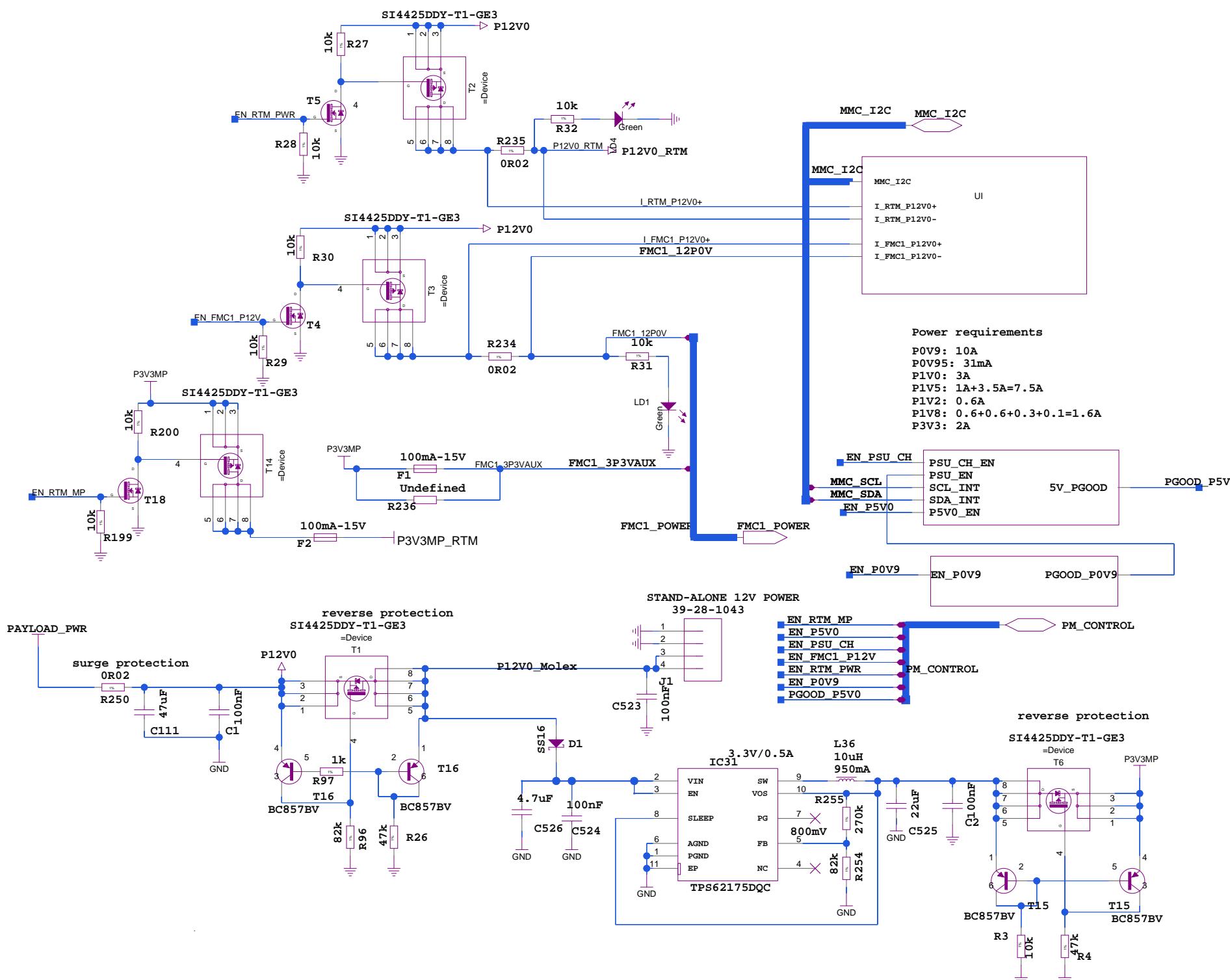
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SIZE	DWG NO	REV	v0.95
A3	SHEET 14	OF 28	08/01/2017:00:18
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JTAG Configuration

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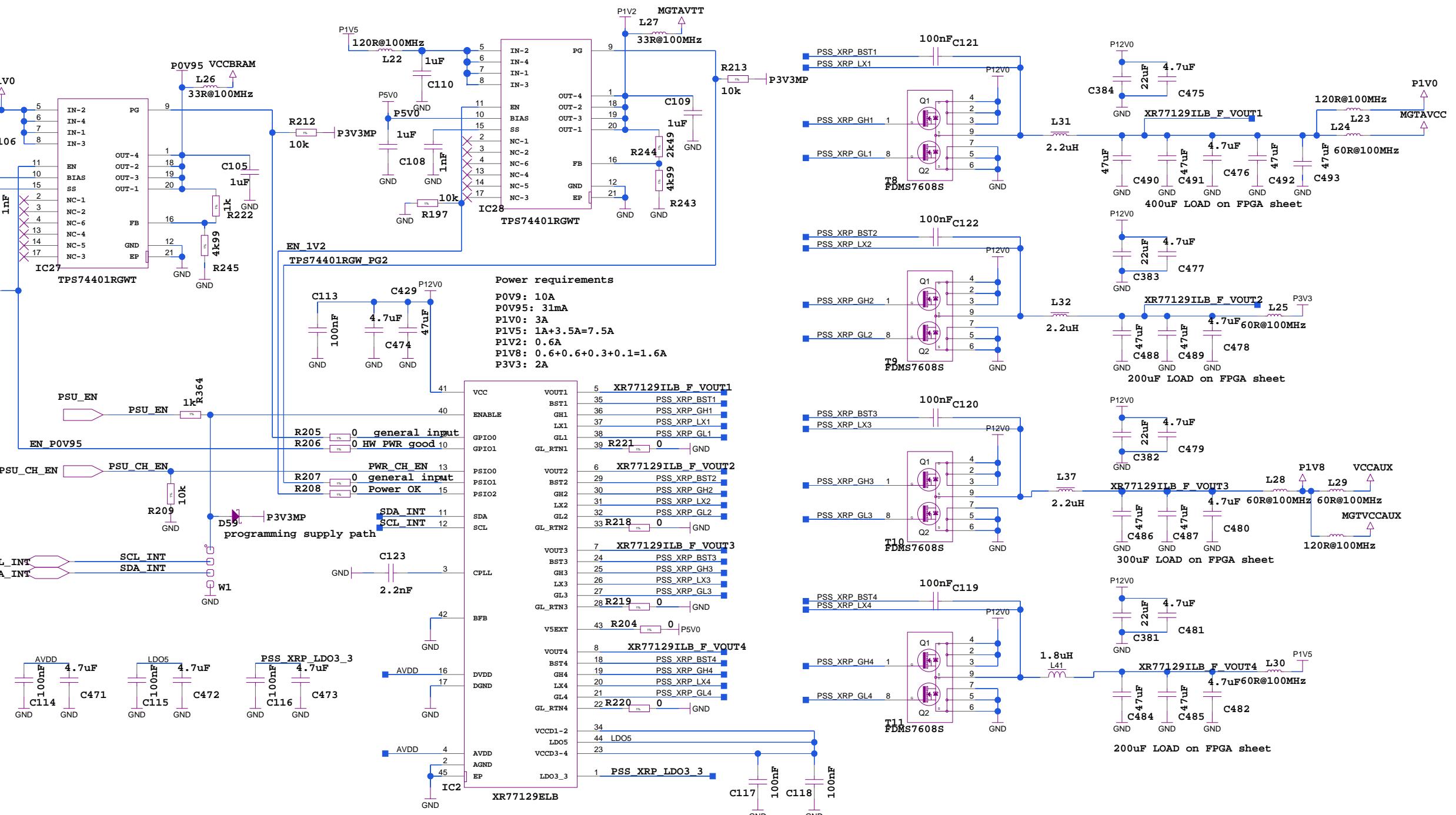
Power Supply		
Source	Voltage	Total (A)
V _{CCINT}	0.900	9.165
V _{CCINT_IO}	0.900	0.620
V _{CCBRAM}	0.950	0.031
V _{CCAUX}	1.800	0.660
V _{CCAUX_IO}	1.800	0.546
V _{CCO 3.3V}	3.300	0.000
V _{CCO 2.5V}	2.500	
V _{CCO 1.8V}	1.800	0.380
V _{CCO 1.5V}	1.500	0.936
V _{CCO 1.35V}	1.350	
V _{CCO 1.2V}	1.200	
V _{CCO 1.0V}	1.000	
MGT _{VCCAUX}	1.800	0.081
MGT _{AV_{CC}}	1.000	3.038
MGT _{AV_{TT}}	1.200	0.592
-	-	
-	-	
V _{CCADC}	1.800	0.014

The recommended power-on sequence is VCCINT/VCCINT_IO, VCCBRAM, VCCAUX/VCCAUX_IO, and VCCO to achieve minimum current draw and ensure that the 1/0s are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCINT/VCCINT_IO and VCCO have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. If VCCAUX/VCCAUX_IO and VCCO have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. VCCAUX and VCCO must be connected together. When the current minimums are met, the device powers on after the VCCINT/VCCINT_IO, VCCBRAM, VCCAUX/VCCAUX_IO, and VCCO supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after VCCINT is applied. VCCADC and VREF can be powered at any time and have no power-up sequencing recommendations. The recommended power-on sequence to achieve minimum current draw for the GTH or GT_T transceivers is VCCINT, VMGTA_{VCC}, VMGTA_{VIT} OR VMGTA_{VCC}, VCCINT, VMGTA_{VTT}. There is no recommended sequencing for VMGTA_{VCC}, VMGTA_{VIT}, VMGTA_{VTT}, VCCINT, and VCCADC simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from VMGTA_{VTT} can be higher than specifications during power-up and power-down.

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POWER_Management

Power Supply		
Source	Voltage	Total (A)
VCCINT	0.800	9.165
VCCINTIO	0.900	0.620
VCCBRAM	0.950	0.031
VCCAUX	1.800	0.660
VCCAUXIO	1.800	0.546
VCCO 3.3V	3.300	0.000
VCCO 2.5V	2.500	
VCCO 1.8V	1.800	0.380
VCCO 1.5V	1.500	0.936
VCCO 1.35V	1.350	
VCCO 1.2V	1.200	
Vcc 1.0V	1.000	
MGTVCAX	1.800	0.081
MGTAVCC	1.000	3.038
MGTAVTT	1.200	0.592
-	-	
VCCADC	1.800	0.014

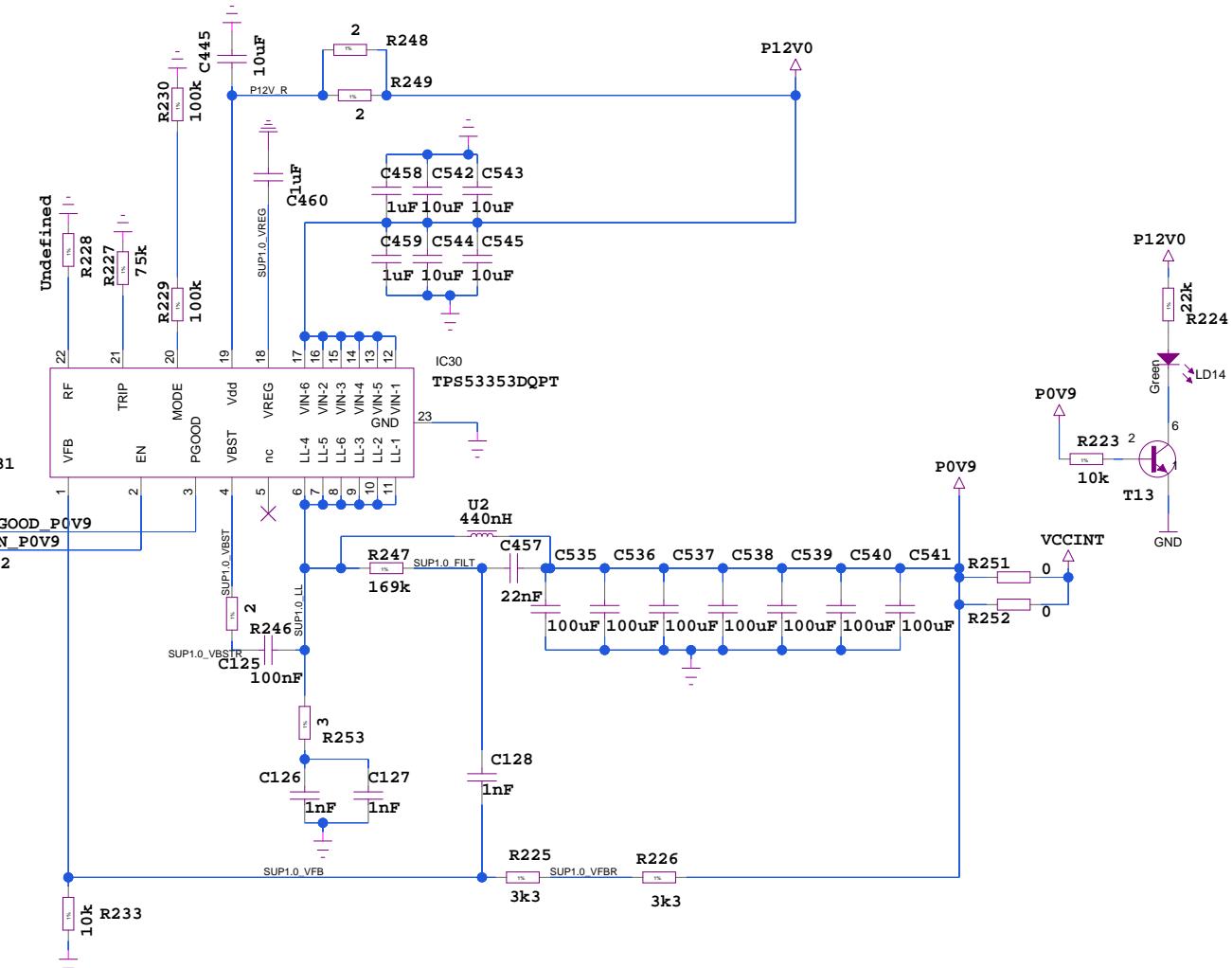
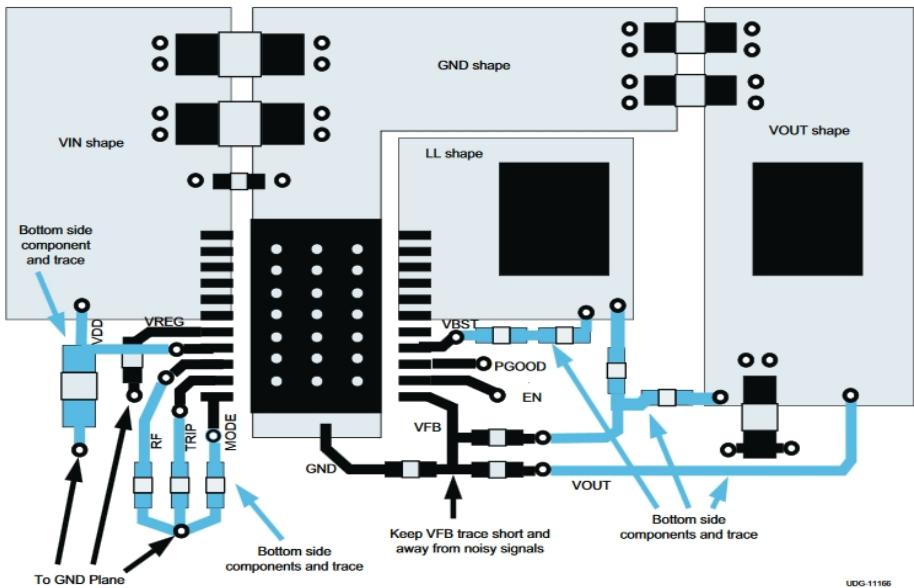


The recommended power-on sequence is VCCINT/VCCINTIO, VCCBRAM, VCCAUX/VCCAUXIO, to achieve minimum current draw and ensure that the I/Os are 3-stated at power-up. Sequence is the reverse of the power-on sequence. I/Os and VCCAUX must have the same recommended voltage levels. They can be powered by the same supply and VCCIN1/IO must be connected to VCCINT. Both VCCINT and VCCAUX must be connected together. When the current minimums are met, the device power-up sequence must have VCCBRAM, VCCAUX/VCCAUXIO, and VCCO. Power-up sequence threshold voltages must be configured until after VCCINT is applied. VCCADC and VREF can be powered up simultaneously. There is no recommended sequencing for VMGTVCAX or VMGTAVTT. Both VMGTAVC and VCCIN can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence. The recommended sequencing for the power-off sequence is not recommended. Current drawn from VMGTAVTT can be higher than specifications during power-up and power-down.

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PWR_DC_DC_EXAR

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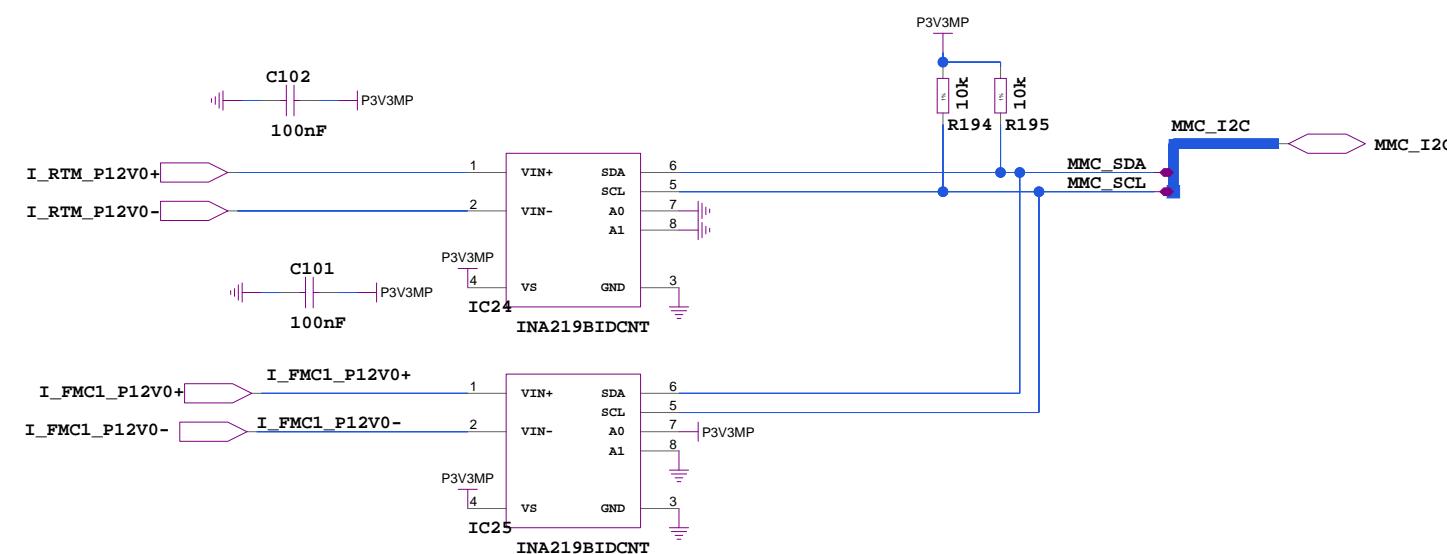


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PWR_0V9

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REV			

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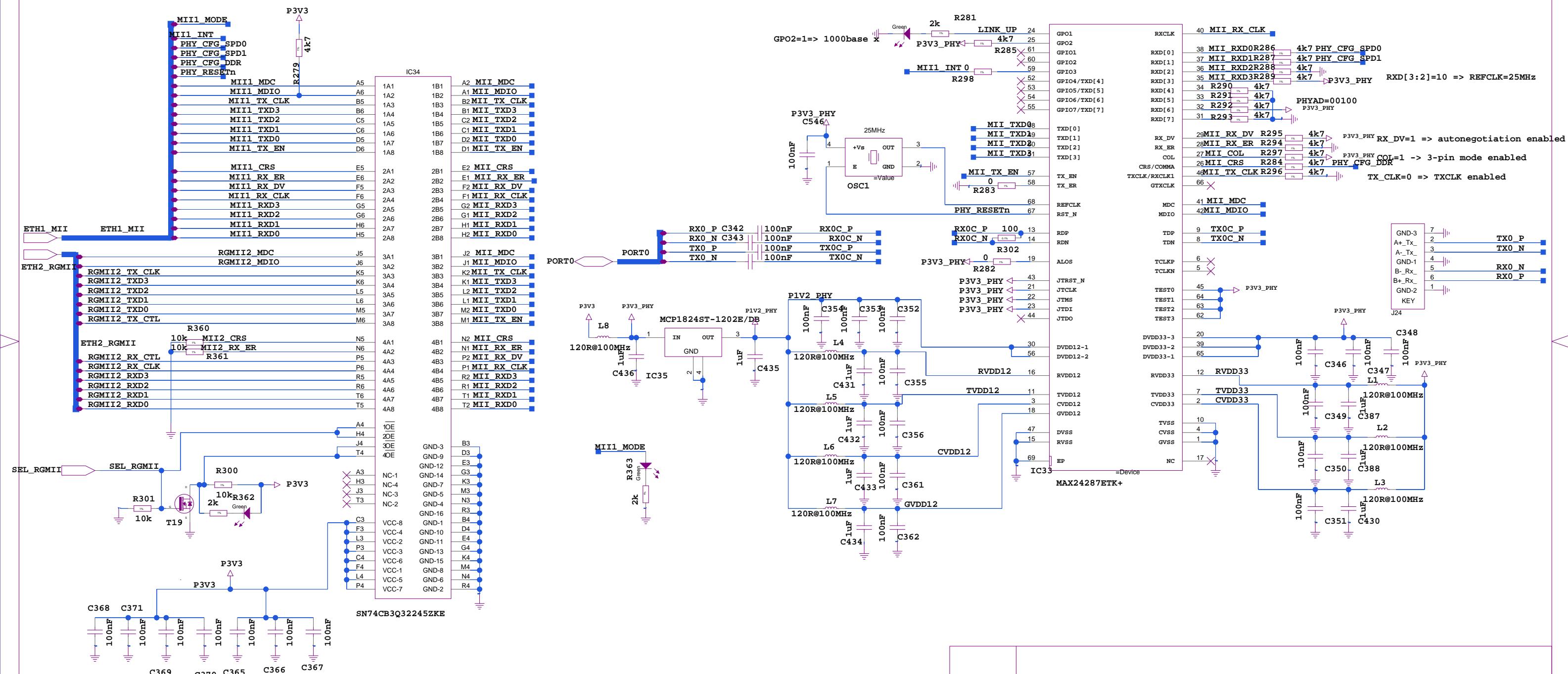
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UI mon

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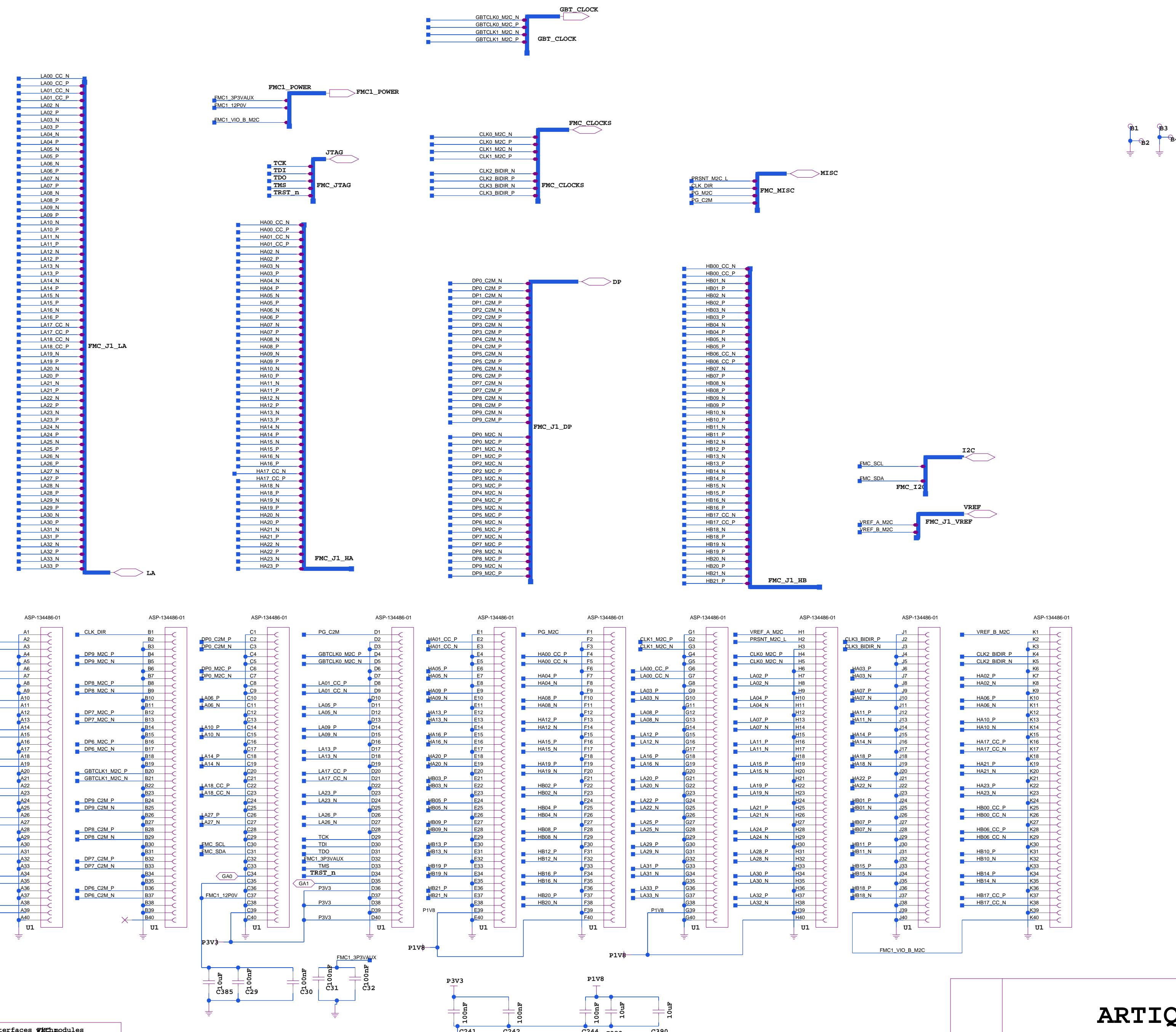
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SIZE	DWG NO	1	REV v0.95
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DRAWN BY G.K.	SHEET 19	of 28	22/12/2016:00:31

We want to have:
 SPD[1:0] DDR
 01 0 in MII
 10 1 in RGMII-1000



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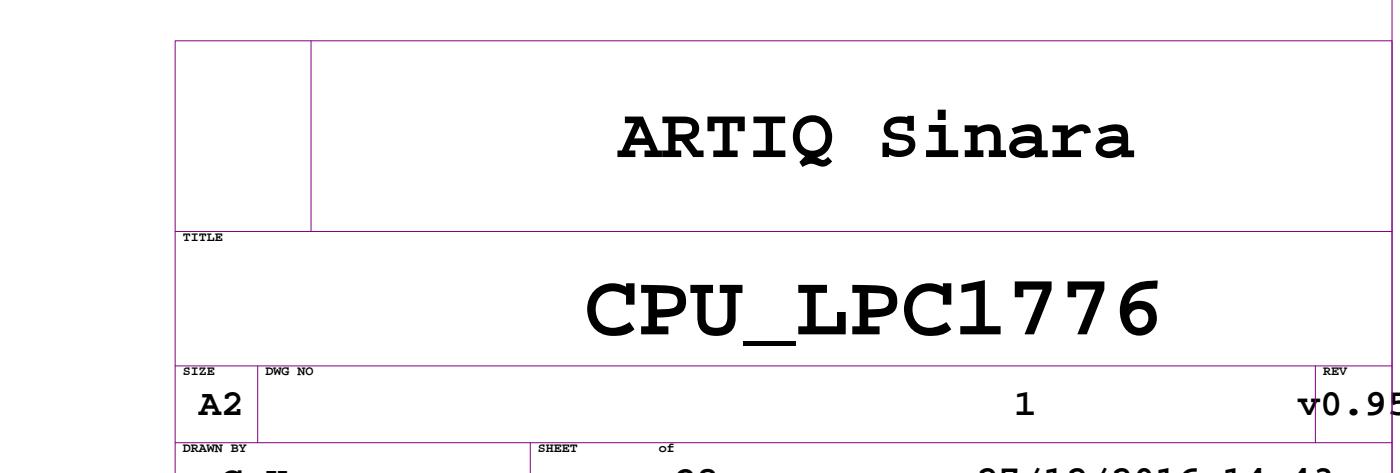
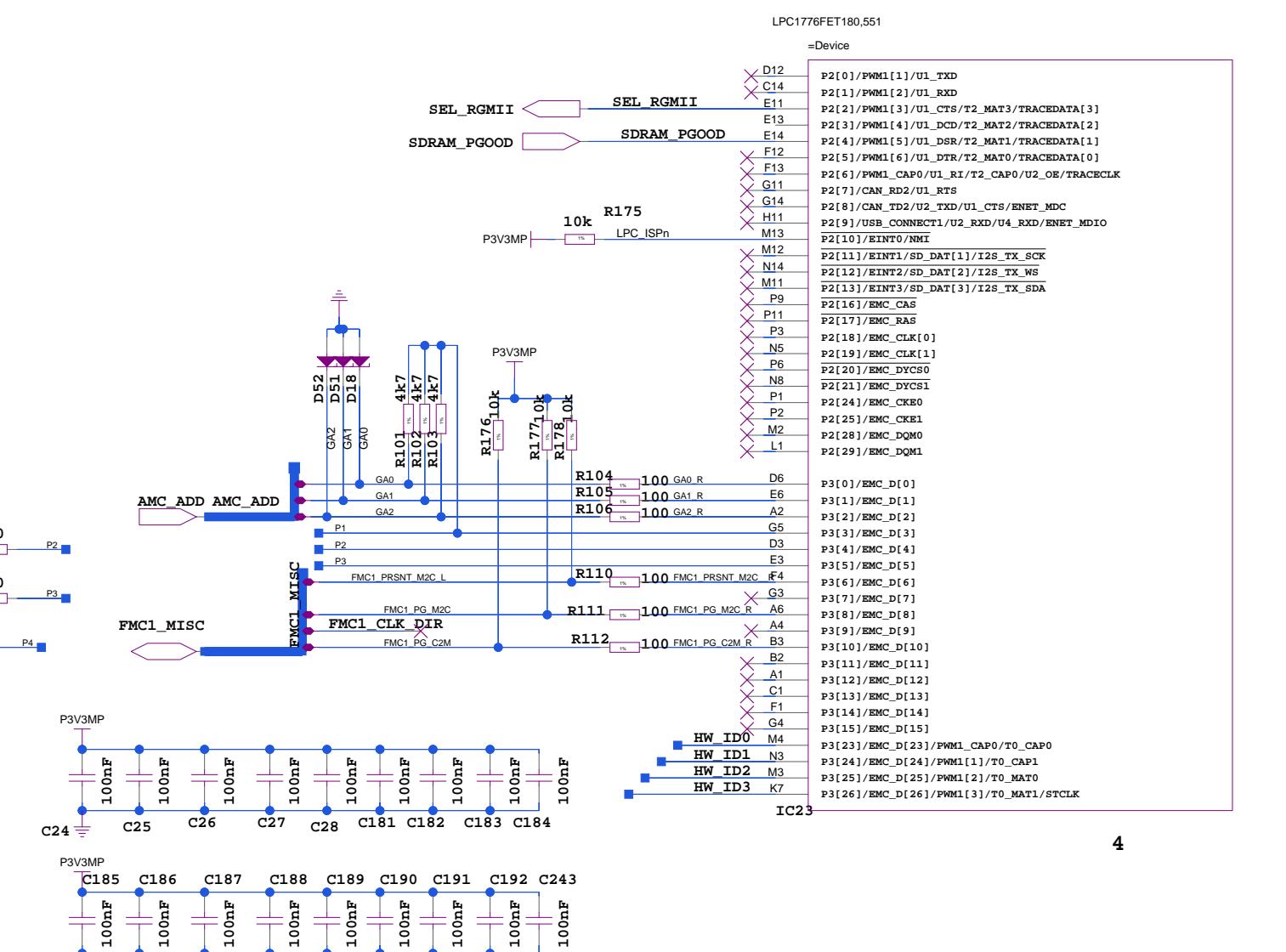
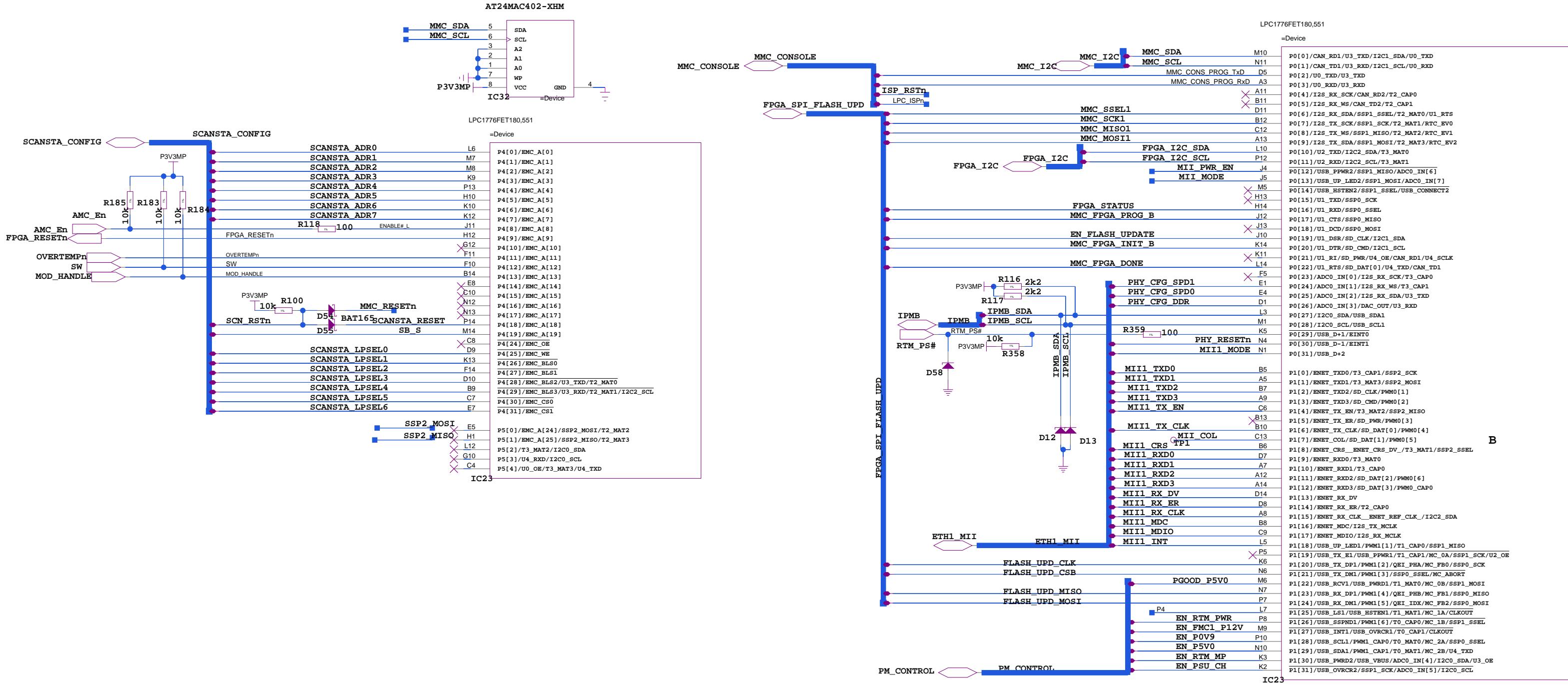
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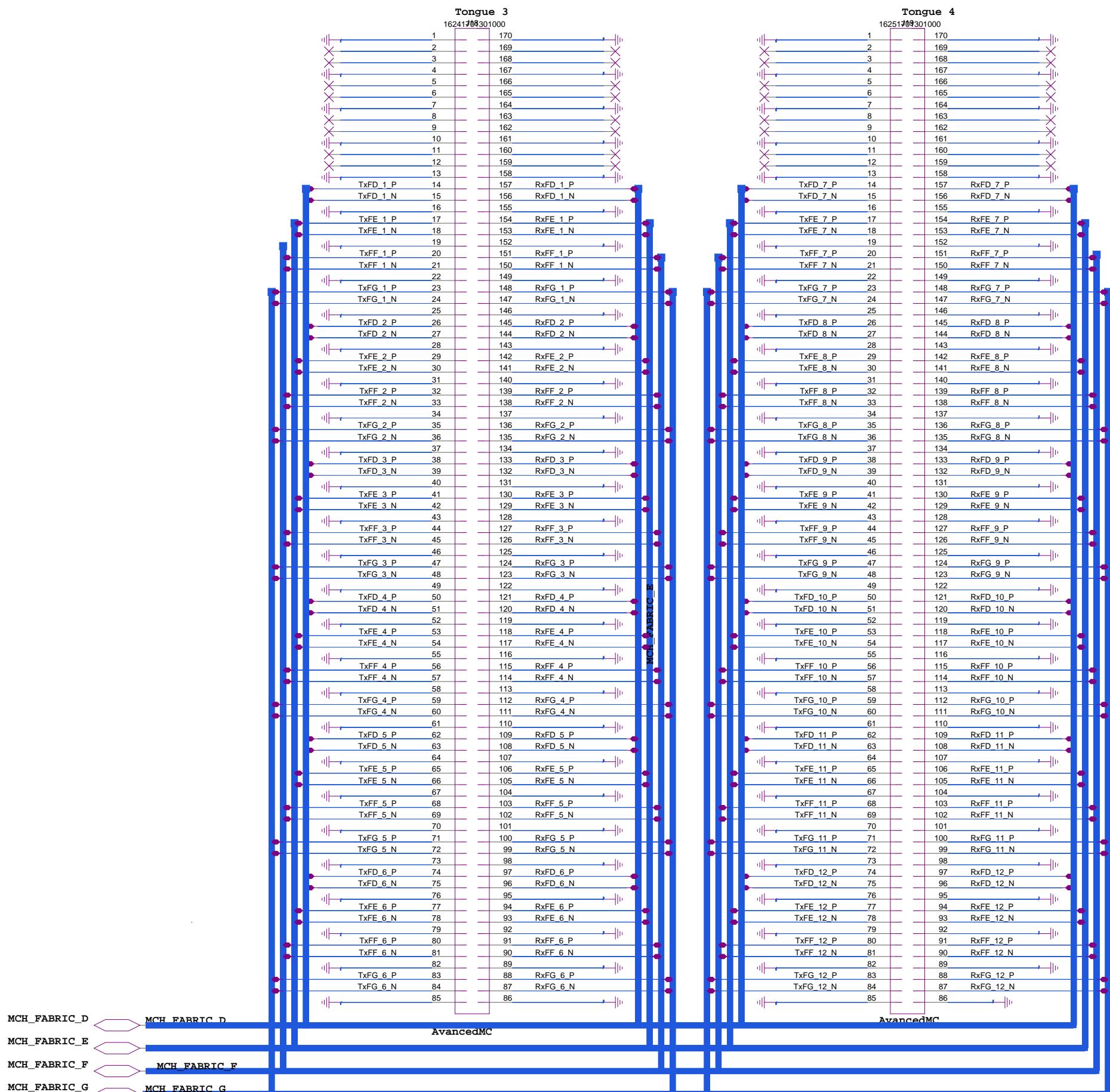
Interfaces with modules
Impedance: 100Ohm diff
diff lines: LVDS 2.5V
control signals: 3.3V LVC MOS

ARTIQ Sinara

FMC_connector

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G.K.	21	28	26/12/2016:19:33





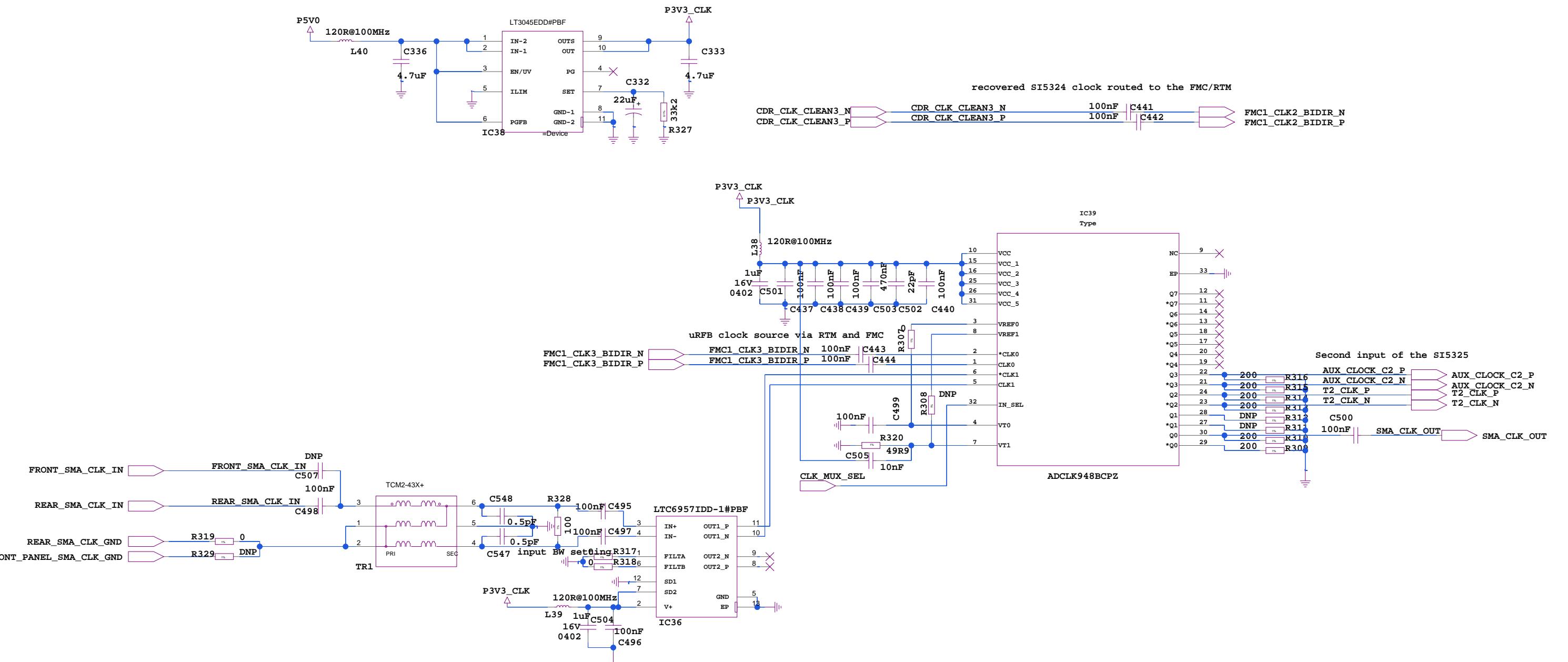
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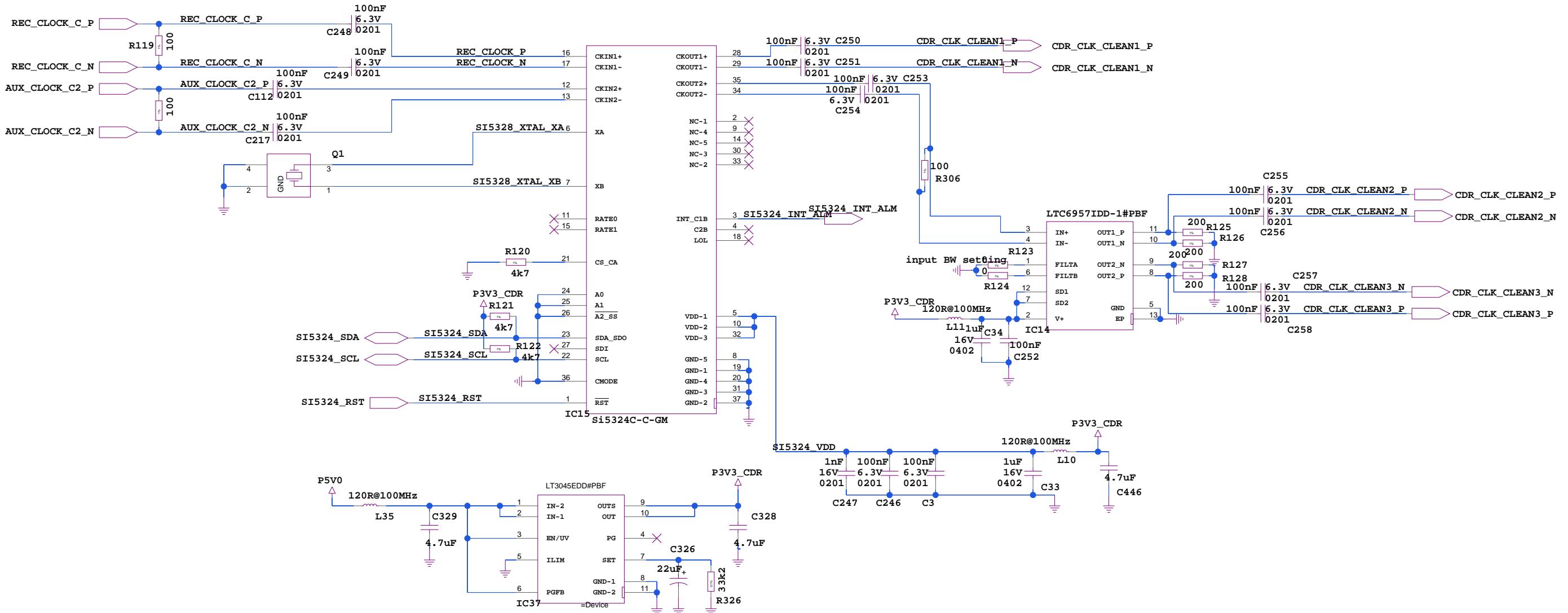
MCH_CON

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SIZE	DWG NO
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SHEET 23 of 28	
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1 21/12/2016:23:49	

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Interfaces MFC: backplane
Impedance: 100Ω diff
control signals: 3.3V LVCMOS



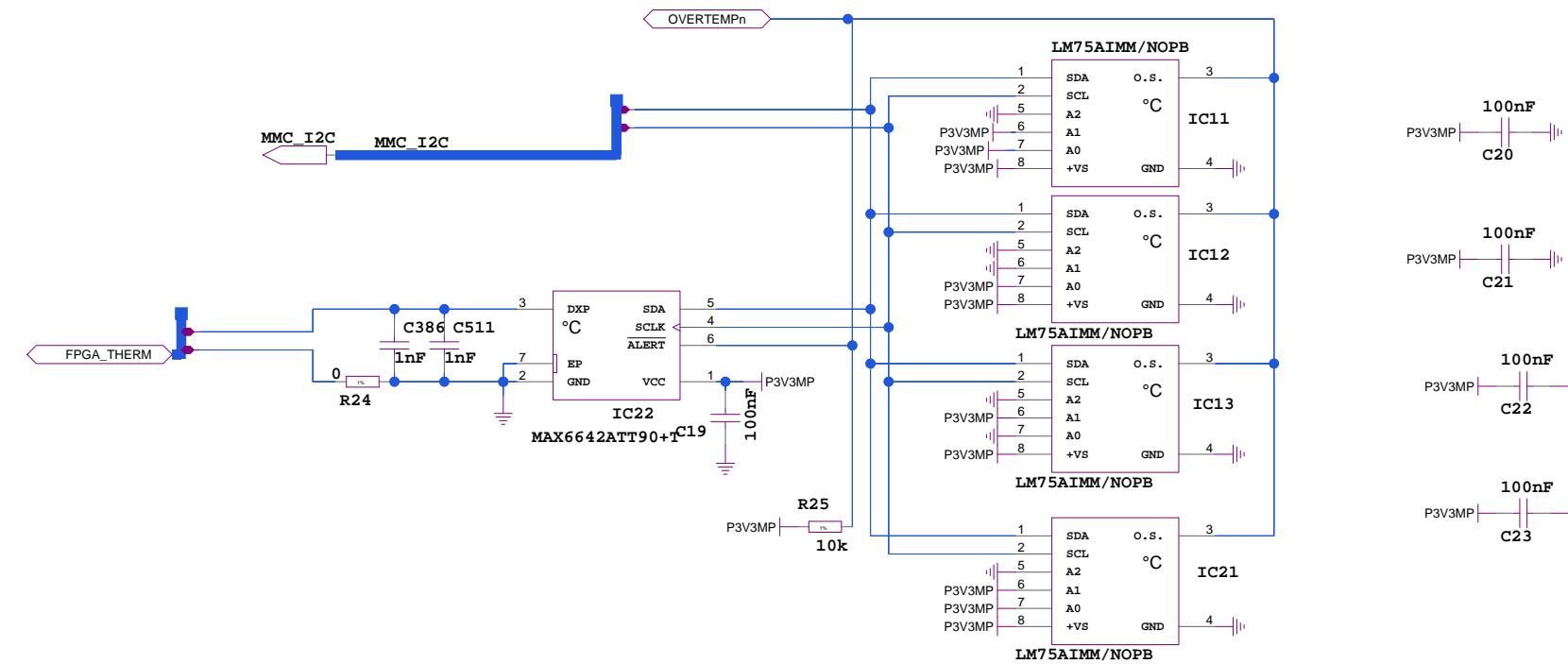


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SI5324_CLK_RECOVERY

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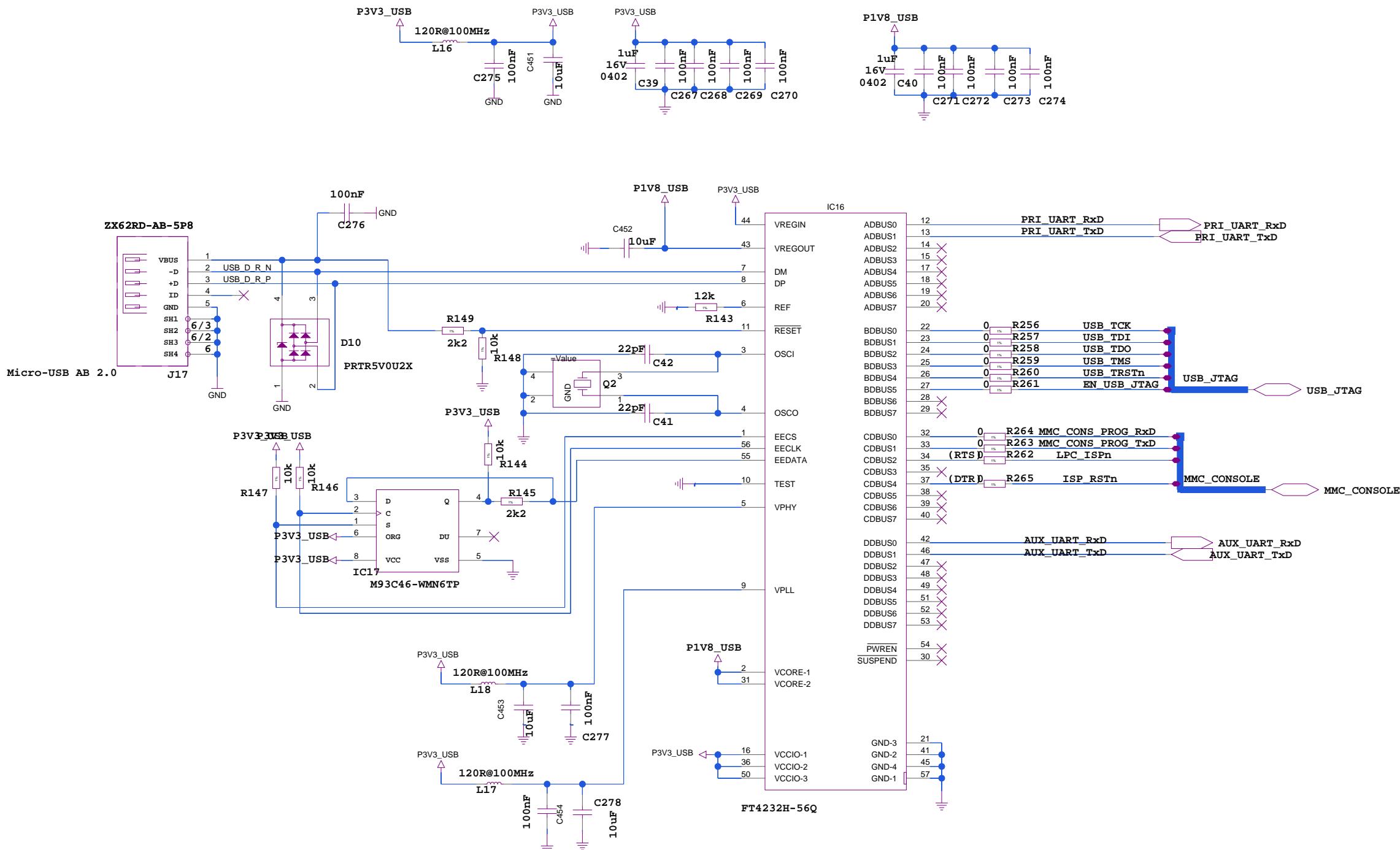


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Thermometers

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23/12/2016:14:41			



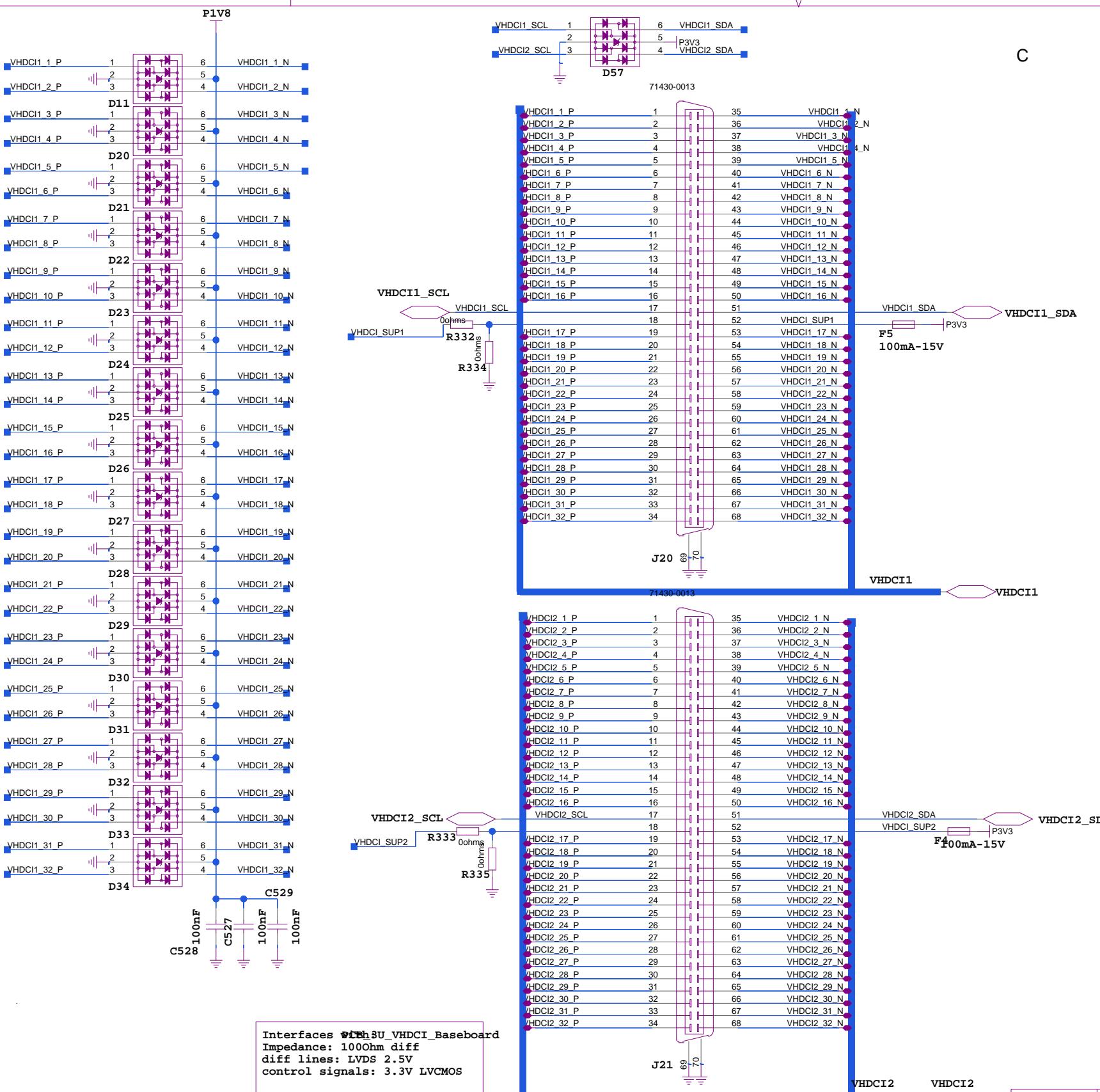
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USB_SERIAL_QUAD

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