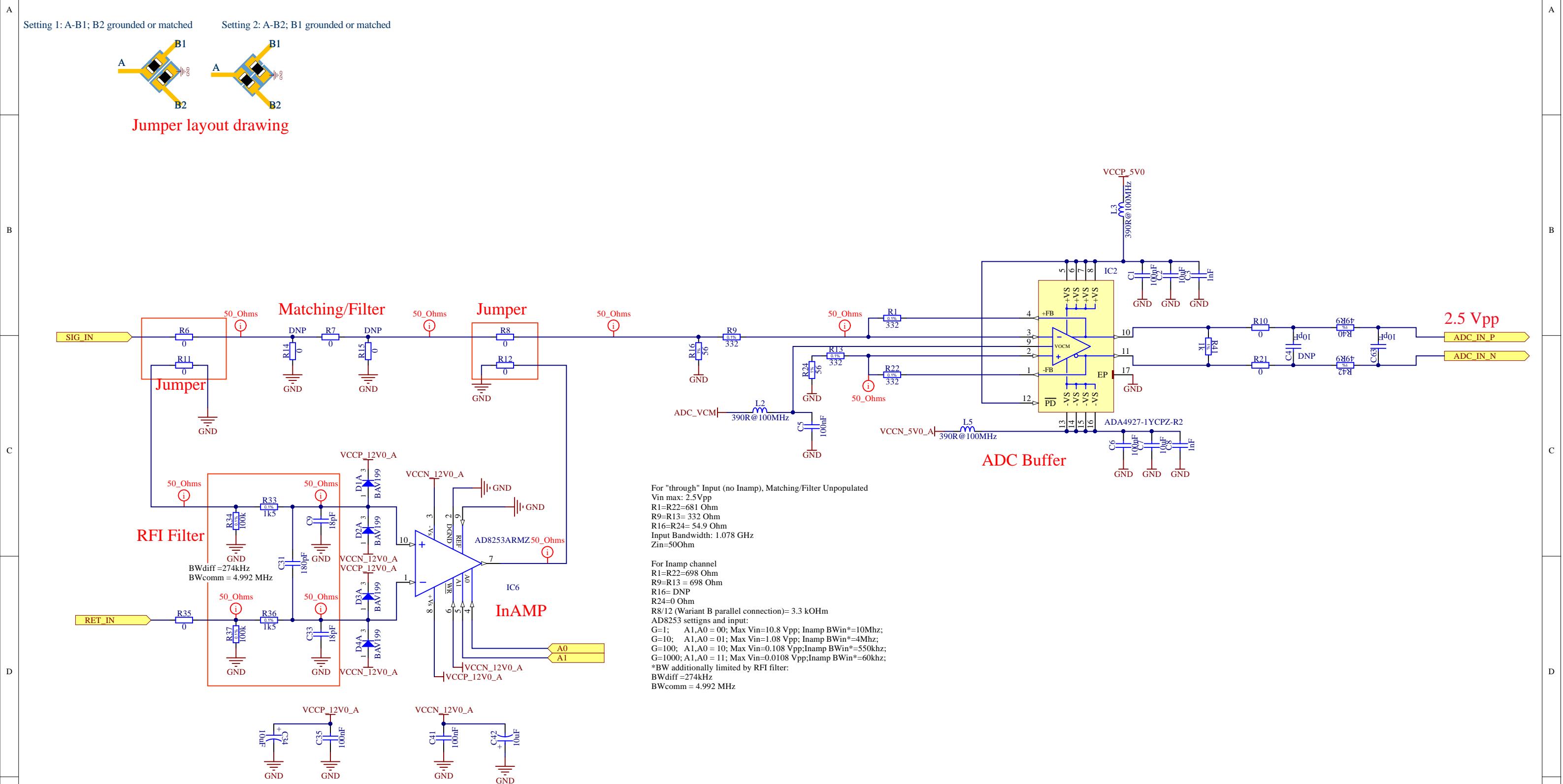
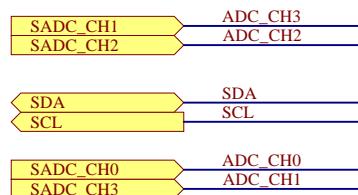
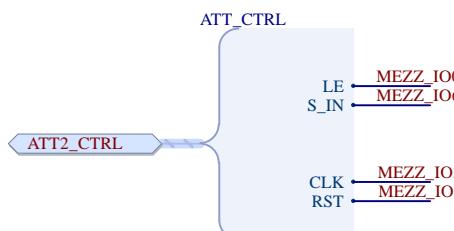
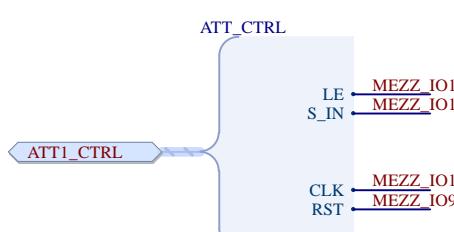
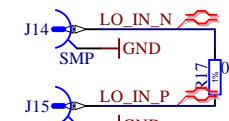
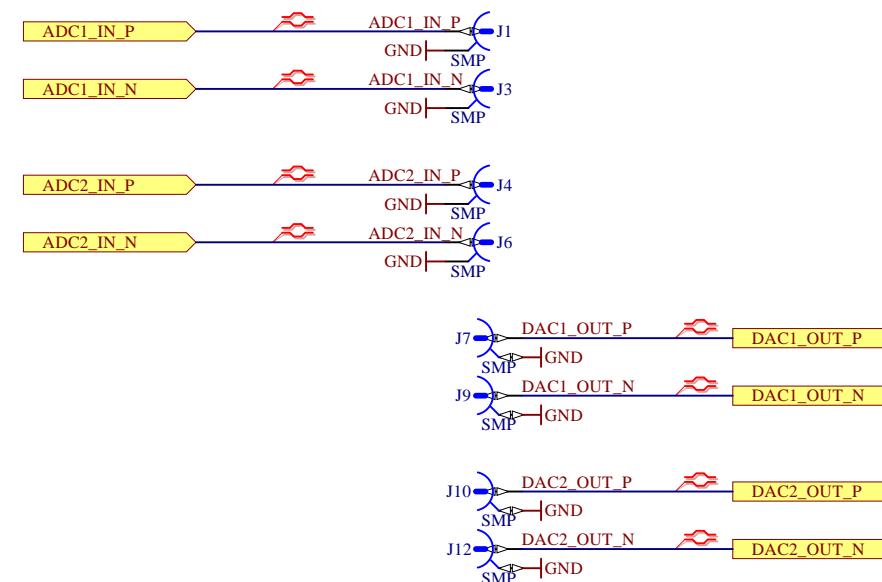


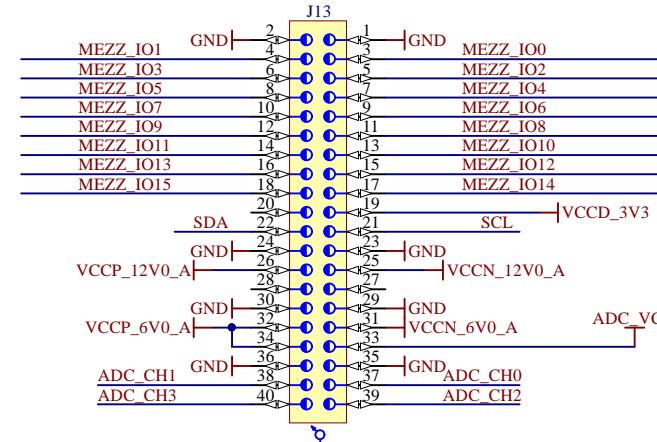
Project/Equipment		ADC/DAC MEZZANINE	
Document		Designer	SBH
		Drawn by	SBH
		Check by	-
		Last Mod.	2017-03-31
		File	allaki_mezz_top.SchDoc
		Print Date	2017-04-01 16:45:34
		Sheet	1 of 1
Warsaw University of Technology ISE Nowowiejska 15/19		ARTIQ	Size A3 Rev -



Board-2-Board Analog Connectors

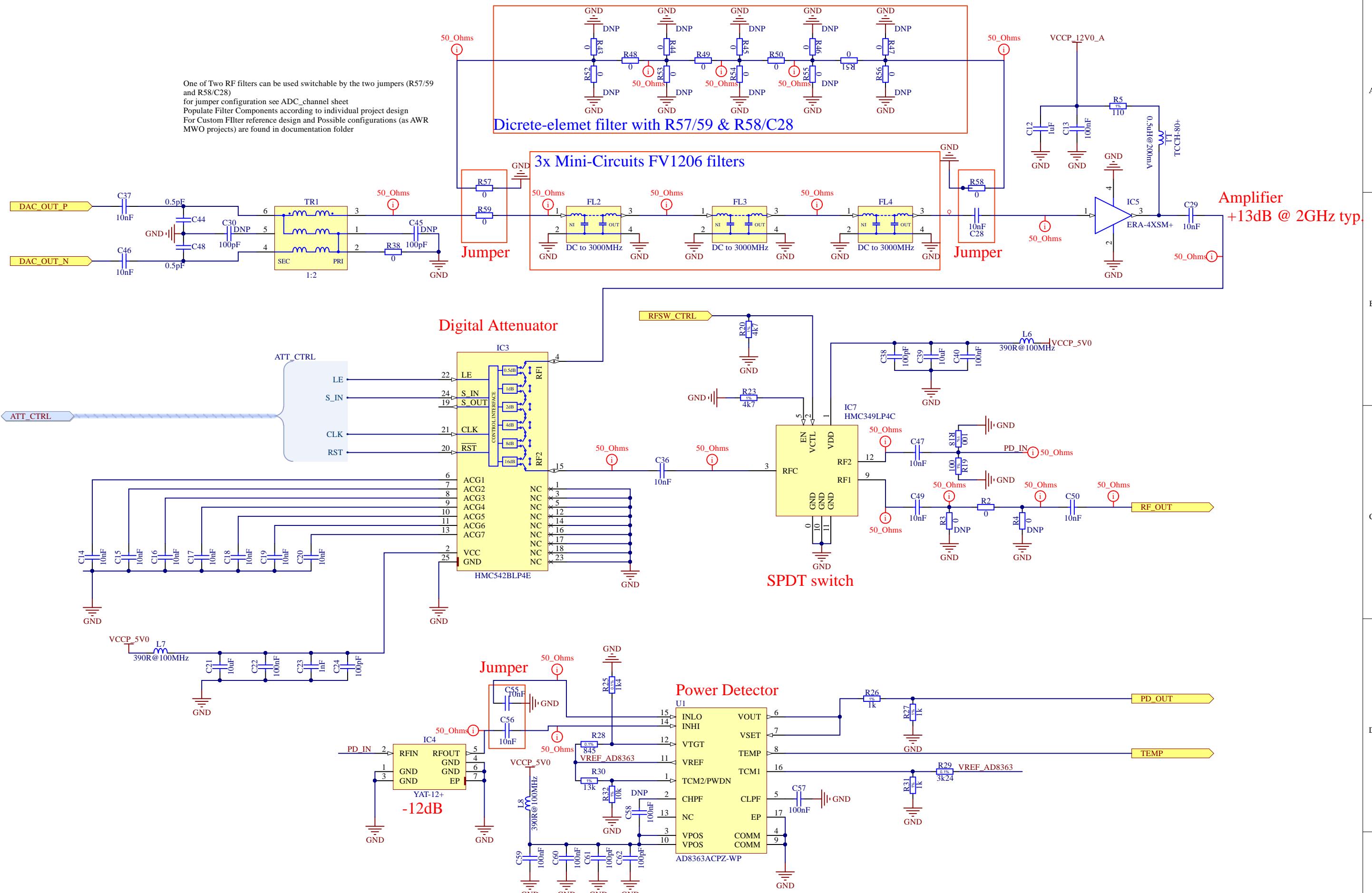


Board-2-Board Digital Connector



Project/Equipment		ADC/DAC MEZZANINE	
Document	allaki_mezzanine.PrjPCB	Drawn by	SBH
	B2B_connectors.SchDoc	Check by	XX/XX/XXXX
Last Mod.	-	-	2017-03-31
File	B2B_connectors.SchDoc	Print Date	2017-04-01 16:45:35
Sheet	1	of	1
Rev			

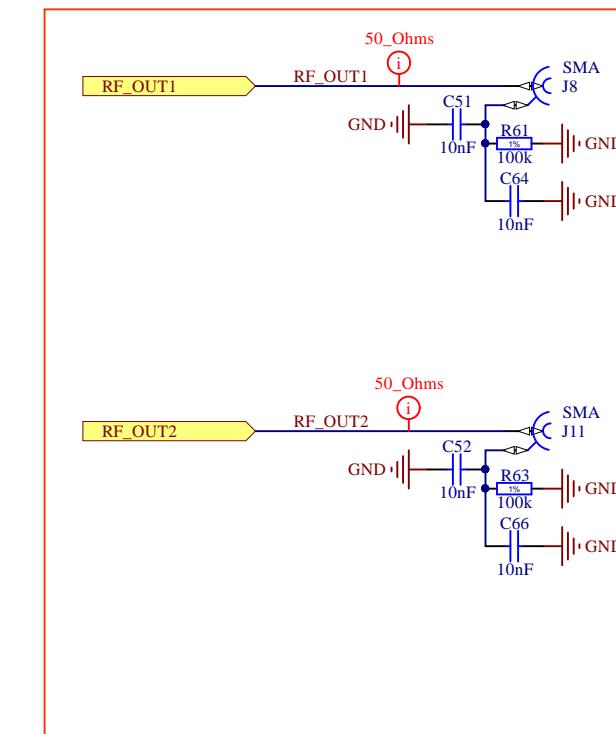
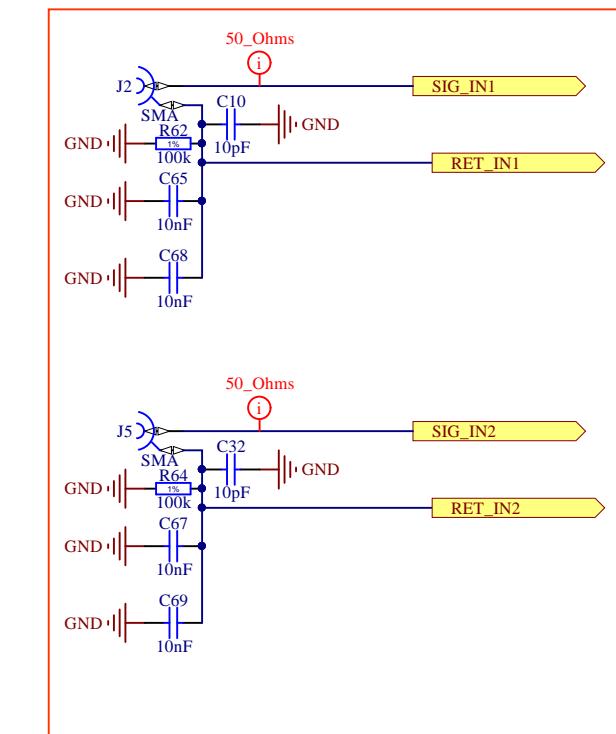
ARTIQ Warsaw University of Technology ISE Nowowiejska 15/19 ARTIQ A3 -



Project/Equipment ADC/DAC MEZZANINE	
Document	Designer SBH
 allaki_mezzanine.PrjPCB DAC_channel.SchDoc	Drawn by SBH
	Check-by -
	Last Mod. -
	File DAC_channel.SchDoc
	Print Date 2017-04-01 16:45:35
	Sheet - of -
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A

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Output SMAs**Input SMAs**

Input considerations and Variants:
-> ADC-channel.SchDoc

B

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E

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Project/Equipment ADC/DAC MEZZANINE

Document



**allaki_mezzanine.PrjPCB
FP_connectors.SchDoc**

Designer	SBH	Drawn by	SBH	XX/XX/XXXX
Check by	-			
Last Mod.	-			2017-04-01
File	FP_connectors.SchDoc			
Print Date	2017-04-01 16:45:35			Sheet of

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ARTIQ

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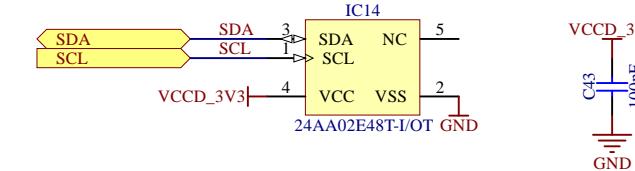
D

D

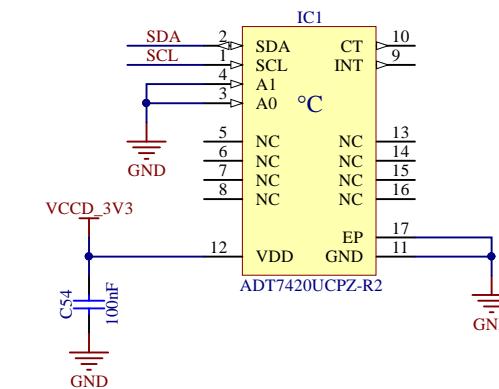
E

E

ID EEPROM

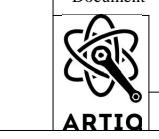


Temperature sensor



Project/Equipment ADC/DAC MEZZANINE

Document



allaki_mezzanine.PrjPCB
Mgmt.SchDoc

Designer SBH	Drawn by SBH	XX/XX/XXXX
Check by	-	
Last Mod.	-	2017-03-31
File Mgmt.SchDoc	Print Date 2017-04-01 16:45:35	Sheet of
		A3 -

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ARTIQ

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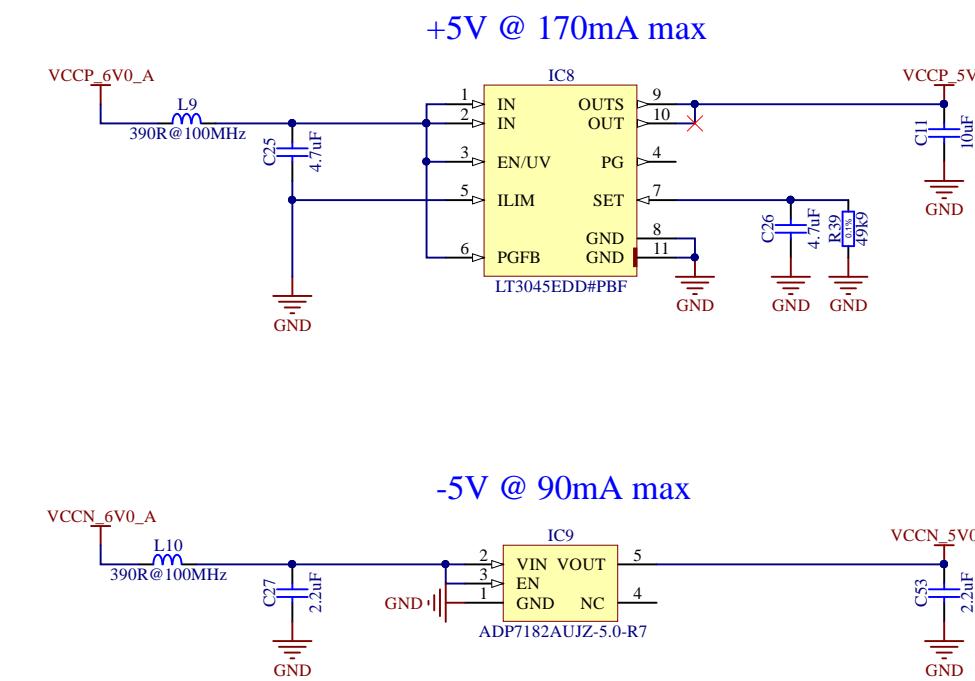
C

D

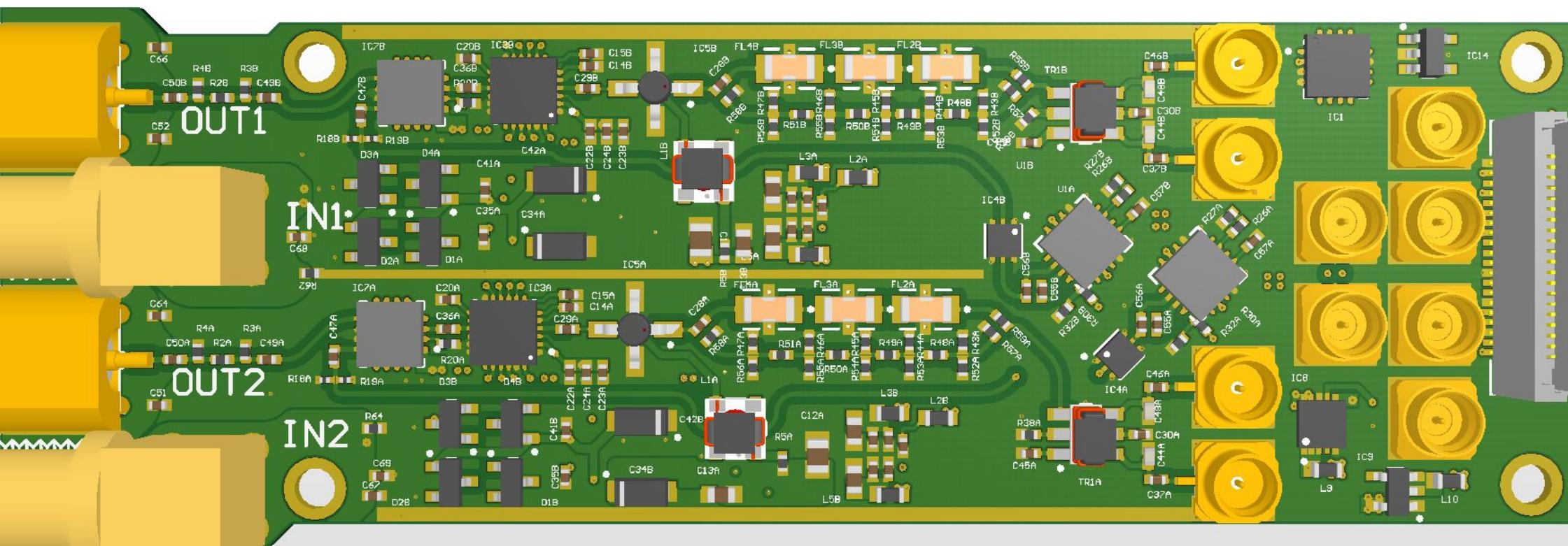
D

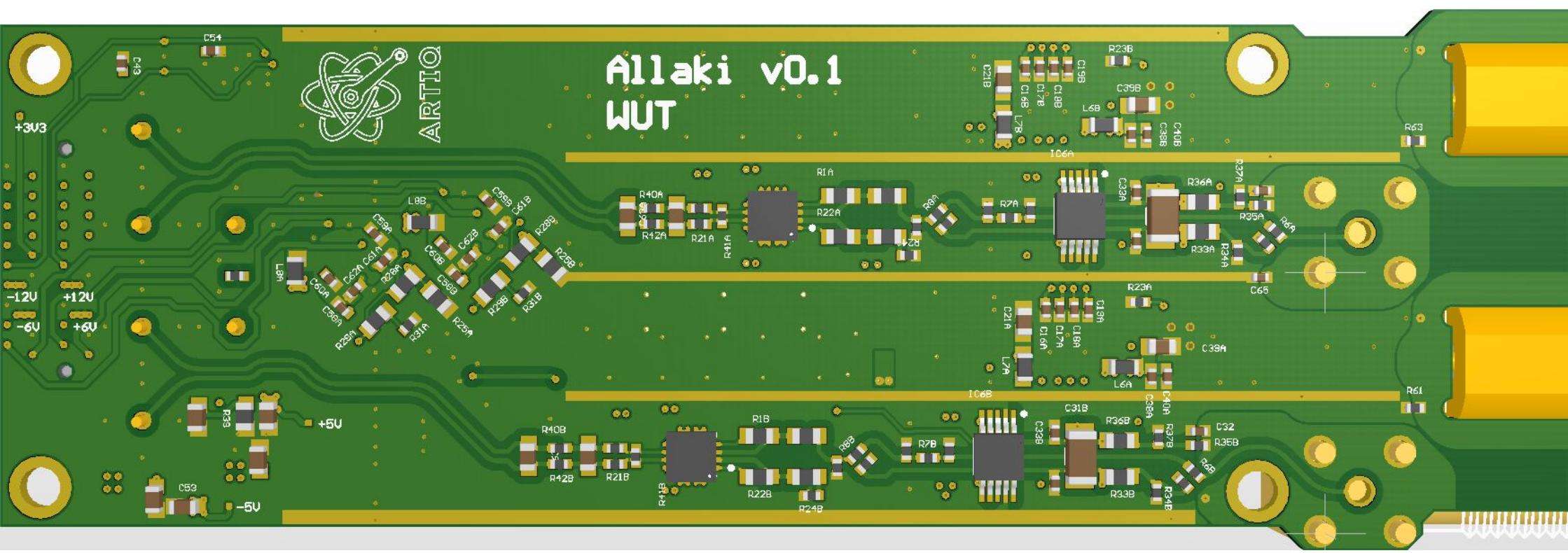
E

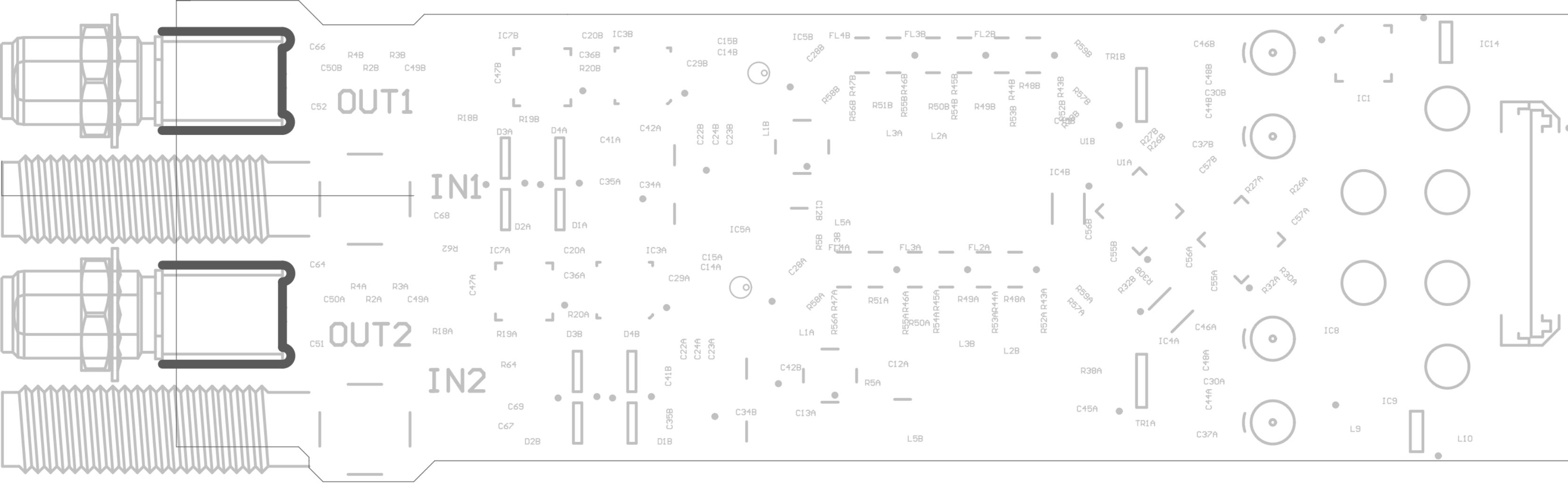
E

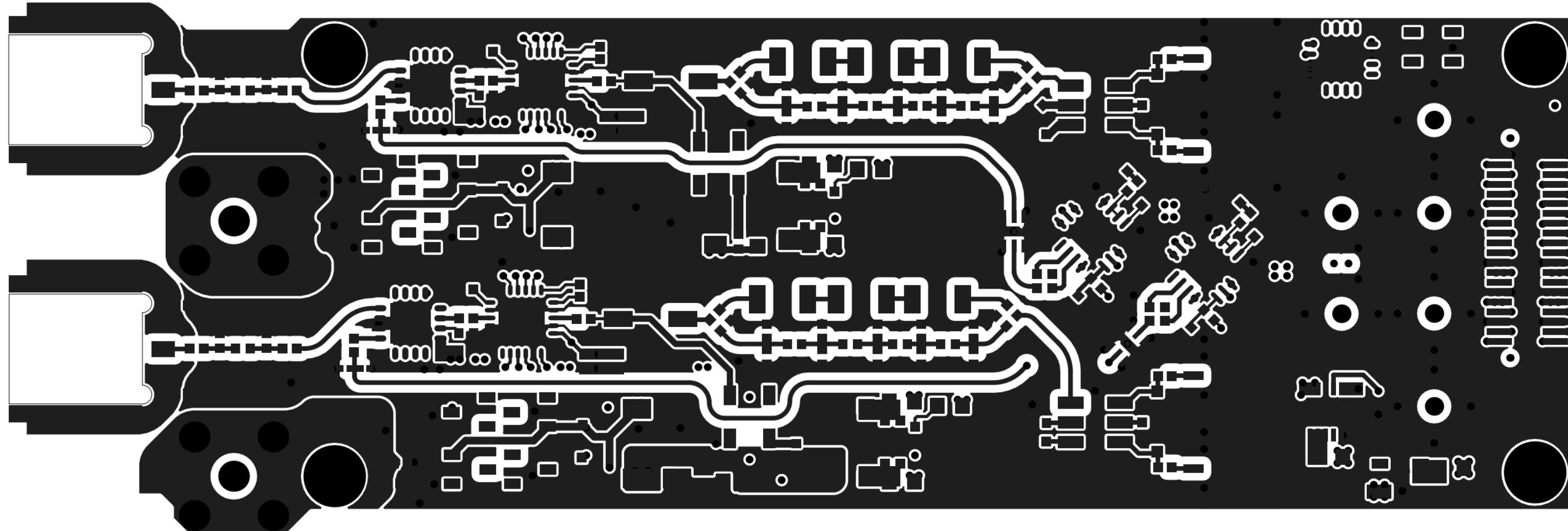


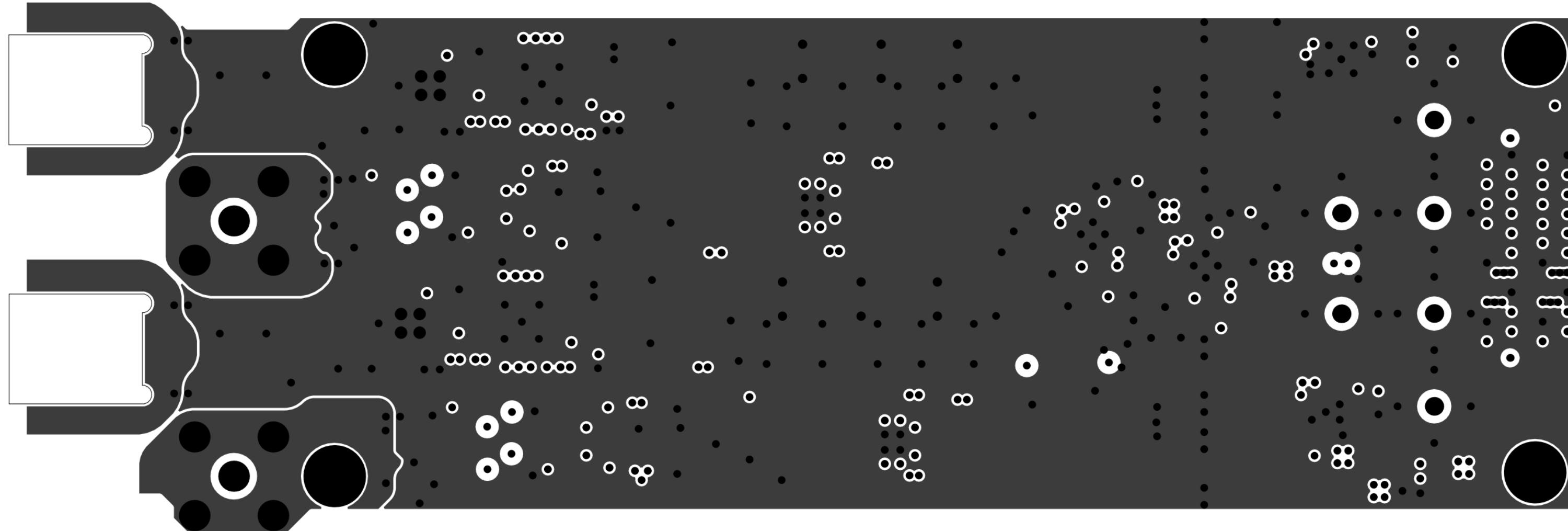
Project/Equipment		ADC/DAC MEZZANINE
Document		Designer SBH Drawn by SBH Check by - Last Mod. - File PowerSupply.SchDoc Print Date 2017-04-01 16:45:35
<i>allaki_mezzanine.PrjPCB PowerSupply.SchDoc</i>		XX/XX/XXXX
		Sheet of -
Warsaw University of Technology ISE Nowowiejska 15/19		Size A3 Rev -

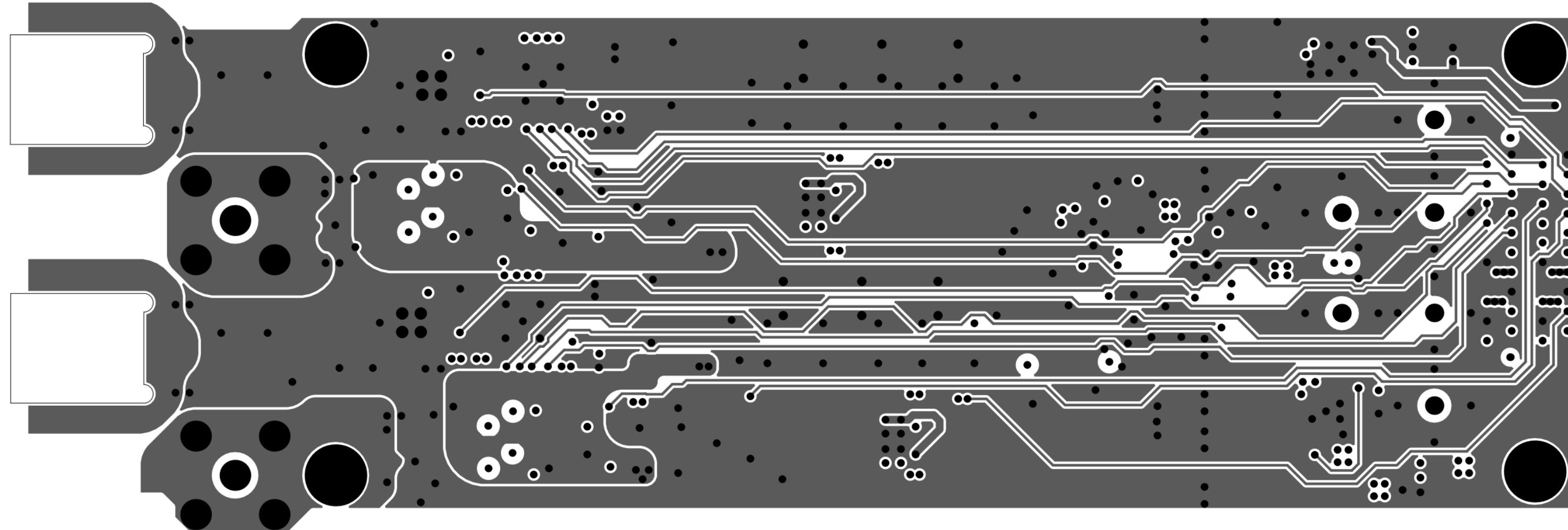


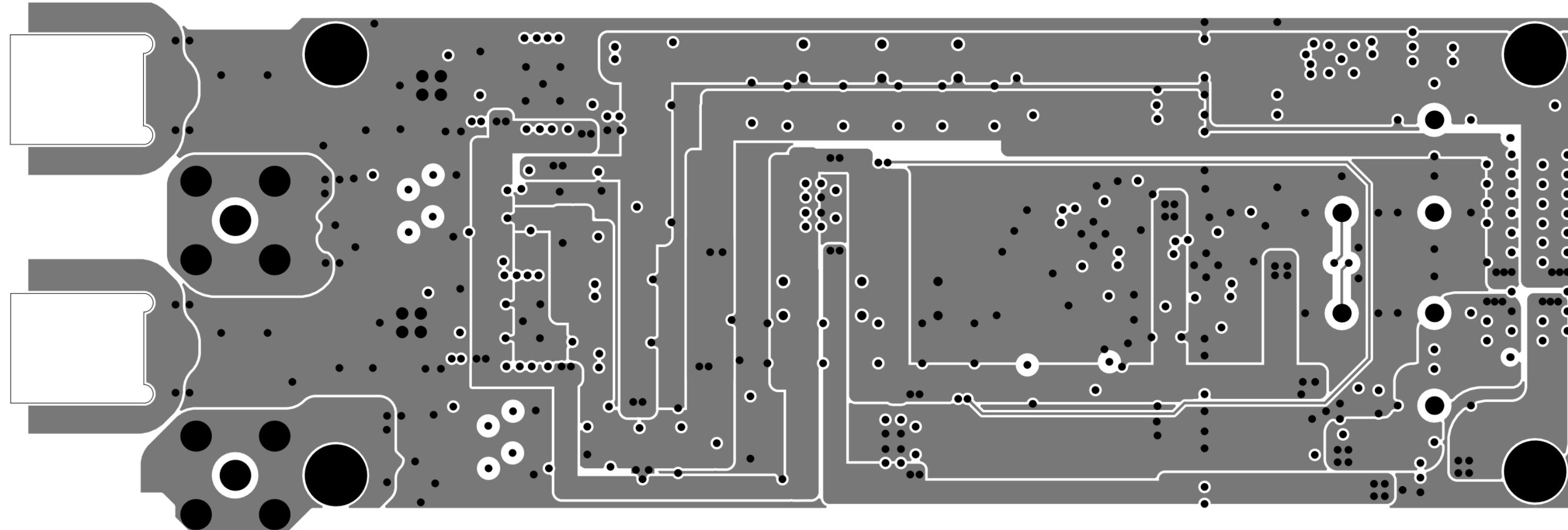




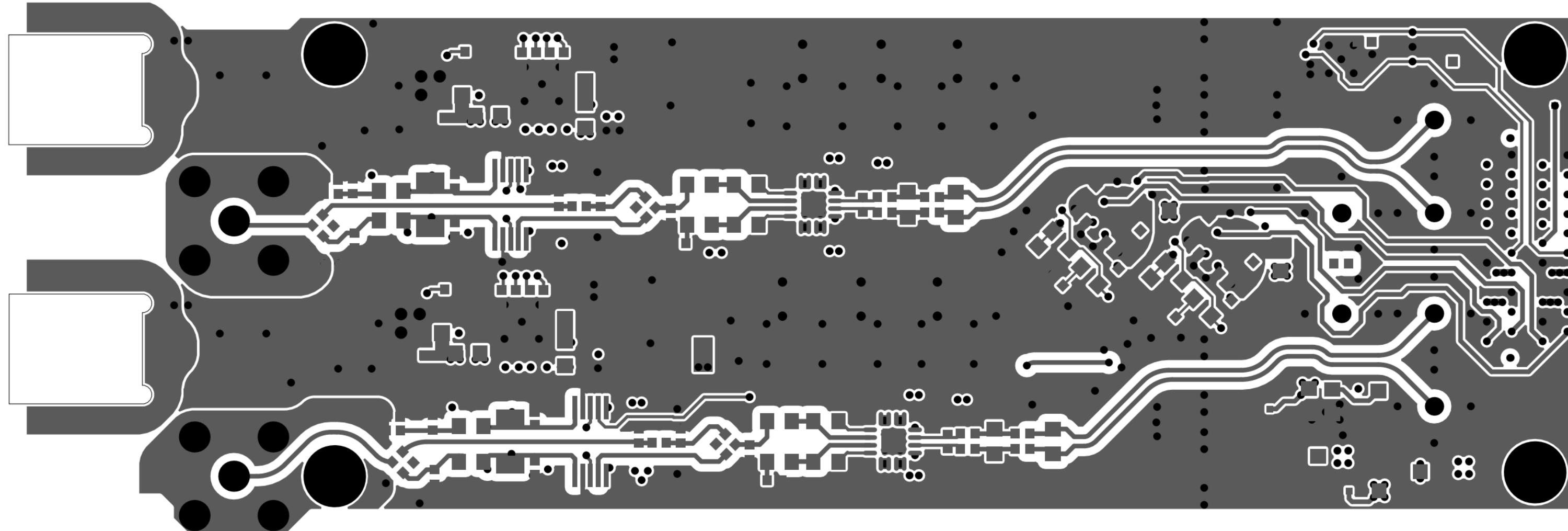














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