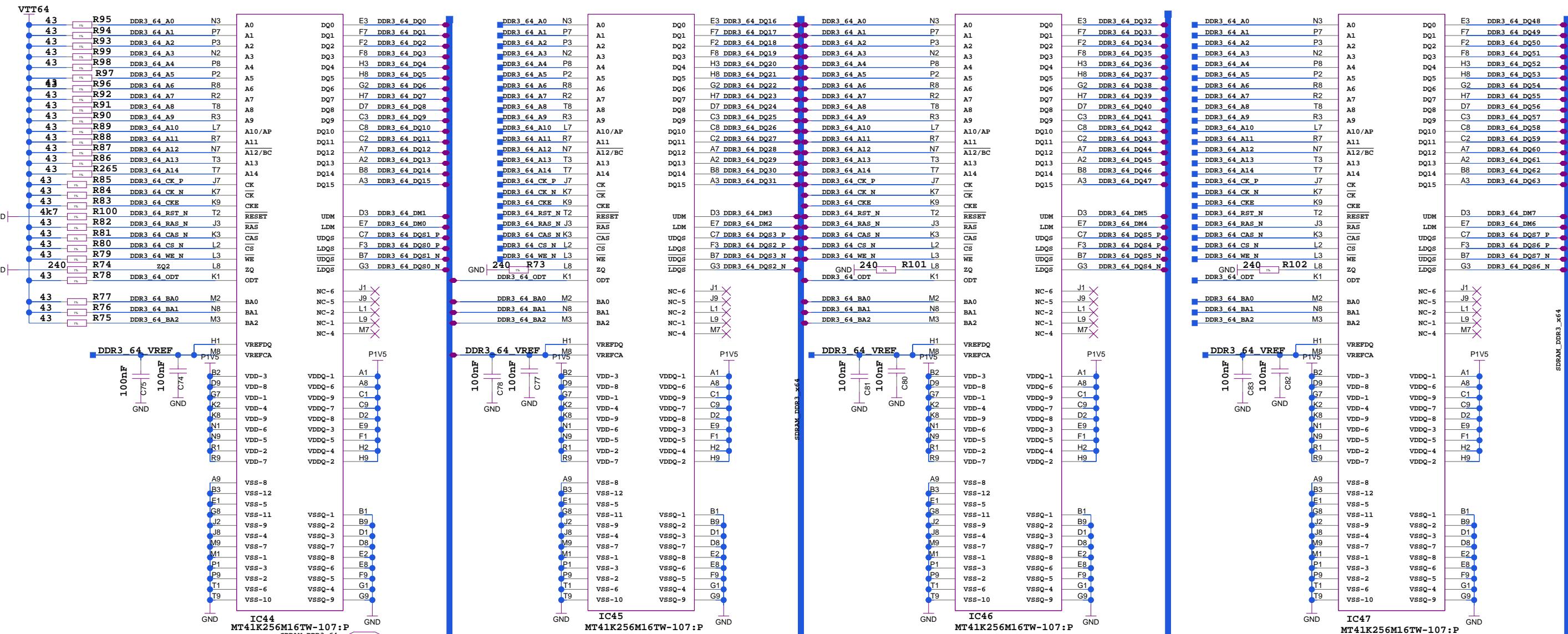


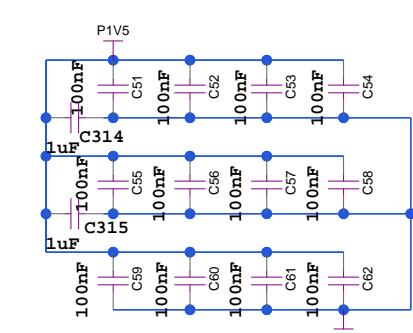
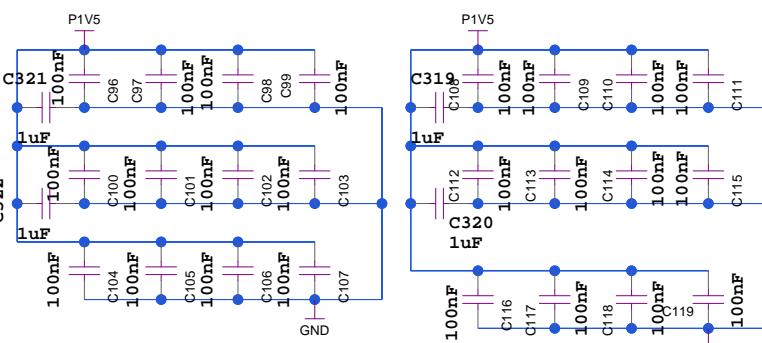
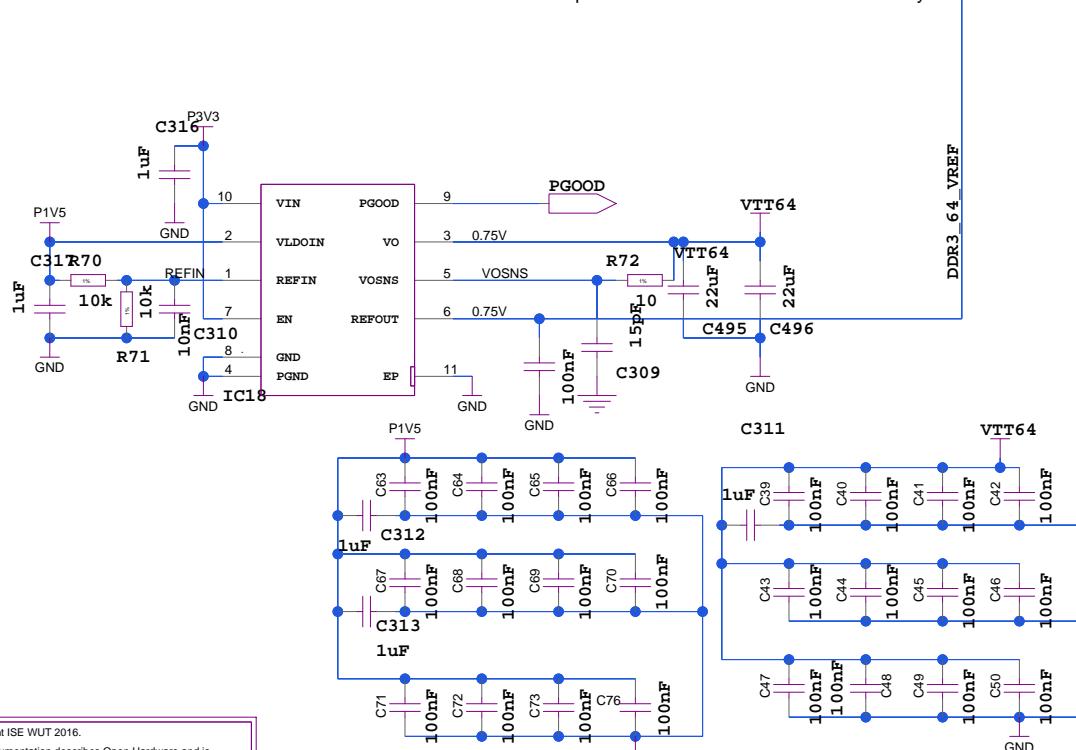
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Sayma_AMC

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All capacitors without values are 100nF 0201 by default



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SDRAM_DDR3_4x16

TITLE

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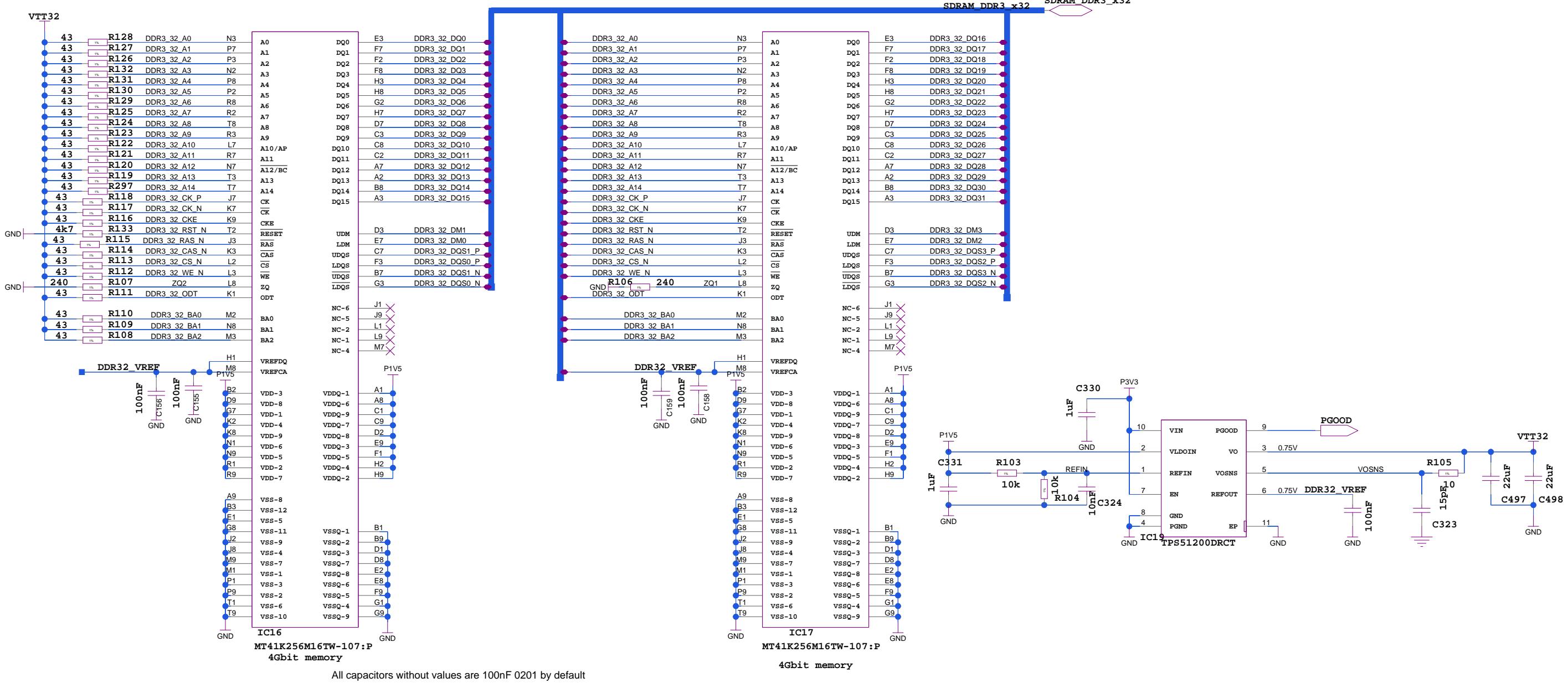
of

1

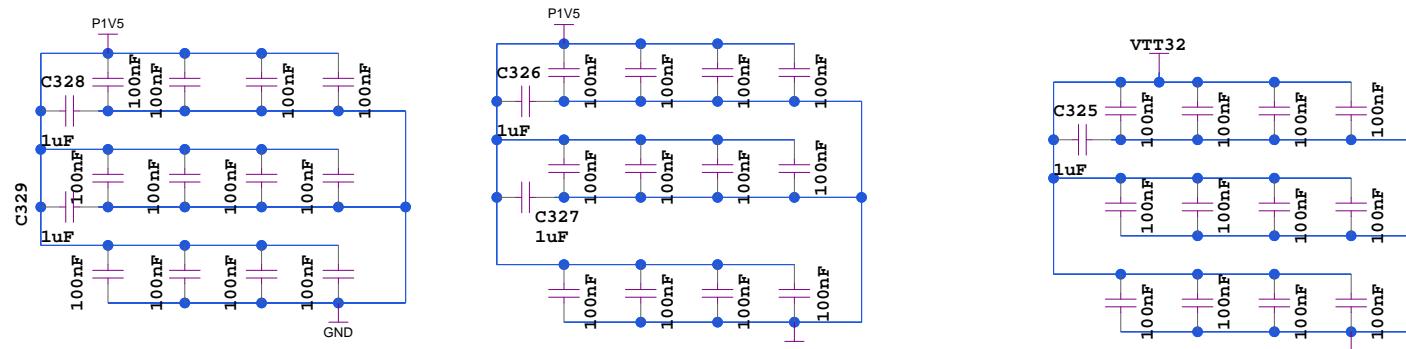
31

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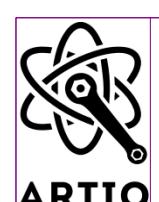
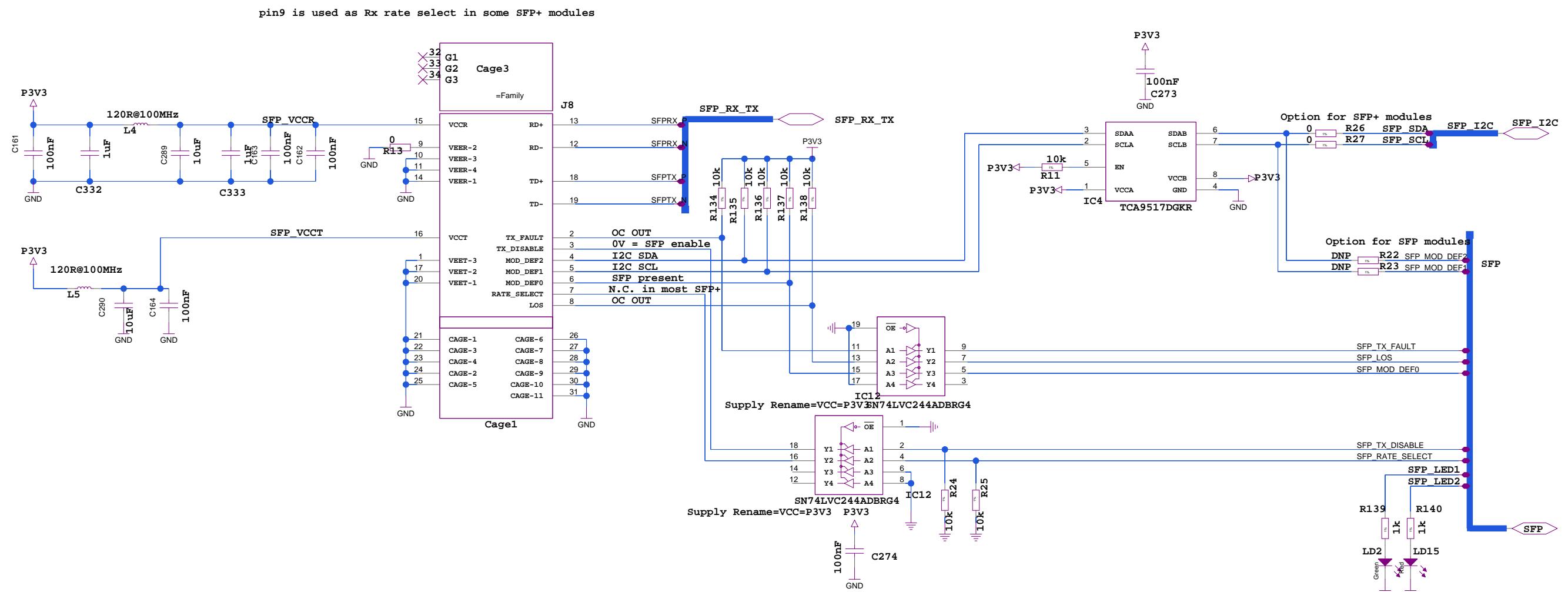
All capacitors without values are 100nF 0201 by default



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SDRAM DDR3 2x16

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SIZE DWG NO

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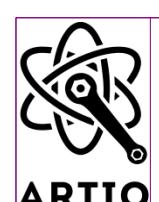
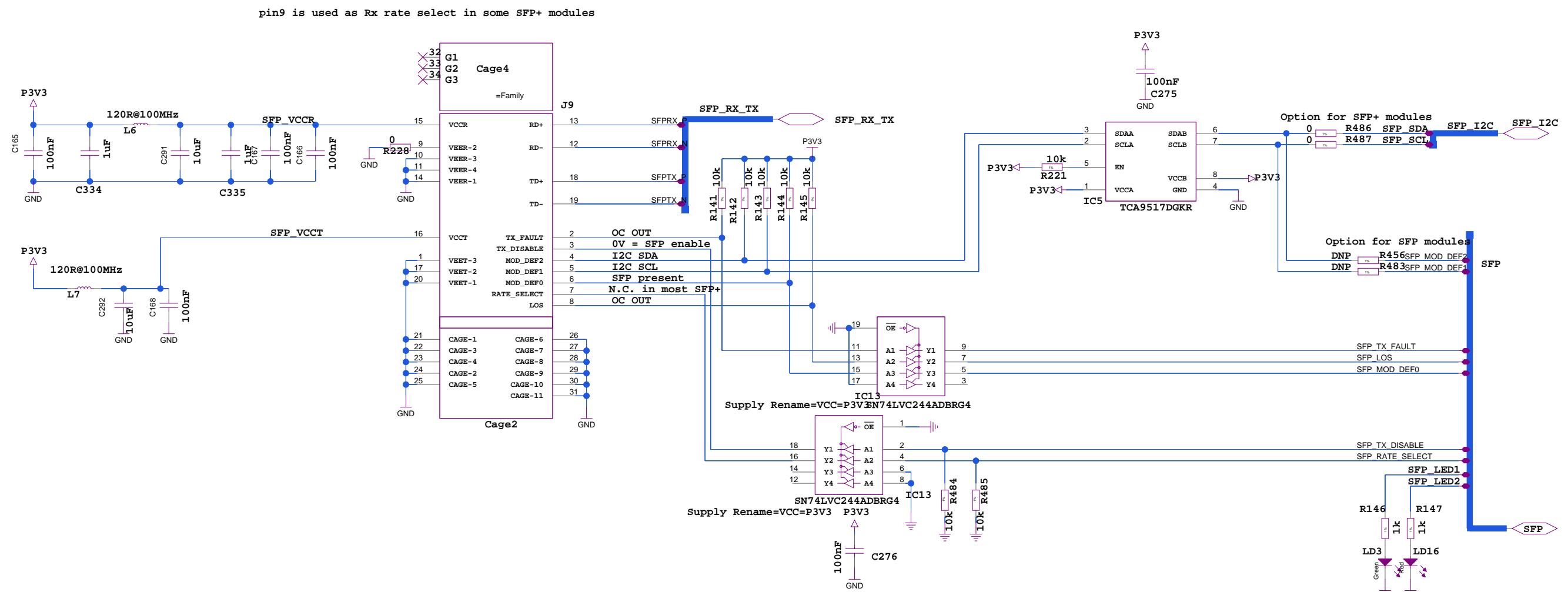
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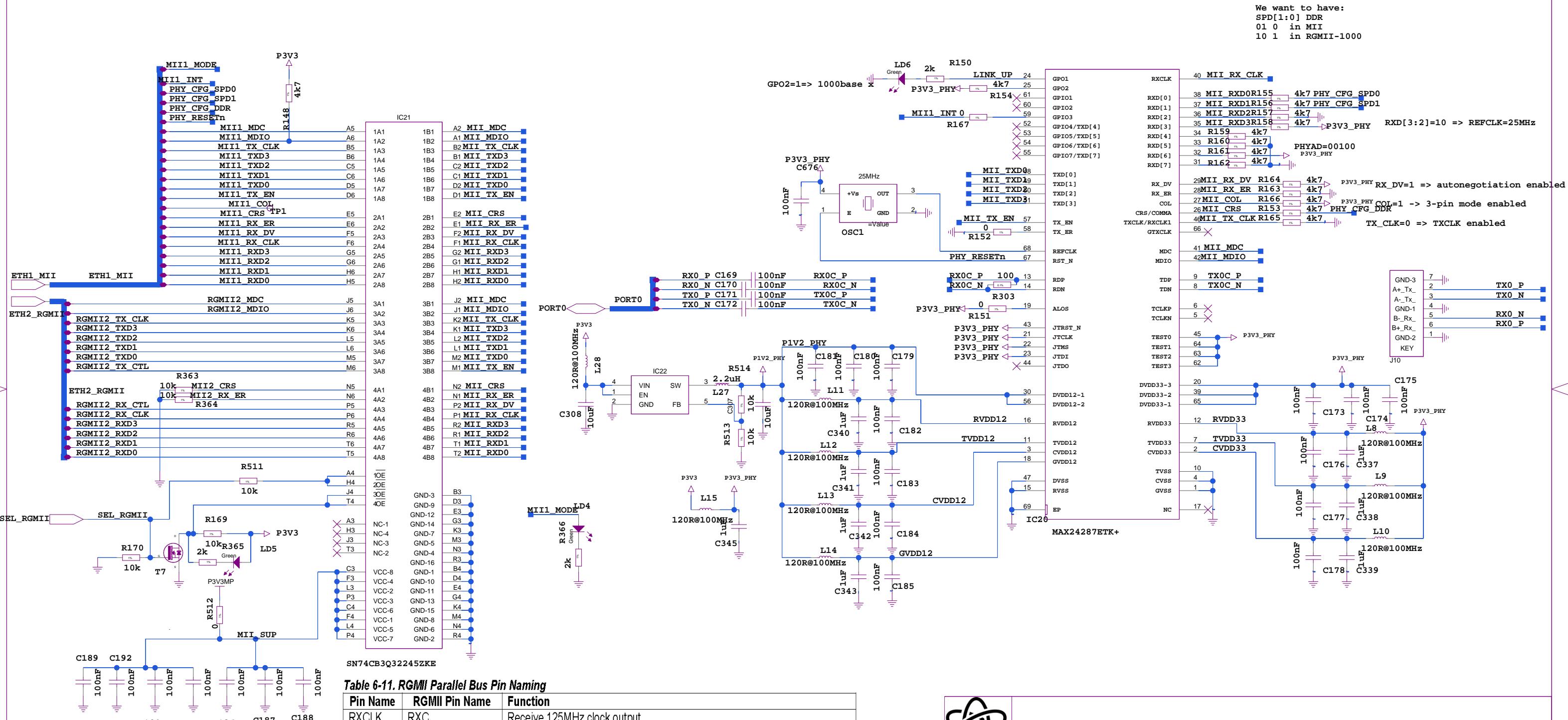
REV

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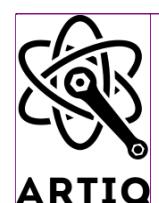
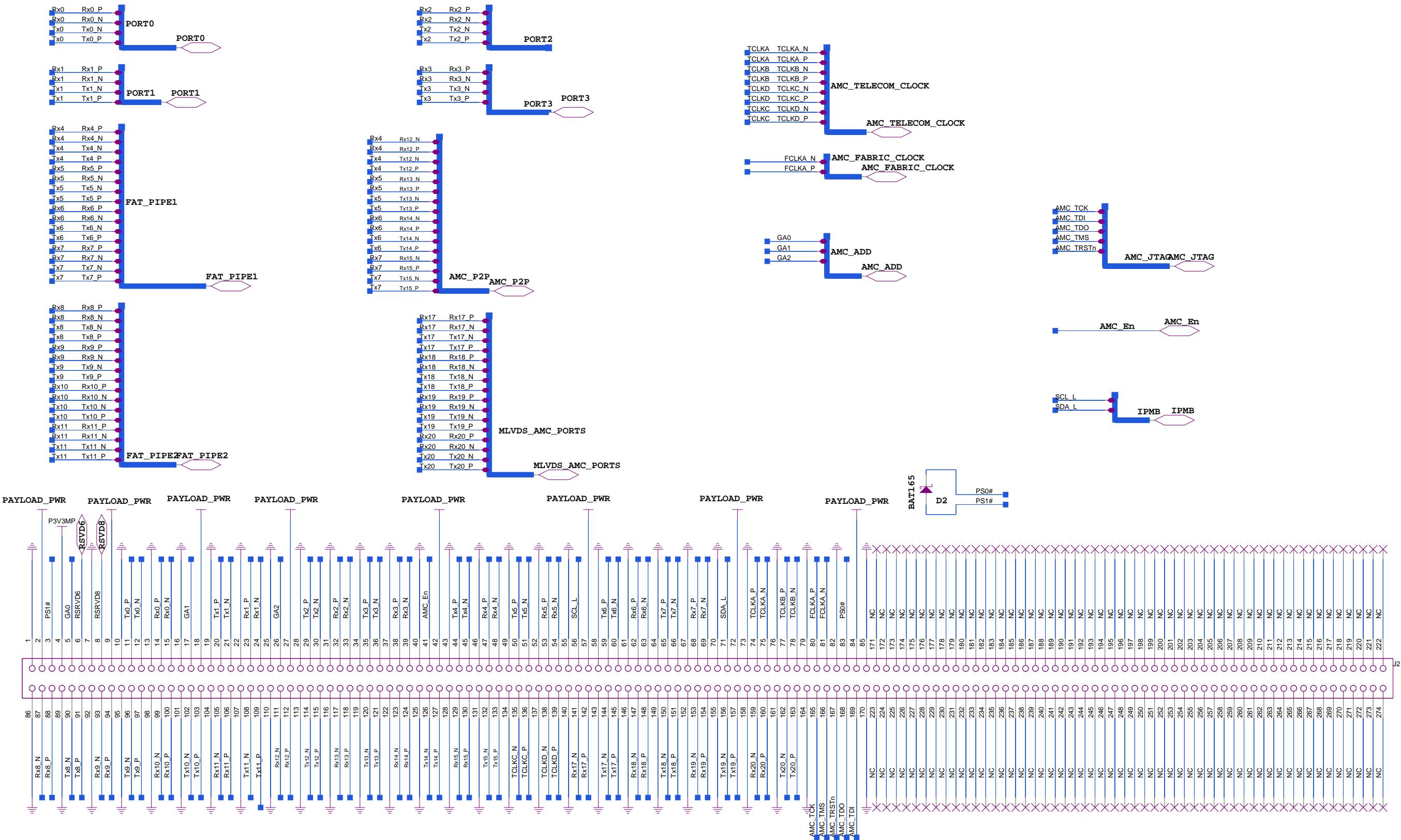


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ETH_PHY_RMII_MII



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AMC_Connector

SIZE	DWG NO	REV
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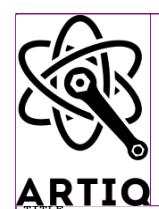
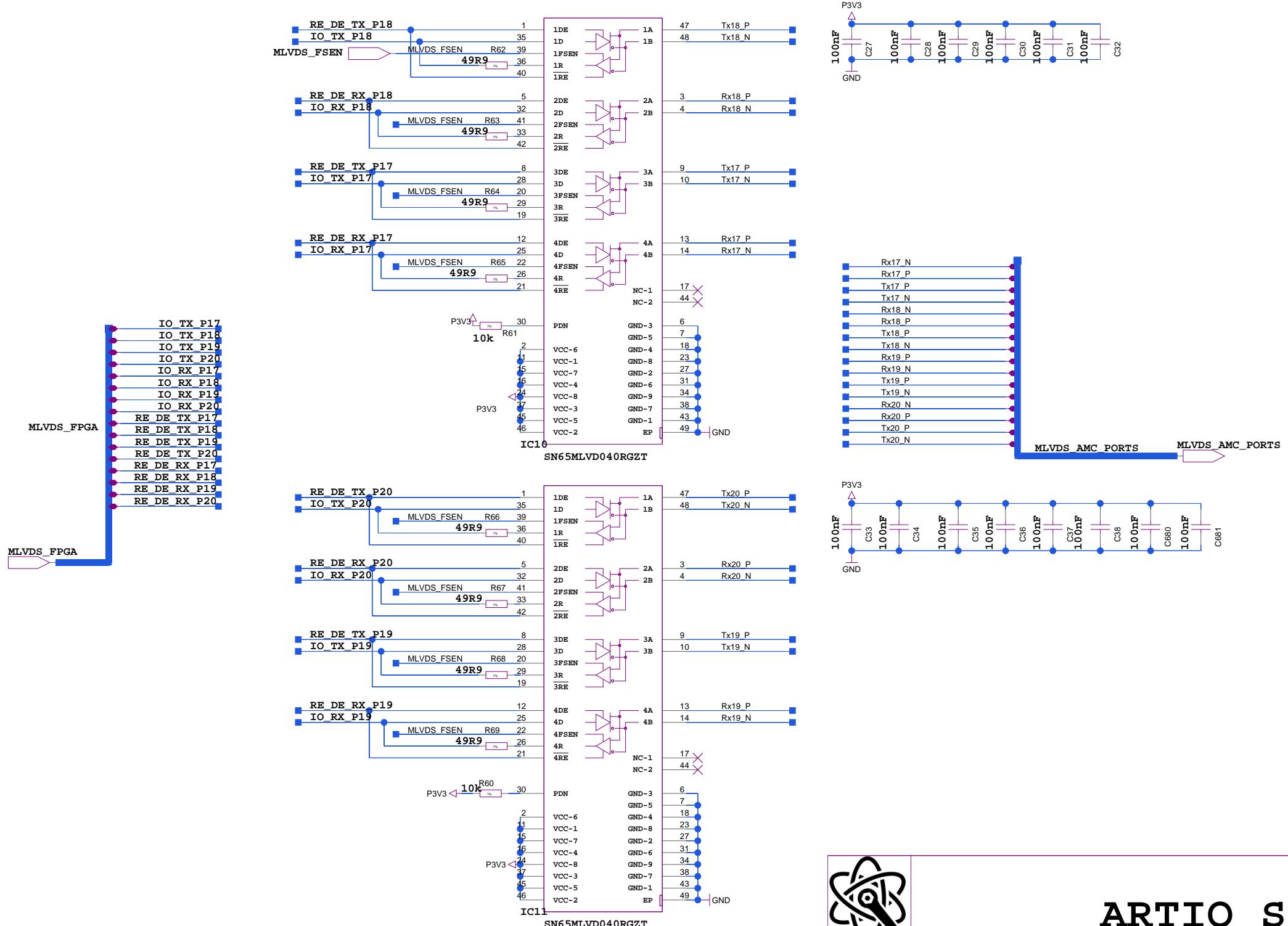
- Dimensions are in MM, nominal values used
- Component height rule derived from AMC Base Specification.PDF, Page 62
- The two corners of outline near the edge-connector are approximated, see AMC Base Specification.PDF, Page 59
- Stackup is not specified in AMC Base Specification.PDF or implemented in this template.

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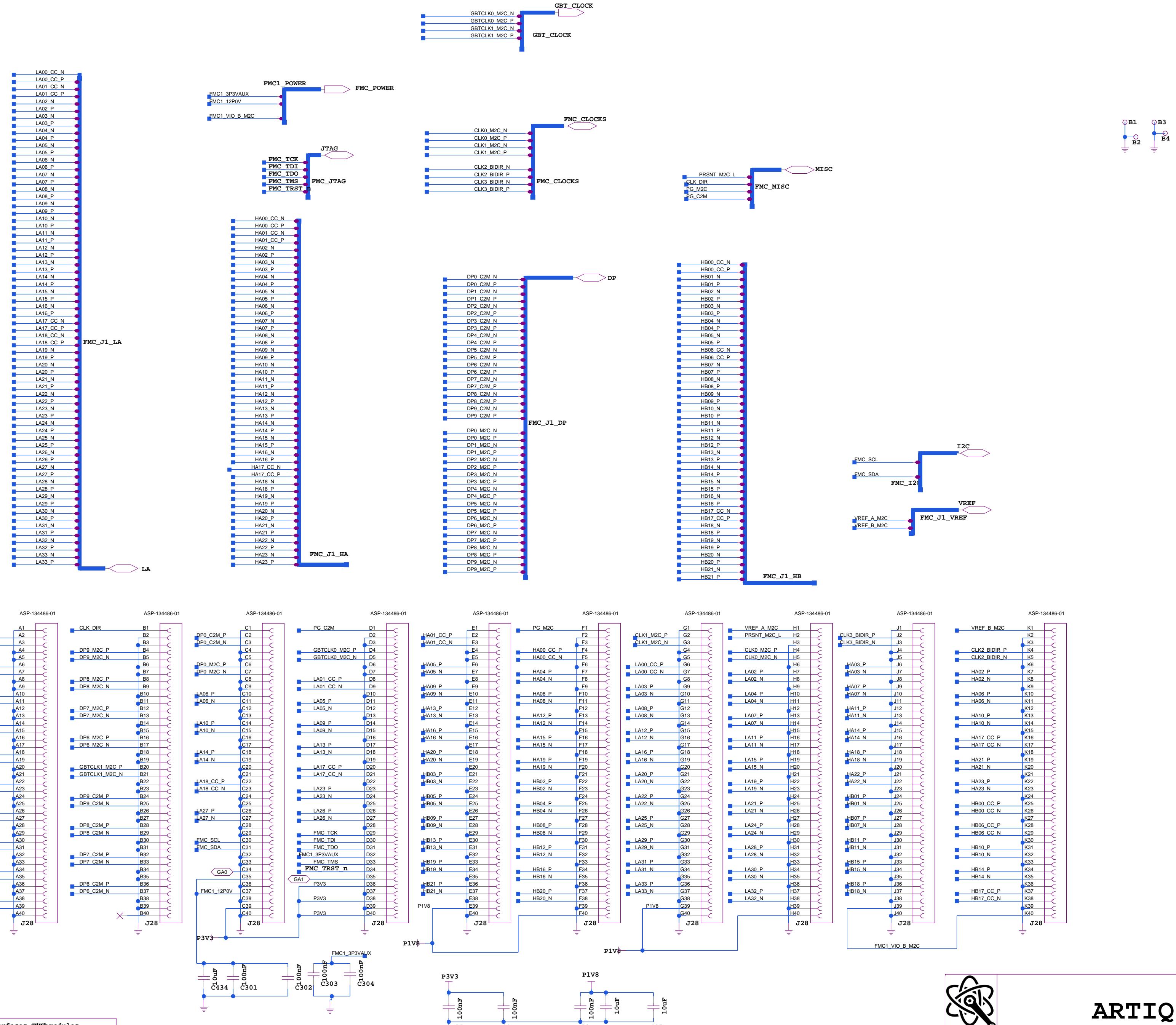
ARTIQ Sinara

M-LVDS_PHY

SIZE	DWG NO	REV
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G.K.	8	31

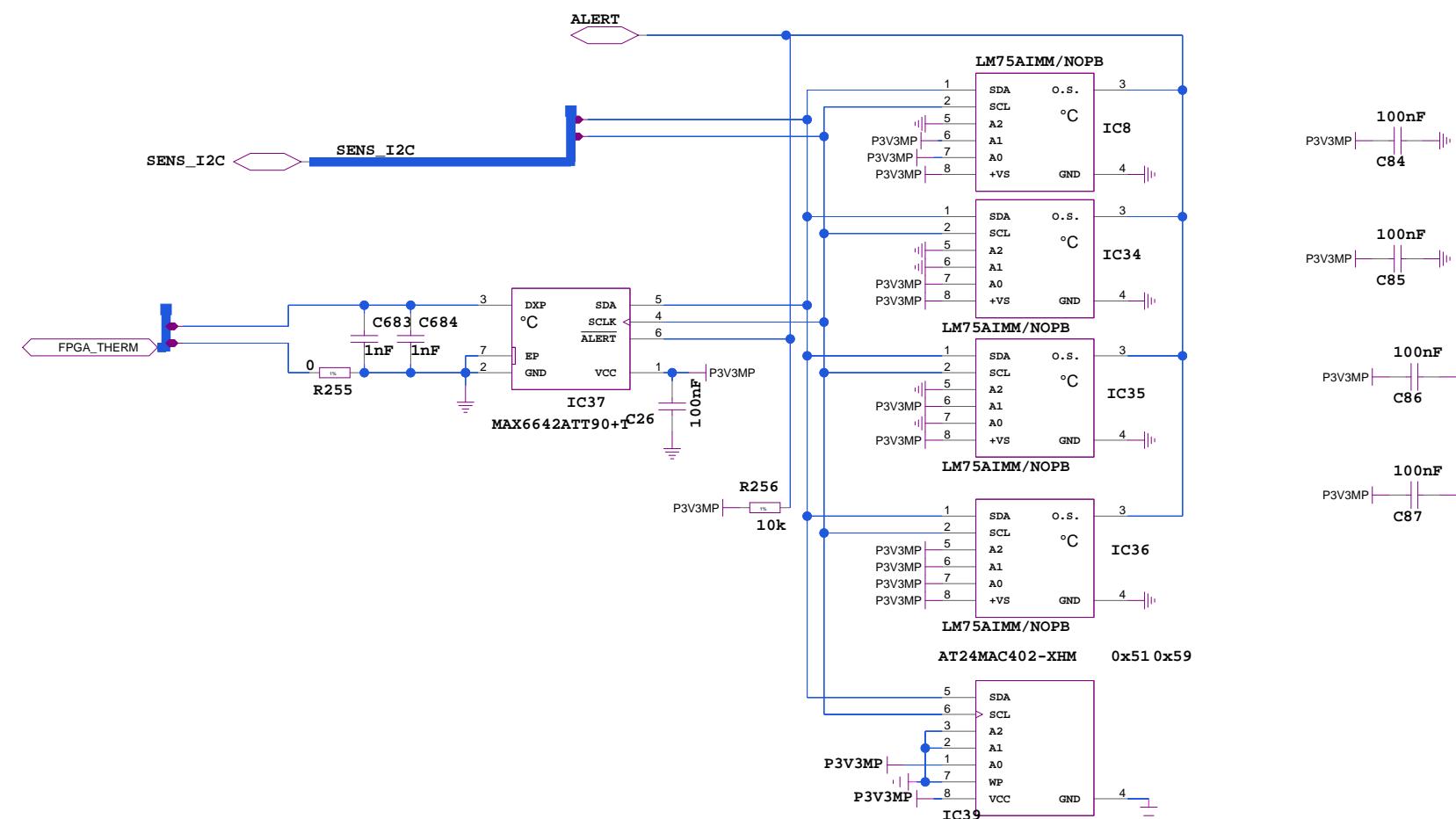
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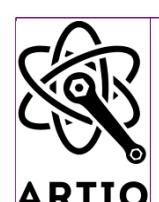


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FMC_connector



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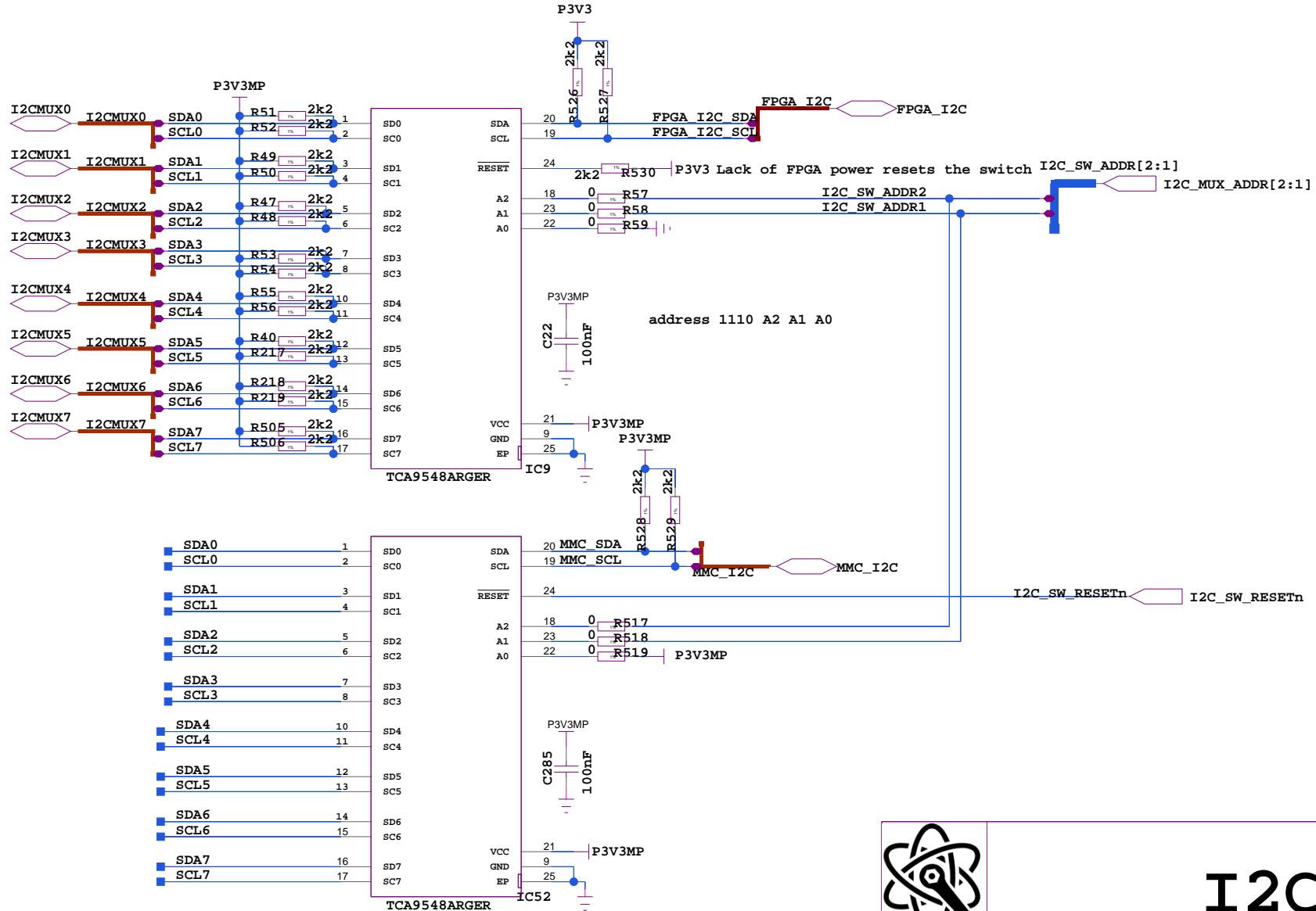


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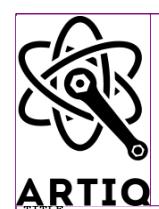
Thermometers

SIZE	DWG NO	REV
A3		v0.97
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I2C switch footprint is compatible with MAX7358 which has interesting anti-lock capabilities



I2C_MUX



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SIZE DWG NO

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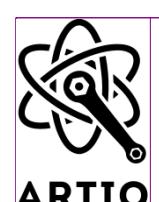
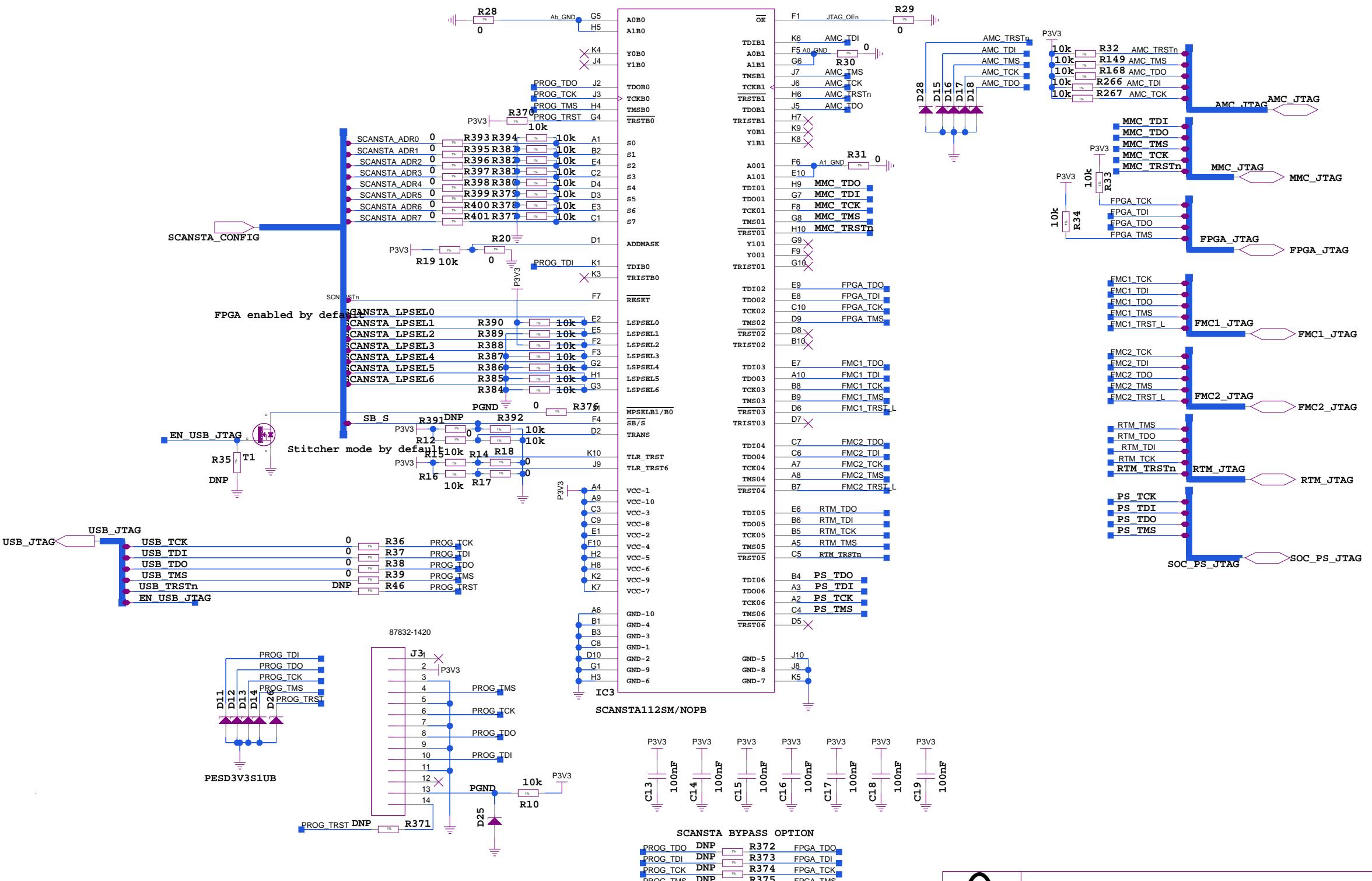
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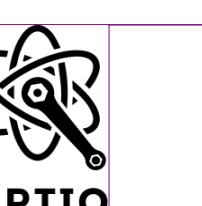
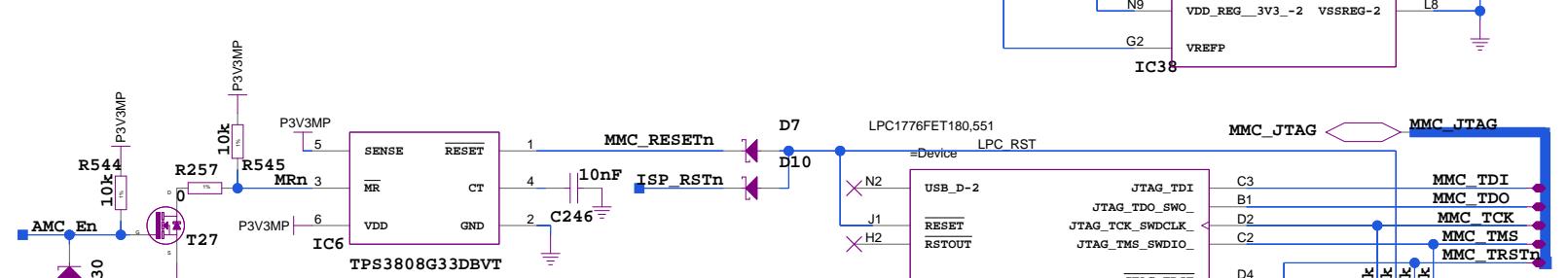
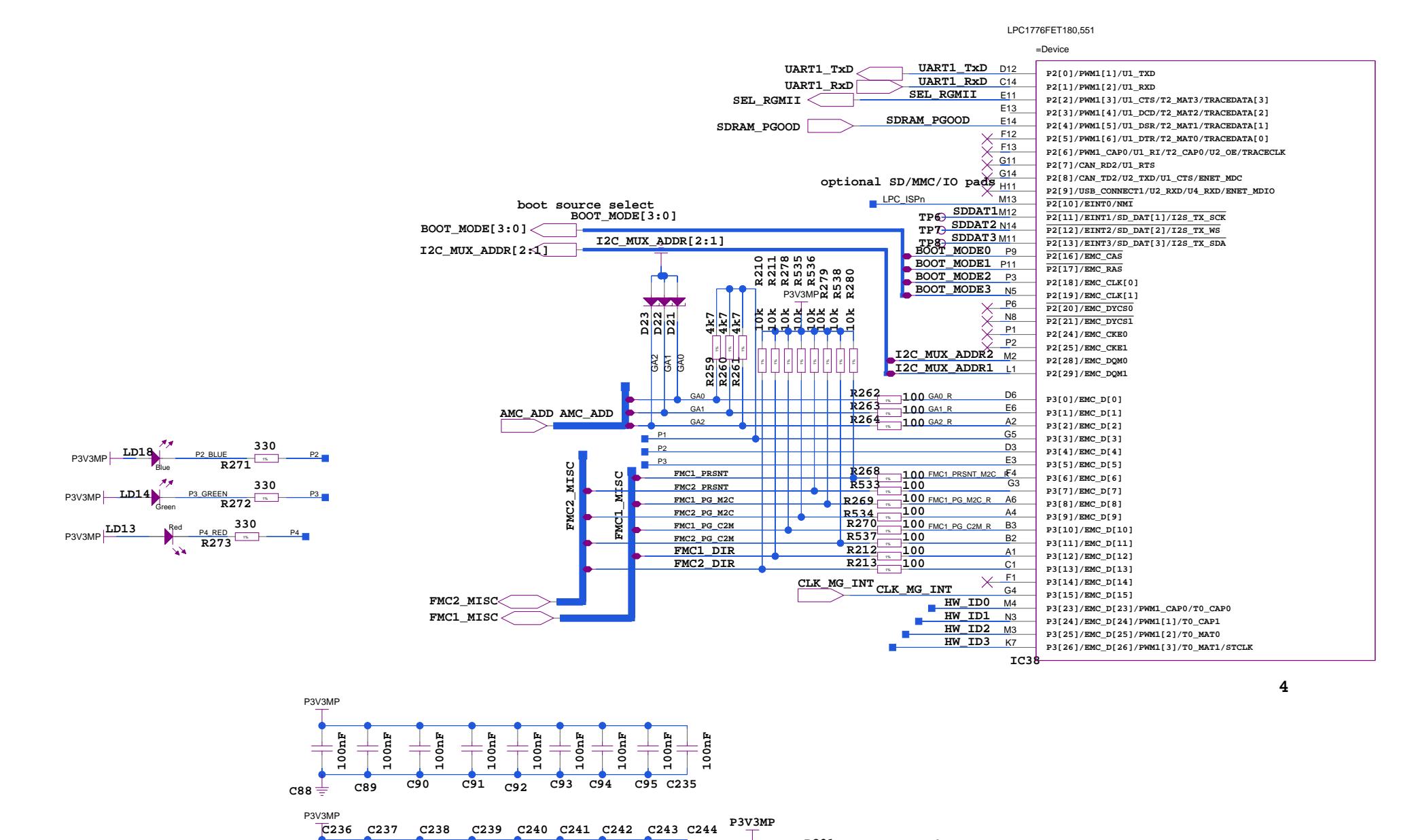
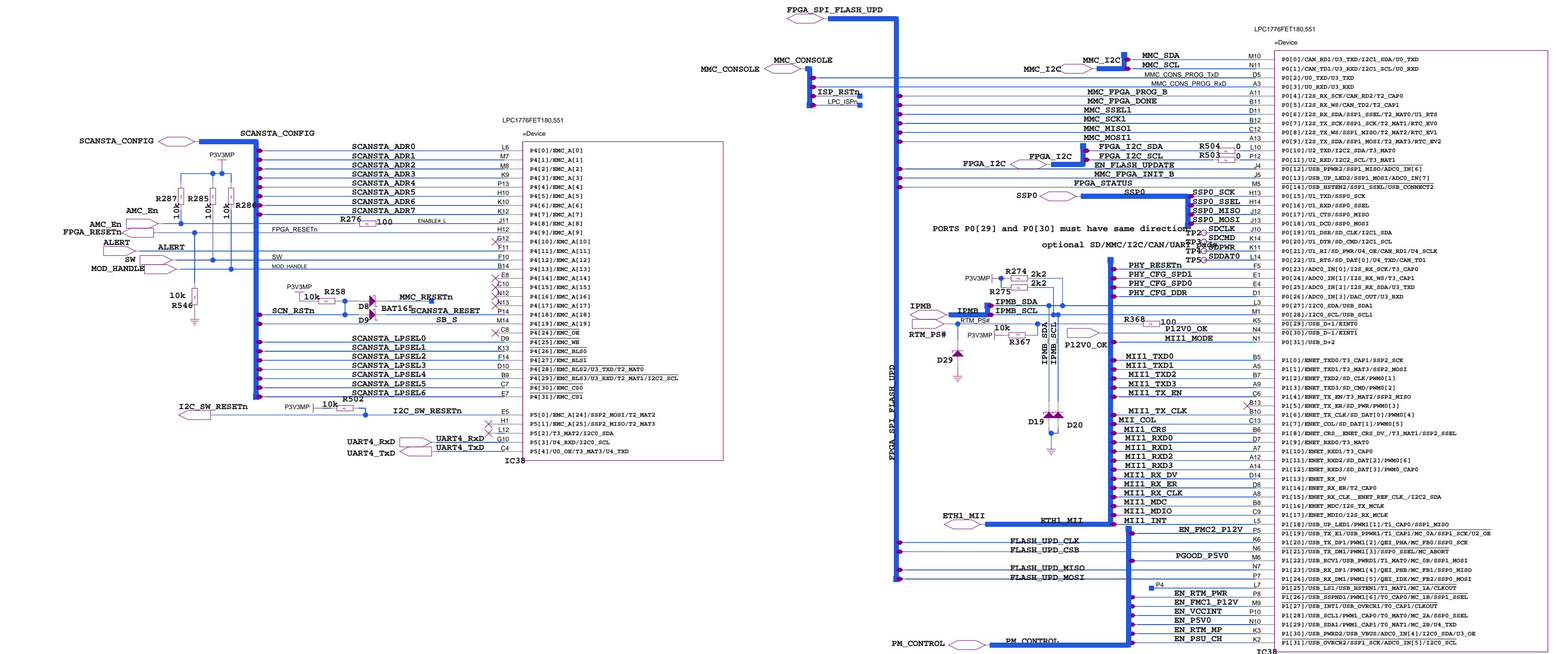
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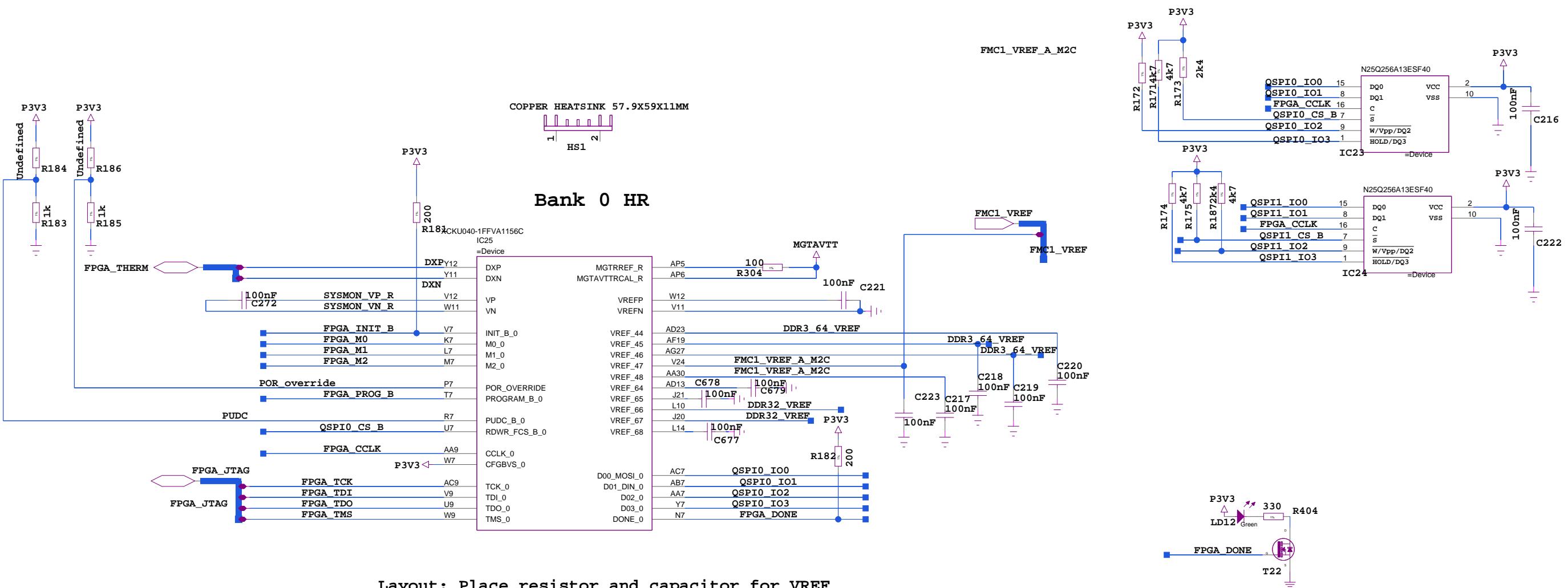
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SIZE	DWG NO	REV
A3		v0.97
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G.K.	13	31

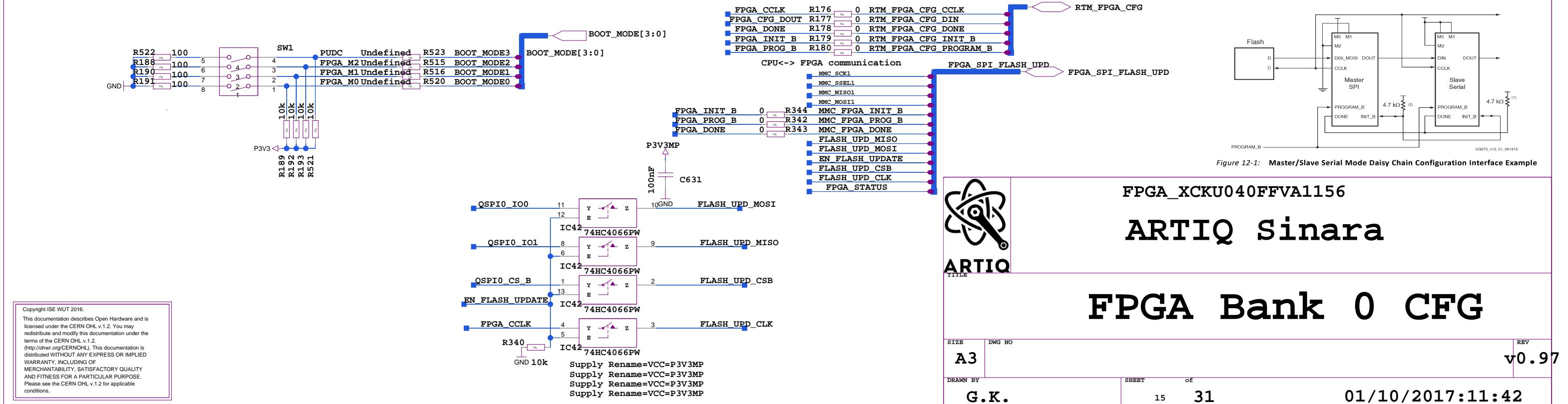


ARTIO Sinara

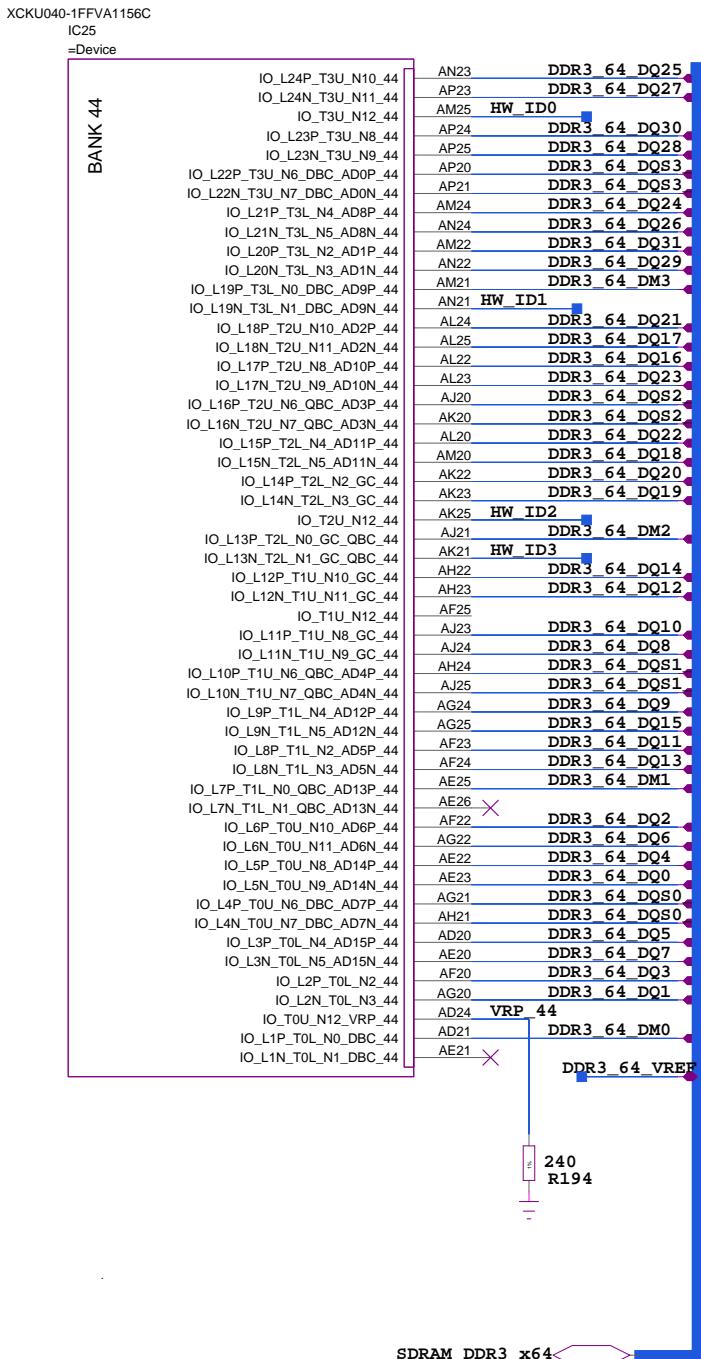
CPU LPC1776



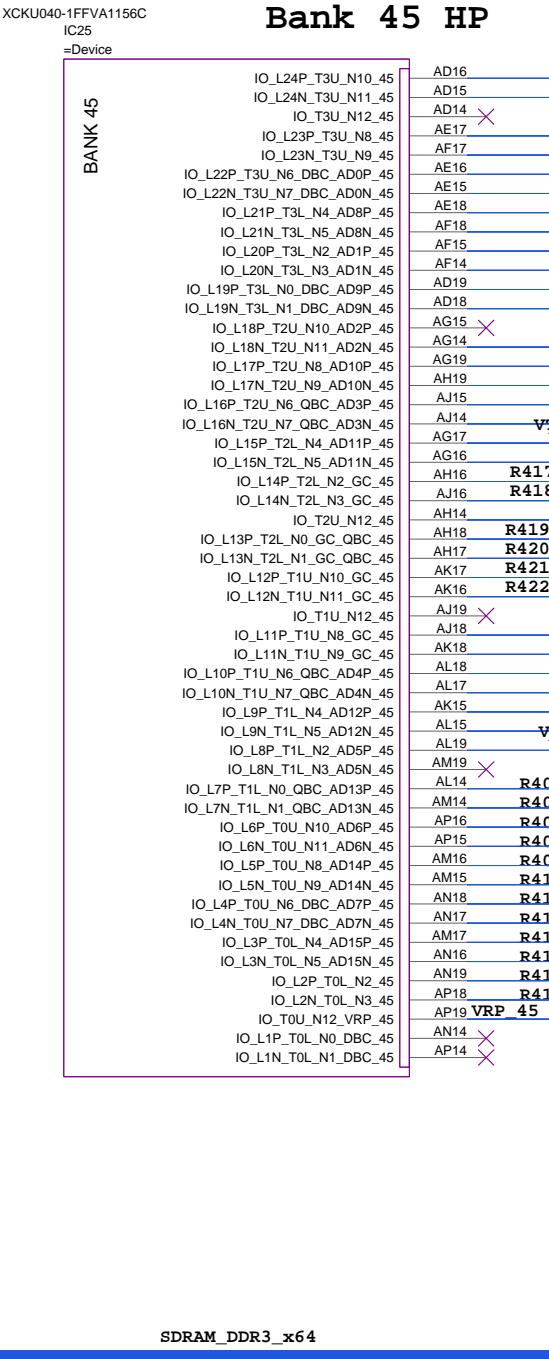
Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via



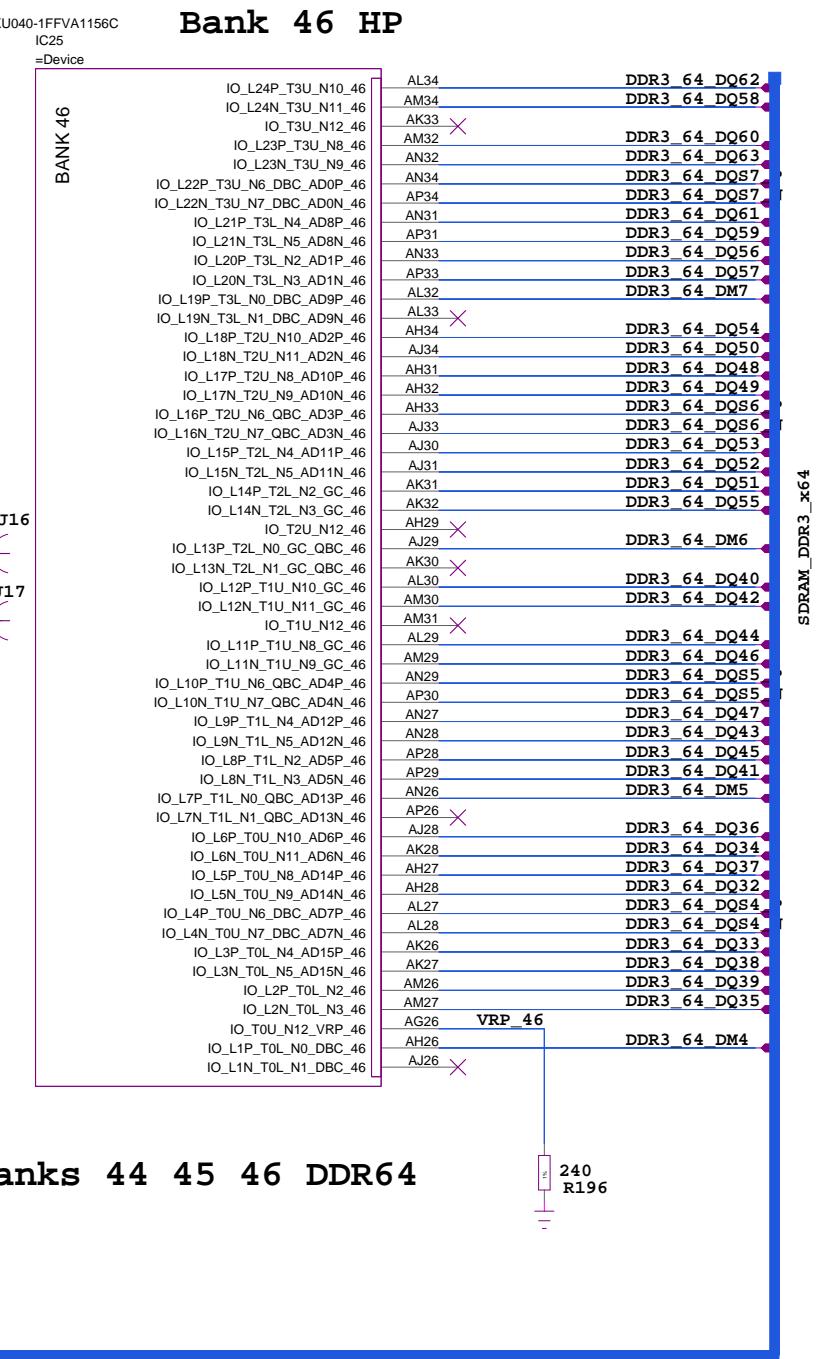
Bank 44 HP



Bank 45 HP

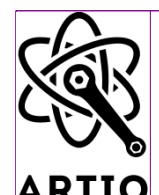


Bank 46 HP



FPGA Banks 44 45 46 DDR64

FPGA_XCKU040FFVA1156



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FPGA Banks 44 45 46 DDR64

SIZE DWG NO

A3

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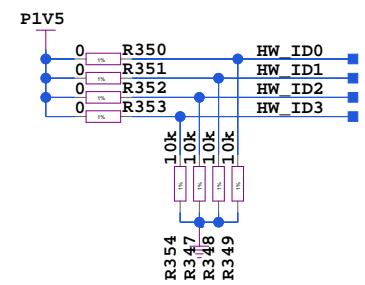
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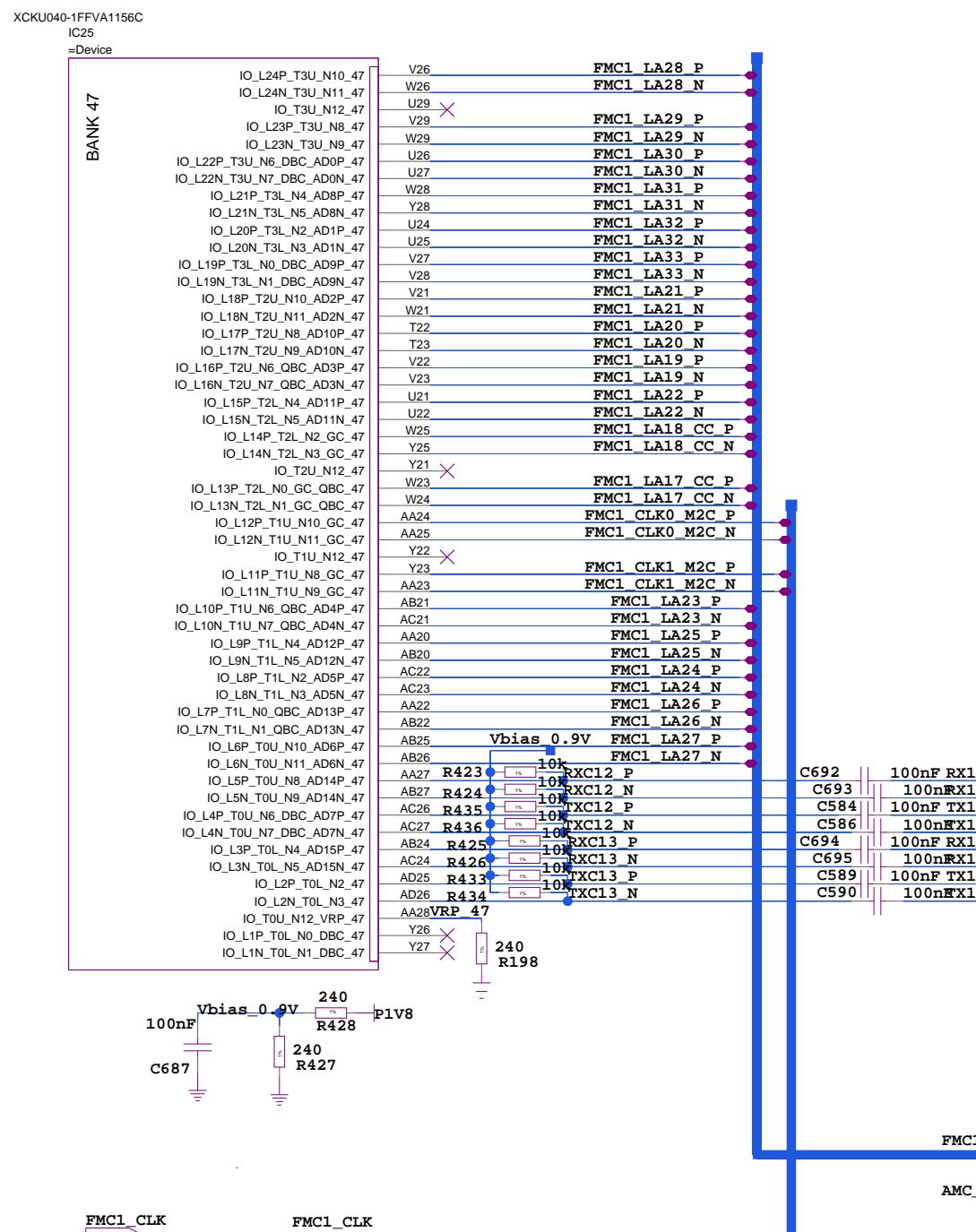
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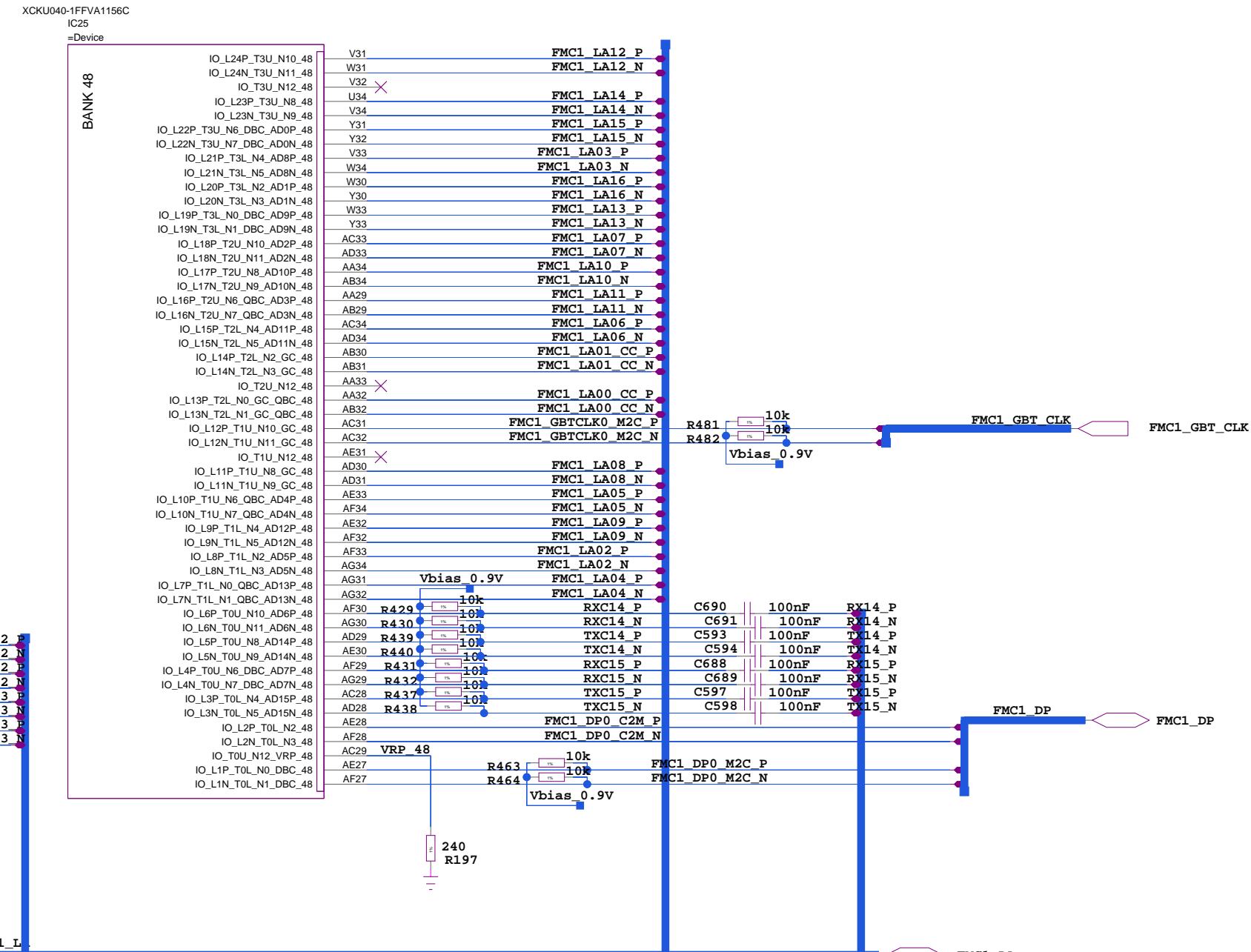


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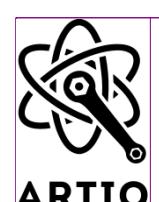
Bank 47 HP



Bank 48 HP



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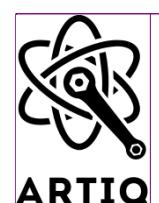
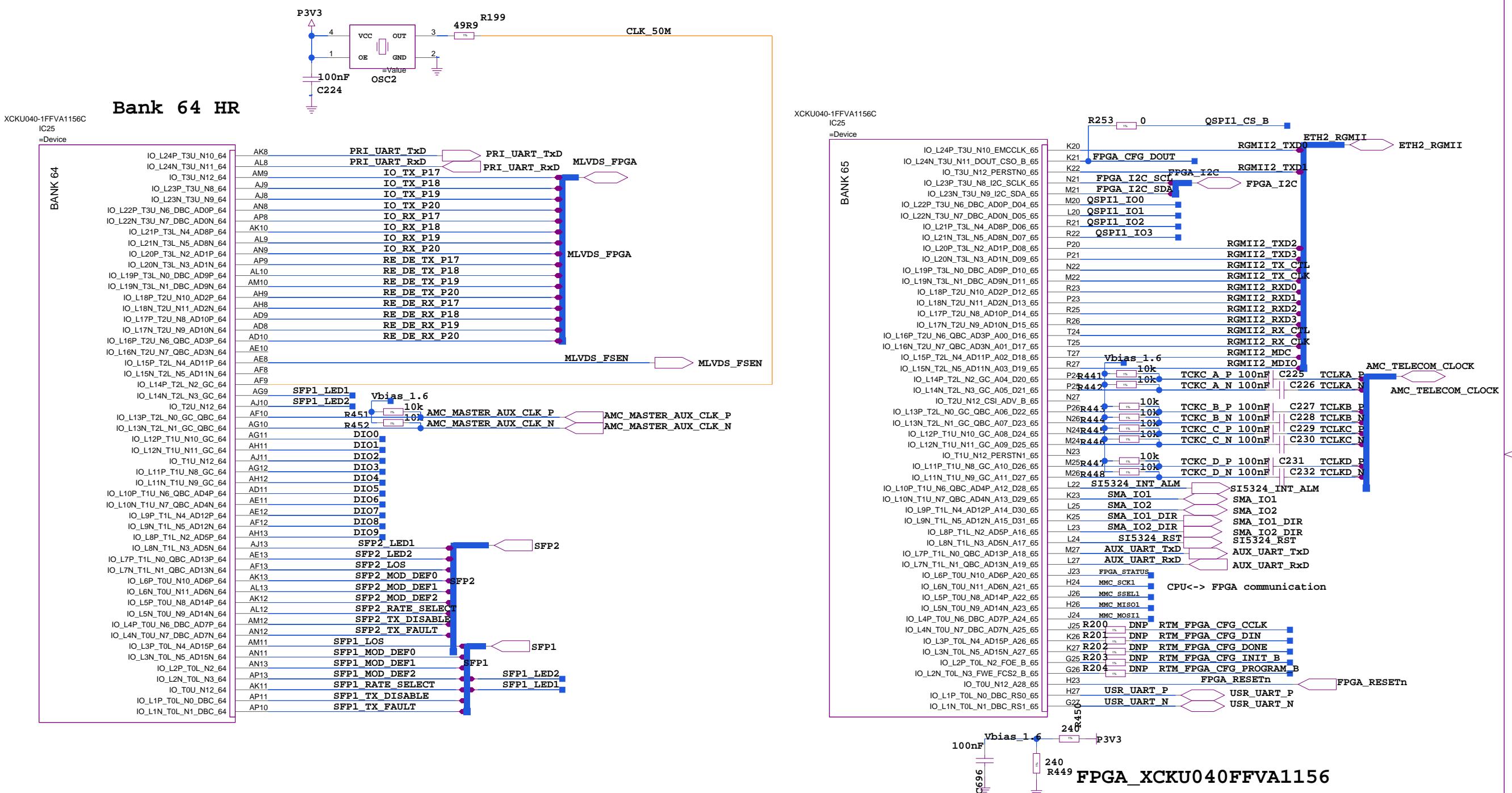


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FPGA Banks 47 48 HP FM

SIZE	DWG NO	REV
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Bank 65 HI



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FPGA Banks 64 65 HR

SIZE DWG NO

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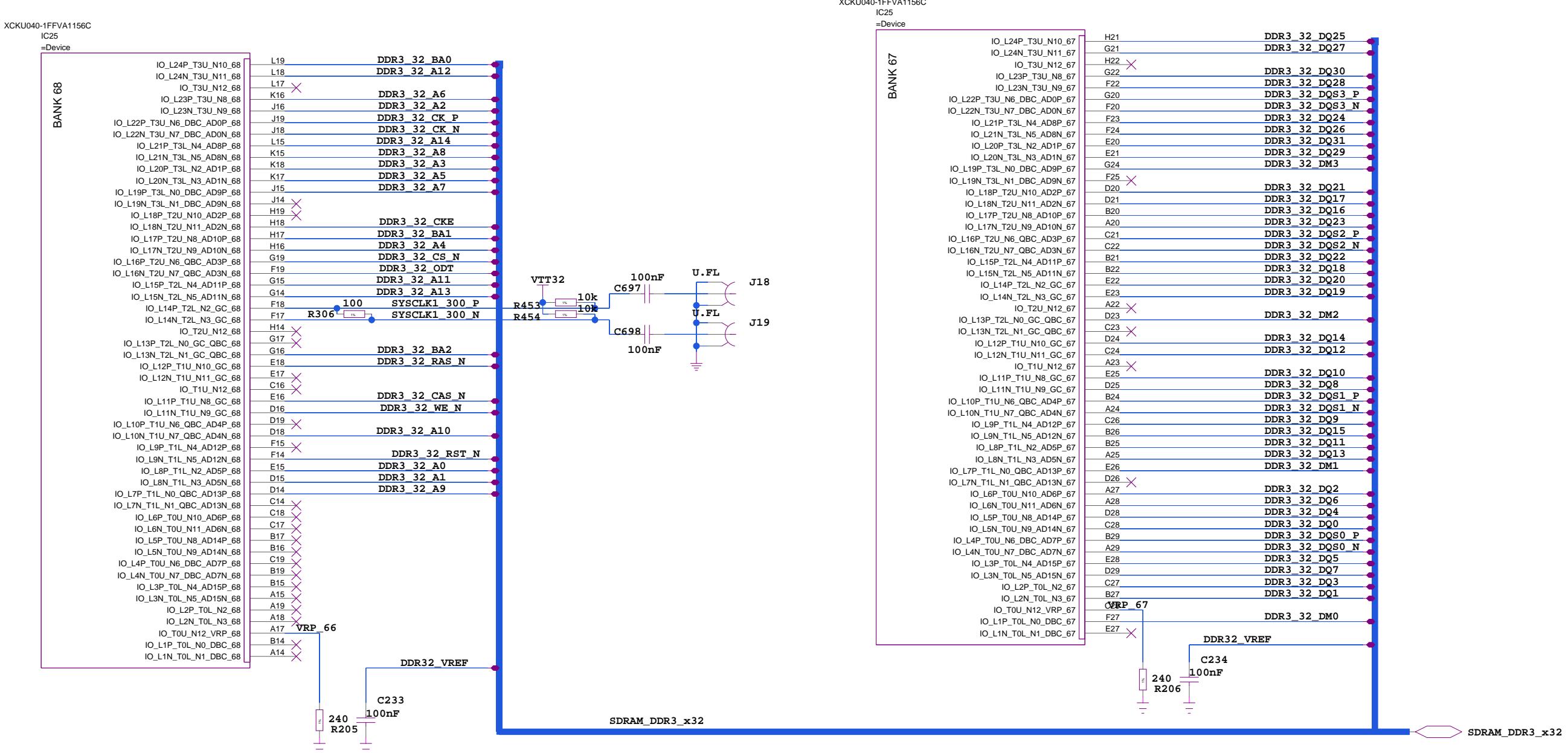
Page 1 of 1

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Bank 68 HP Underneath the FPGA via array right next to the via

Bank 67 HE



FPGA Banks 67 68 DDR32

FPGA_XCKU040FFVA1156

ARTIQ Sinara

FPGA Banks 67 68 DDR3

WG NO

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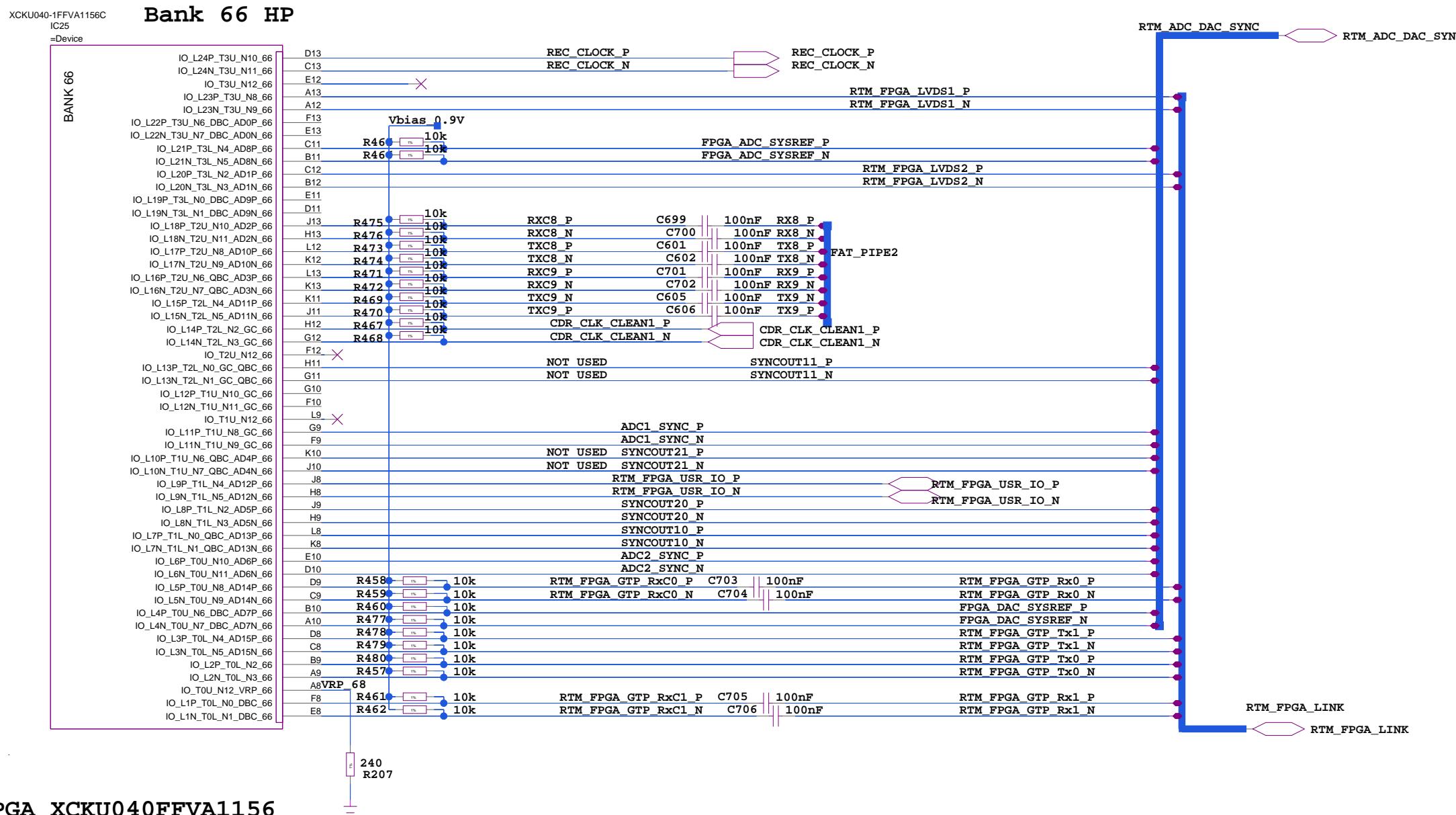
3

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Layout: Place resistor and capacitor for VREF

Vbias_0.9V

Underneath the FPGA via array
right next to the via

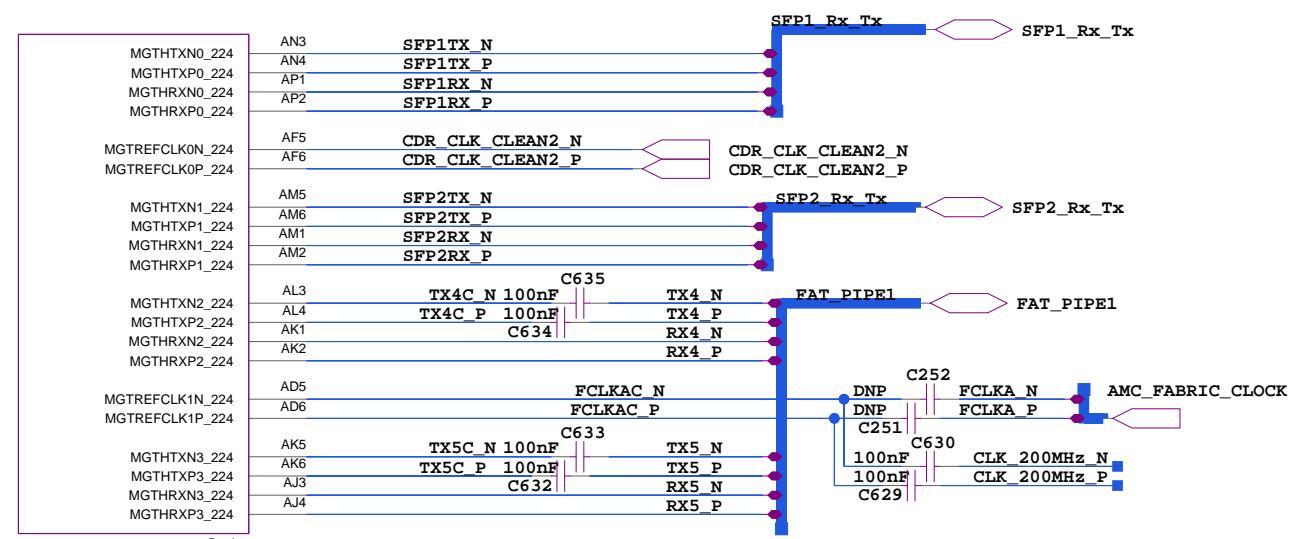
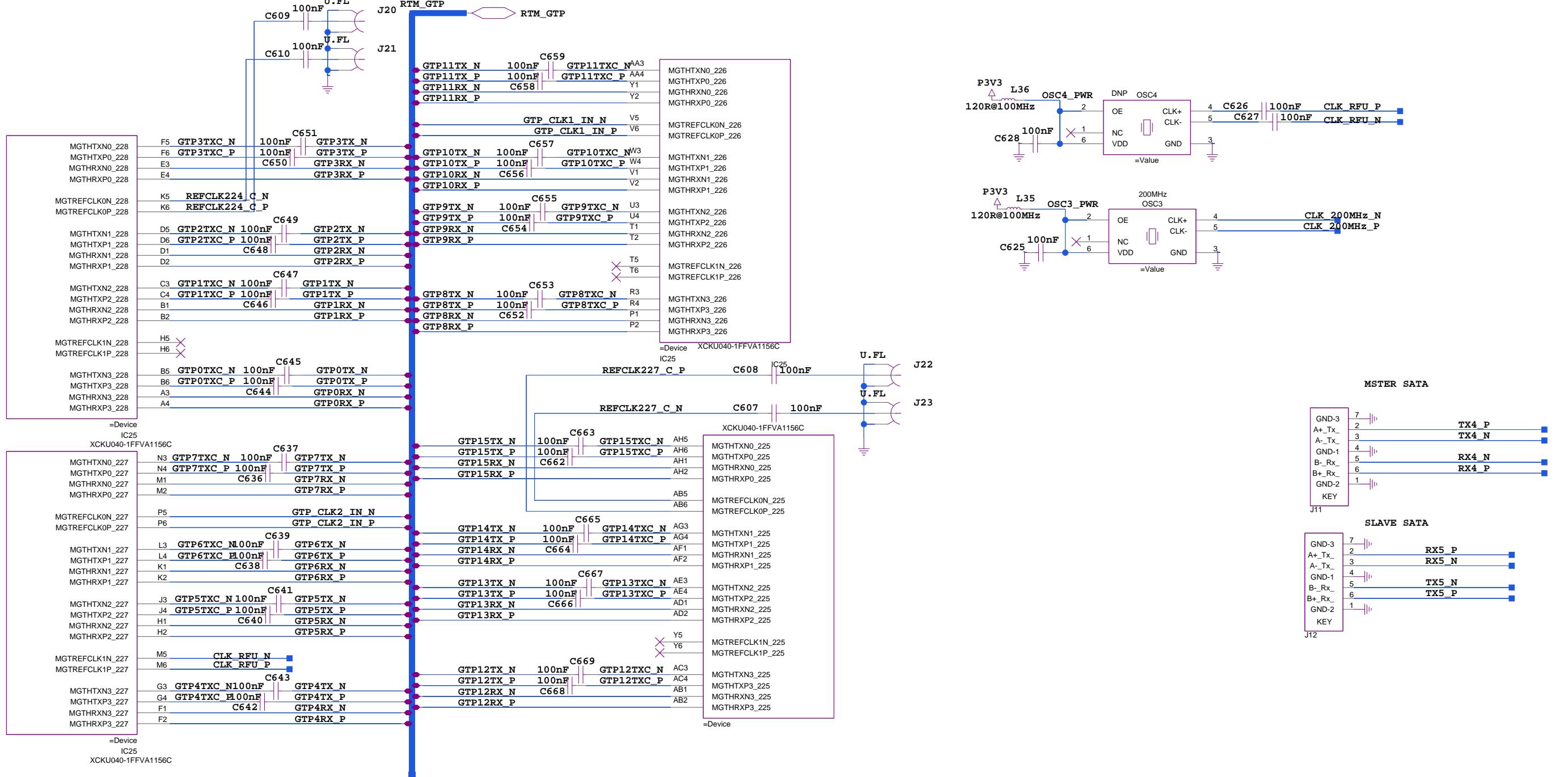


FPGA Bank 66 HF

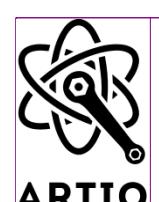
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FPGA Bank 66 HP

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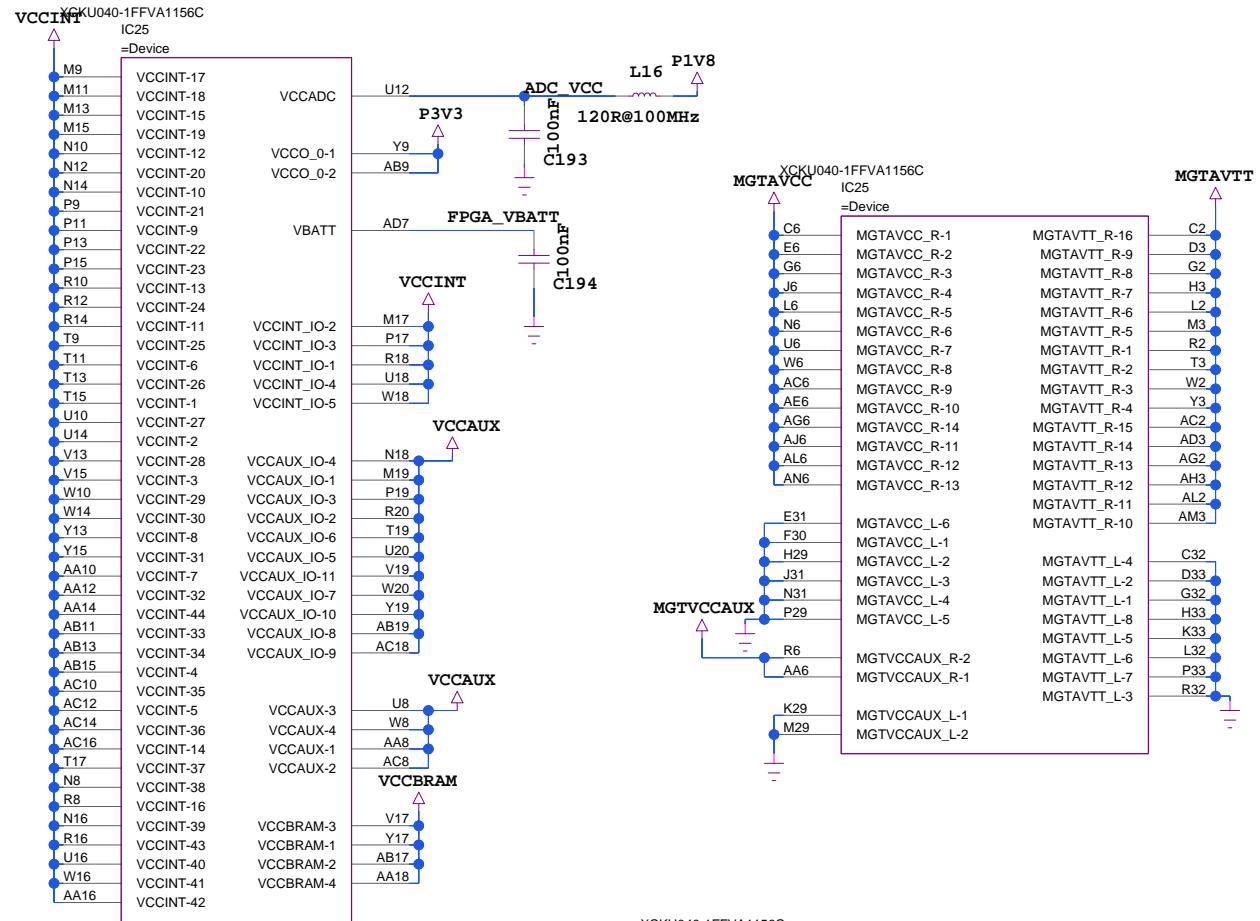


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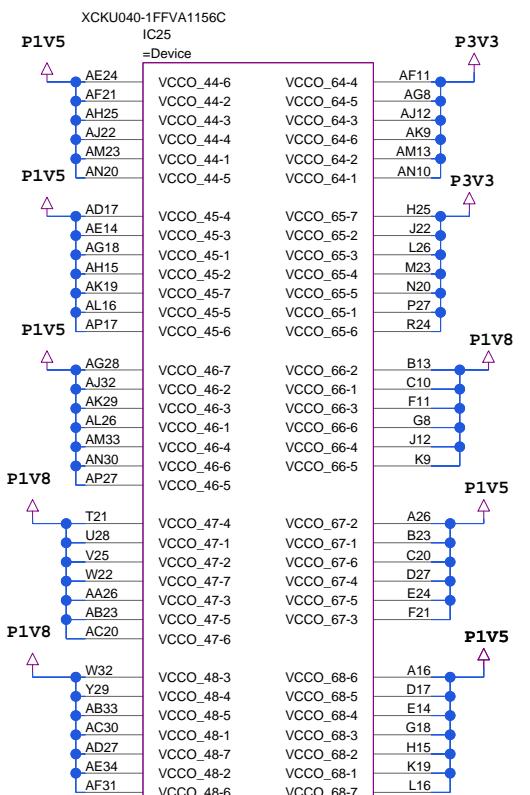


FPGA Banks 224 225 226 22

ARTIQ Sinara



Power Supply		
Source	Voltage	Total (A)
V _{CCINT}	0.900	9.165
V _{CCINT_IO}	0.900	0.620
V _{CCBRAM}	0.950	0.031
V _{CCAUX}	1.800	0.660
V _{CCAUX_IO}	1.800	0.546
V _{CCO 3.3V}	3.300	0.000
V _{CCO 2.5V}	2.500	
V _{CCO 1.8V}	1.800	0.380
V _{CCO 1.5V}	1.500	0.936
V _{CCO 1.35V}	1.350	
V _{CCO 1.2V}	1.200	
V _{CCO 1.0V}	1.000	
MGT _{VCCAUX}	1.800	0.081
MGT _{AV_{CC}}	1.000	3.038
MGT _{AV_{TT}}	1.200	0.592
V _{CCADC}	1.800	0.014



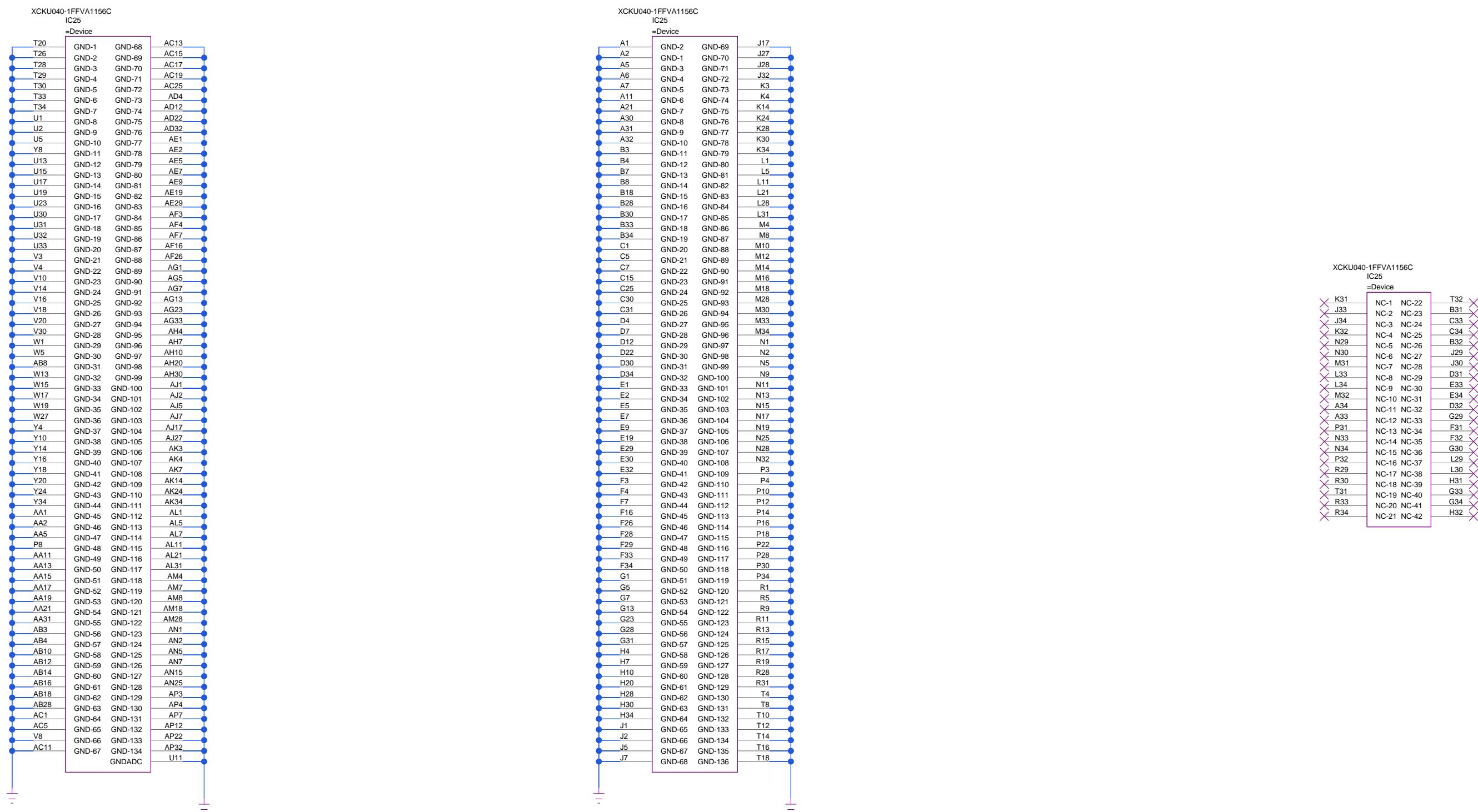
FPGA Power

FPGA_XCKU040FFVA1156

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FPGA Power

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FPGA_XCKU040FARMAQ1s6ara
ARTIQ

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FPGA GND NC

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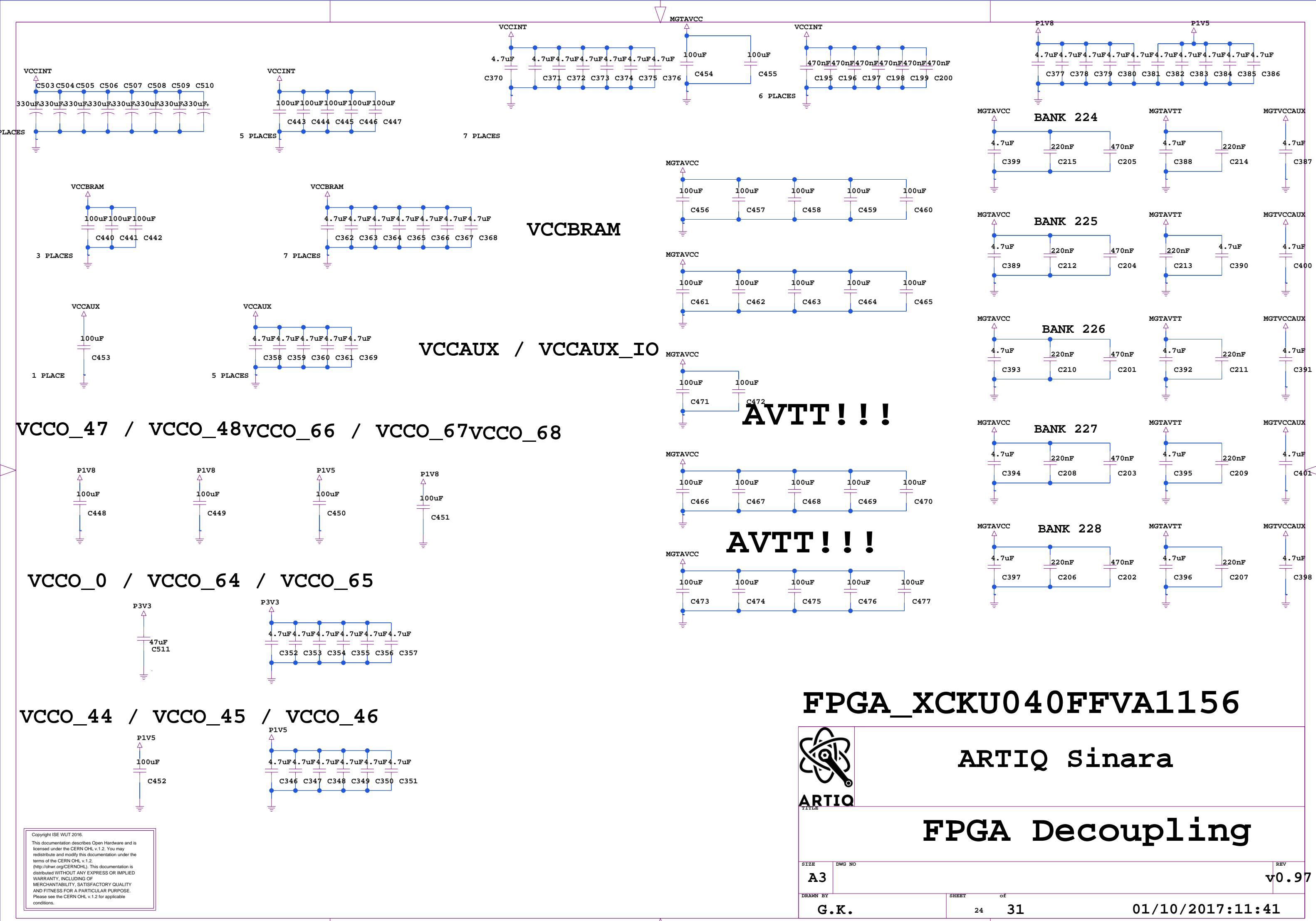
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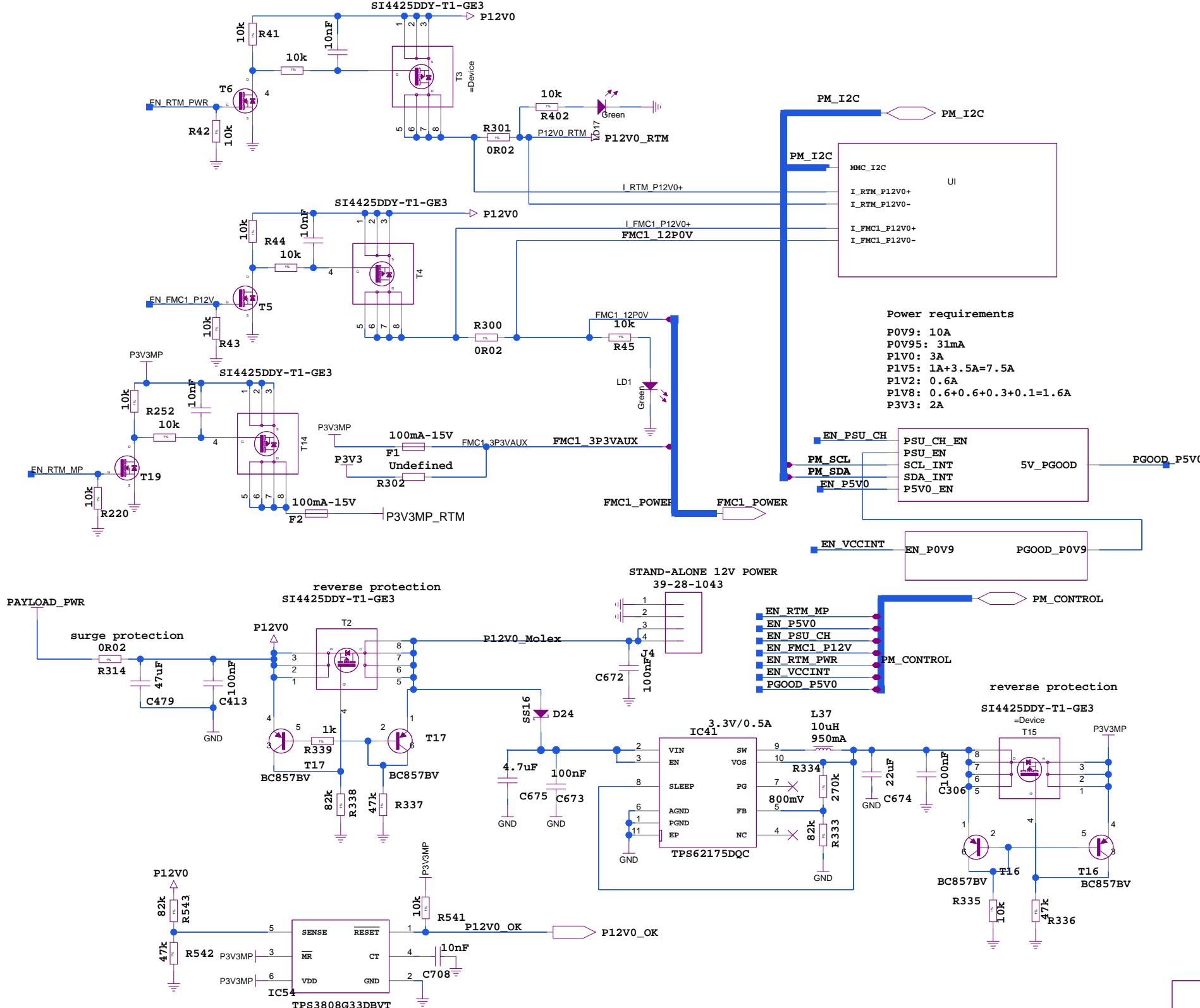
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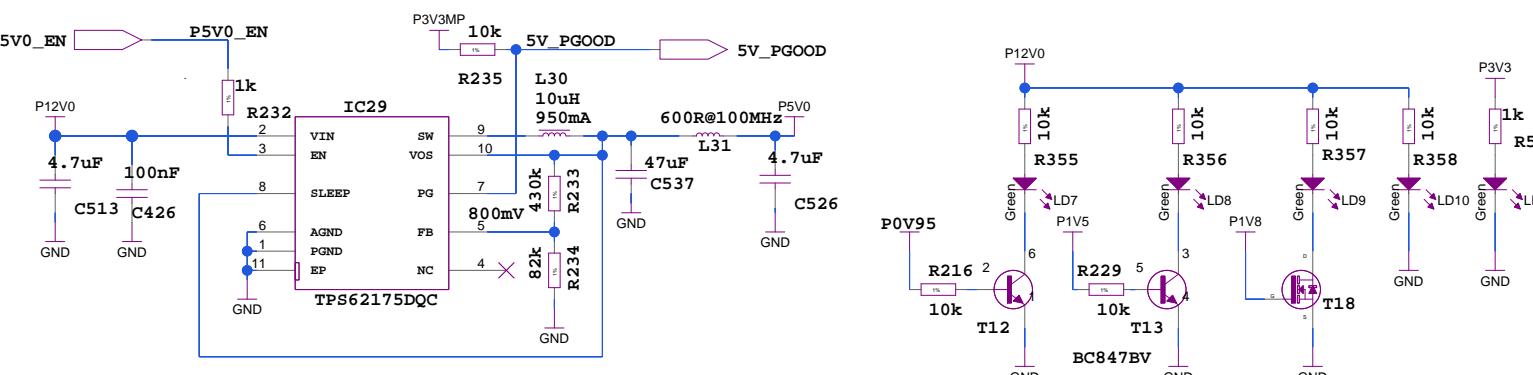
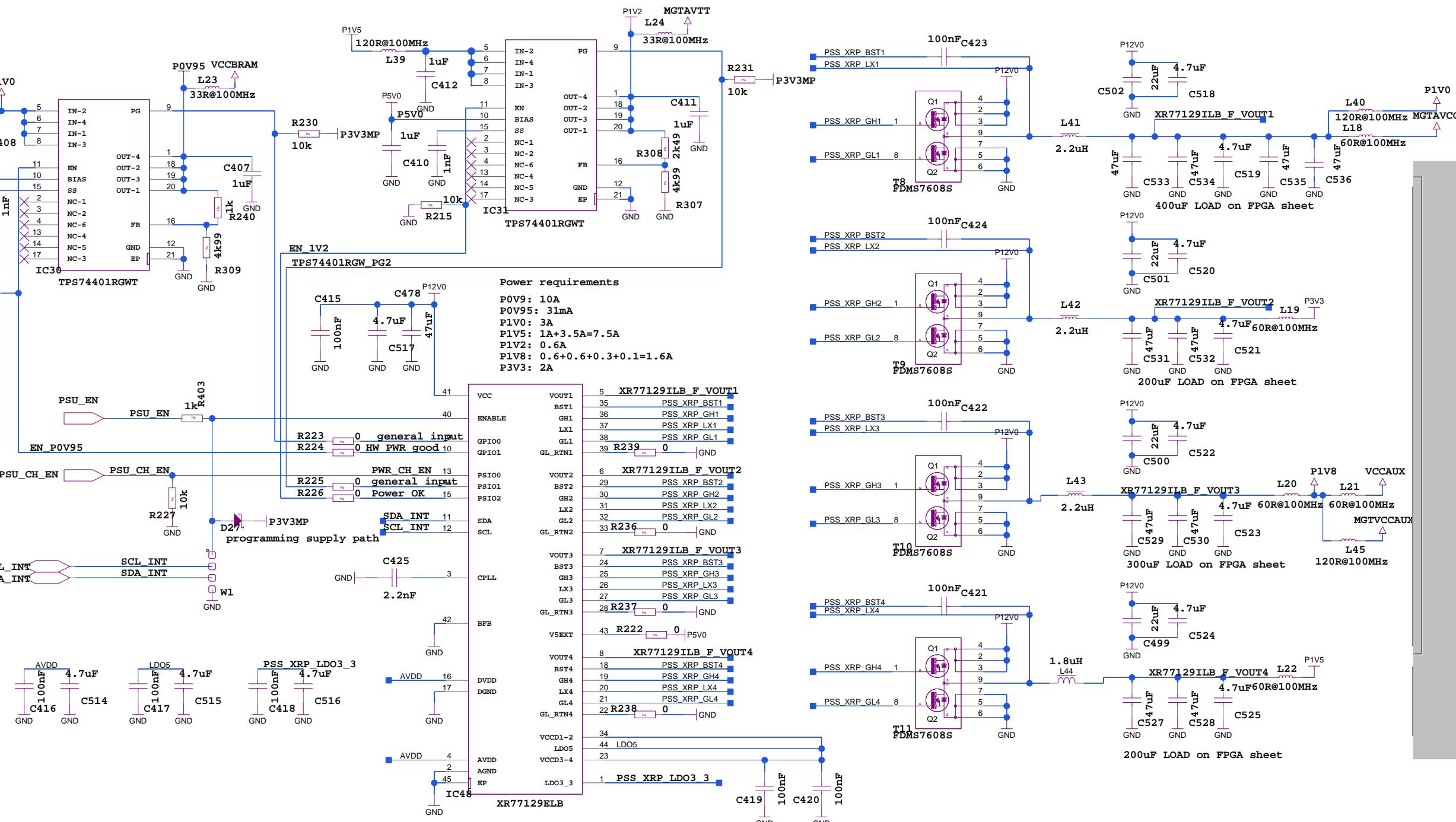
Power Supply		
Source	Voltage	Total (A)
V _{CCINT}	0.900	9.165
V _{CCINT_IO}	0.900	0.620
V _{CCBRAM}	0.950	0.031
V _{CCAUX}	1.800	0.660
V _{CCAUX_IO}	1.800	0.546
V _{CCO 3.3V}	3.300	0.000
V _{CCO 2.5V}	2.500	
V _{CCO 1.8V}	1.800	0.380
V _{CCO 1.5V}	1.500	0.936
V _{CCO 1.35V}	1.350	
V _{CCO 1.2V}	1.200	
V _{CCO 1.0V}	1.000	
MGTAV _{CCAUX}	1.800	0.081
MGTAV _{CC}	1.000	3.038
MGTAV _{TT}	1.200	0.592
-	-	
-	-	
V _{CCADC}	1.800	0.014

The recommended power-on sequence is VCCINT/VCCINT_IO, VCCBRAM, VCCAUX/VCCAUX_IO, and VCCO to achieve minimum current draw and ensure that the 1/0s are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCINT/VCCINT_IO and VCCO have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. If VCCAUX/VCCAUX_IO and VCCO have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. VCCAUX and VCCO must be connected together. When the current minimums are met, the device powers on after the VCCINT/VCCINT_IO, VCCBRAM, VCCAUX/VCCAUX_IO, and VCCO supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after VCCINT is applied. VCCADC and VREF can be powered at any time and have no power-up sequencing recommendations. The recommended power-on sequence to achieve minimum current draw for the GTH or GTx transceivers is VCCINT, VMGTAVCC, VMGTAVT, VMGTAVTT, VCCINT, VMGTAVTT. There is no recommended sequencing for VMGTAVCC. Both VMGTAVC and VCCINT can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from VMGTAVTT can be higher than specifications during power-up and power-down.

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POWER Management

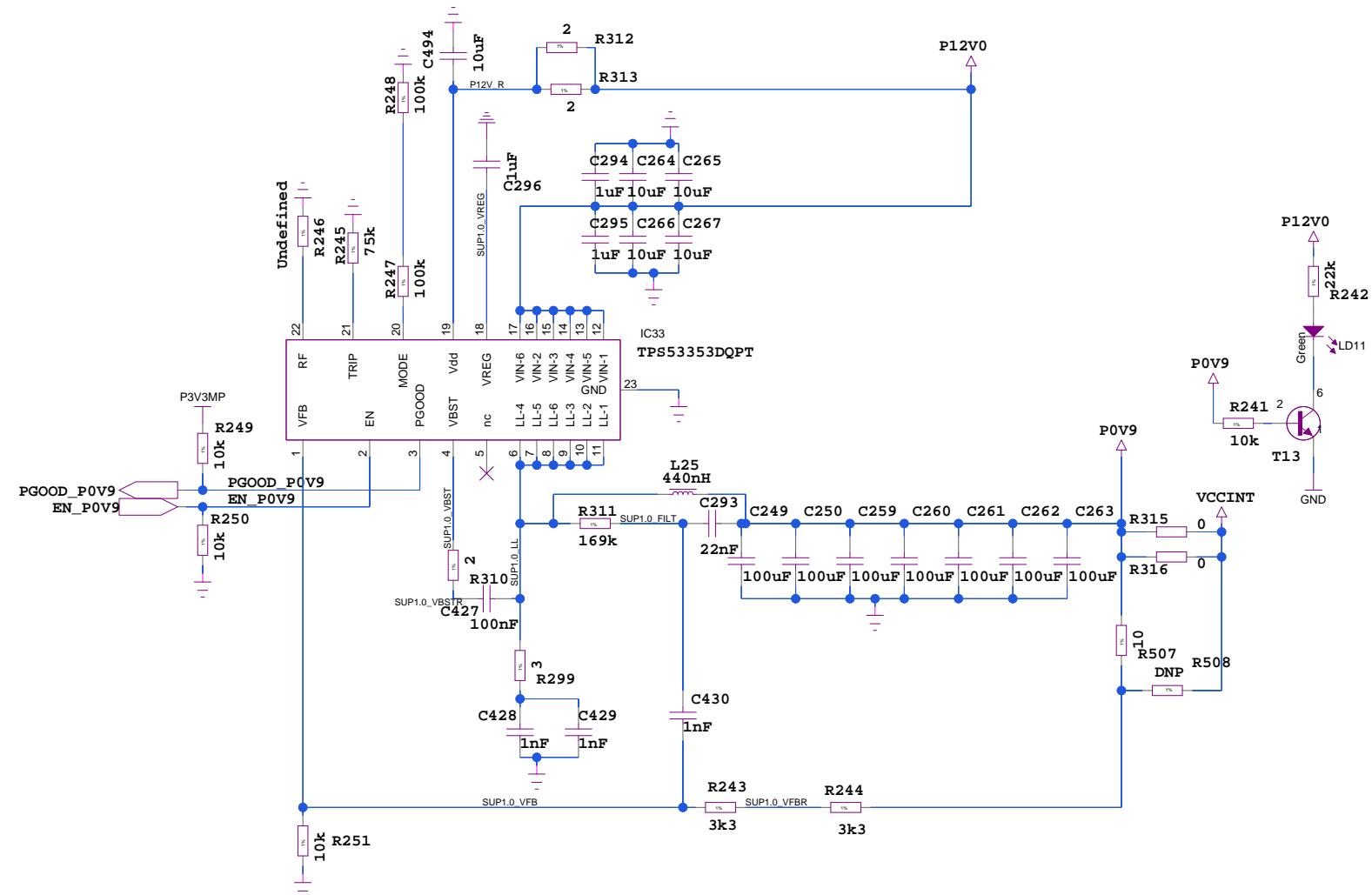
Power Supply		
Source	Voltage	Total (A)
V_{CCINT}	0.900	9.165
V_{CCINT_IO}	0.900	0.620
V_{CCBRAM}	0.950	0.031
V_{CCAUX}	1.800	0.660
V_{CCAUX_IO}	1.800	0.546
$V_{CCO} 3.3V$	3.300	0.000
$V_{CCO} 2.5V$	2.500	
$V_{CCO} 1.8V$	1.800	0.380
$V_{CCO} 1.5V$	1.500	0.936
$V_{CCO} 1.35V$	1.350	
$V_{CCO} 1.2V$	1.200	
$V_{CCO} 1.0V$	1.000	
$MGTVCaux$	1.800	0.081
$MGTAV_{CC}$	1.000	3.038
$MGTAV_{TT}$	1.200	0.592
V_{CCADC}	1.800	0.014
-	-	
-	-	
-	-	
-	-	
-	-	



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PWR_DC_DC_EXAR



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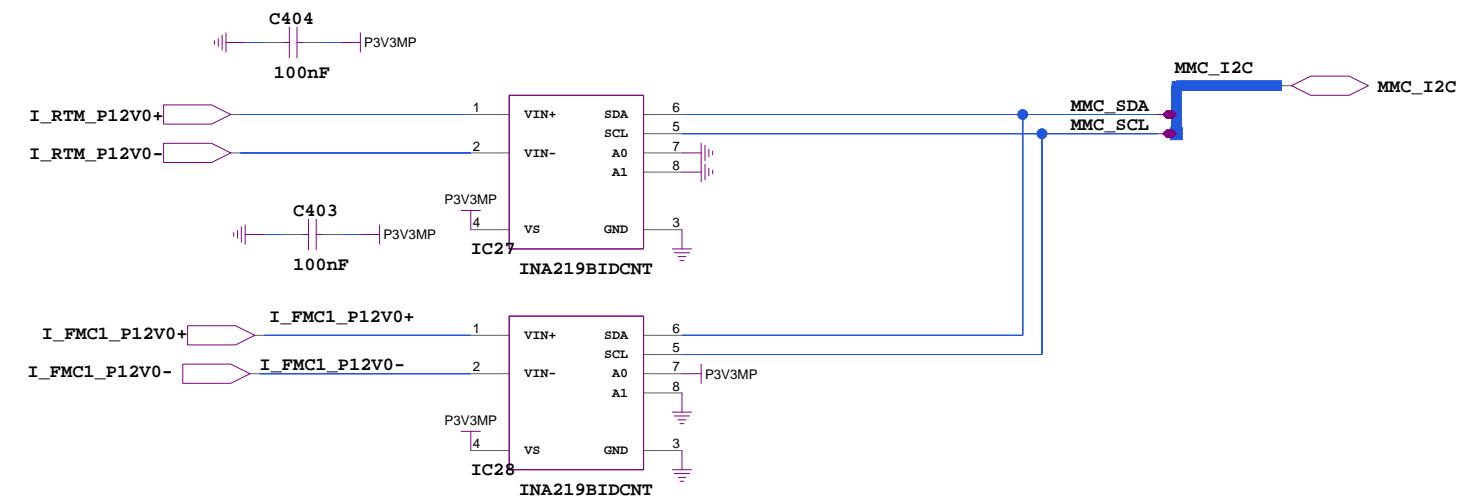
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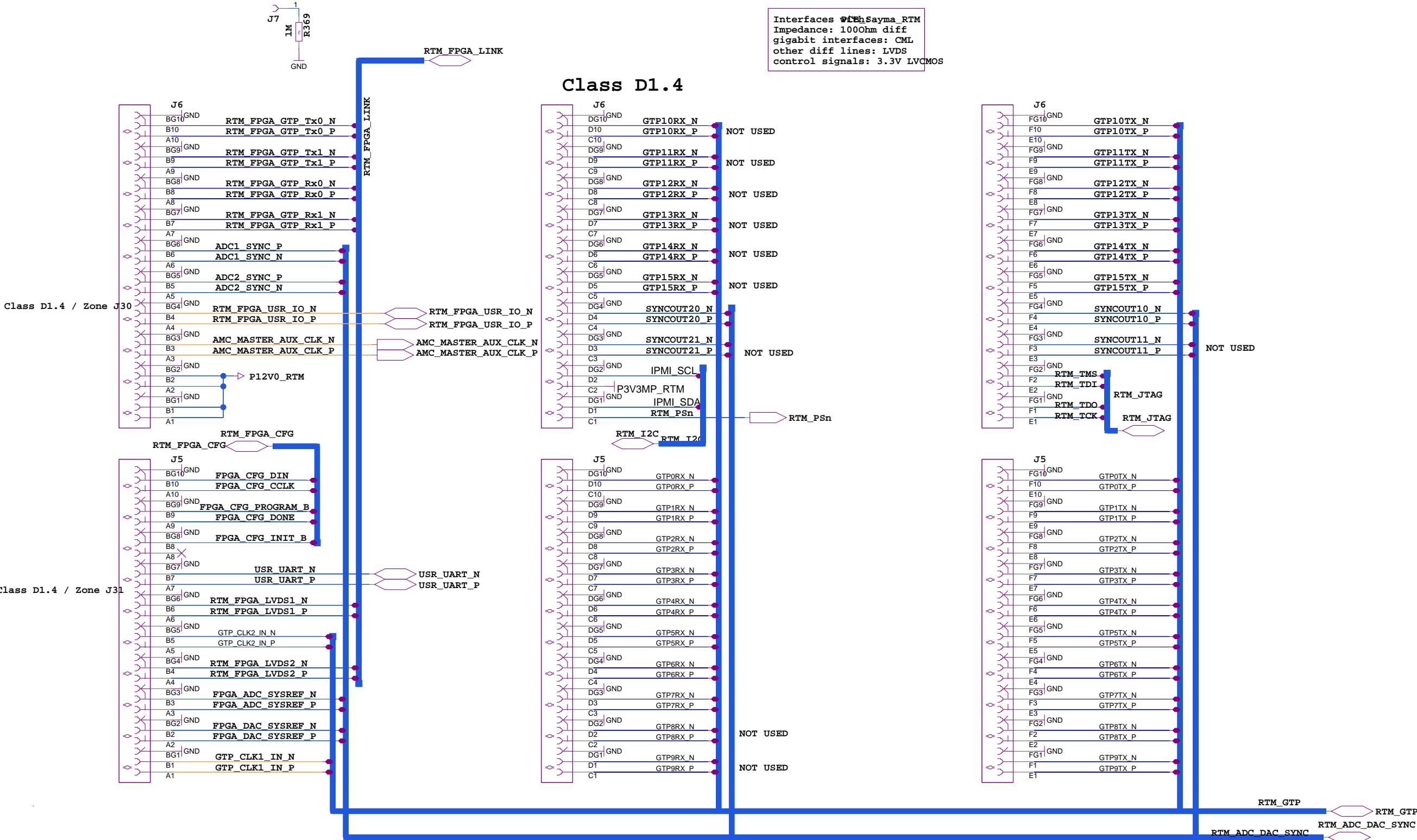


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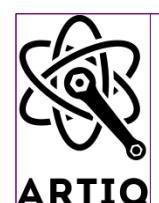
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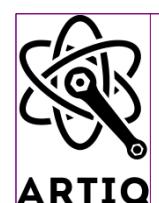
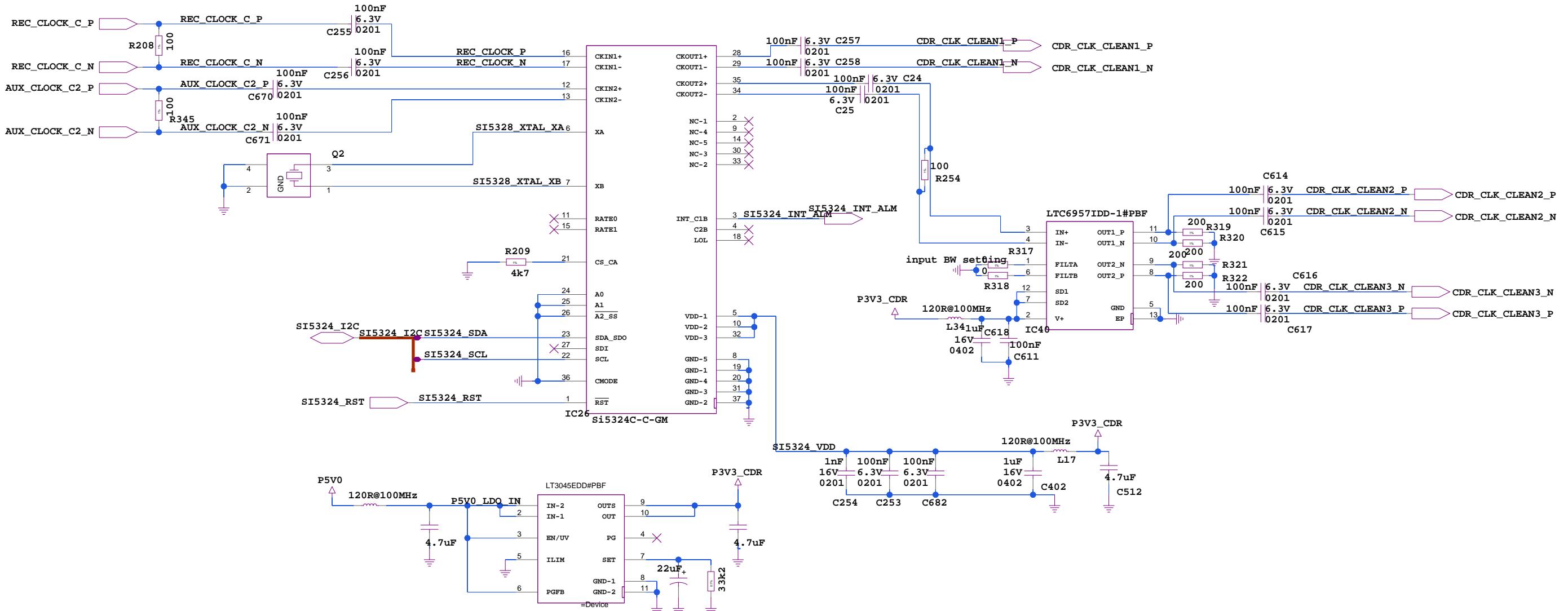
Class D1.4 / Zone	a	b	c	d	e	f
MTCA.4 management	1 PWR A1	PWR B1	PS#	SDA	TCK	TDO
	2 PWR A2	PWR B2	MP	SCL	TDI	TMS
	3 AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
	4 AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
	5 P30_IO+ / CC*	P30_IO+ / CC*	GTP15_RX+	GTP15_RX-	GTP15_TX+	GTP15_TX-
	6 P30_IO+ / CC*	P30_IO+ / CC*	GTP14_RX+	GTP14_RX-	GTP14_TX+	GTP14_TX-
	7 GTP12-15_CLK_IN+	GTP12-15_CLK_IN+	GTP13_RX+	GTP13_RX-	GTP13_TX+	GTP13_TX-
	8 GTP12-15_CLK_OUT+	GTP12-15_CLK_OUT+	GTP12_RX+	GTP12_RX-	GTP12_TX+	GTP12_TX-
	9 P30_IO+ / CC*	P30_IO+ / CC*	GTP11_RX+	GTP11_RX-	GTP11_TX+	GTP11_TX-
	10 P30_IO+ / CC*	P30_IO+ / CC*	GTP10_RX+	GTP10_RX-	GTP10_TX+	GTP10_TX-
Digital clocks fixed IO	1 P30_IO+ / CC*	P30_IO+ / CC*	GTP8-11_CLK_IN+	GTP8-11_CLK_IN-	GTP9_RX+	GTP9_TX+
	2 GTP8-11_CLK_OUT+	GTP8-11_CLK_OUT+	GTP8_RX+	GTP8_RX-	GTP8_TX+	GTP8_TX-
	3 P31_IO+ / CC	P31_IO+ / CC	GTP7_RX+	GTP7_RX-	GTP7_TX+	GTP7_TX-
	4 P31_IO+ / CC	P31_IO+ / CC	GTP6_RX+	GTP6_RX-	GTP6_TX+	GTP6_TX-
	5 GTP4-7_CLK_IN+	GTP4-7_CLK_IN+	GTP5_RX+	GTP5_RX-	GTP5_TX+	GTP5_TX-
	6 GTP4-7_CLK_OUT+	GTP4-7_CLK_OUT+	GTP4_RX+	GTP4_RX-	GTP4_TX+	GTP4_TX-
	7 P31_IO+ / CC*	P31_IO+ / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
	8 P31_IO+ / CC*	P31_IO+ / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
	9 GTP0-3_CLK_IN+	GTP0-3_CLK_IN+	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
	10 GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT+	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-
Standard Gbit-Links						



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RTM_CON

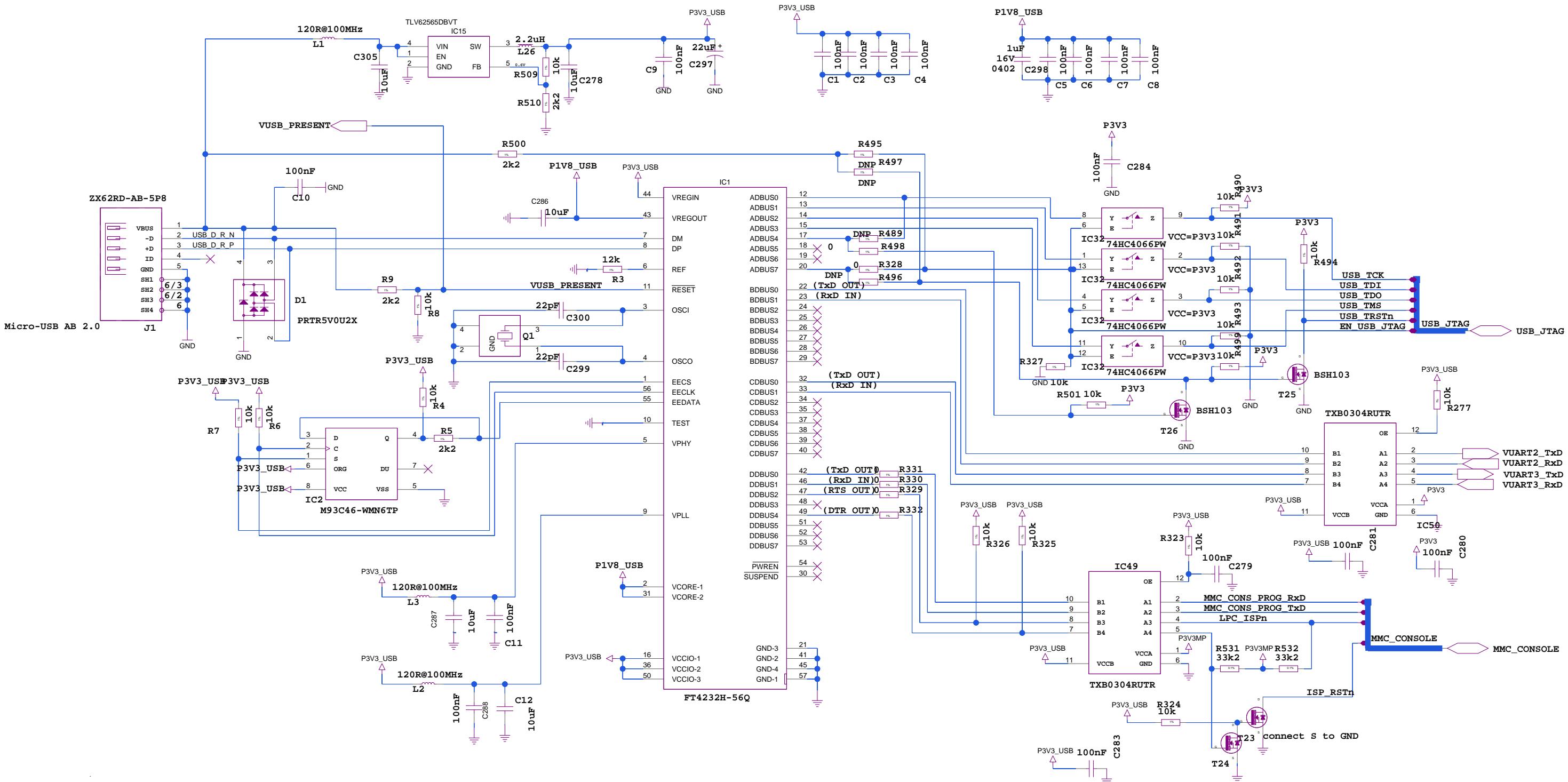
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SI5324_CLK_RECOVERY

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USB_SERIAL_QUAD

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