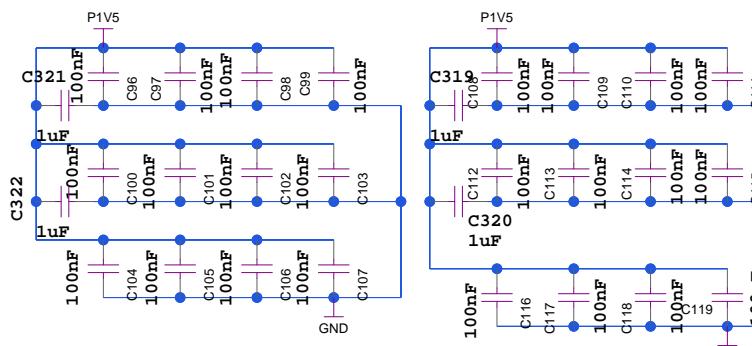
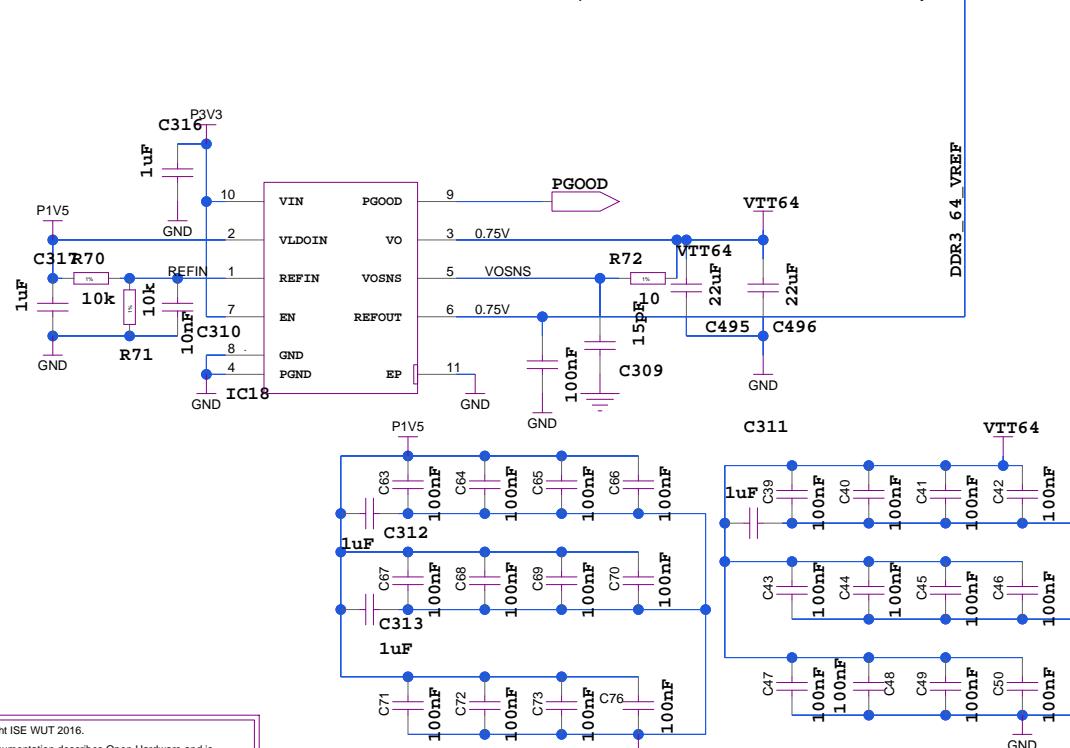




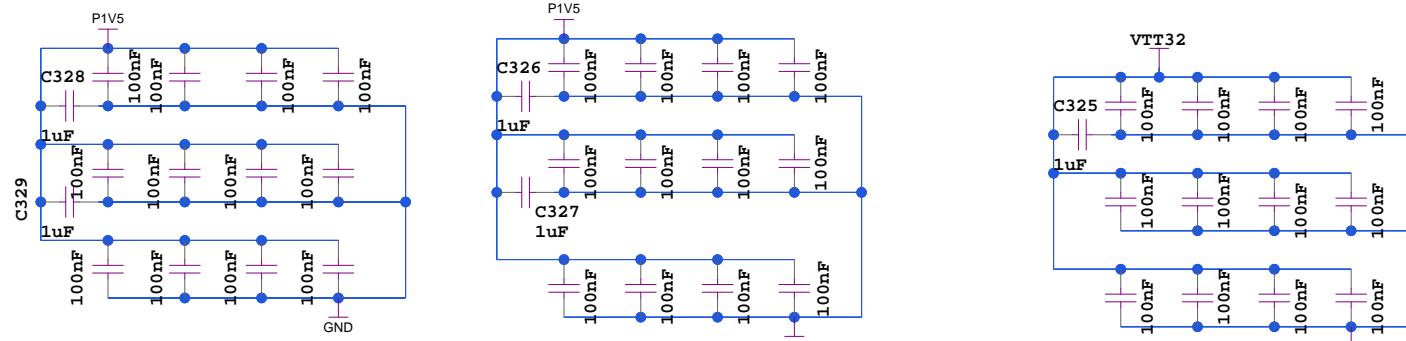
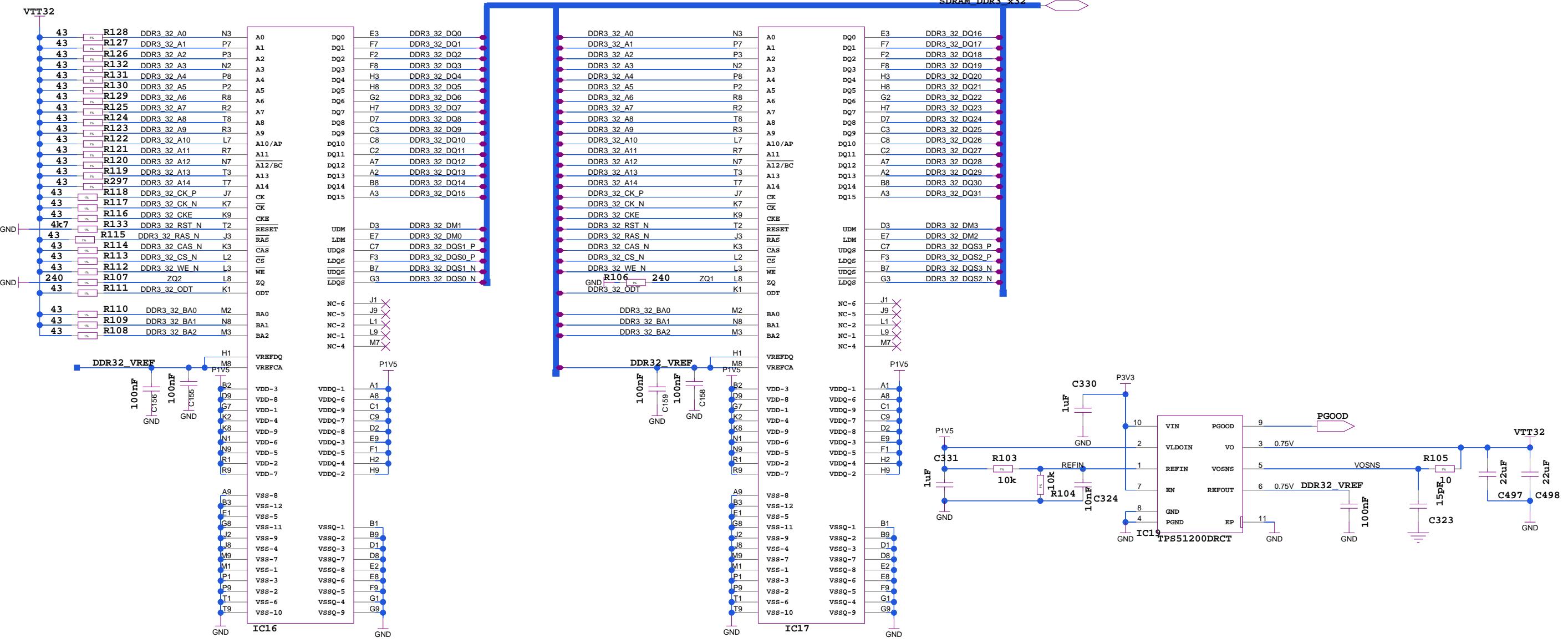
All capacitors without values are 100nF 0201 by default



# ARTIQ Sinara

# **SDRAM DDR3 4x16**

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**SDRAM\_DDR3\_2x16**

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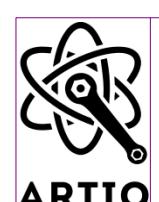
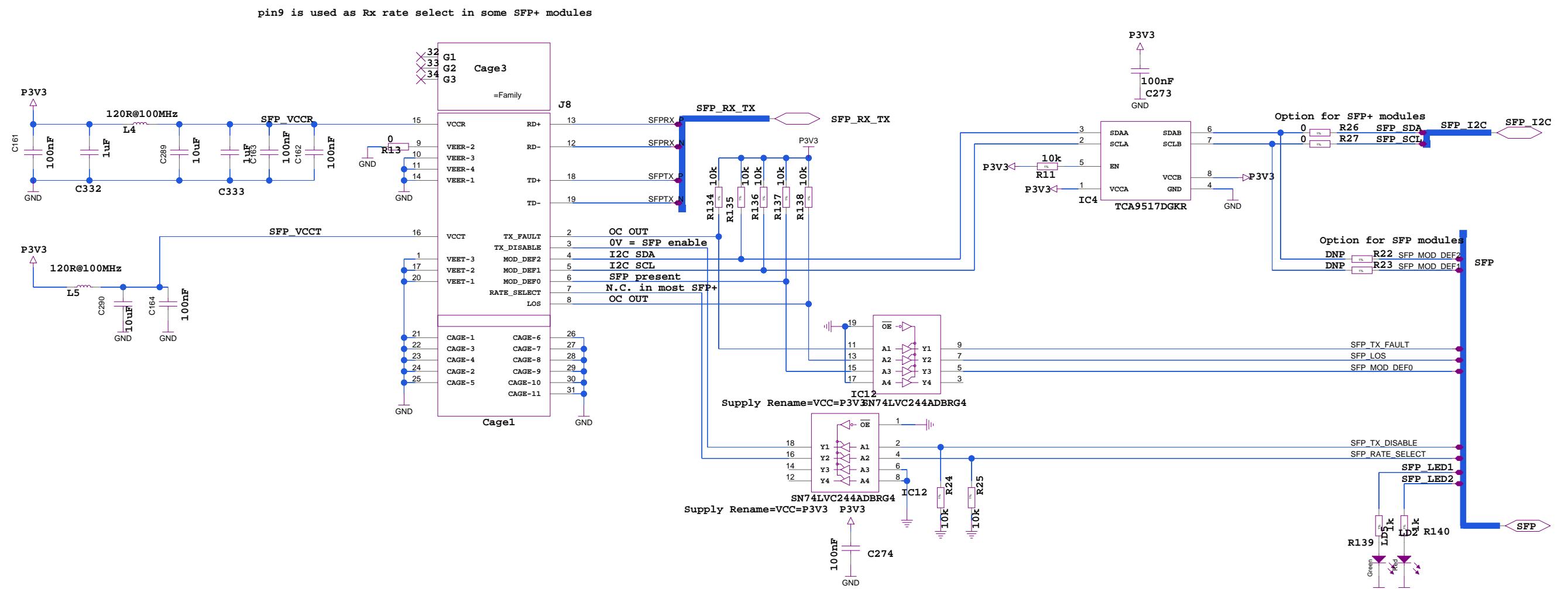
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# ARTIQ Sinara

SFP

SFP

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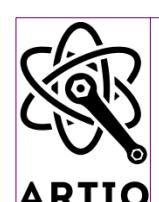
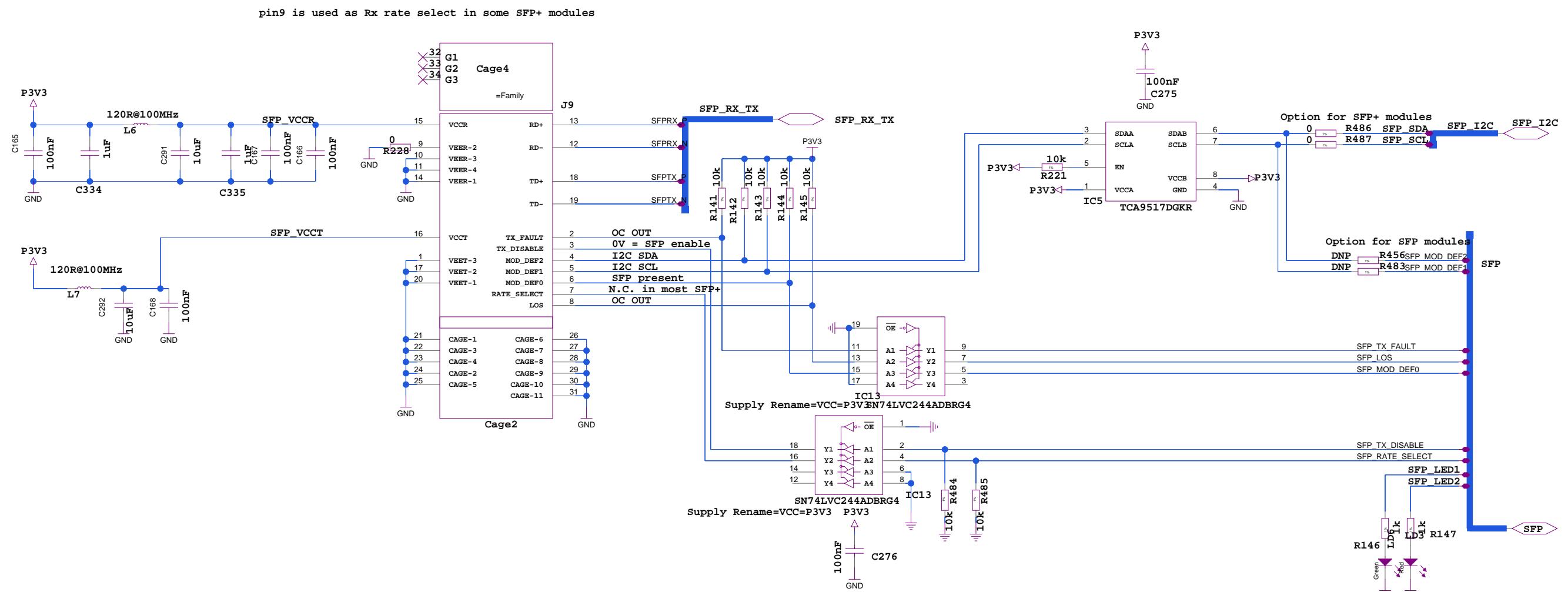
Page 1

31

SFP

v0.97

34 / 01 / 2017 • 33 • 13



ARTIQ Sinara

SFP

SIZE DWG NO

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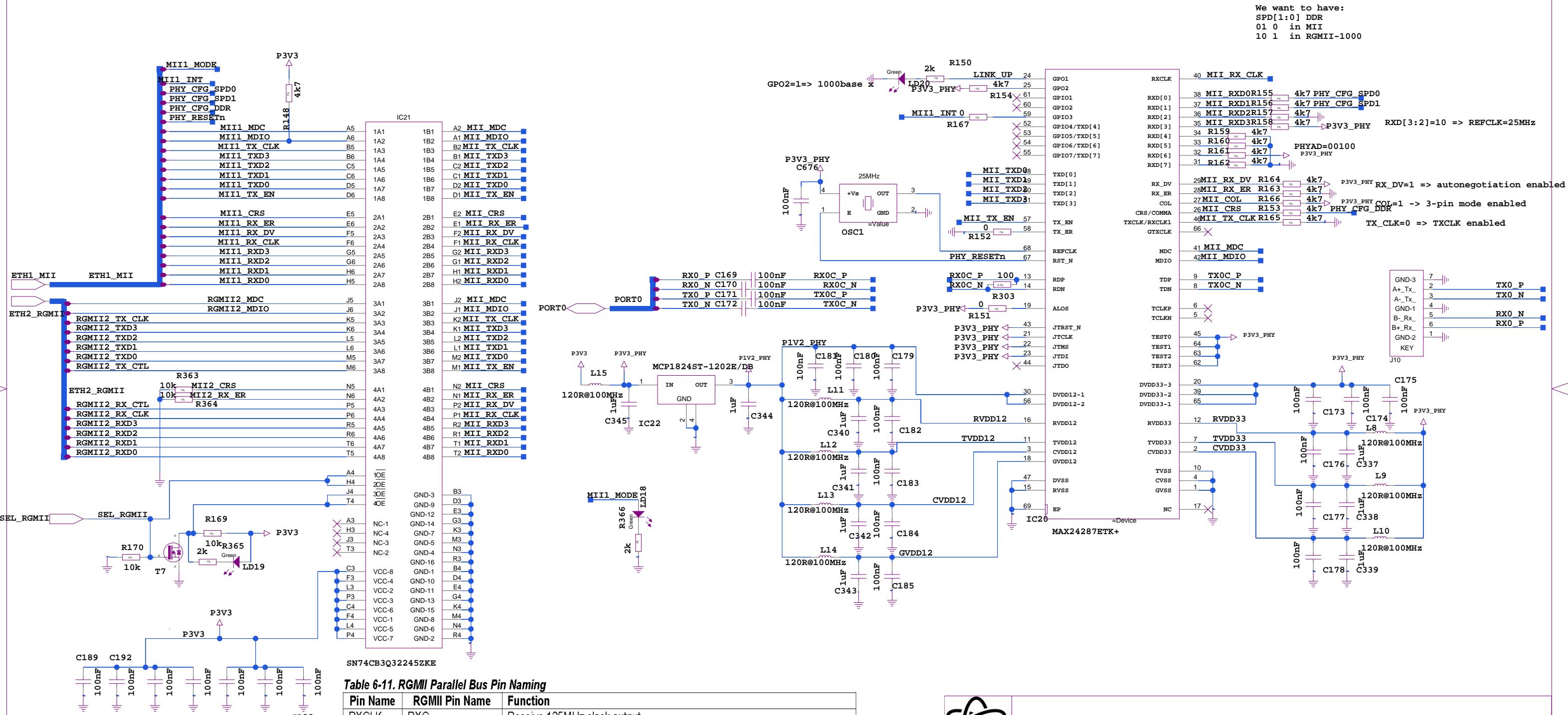
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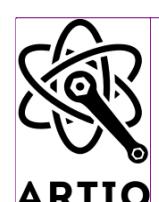
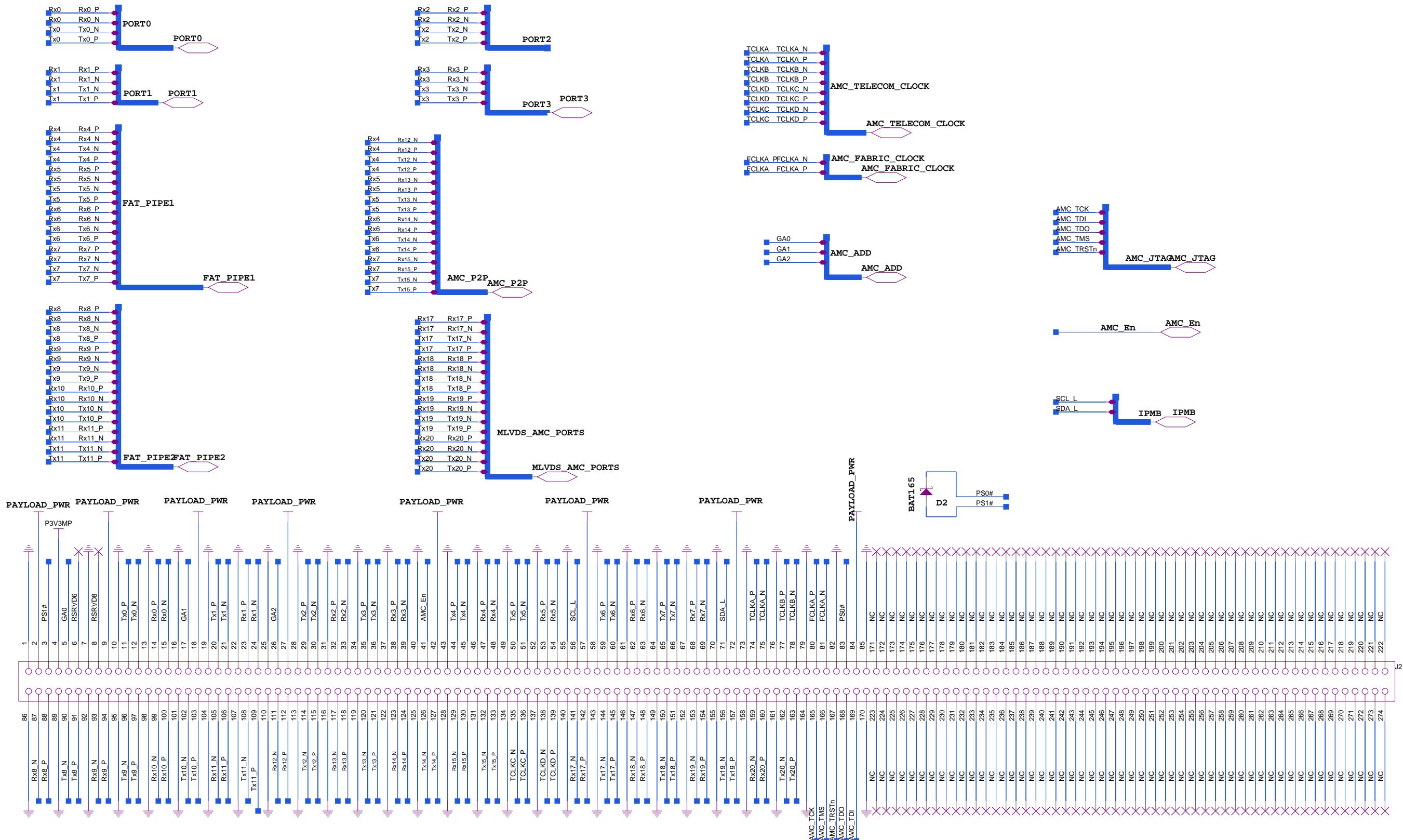


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**ETH\_PHY\_RMII\_MII**



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# AMC\_Connector

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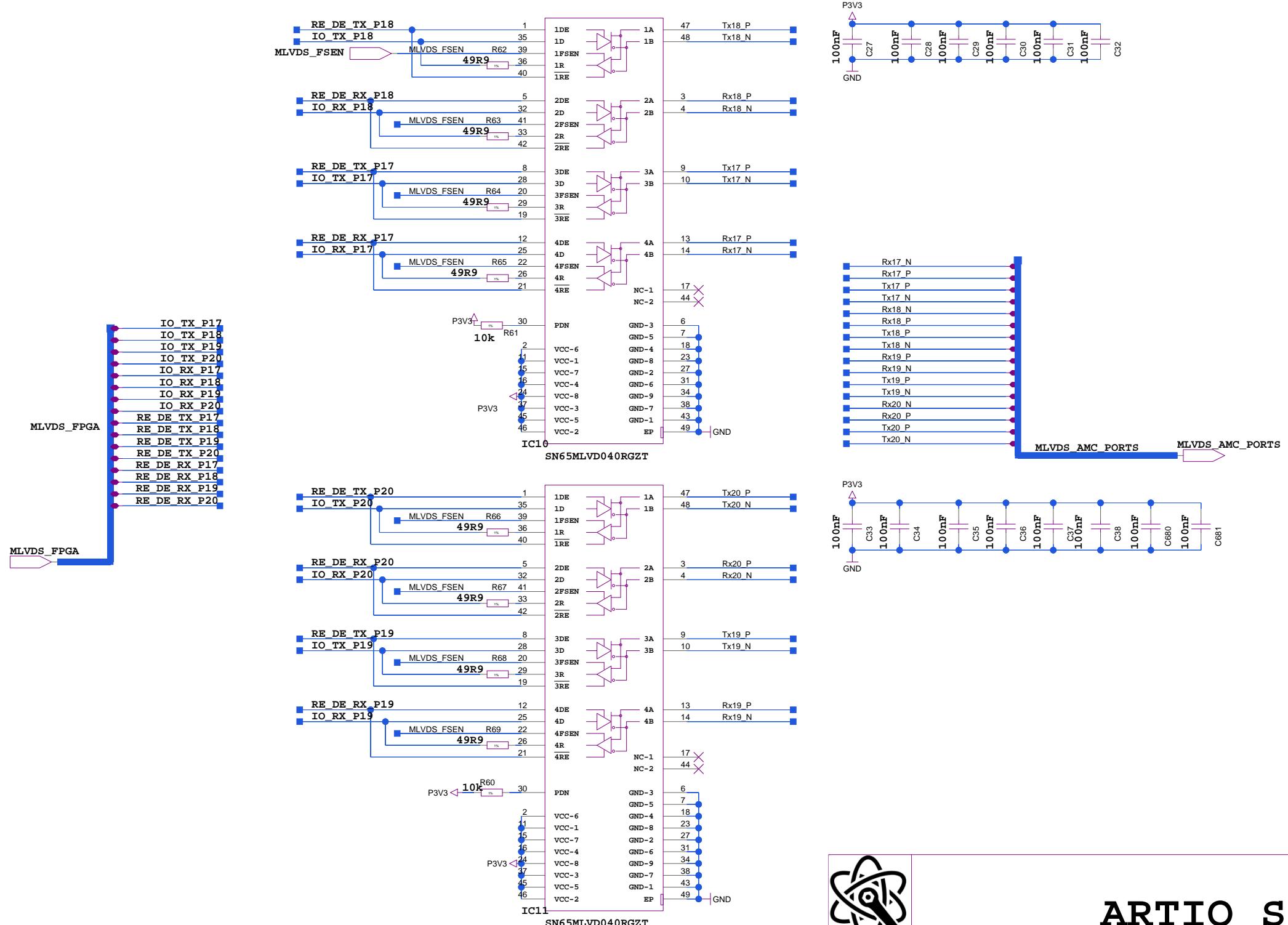
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- Dimensions are in MM, nominal values used
- Component height rule derived from AMC Base Specification.PDF, Page 62
- The two corners of outline near the edge-connector are approximated, see AMC Base Specification.PDF, Page 59
- Stackup is not specified in AMC Base Specification.PDF or implemented in this template.

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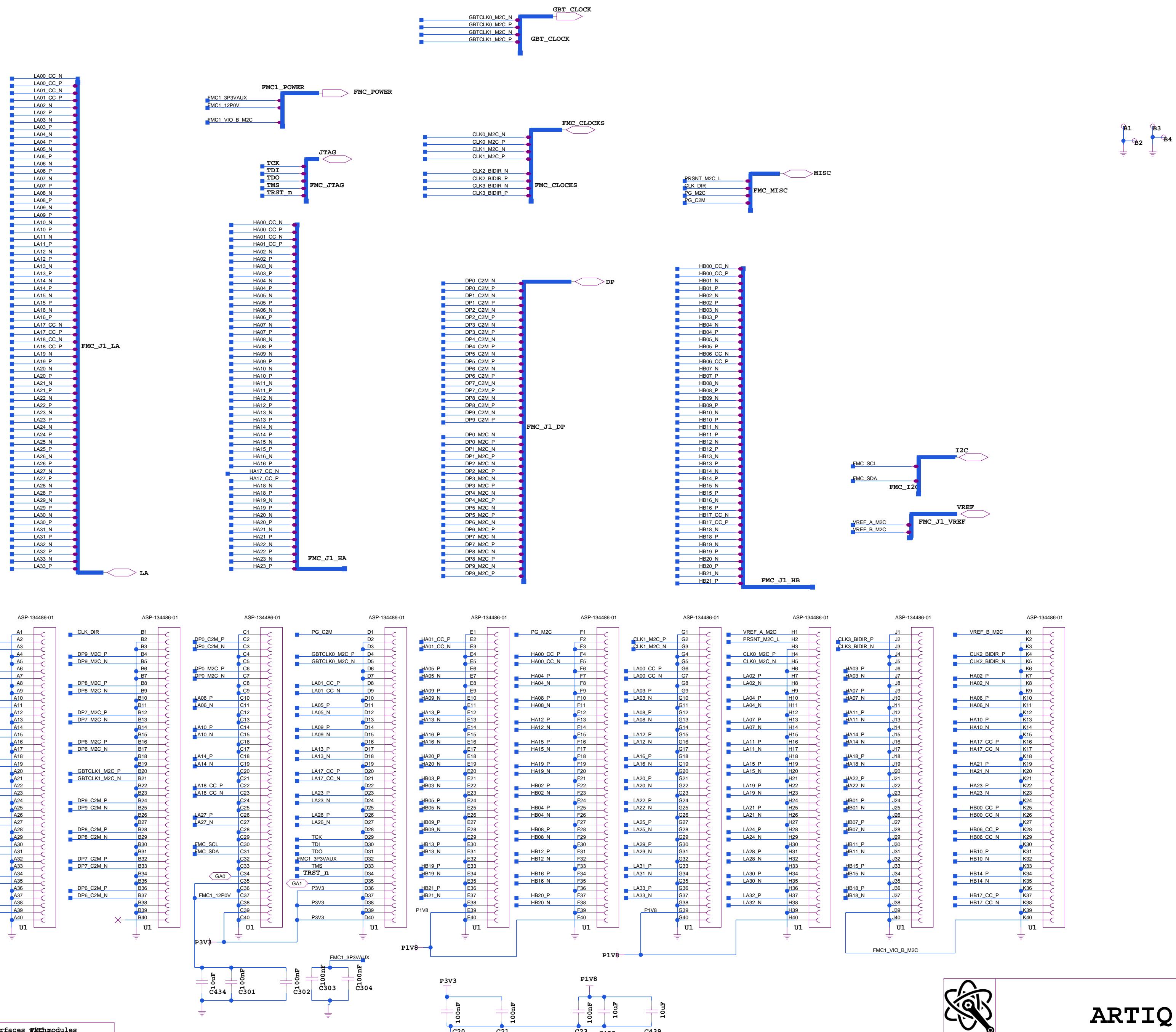


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## M-LVDS\_PHY

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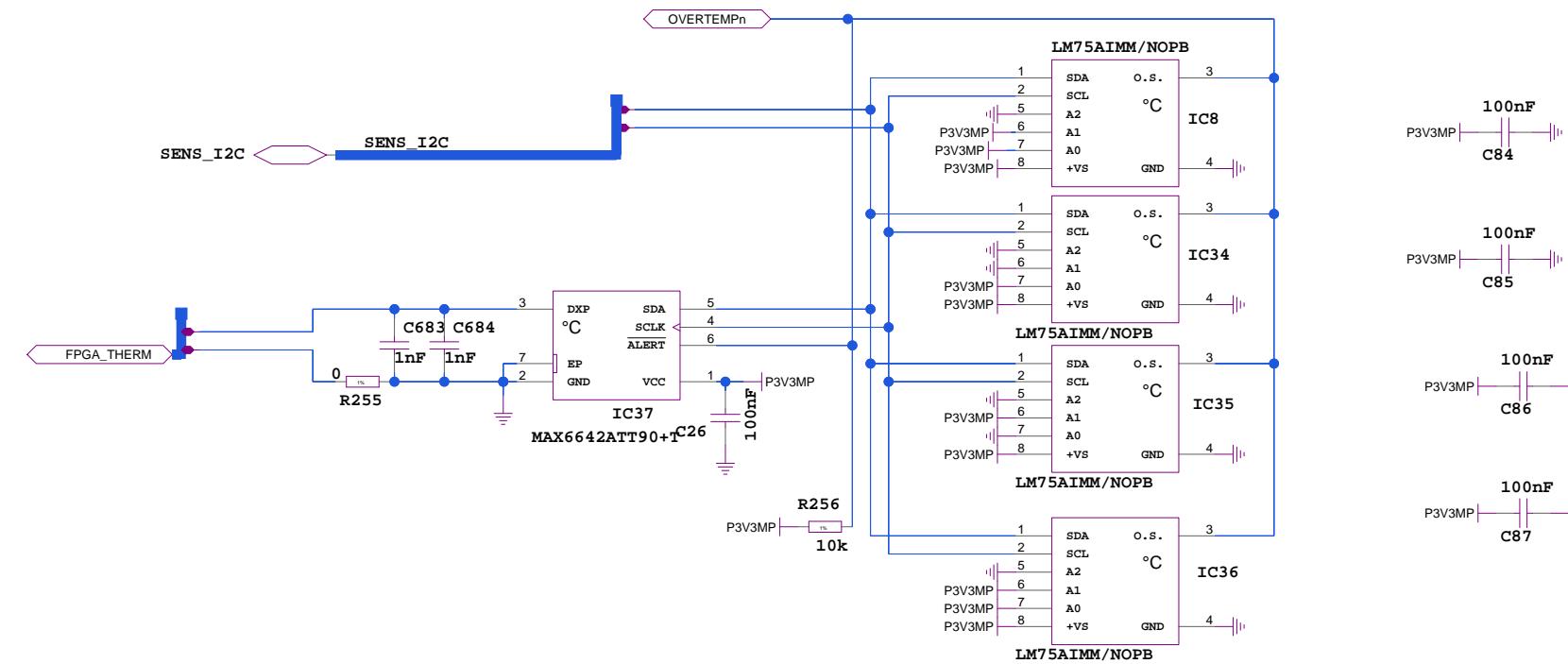
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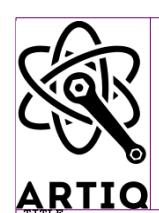
**ARTIQ Sinara**

# FMC\_connector

SIZE	DWG NO	REV
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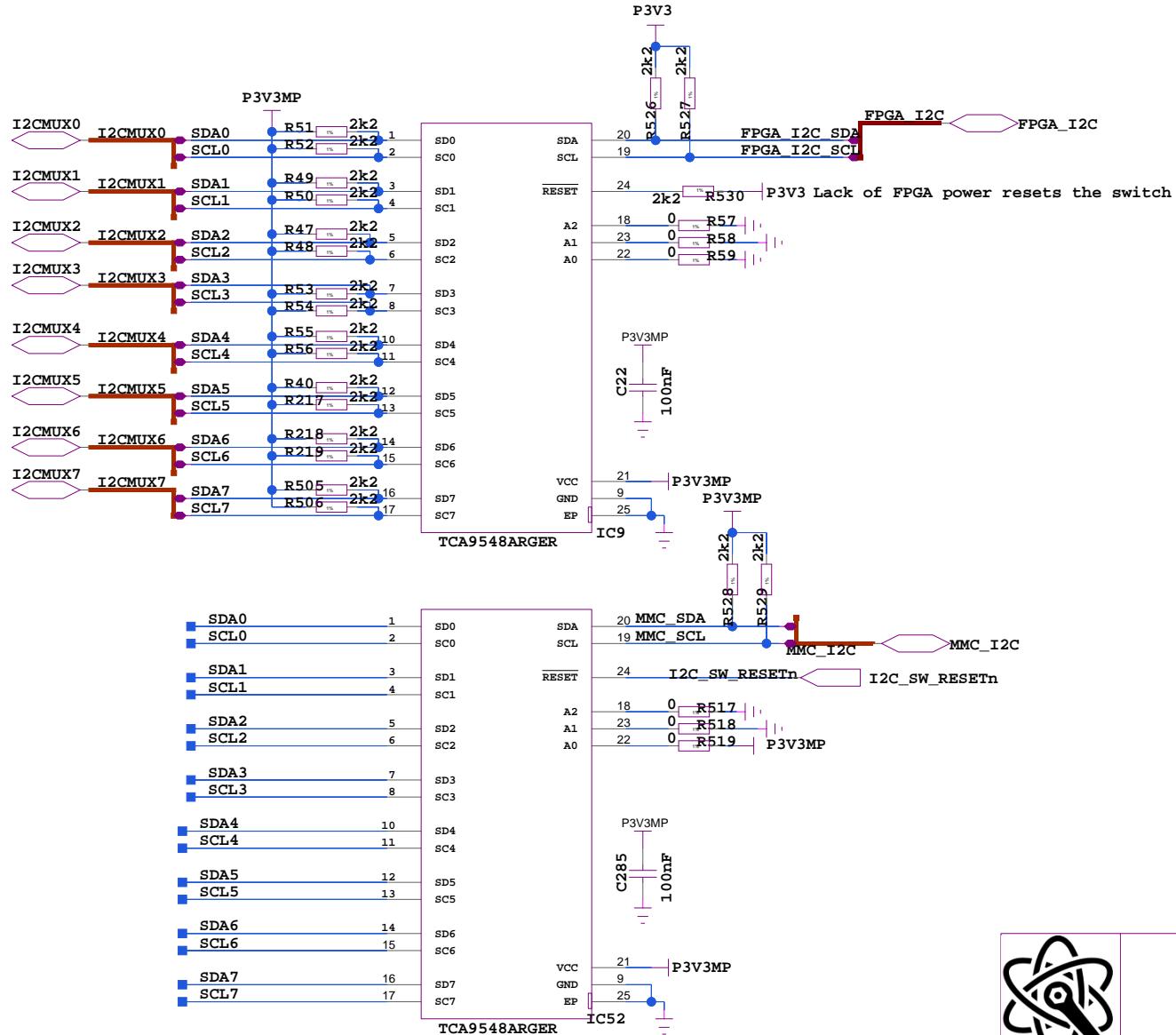


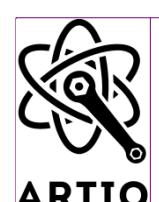
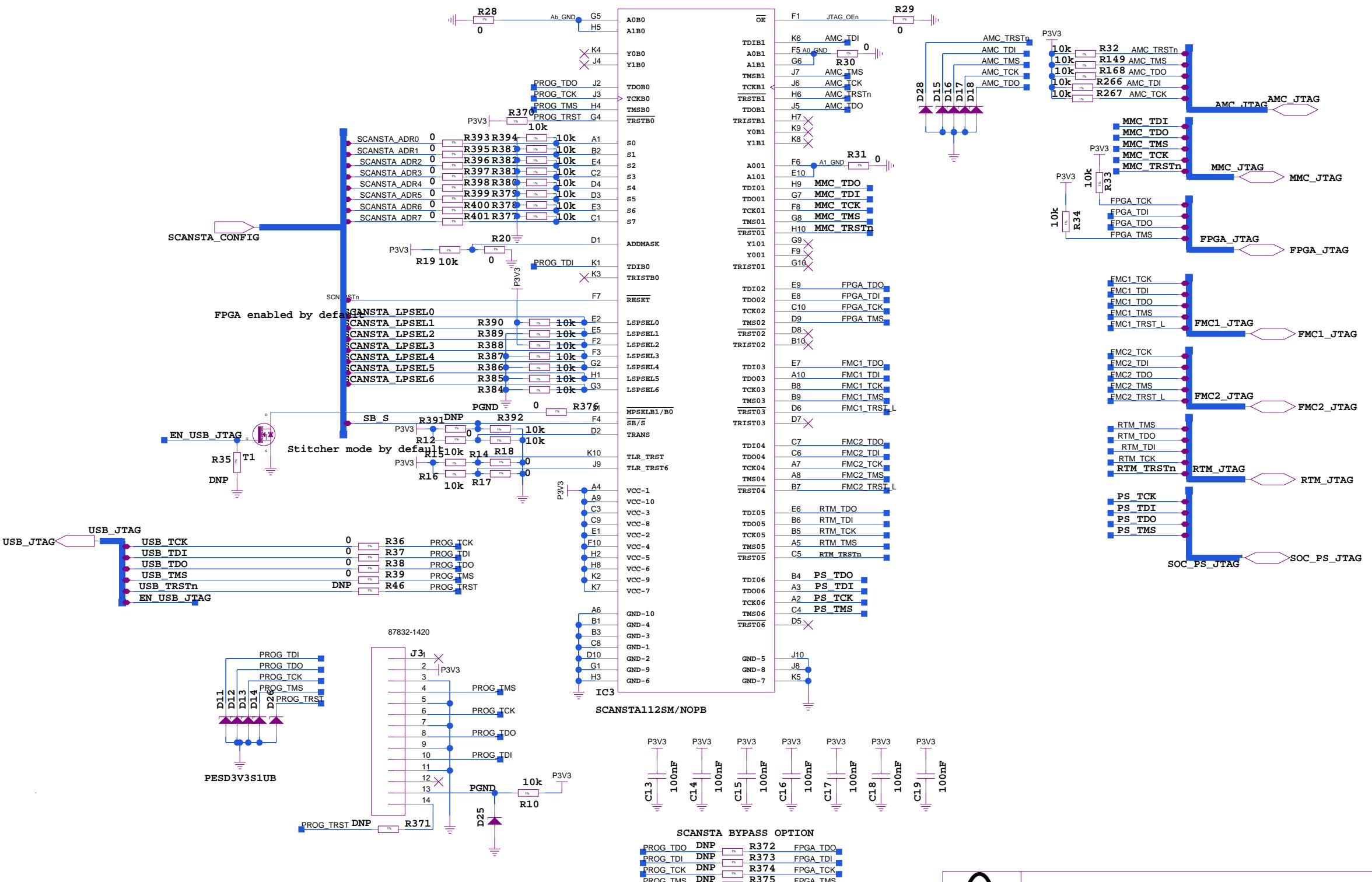
**ARTIQ Sinara**

**Thermometers**

SIZE	DWG NO	REV
A3		v0.97
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I2C switch footprint is compatible with MAX7358 which has interesting anti-lock capabilities

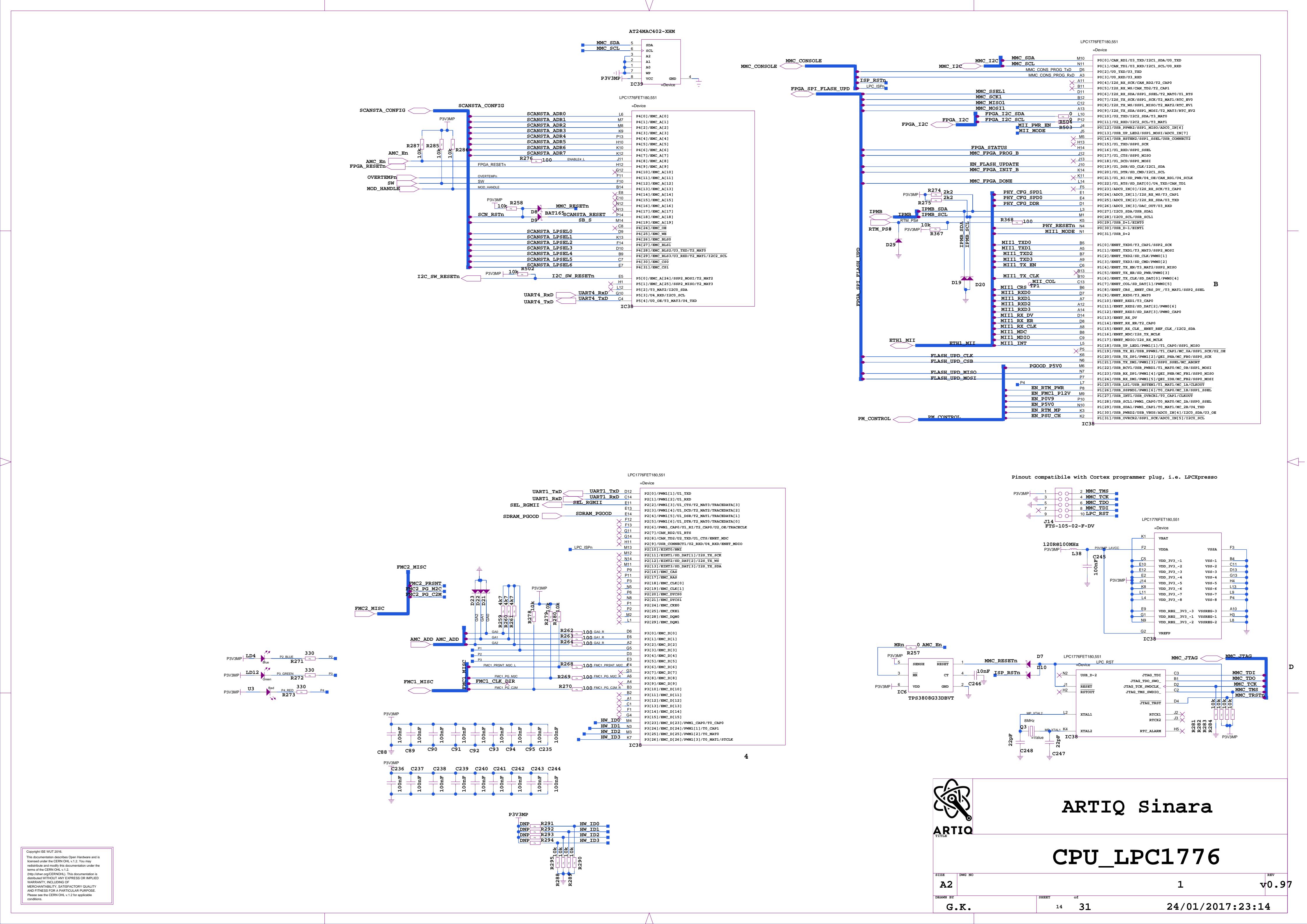


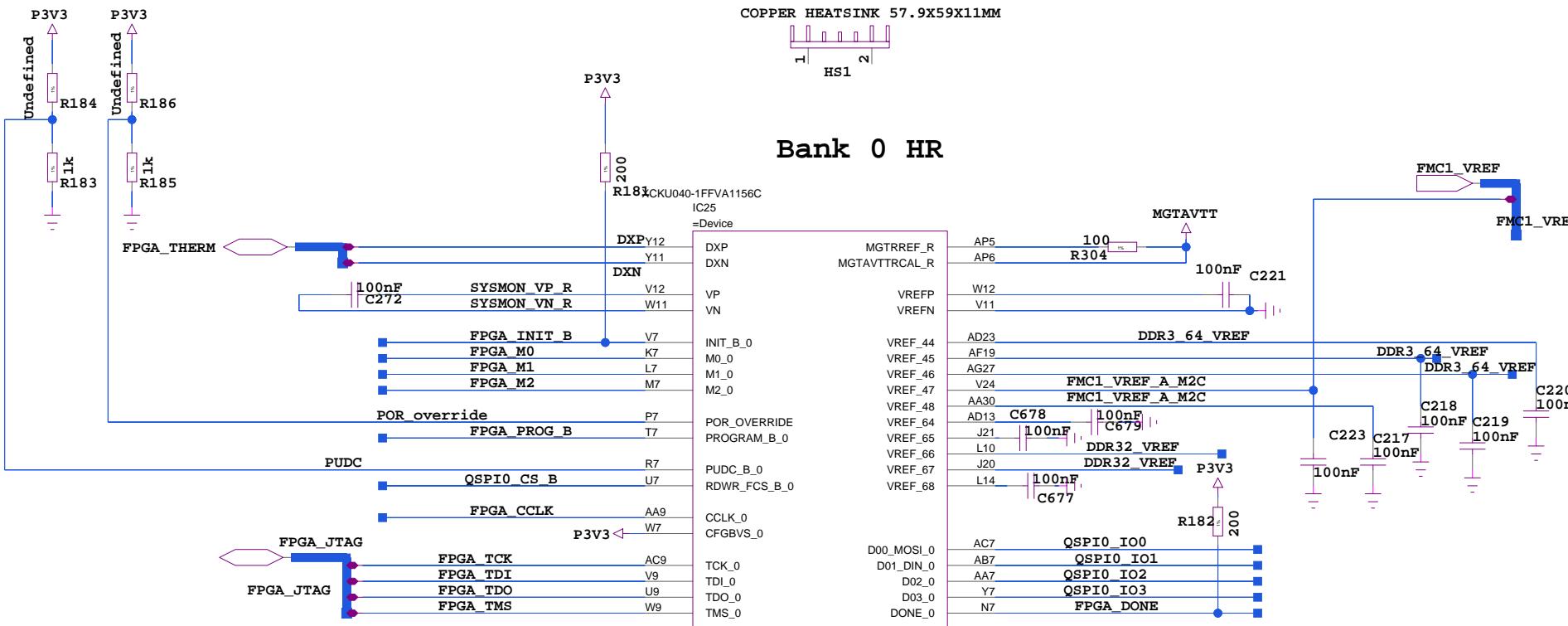


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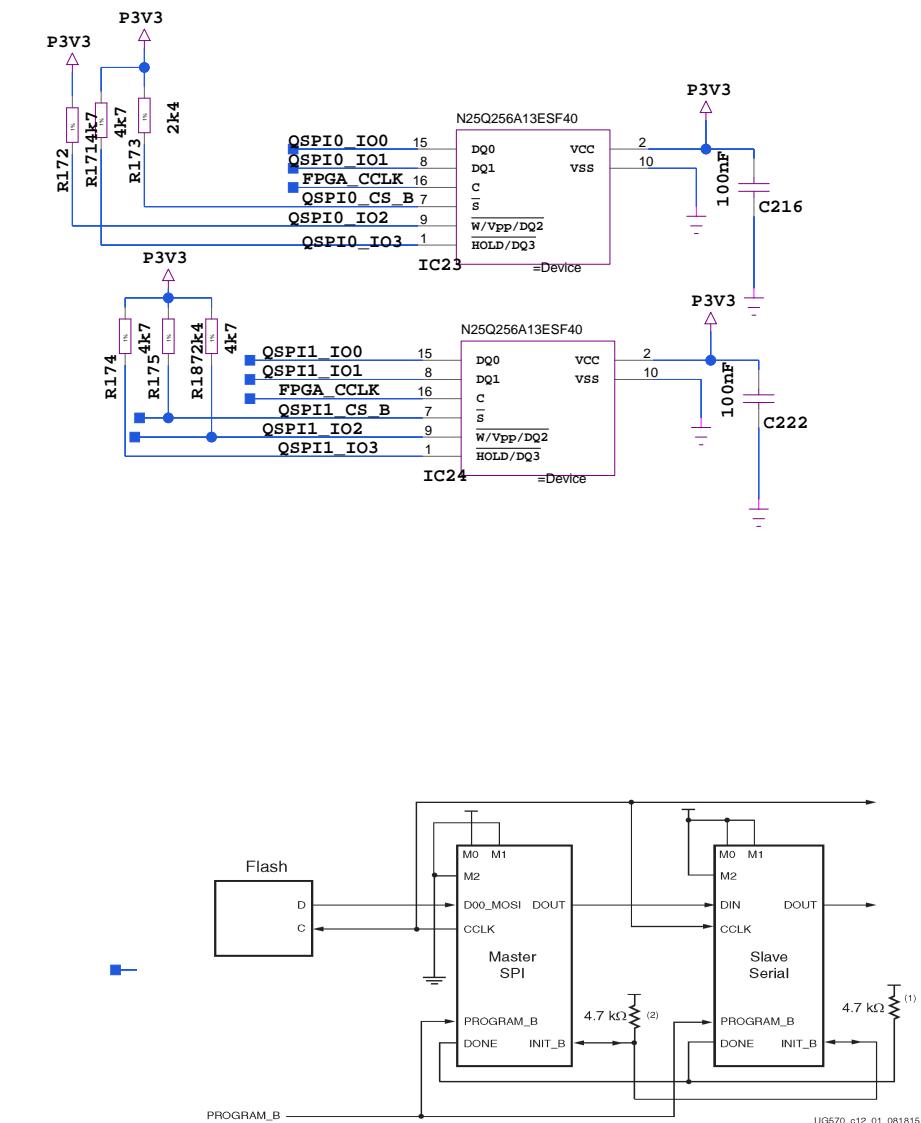
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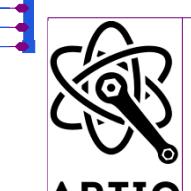
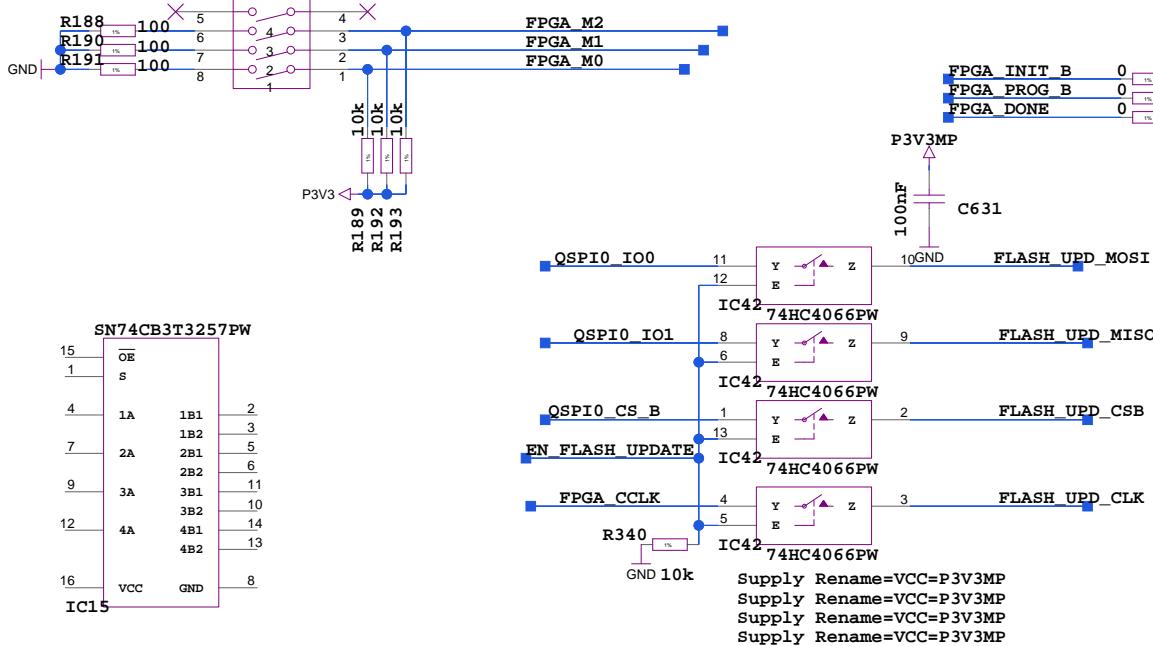




Layout: Place resistor and capacitor for VREF  
Underneath the FPGA via array  
right next to the via



*Figure 12-1: Master/Slave Serial Mode Daisy Chain Configuration Interface Example*

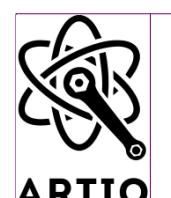
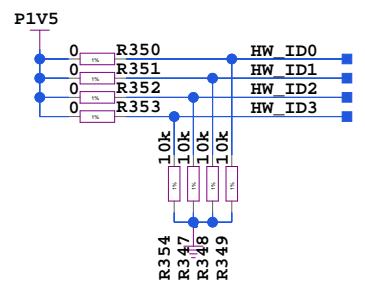
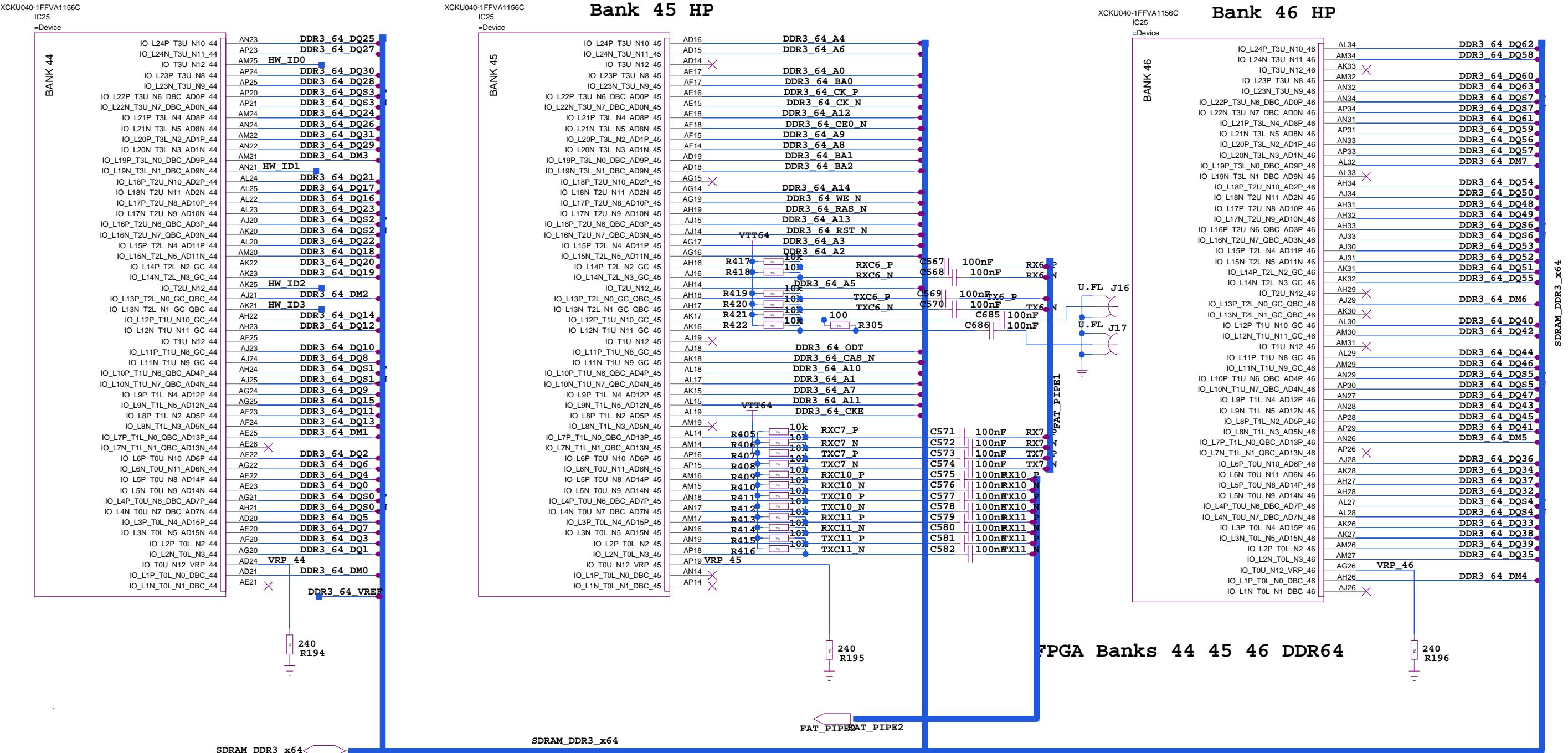


FPGA\_XCKU040FFVA1156

# FPGA Bank 0 CFG

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Bank 44 HP



# ARTIQ Sinara

FPGA Banks 44 45 46 DDR

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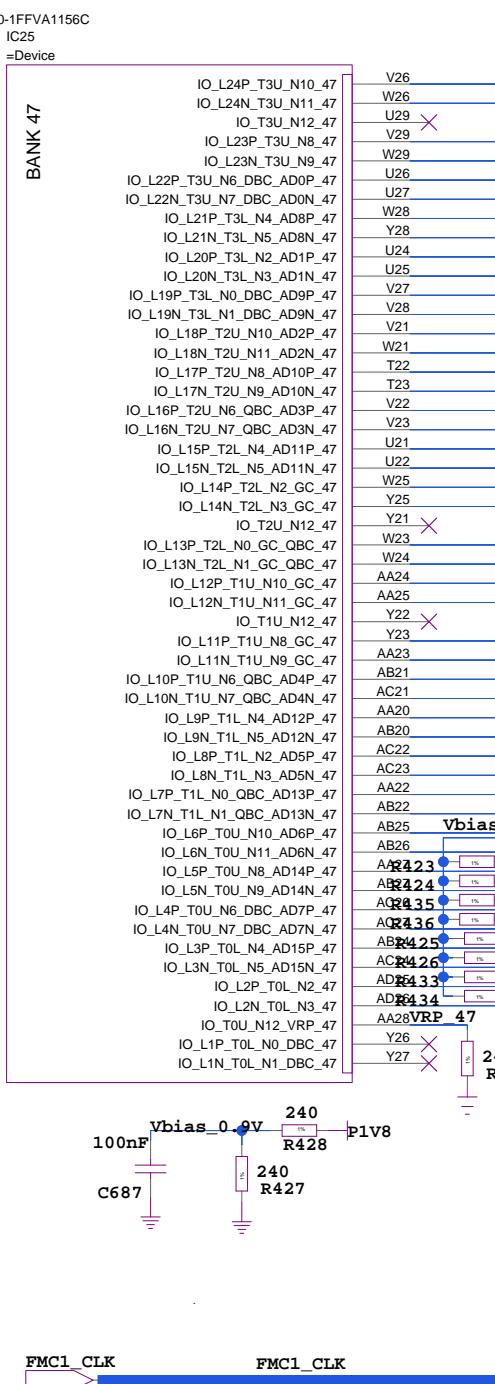
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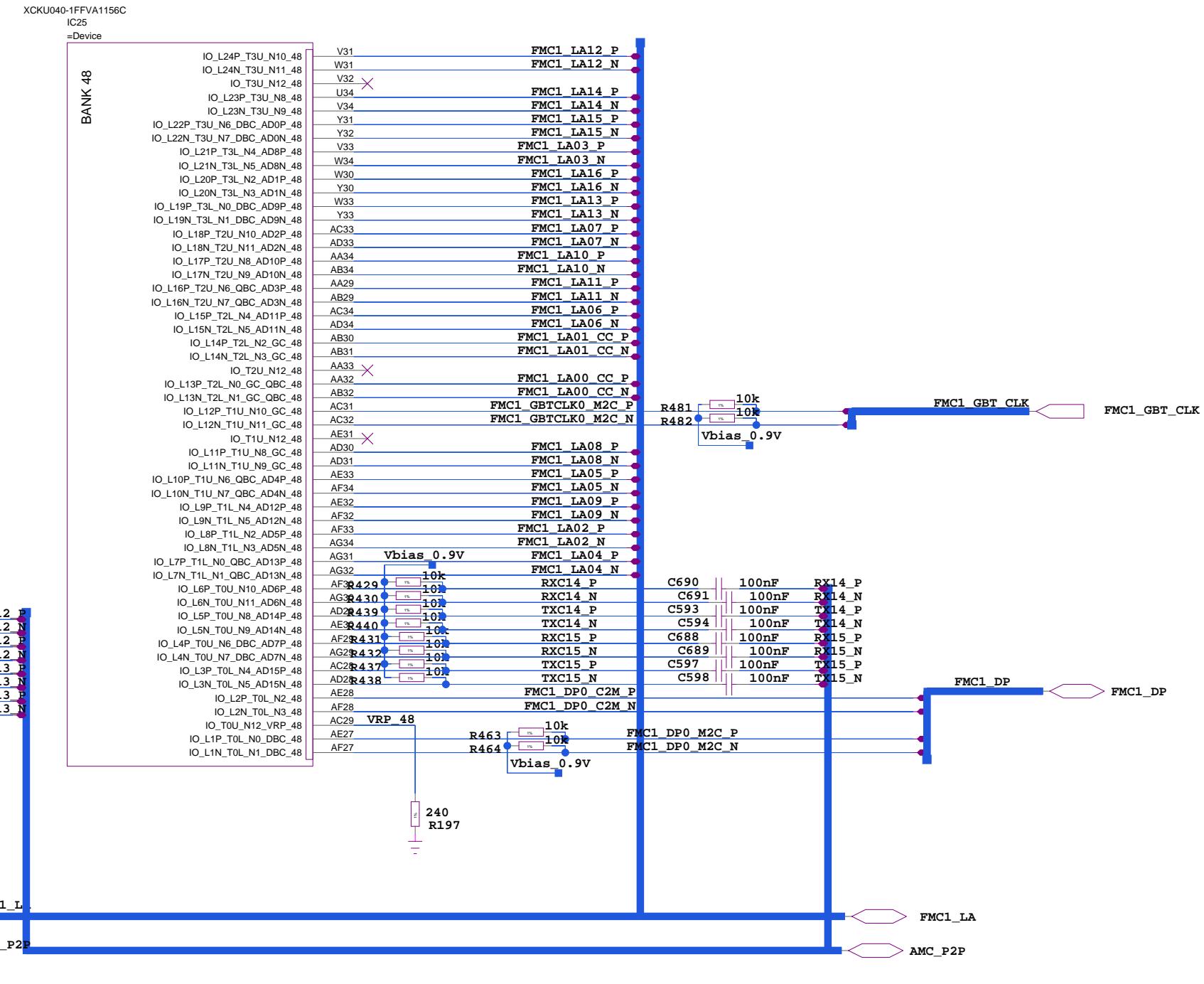
REV

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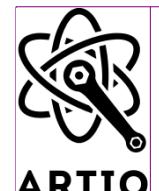
## Bank 47 HP



## Bank 48 HP



FPGA\_XCKU040FFVA1156



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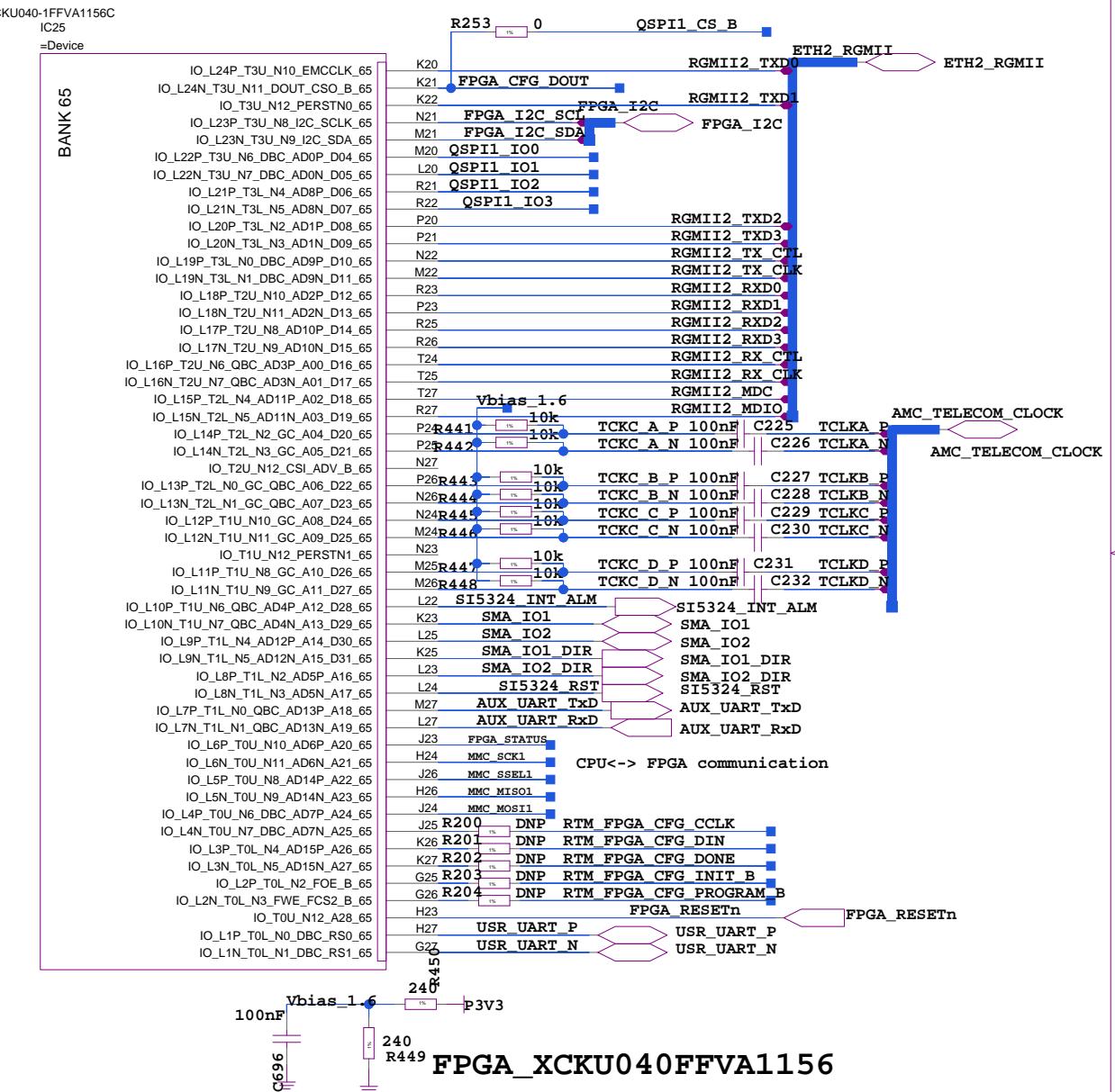
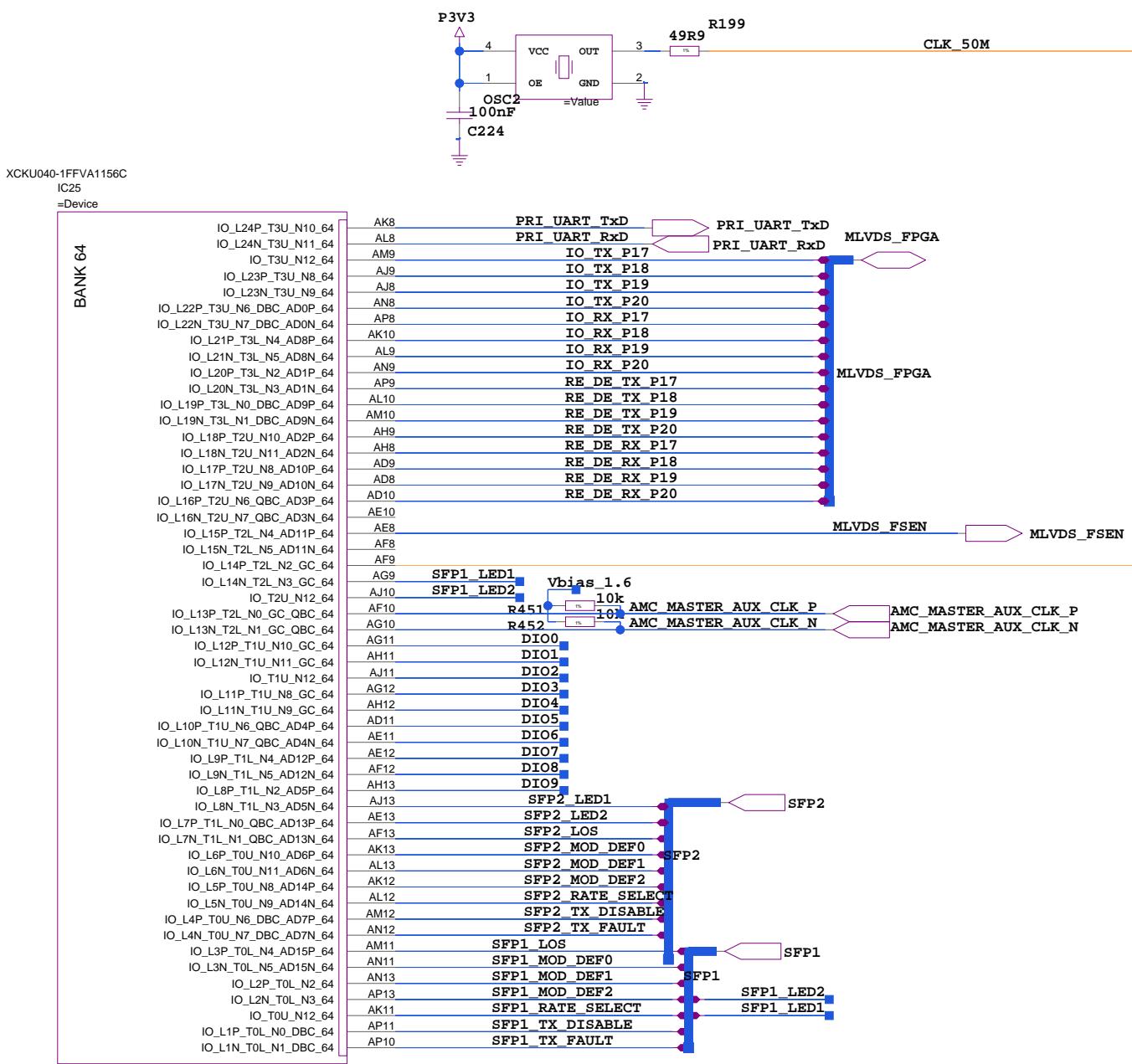
FPGA Banks 47 48 HP FM

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## Bank 64 HR

Bank 65 HE



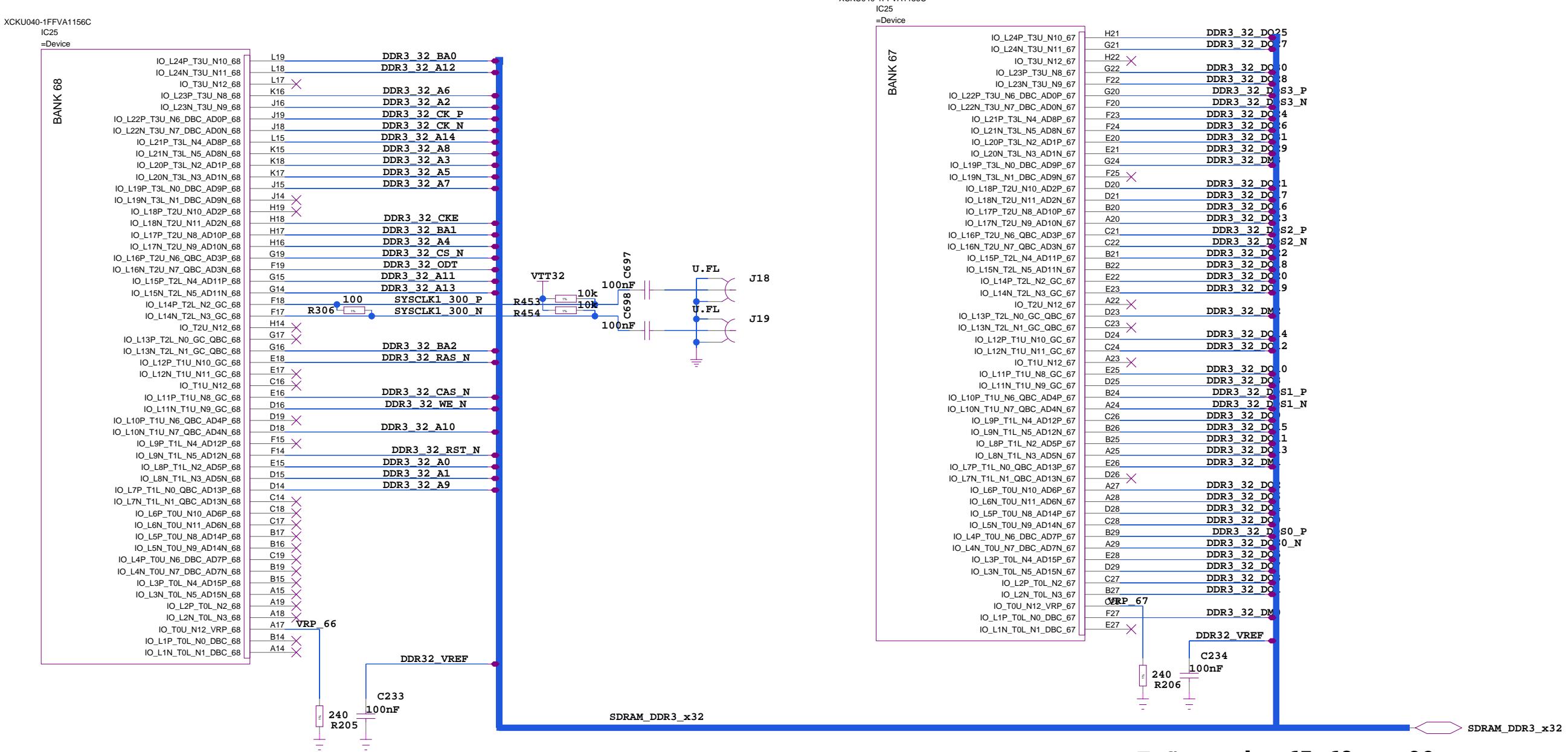
# ARTIQ Sinara

## FPGA Banks 64 65 HR

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Layout: Place resistor and capacitor for VREF  
 Underneath the FPGA via array  
**Bank 68 HP**  
 right next to the via

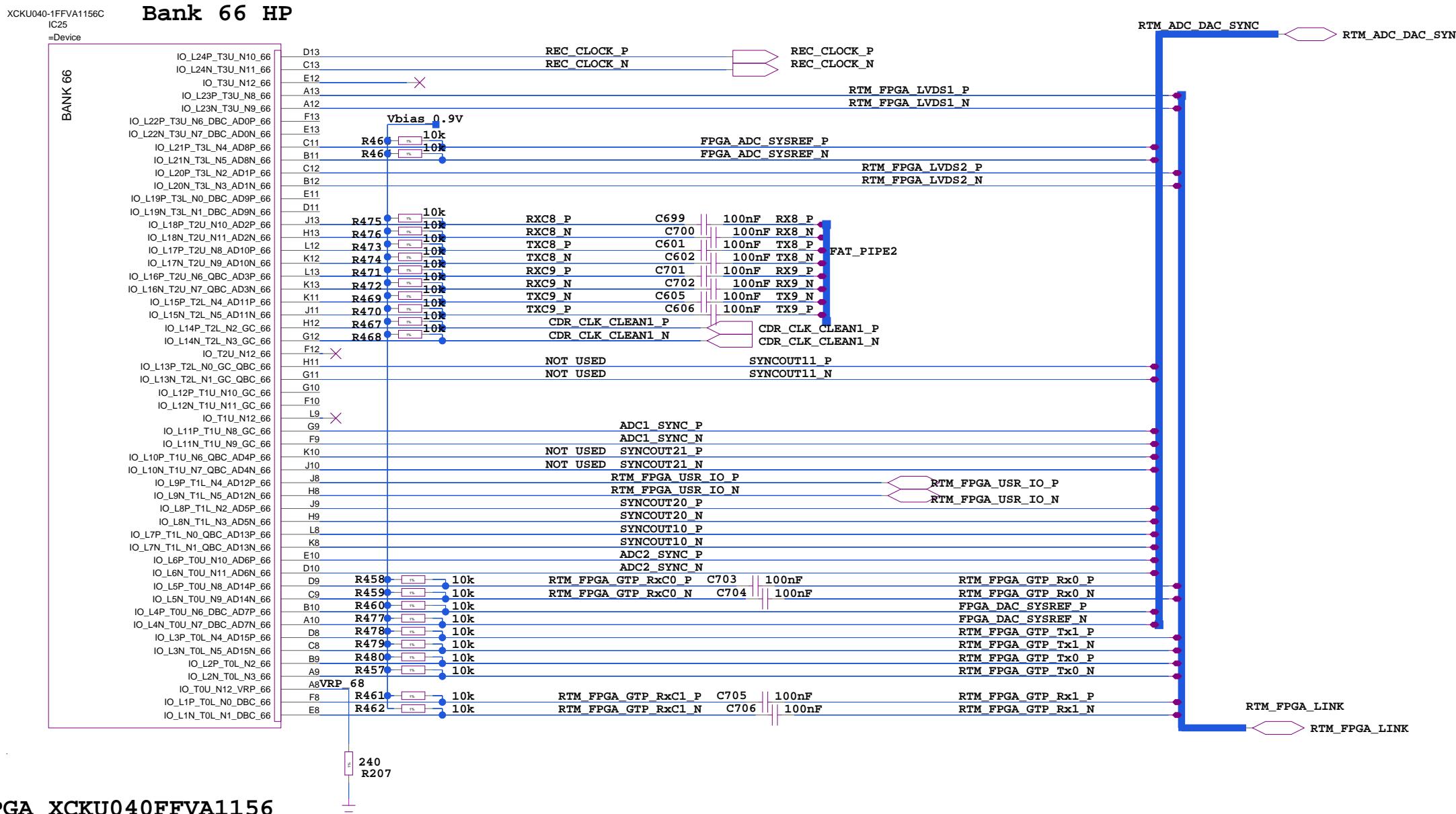
**Bank 67 HP**



Layout: Place resistor and capacitor for VREF

vbias\_0.9V

Underneath the FPGA via array  
right next to the via

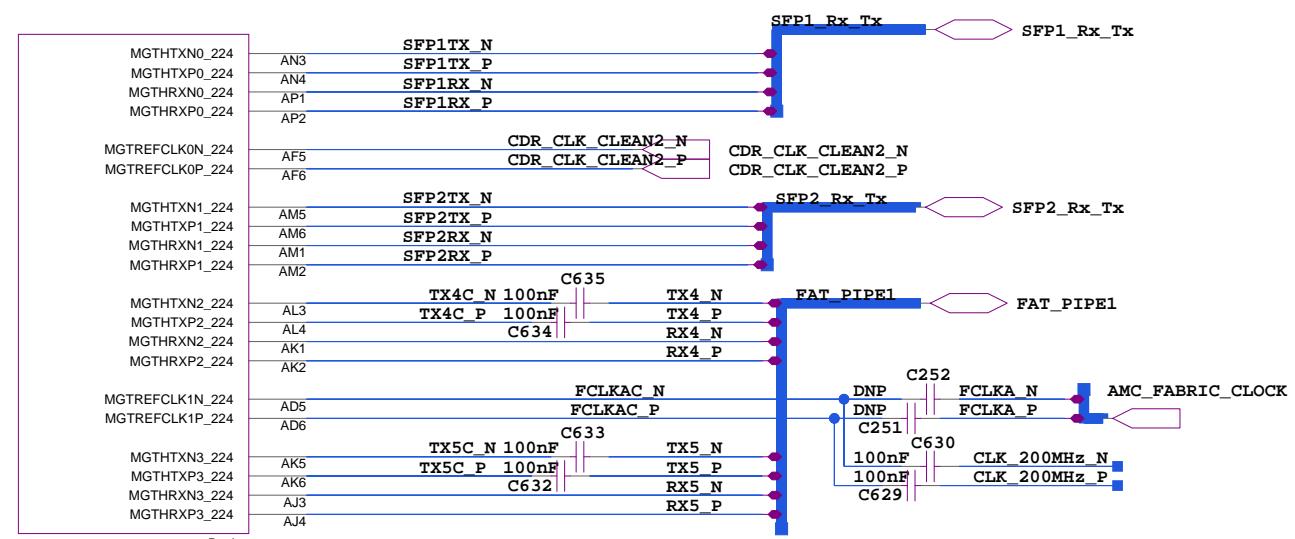
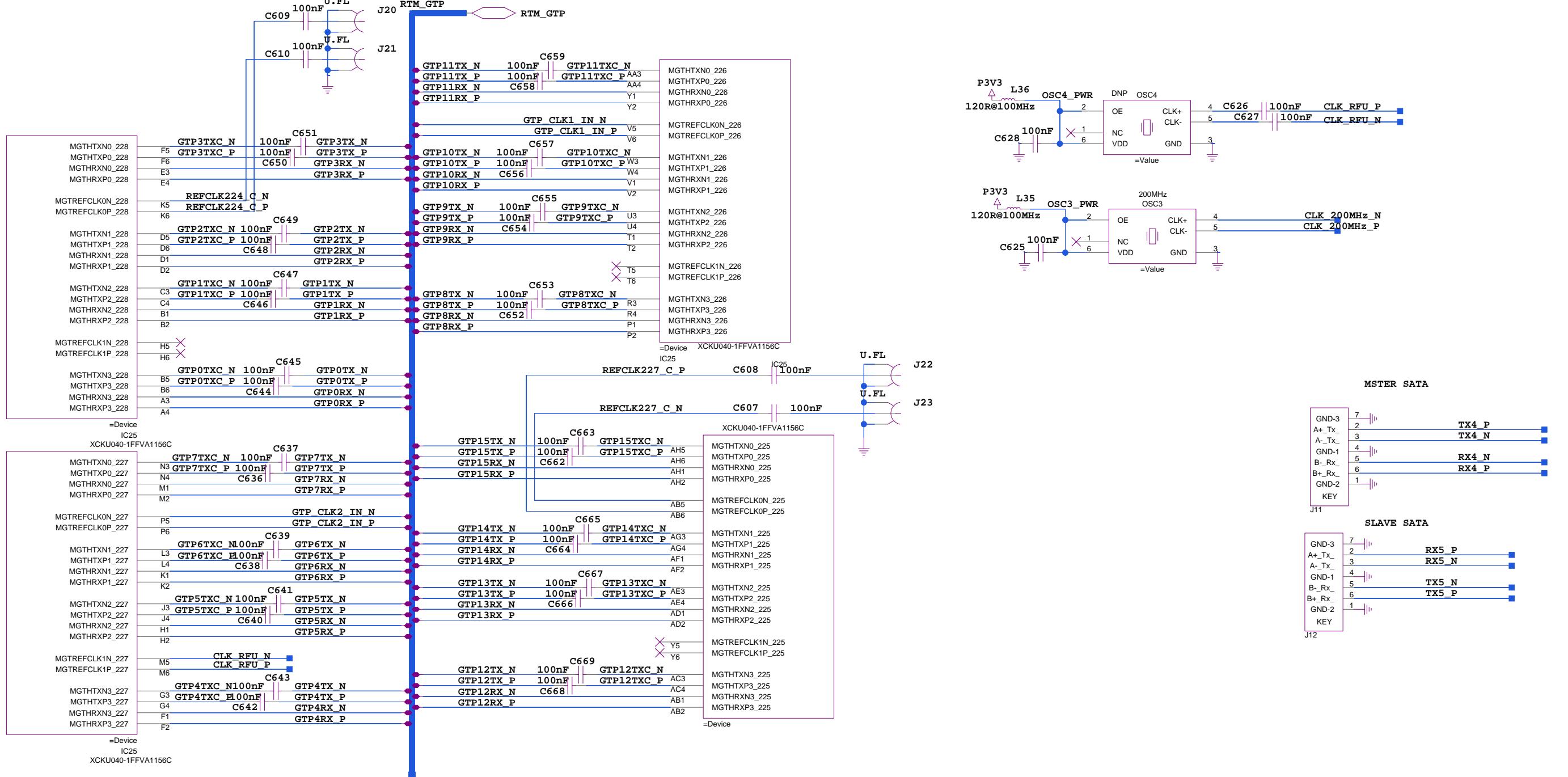


FPGA Bank 66 HF

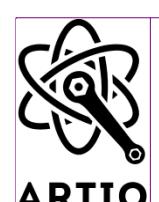
ARTIQ Sinara

# FPGA Bank 66 HP

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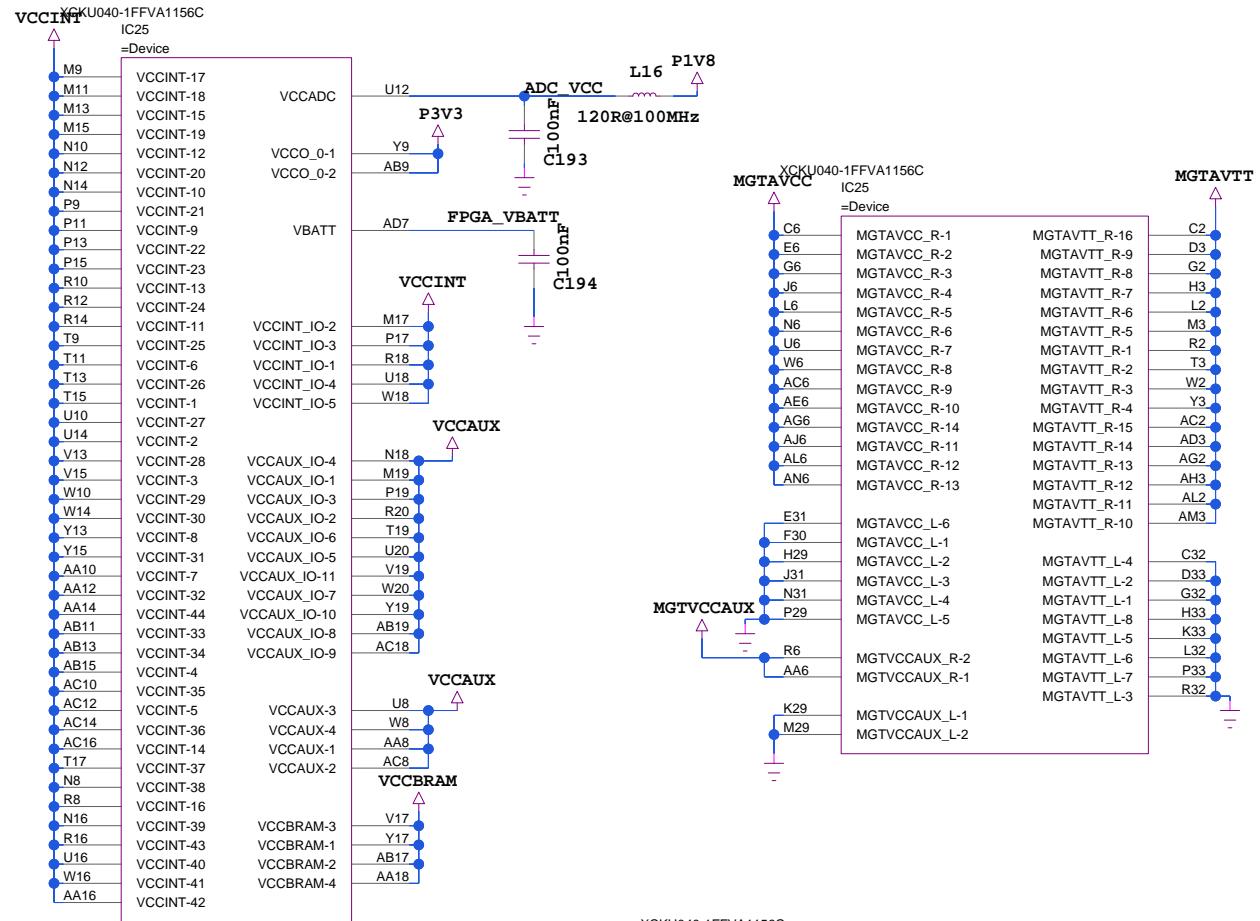


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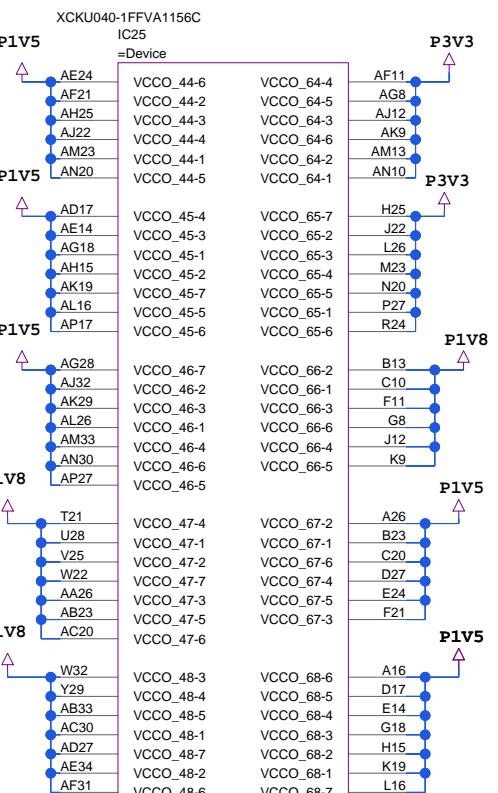


FPGA Banks 224 225 226 22

ARTIQ Sinara



Power Supply		
Source	Voltage	Total (A)
V <sub>CCINT</sub>	0.900	9.165
V <sub>CCINT_IO</sub>	0.900	0.620
V <sub>CCBRAM</sub>	0.950	0.031
V <sub>CCAUX</sub>	1.800	0.660
V <sub>CCAUX_IO</sub>	1.800	0.546
V <sub>CCO 3.3V</sub>	3.300	0.000
V <sub>CCO 2.5V</sub>	2.500	
V <sub>CCO 1.8V</sub>	1.800	0.380
V <sub>CCO 1.5V</sub>	1.500	0.936
V <sub>CCO 1.35V</sub>	1.350	
V <sub>CCO 1.2V</sub>	1.200	
V <sub>CCO 1.0V</sub>	1.000	
MGTVC <sub>CAUX</sub>	1.800	0.081
MGTAV <sub>CC</sub>	1.000	3.038
MGTAV <sub>TT</sub>	1.200	0.592
V <sub>CCADC</sub>	1.800	0.014



FPGA Power

FPGA\_XCKU040FFVA1156

ARTIQ Sinara

FPGA Power

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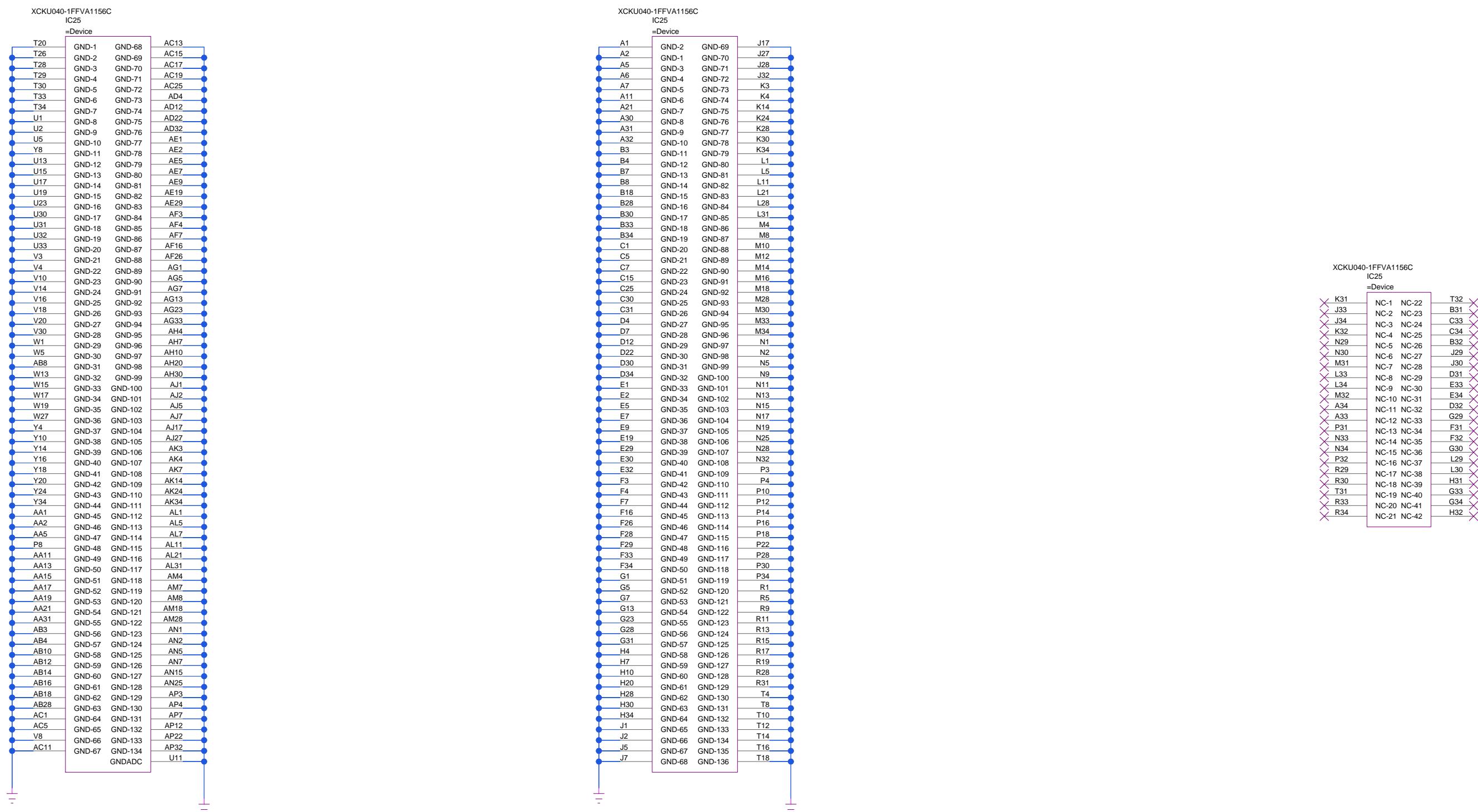
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**FPGA\_XCKU040FARMAQ1s6ara**  
ARTIQ

**FPGA GND NC**

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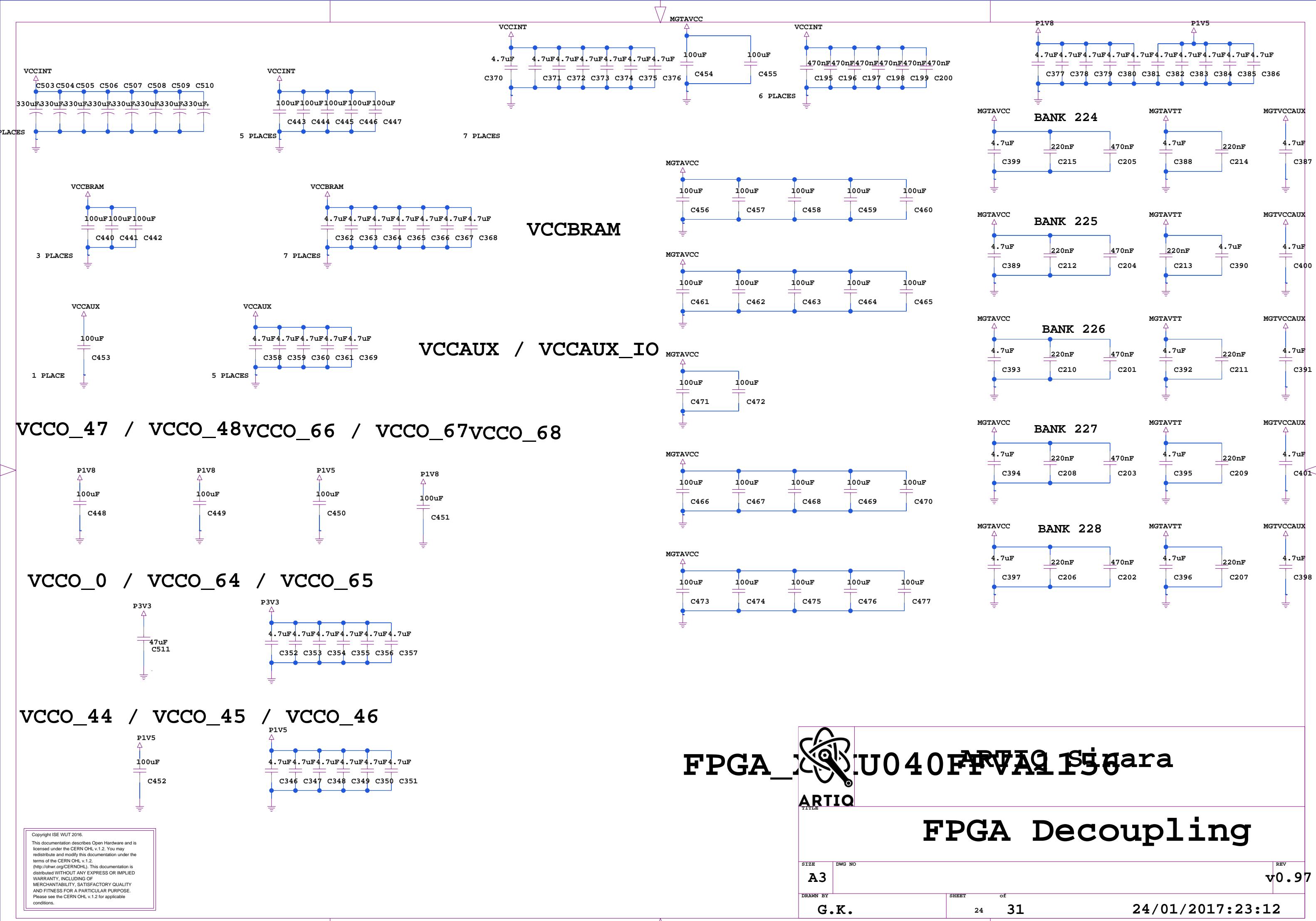
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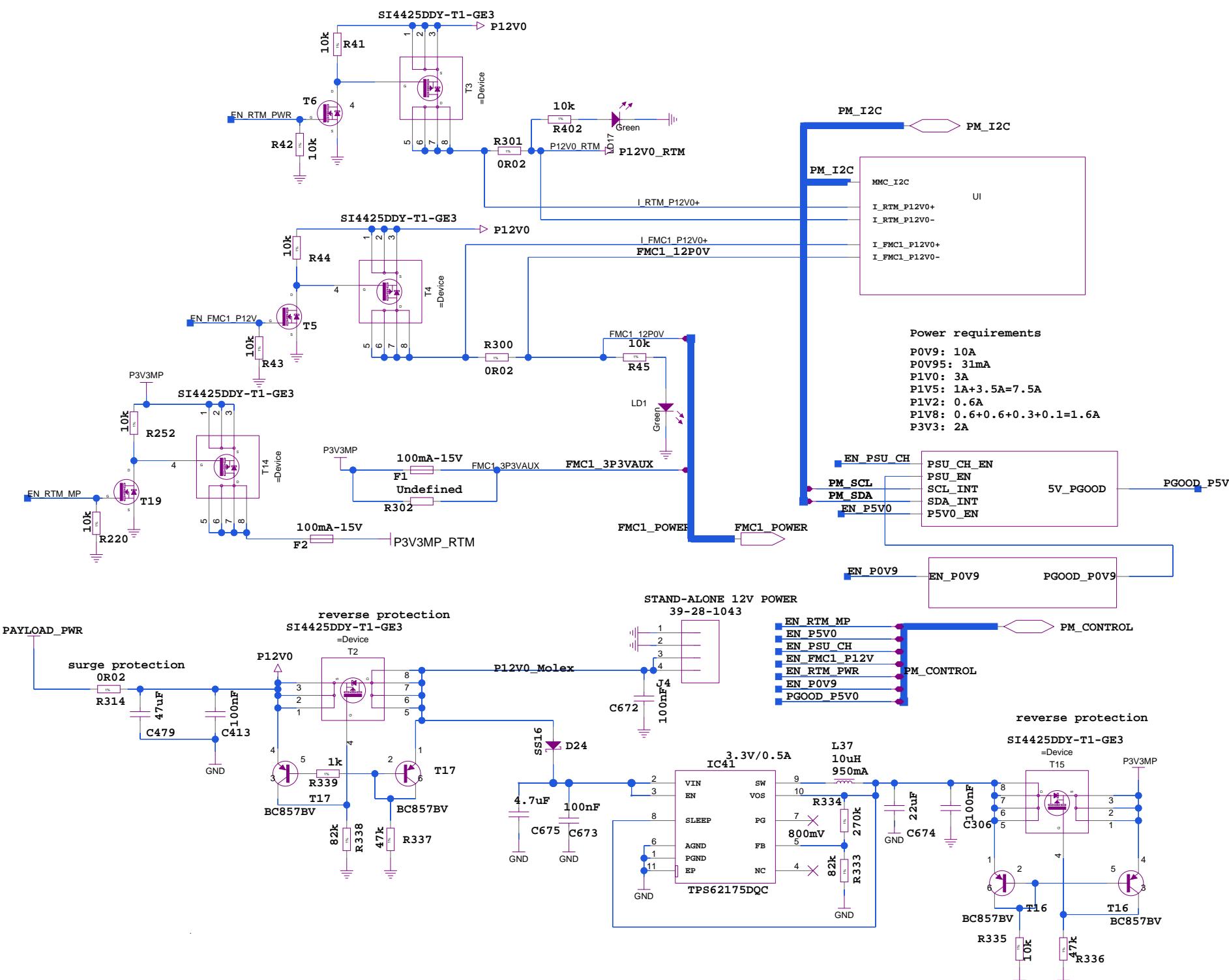
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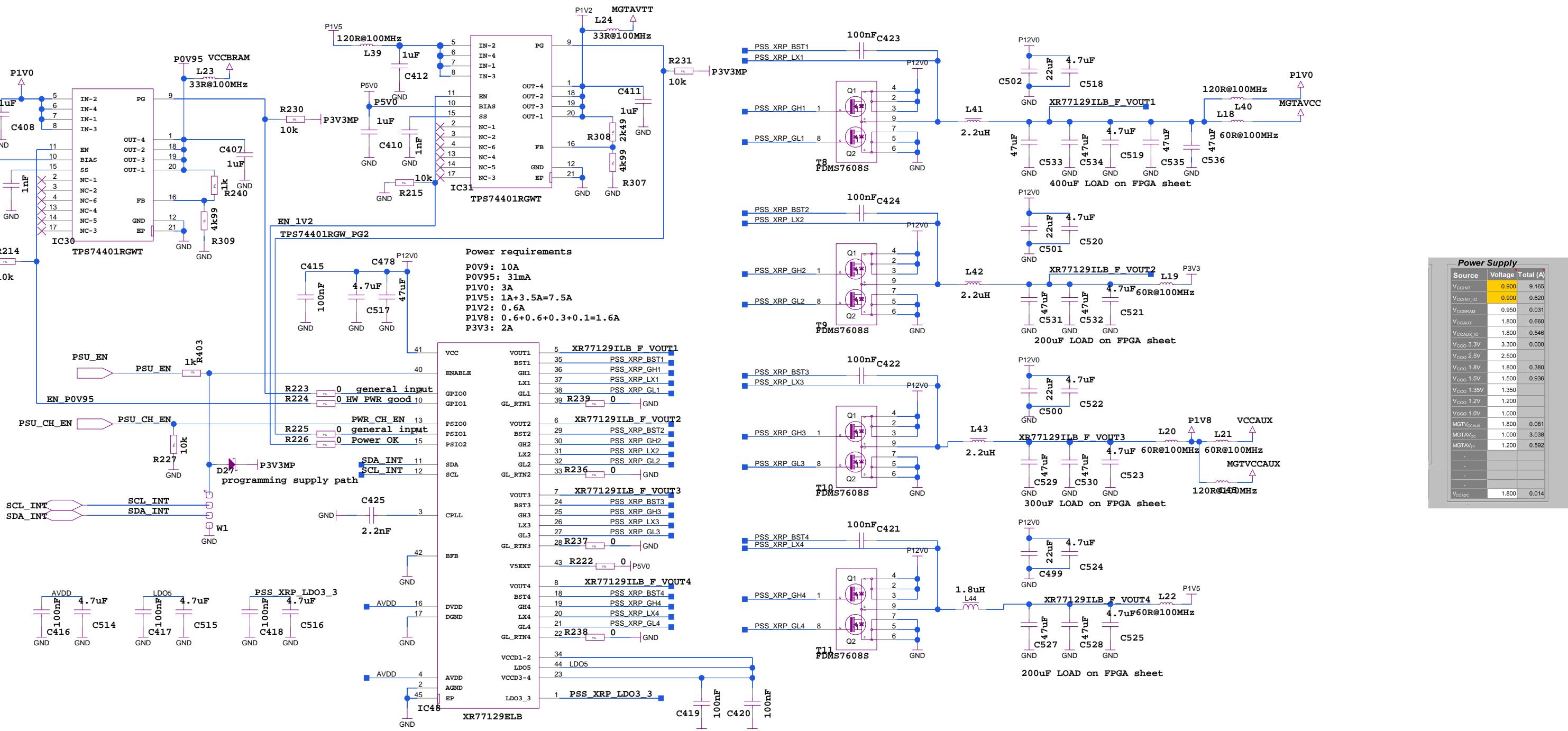


Power Supply		
Source	Voltage	Total (A)
V <sub>CCINT</sub>	0.900	9.165
V <sub>CCINT_IO</sub>	0.900	0.620
V <sub>CCBRAM</sub>	0.950	0.031
V <sub>CCAUX</sub>	1.800	0.660
V <sub>CCAUX_IO</sub>	1.800	0.546
V <sub>CCO 3.3V</sub>	3.300	0.000
V <sub>CCO 2.5V</sub>	2.500	
V <sub>CCO 1.8V</sub>	1.800	0.380
V <sub>CCO 1.5V</sub>	1.500	0.936
V <sub>CCO 1.35V</sub>	1.350	
V <sub>CCO 1.2V</sub>	1.200	
V <sub>CCO 1.0V</sub>	1.000	
MGTAV <sub>CCAUX</sub>	1.800	0.081
MGTAV <sub>CC</sub>	1.000	3.038
MGTAV <sub>TT</sub>	1.200	0.592
-	-	
-	-	
V <sub>CCADC</sub>	1.800	0.014

The recommended power-on sequence is VCCINT/VCCINT\_IO, VCCBRAM, VCCAUX/VCCAUX\_IO, and VCCO to achieve minimum current draw and ensure that the 1/0s are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCINT/VCCINT\_IO and VCCO have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. If VCCAUX/VCCAUX\_IO and VCCO have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. VCCAUX and VCCO must be connected together. When the current minimums are met, the device powers on after the VCCINT/VCCINT\_IO, VCCBRAM, VCCAUX/VCCAUX\_IO, and VCCO supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after VCCINT is applied. VCCADC and VREF can be powered at any time and have no power-up sequencing recommendations. The recommended power-on sequence to achieve minimum current draw for the GTH or GTx transceivers is VCCINT, VMGTAVCC, VMGTAVT, OR VMGTAVC, VCCINT, VMGTAVT. There is no recommended sequencing for VMGTAVCC, VMGTAVT, VCCINT, VMGTAVC and VCCINT can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from VMGTAVT can be higher than specifications during power-up and power-down.

# ARTIQ Sinara

## POWER\_Management

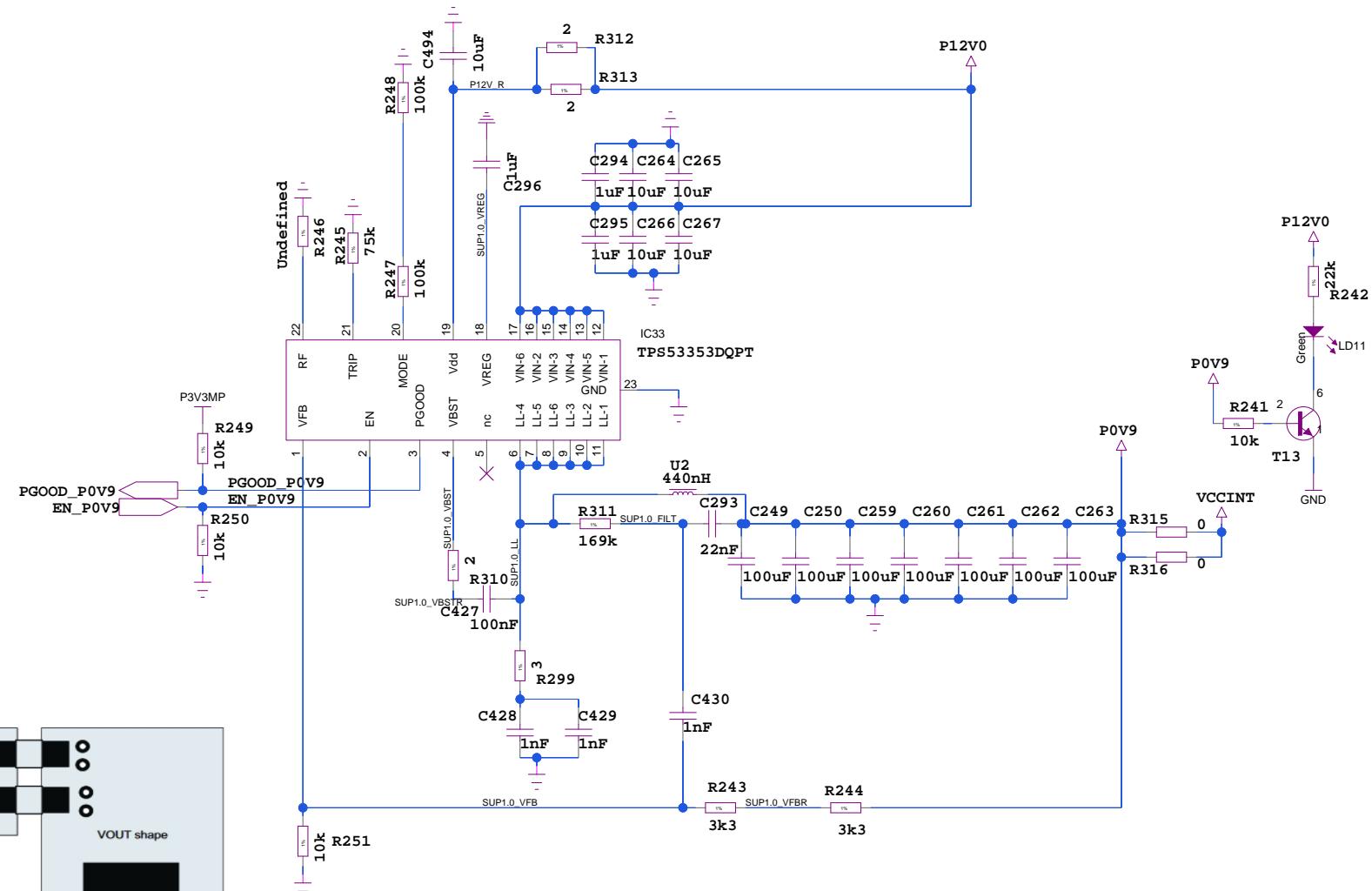
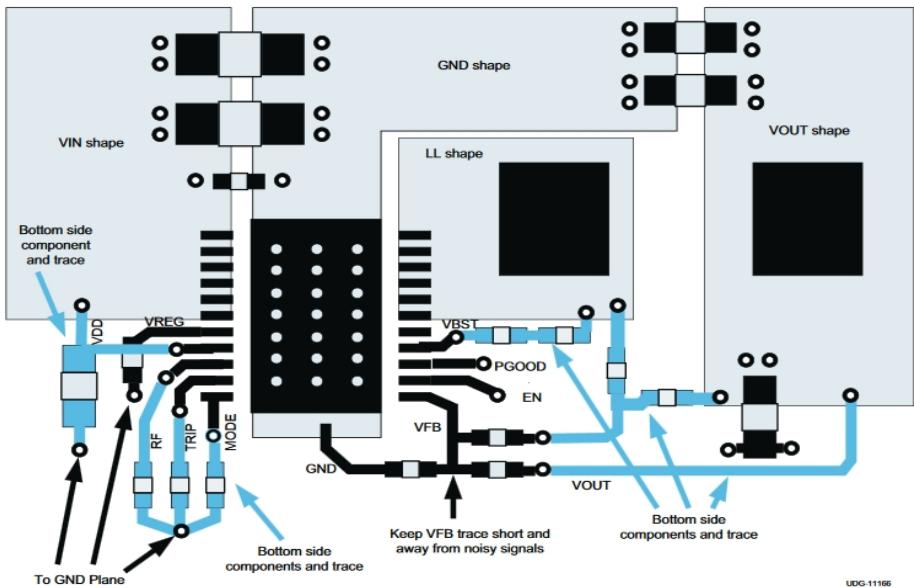


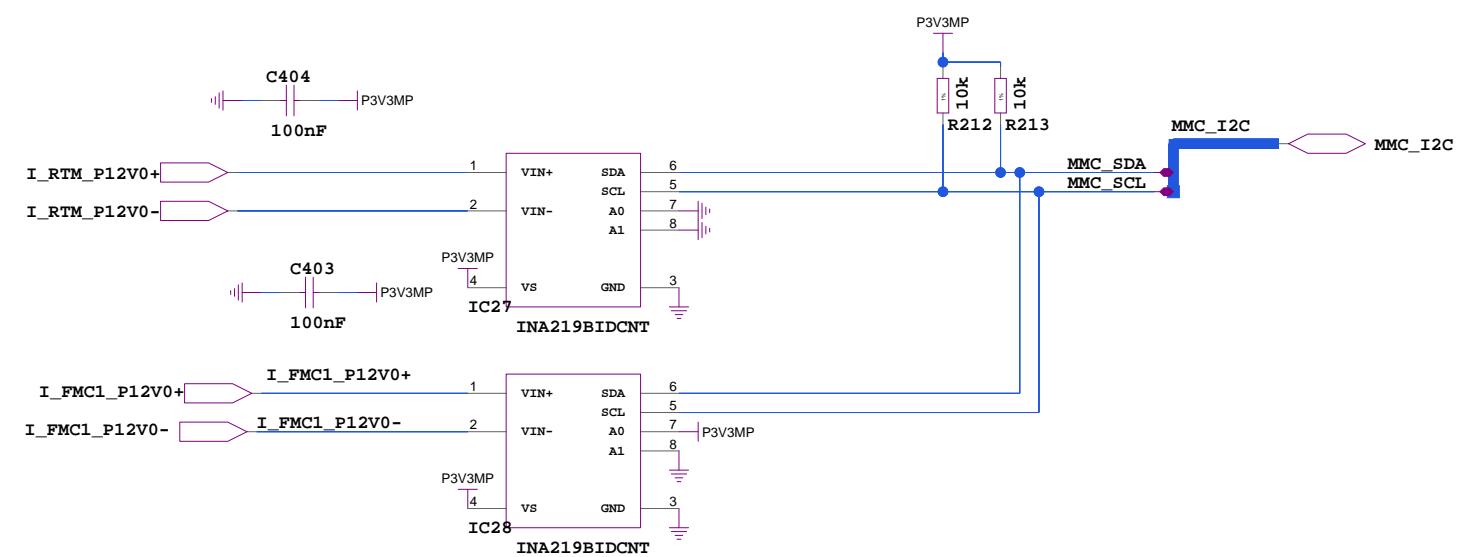
The recommended power-on sequence is VCCINT/VCCINT IO, VCCBRAM, VCCAUX/VCCAUX IO to achieve minimum current draw and ensure that the f<sub>1</sub>/f<sub>0</sub>s are 3-stated at power-on. The sequence is the reverse of the power-on sequence. In VCCINT and VCCAUX have the same recommended voltage levels, they can be powered by the same supply and VCCINT IO must be connected to VCCINT. VCCAUX IO and VCCAUX have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. When the current minimums are met, the device powers up. VCCINT/VCCINT IO, VCCBRAM, VCCAUX/VCCAUX IO, and VCCO must be connected together. Once the current minimums are met, the device powers up. VCCINT/VCCINT IO, VCCBRAM, VCCAUX/VCCAUX IO, and VCCO must be configured first after VCCINT has been ramped. VREFC and VREFB can be powered up simultaneously after VCCINT has been ramped. The recommended power-on sequence to no power-up sequencing recommendations. The recommended power-on sequence to minimum current draw for VMGTAUT/VMGTAUV or VMGTAUT/VMGTAUV is. There is no recommended sequencing for VMGTAUV/VCCAUX. Both VMGTAUV and VCCINT can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. Recommended sequencing specifications during power-down. The recommended sequencing specifications during power-down.

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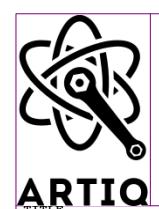
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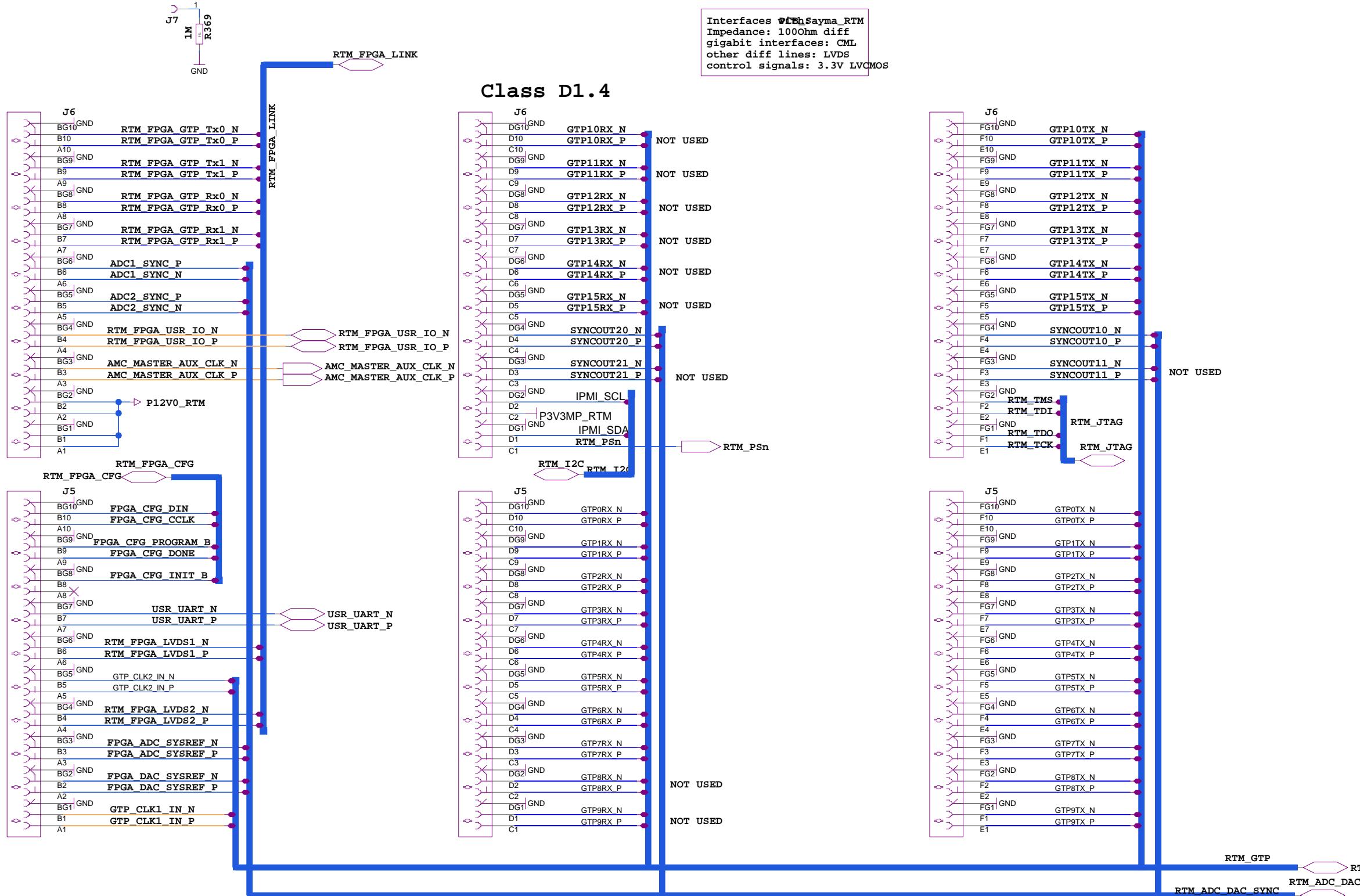
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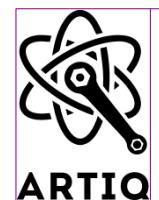
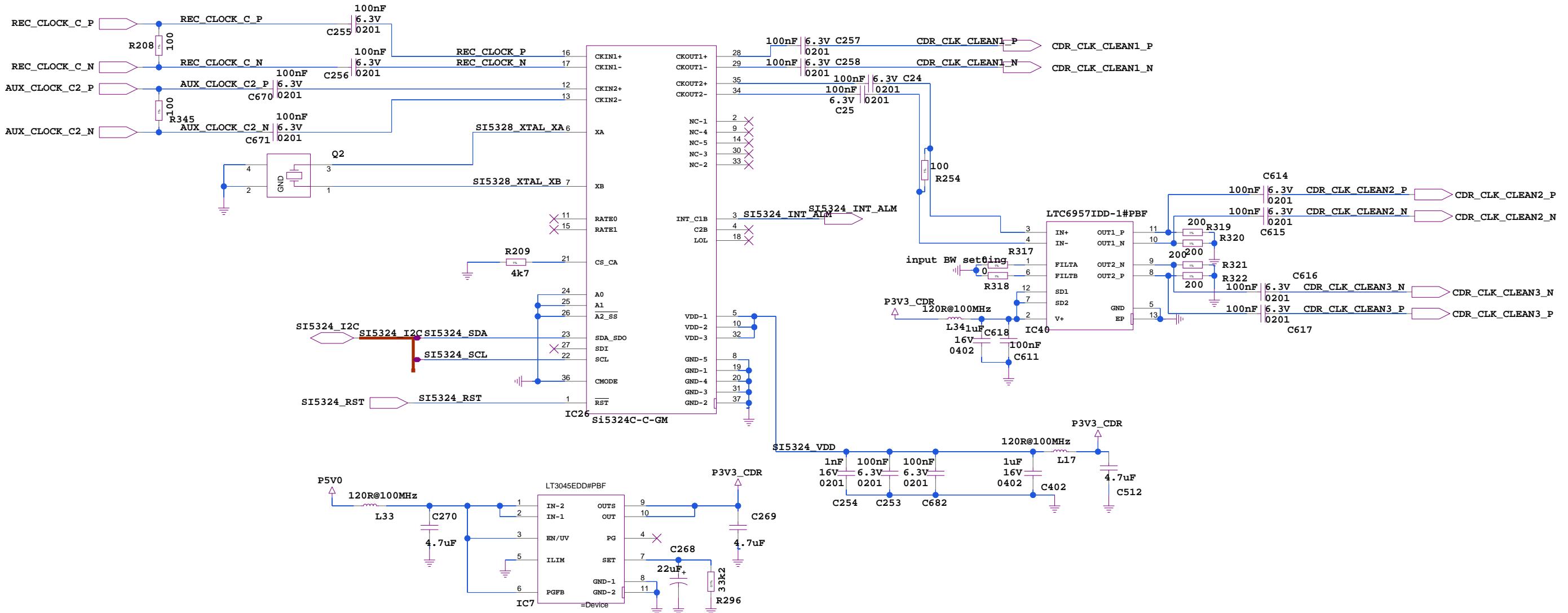


**ARTIQ Sinara**

**UI\_mon**

SIZE	DWG NO		
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<b>G.K.</b>		28	31
REV <b>v0.97</b>			
24/01/2017:23:15			



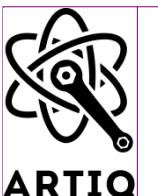
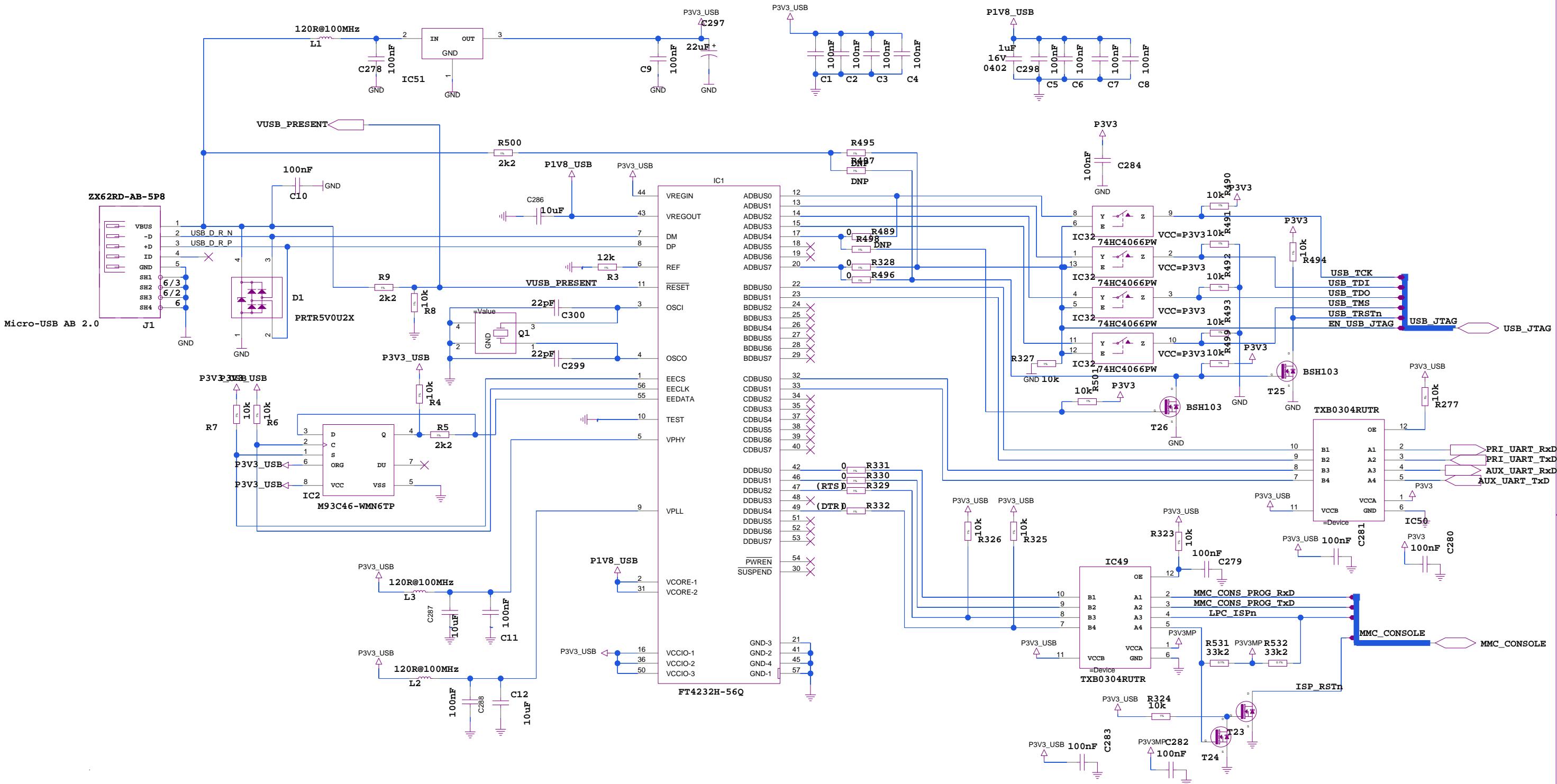


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# SI5324\_CLK\_RECOVERY

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SIZE	DWG NO	REV
A3		v0.97
DRAWN BY	SHEET of	
G.K.	30	31



# ARTIQ Sinara

# USB SERIAL QUAD

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