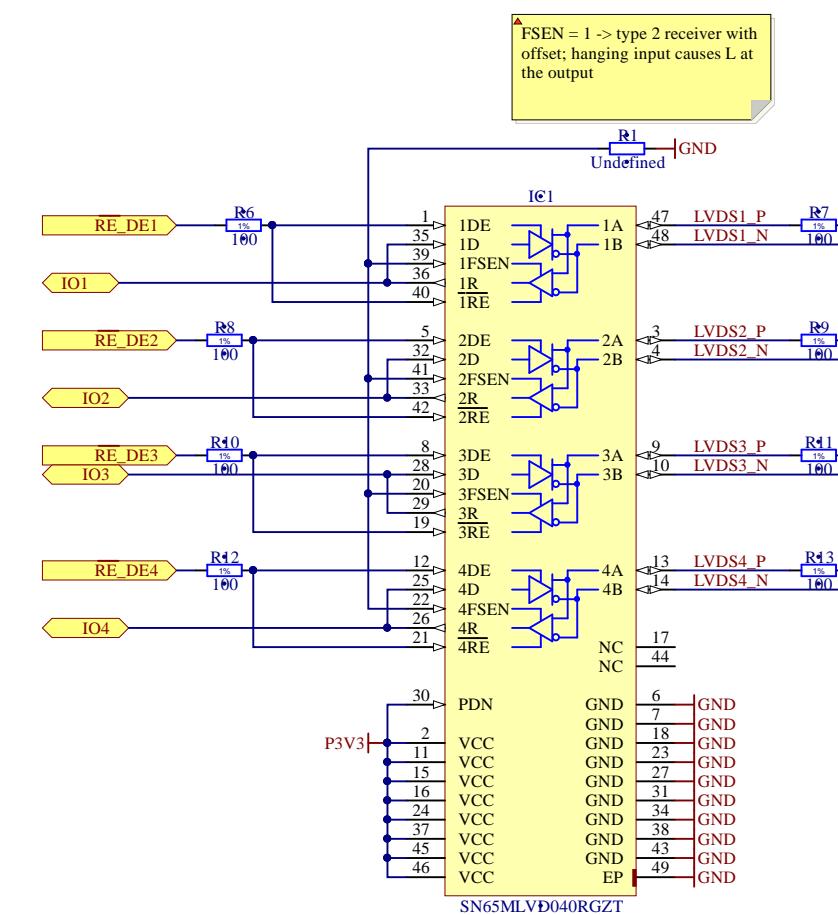
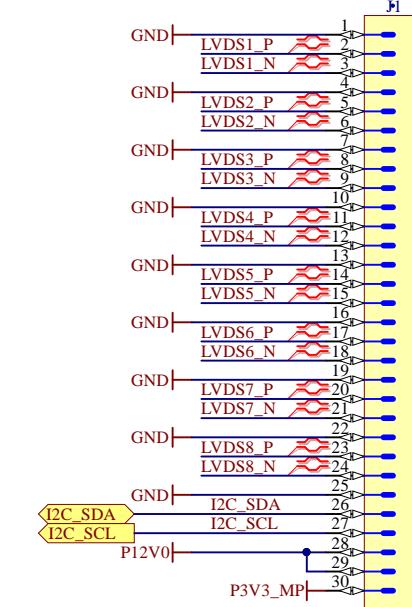




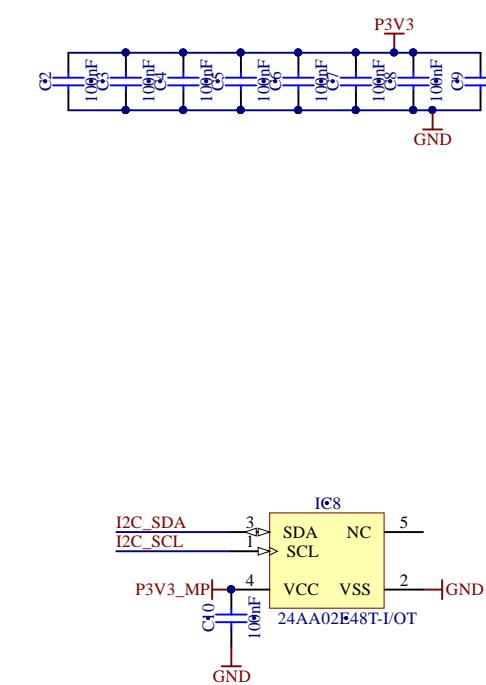
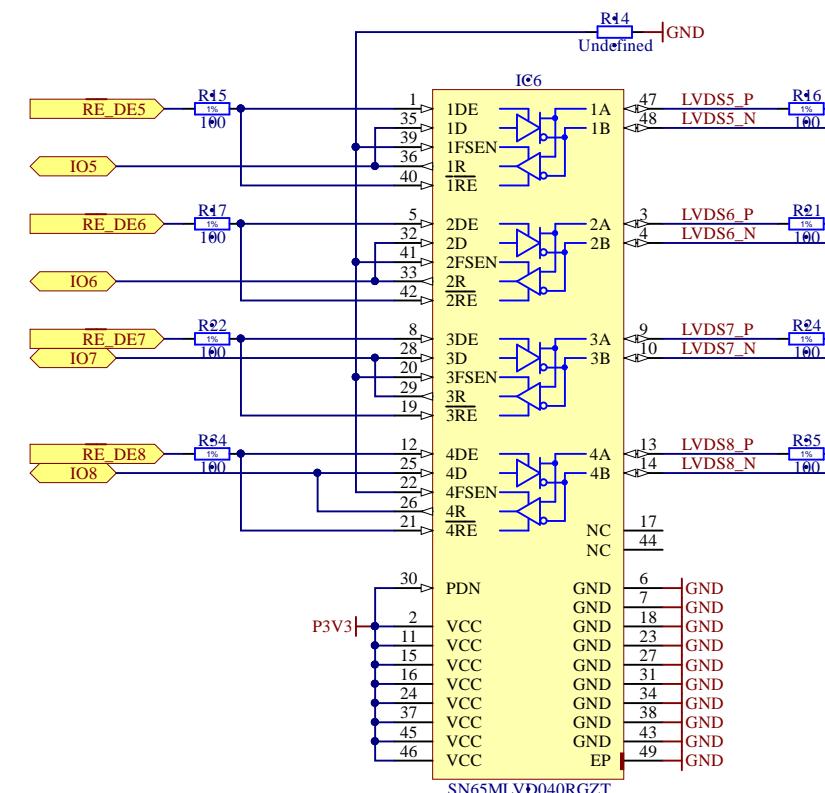
A



This module connects to Kasli or to VHDCI Metlino breakout board  
All signals are LVDS, in case of Metlino VCC is 1.8V  
I2C is 3.3V LVCMOS  
P3V3\_MP can handle up to 20mA  
P12V0 current is up to 500mA



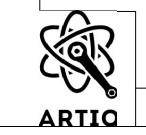
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Document



**PCB\_3U\_DDS.PjPCB**  
**LVDS\_IFC\_DDS.SchDoc**

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| Check by      | -                   |              |
| Last Mod.     | -                   | 20.05.2017   |
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Nowowiejska 15/19

ARTIQ

Size A3 Rev -

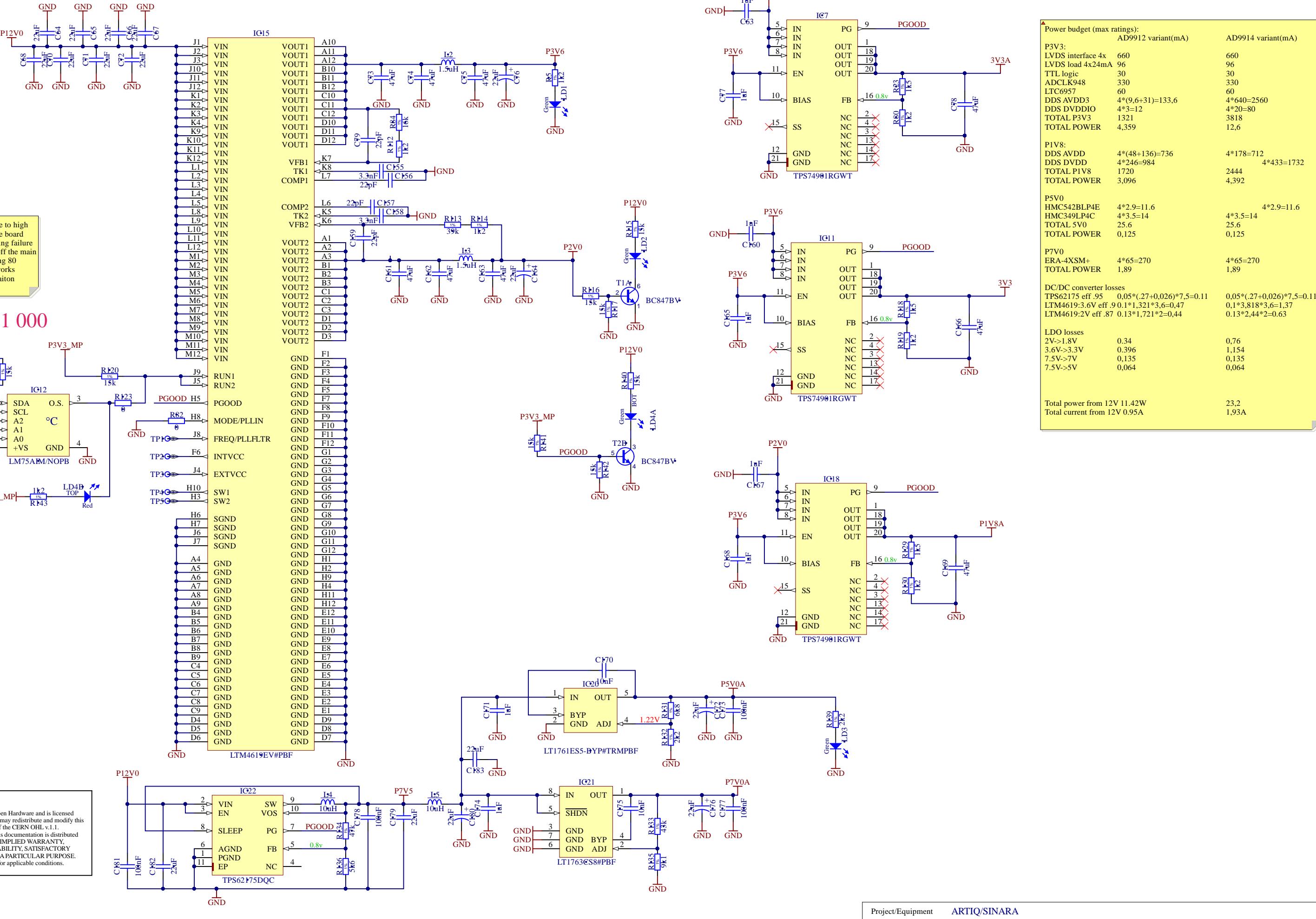
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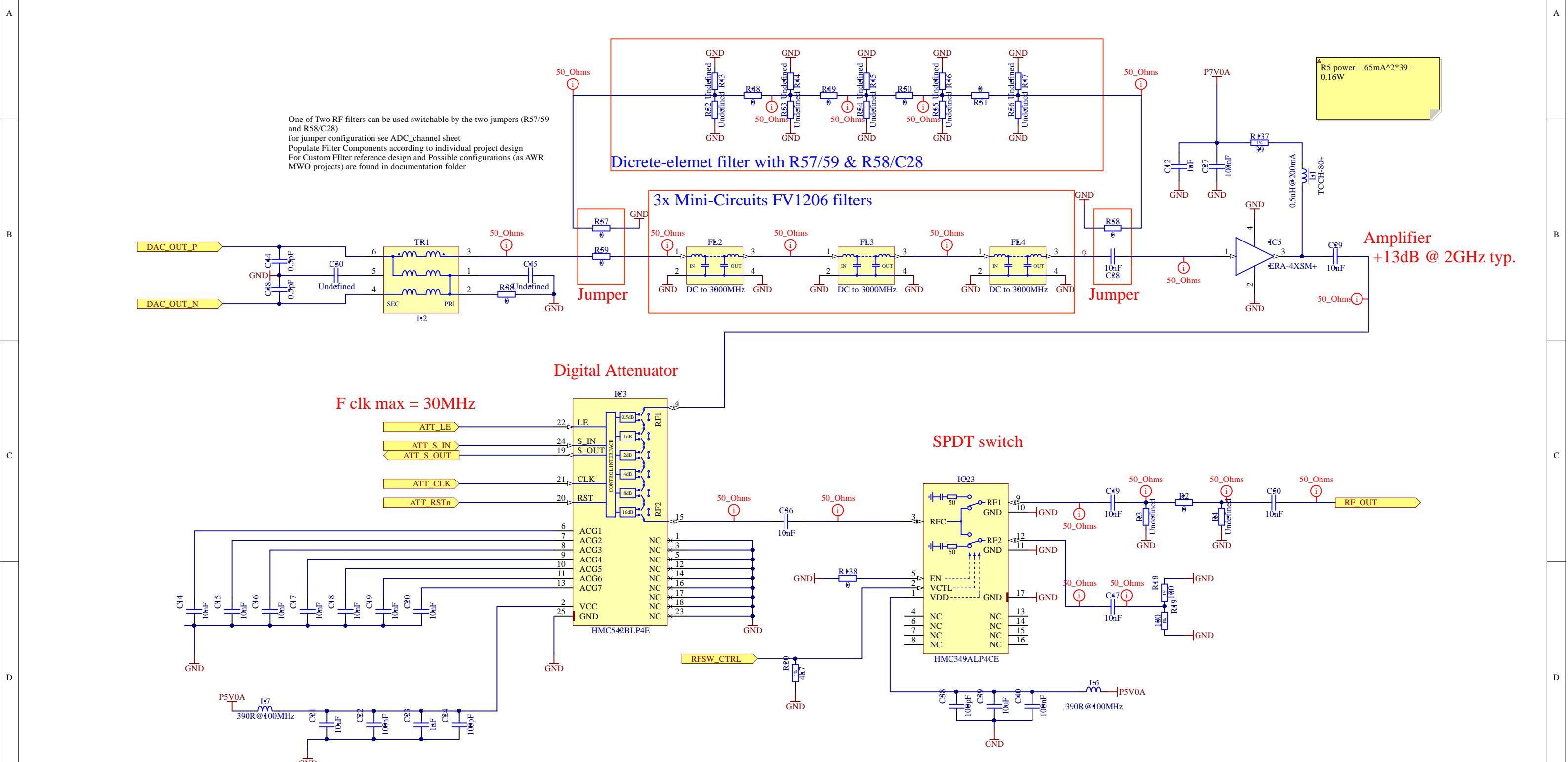
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4

5



| Power budget (max ratings):  |   |
|--|---|
| AD9912 variant(mA)   | AD9914 variant(mA)  |
| P3V3:<br>LVDS interface 4x 660<br>LVDS load 4x24mA 96<br>TTL logic 30<br>ADCLK948 330<br>LTC6957 60<br>DDS AVDD3 4*(9,6+31)=133,6<br>DDS DVDD 4*3=12<br>TOTAL P3V3 1321<br>TOTAL POWER 4,359 | 660<br>96<br>30<br>330<br>60<br>4*640=2560<br>4*20=80<br>3818<br>12,6 |
| P1V8:<br>DDS AVDD 4*(48+136)=736<br>DDS DVDD 4*246=984<br>TOTAL P1V8 1720<br>TOTAL POWER 3,096   | 4*178=712<br>4*433=1732   |
| P5V0<br>HMC542BLP4E 4*2.9=11.6<br>HMC349LP4C 4*3.5=14<br>TOTAL 5V0 25.6<br>TOTAL POWER 0,125   | 25.6<br>0,125   |
| P7V0<br>ERA-4XSM+ 4*65=270<br>TOTAL POWER 1,89   | 4*65=270<br>1,89  |
| DC/DC converter losses<br>TPS62175 eff .95 0,05*(.27+0,026)*7,5=0,11<br>LTM4619:3.6V eff .90 0,1*1,321*3,6=0,47<br>LTM4619:2V eff .87 0,13*1,721*2=0,44                                      | 0,05*(.27+0,026)*7,5=0,11<br>0,1*3,818*3,6=1,37<br>0,13*2,44*2=0,63   |
| LDO losses<br>2V->1.8V 0.34<br>3.6V->3.3V 0.396<br>7.5V->7V 0.135<br>7.5V->5V 0,064  | 0.76<br>1.154<br>0.135<br>0,064                                       |
| Total power from 12V 11.42W<br>Total current from 12V 0.95A  | 23.2<br>1.93A   |



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| Last Mod.         | -                      | -             | 21.05.2017    |
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|                   |                        | Size A3       | Rev -         |

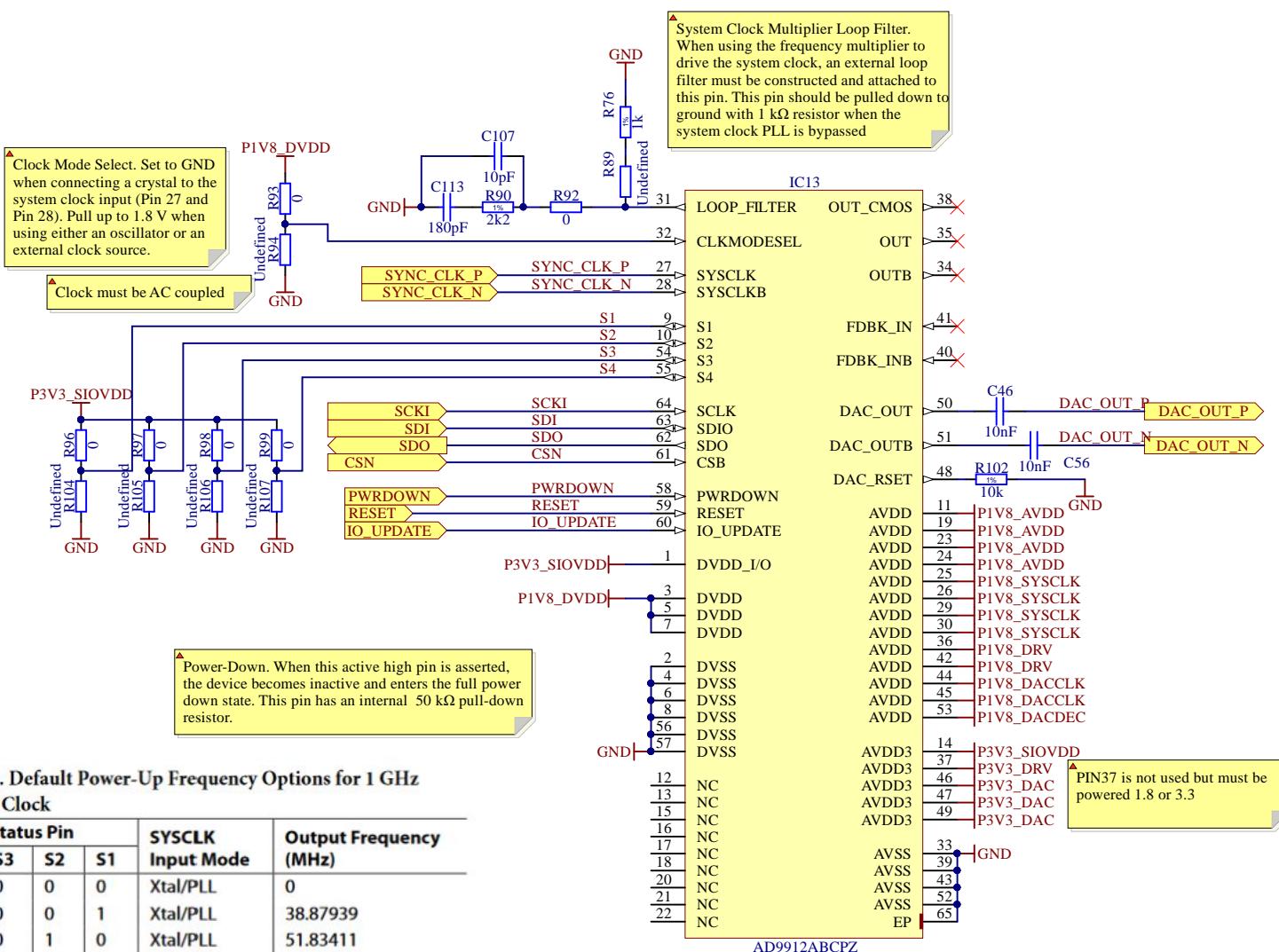
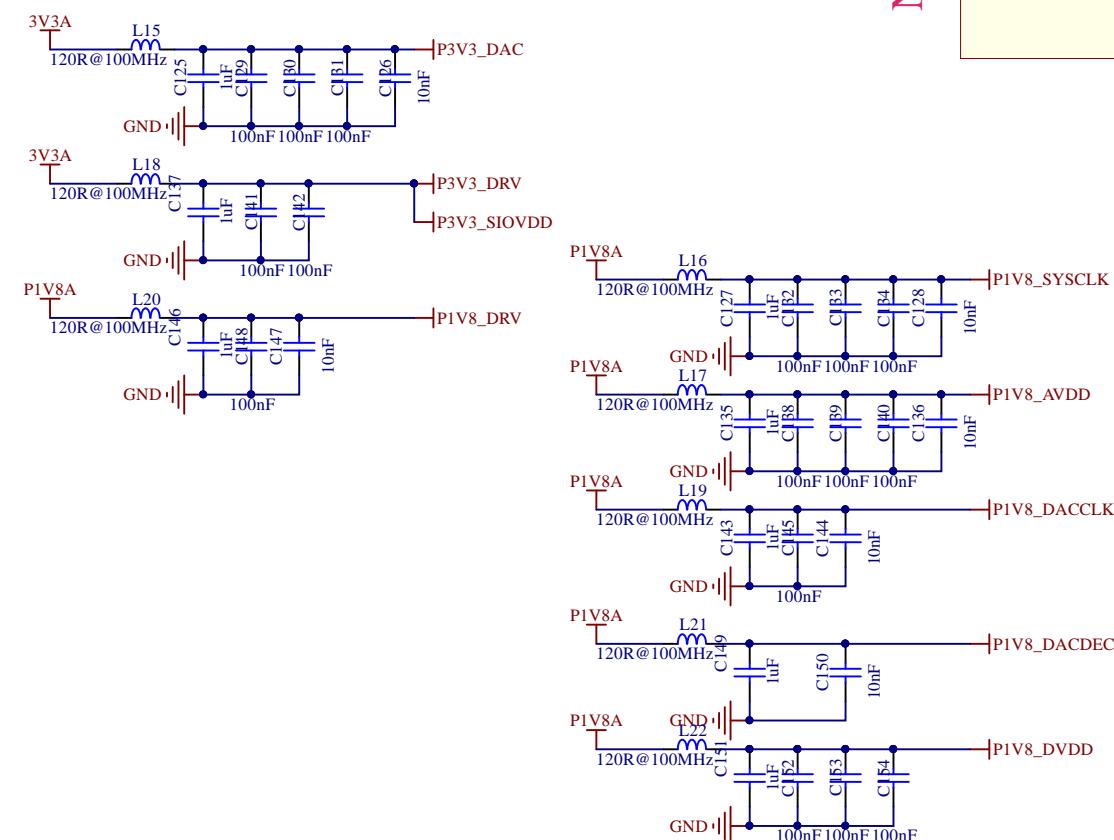
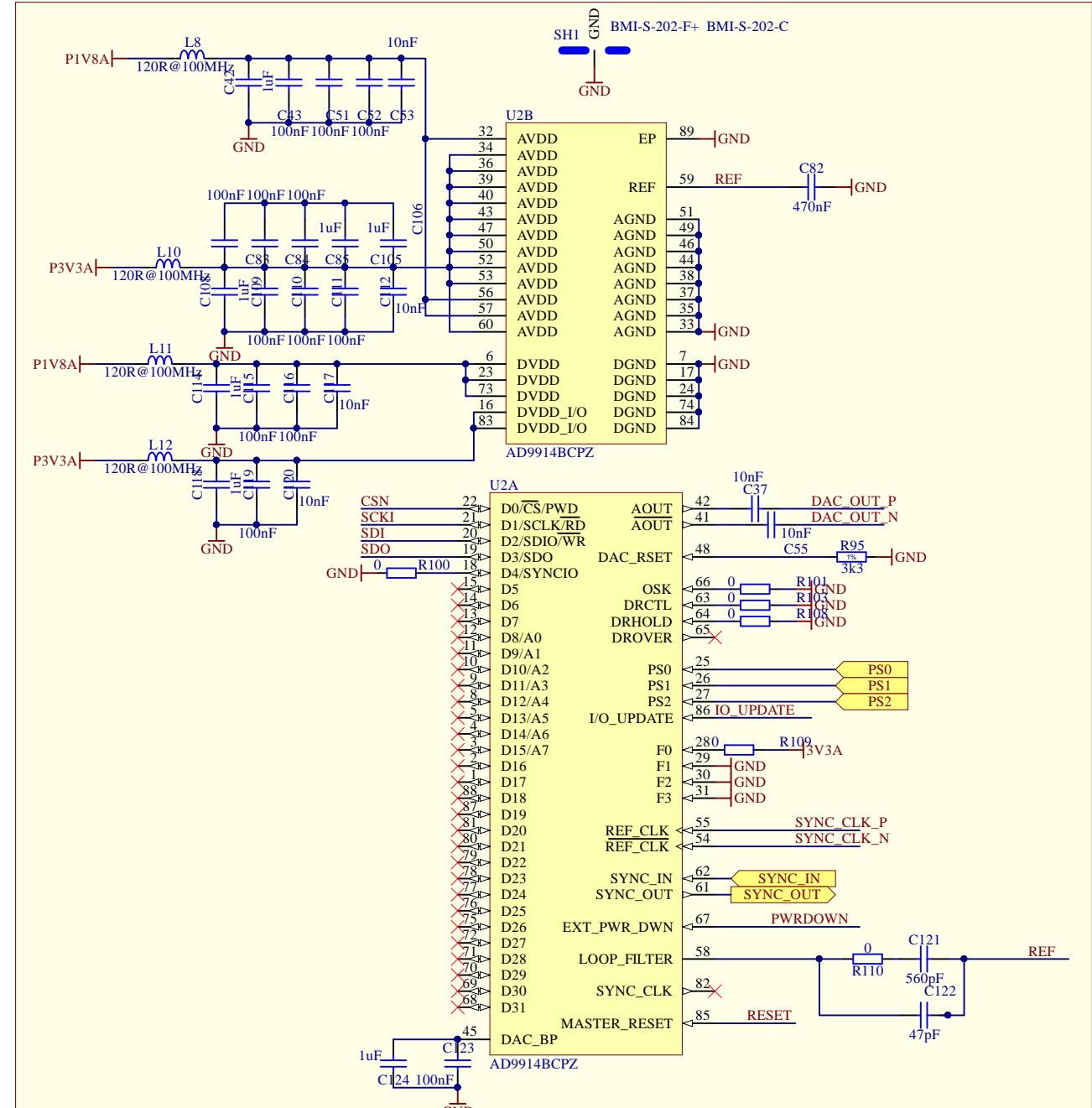


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

| Status Pin |    | SYSCLK Input Mode | Output Frequency (MHz) |           |
|------------|----|-------------------|------------------------|-----------|
| S4         | S3 | S2                | S1                     |           |
| 0          | 0  | 0                 | 0                      | Xtal/PLL  |
| 0          | 0  | 0                 | 1                      | 38.87939  |
| 0          | 0  | 1                 | 0                      | 51.83411  |
| 0          | 0  | 1                 | 1                      | 61.43188  |
| 0          | 1  | 0                 | 0                      | 77.75879  |
| 0          | 1  | 0                 | 1                      | 92.14783  |
| 0          | 1  | 1                 | 0                      | 122.87903 |
| 0          | 1  | 1                 | 1                      | 155.51758 |
| 1          | 0  | 0                 | 0                      | Direct    |
| 1          | 0  | 0                 | 1                      | 38.87939  |
| 1          | 0  | 1                 | 0                      | 51.83411  |
| 1          | 0  | 1                 | 1                      | 61.43188  |
| 1          | 1  | 0                 | 0                      | 77.75879  |
| 1          | 1  | 0                 | 1                      | 92.14783  |
| 1          | 1  | 1                 | 0                      | 122.87903 |
| 1          | 1  | 1                 | 1                      | 155.51758 |



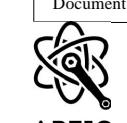
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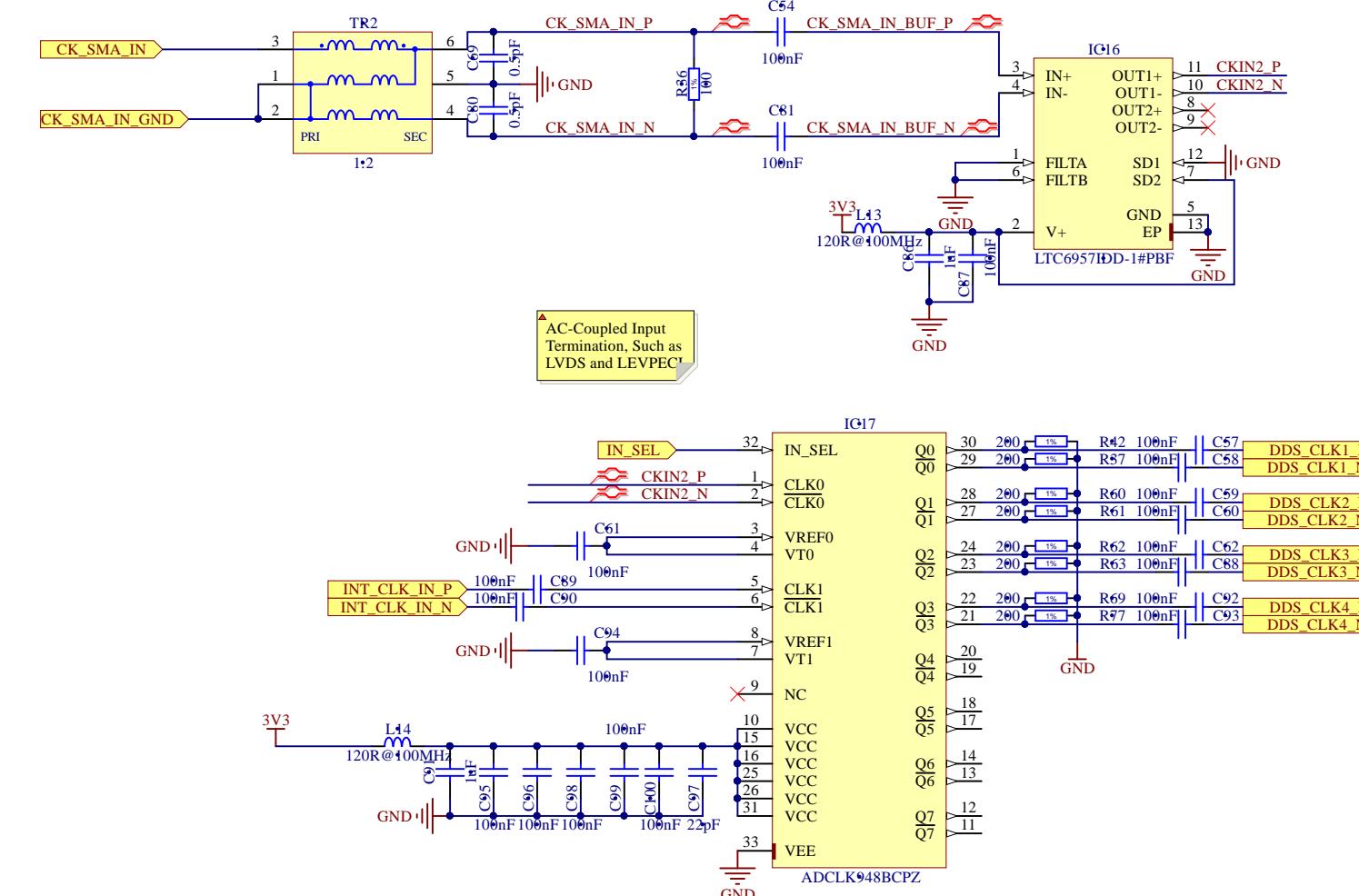
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**PCB\_3U\_DDS.PjPCB**  
**DDS\_channel.SchDoc**

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| Drawn by   | G.K.                |
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| Print Date | 21.05.2017 16:47:55 |
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3



*PCB\_3U\_DDS.PrjPCB*  
*CLK INPUT.SchDoc*

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| Designer    | G.K.                |              |
| Drawn by    | G.K.                | XX/XX/XXXX   |
| Check by    | -                   |              |
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| File        | CLK_INPUT.SchDoc    |              |
| Print Date  | 21.05.2017 16:47:55 | Sheet 6 of 7 |

