

A

A

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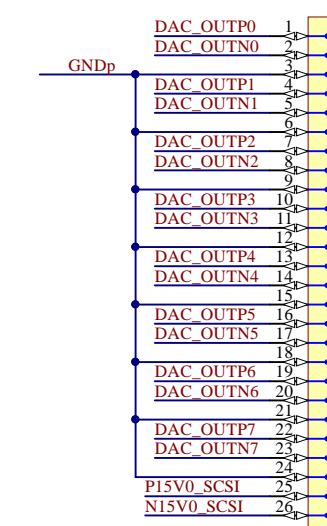
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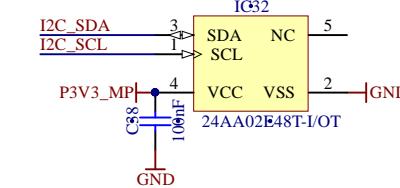
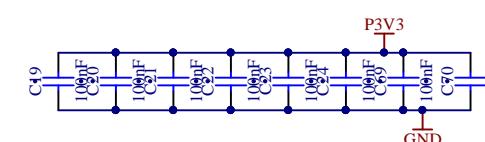
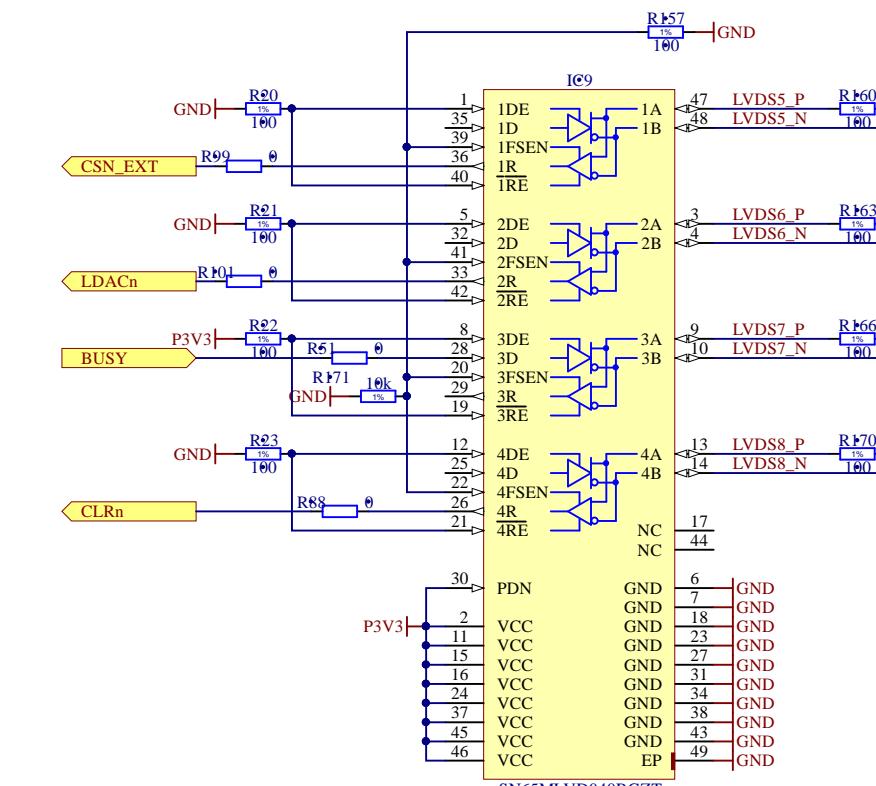
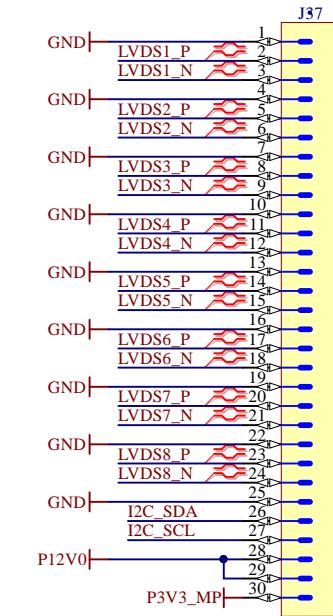
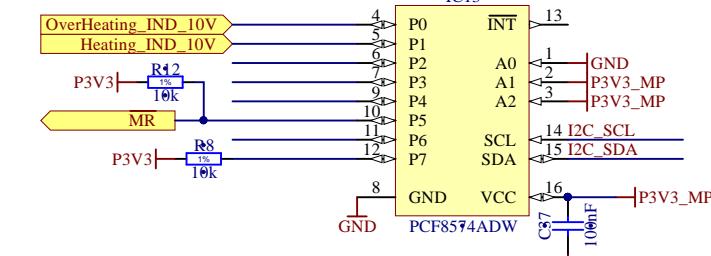
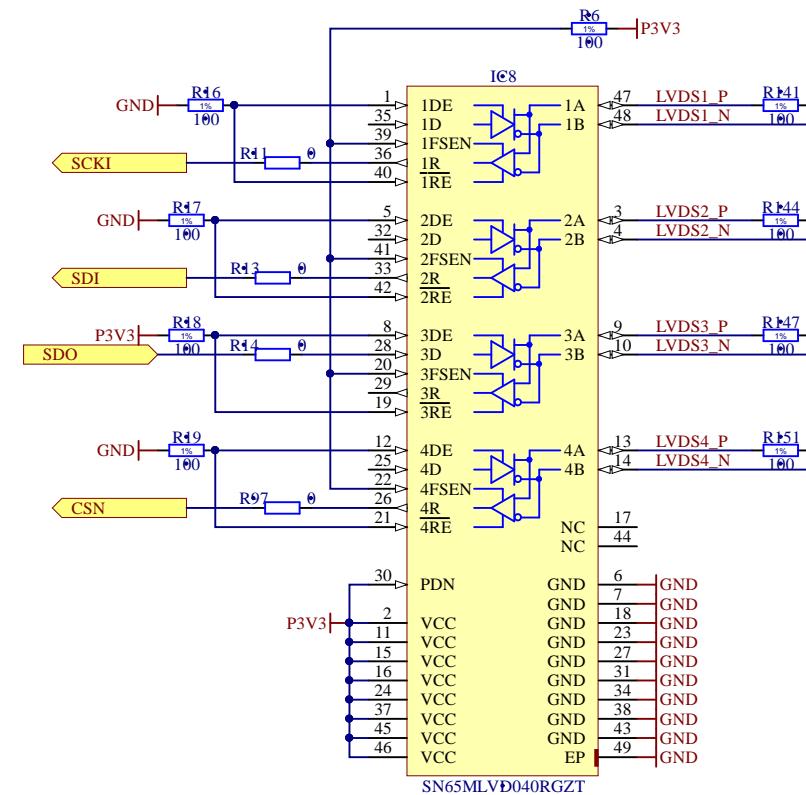
E

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| Project/Equipment | ARTIQ/SINARA | Document | Designer G.K. |
| | | | Drawn by G.K. |
| | | | Check by - |
| | | Last Mod. - | 30.04.2017 |
| | | File IDC2BNC.SchDoc | Print Date 02.05.2017 01:36:37 |
| | | | Sheet of A3 Rev - |
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This module connects to Kasli or to VHDCI Metlino breakout board
 All signals are LVDS, in case of Metlino VCC is 1.8V
 I2C is 3.3V LVCMOS
 P3V3_MP can handle up to 20mA
 P12V0 current is up to 500mA



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Document

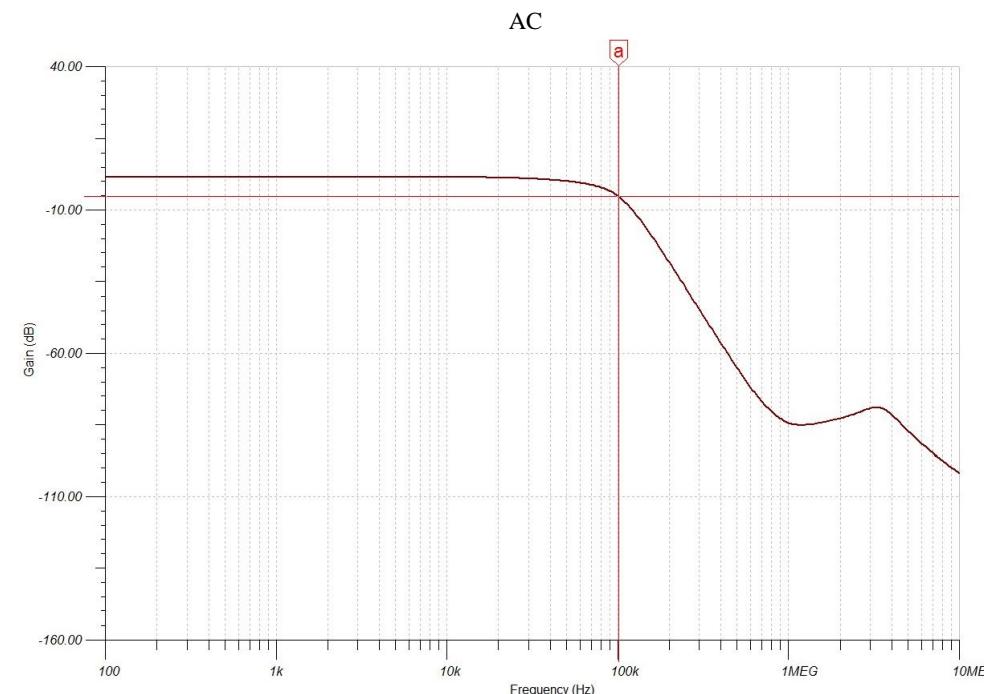
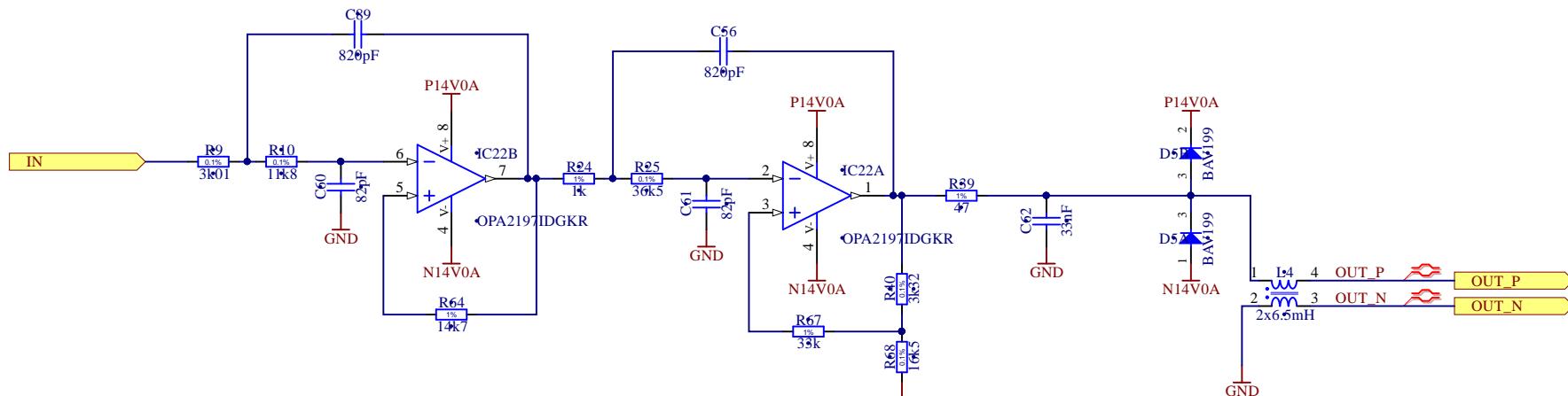


LVDS & I2C interfaces

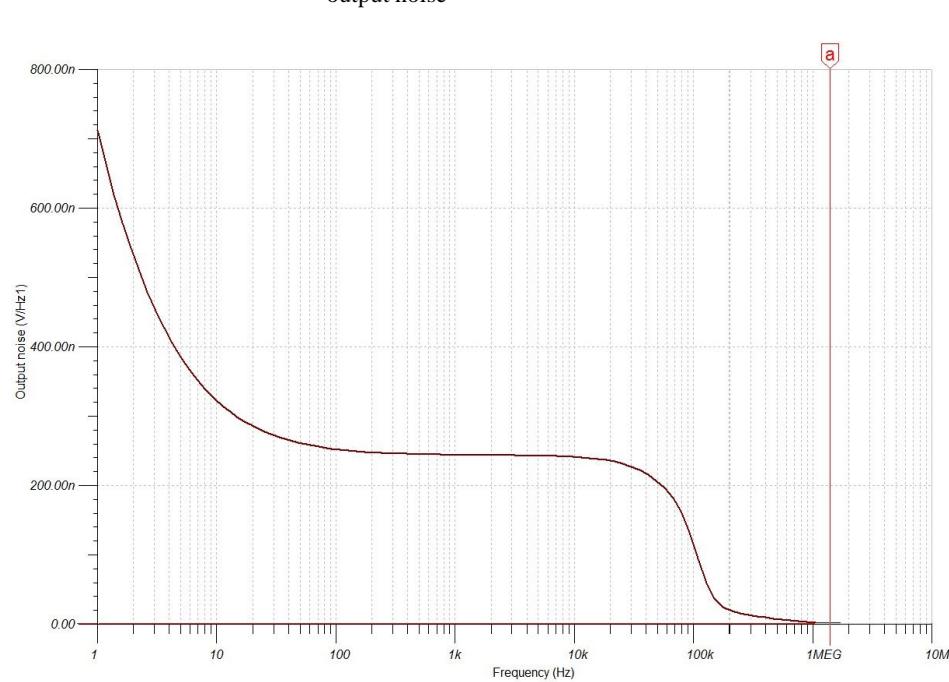
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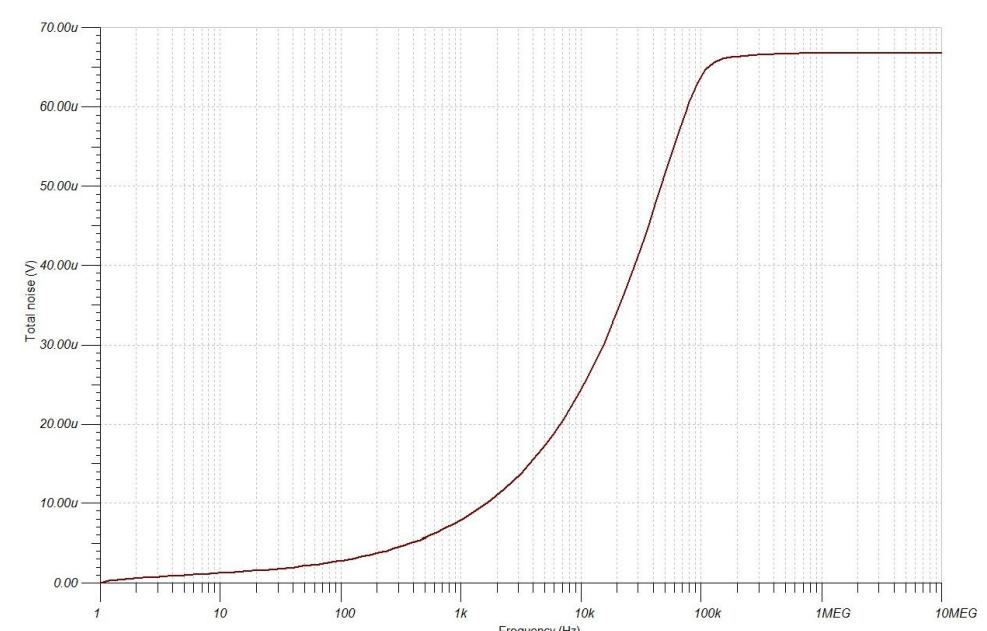
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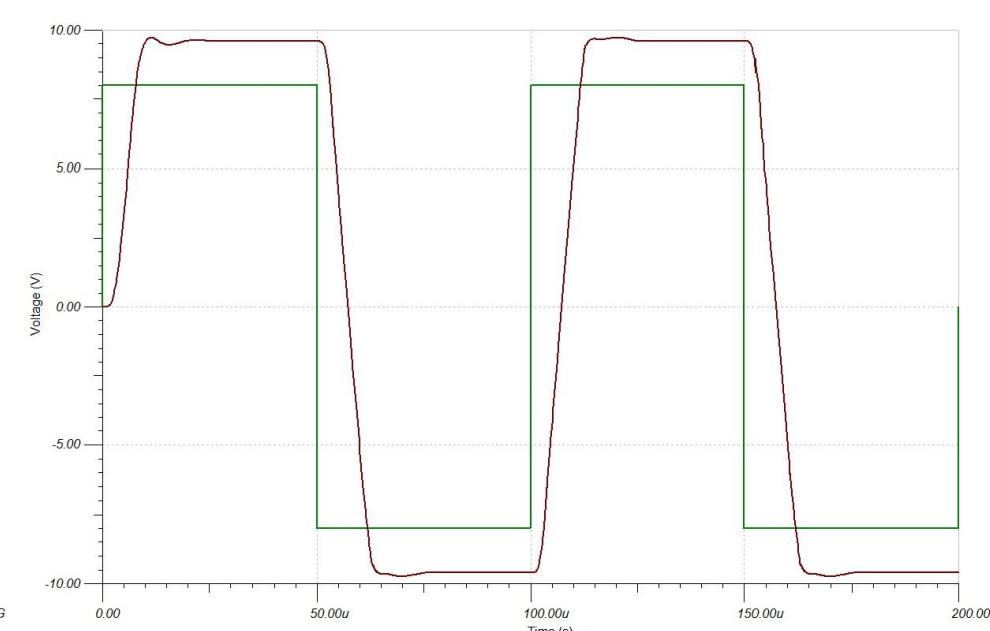
output noise



total noise



transient



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Document



Output filter

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| Last Mod. - | - | 01.05.2017 |
| File Output_channel.SchDoc | Print Date 02.05.2017 01:36:37 | Sheet of A3 Rev - |
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ARTIQ

Channel count: 32 channels from a single 32 channel DAC
 update rate: 10 channels simultaneously at >100kSPS (assume SPI running at 50MHz)
 Outputs: +12V
 Resolution: 16 bits
 Bandwidth:
 differential: Butterworth response with 100kHz cut-off
 common-mode: suitable chokes and common-mode filter to keep worst-case channel-channel cross-talk <-60dB when driving 1MHz sine into a high-impedance load using a 5m cable.
 Recommendation should also be made for common-mode/differential mode Rx filter as part of this design (will be required for testing).
 Output drive: the outputs should be able to drive 5m of SCSI cable with a 100kHz full-scale sinusoid without significant degradation of bandwidth, SFDR etc.
 Low-frequency noise: 0.1Hz - 1kHz noise < 10ppm RMS
 Integrated noise - 10Hz to 20MHz integrated noise < 30ppm RMS.
 Noise density - <1nVrtHz for all frequencies >=1MHz (includes both white noise and output spurs due to SMPSs, DAC clocks, etc.)
 Drift: <10ppm over 24 hours in a +/-1K "lab" environment
 Connectors:
 1xHD68 (SCSI III) connector on front panel. 32 twisted pairs used for the DACs (1 conductor of each pair is GND), 2 pairs used for +15V, GND.
 4 10x2 100mil header on the PCB, each providing 8 DAC channels, +15V. (If room, also add unregulated +12V to this header).

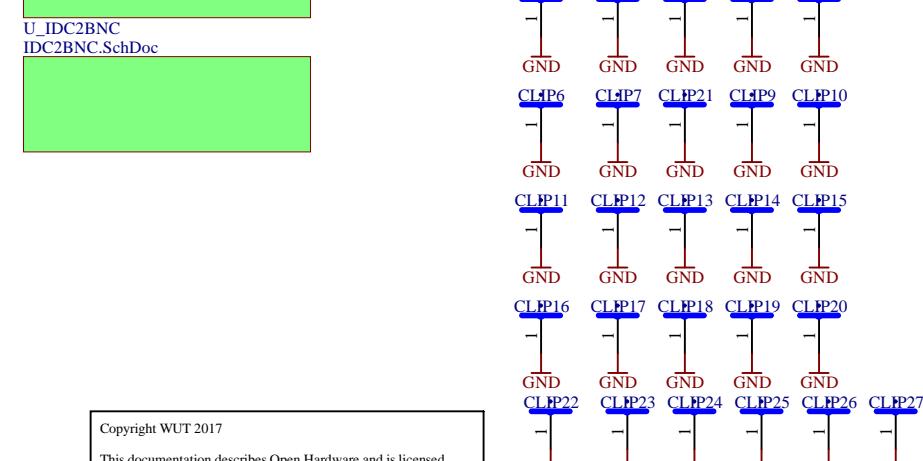
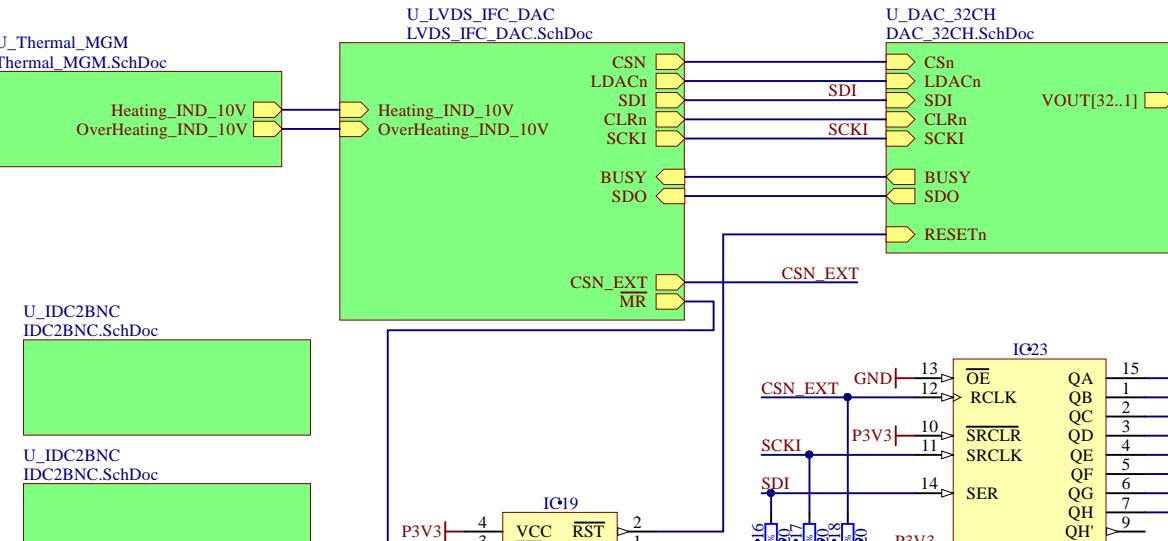
We additionally design a 3U passive (straight through) BNC breakout board. Up to 4 of these can be connected to the headers to break the DAC channels out onto BNCs for low-density applications. It is anticipated that the HD68 will be DNP when these boards are used.

DIO: "Standard" Kasli extension board connections (I2C, 8xLVDS, power, etc) either from pin header or backplane. Will require switching/jumpers to select BP & header. 5xLVDS lines used for DAC SPI bus: CLK, MOSI, MISO, SYNC, LDAC

Thermal: ideally, this board should be designed to operate (and meet drift specification) without forced air cooling (e.g. suitable heat-sinks and choice of lowish power OpAmps). If not possible, add suitable fans/etc.

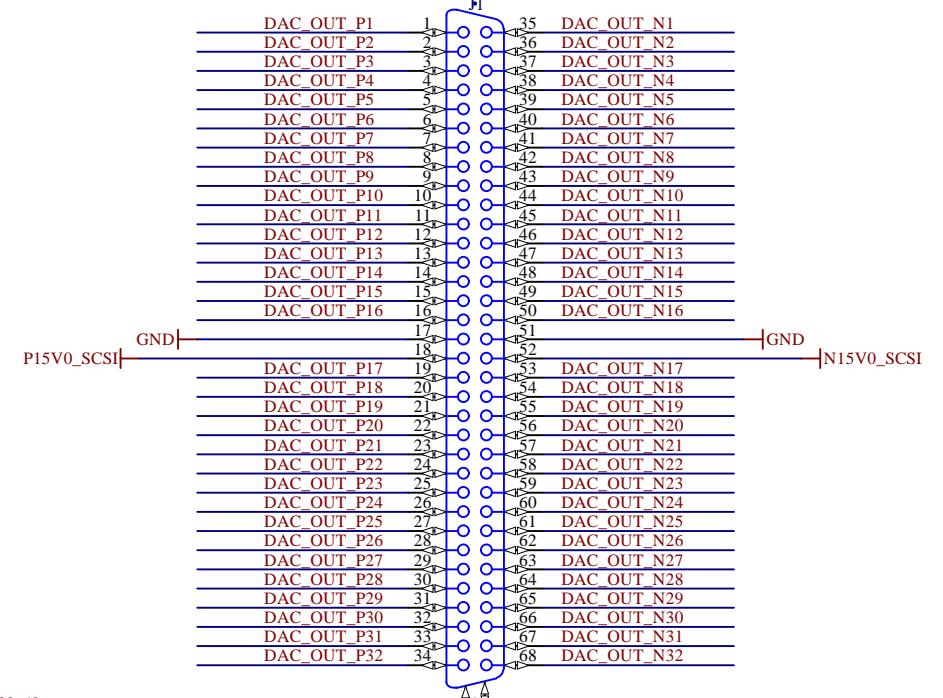
Screening: as required to ensure noise specifications are met in a realistic EMI environment (e.g. adjacent Kasli etc).

Misc: EEPROM etc per Kasli extension standard



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SHIELD for PSU

SHIELD for analog part

move fragile components to top

increase load resistance of gain amp

FIG1
FIG2
FIG3
FIG4



Project/Equipment ARTIQ/SINARA

Document

32 CHANNEL 16 BIT DAC - TOP

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| Designer G.K. | |
| Drawn by G.K. | |
| Check by | - |
| Last Mod. - | 01.05.2017 |
| File PCB_3U_DAC.schdoc | |
| Print Date 02.05.2017 01:36:37 | |
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| Size A3 | |

Rev -

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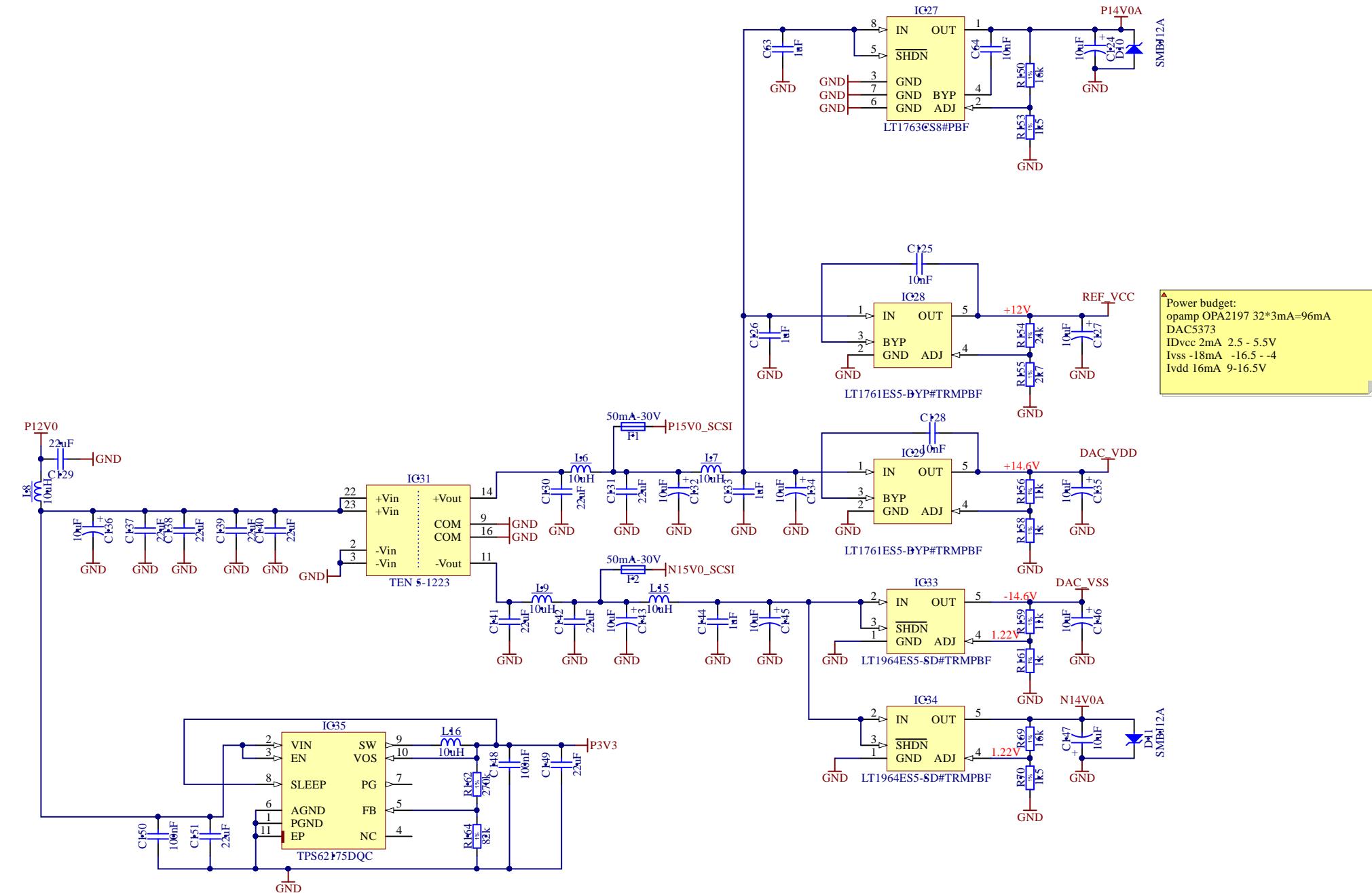
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Project/Equipment ARTIQ/SINARA

Document

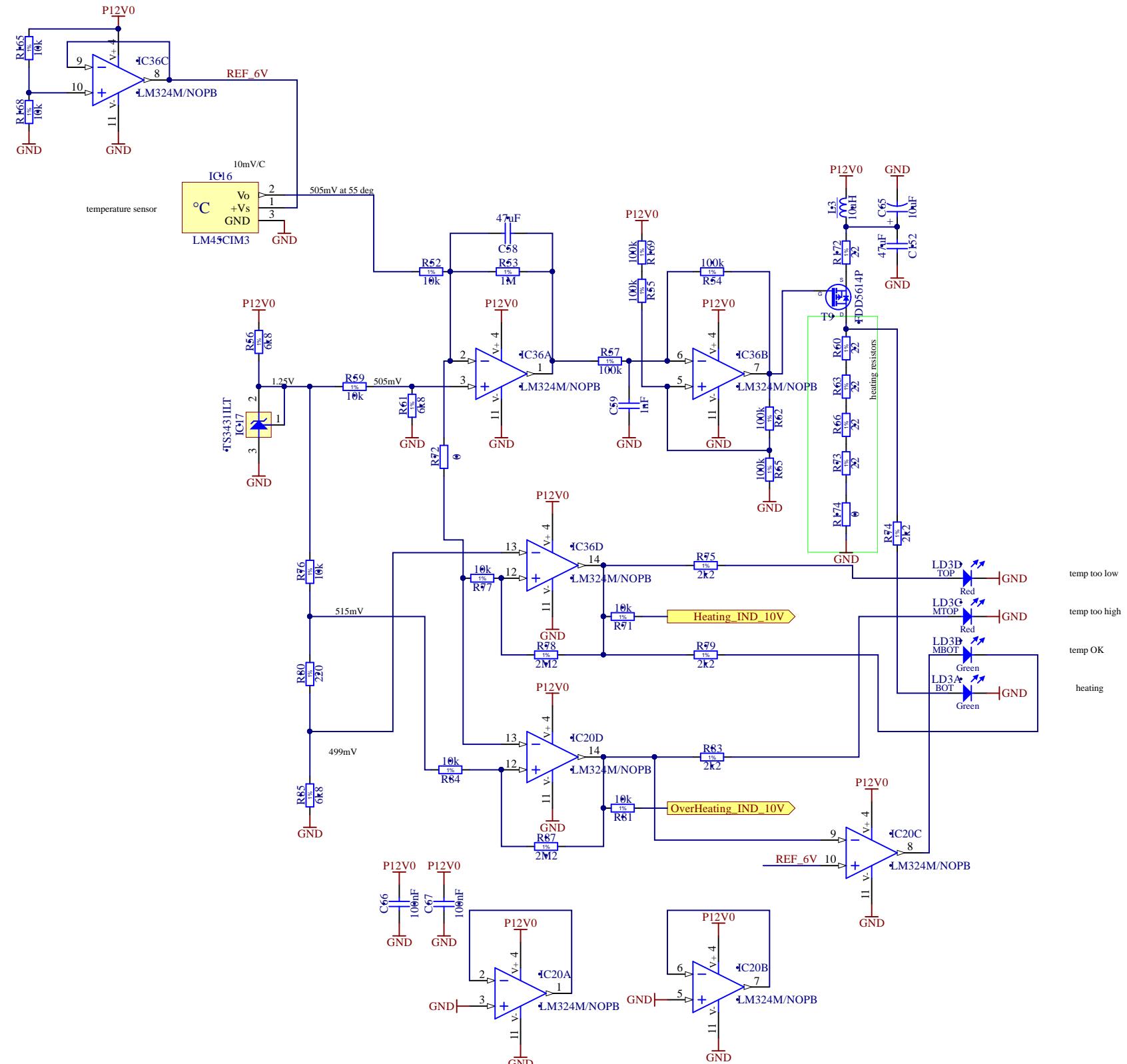


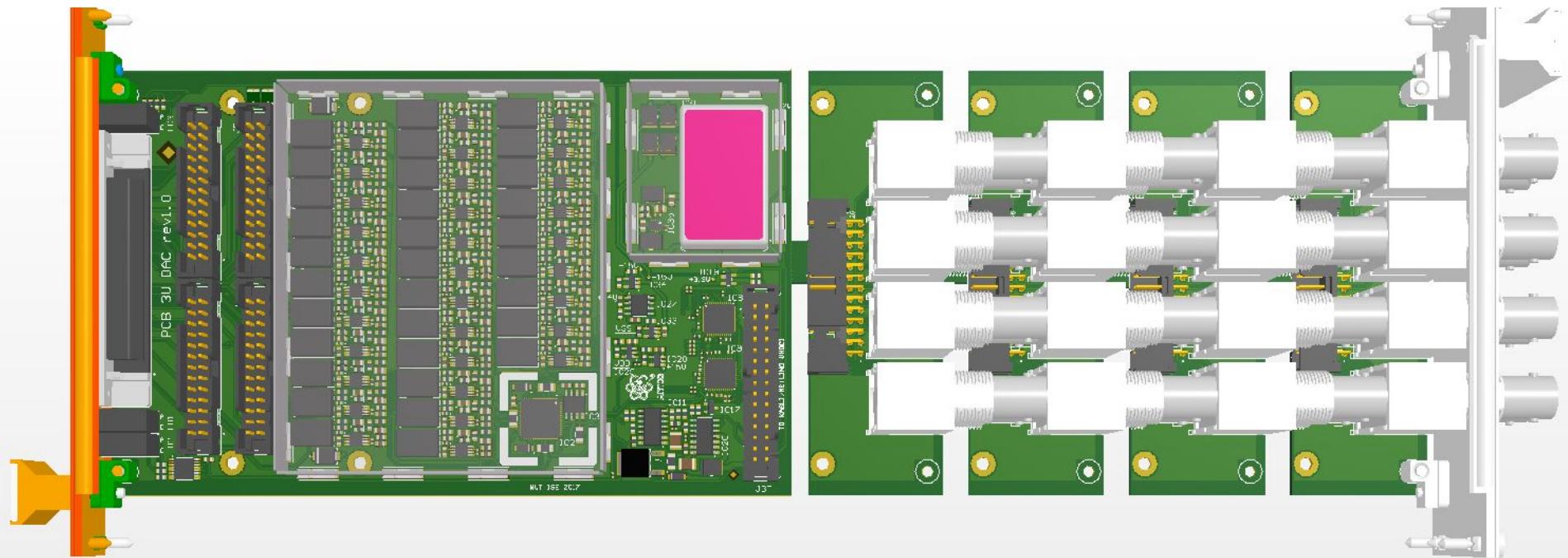
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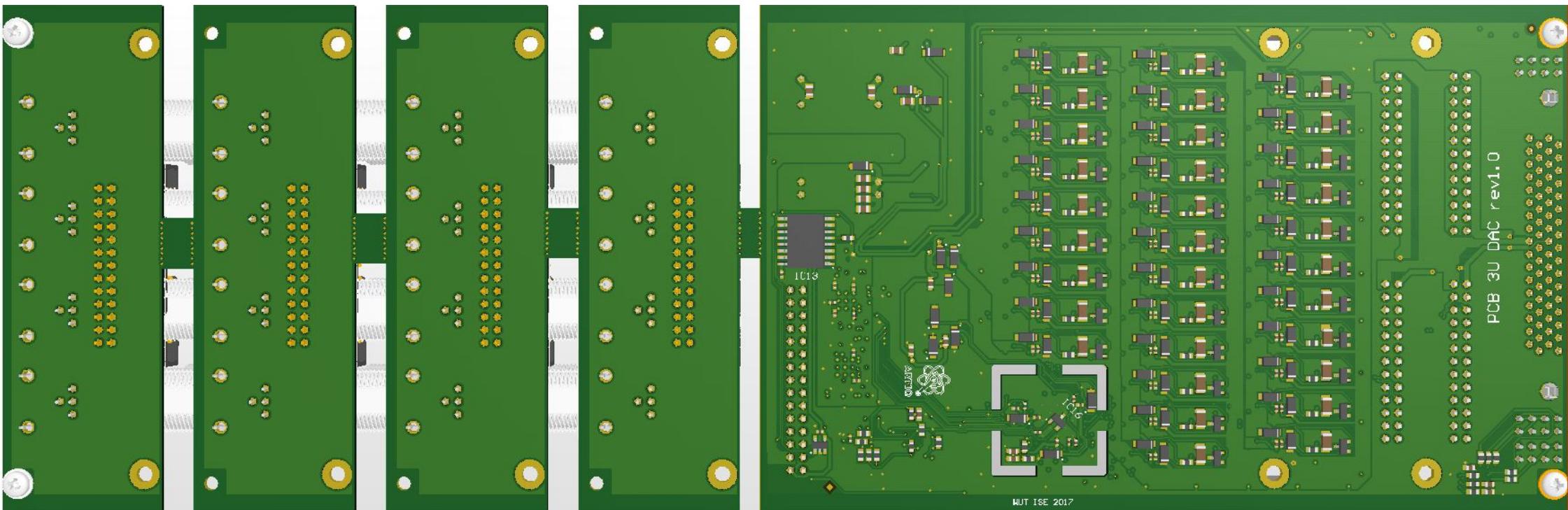
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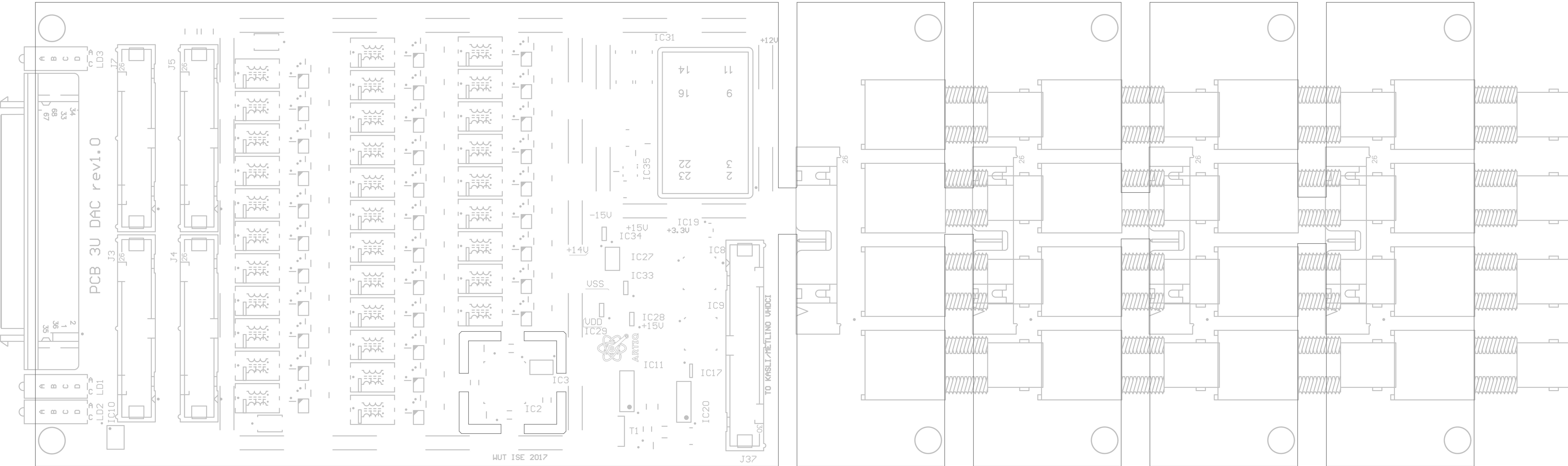
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| Last Mod. - | - | 01.05.2017 |
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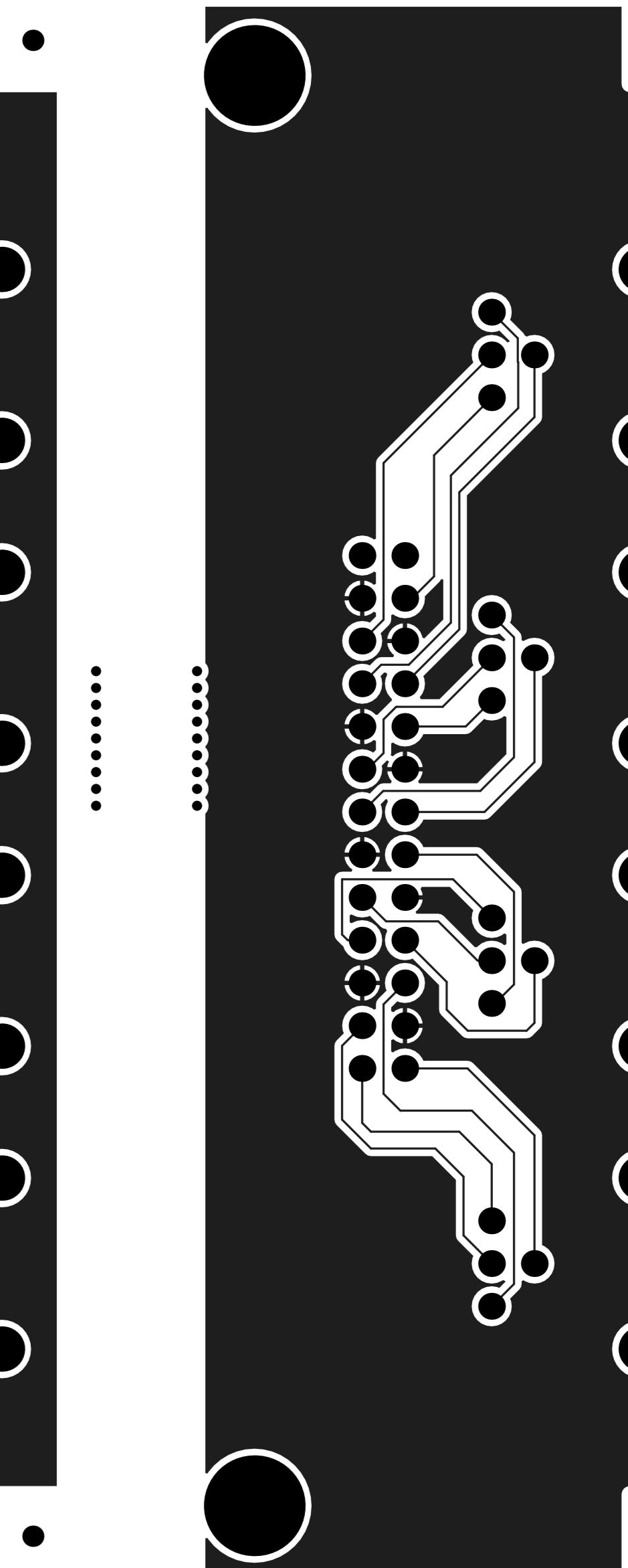
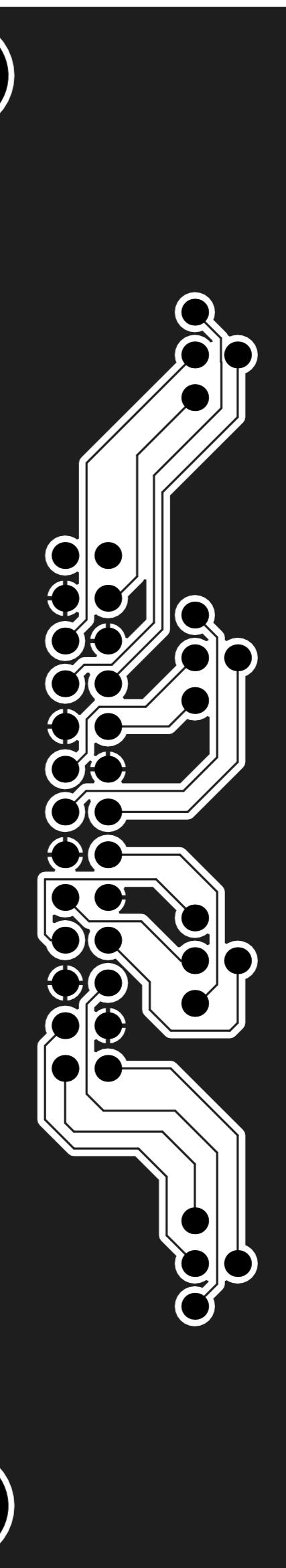
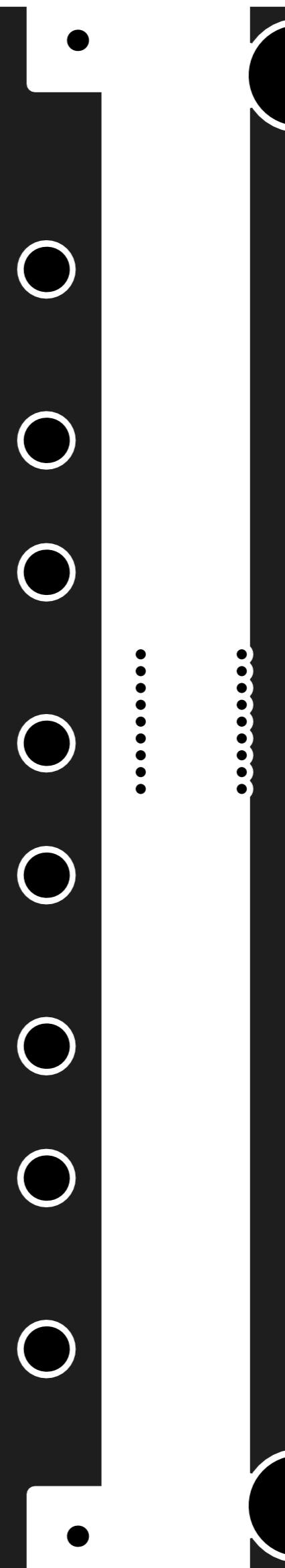
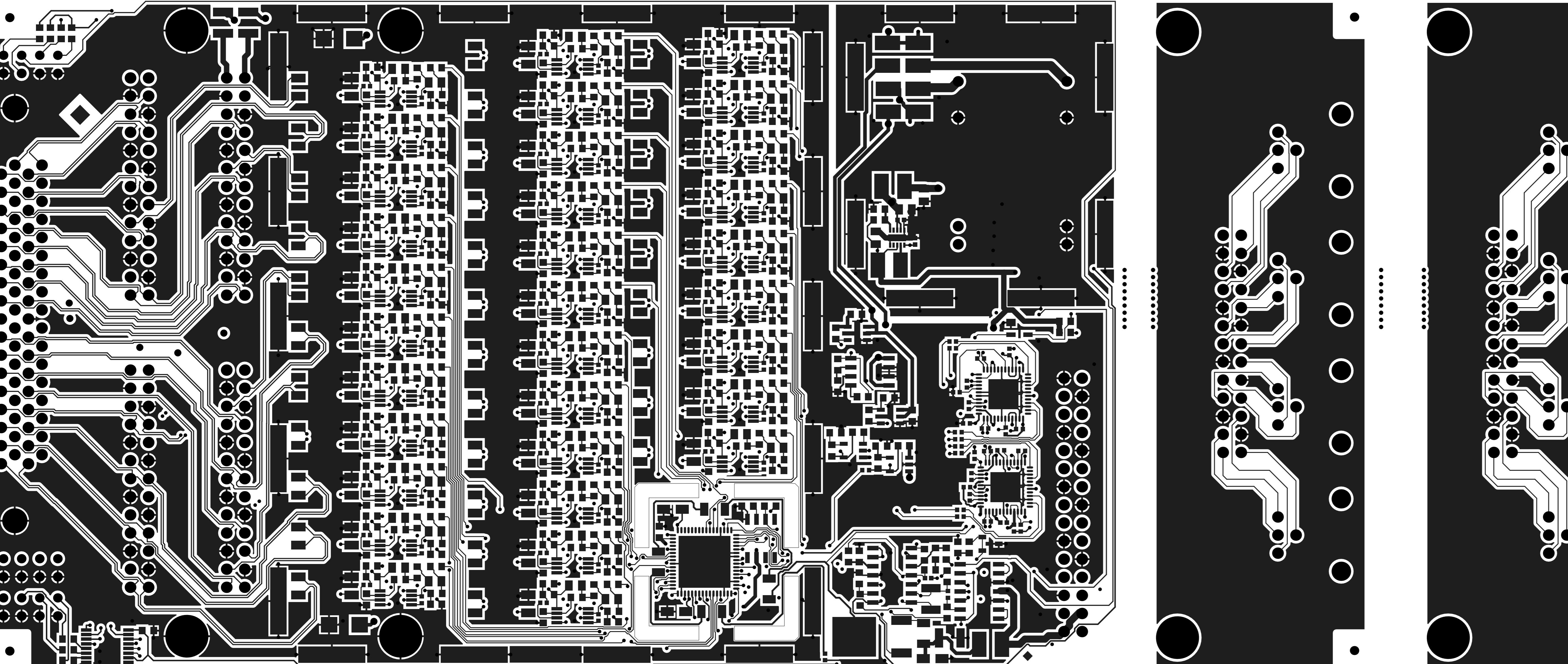
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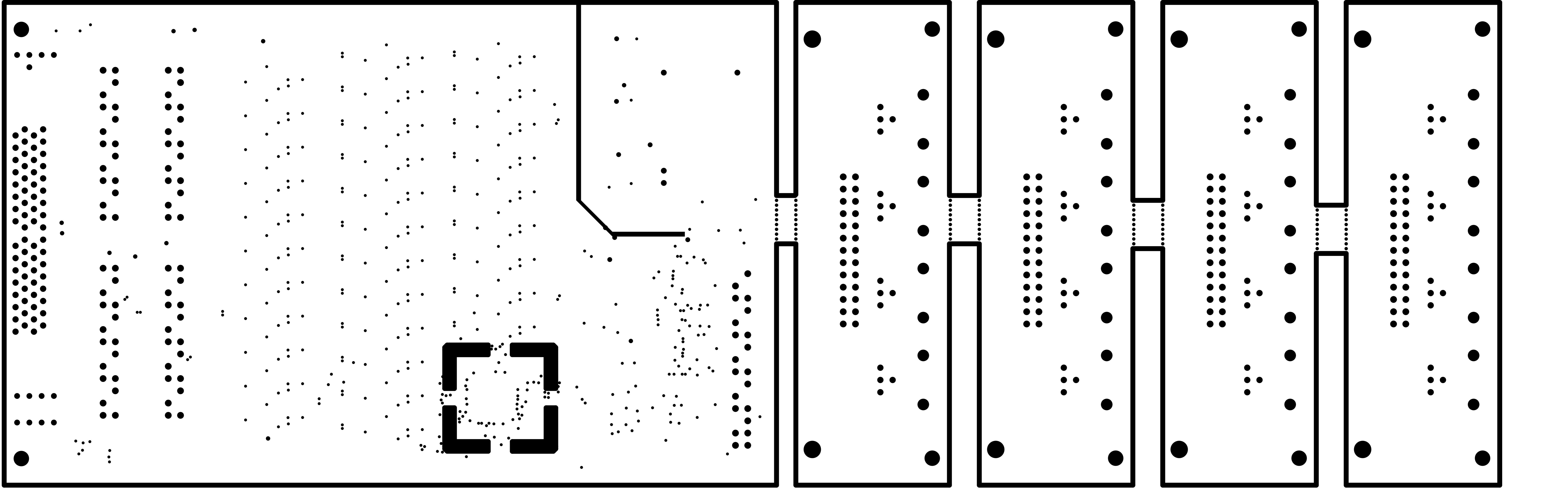


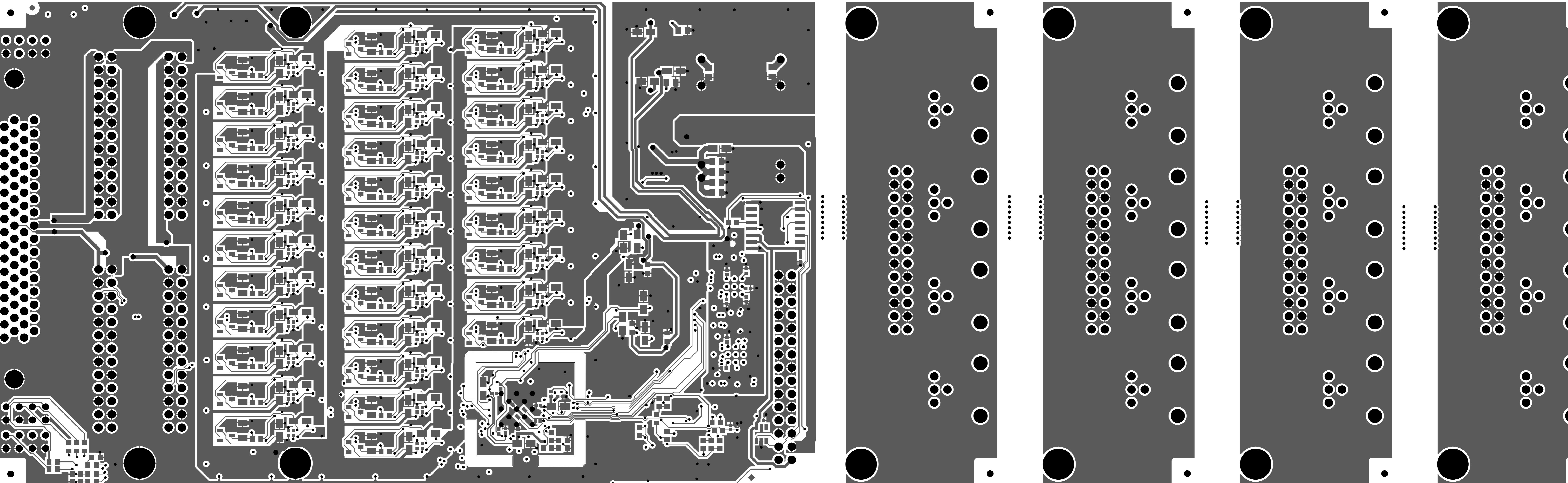






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bCB 3U DYC 1.6V1.0

MUT USE 2012



IC1P

ARLIO

1

IC13

