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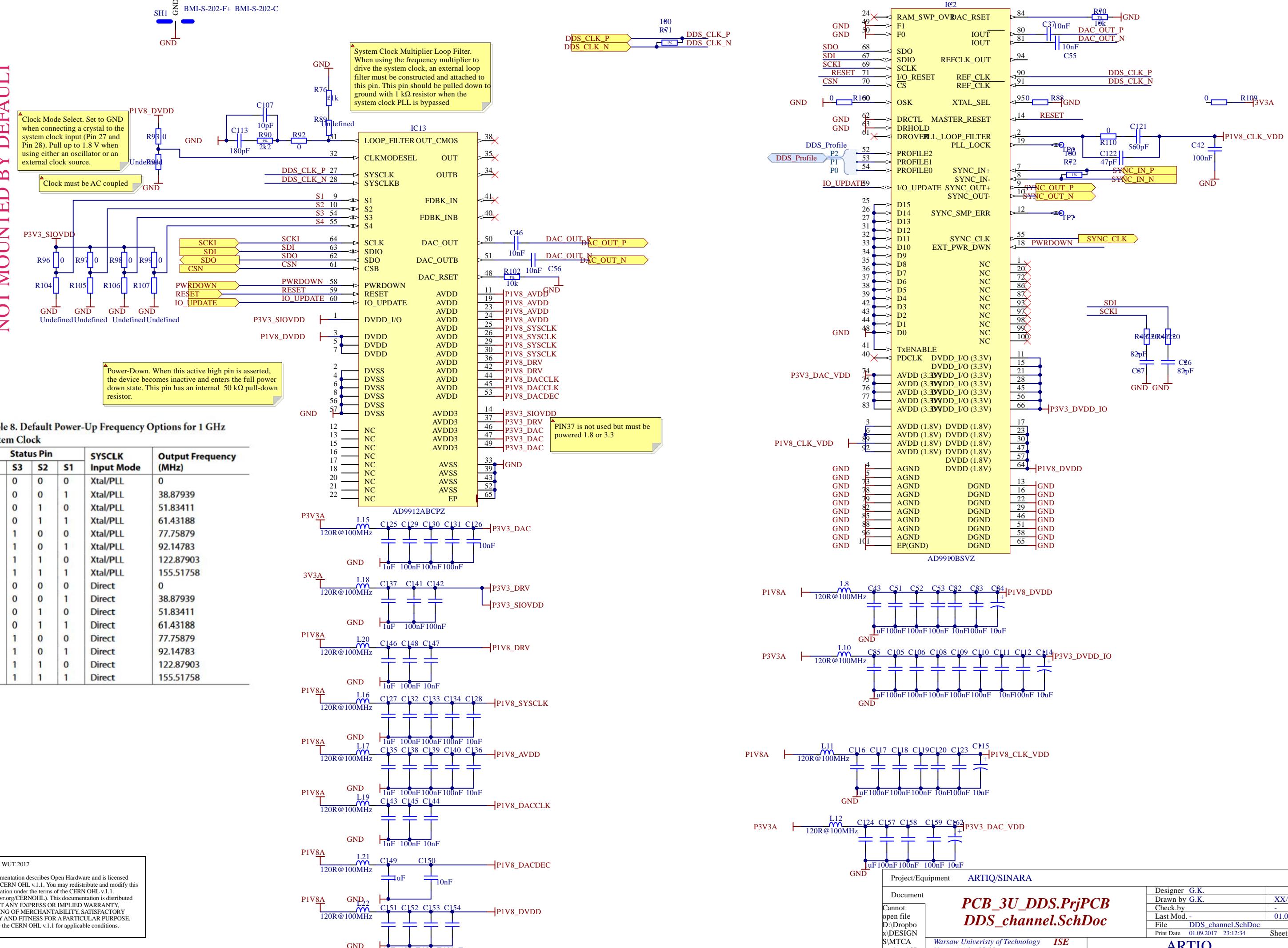


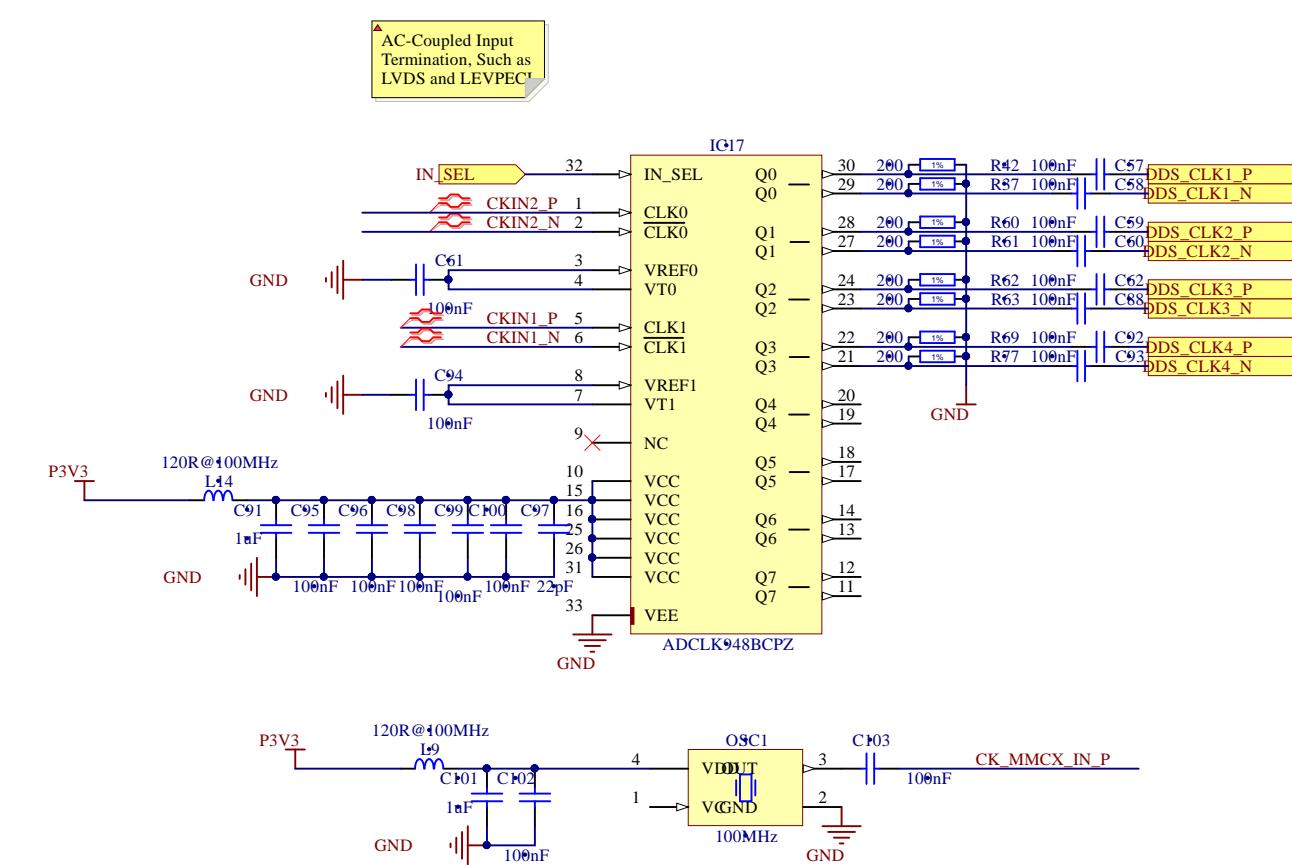
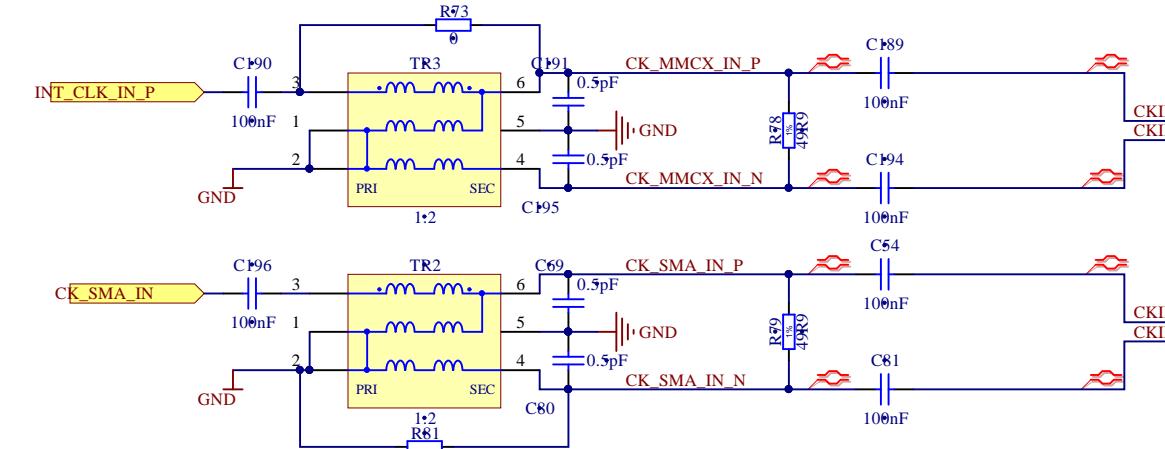
Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin		SYSCLK Input Mode	Output Frequency (MHz)	
S4	S3	S2	S1	
0	0	0	0	Xtal/PLL
0	0	0	1	Xtal/PLL
0	0	1	0	Xtal/PLL
0	0	1	1	Xtal/PLL
0	1	0	0	Xtal/PLL
0	1	0	1	Xtal/PLL
0	1	1	0	Xtal/PLL
0	1	1	1	Xtal/PLL
1	0	0	0	Direct
1	0	0	1	38.87939
1	0	1	0	51.83411
1	0	1	1	61.43188
1	1	0	0	77.75879
1	1	0	1	92.14783
0	1	1	0	122.87903
0	1	1	1	155.51758
1	0	0	0	0
1	0	0	1	38.87939
1	0	1	0	51.83411
1	0	1	1	61.43188
1	1	0	0	77.75879
1	1	0	1	92.14783
1	1	1	0	122.87903
1	1	1	1	155.51758

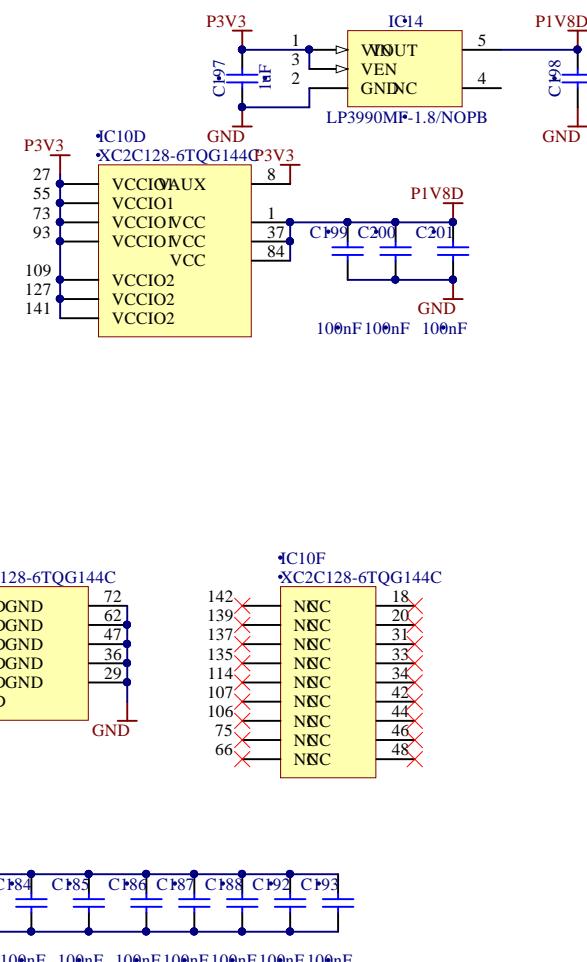
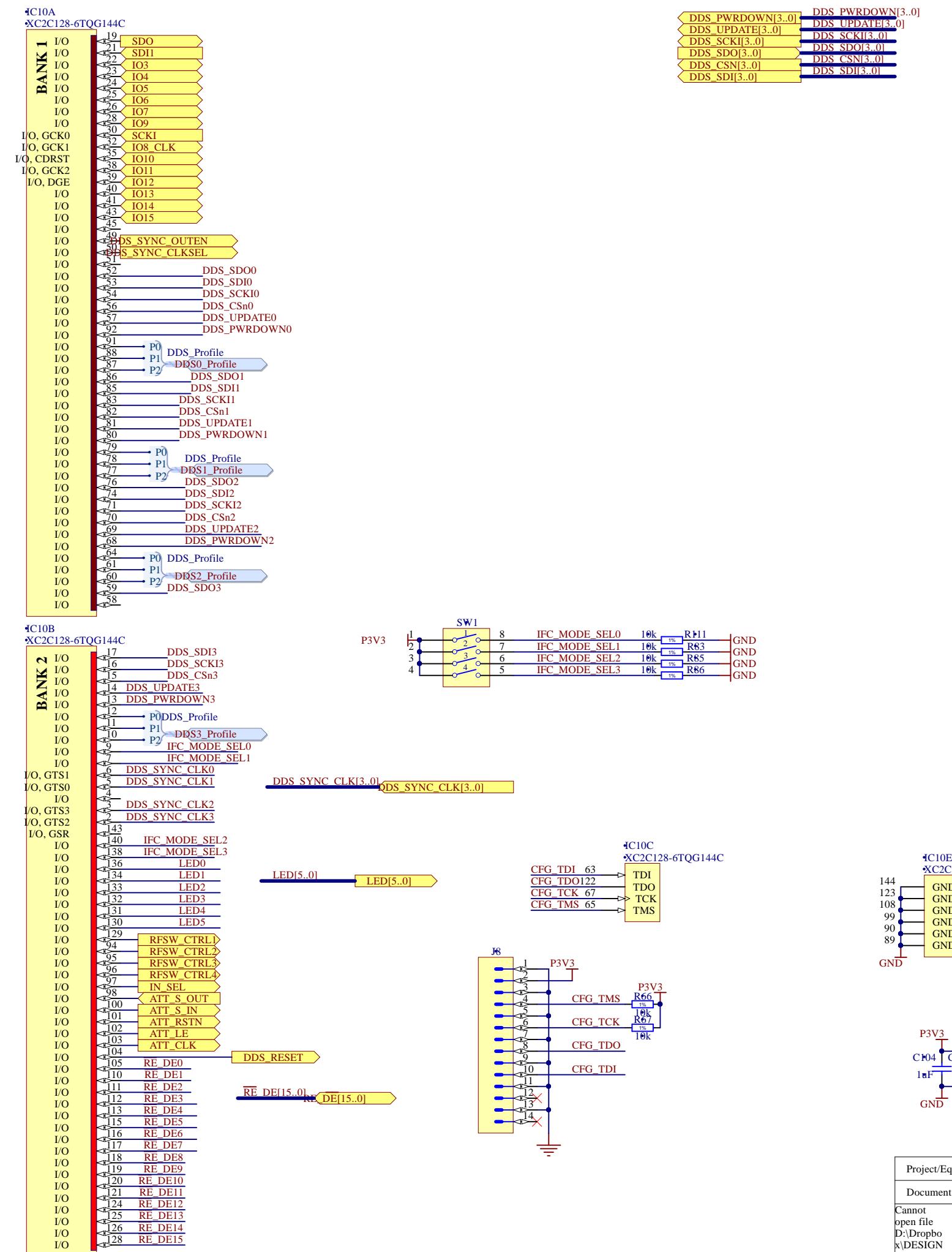
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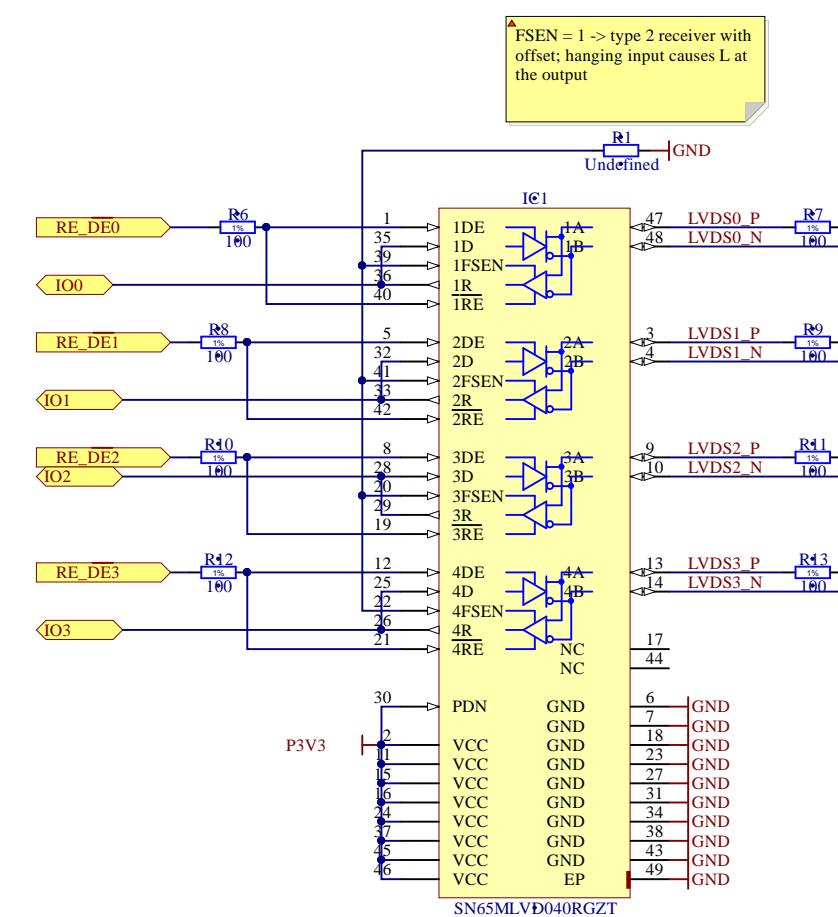
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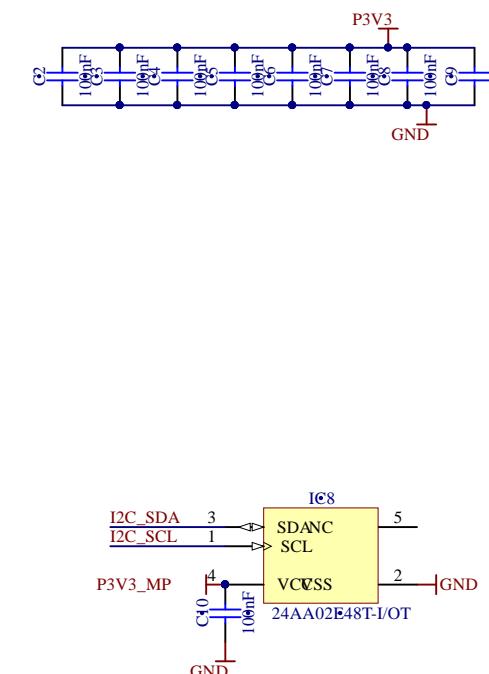
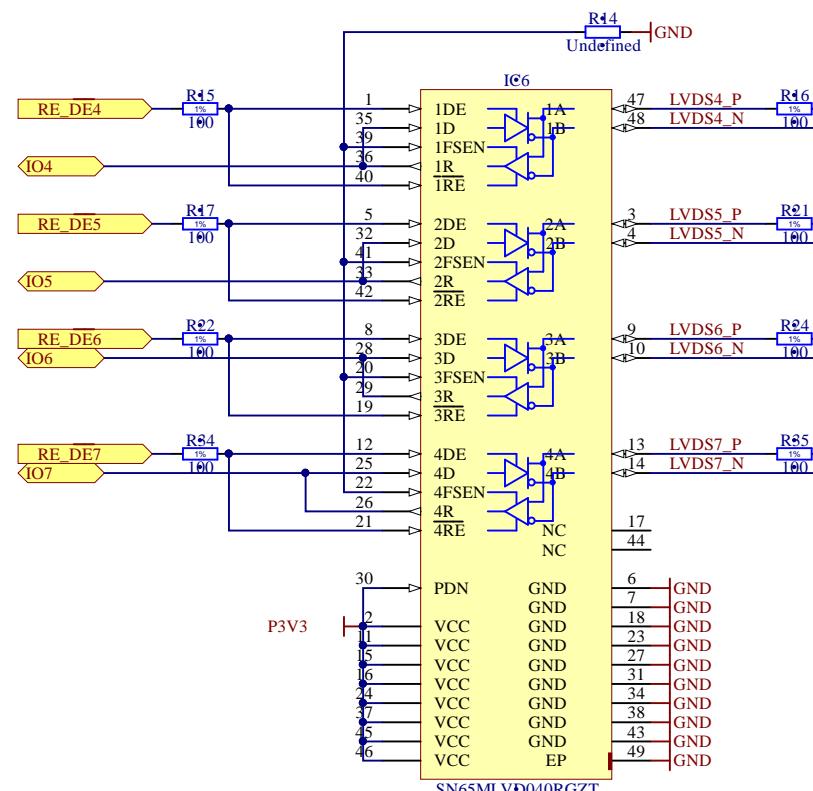
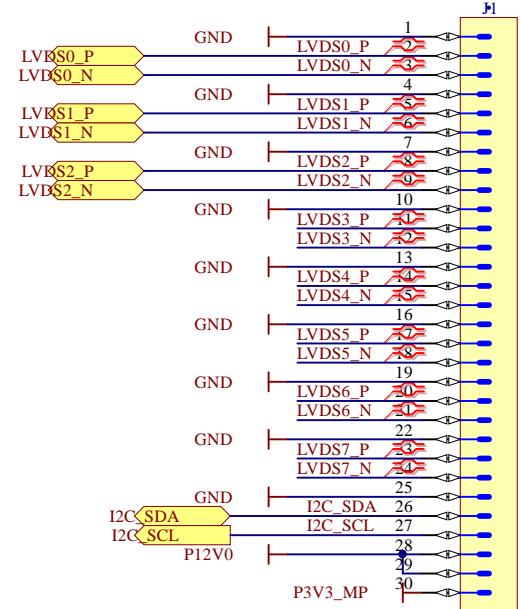
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This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 500mA



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ARTIQ

