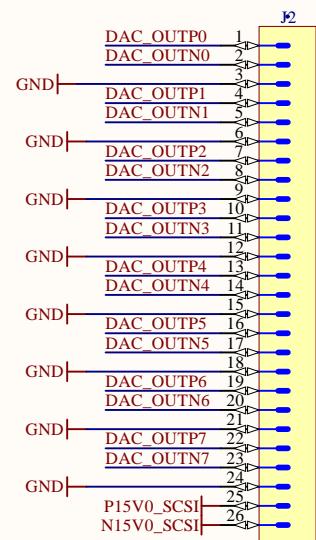
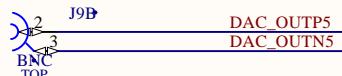
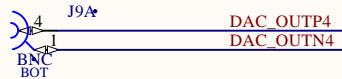


A



Title

Size	Number	Revision
A4		
Date:	23.04.2017	Sheet of
File:	D:\Dropbox\..\IDC2BNC.SchDoc	Drawn By:

A

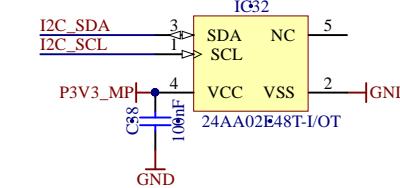
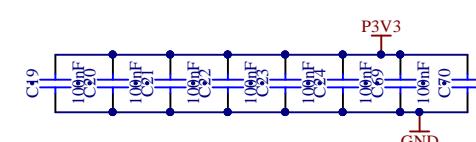
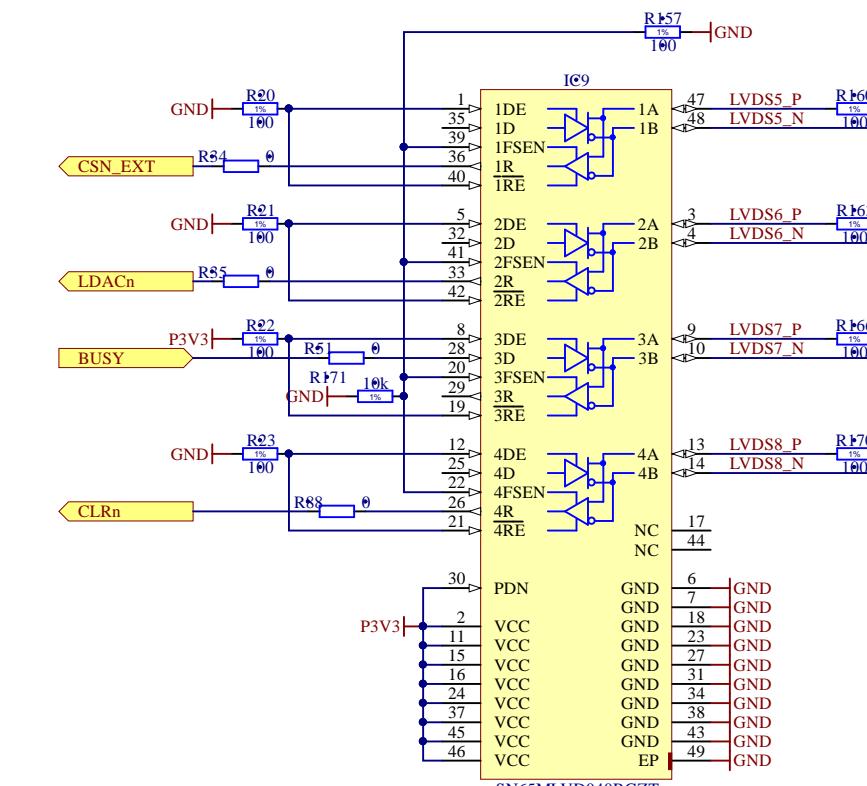
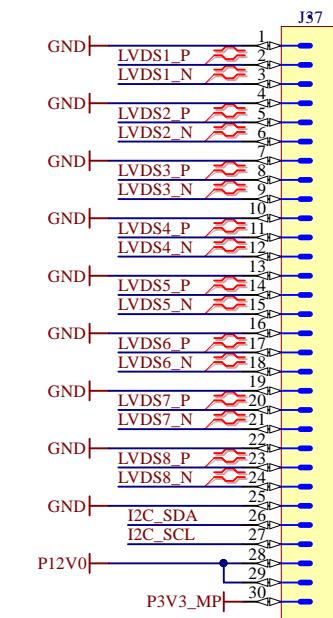
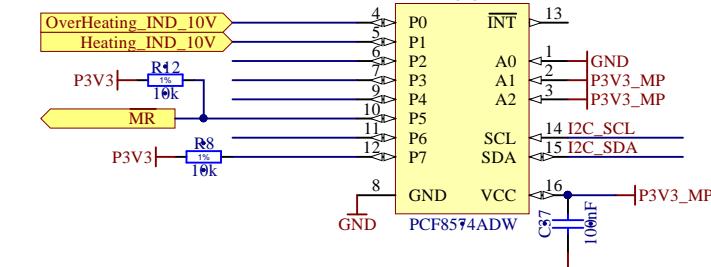
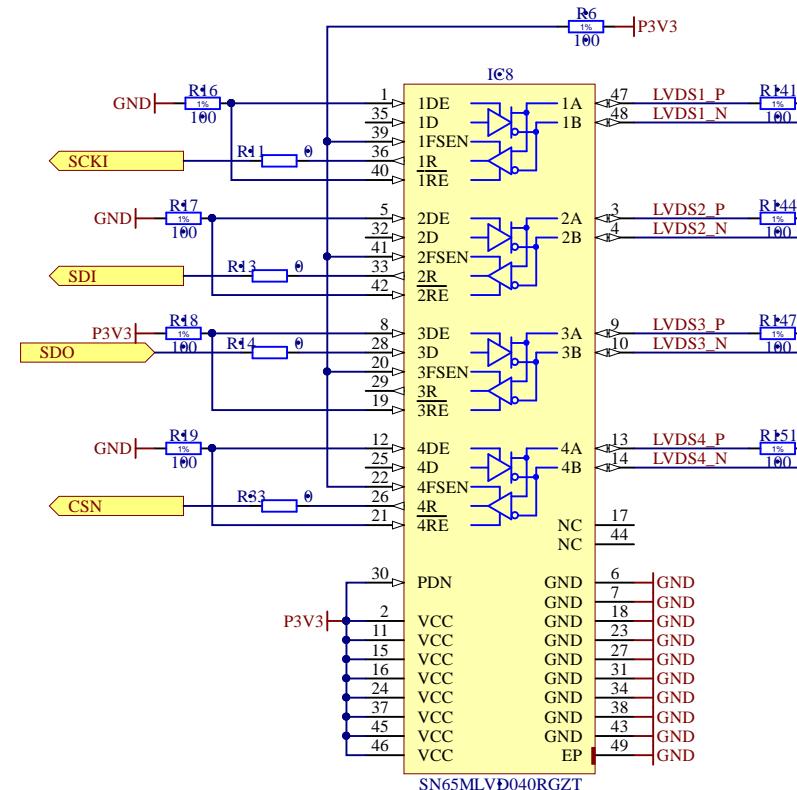
B

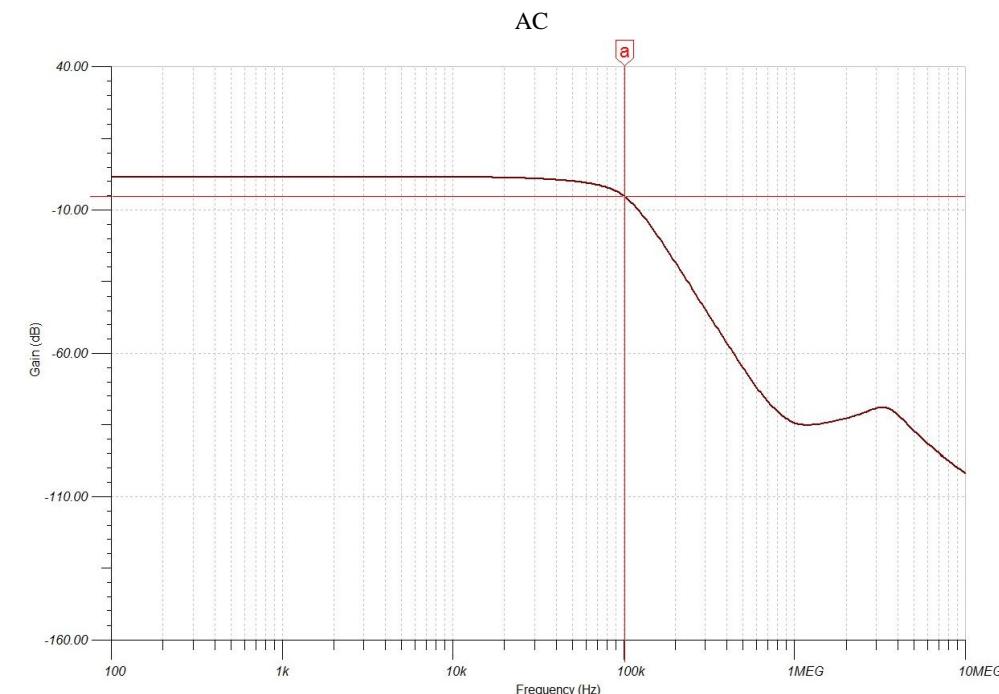
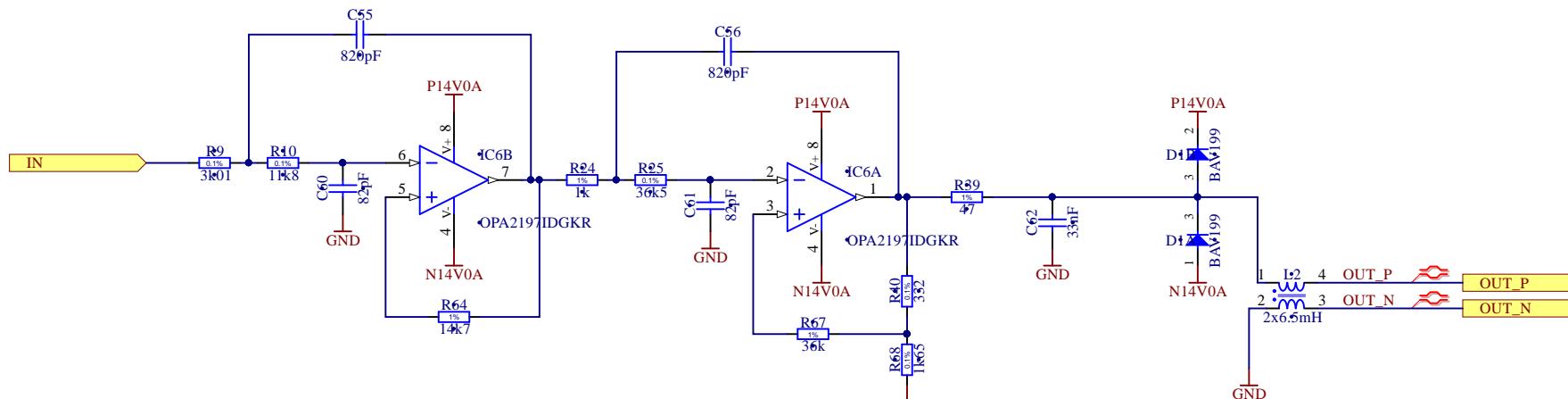
C

D

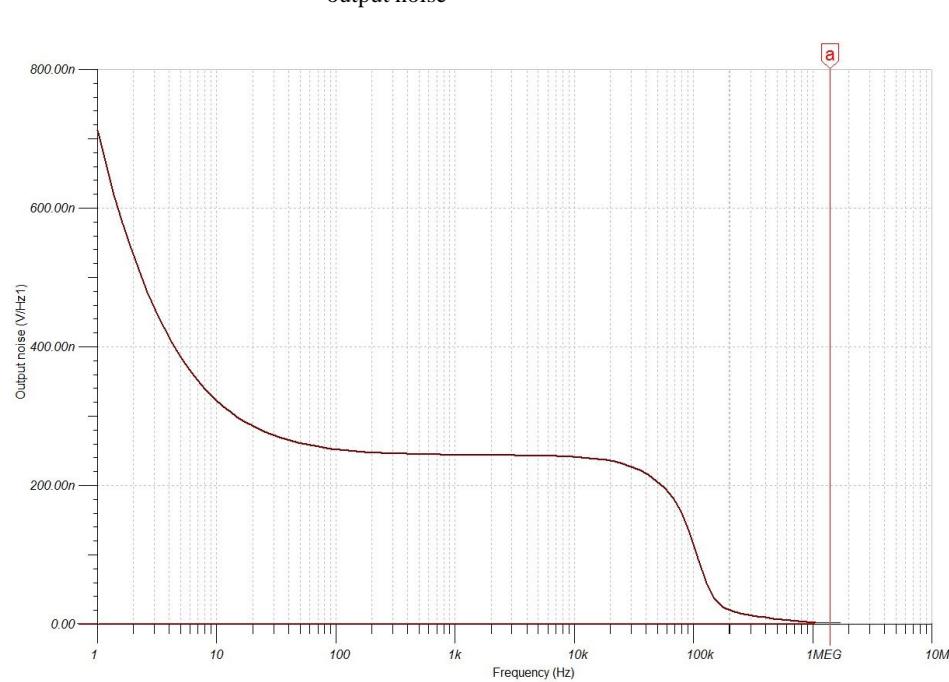
This module connects to Kasli or to VHDCI Mettino breakout board
 All signals are LVDS, in case of Mettino VCC is 1.8V
 I2C is 3.3V LVCMOS
 P3V3_MP can handle up to 20mA
 P12V0 current is up to 500mA

please make a list of IC names and functions in corner of schematic for easier reading

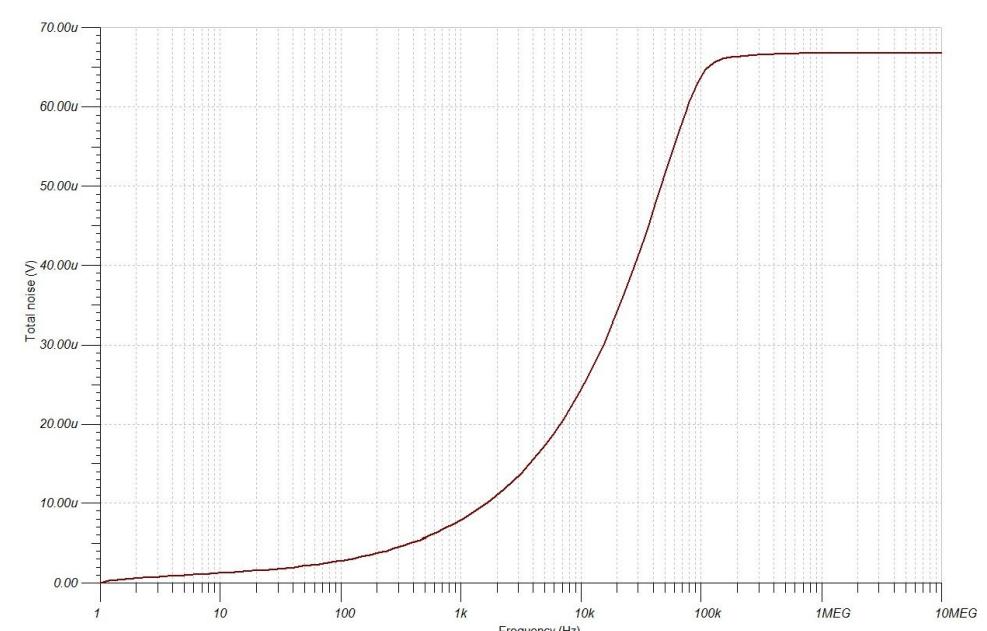




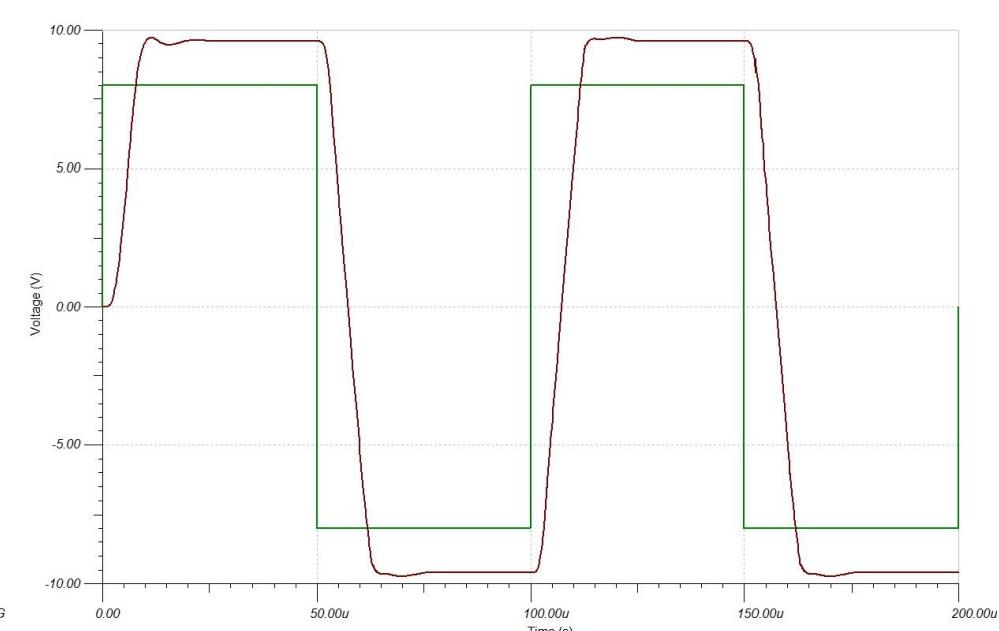
output noise



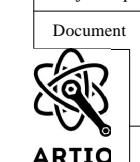
total noise



transient



Project/Equipment 3U ADC



Input chnnnel DPGA

Designer G.K.	Drawn by G.K.	XX/XX/XXXX
Check by -	-	
Last Mod. -	23.04.2017	
File Output_channel.SchDoc	Print Date 23.04.2017 12:55:57	Sheet of
		A3 -

Channel count: 32 channels from a single 32 channel DAC
 update rate: 10 channels simultaneously at >100kSPS (assume SPI running at 50MHz)
 Outputs: +12V
 Resolution: 16 bits
 Bandwidth:
 differential: Butterworth response with 100kHz cut-off
 common-mode: suitable chokes and common-mode filter to keep worst-case channel-channel cross-talk <-60dB when driving 1MHz sine into a high-impedance load using a 5m cable.
 Recommendation should also be made for common-mode/differential mode Rx filter as part of this design (will be required for testing).
 Output drive: the outputs should be able to drive 5m of SCSI cable with a 100kHz full-scale sinusoid without significant degradation of bandwidth, SFDR etc.
 Low-frequency noise: 0.1Hz - 1kHz noise < 10ppm RMS
 Integrated noise - 10Hz to 20MHz integrated noise < 30ppm RMS.
 Noise density - <1nVrtHz for all frequencies >=1MHz (includes both white noise and output spurs due to SMPSs, DAC clocks, etc.)
 Drift: <10ppm over 24 hours in a +/-1K "lab" environment
 Connectors:
 1xHD68 (SCSI III) connector on front panel. 32 twisted pairs used for the DACs (1 conductor of each pair is GND), 2 pairs used for +15V, GND.
 4 10x2 header on the PCB, each providing 8 DAC channels, +15V. (If room, also add unregulated +12V to this header).

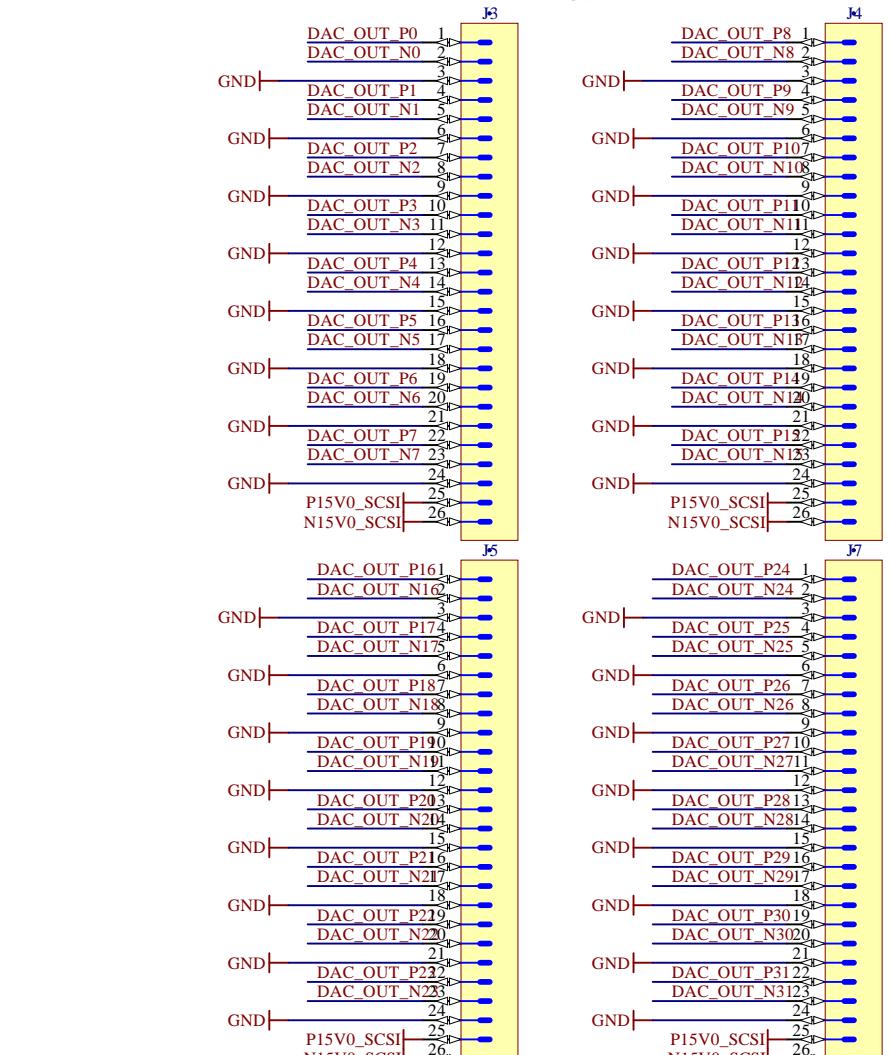
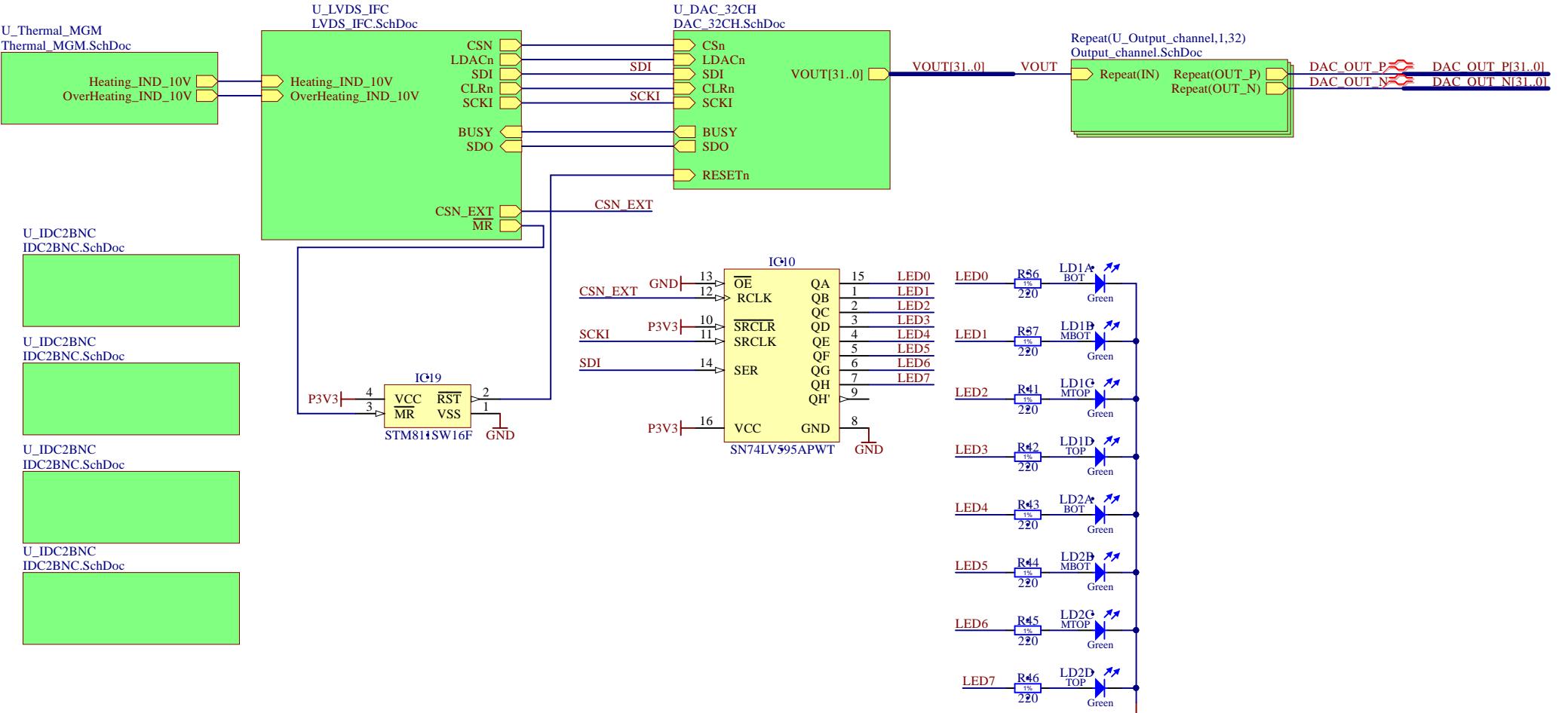
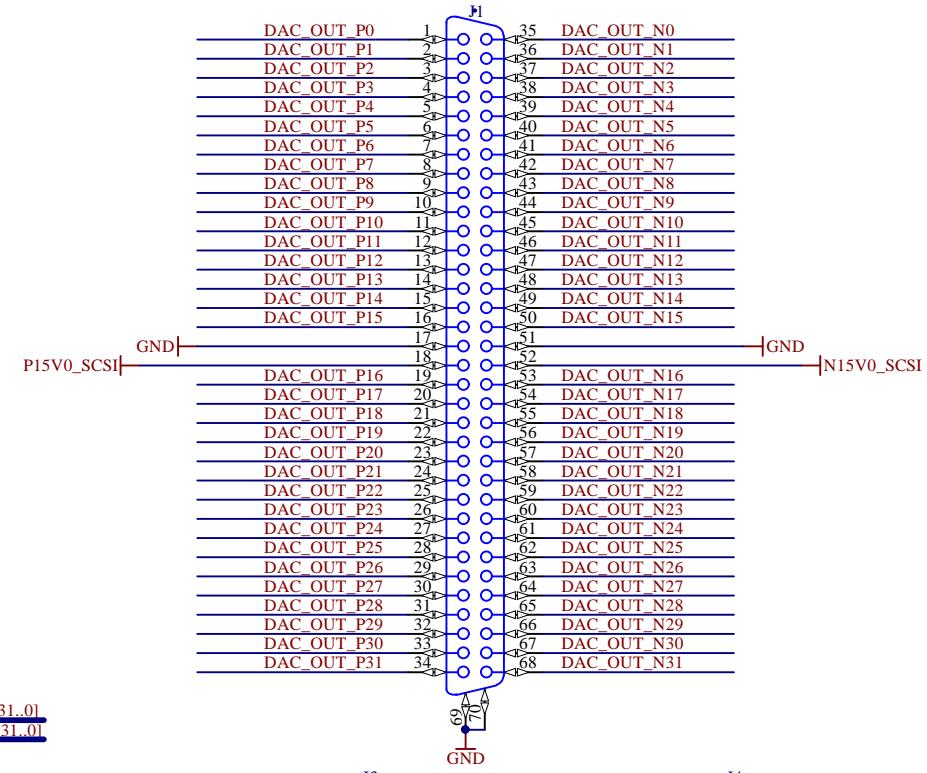
We additionally design a 3U passive (straight through) BNC breakout board. Up to 4 of these can be connected to the headers to break the DAC channels out onto BNCs for low-density applications. It is anticipated that the HD68 will be DNP when these boards are used.

DIO: "Standard" Kasli extension board connections (I2C, 8xLVDS, power, etc) either from pin header or backplane. Will require switching/jumpers to select BP & header. 5xLVDS lines used for DAC SPI bus: CLK, MOSI, MISO, SYNC, LDAC

Thermal: ideally, this board should be designed to operate (and meet drift specification) without forced air cooling (e.g. suitable heat-sinks and choice of lowish power OpAmps). If not possible, add suitable fans/etc.

Screening: as required to ensure noise specifications are met in a realistic EMI environment (e.g. adjacent Kasli etc).

Misc: EEPROM etc per Kasli extension standard



Copyright WUT 2017

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Project/Equipment		3U ADC	Designer	G.K.
Document			Drawn by	G.K.
			Check by	-
Last Mod.	-		Last Mod.	-
File	PCB_3U_DAC.schdoc		Print Date	23.04.2017 12:55:57
				Sheet of
				A3 Rev -
Warsaw University of Technology	ISE			
Nowowiejska 15/19				
ARTIQ				

3U ADC - top 8 channel ADC

A

A

B

B

C

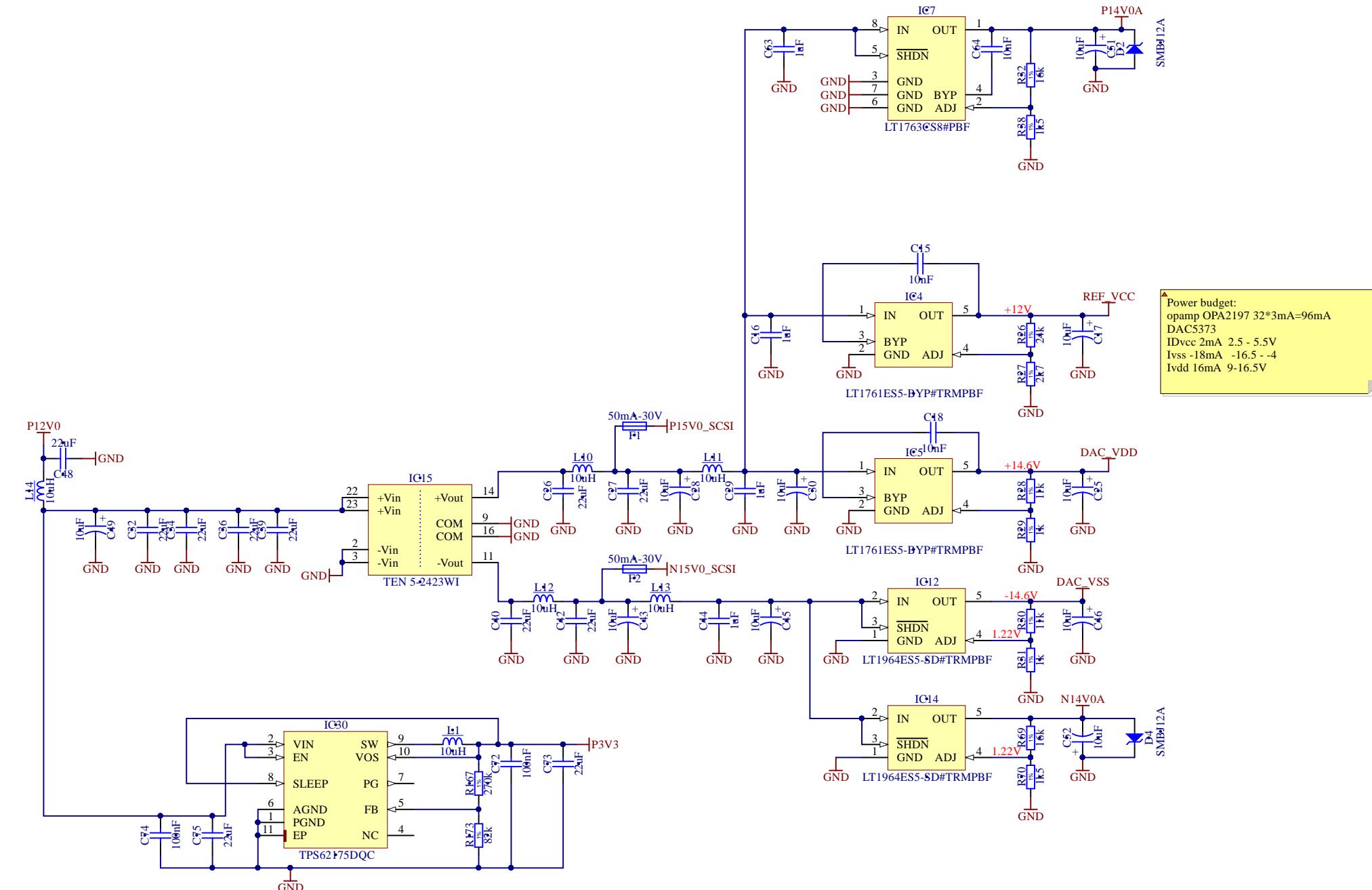
C

D

D

E

E



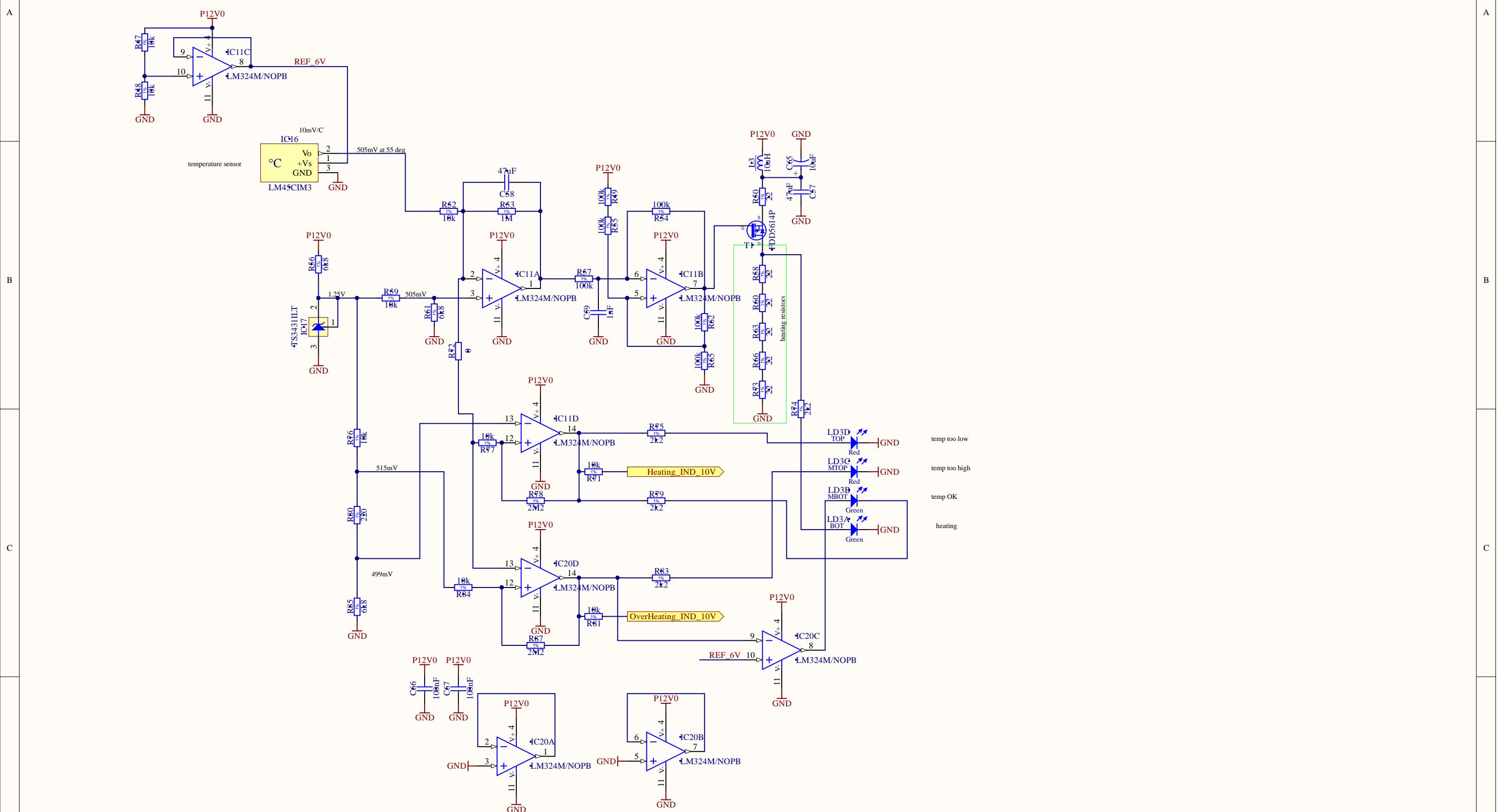
Project/Equipment 3U ADC

Document



Power Supply converters + LDOs

Designer G.K.	Drawn by G.K.	XX/XX/XXXX
Check by	-	
Last Mod.	-	23.04.2017
File Supply.SchDoc	Print Date	23.04.2017 12:55:58
		Sheet of
		A3 Rev -

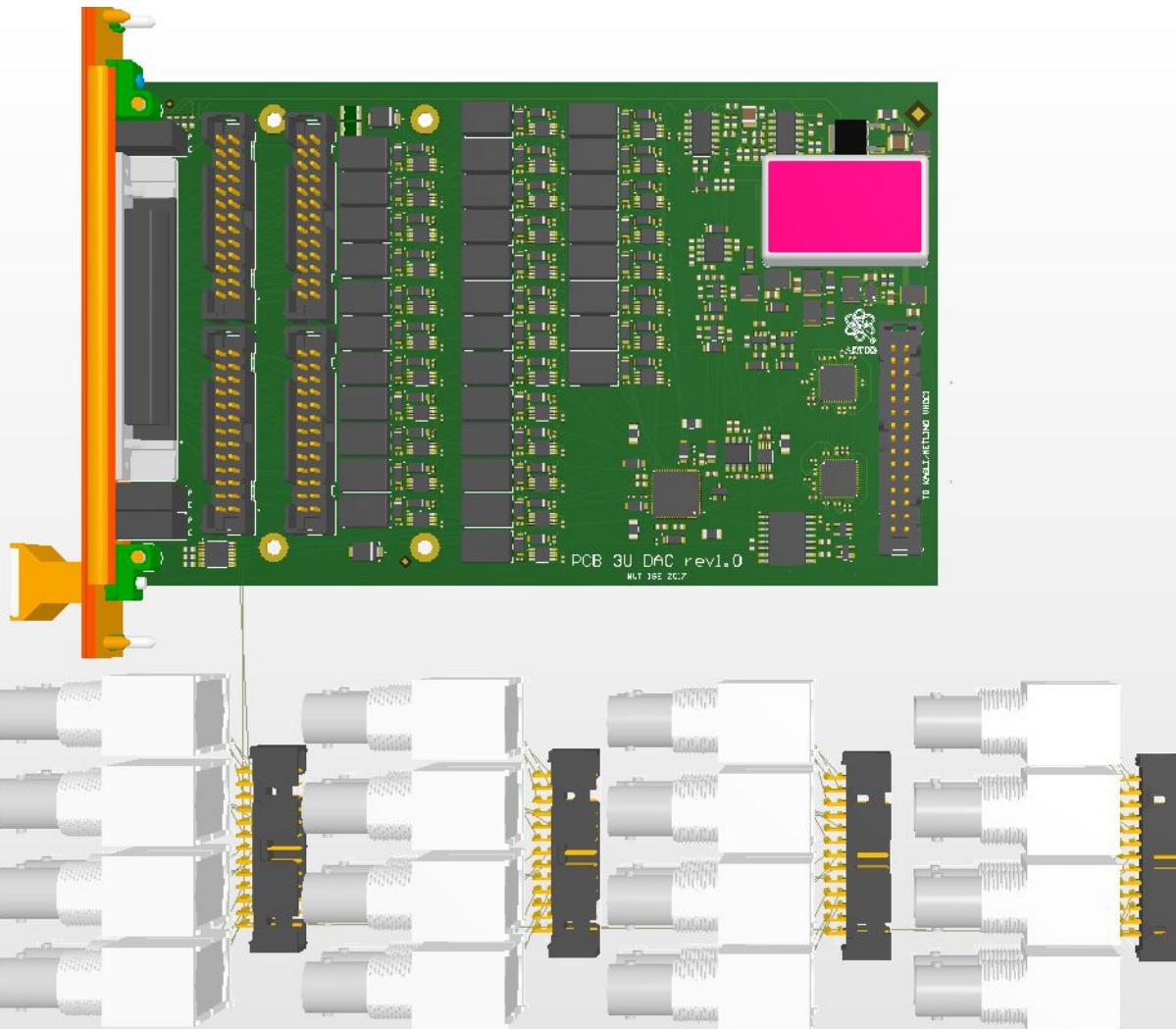


Title

Size Number Revision

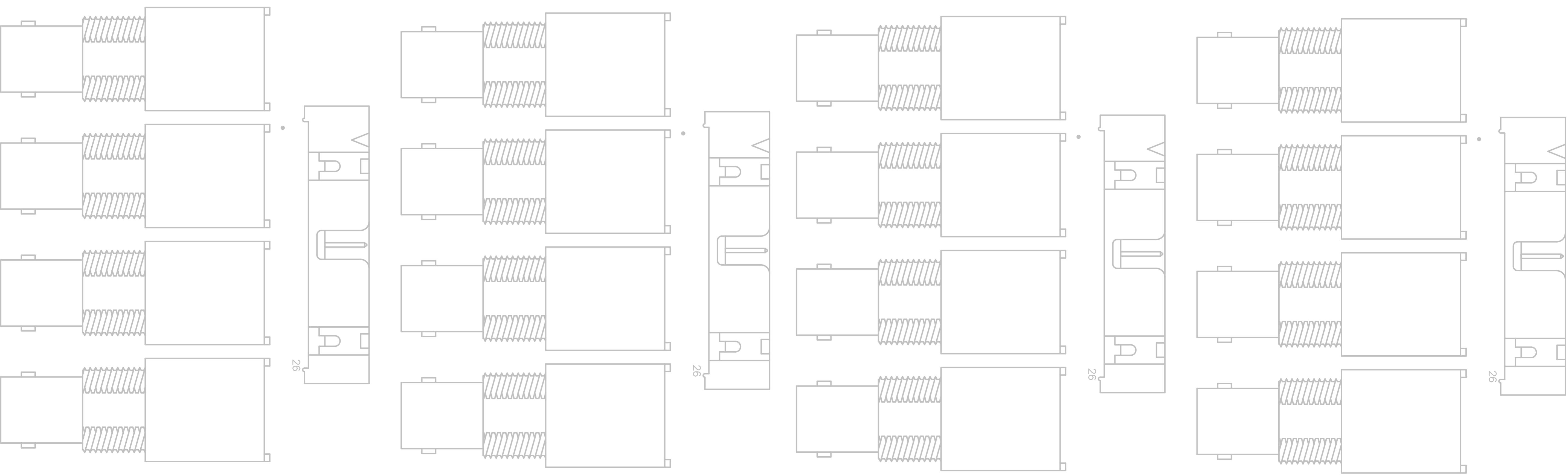
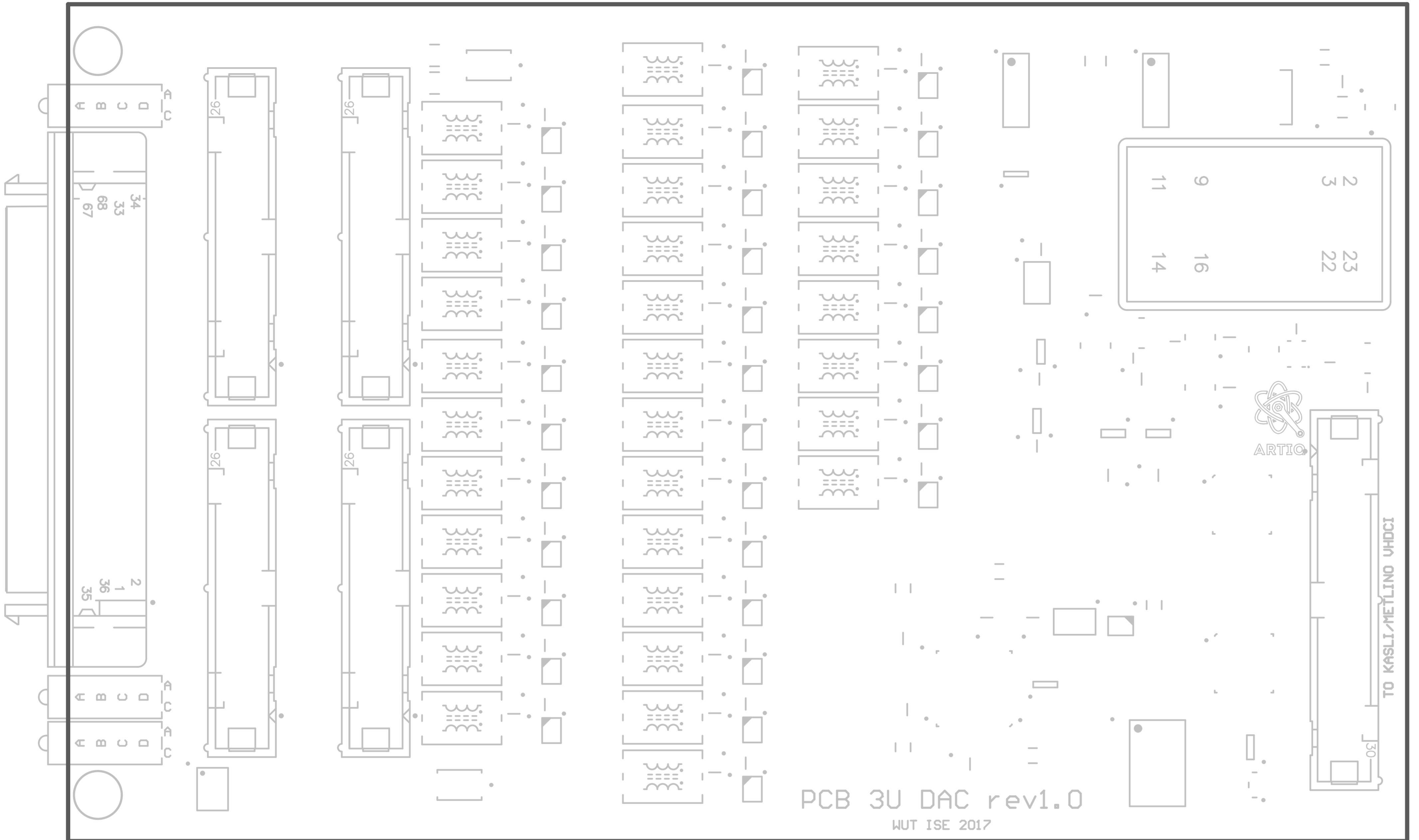
Date: 23.04.2017 Sheet of

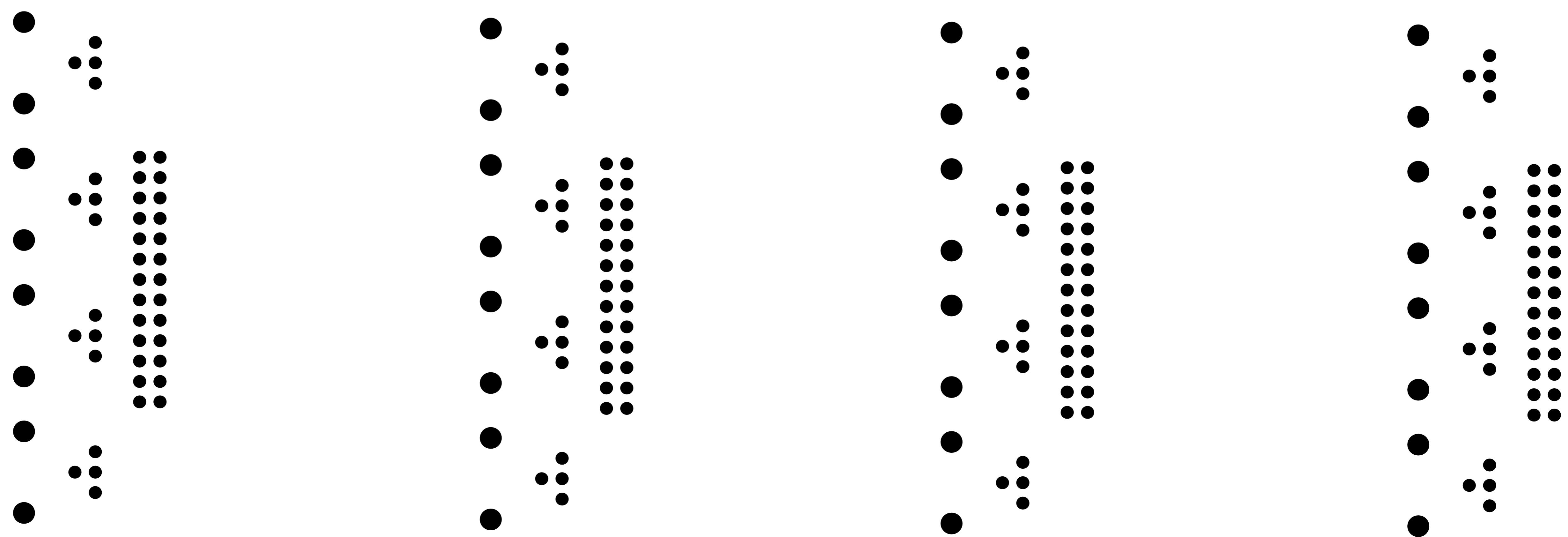
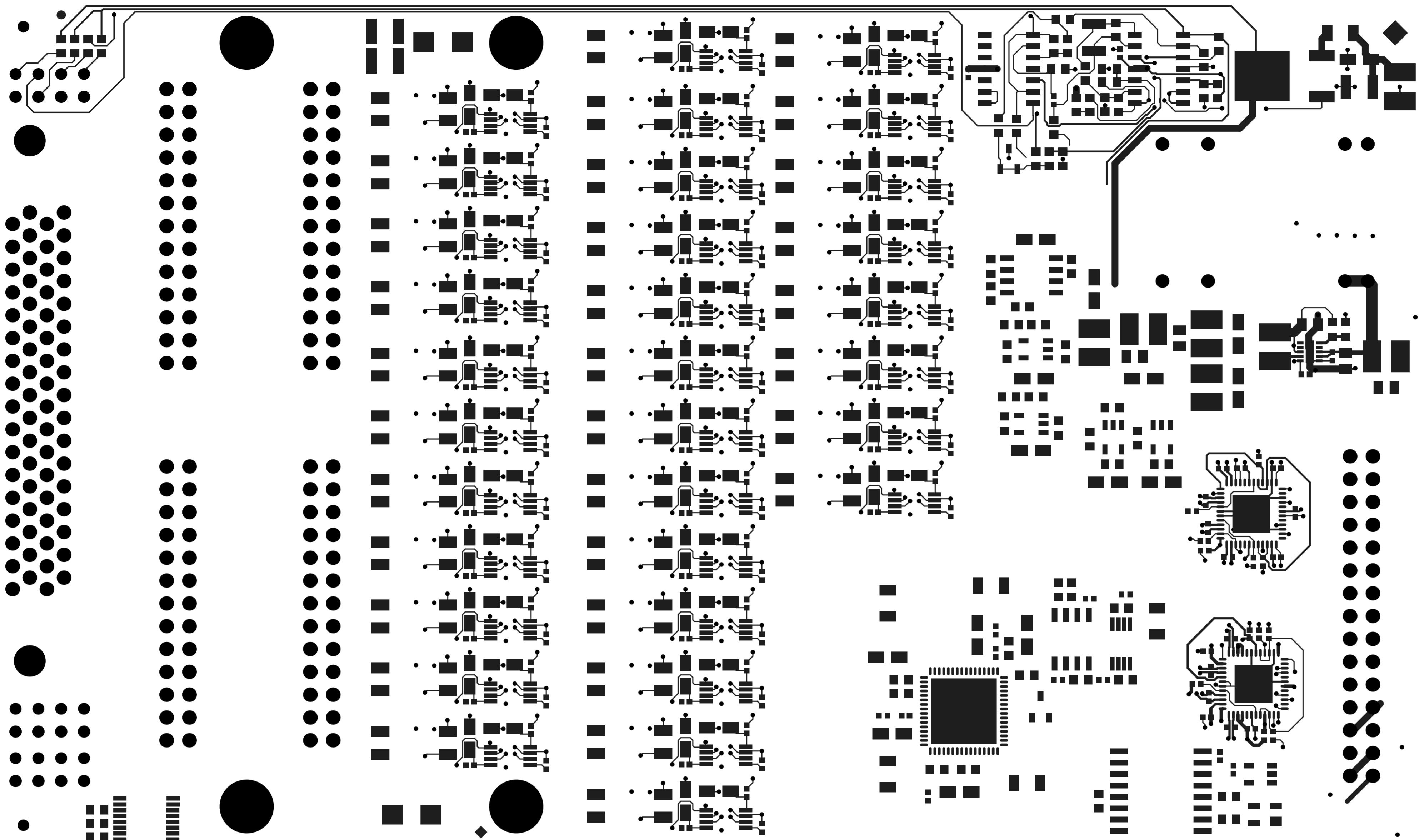
File: D:\Dropbox\Thermal_MGM.SchDoc Drawn By:

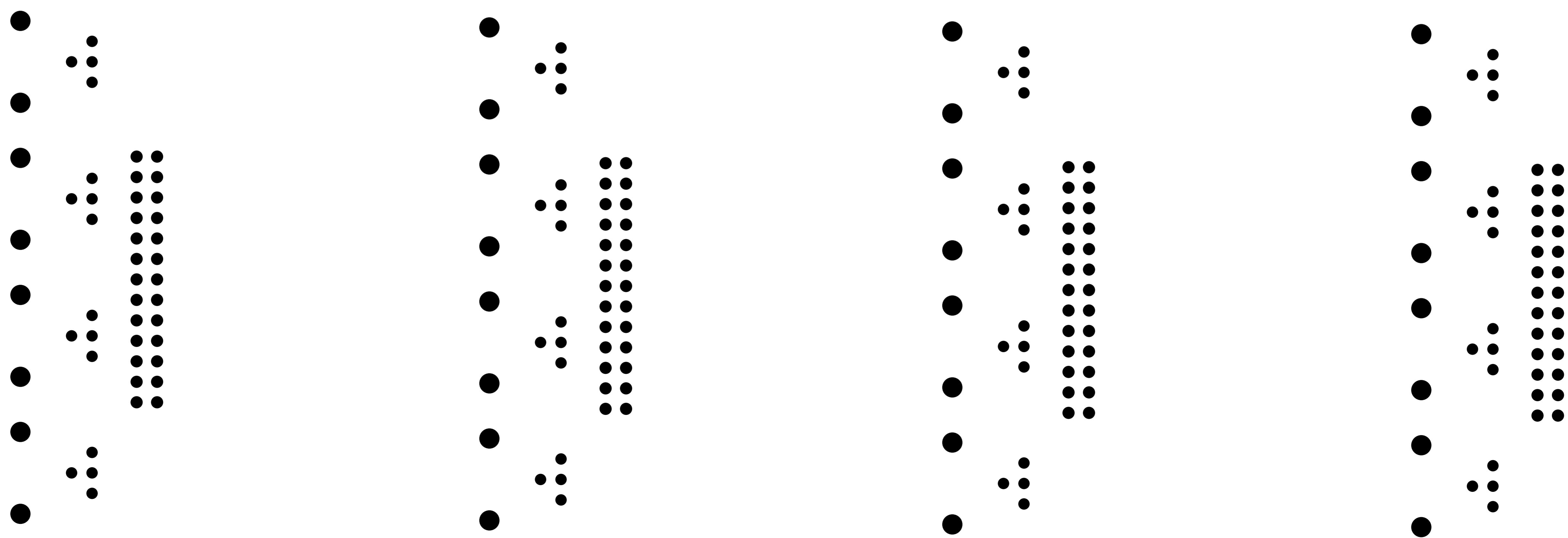
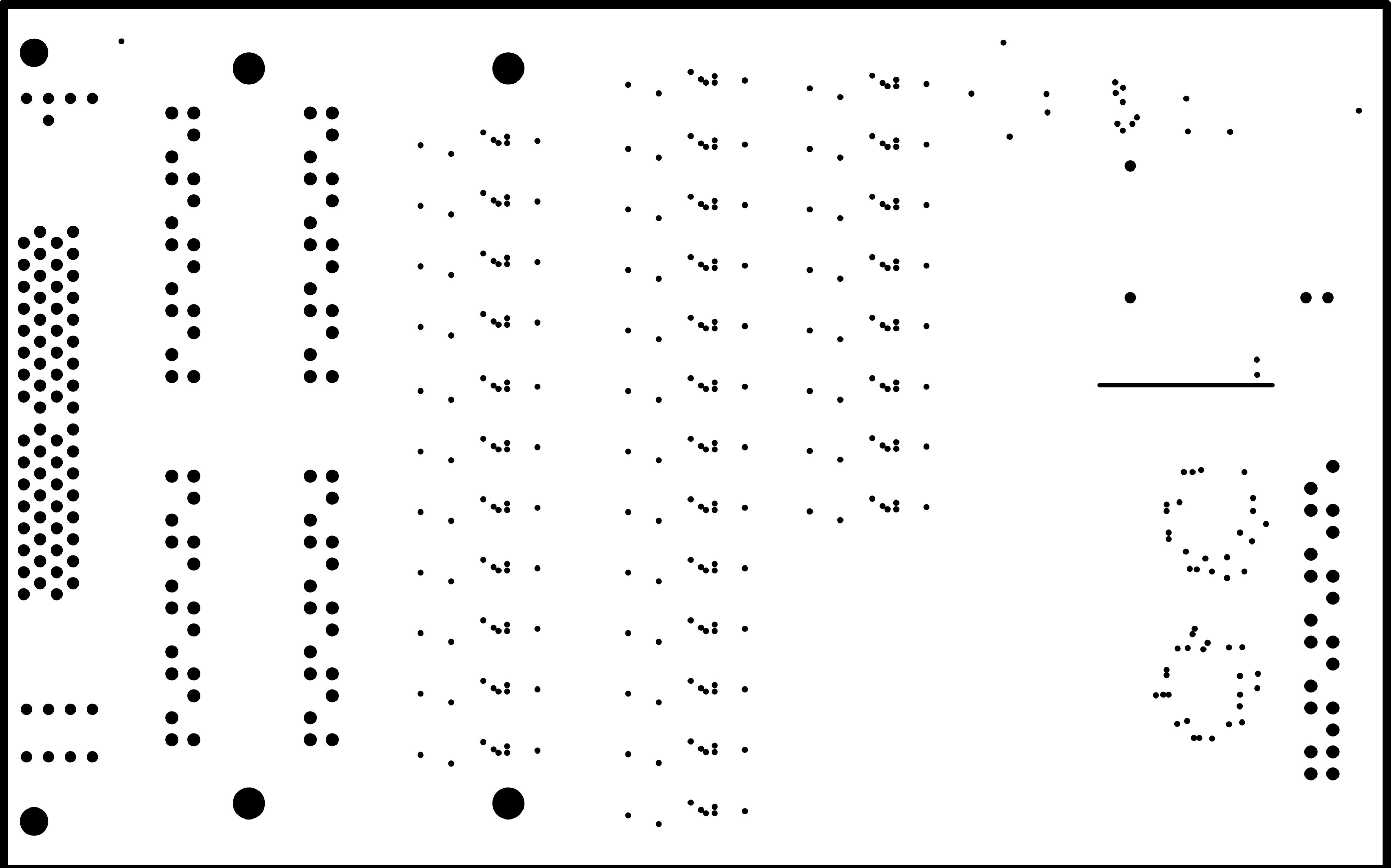


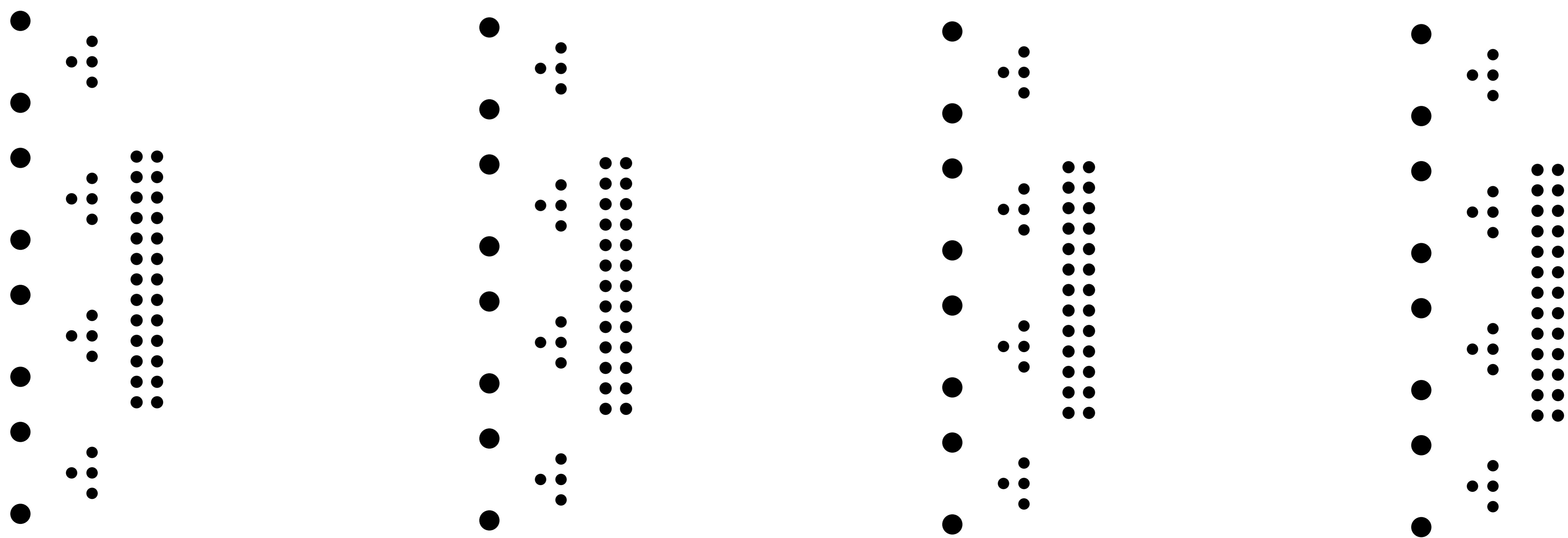
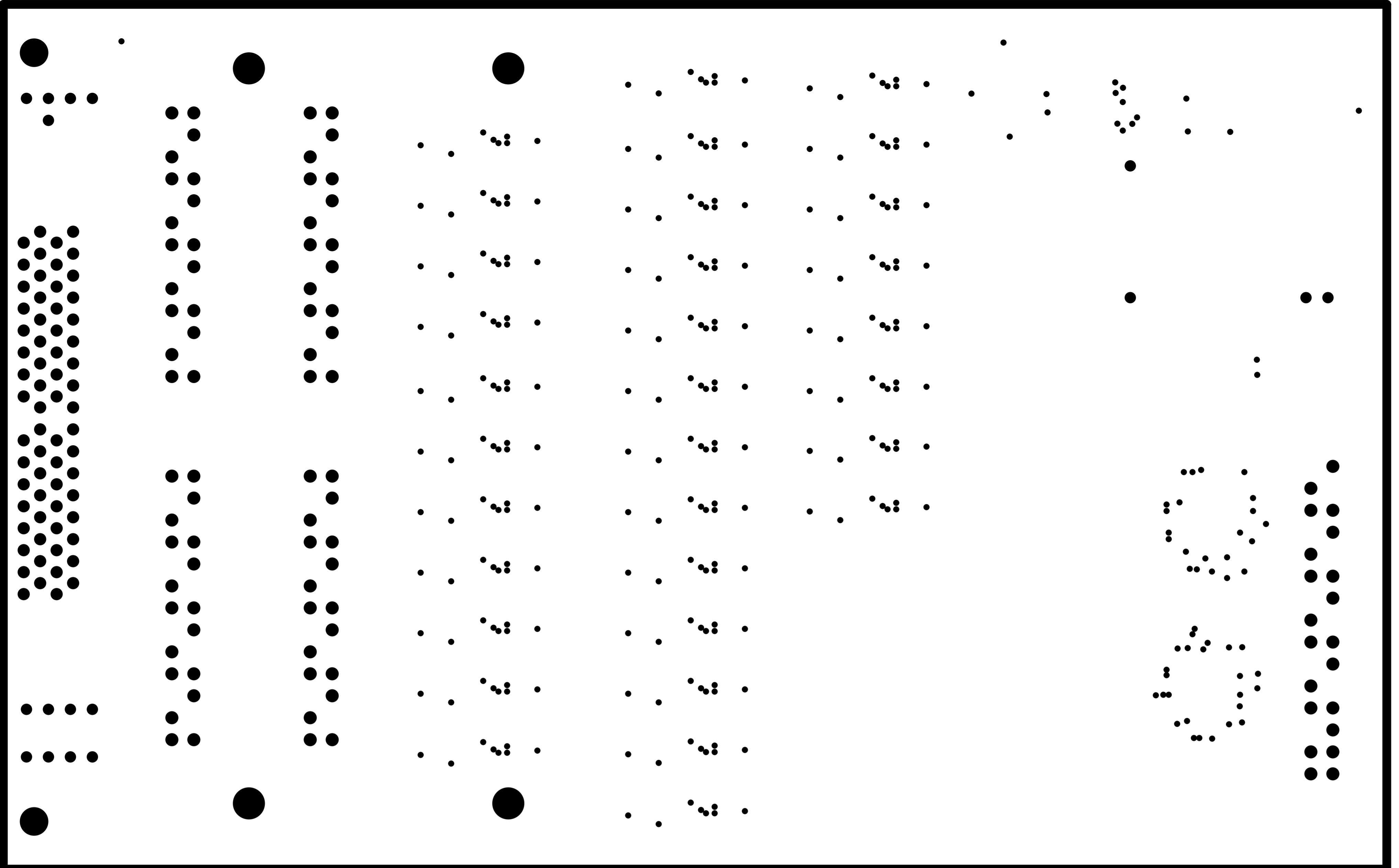
PCB 3U DAC rev1.0

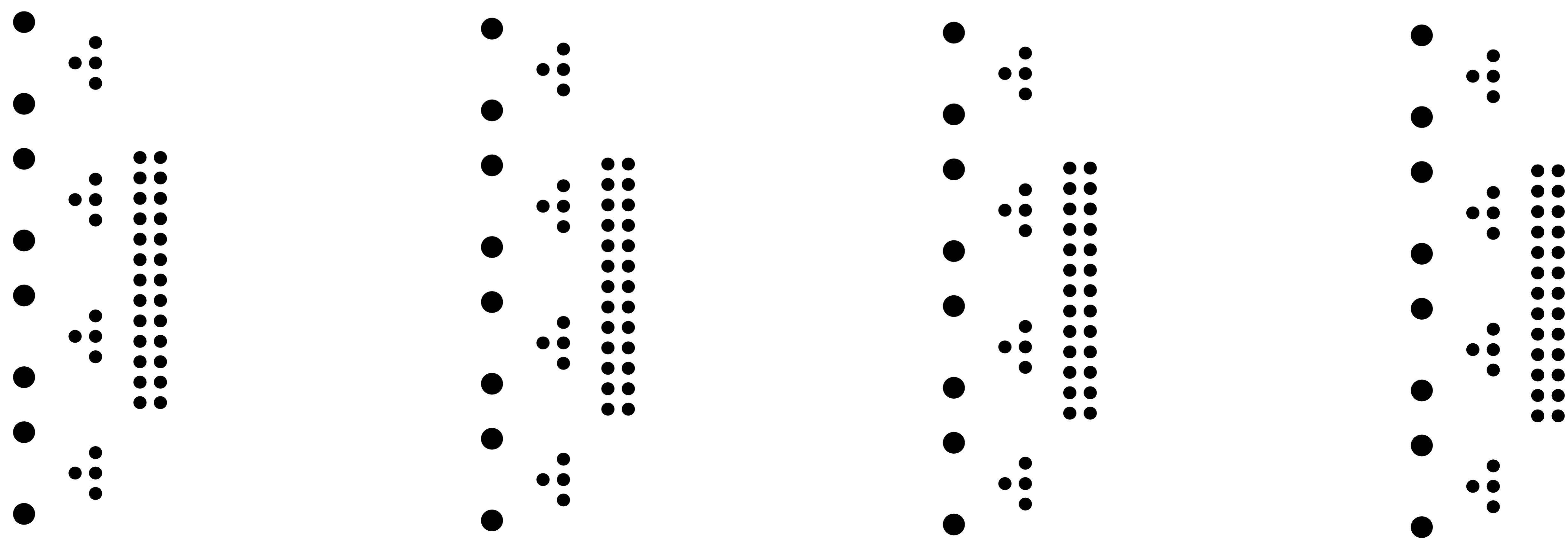
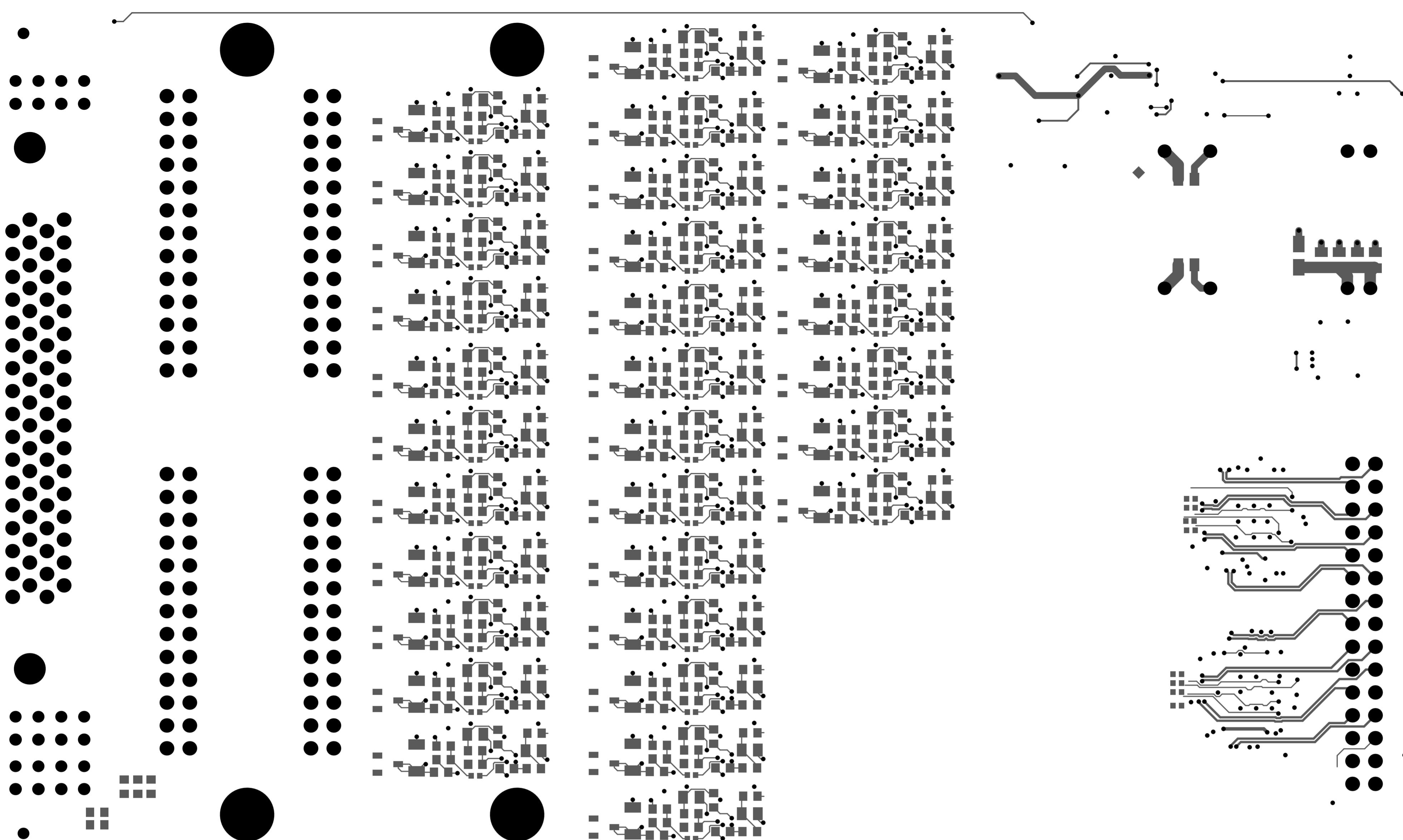
WUT ISE 2017













ATLAS

PCB 3U DAC Rev1.0

Mult ISE 2012