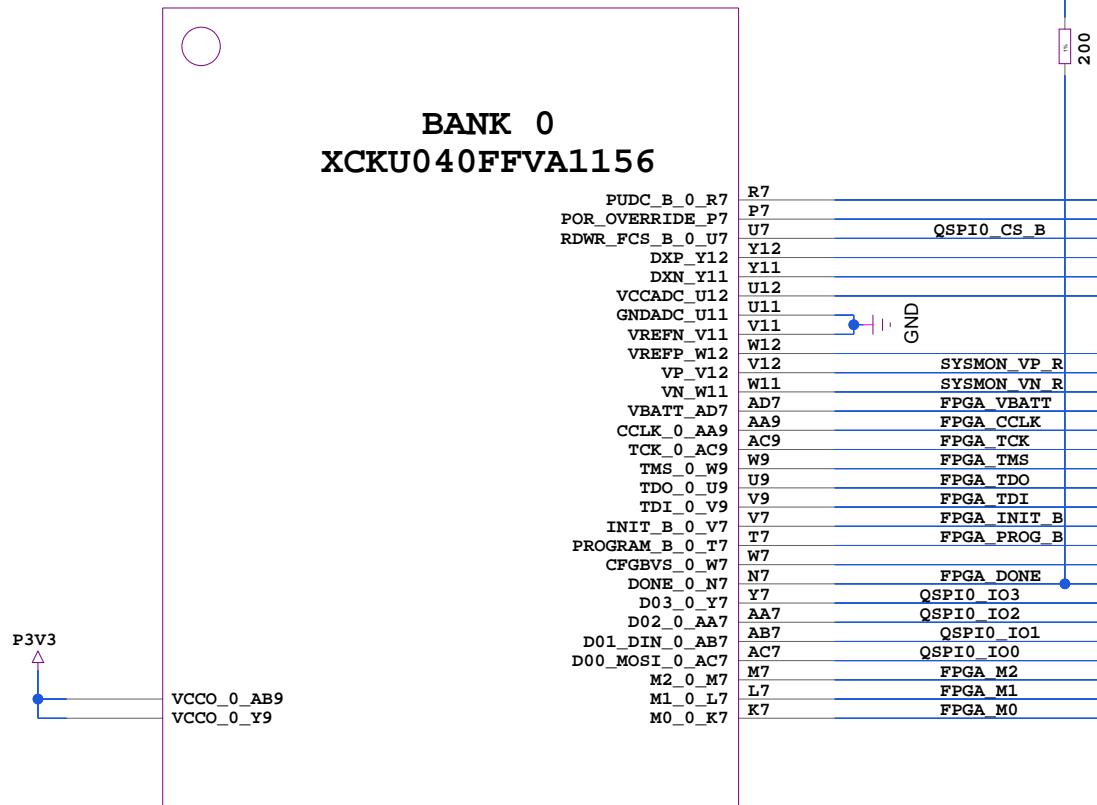


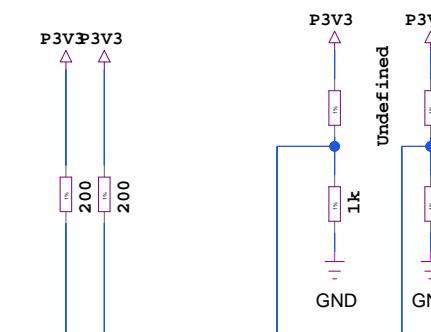
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SOC_KU040_FFVA1156_REV0



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SOC_IRONWOOD_FF1156



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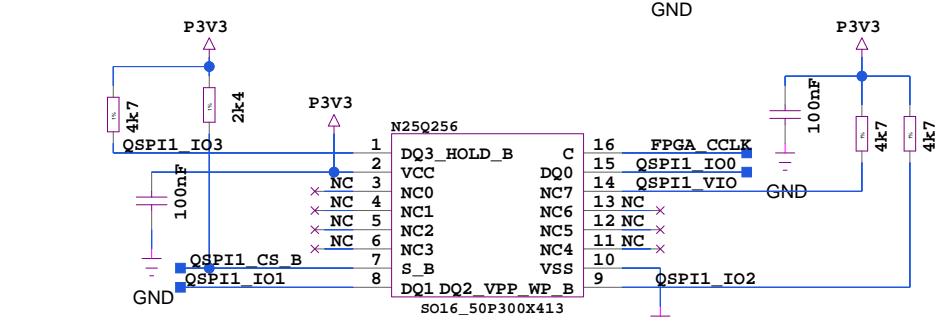
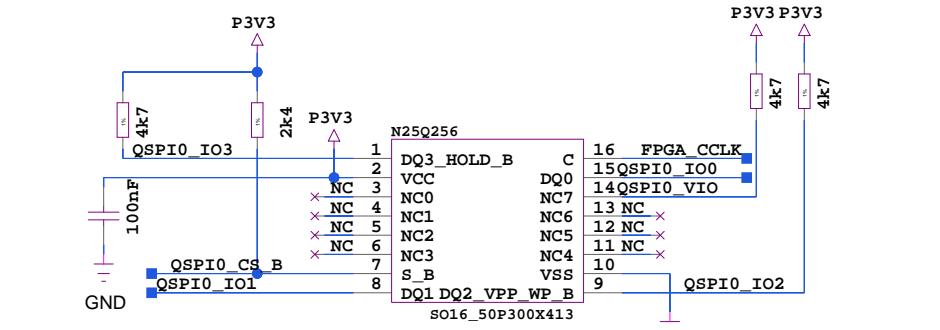
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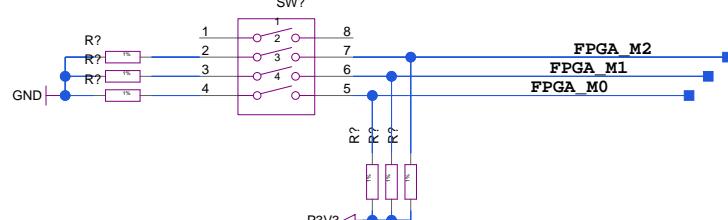
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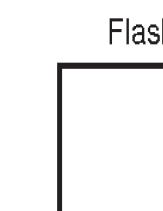


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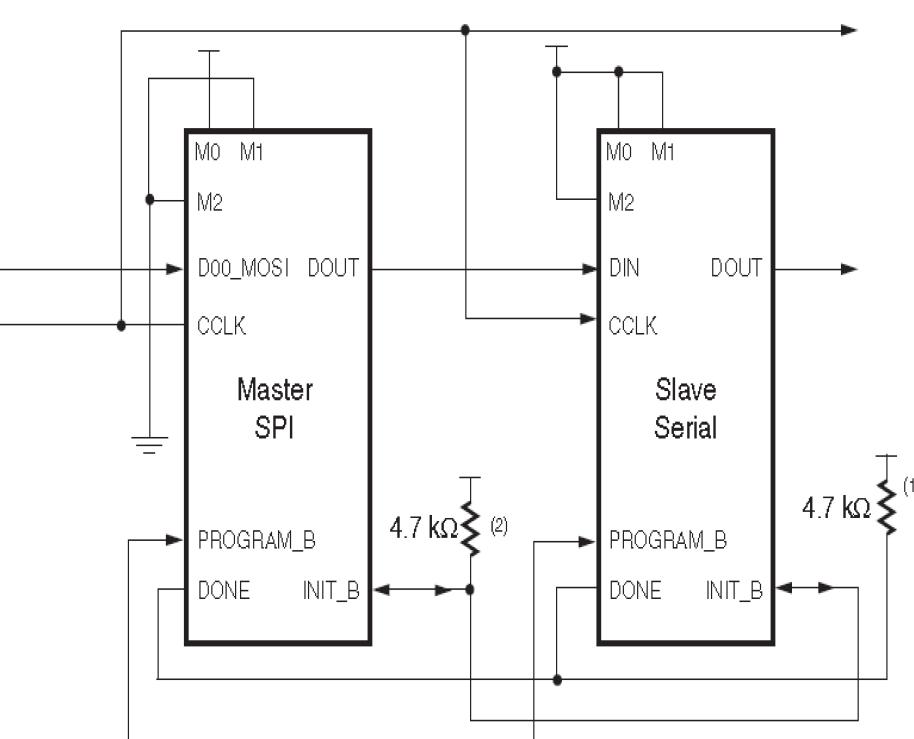
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Flash



PROGRAM_B



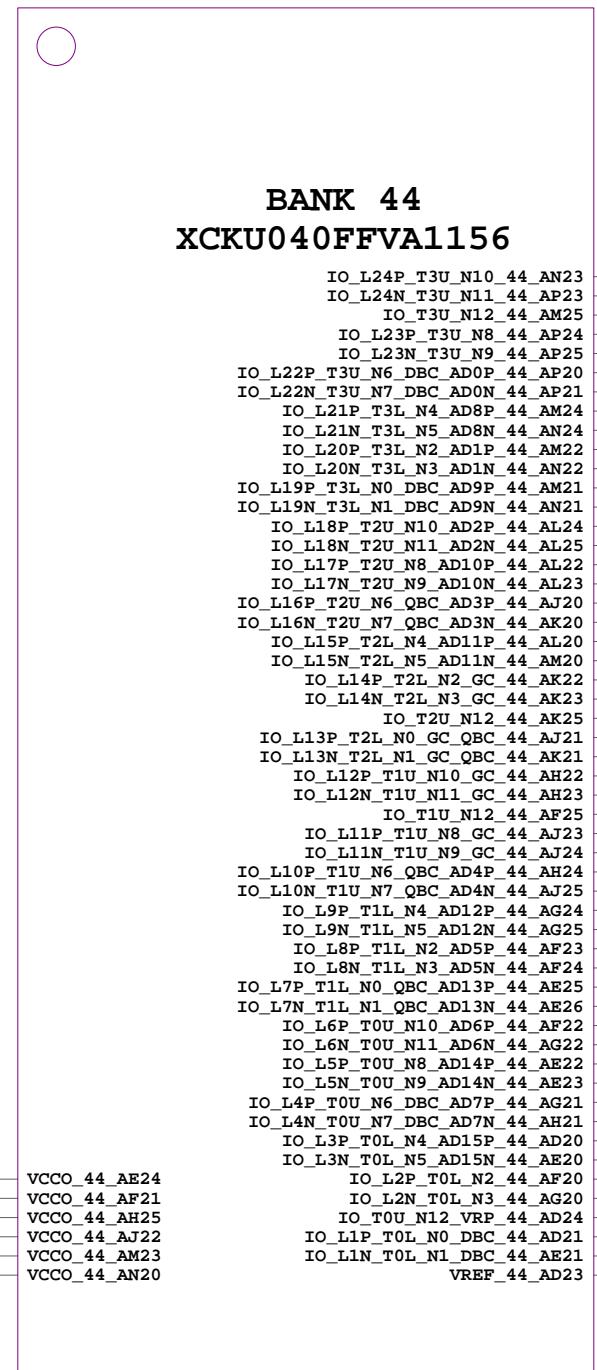
UG570_c12_01_081815

Layout: Place resistor and capacitor for VREF

Underneath the FPGA via array
right next to the via

Bank 44 HP

SOC_KU040_FFVA1156_IRON_REV0



U1 SOC_IRONWOOD_FF1156

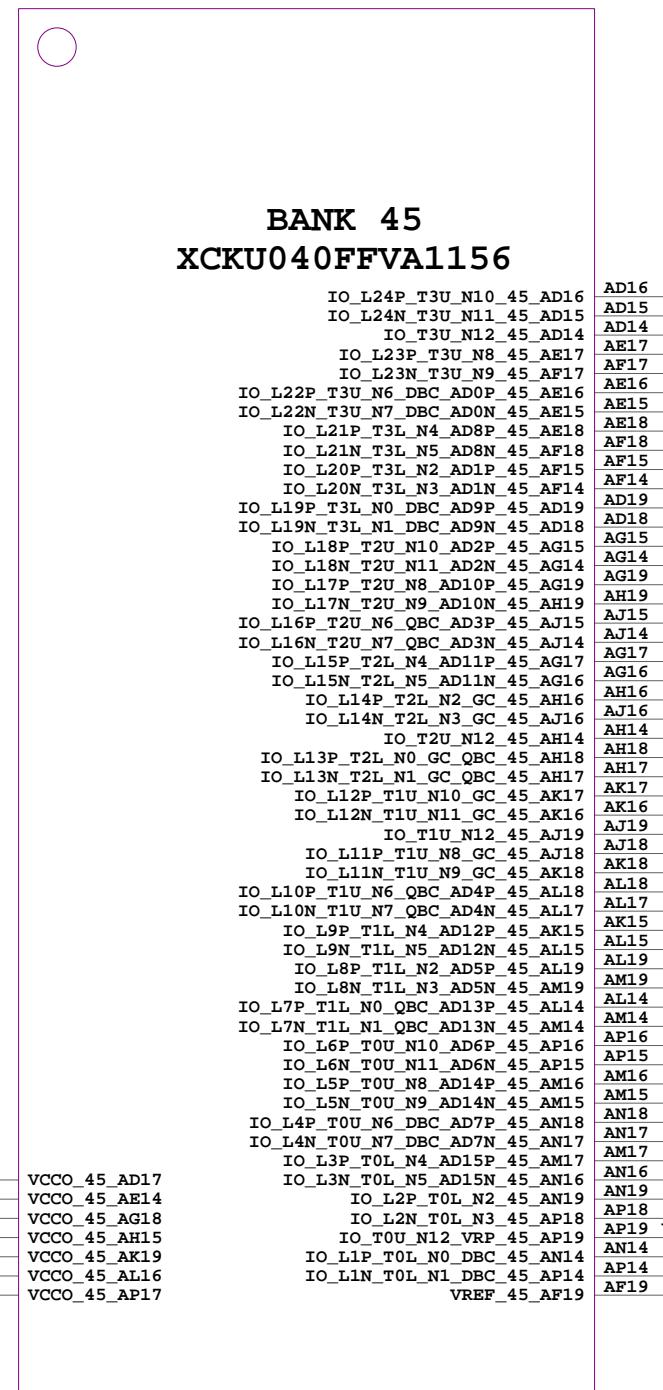
GND GND

SDRAM_DDR3_64

SDRAM_DDR3_x64

Bank 45 HP

SOC_KU040_FFVA1156_IRON_REV0



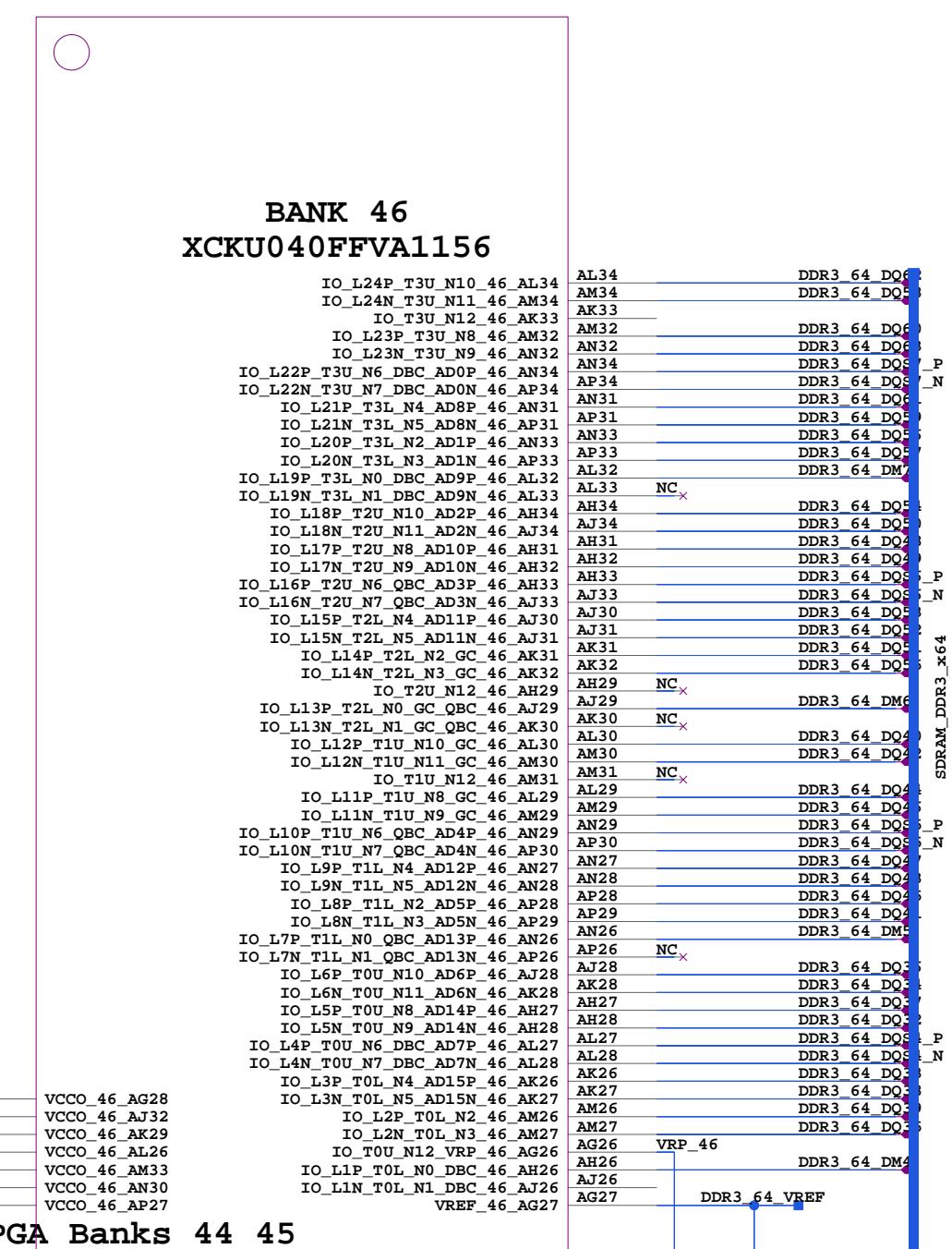
U1 SOC_IRONWOOD_FF1156

GND GND

SDRAM_DDR3_x64

Bank 46 HP

SOC_KU040_FFVA1156_IRON_REV0



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GND GND

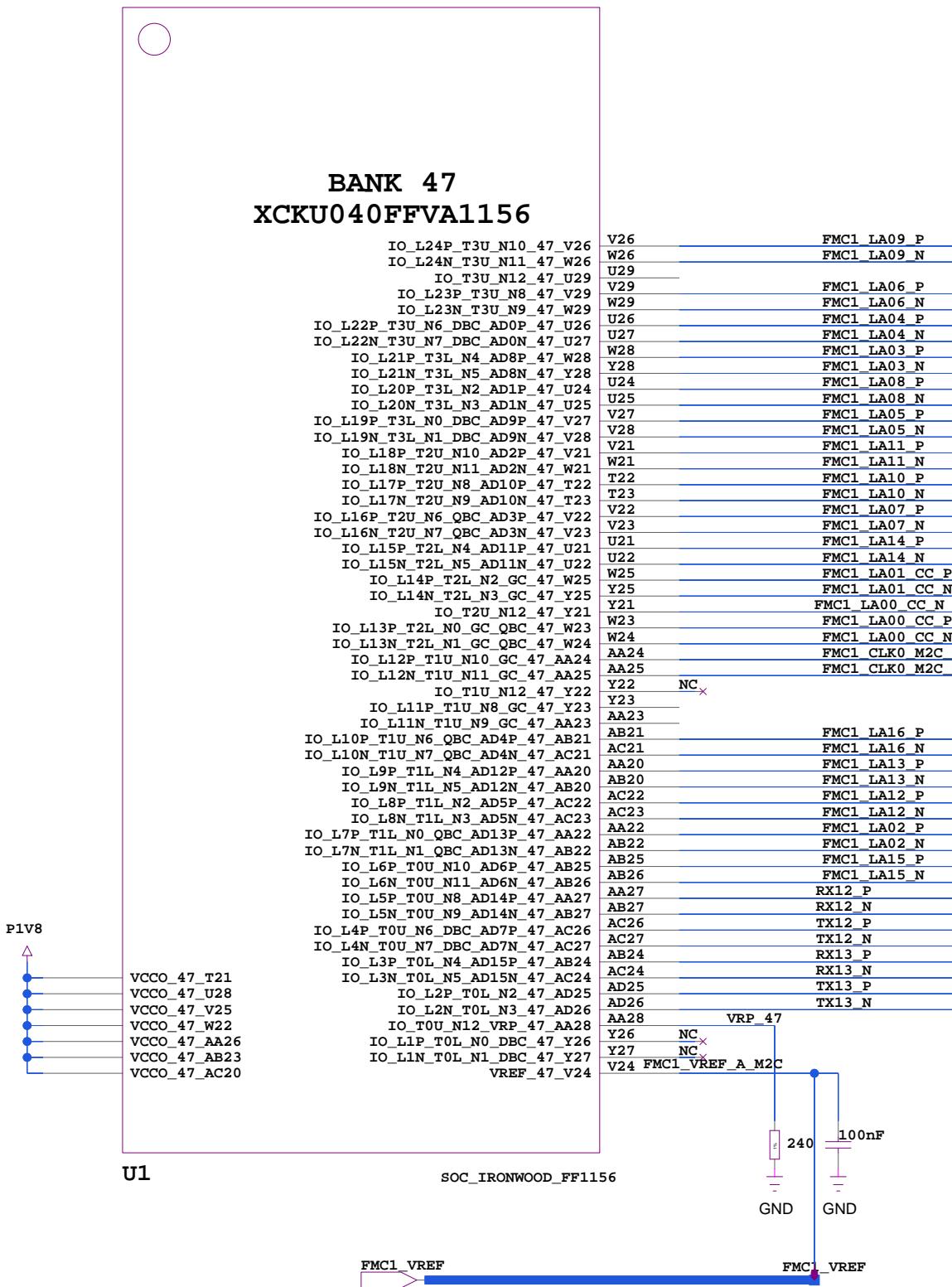
SDRAM_DDR3_x64

FPGA Banks 44 45

Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

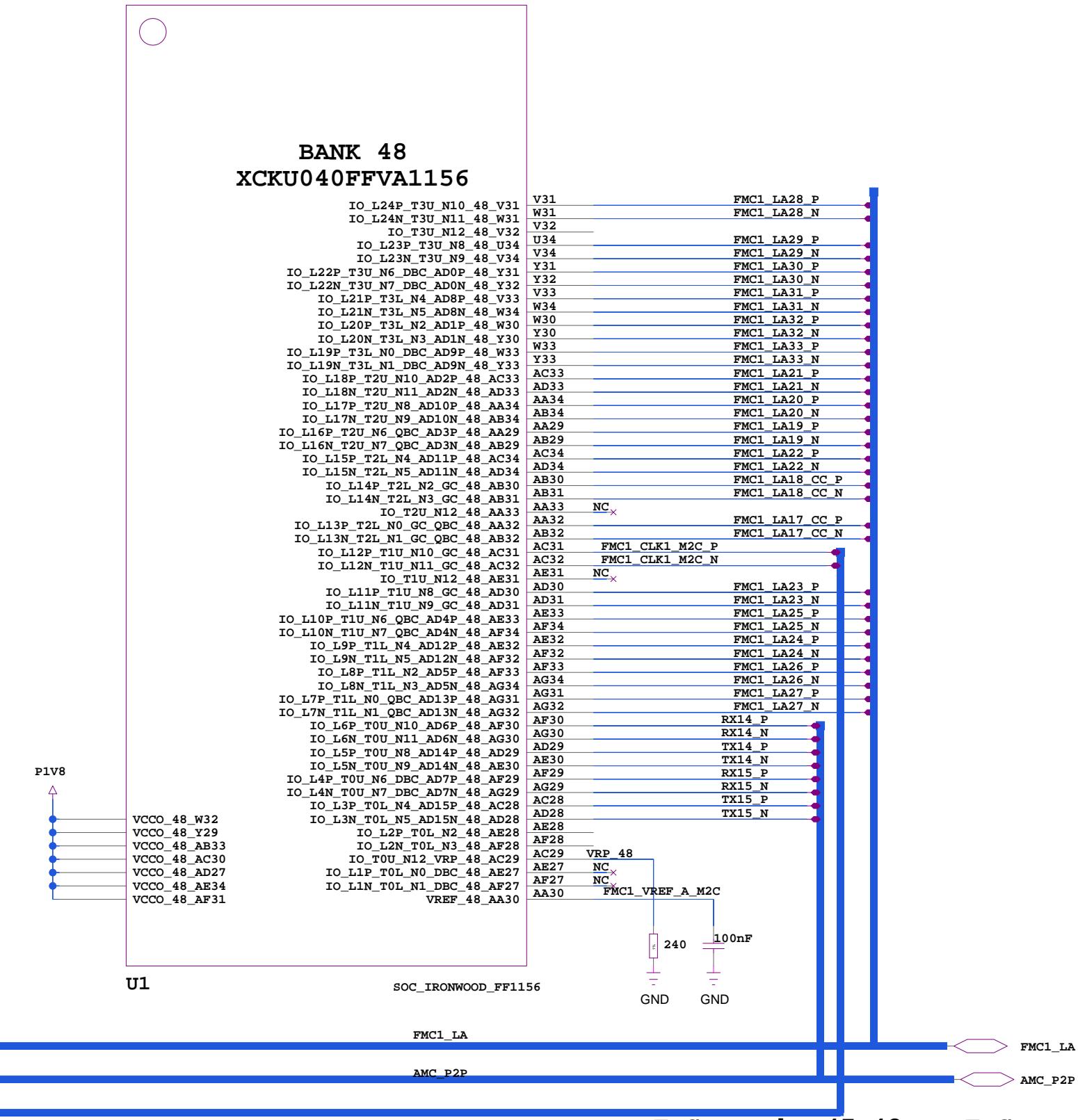
Bank 47 HP

SOC_KU040_FFVA1156_IRON_REV0



Bank 48 HP

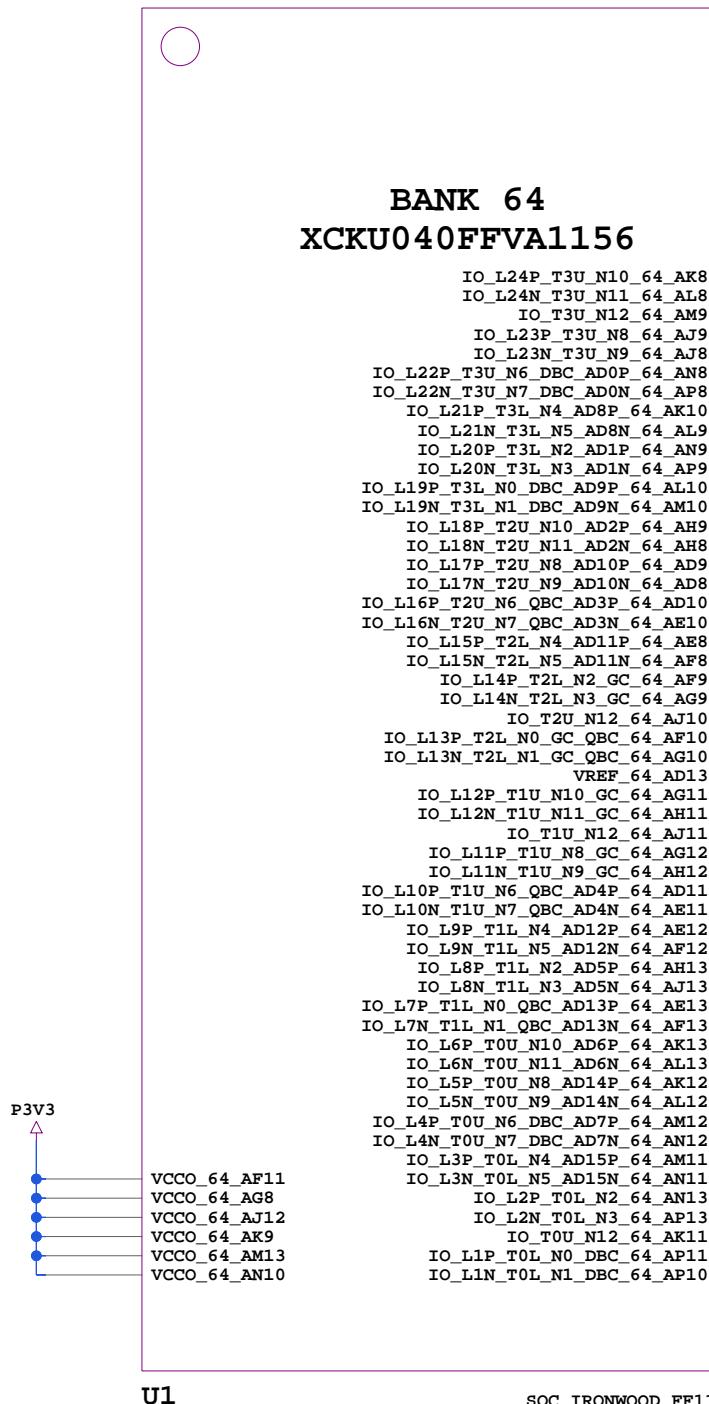
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FPGA Banks 47 48 HP FMC

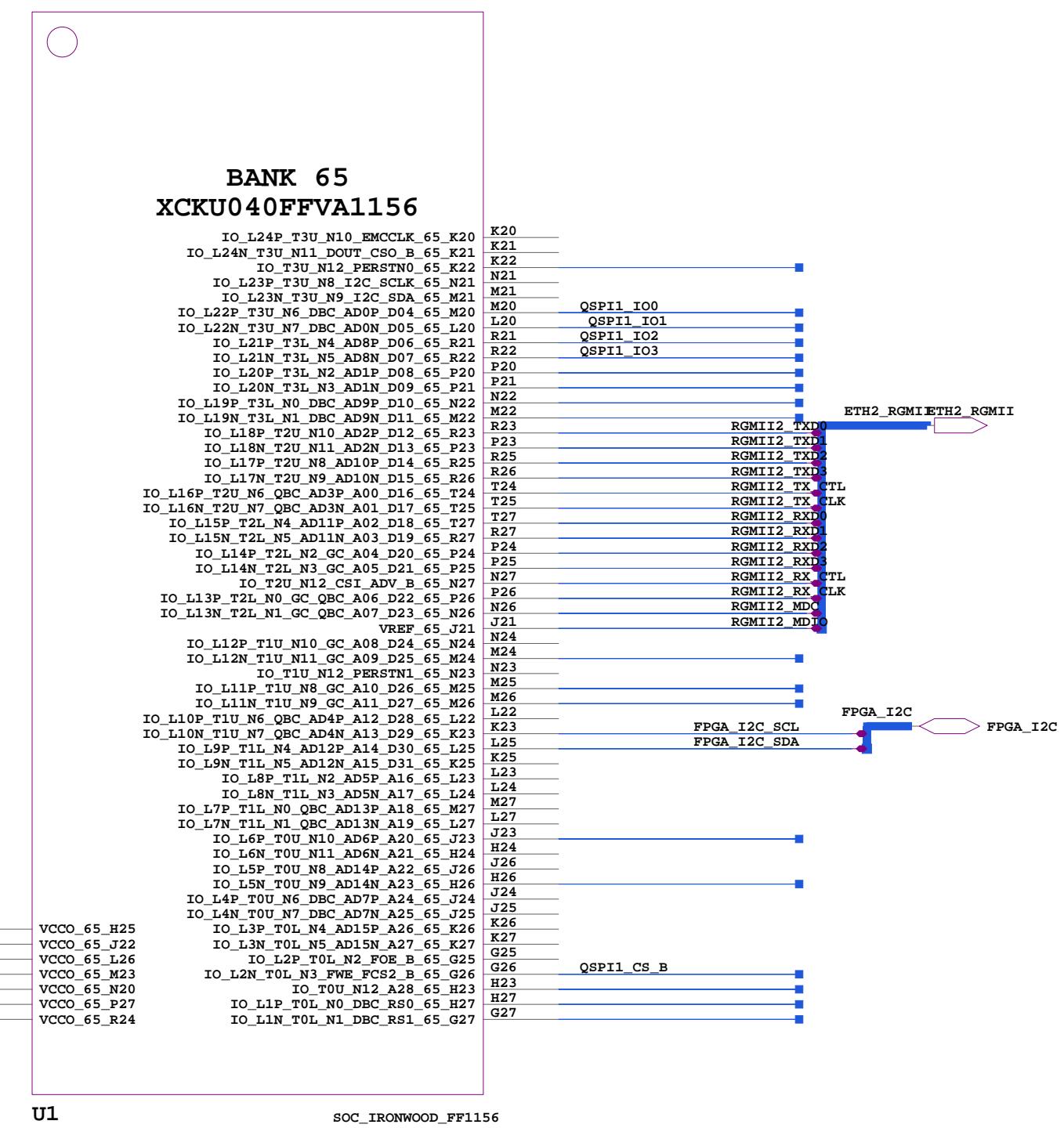
Bank 64 HR

SOC_KU040_FFVA1156_IRON_REV0



Bank 65 HR

SOC_KU040_FFVA1156_IRON_REV0



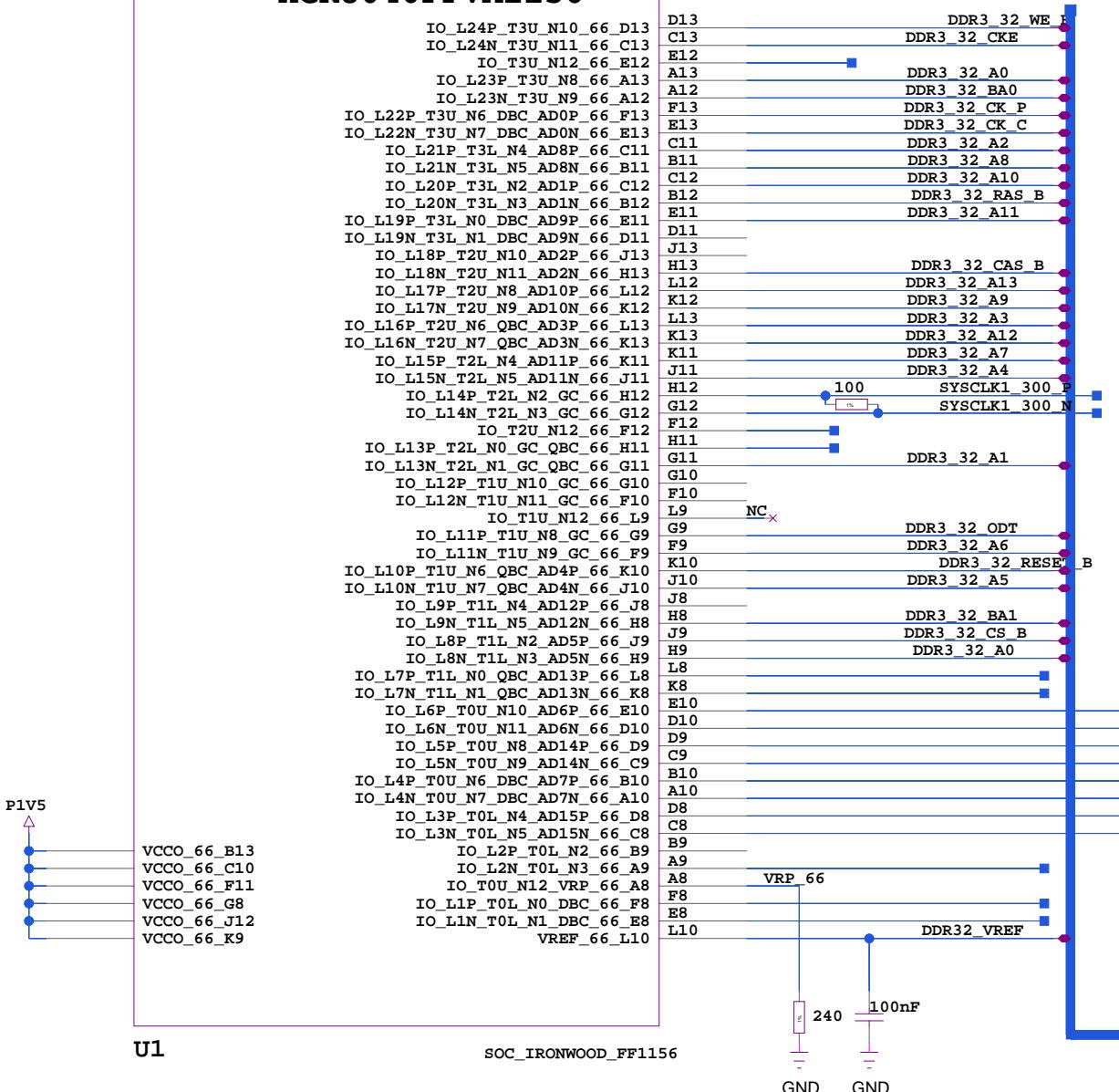
FPGA Banks 64 65 HR

Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

Bank 66 HP

SOC_KU040_FFVA1156_IRON_REV0

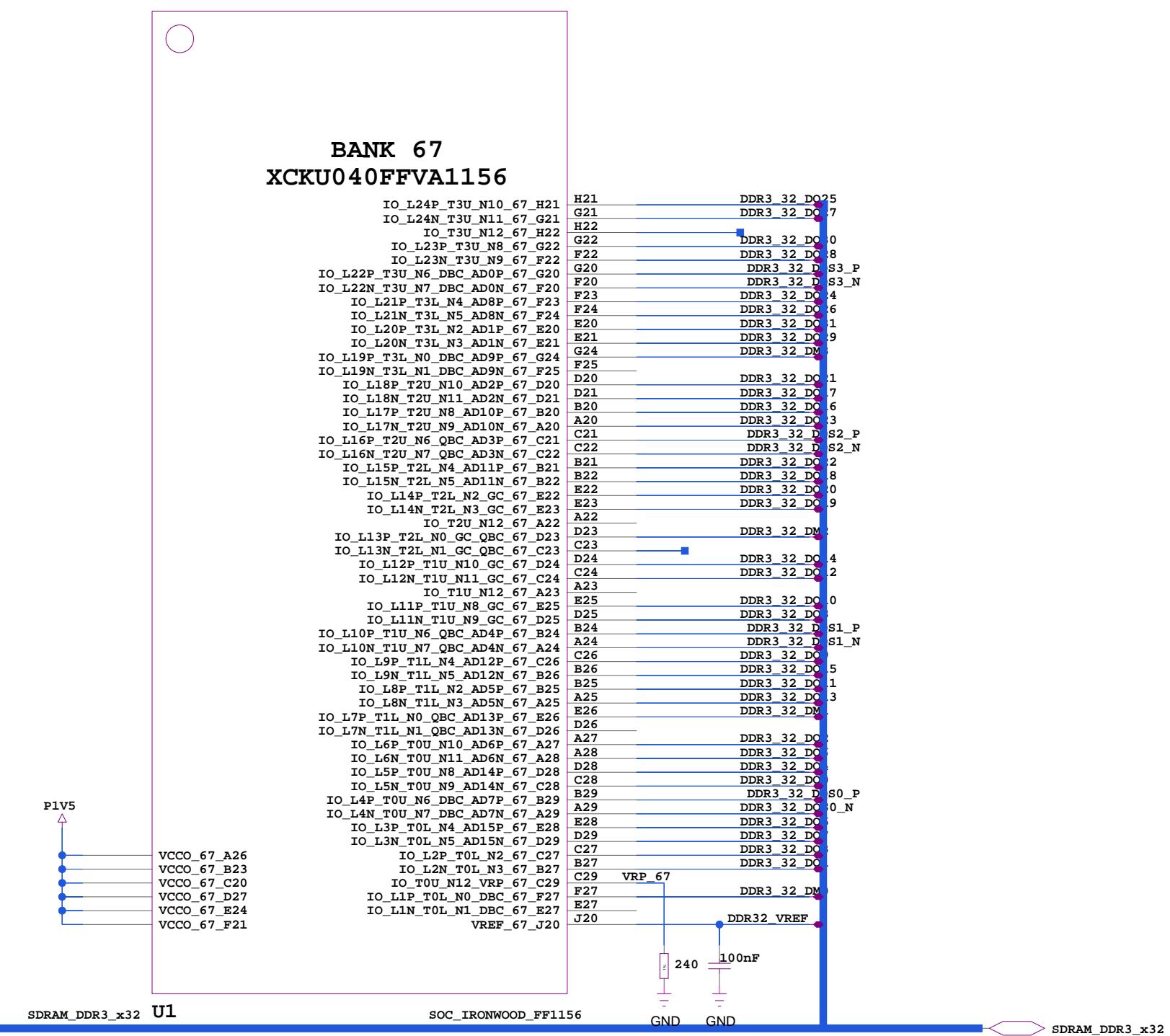
BANK 66 XCKU040FFVA1156



Bank 67 HP

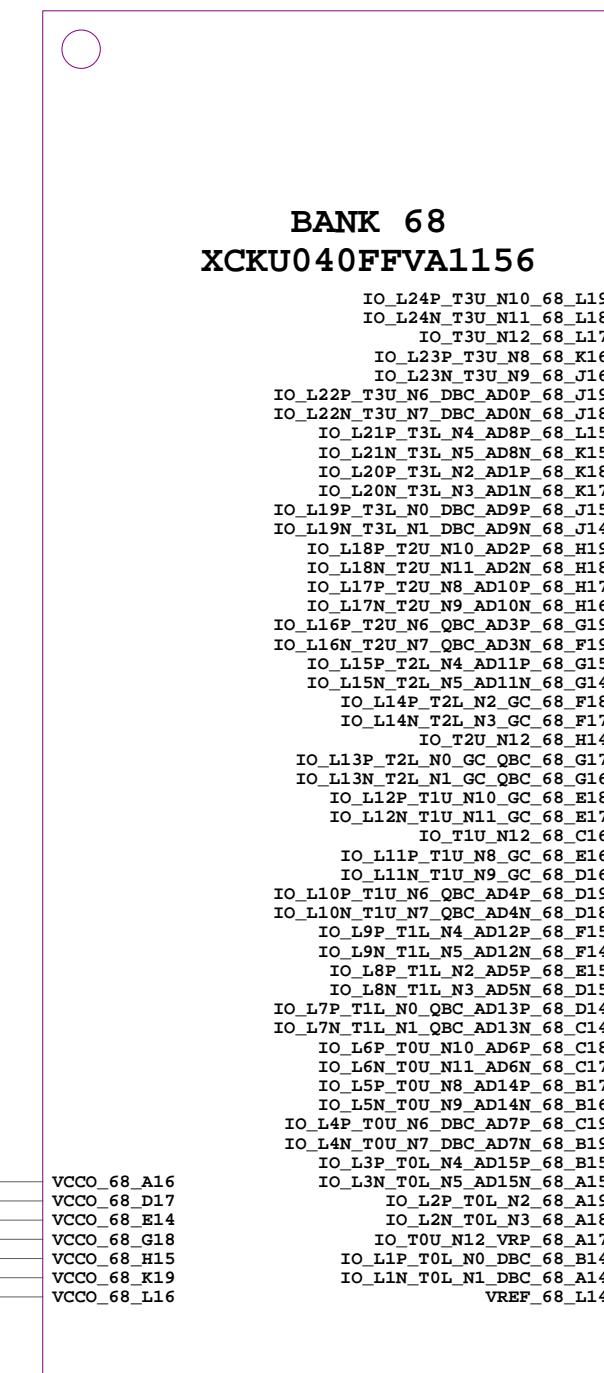
SOC_KU040_FFVA1156_IRON_REV0

BANK 67 XCKU040FFVA1156



Bank 68 HP

SOC_KU040_FFVA1156_IRON_REVD



U1

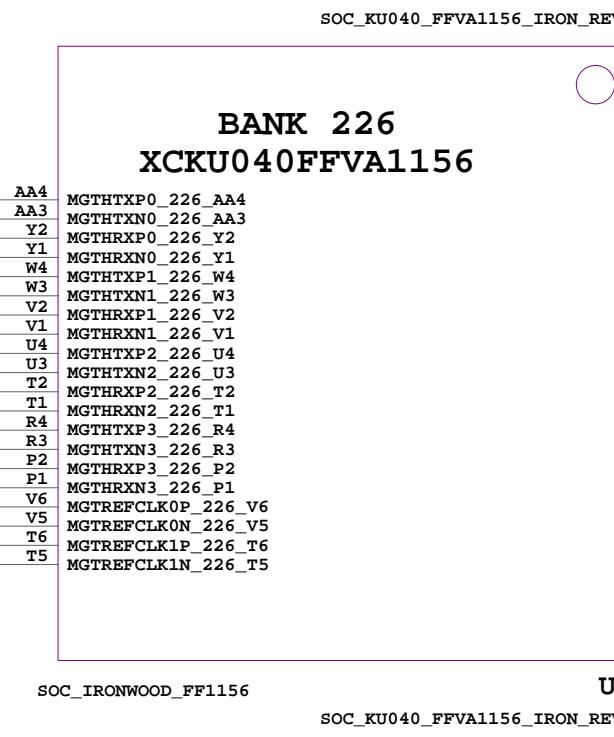
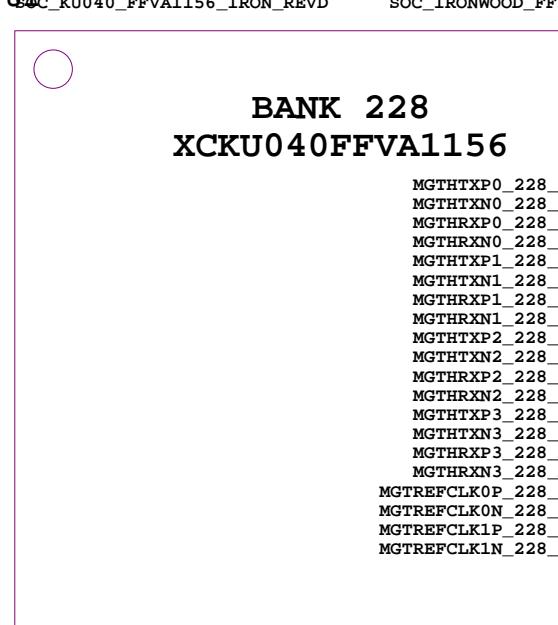
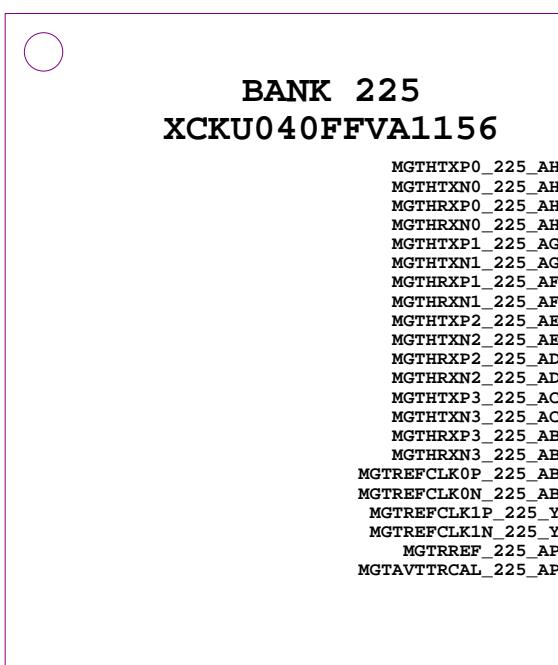
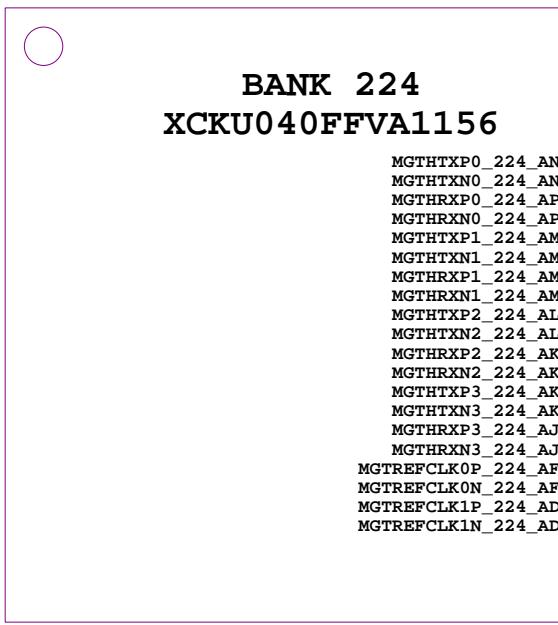
SOC_IRONWOOD_FF1156

Layout: Place resistor and capacitor for VREF

Underneath the FPGA via array
right next to the via

FPGA Bank 68

240
GND

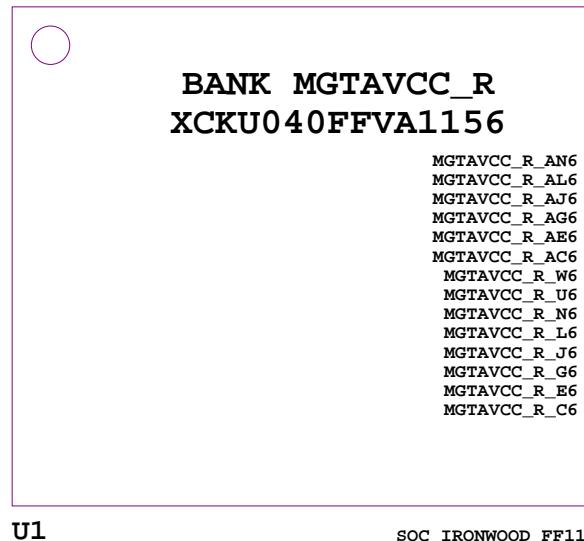


HP I/O Bank 48 H	HP I/O Bank 68 K	PCIe X0Y2	GTH Quad 228 X0Y16-X0Y19 E [R]
HP I/O Bank 47 G	HP I/O Bank 67 J	PCIe X0Y1	GTH Quad 227 X0Y12-X0Y15 D [R]
HP I/O Bank 46 F	HP I/O Bank 66 I	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [R]
HP I/O Bank 45 E	HR I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [R] (RCAL)
HP I/O Bank 44 D	HR I/O Bank 64 R	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [R]

X16439-031816

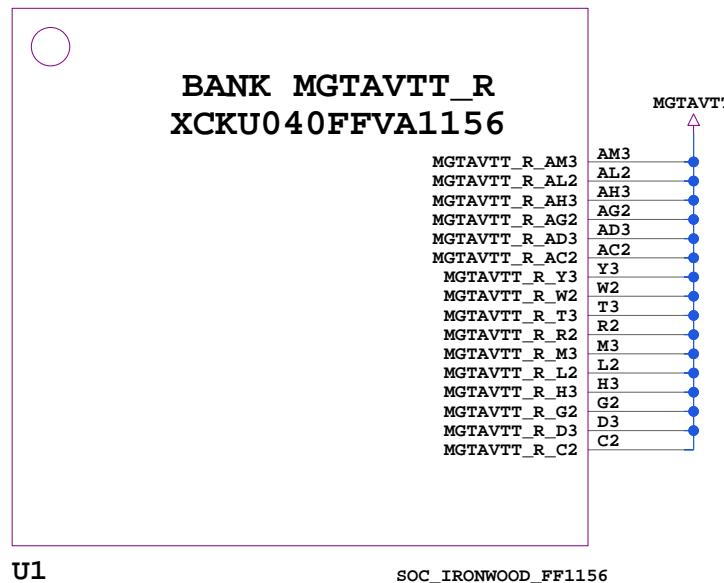
Figure 1-13: XCKU040 Banks in FFVA1156 Package

SOC_KU040_FFVA1156_IRON_REV0



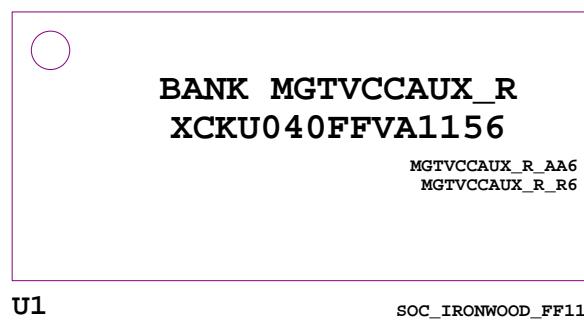
U1 SOC_IRONWOOD_FF1156

SOC_KU040_FFVA1156_IRON_REV0



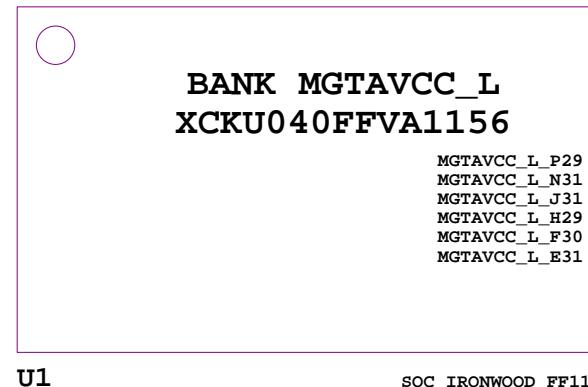
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SOC_KU040_FFVA1156_IRON_REV0



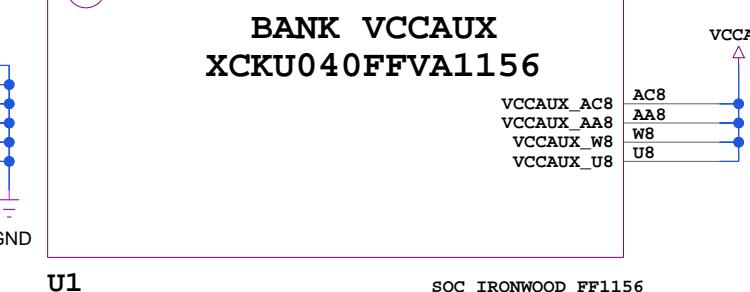
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SOC_KU040_FFVA1156_IRON_REV0



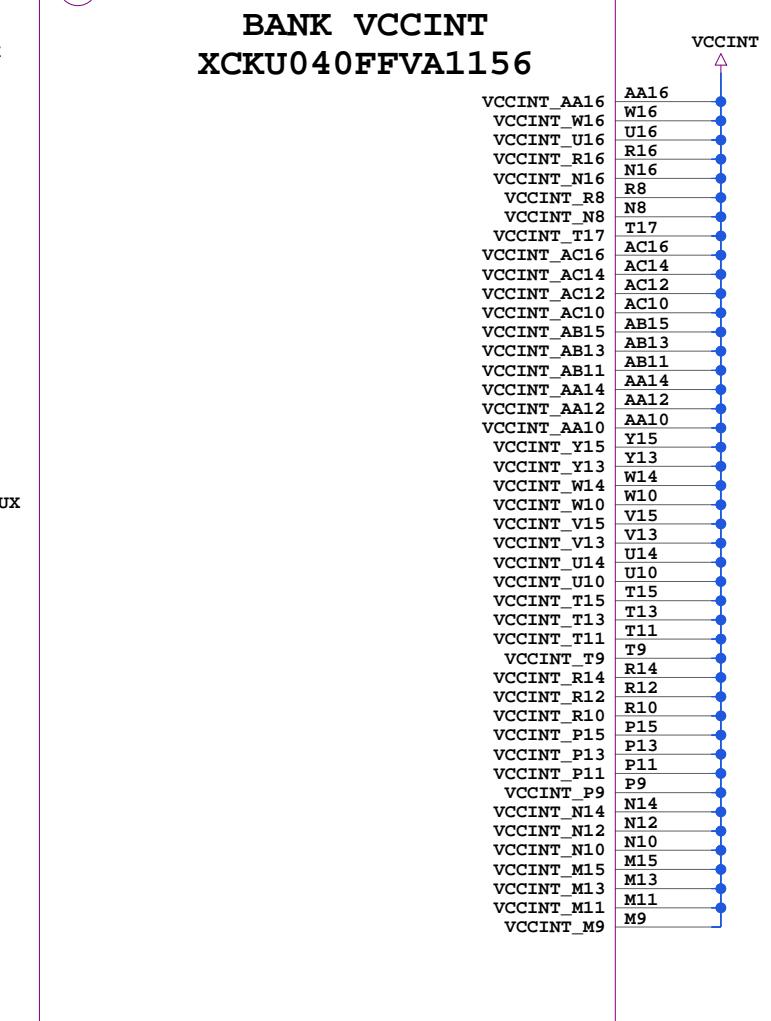
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SOC_KU040_FFVA1156_IRON_REV0



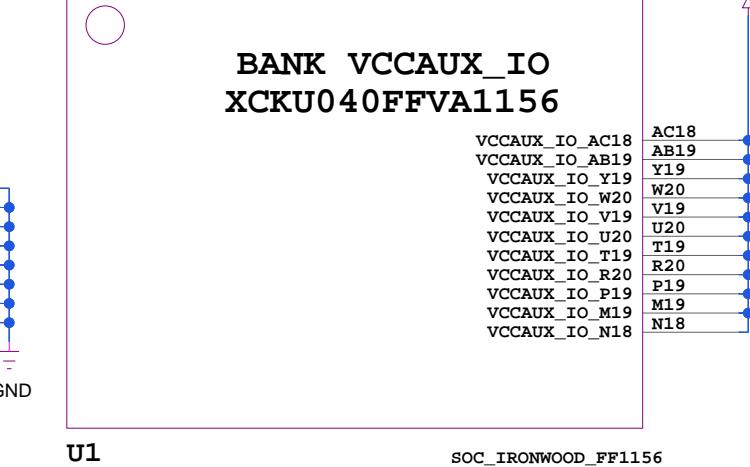
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SOC_KU040_FFVA1156_IRON_REV0



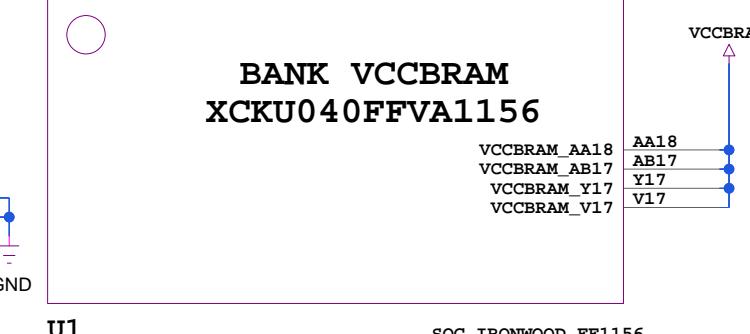
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SOC_KU040_FFVA1156_IRON_REV0



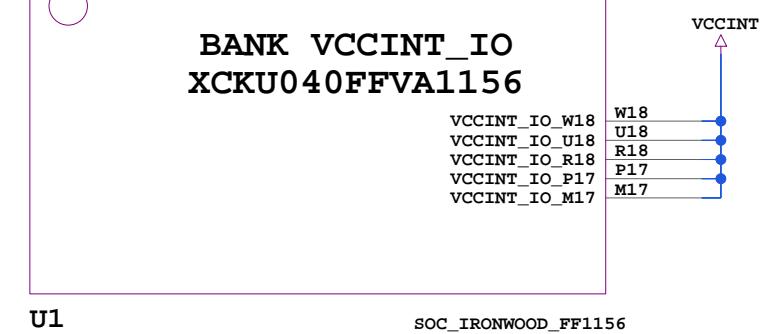
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SOC_KU040_FFVA1156_IRON_REV0



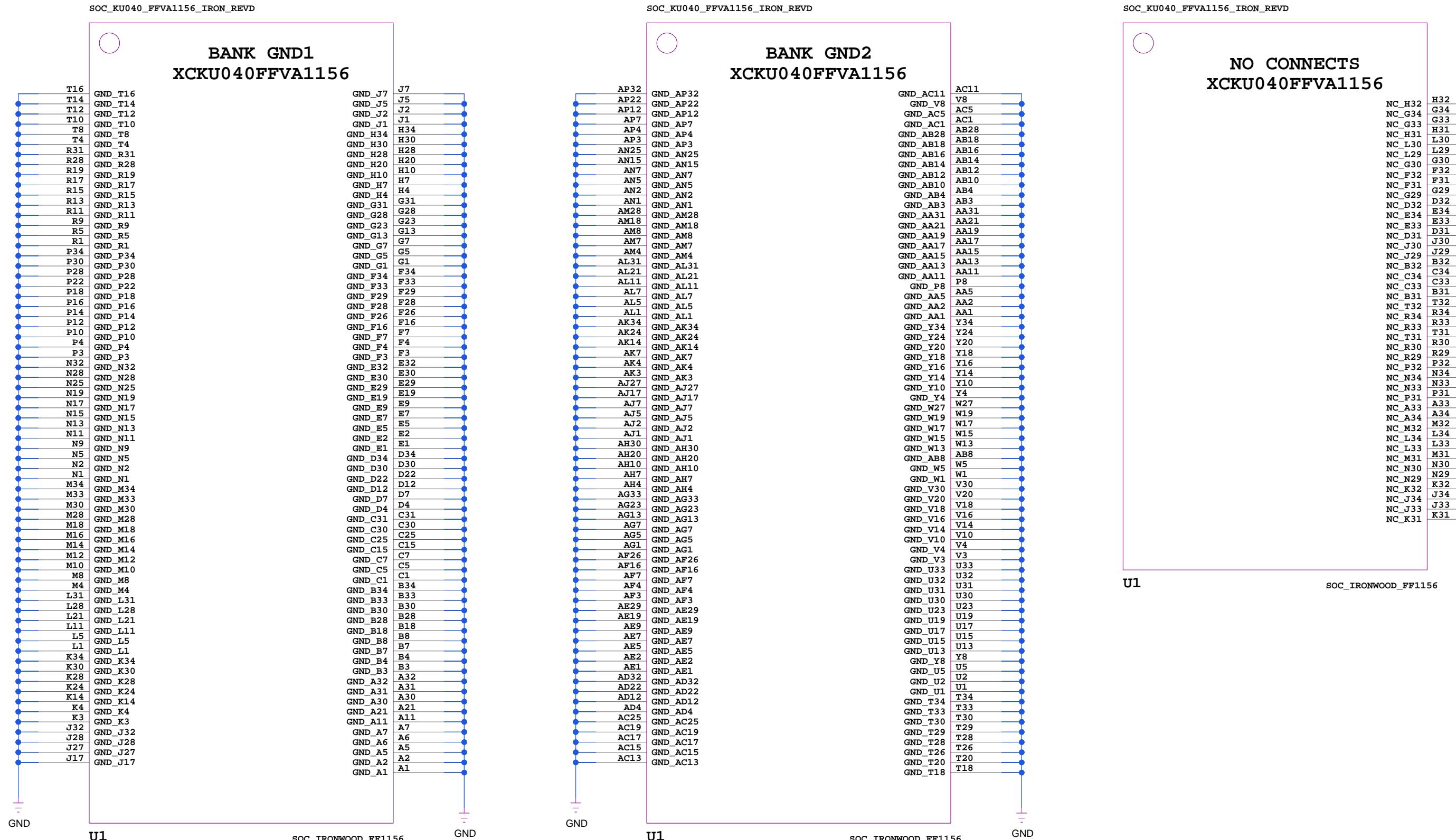
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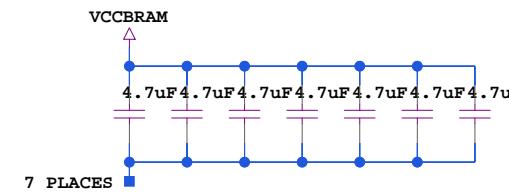
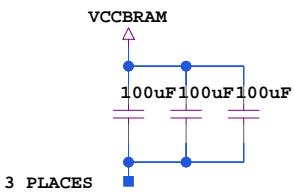
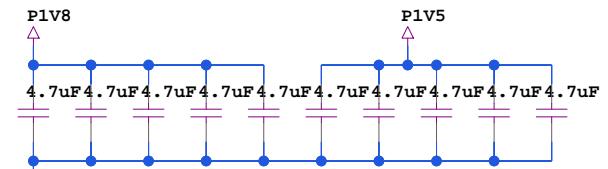
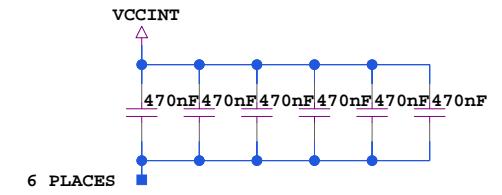
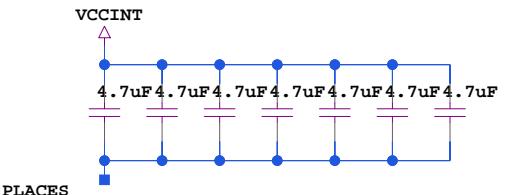
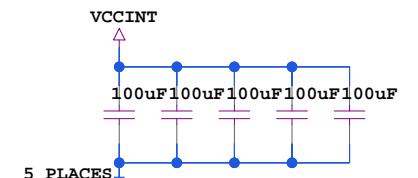
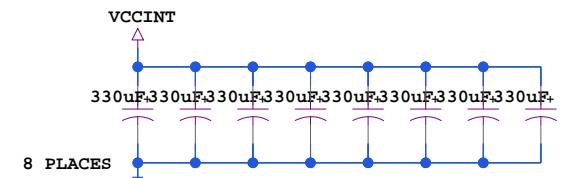
SOC_KU040_FFVA1156_IRON_REV0



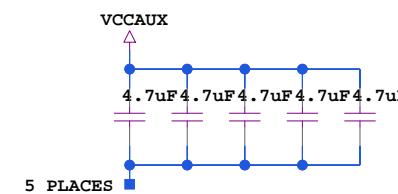
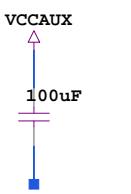
U1 SOC_IRONWOOD_FF1156

FPGA Power 1

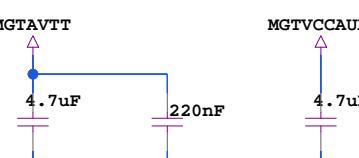
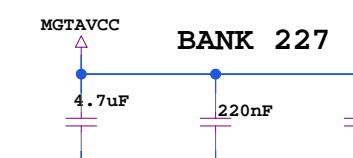
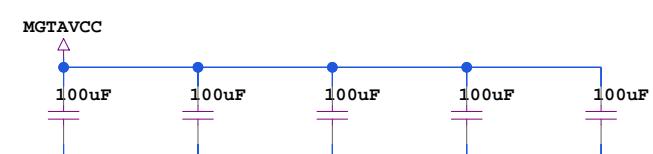
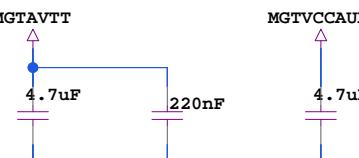
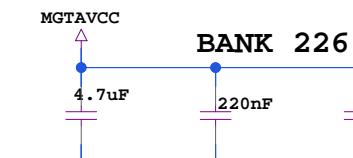
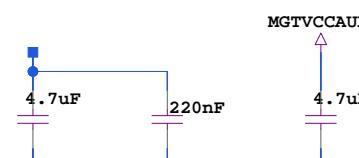
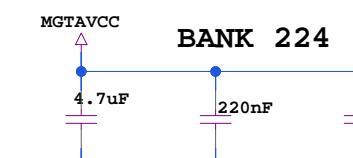
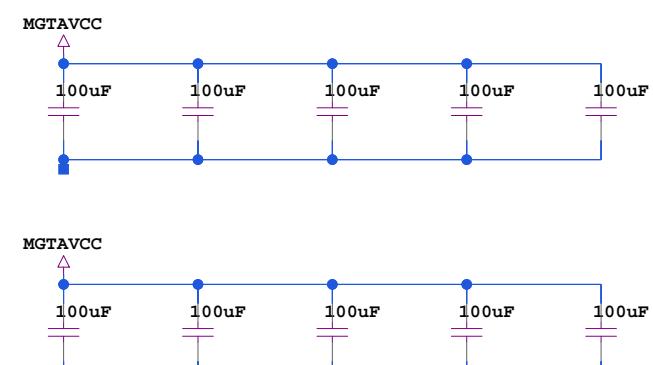
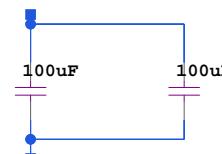




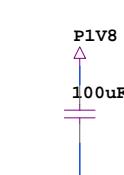
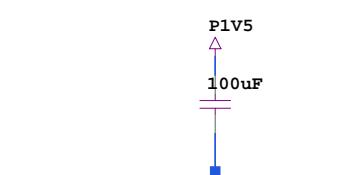
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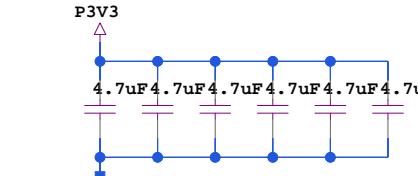
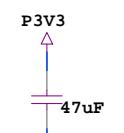
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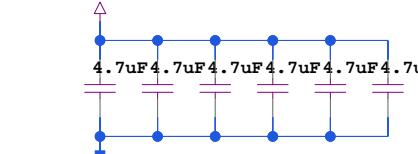
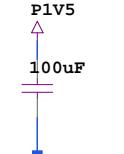
VCCO_47 / VCCO_48 VCCO_66 / VCCO_67 VCCO_68

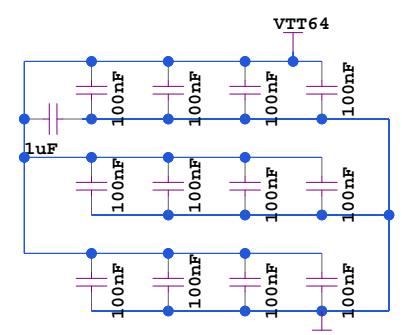
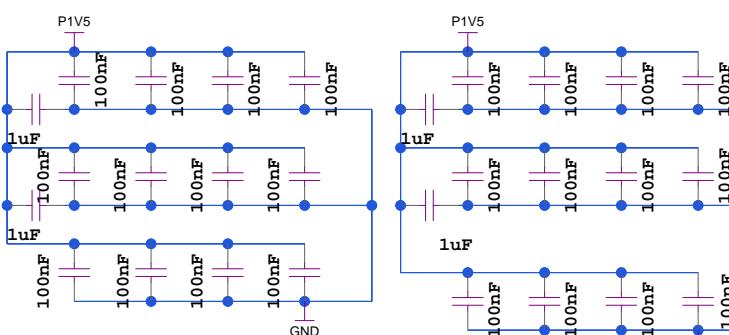
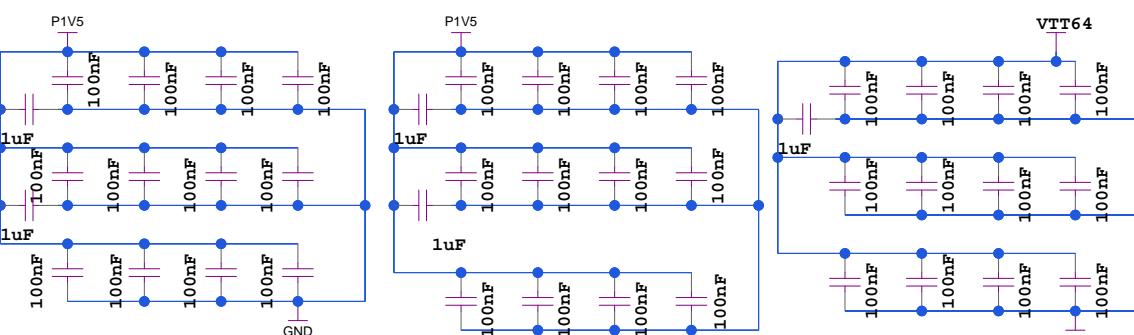
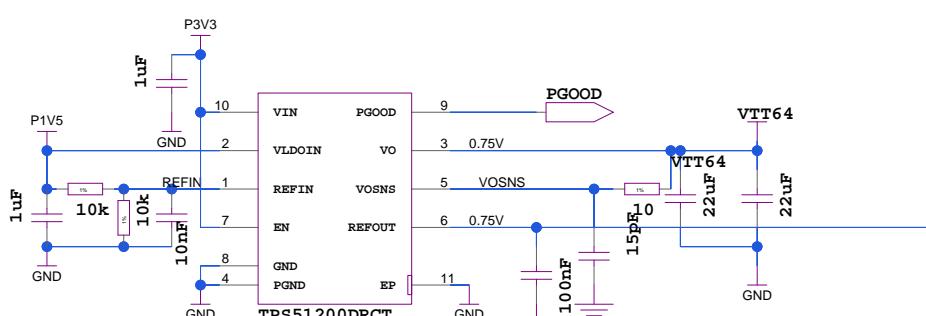
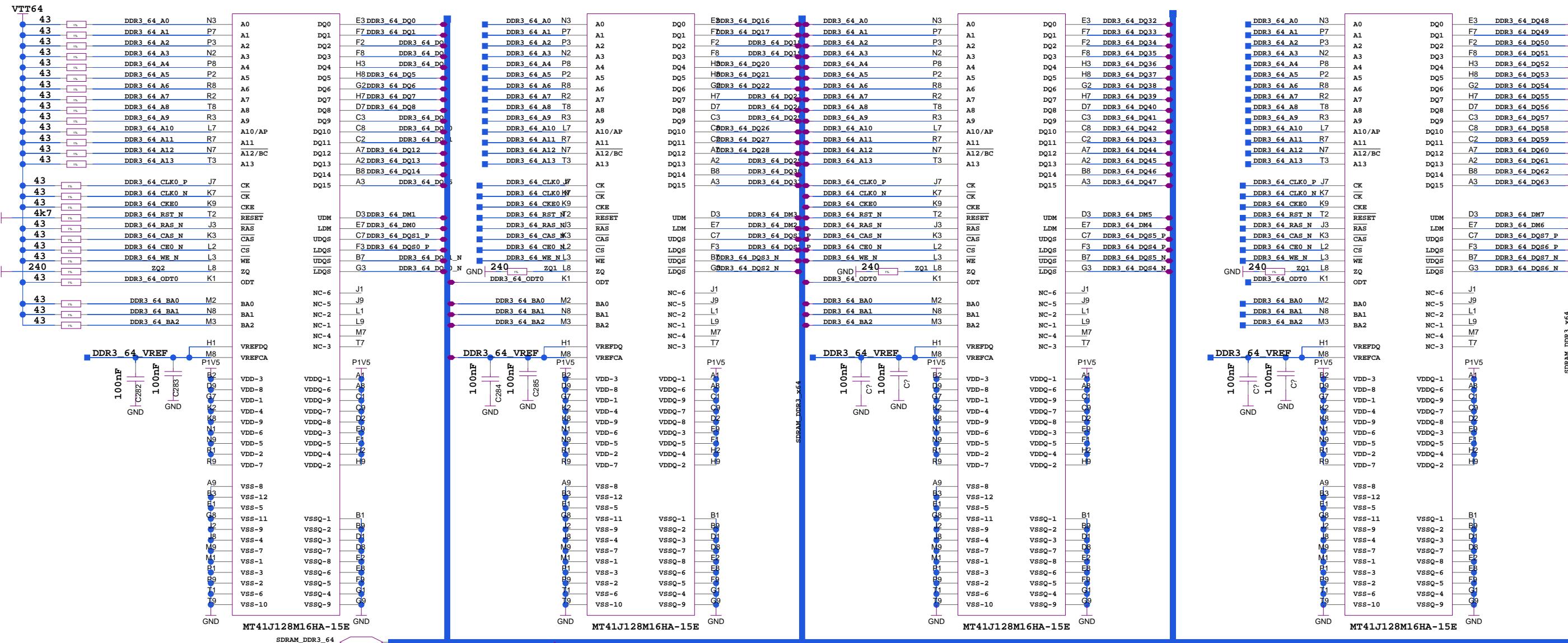


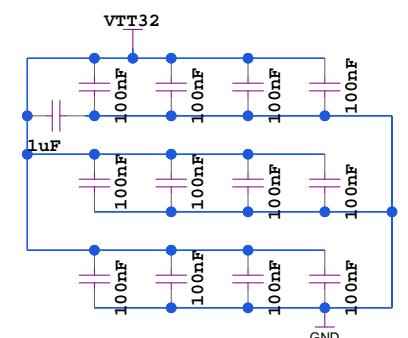
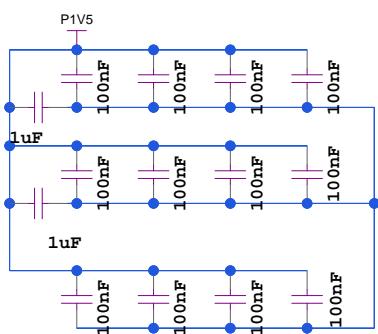
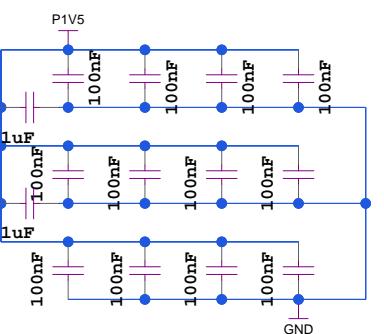
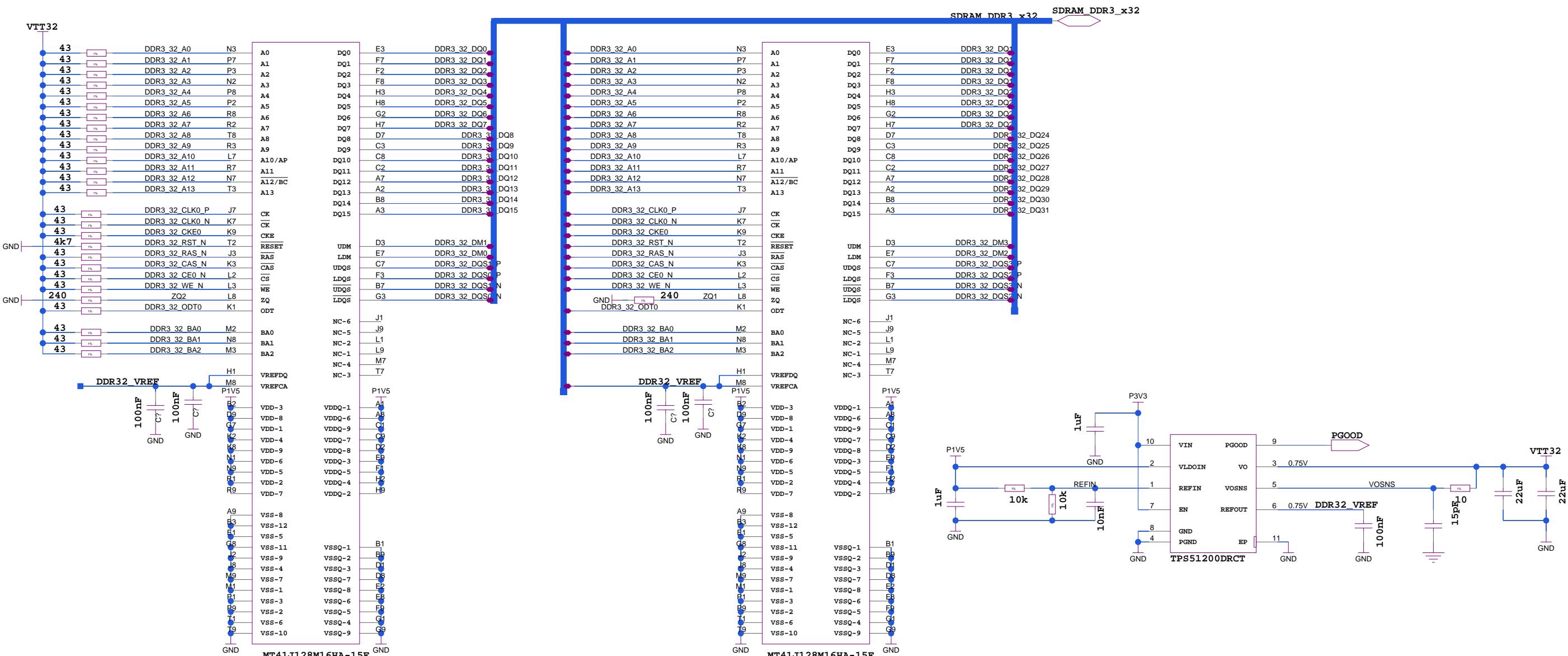
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VCCO_44 / VCCO_45 / VCCO_46







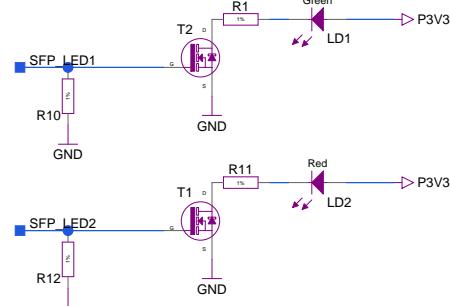
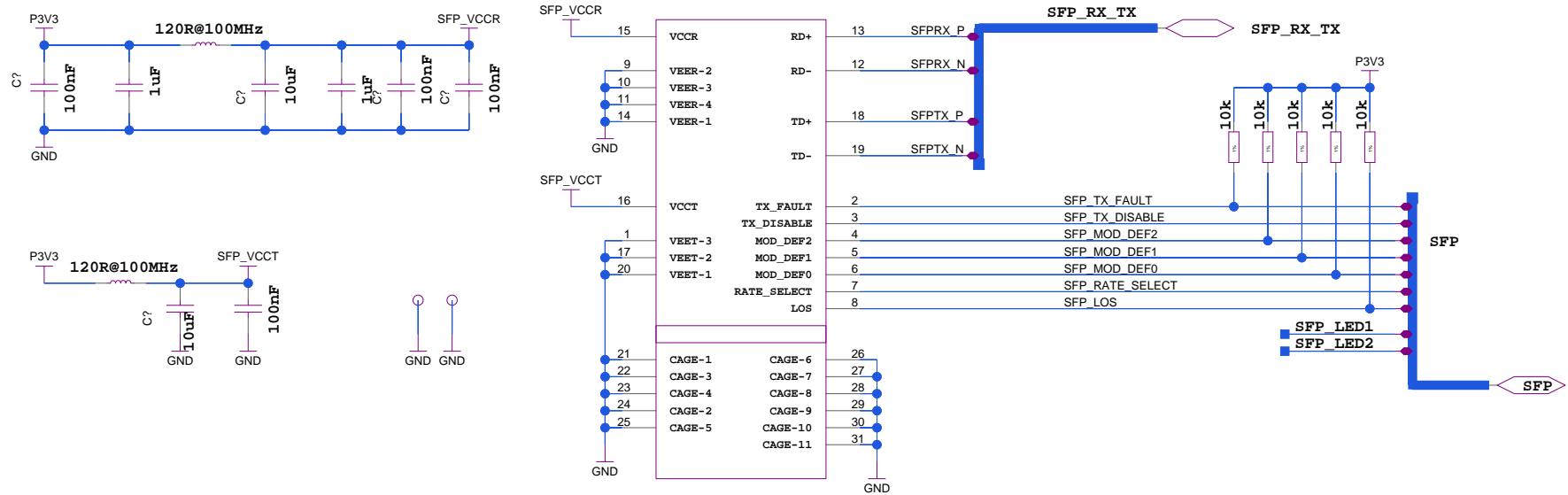
SDRAM_MEM

TITLE

SIZE A3 DWG NO

DRAWN BY <YOUR NAME HERE> SHEET of 1 1

29/10



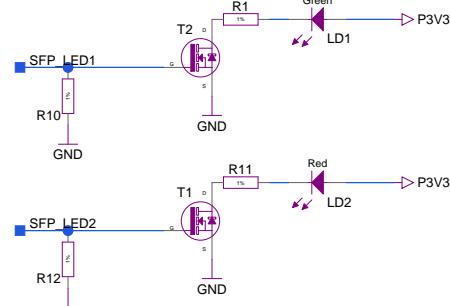
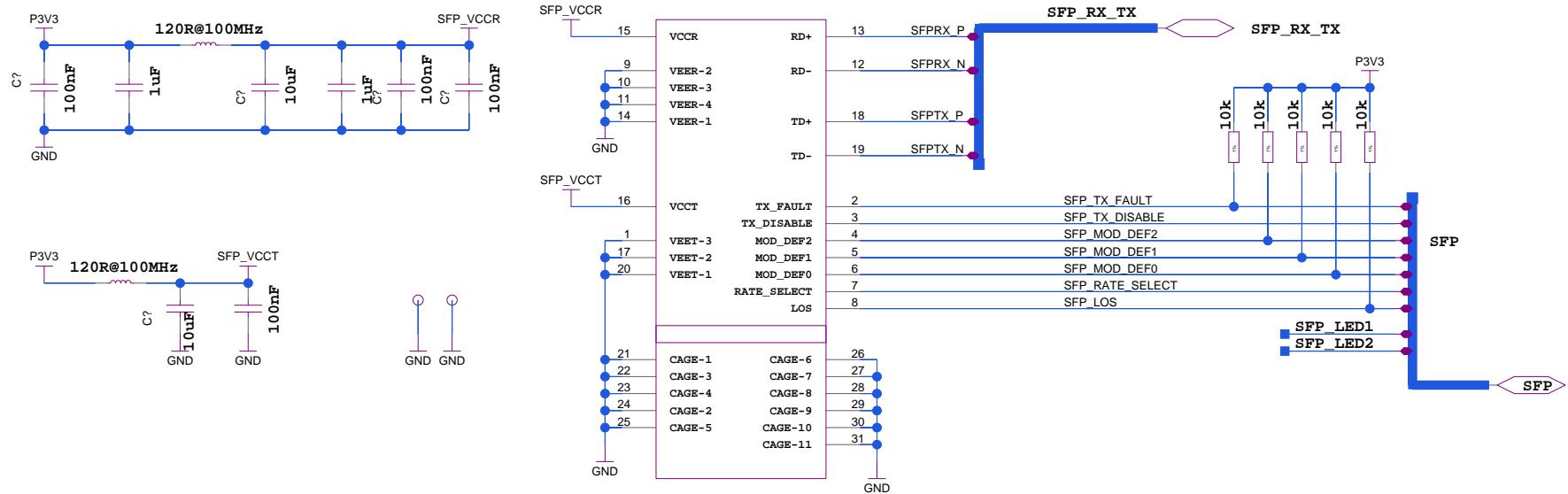
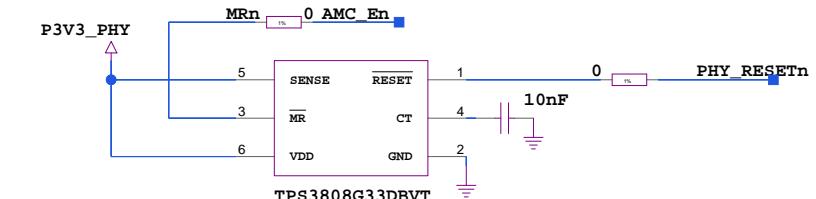


Table 6-1. Reset Configuration Pins, 15-Pin Mode (COL=0)

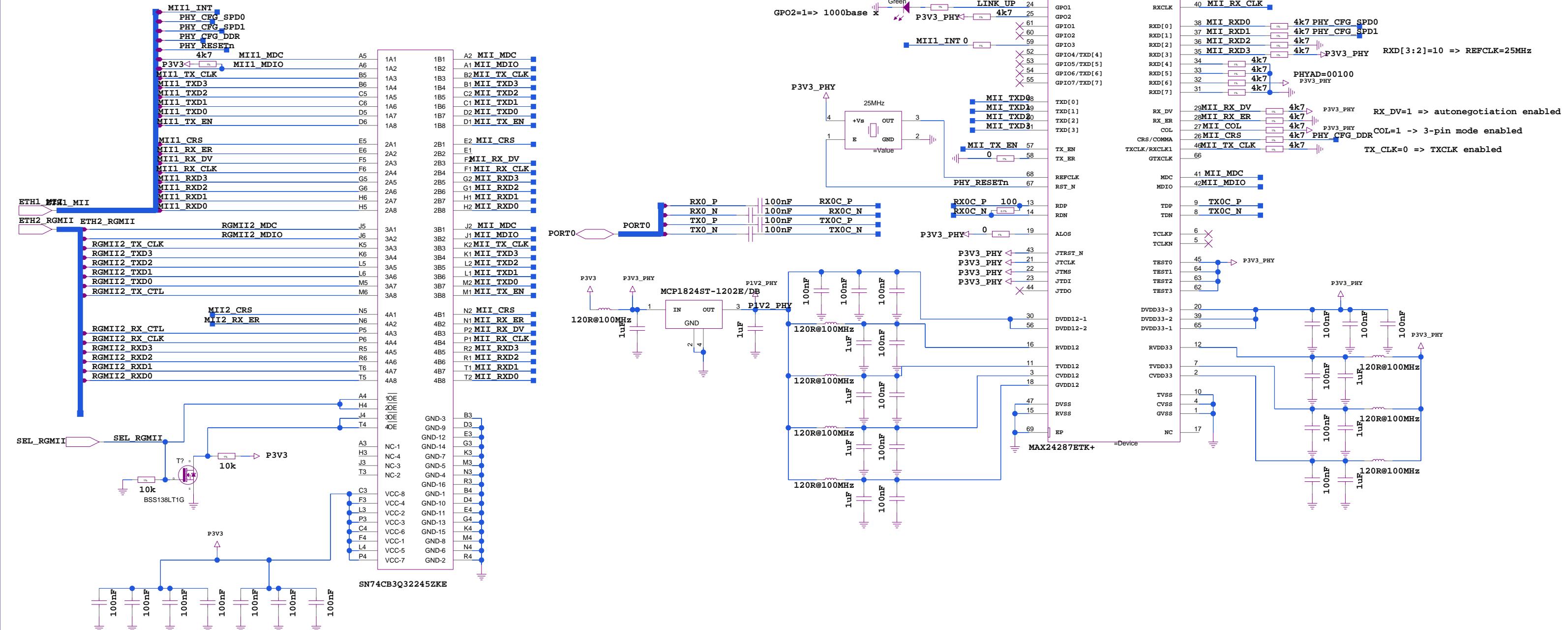
Pin	Function	Register Bit Affected	Notes
CRS	Double Date Rate	GMIICR.DDR-CRS	See Table 6-2. 0=DCE, 1=DTE
GPO2	10/100 MII DTE or DCE	10/100 MII: GMIICR.DTE_DCE Other: Serial Interface Other: PCSCR.BASEX	0=DCE, 1=DTE (serial interface is configured for SGMII mode, PCSCR.BASEX=0) 0=SGMII, 1=1000BASE-X
GPO1	GPIO1 Configuration	GPIOCR1.GPIO1_SEL[2]	See Table 6-2.
RXD[1:0]	Parallel Interface Speed	GMIICR.SPDI[1:0]	See Table 6-2.
RXD[3:2]	REFCLK Frequency	None	0=10MHz, 01=12.8MHz, 10=25MHz, 11=125MHz
RXD[7:4]	MDIO PHYAD[3:0]	Internal MDIO PHYAD register	Note: PHYAD[4:0]=11111 enables factory test mode. Do not use.
RX_ER	MDIO PHYAD[4]	(device address on MDIO bus)	0=one-clock mode (125MHz) 1=normal mode (62.5MHz x 2)
RX_DV	TBI Mode	GMIICR.TBI_RATE	0=Disable, 1=Enable
	Other: Auto-negotiation	BMCR.AN_EN	0=high impedance 1=125MHz from TX PLL
TXCLK	TXCLK Enable	GMIICR.TXCLK_EN	Ignored in MII mode and TBI with two 62.5MHz Rx clocks

Table 6-2. Parallel Interface Configuration

SPD[1]	SPD[0]	Speed	DDR=0	DDR=1
0	0	10Mbps	MII	RGMII-10
0	1	100Mbps	MII	RGMII-100
1	0	1000Mbps	GMII	RGMII-1000
1	1	1000Mbps	TBI	RTBI



We want to have:
 SPD[1:0] DDR
 01 0 in MII
 10 1 in RGMII-1000



1

2

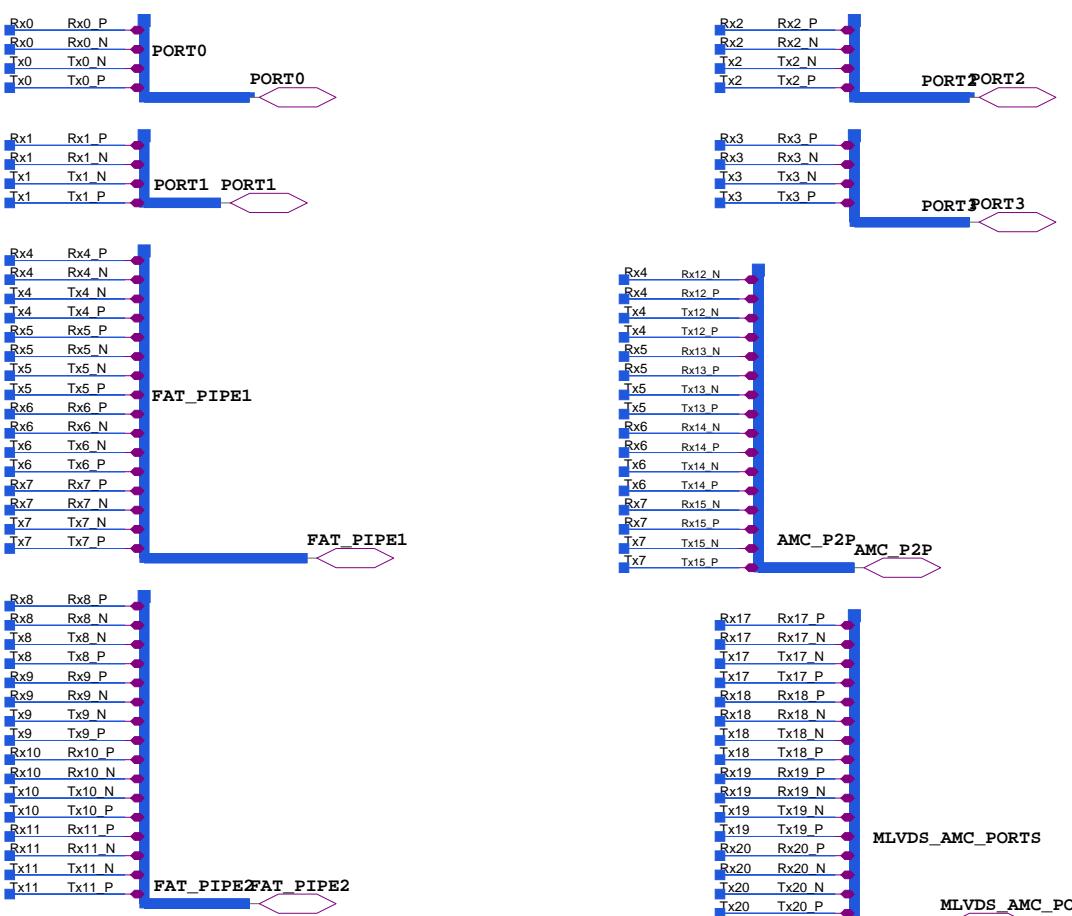
3

4

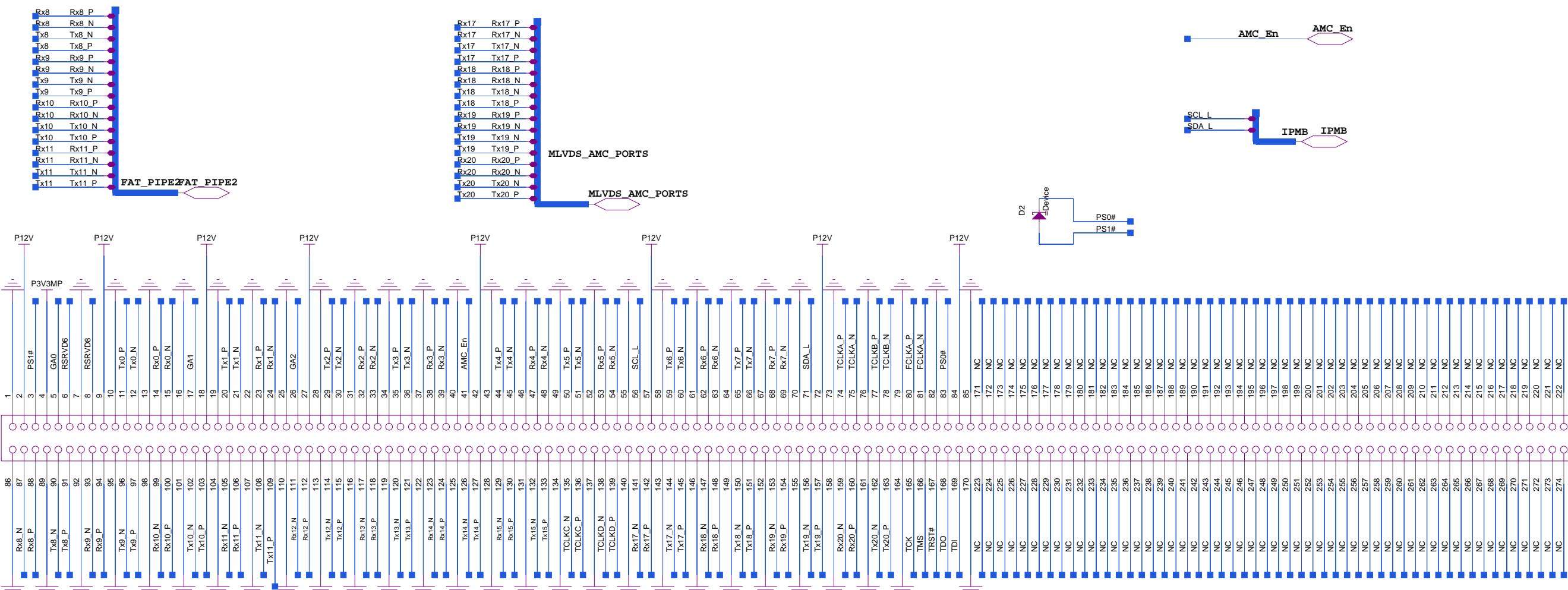
5

6

A



B



P2P Signals - NOT USED



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- Dimensions are in MM, nominal values used
- Component height rule derived from AMC Base Specification.PDF, Page 62
- The two corners of outline near the edge-connector are approximated, see AMC Base Specification.PDF, Page 59
- Stackup is not specified in AMC Base Specification.PDF or implemented in this template.

Sheet Title			AMC Top Sheet		
Project Title					
Size: A3			Item: Revision:		
Date:	Time:	File:	Sheet 1 of 30		

1

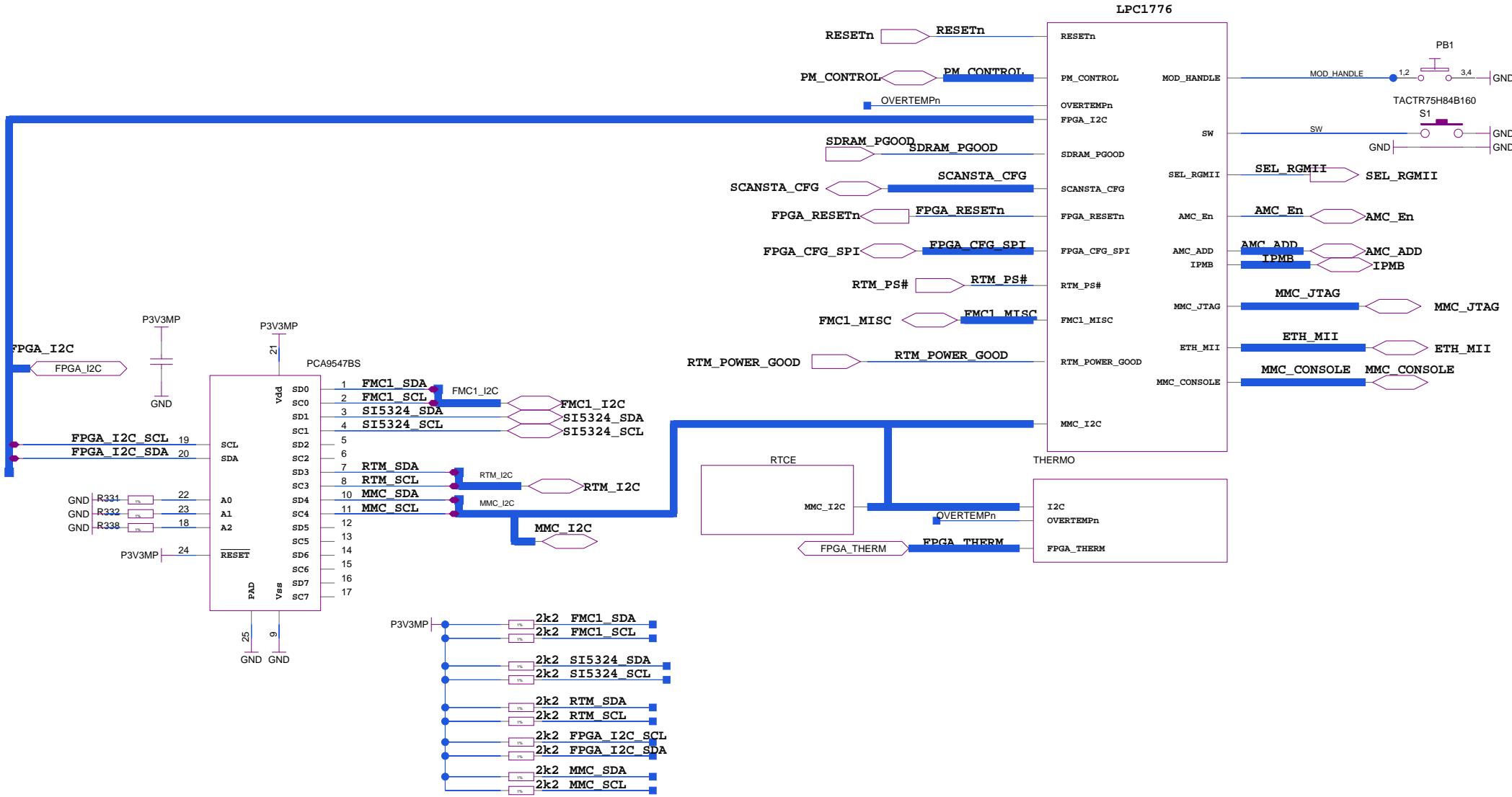
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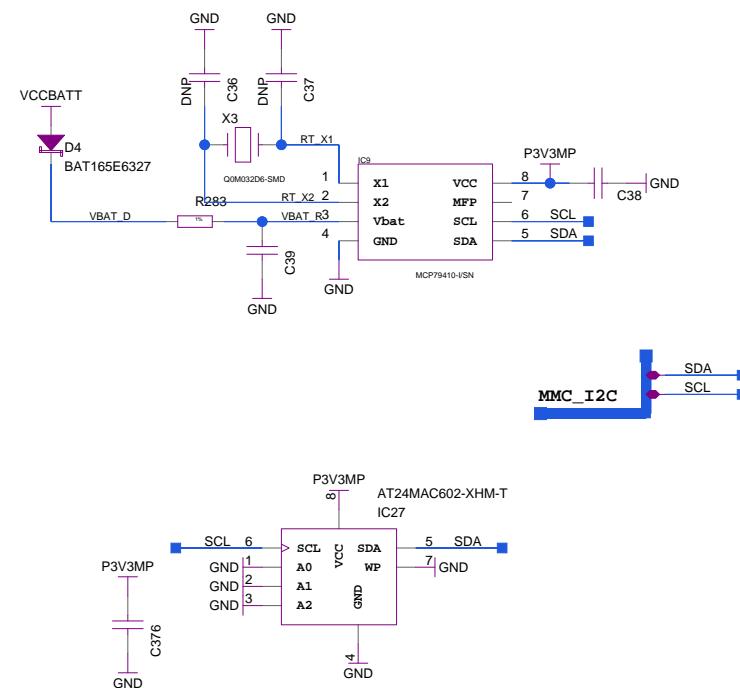
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4

5

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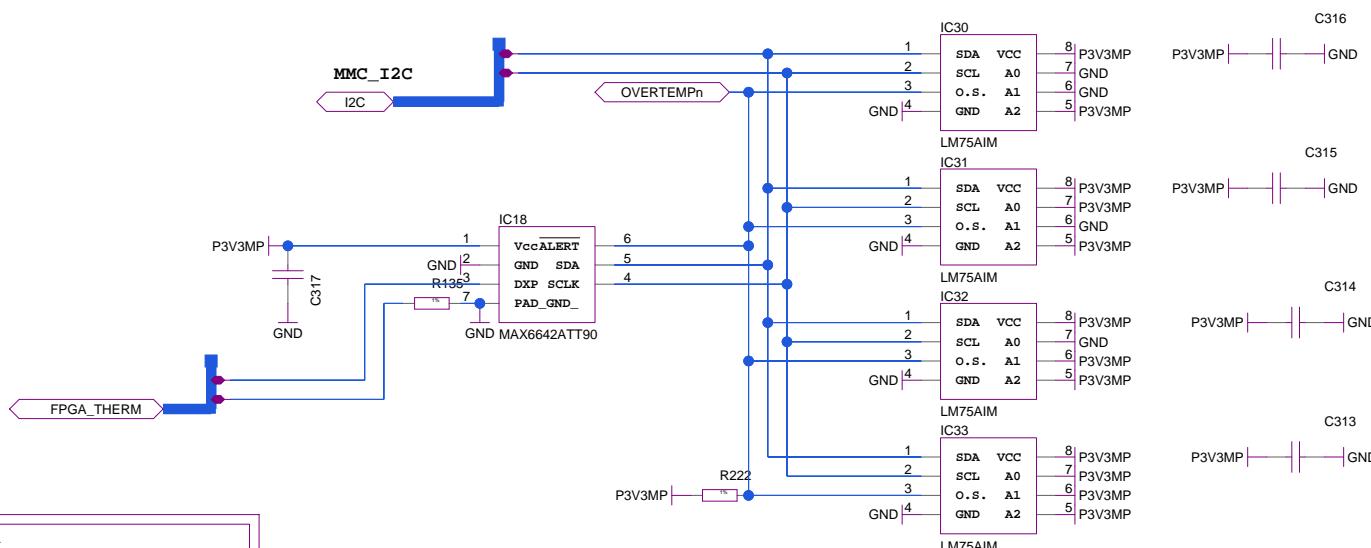




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Size	Number
Date: File:	Sheet _____ of _____ Drawn By:

A**B****C****D**

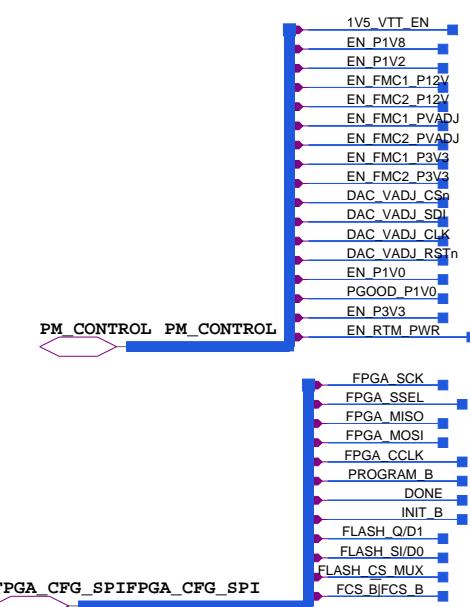
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<http://ohwr.org/CERNOHL>. This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.

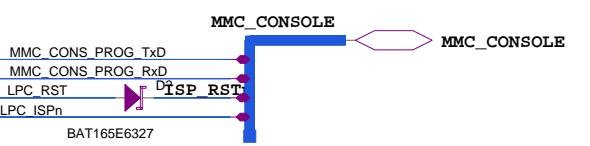
Please see the CERN OHL v.1.1 for applicable conditions.

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		Drawn By:

1



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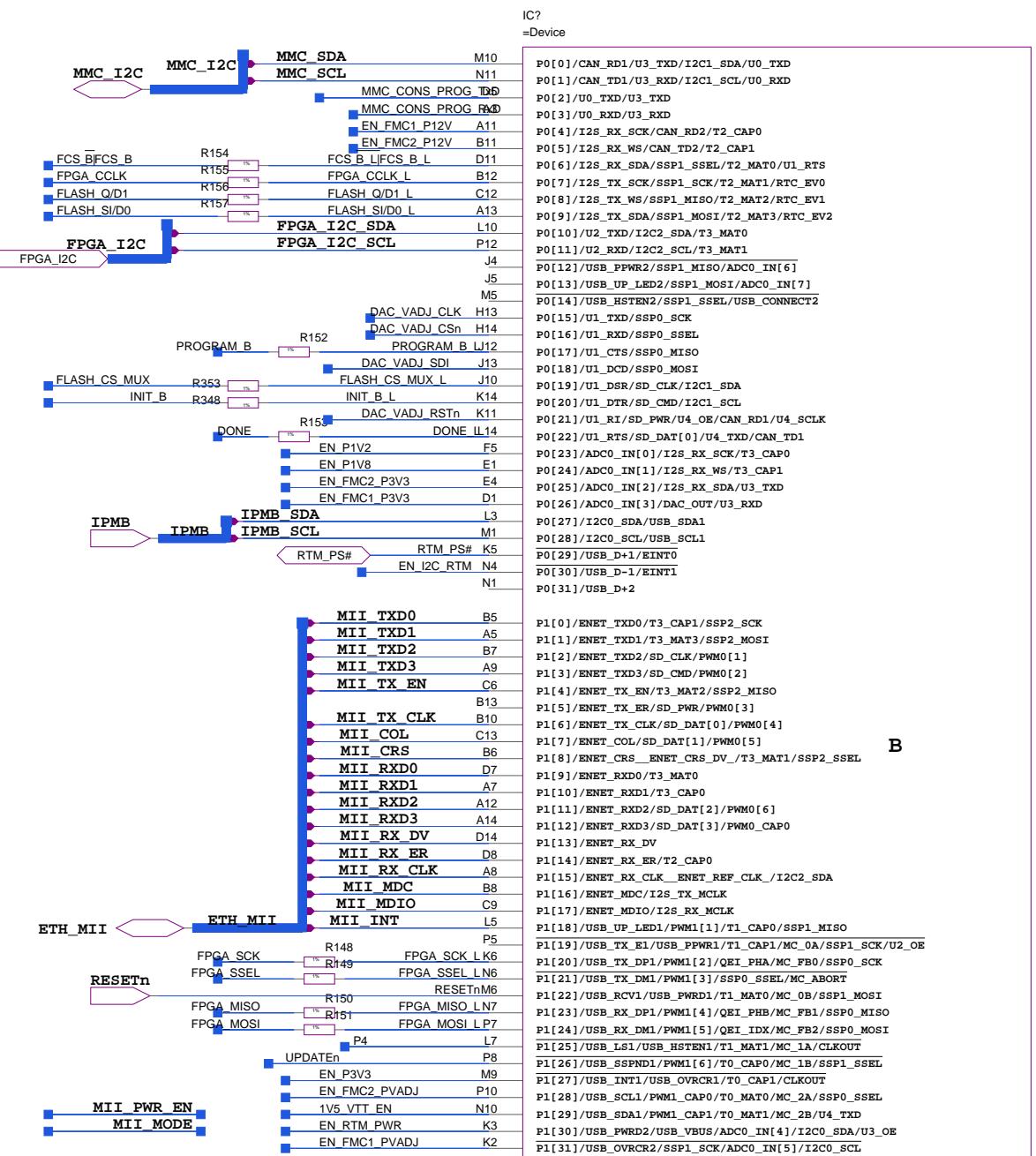


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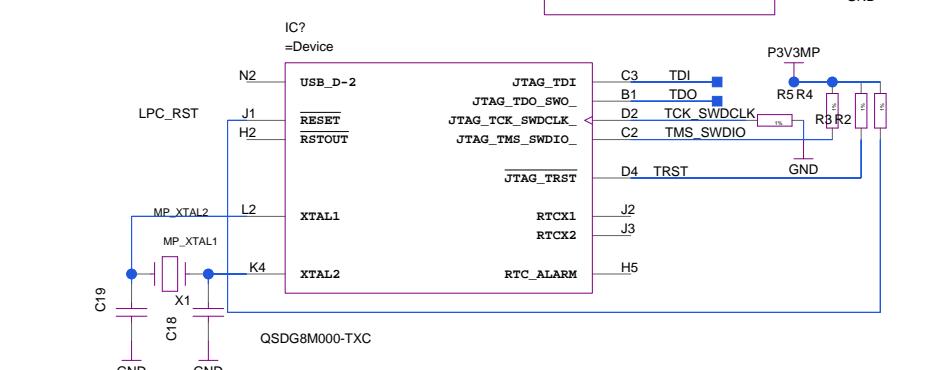
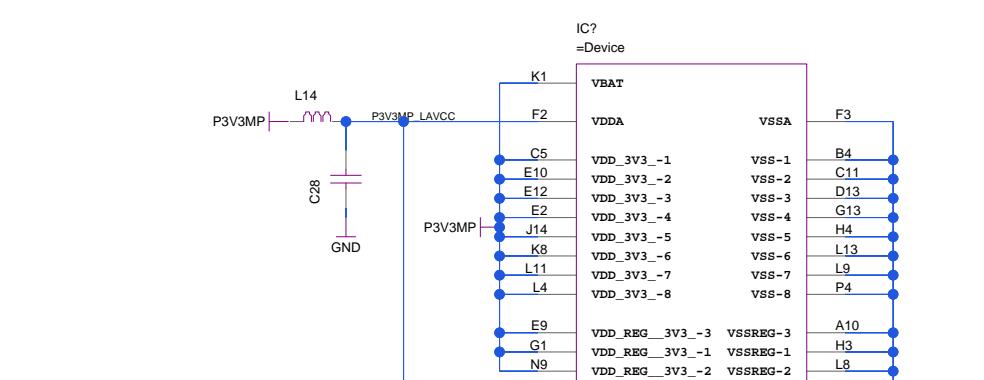
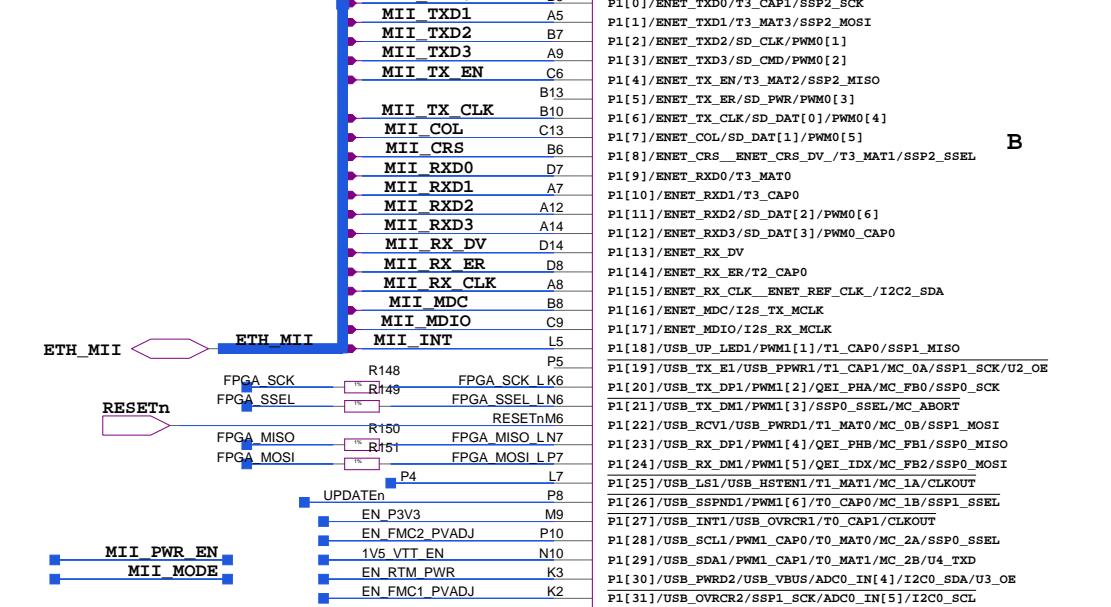
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C

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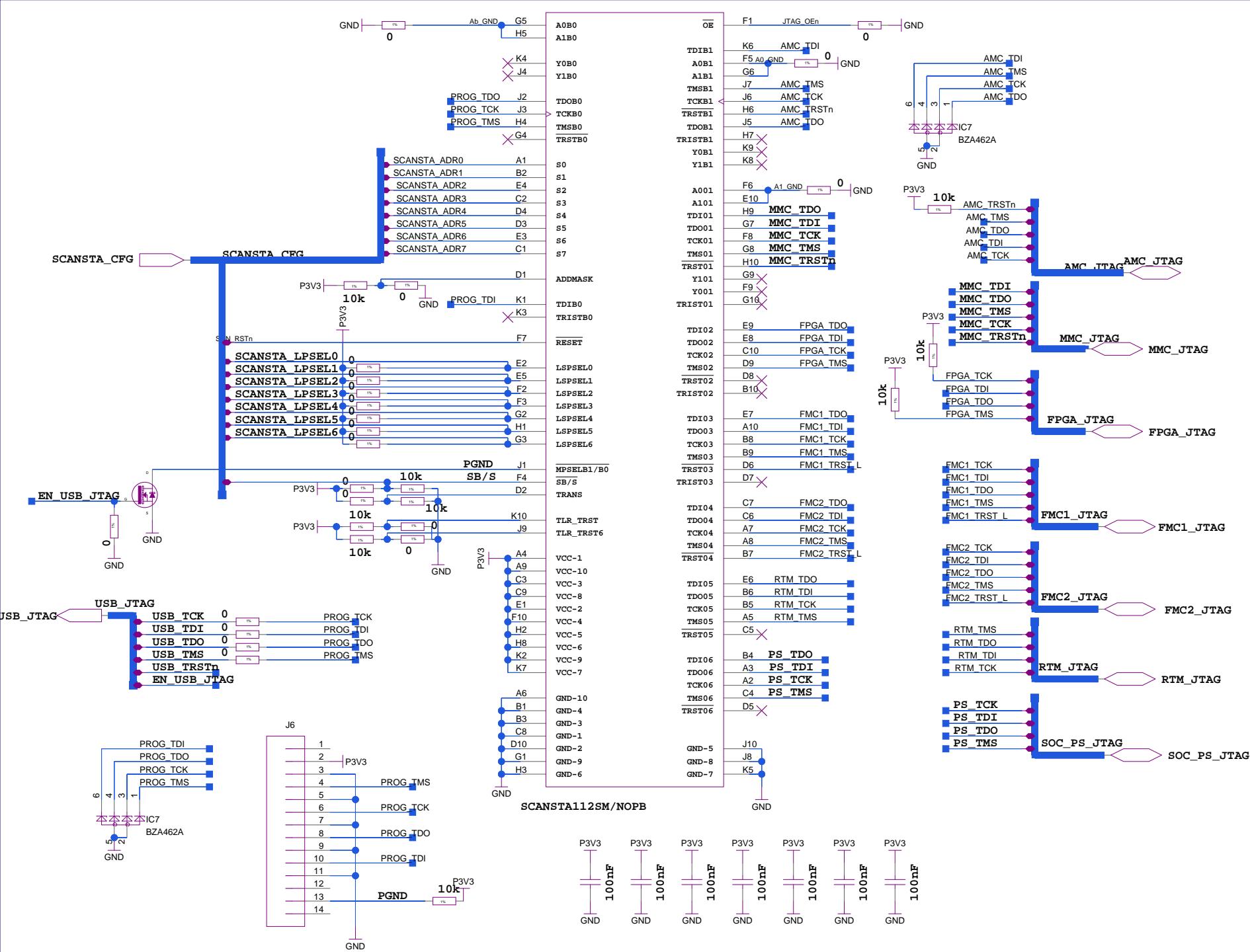


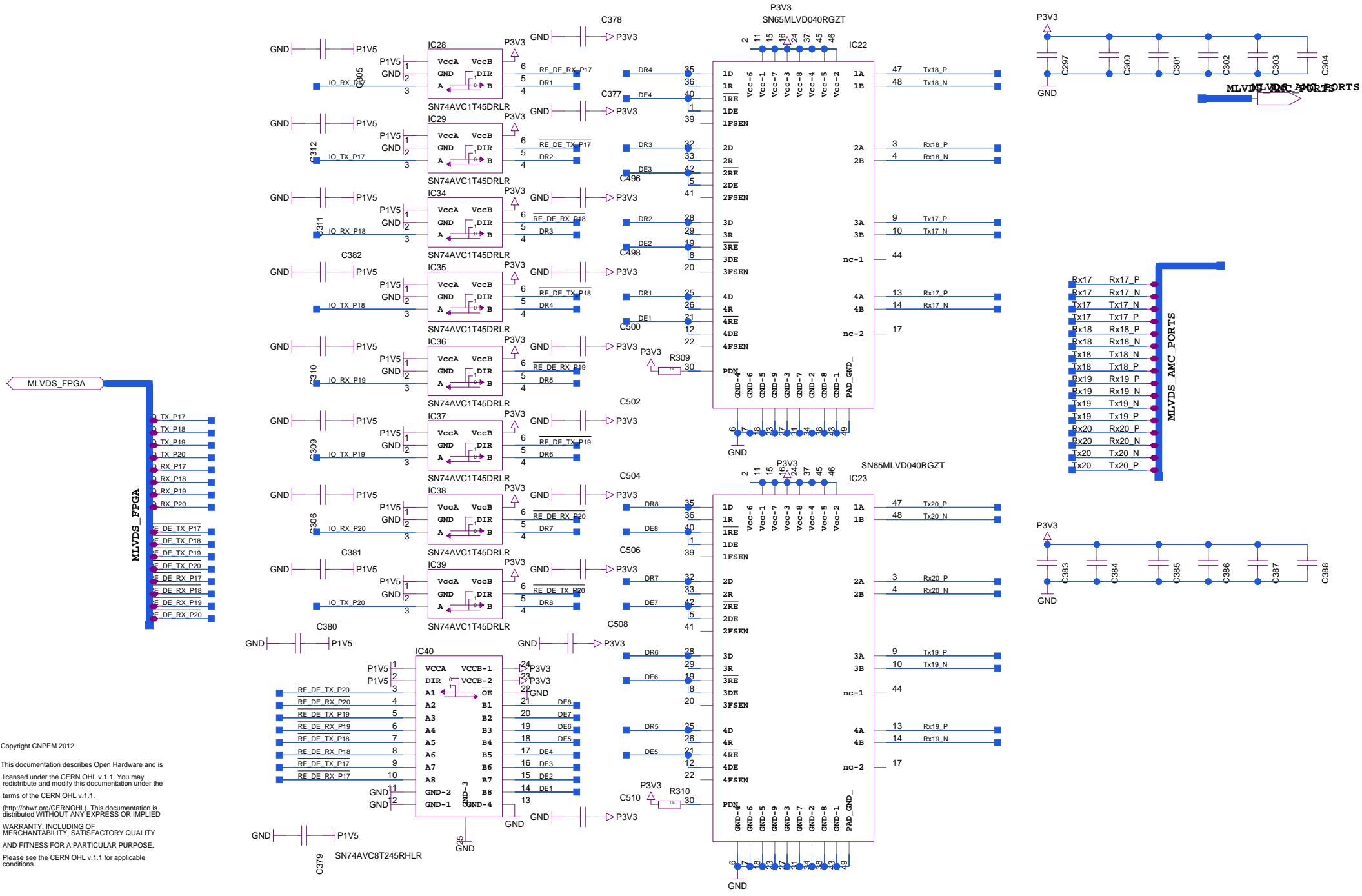
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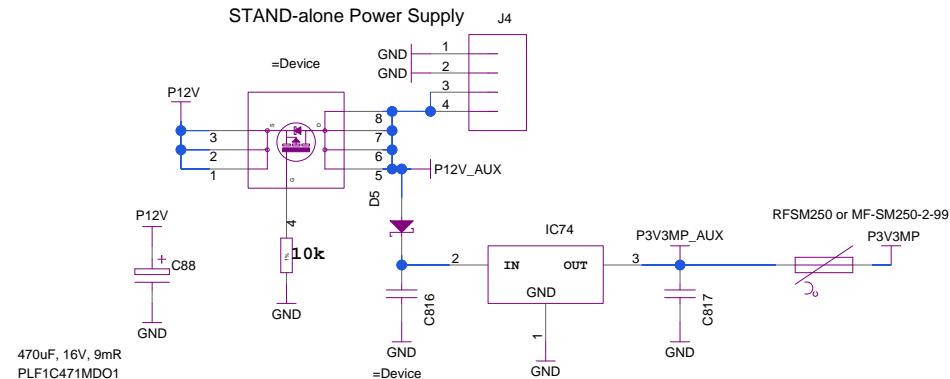
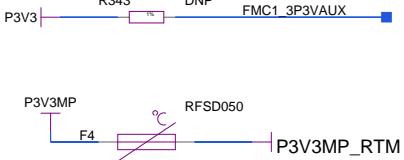
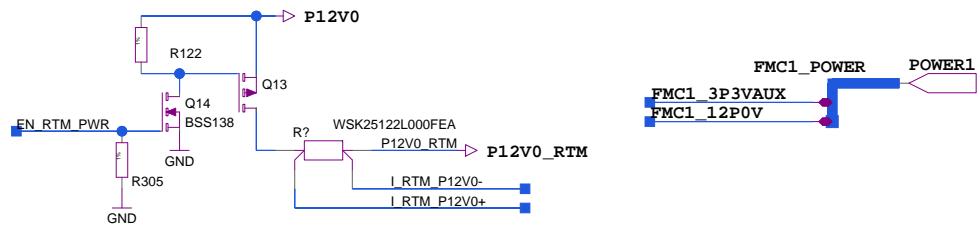
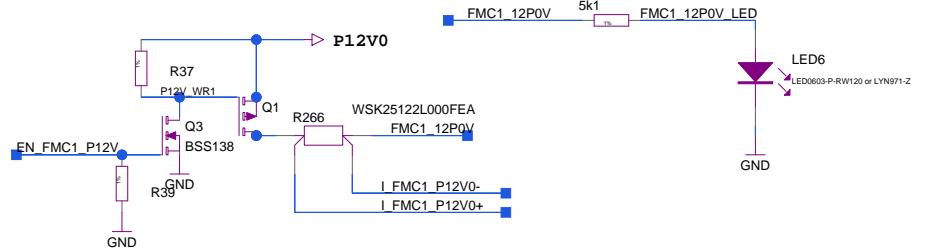


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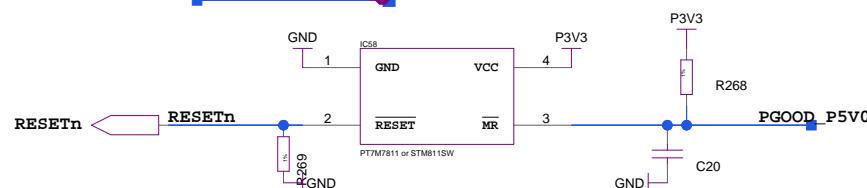
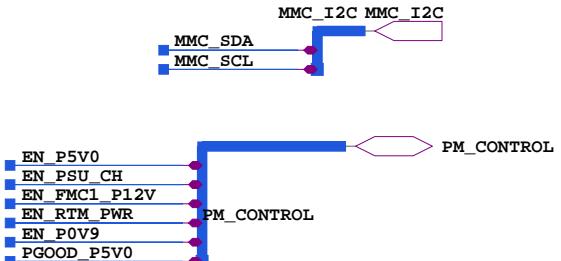
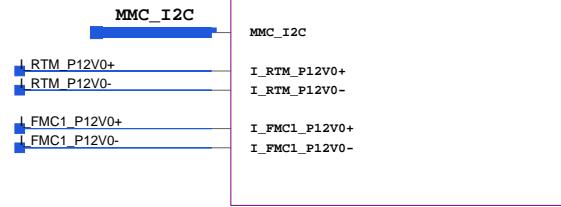
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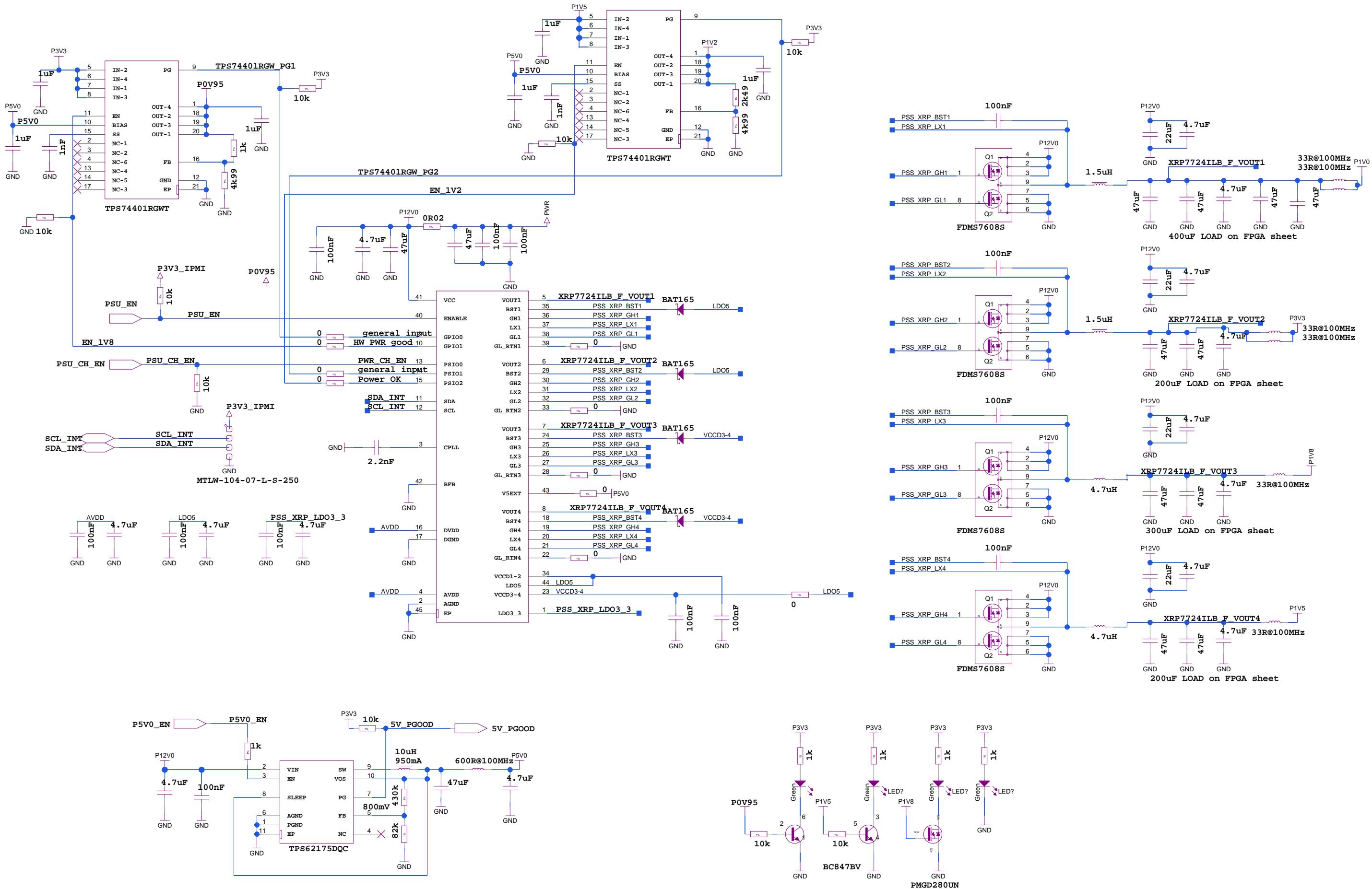


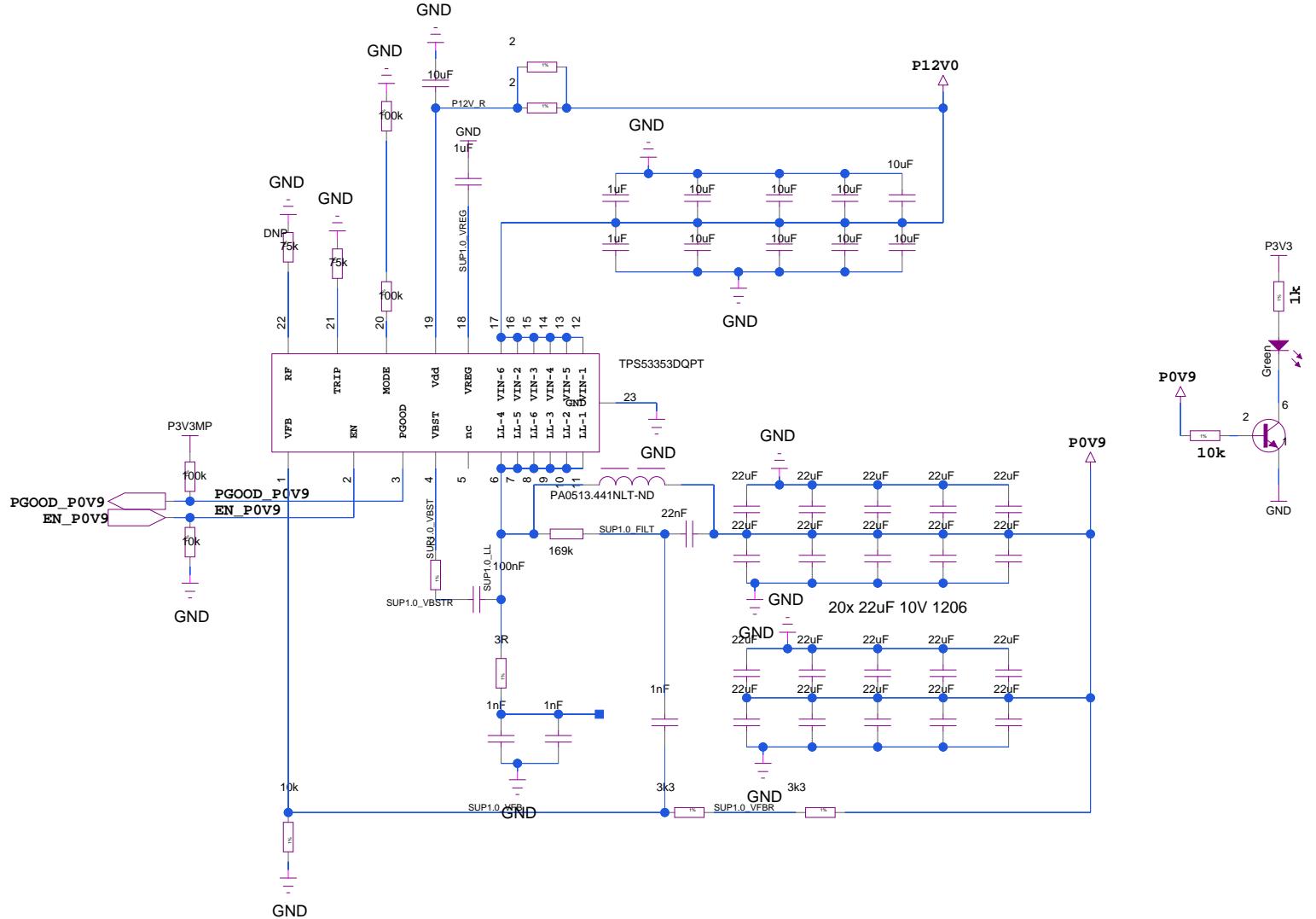
UI
UI_mon.SchDoc

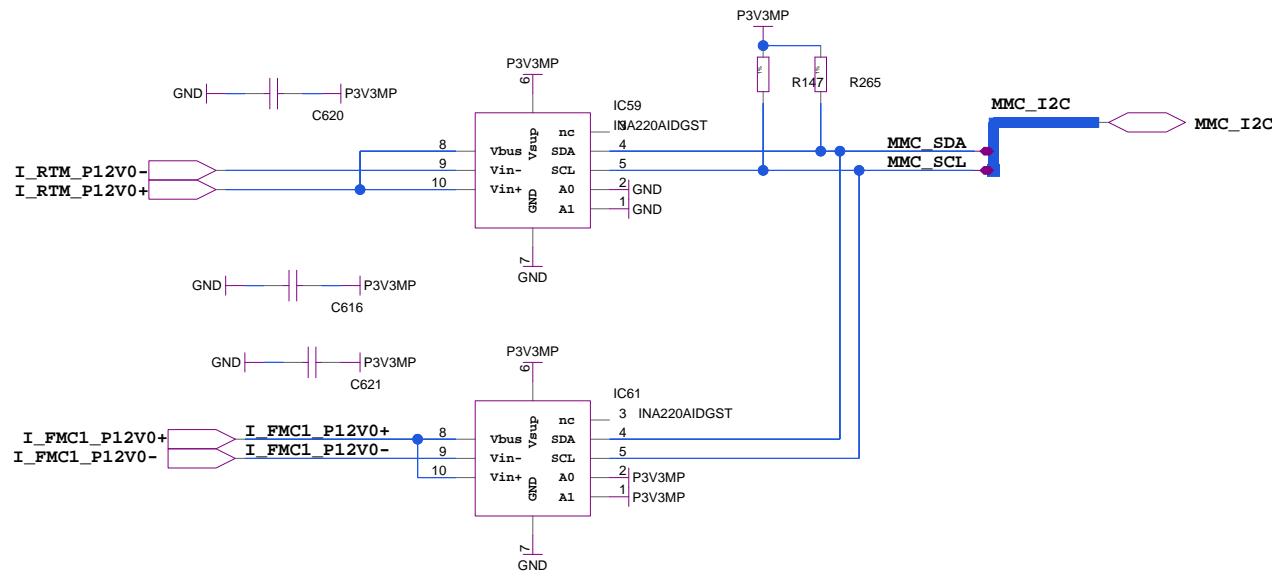


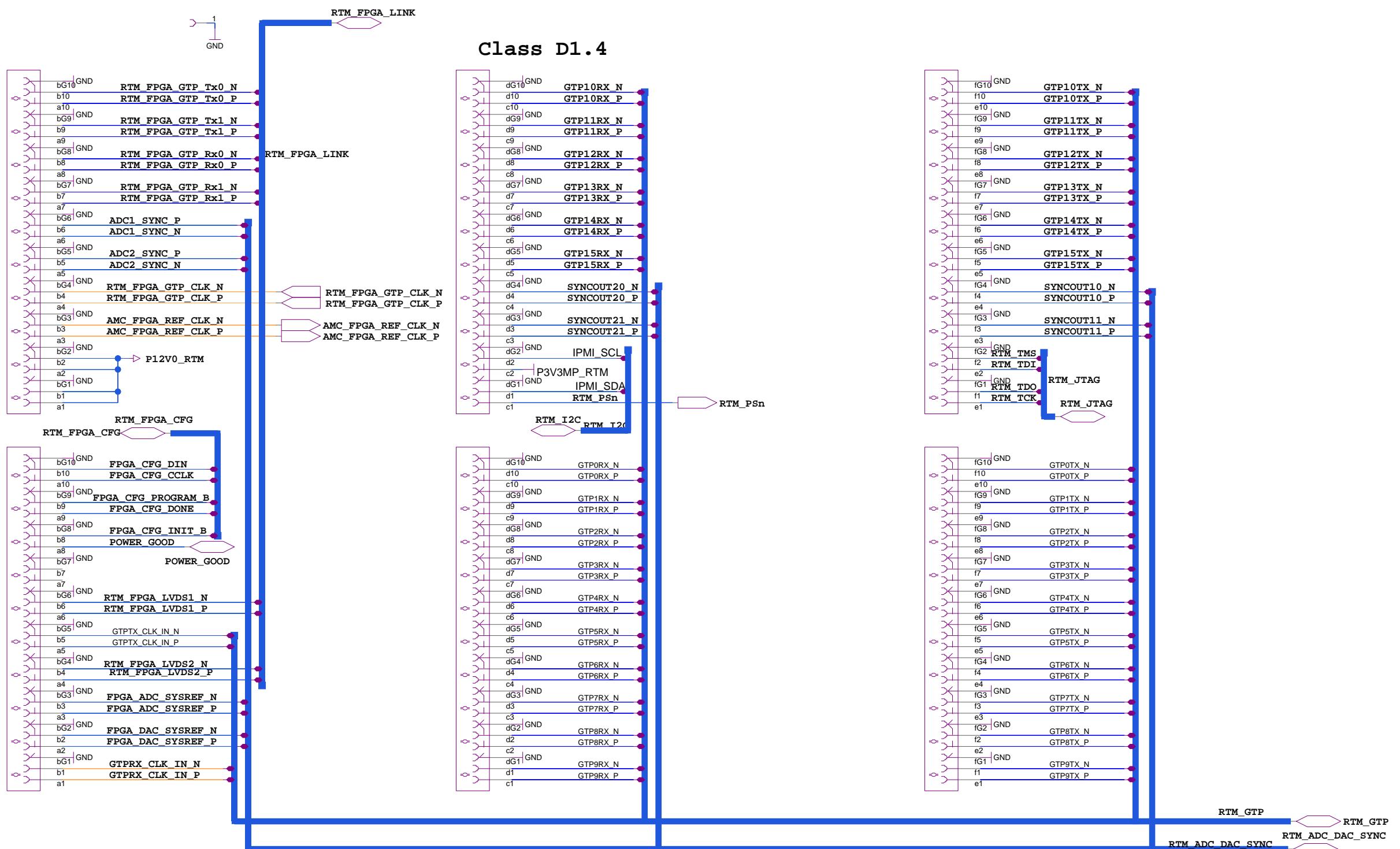
Power requirements

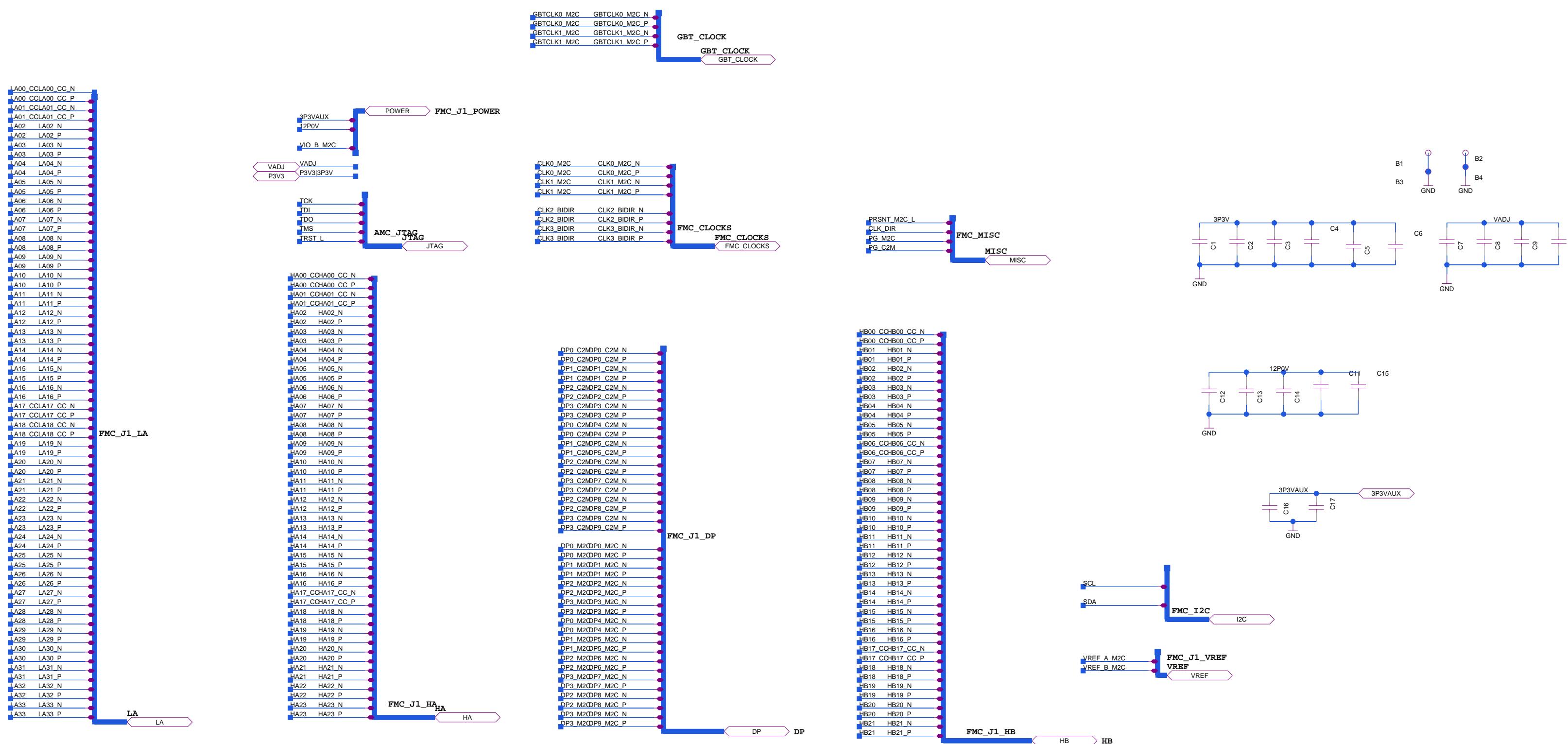
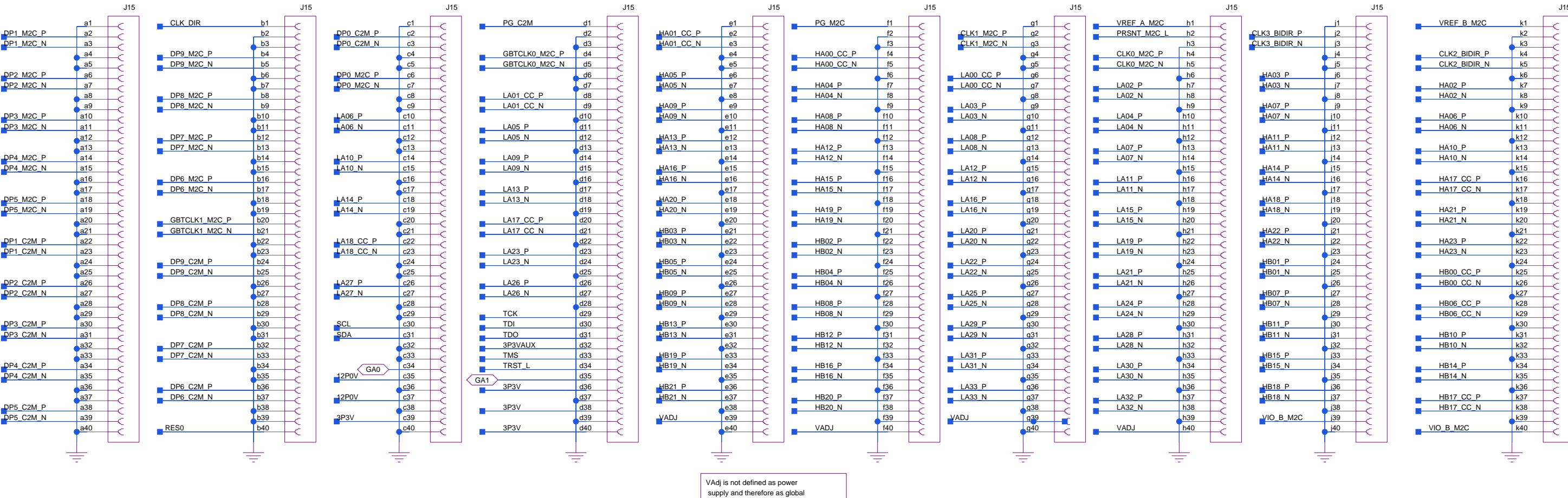
P0V9: 10A
P0V95: 31mA
P1V0: 3A
P1V1: 1A+3.5A=7.5A
P1V2: 0.6A
P1V8: 0.6+0.6+0.3+0.1=1.6A
P3V3: 2A

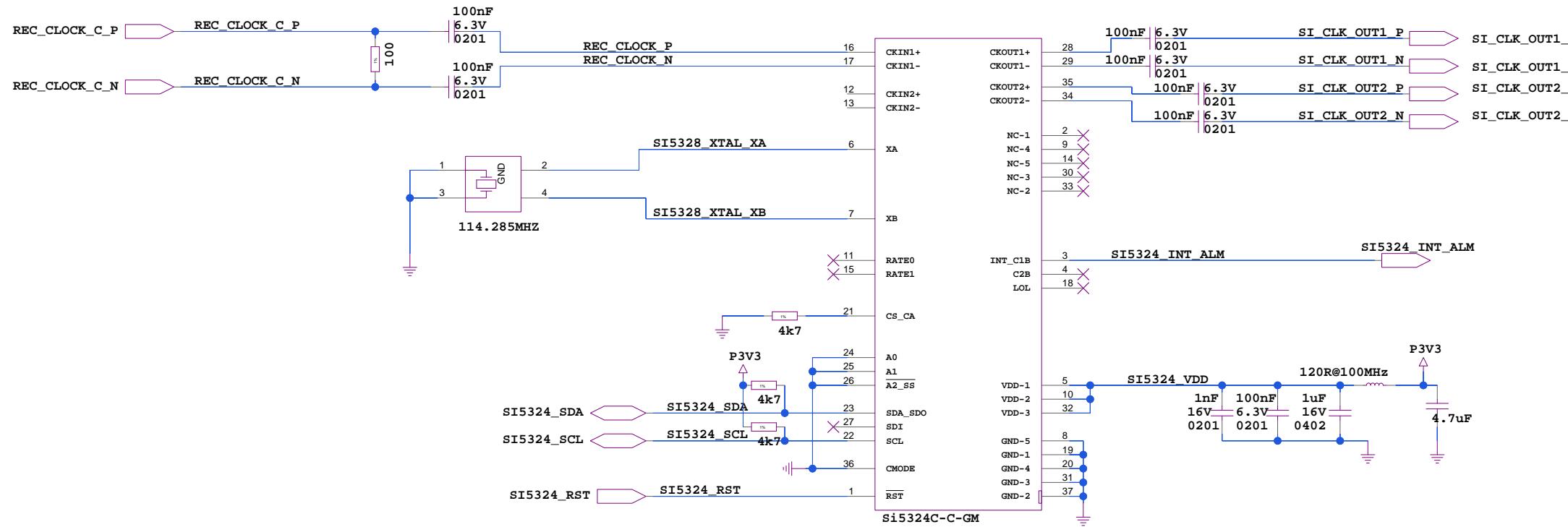


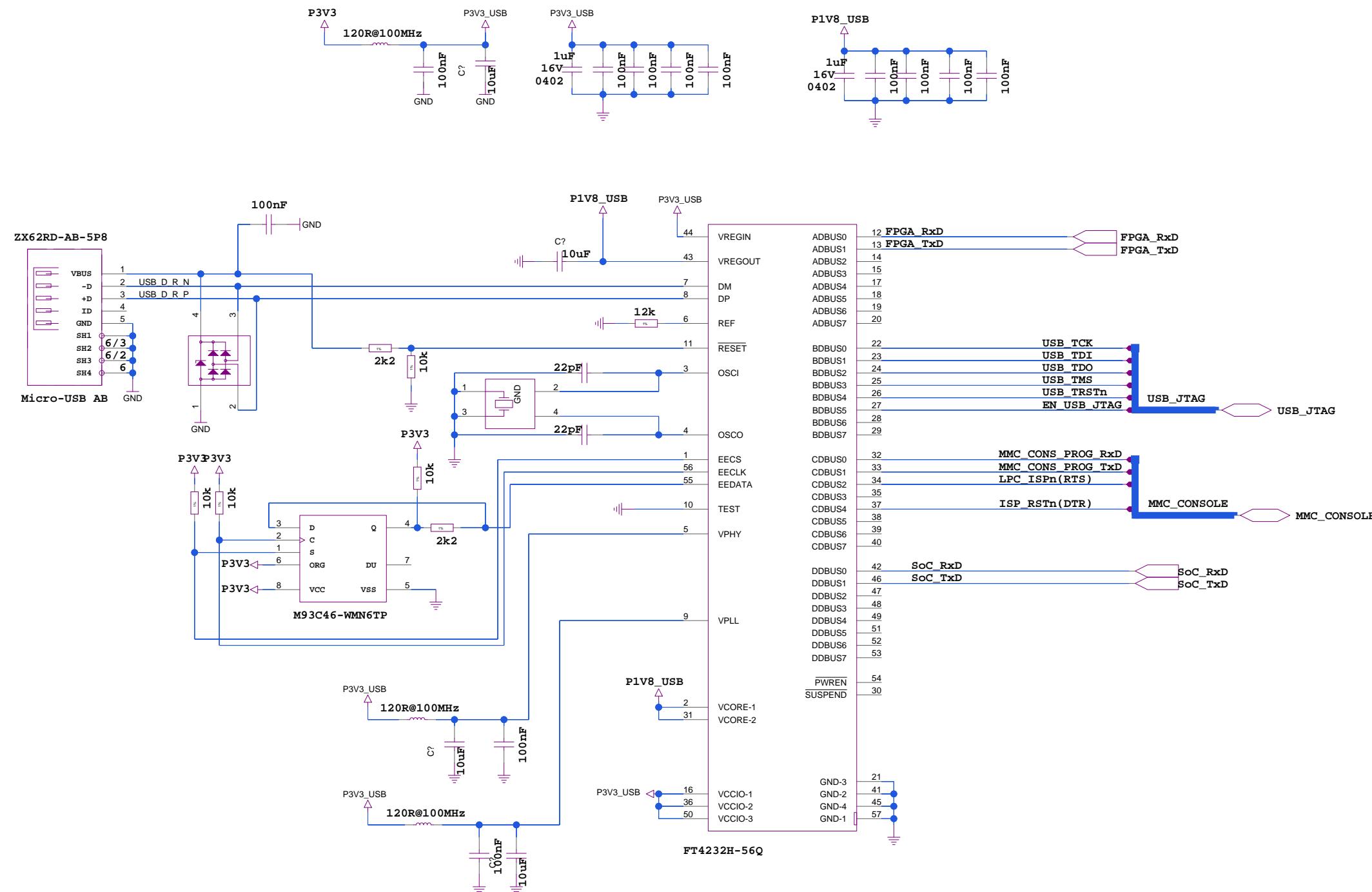






A**B****C**





supply from USB to enable MMC at 3.3V MP