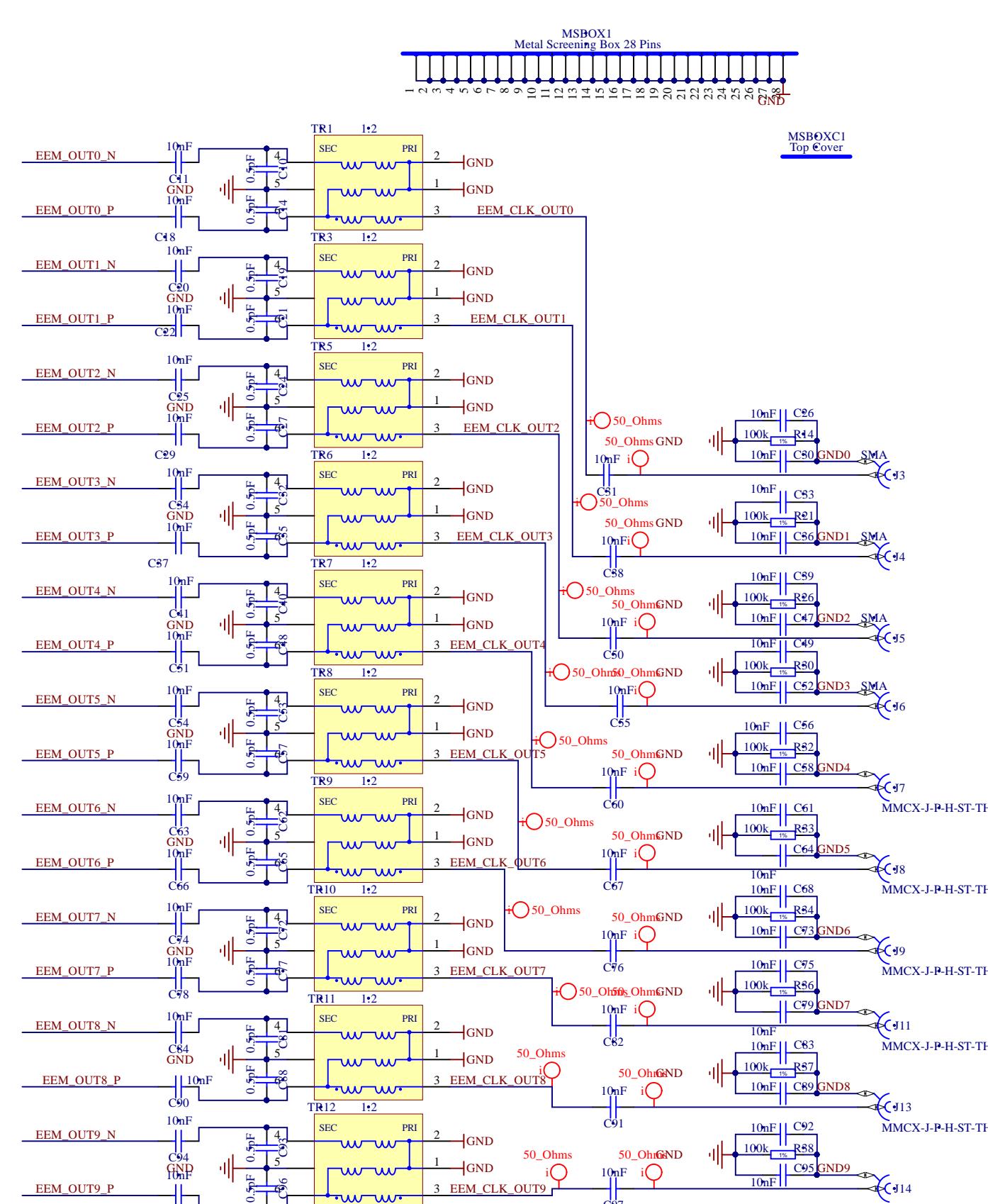
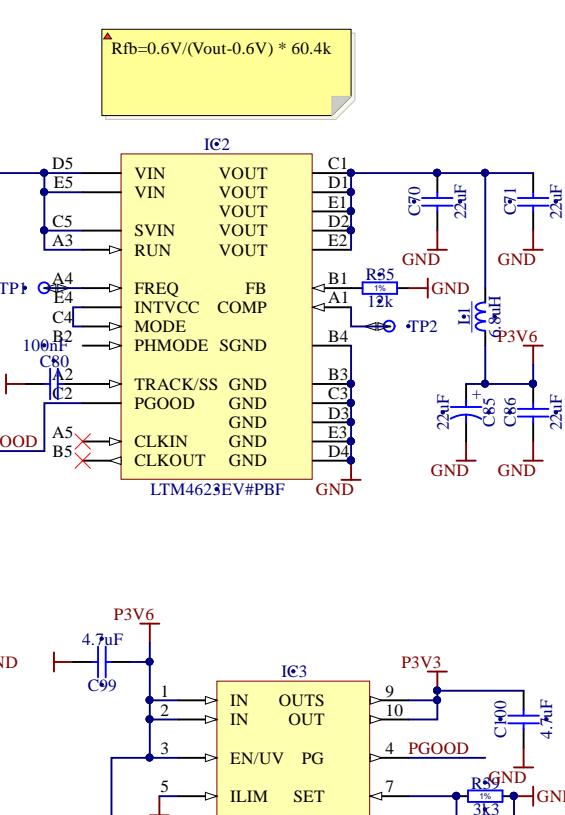
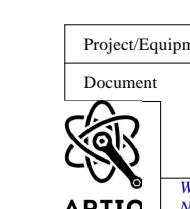


Power budget
ADCLK950 390mA * 3.3V = 0.5W
LDO losses 390mA * 0.3 = 0.117W
LTM4623 losses 0.6W * 0.2 = 0.12W
Total power: 0.73W
12V supply current: 60mA

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B1 GND
B2 GND
B3 GND
B4 GND P3V3
B5 GND P12V0



Project/Equipment ARTIQ EEM

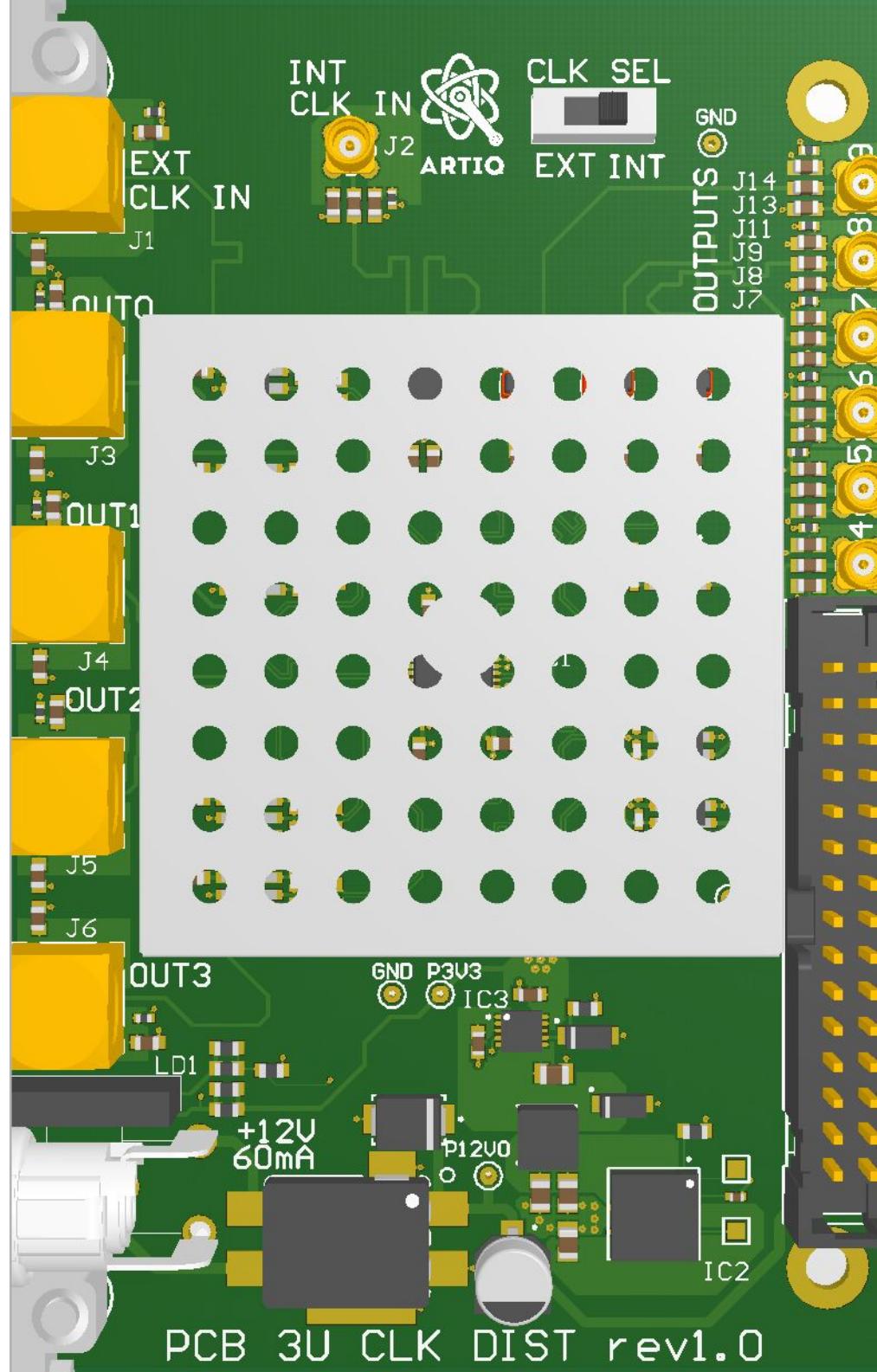
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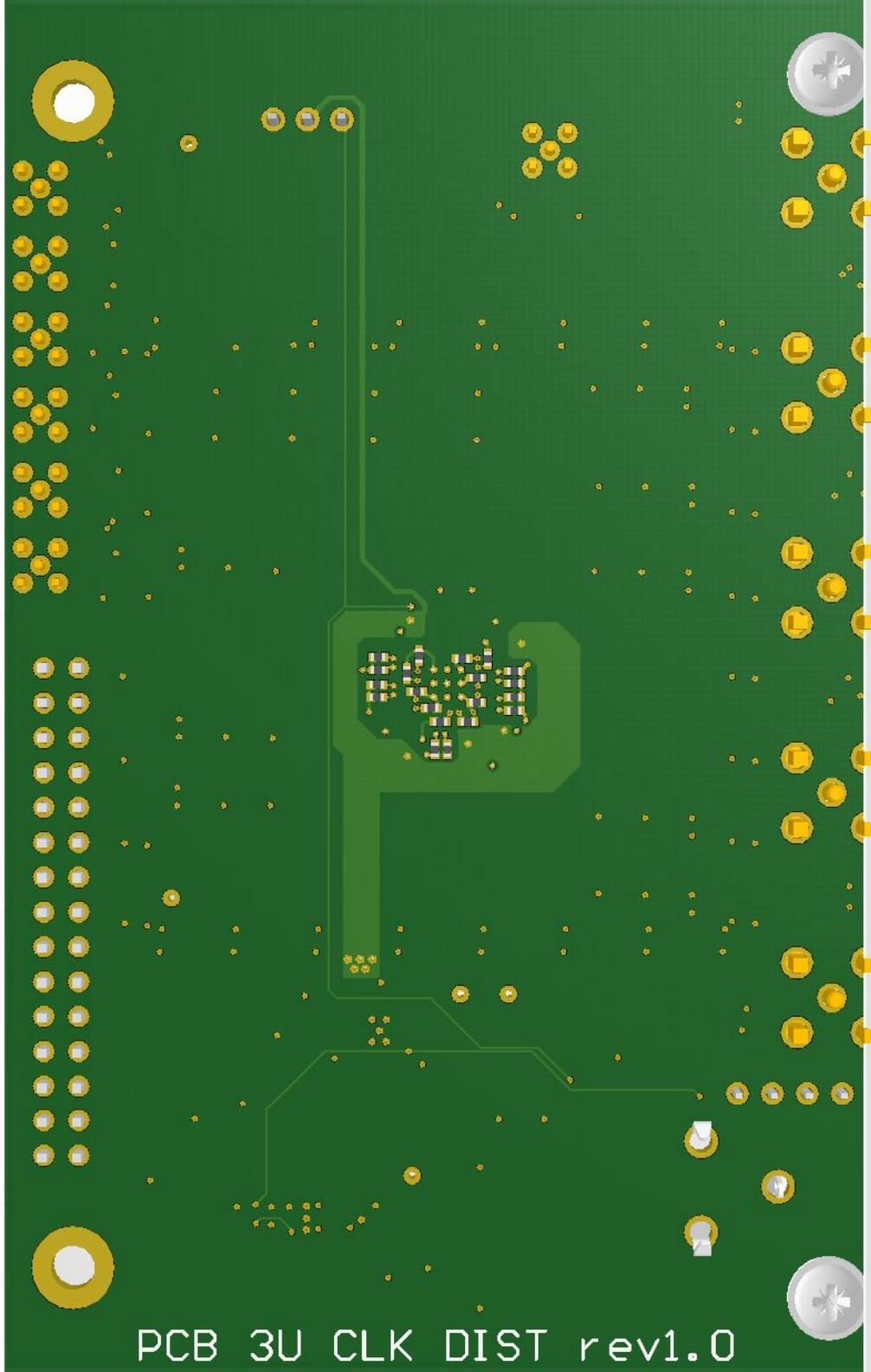
**Low noise
clock buffer**

Warsaw University of Technology ISE
Nowowiejska 15/19

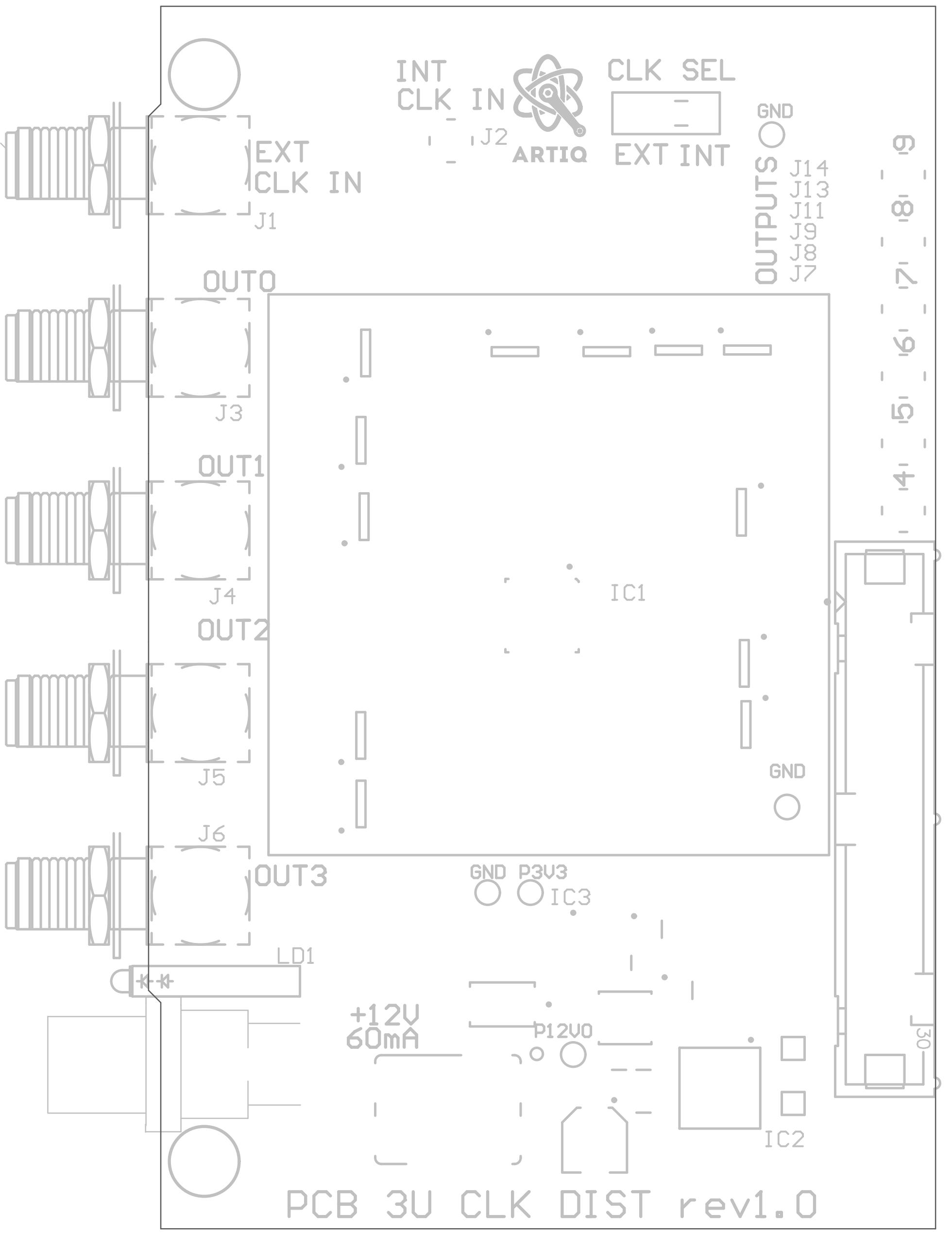
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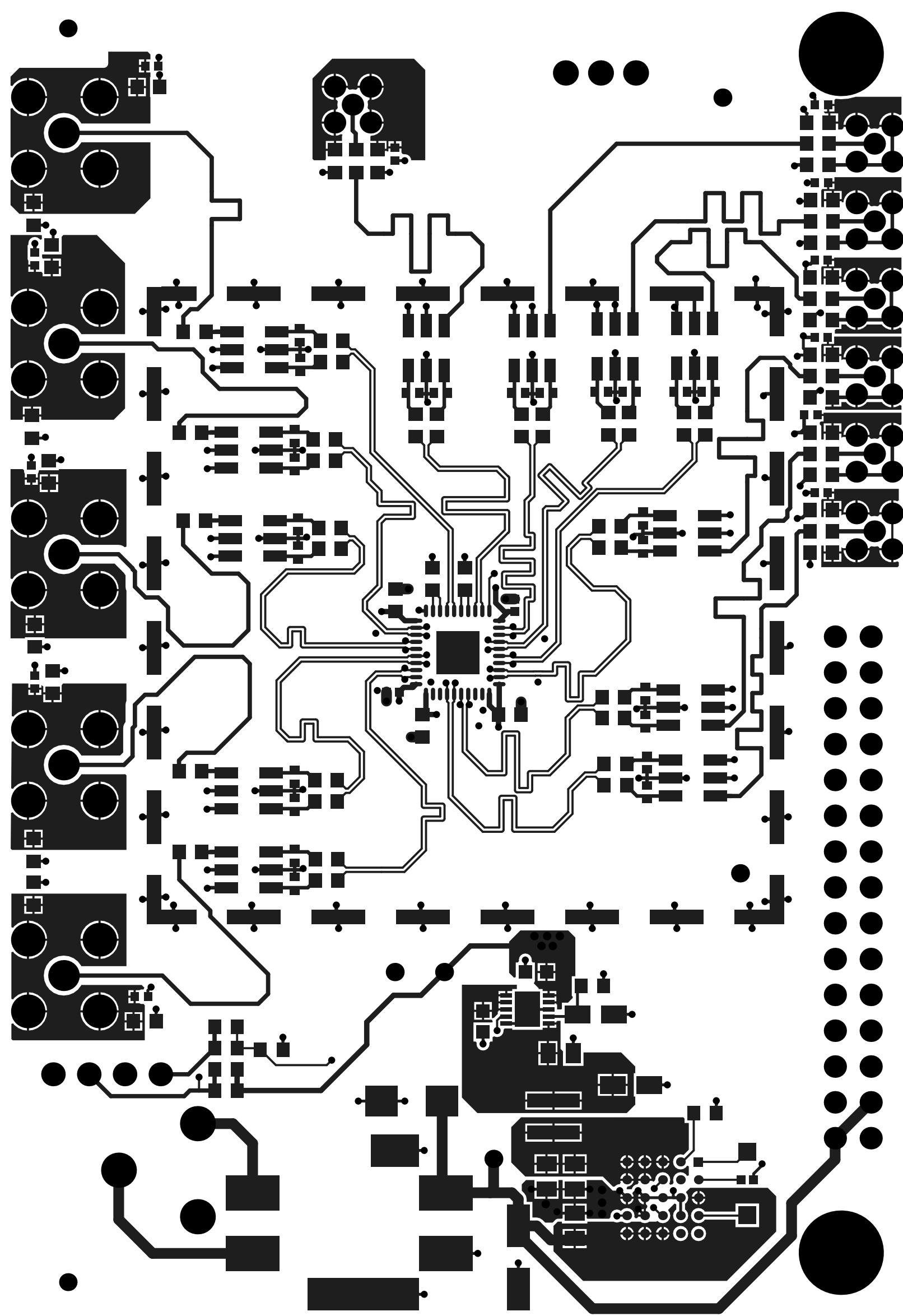
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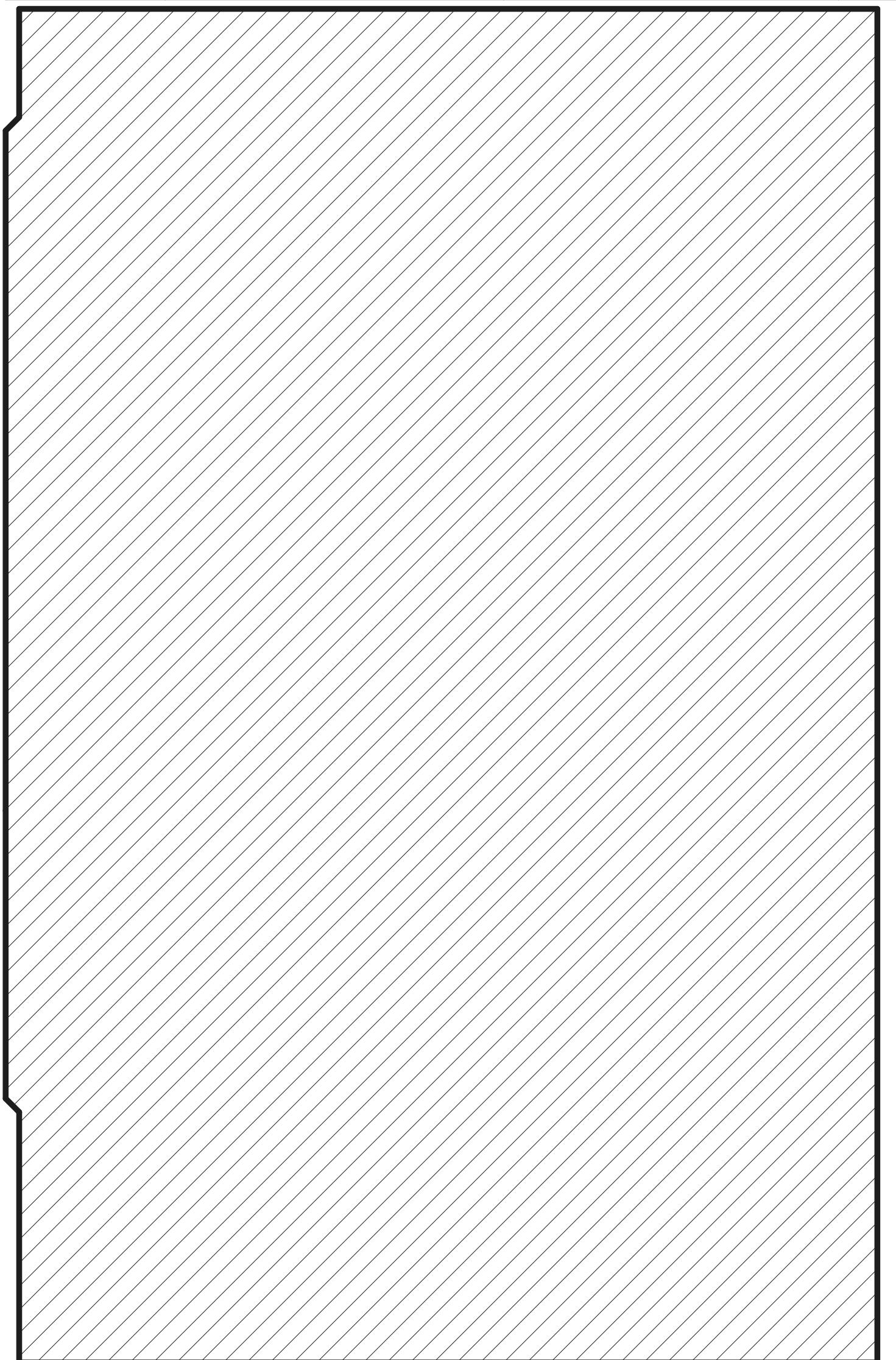


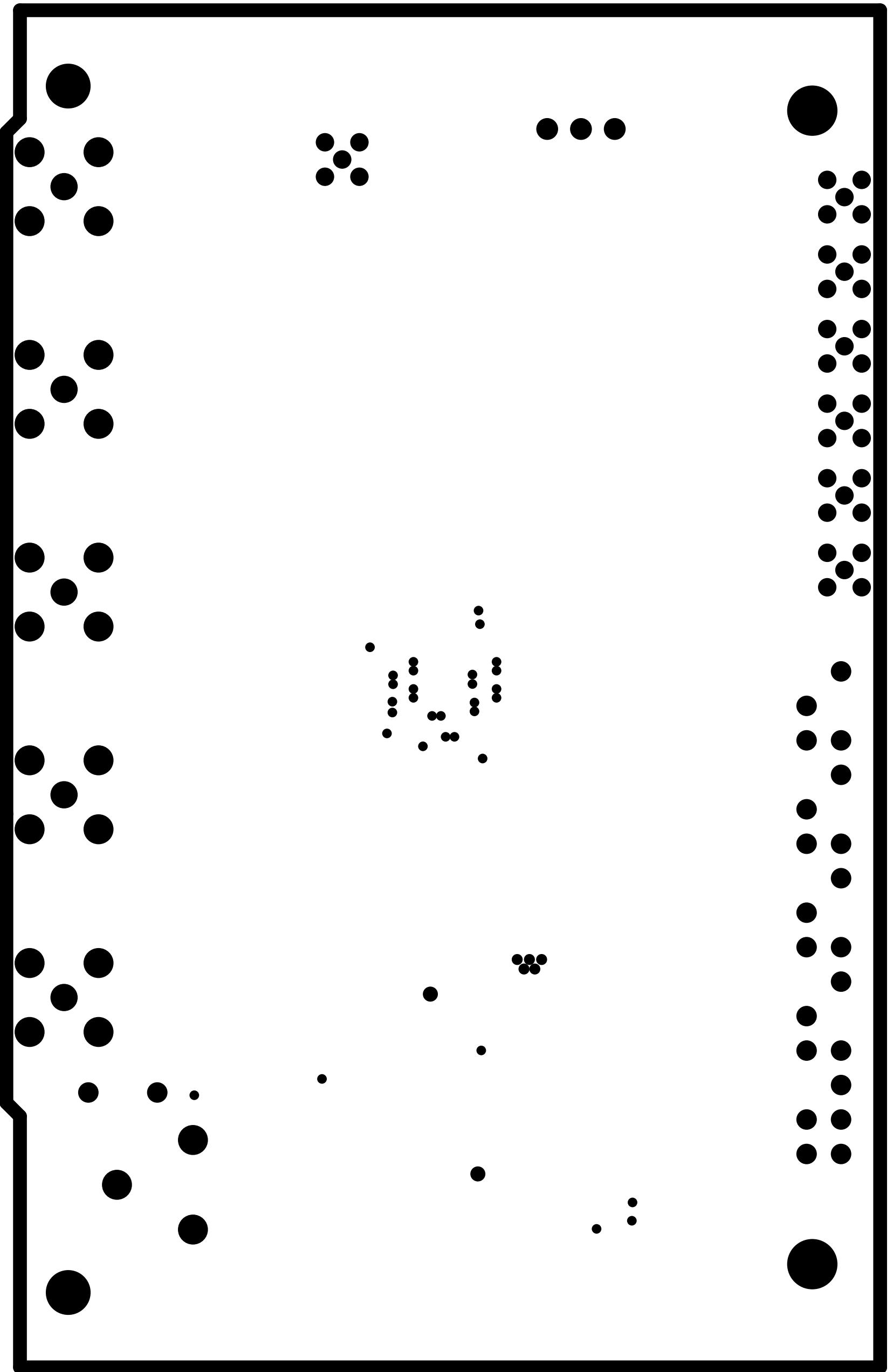
PCB 3U CLK DIST rev1.0

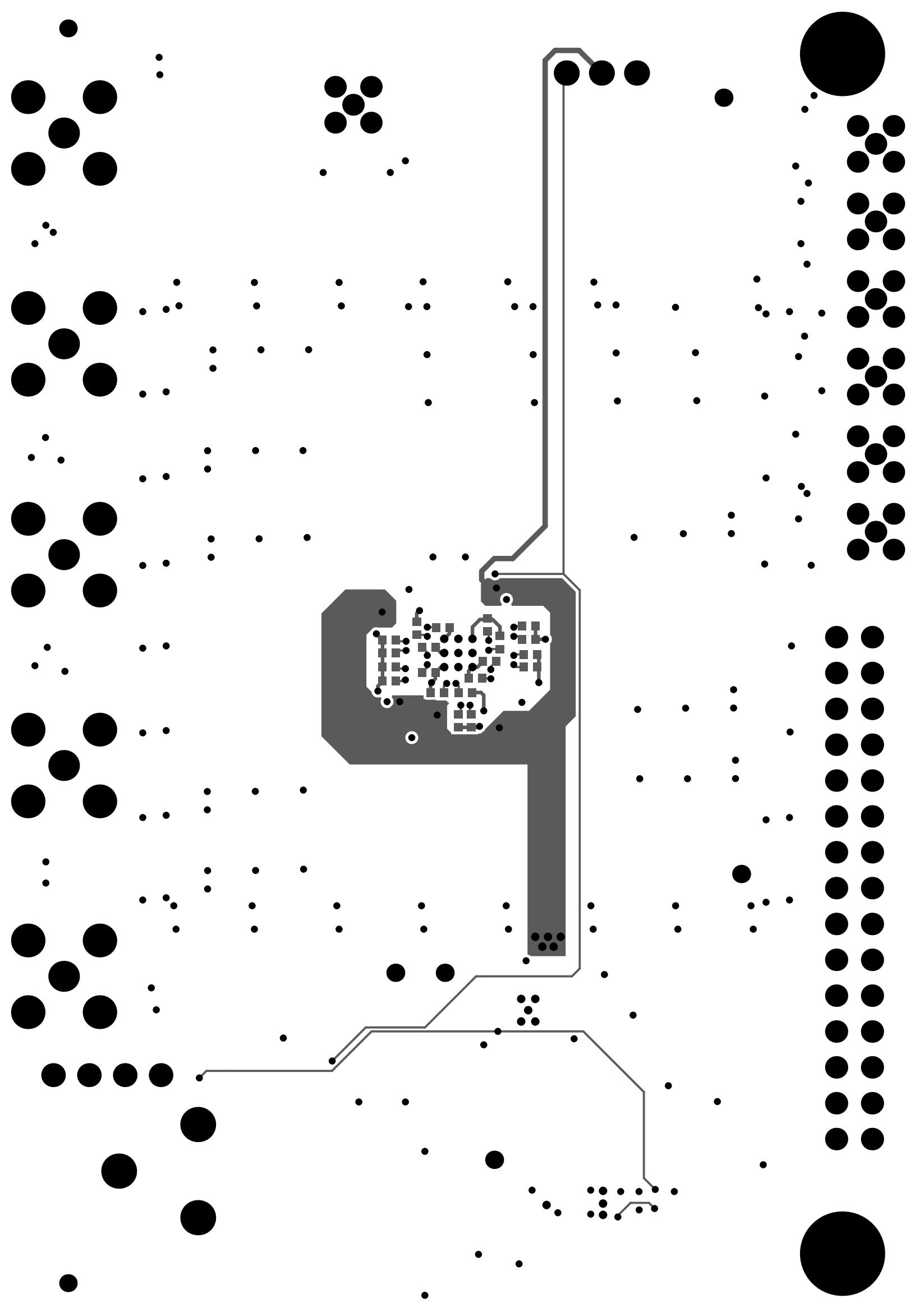


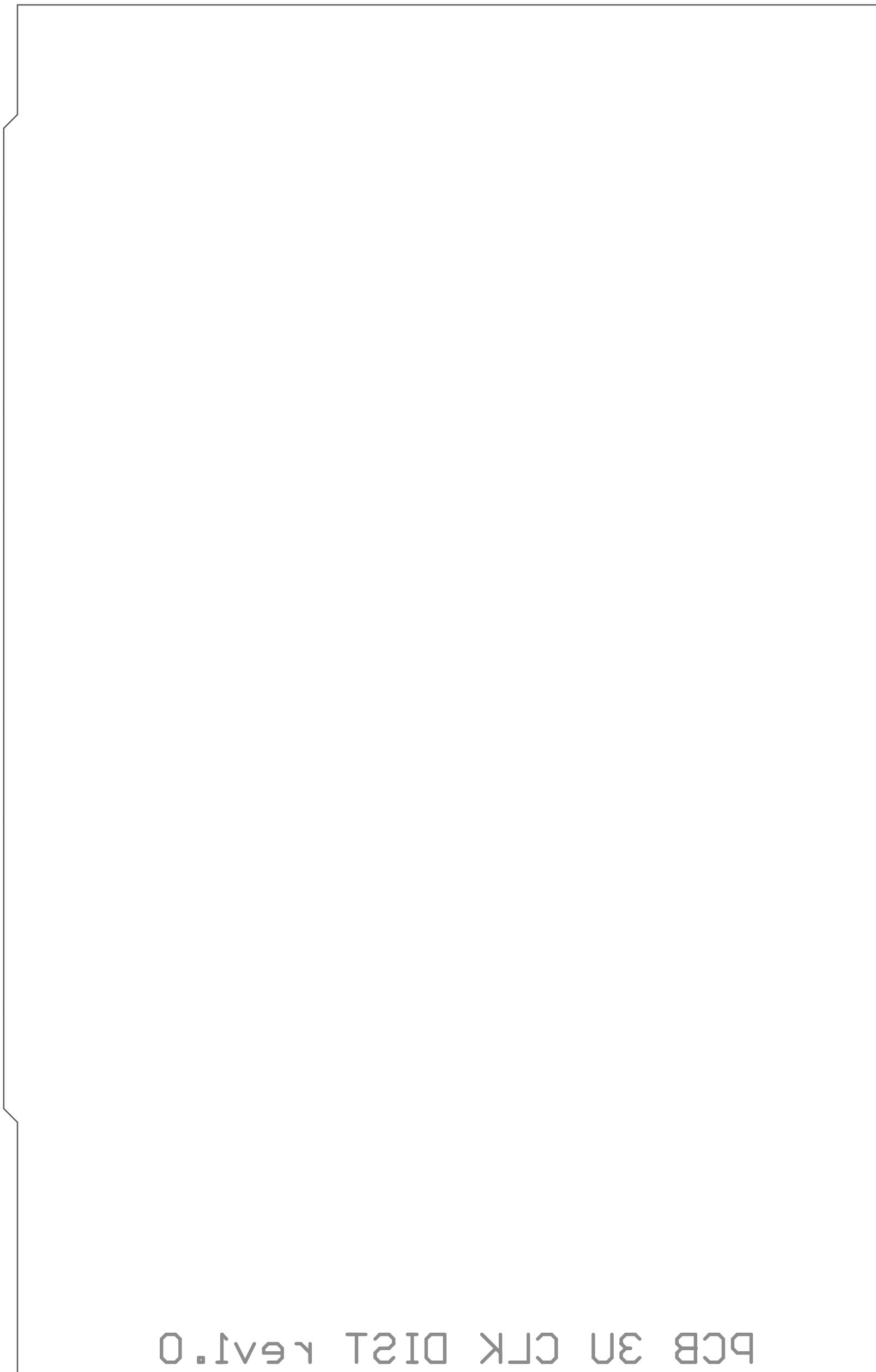


Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	TopOverlay				
2	TopSolder	Solder Resist	0.010mm	3.5	
3	Top	Copper	0.056mm		
4	Dielectric1	FR-4	0.180mm	4.8	
5	MP(G)	Copper	0.036mm		
6	Dielectric 3		1.080mm	4.2	
7	L3	Copper	0.036mm		
8	Dielectric 4		0.180mm	4.2	
9	Bot	Copper	0.056mm		
10	BottomSolder	Solder Resist	0.010mm	3.5	
11	BottomOverlay				









PCB 3U CLK DISI Rev1.0