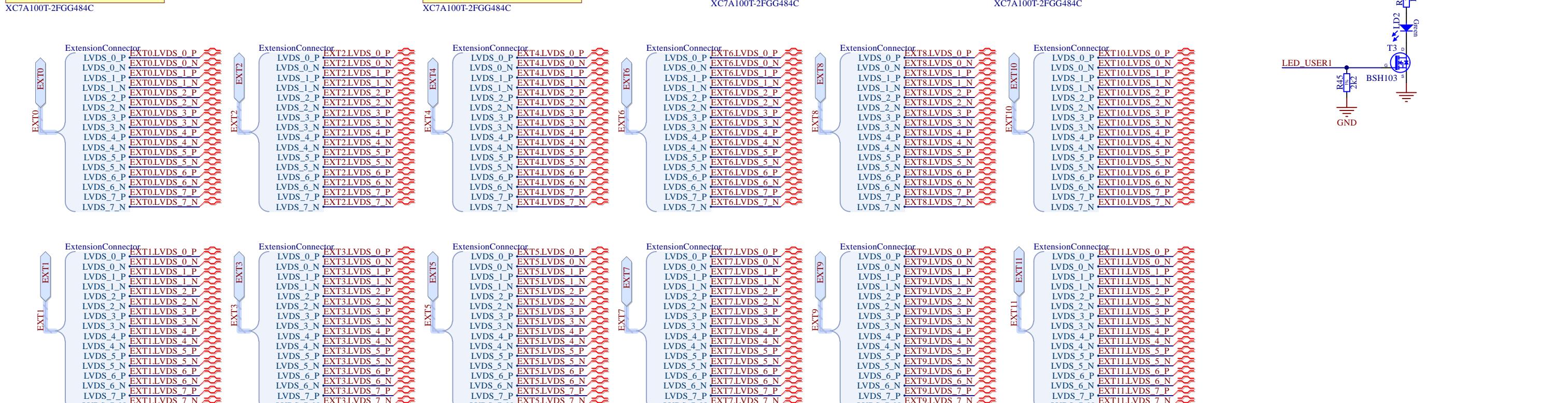
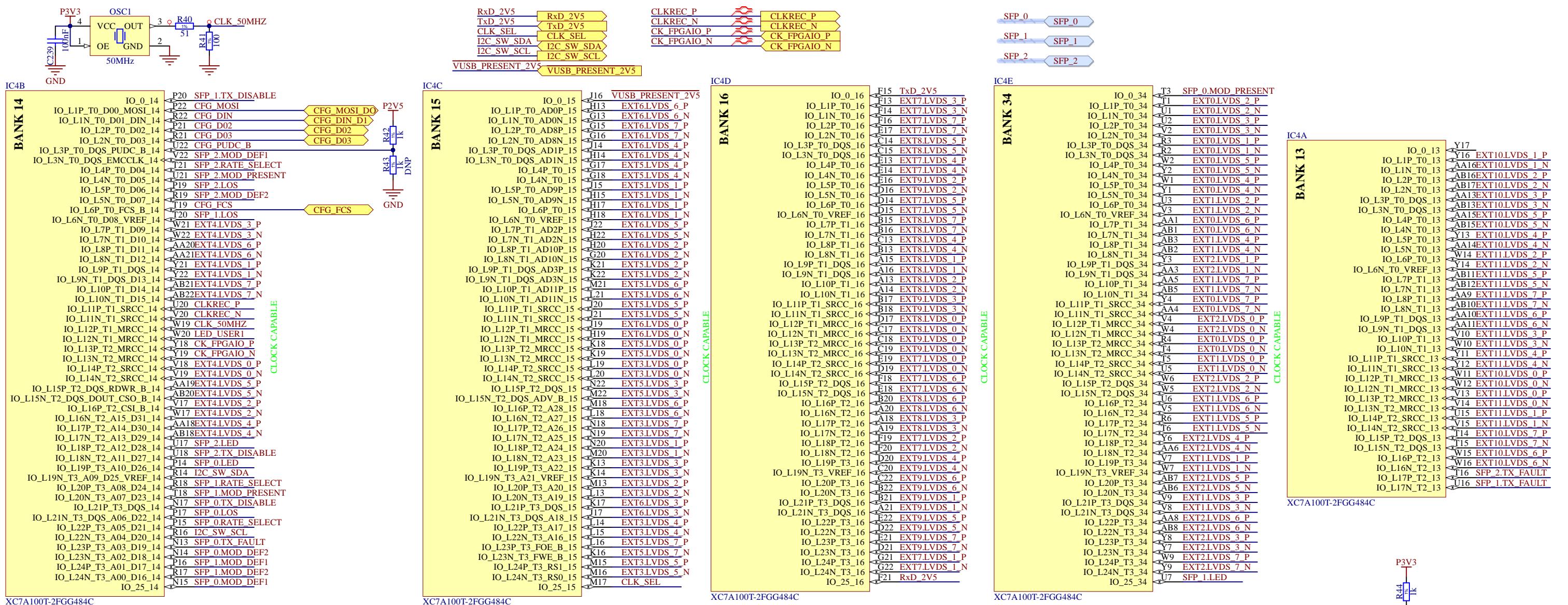


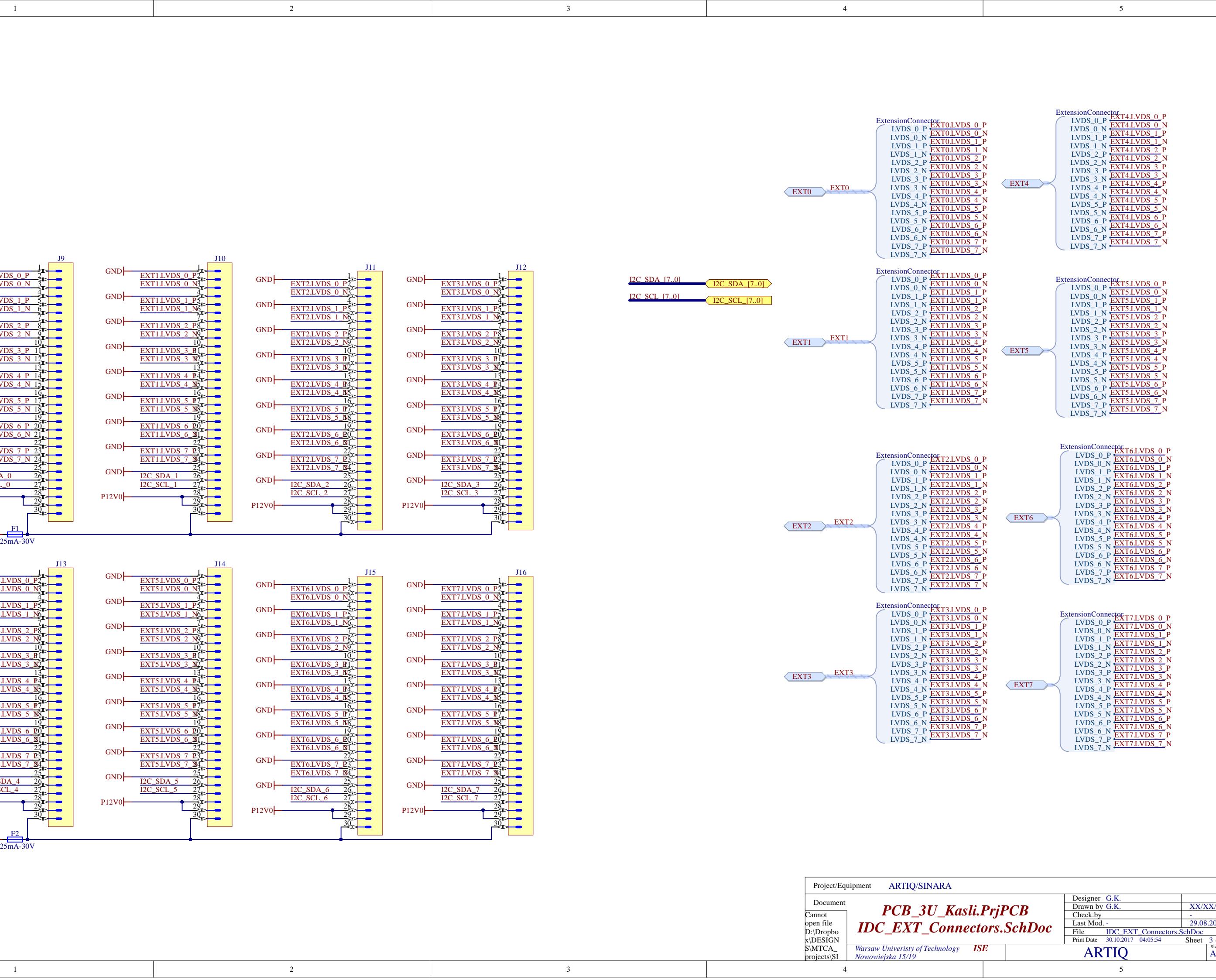
Project/Equipment		ARTIQ/SINARA	
Document		Designer G.K.	
Cannot open file D:\Dropbox\DESIGN\SMTCA_projects\SI		Drawn by G.K.	XX/XX/XXXX
		Check by	
		Last Mod. -	21.10.2017
		File TOP.SchDoc	
		Print Date 30.10.2017 04:05:52	
		Sheet 1 of 12	
PCB_3U_Kasli.PrjPCB TOP.SchDoc		Warsaw University of Technology ISE	
Nowowiejska 15/19		ARTIQ	



Project/Equipment		ARTIQ/SINARA	
Document		Designer	G.K.
Cannot open file		Draw by	G.K.
D:\Dropbox\DESIGN		Check by	XX/XX/XXXX
S\MTCA_projects\SI		Last Mod.	-
		File	FPGA.schdoc
		Print Date	30.10.2017 04:05:53
		Sheet	2 of 12
		Size	A3
		Rev	-

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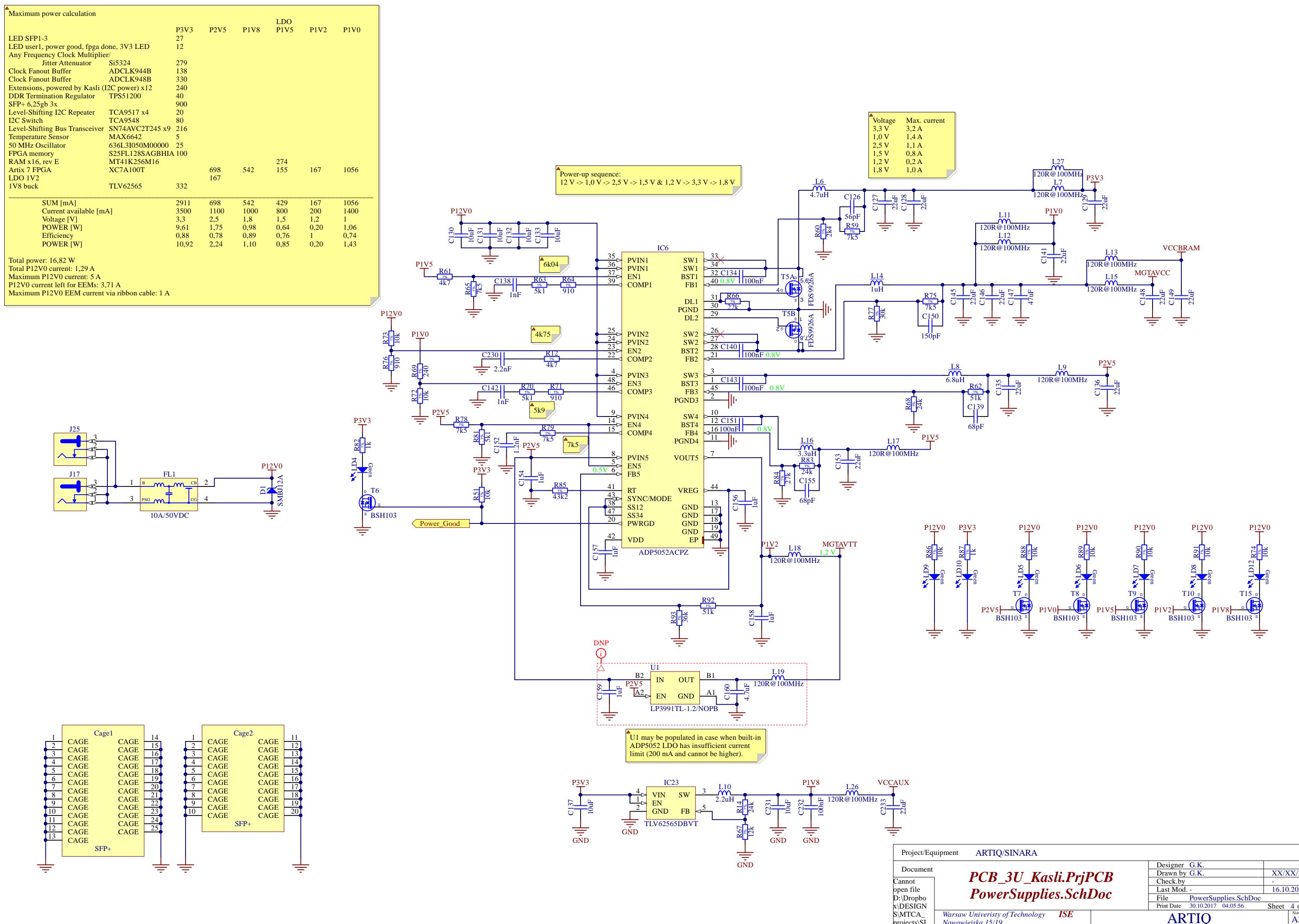
PCB_3U_Kasli.PrjPCB
FPGA.schdoc



Project/Equipment		ARTIQ/SINARA	
Document	PCB_3U_Kasli.PrjPCB	Designer	G.K.
Cannot open file	IDC_EXT_Connectors.SchDoc	Drawn by	G.K.
D:\Dropbox\DESIGN		Check by	XX/XX/XXXX
SMTCA_projects\SI		Last Mod.	- 29.08.2017
		File	IDC_EXT_Connectors.SchDoc
		Print Date	30.10.2017 04:05:54
		Sheet	3 of 12
		Size	A3
		Rev	-

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Nowowiejska 15/19

ARTIQ



A

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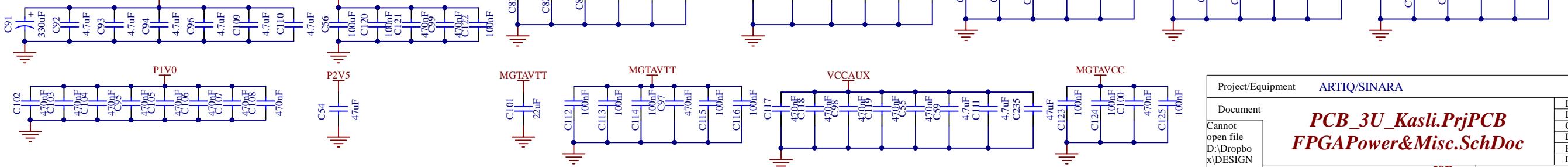
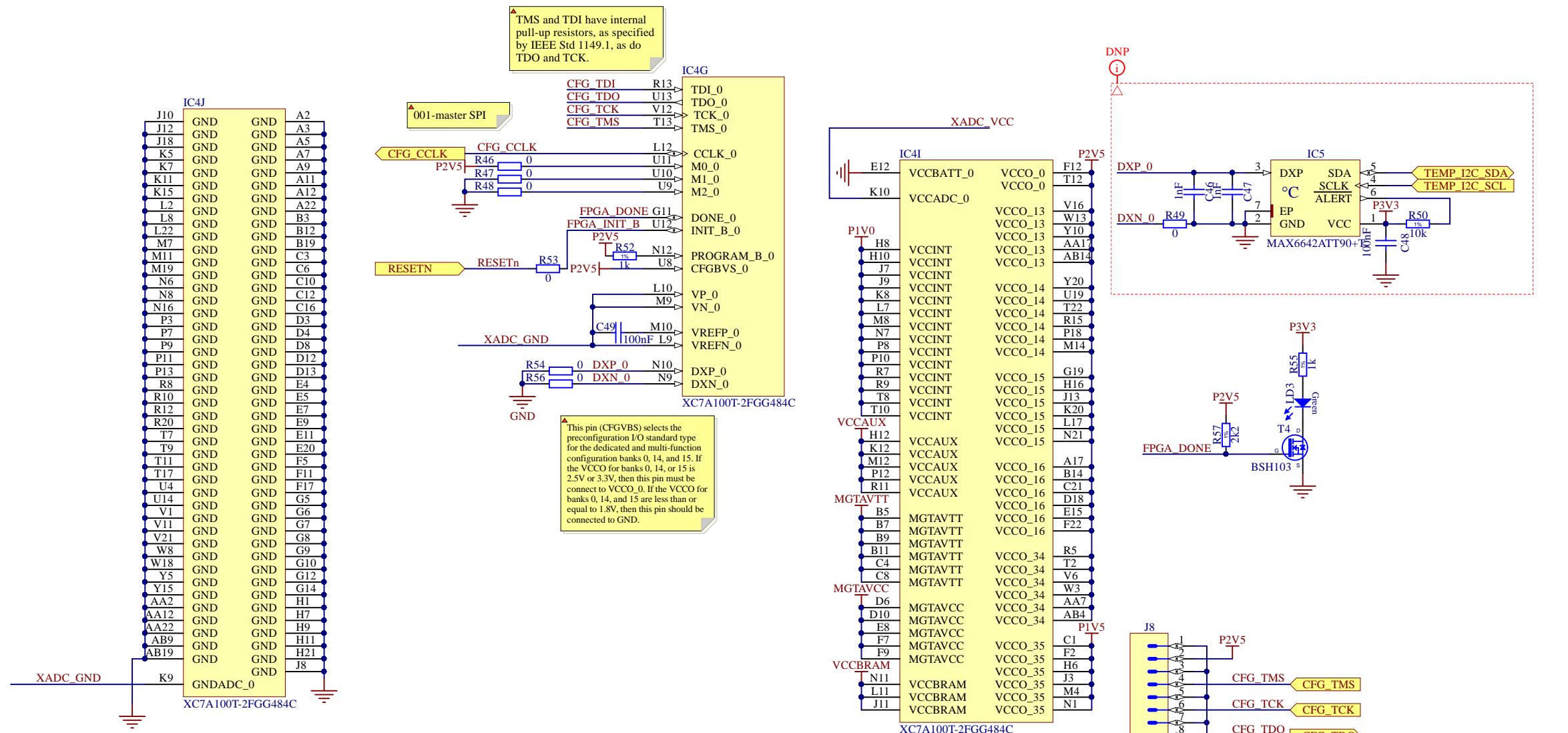
A

B

C

D

E



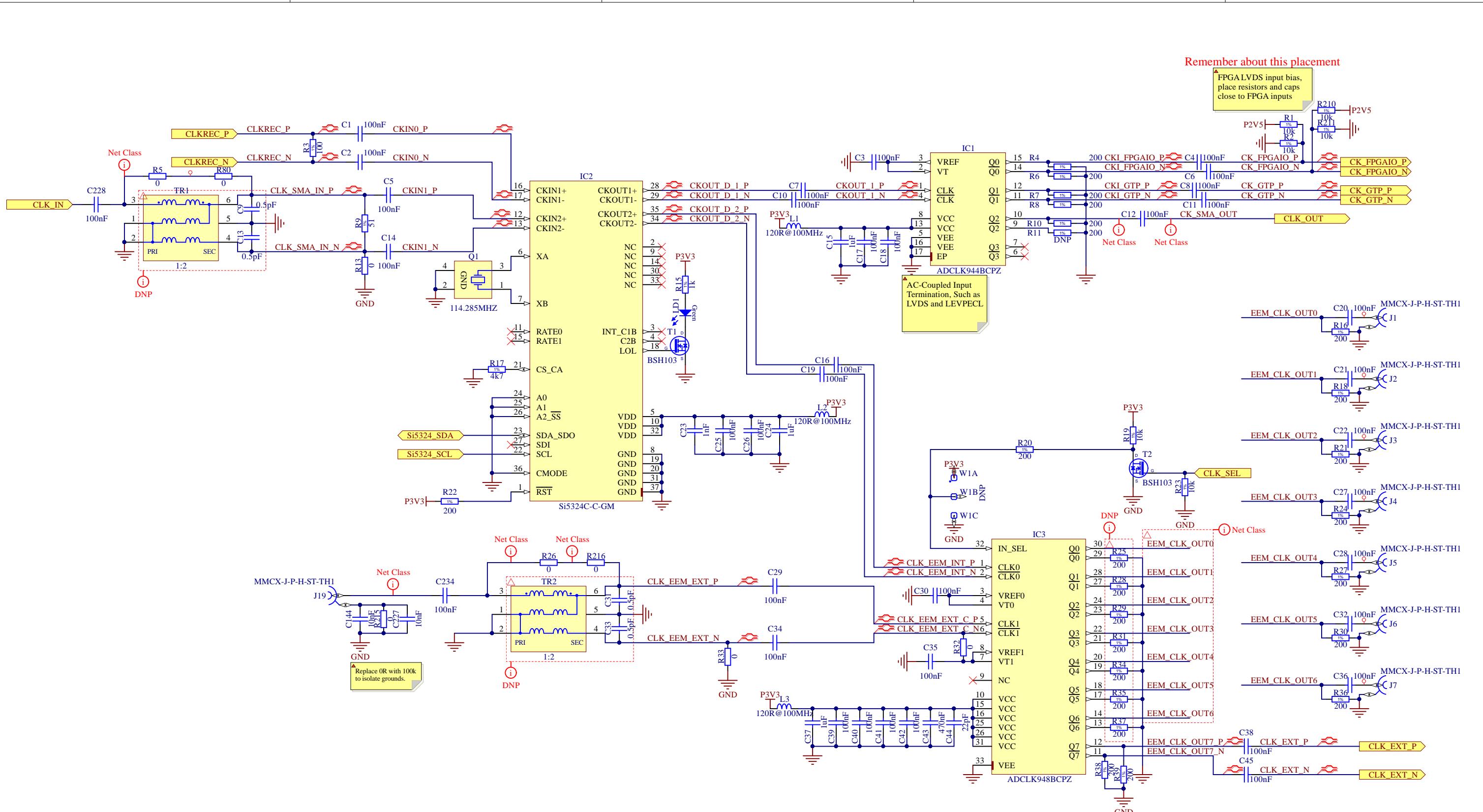
Project/Equipment: ARTIQ/SINARA
Document: PCB_3U_Kasli.PrjPCB
Last Mod.: 25.10.2017
File: FPGAPower&Misc.SchDoc
Print Date: 30.10.2017 04:05:57
Sheet 5 of 12

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Designer: G.K.	Drawn by: G.K.	Check by: XX/XX/XXXX
Cannot open file D:\Dropbox\DESIGN\S\MTCA_projects\SI		
Last Mod.: -	25.10.2017	
File: FPGAPower&Misc.SchDoc		
Print Date: 30.10.2017 04:05:57		
Sheet 5 of 12		

ARTIQ

Size A3 Rev -

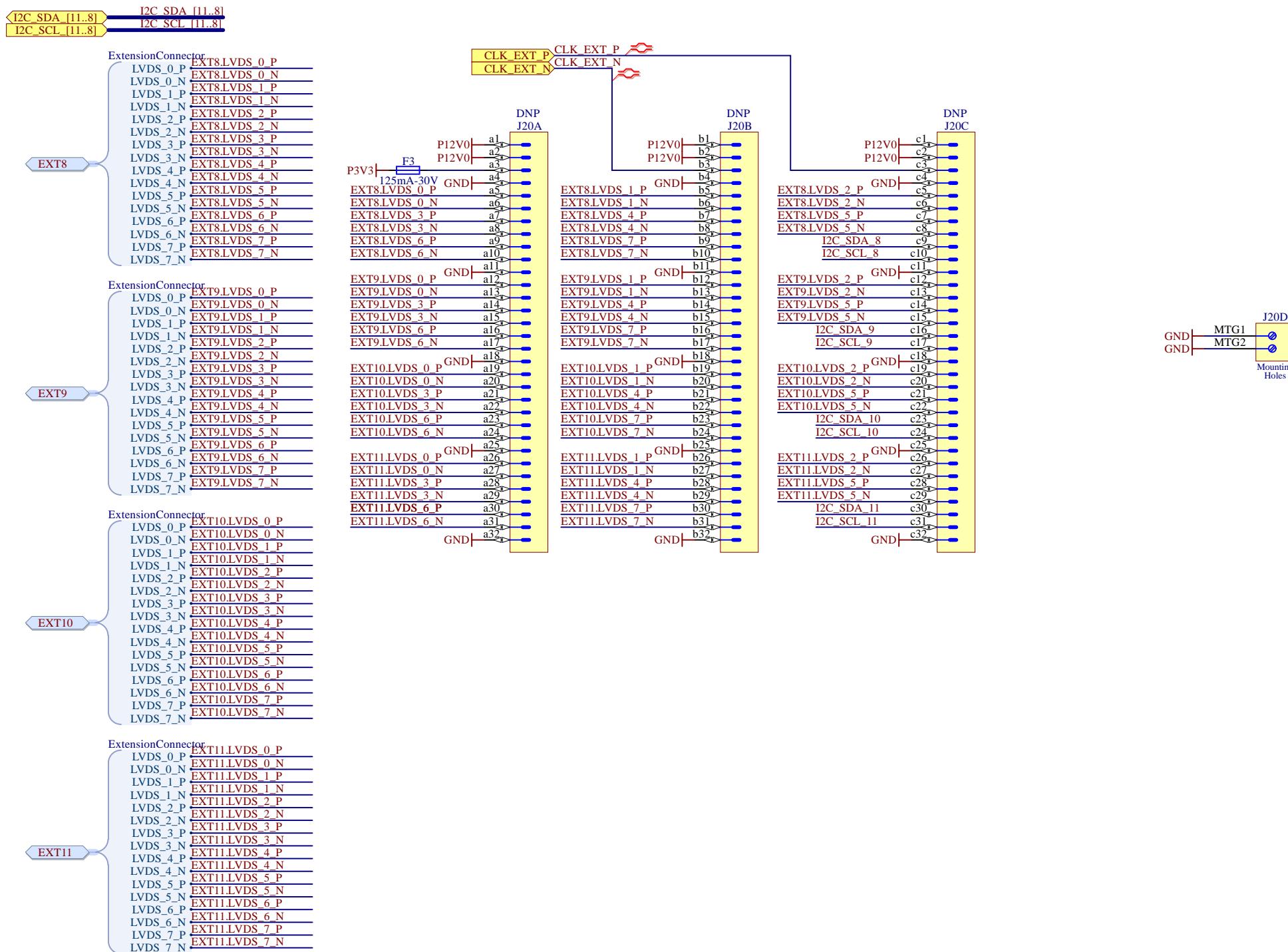


Project/Equipment		ARTIQ/SINARA	
Document	Designer G.K.	Drawn by G.K.	XX/XX/XXXX
Cannot open file D:\Dropbox\DESIGN\SMTCA_projects\SI	Check by	Last Mod. -	24.10.2017
		File	ClockRecovery.SchDoc
		Print Date	30.10.2017 04:05:58
		Sheet	6 of 12
		Size	A3
		Rev	-

PCB_3U_Kasli.PrjPCB
ClockRecovery.SchDoc

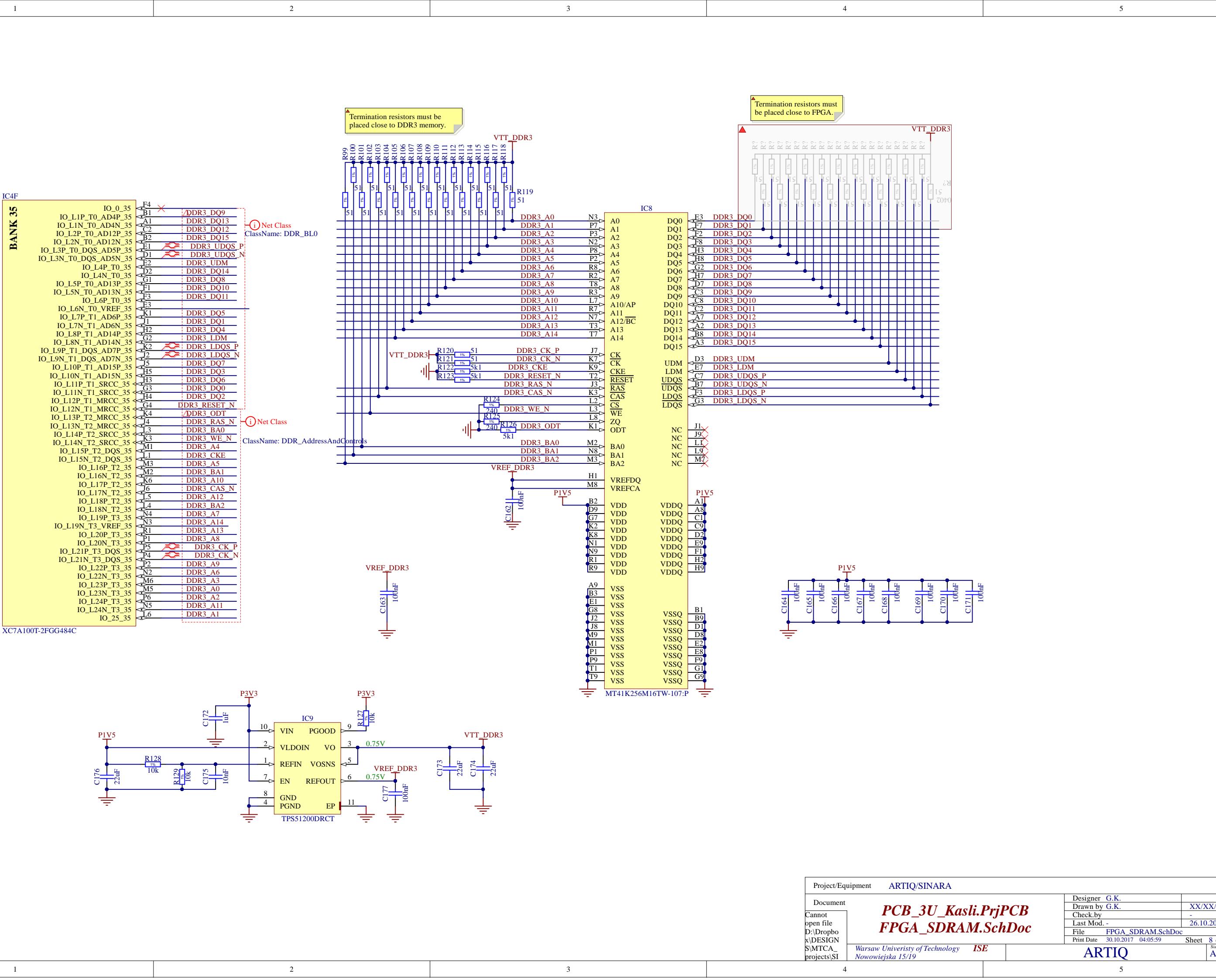
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Nowowiejska 15/19

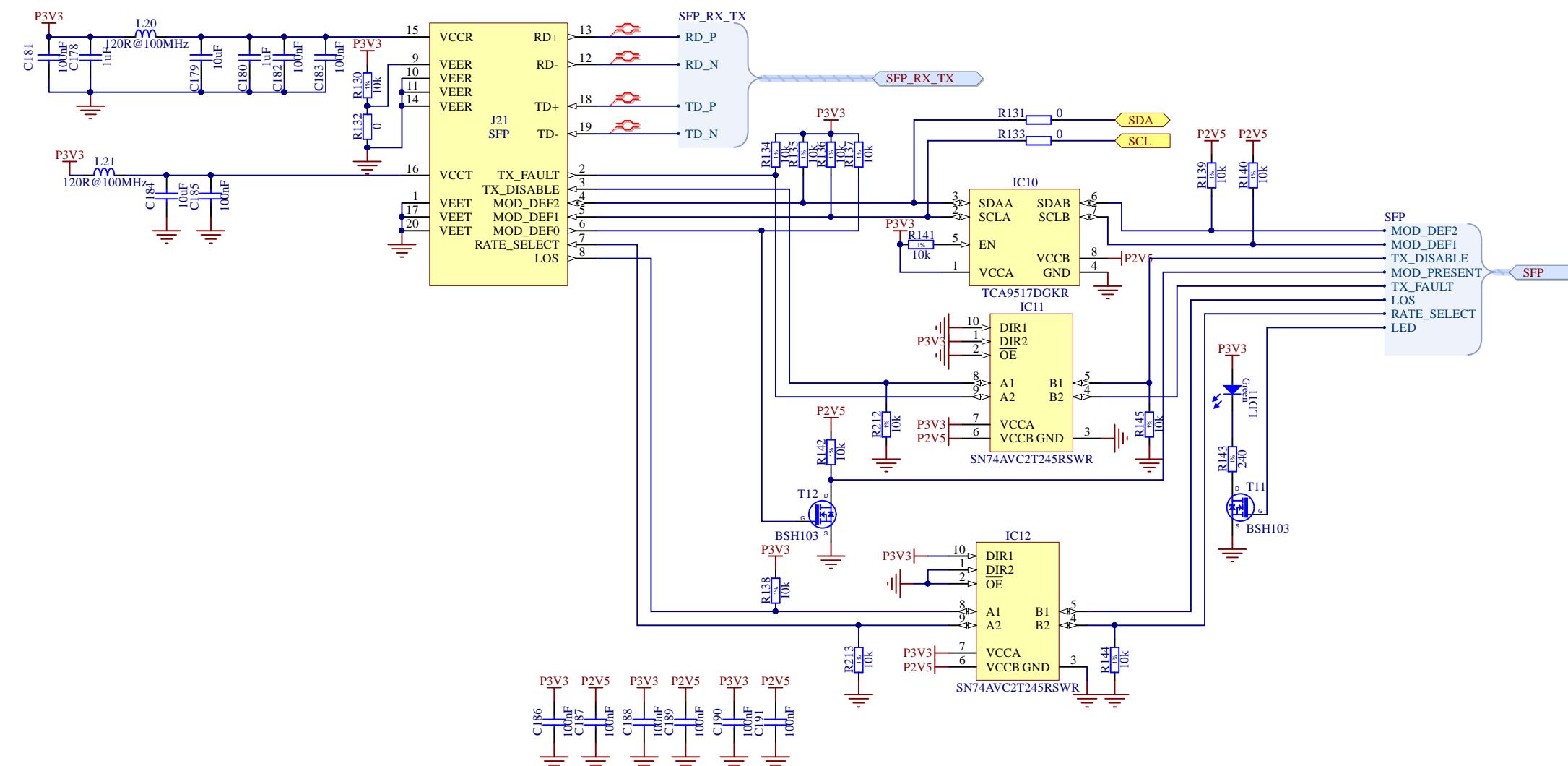
ARTIQ



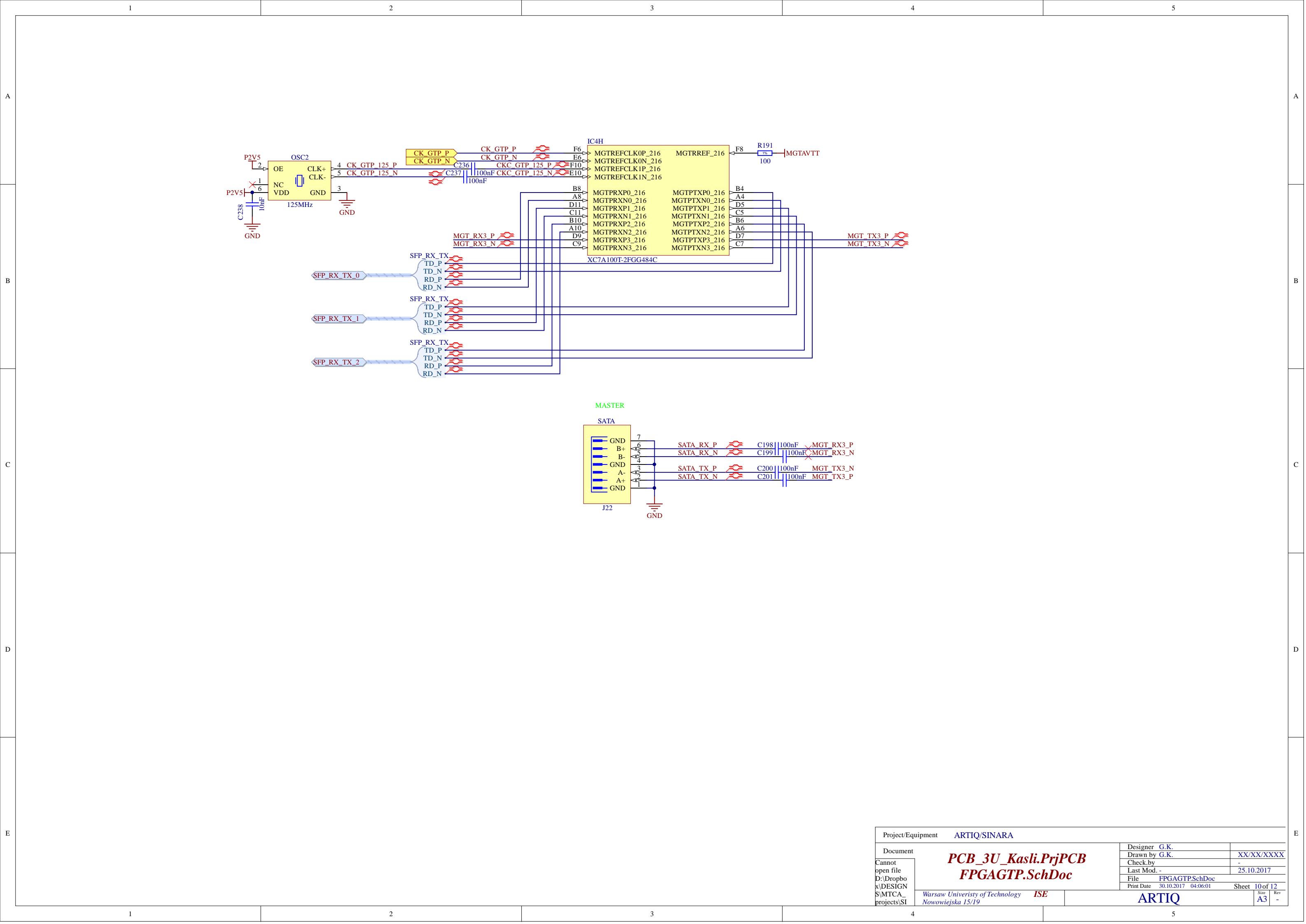
Project/Equipment		ARTIQ/SINARA	
Document	Designer	G.K.	Drawn by
Cannot open file D:\Dropbox\DESIGN\S\MTCA_projects\SI	Check by		XX/XX/XXXX
	Last Mod.	-	16.10.2017
	File	BackplaneConnector.SchDoc	
	Print Date	30.10.2017 04:05:59	Sheet 7 of 12
	Warsaw University of Technology ISE Nowowiejska 15/19		Size A3 Rev -

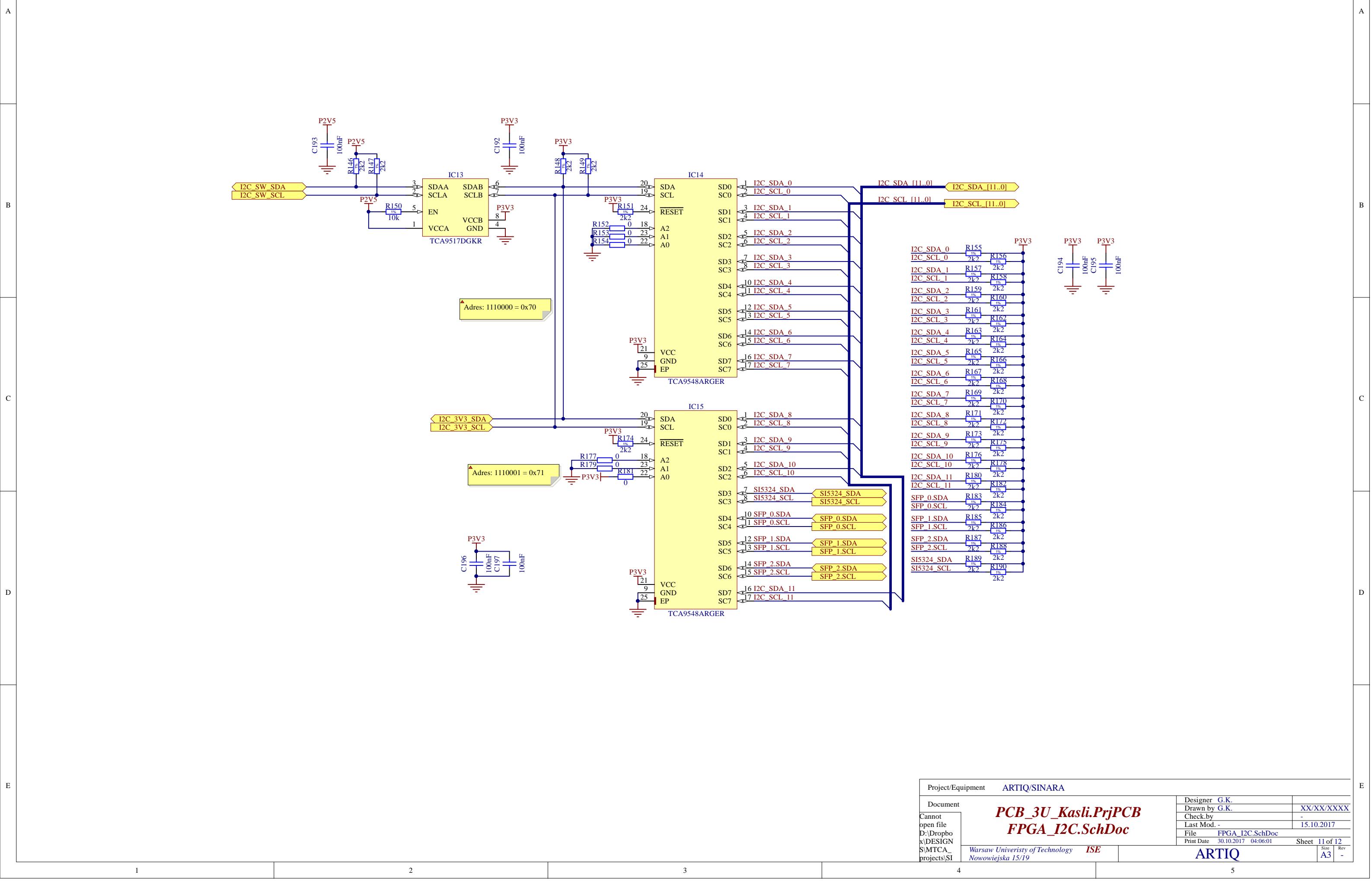
PCB_3U_Kasli.PrjPCB
BackplaneConnector.SchDoc



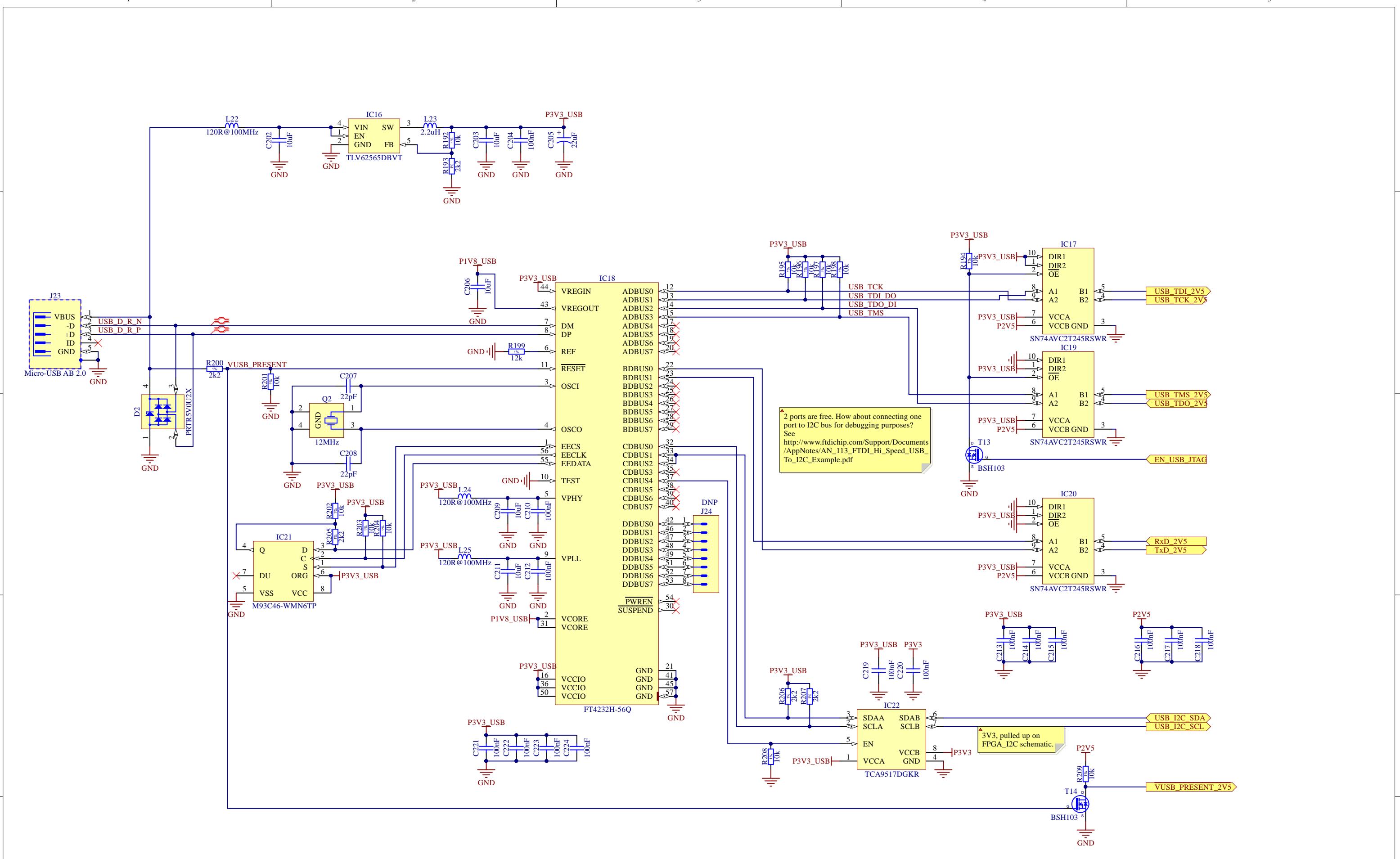


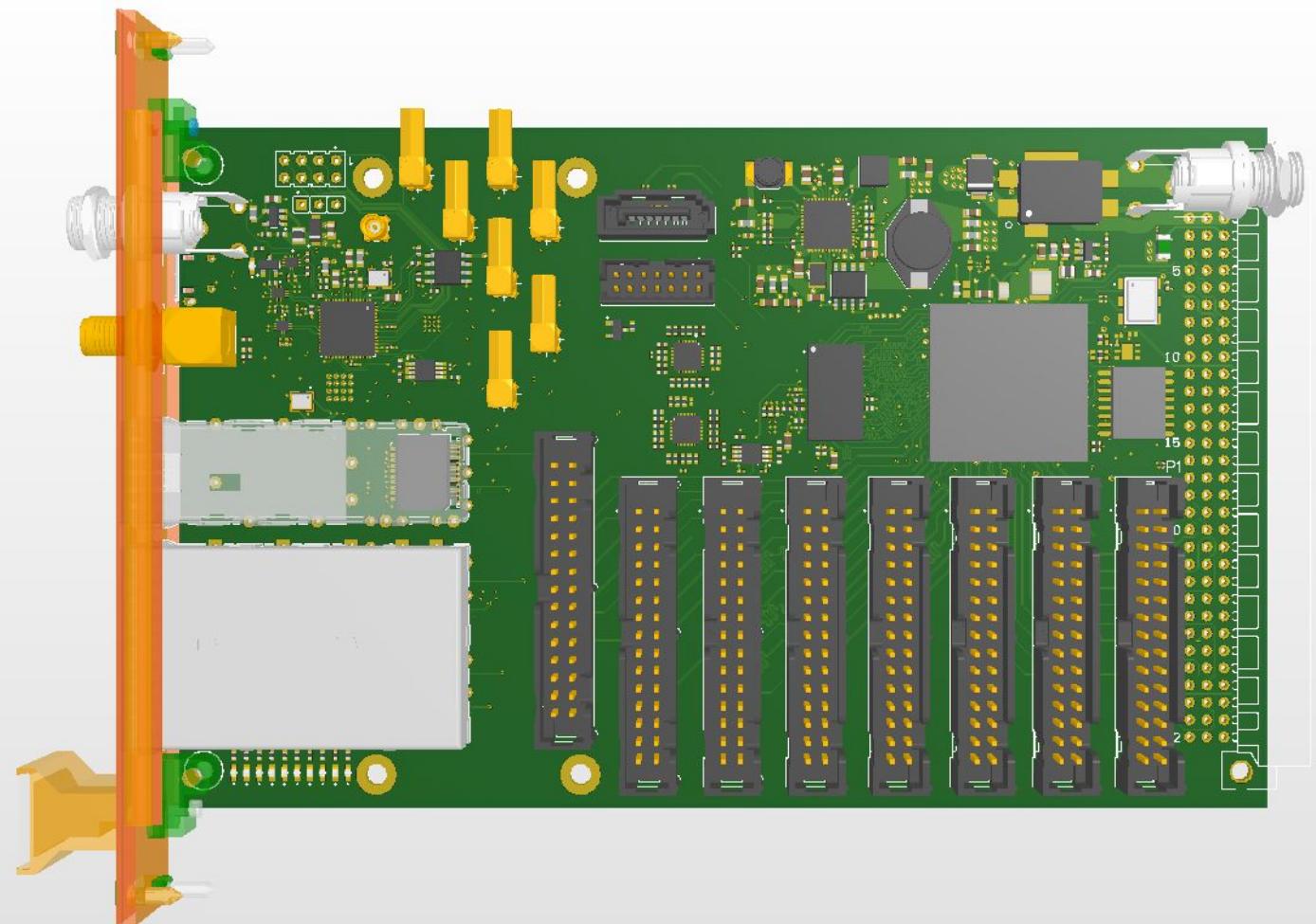
Project/Equipment		ARTIQ/SINARA	
Document	Designer G.K. Drawn by G.K. Check by Last Mod. - File SFP.SchDoc Print Date 30.10.2017 04:06:00	XX/XX/XXXX Check by Last Mod. - 22.10.2017 File SFP.SchDoc Print Date 30.10.2017 04:06:00	Sheet 9 of 12 Size A3 Rev -
PCB_3U_Kasli.PrjPCB SFP.SchDoc		Warsaw University of Technology ISE Nowowiejska 15/19	
		ARTIQ	

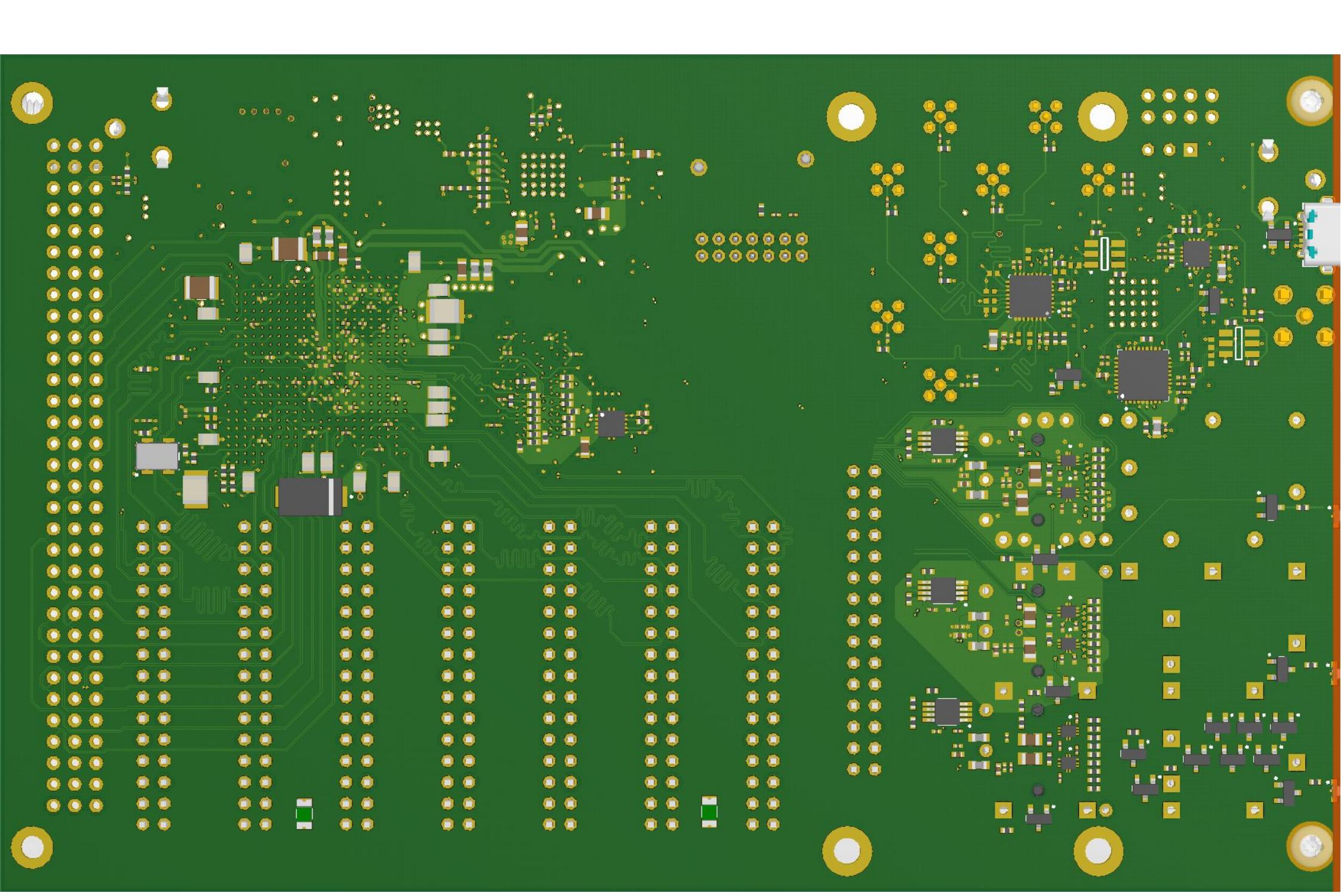


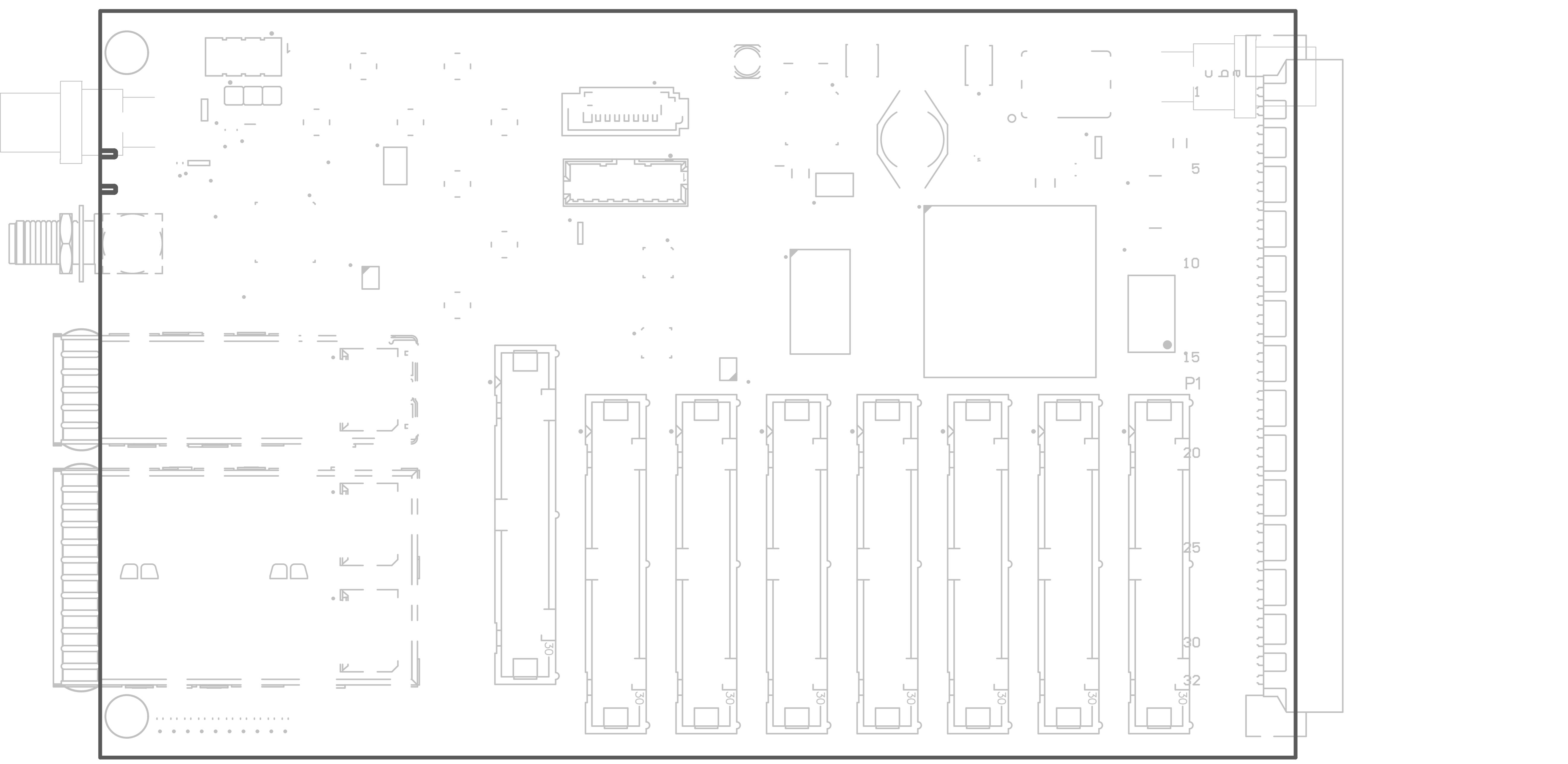


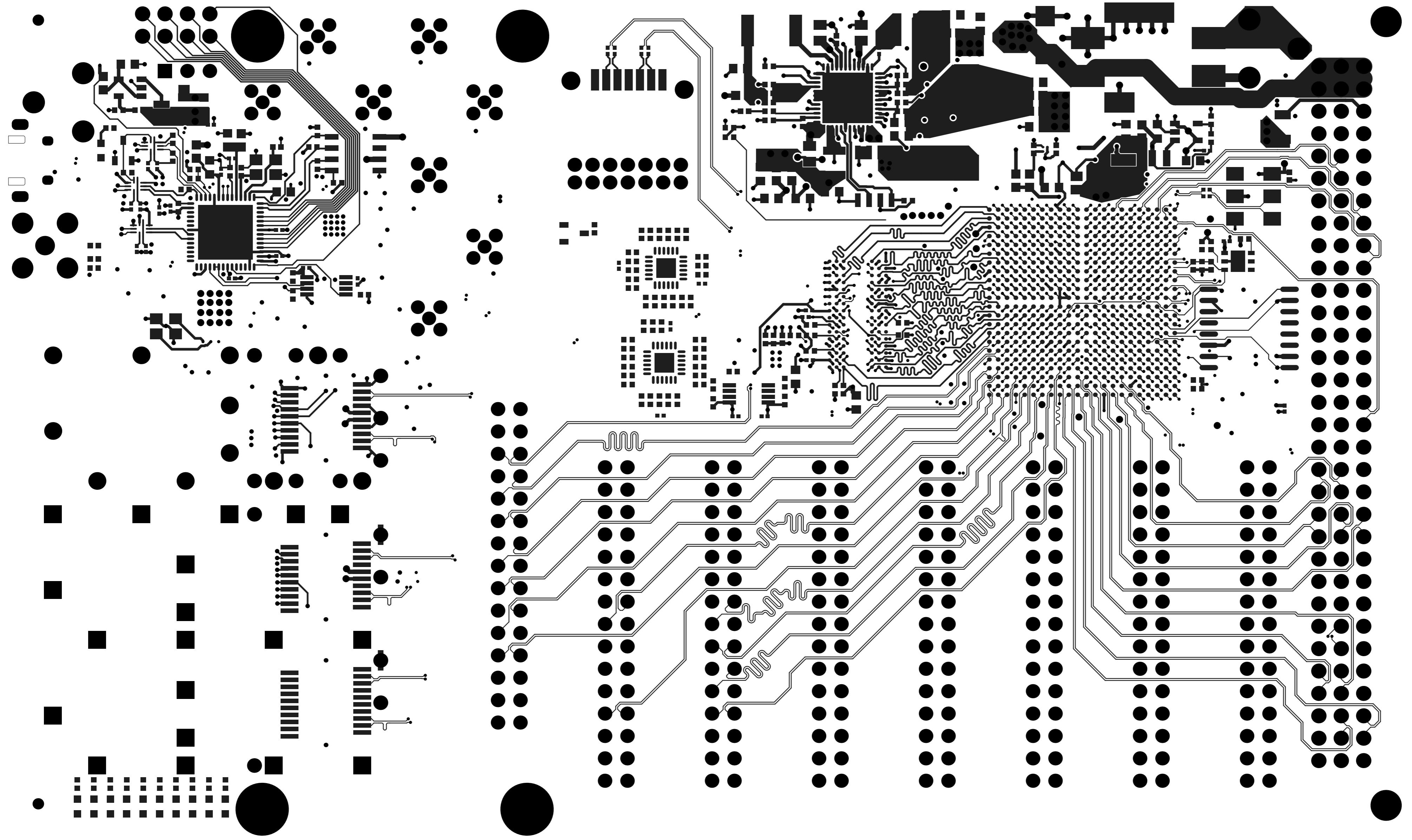
Project/Equipment		ARTIQ/SINARA	
Document		Designer	G.K.
Cannot open file		Drawn by	G.K.
D:\Dropbox\DESIGN		Check by	XX/XX/XXXX
S\MTCA_projects\SI		Last Mod.	-
		File	FPGA_I2C.SchDoc
		Print Date	30.10.2017 04:06:01
		Sheet	11 of 12
PCB_3U_Kasli.PrjPCB		ARTIQ	
FPGA_I2C.SchDoc		Warsaw University of Technology ISE	
Nowowiejska 15/19		Size A3 Rev -	

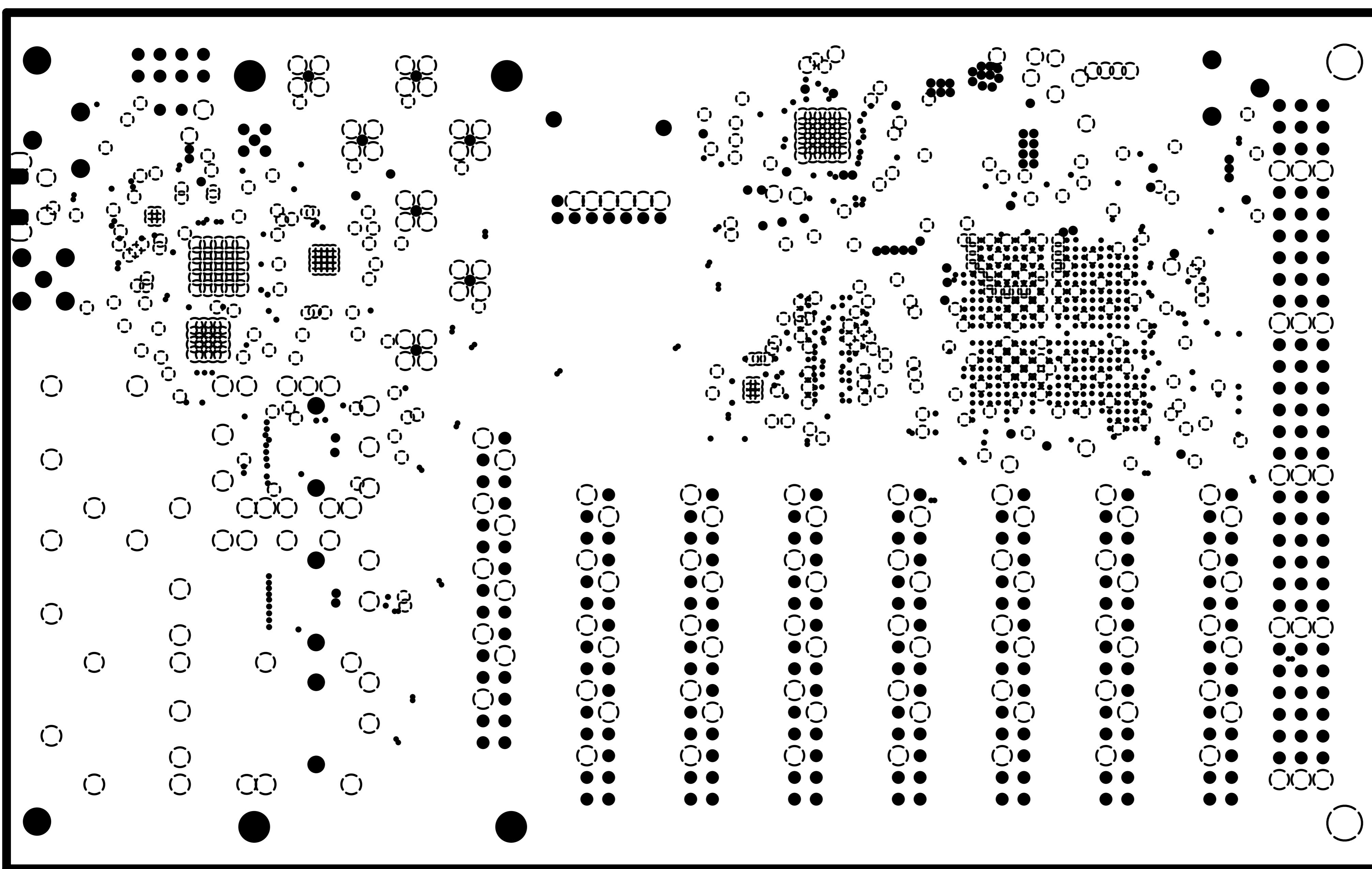












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