

ARTIQ Sayma

Sayma_AMC



TITLE

SIZE

A3

DWG NO

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G.K.

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29

2016/11/07:18:08:13

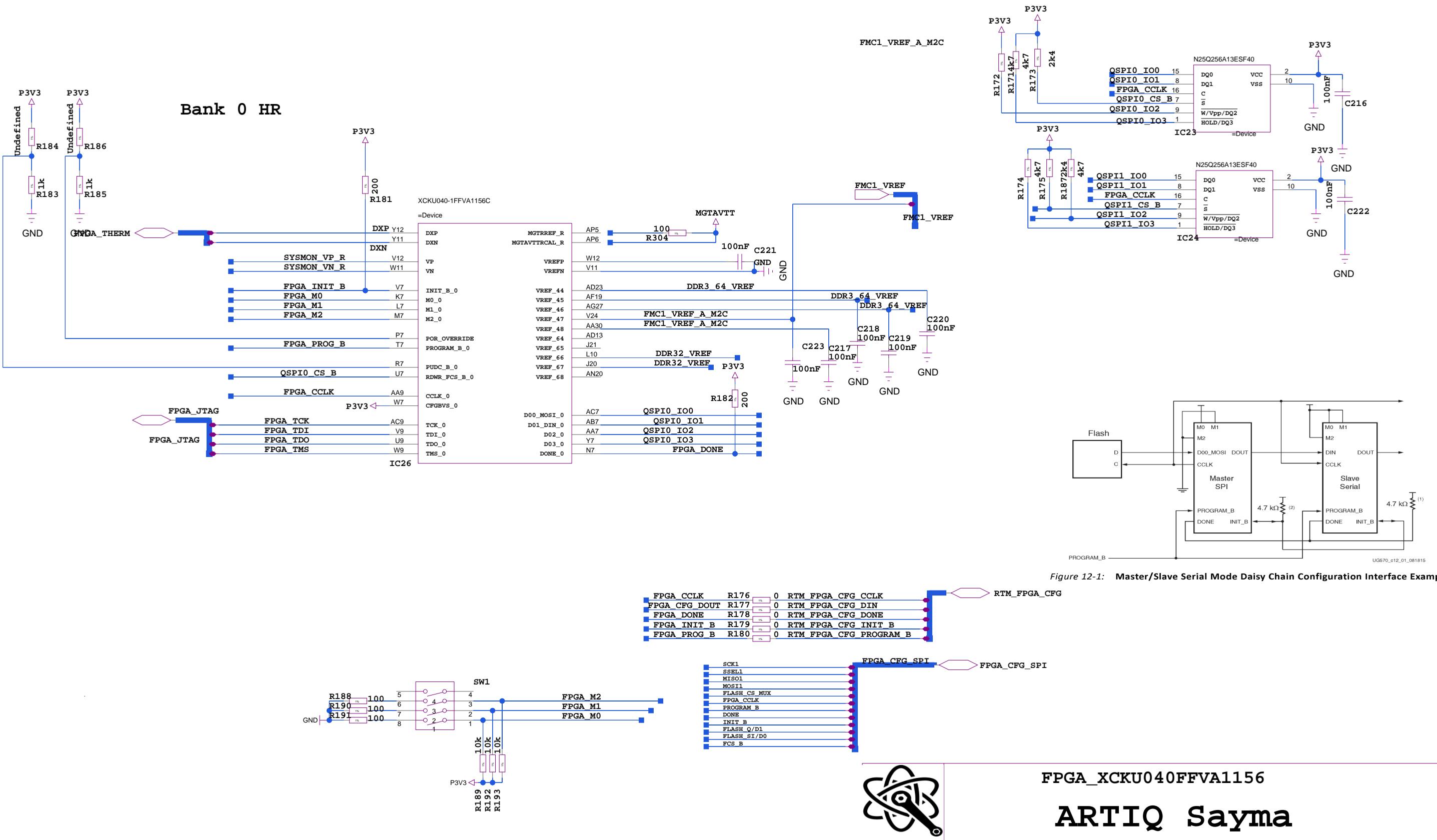


Figure 12-1: Master/Slave Serial Mode Daisy Chain Configuration Interface Example

UG670_c12_01_081815



FPGA_XCKU040FFVA1156

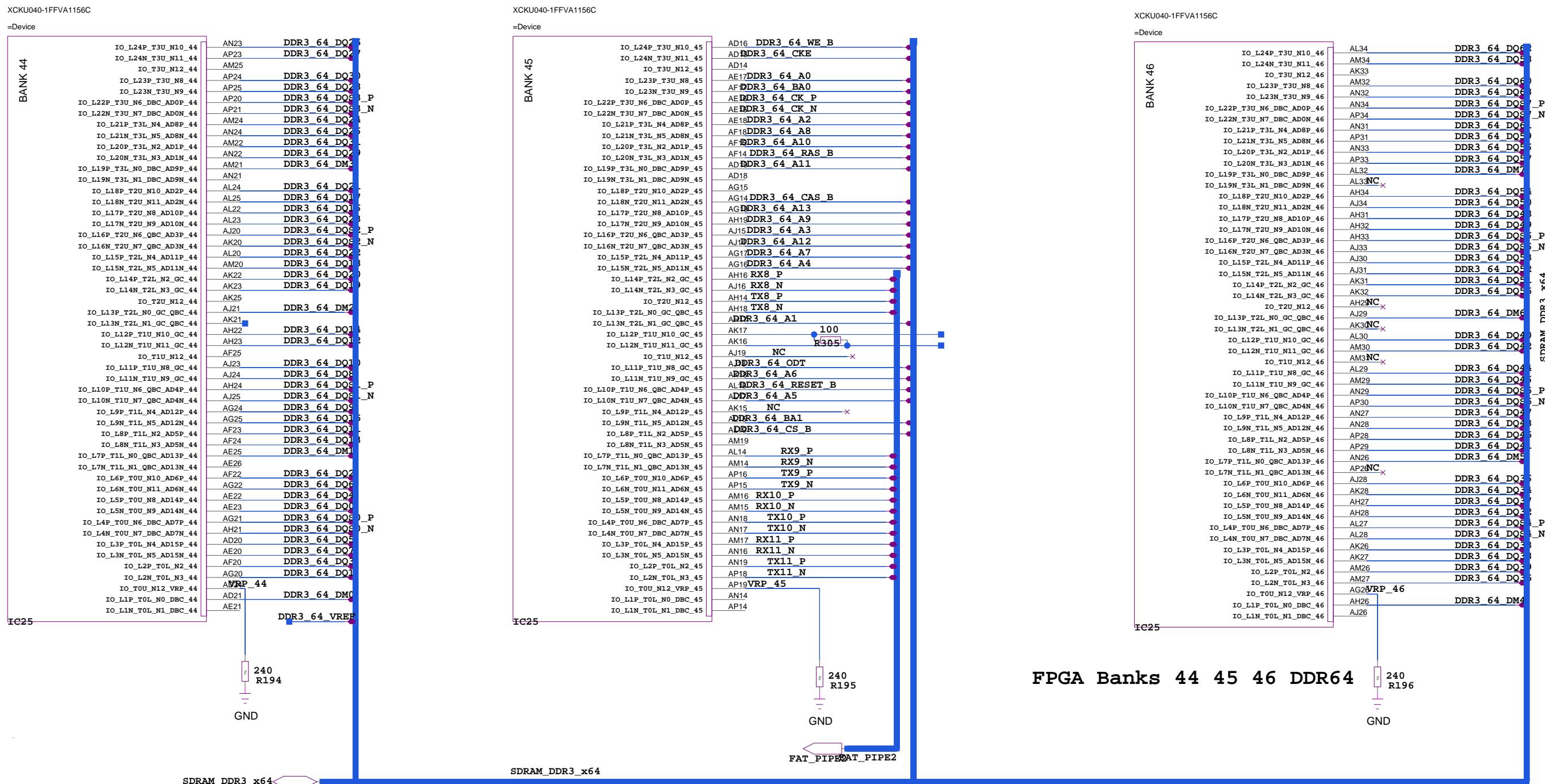
ARTIQ Sayma

FPGA Bank 0 CFG

Bank 44 HP

Bank 45 HF

Bank 46 HP



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FPGA Banks 44 45 46 DDR

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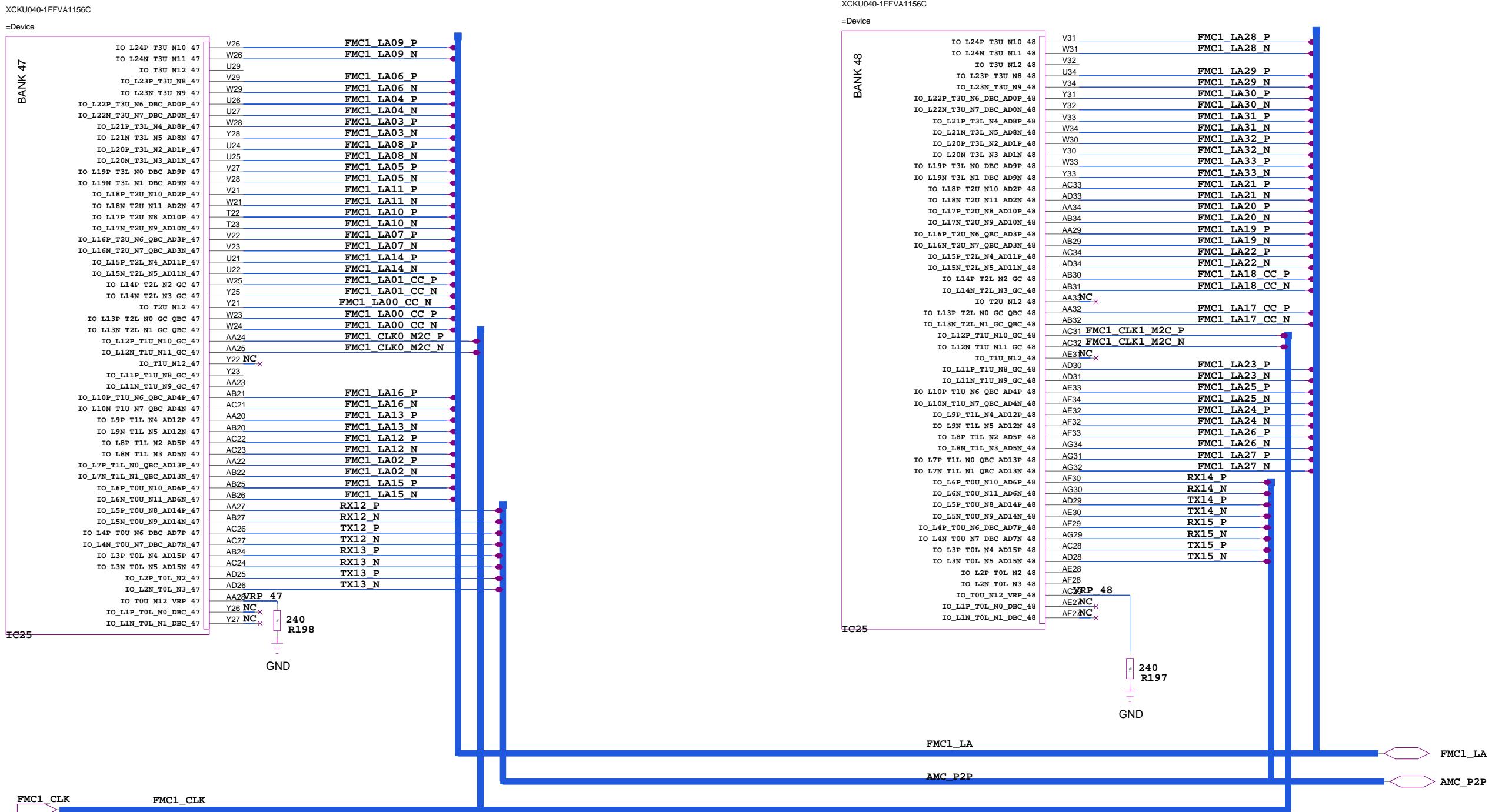
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Bank 47 HP

Bank 48 HF



FPGA_XCKU040FFVA1156



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FPGA Banks 47 48 HP FM

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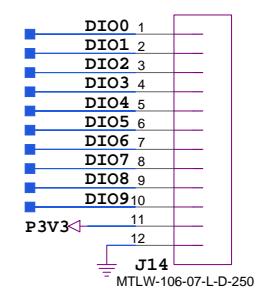
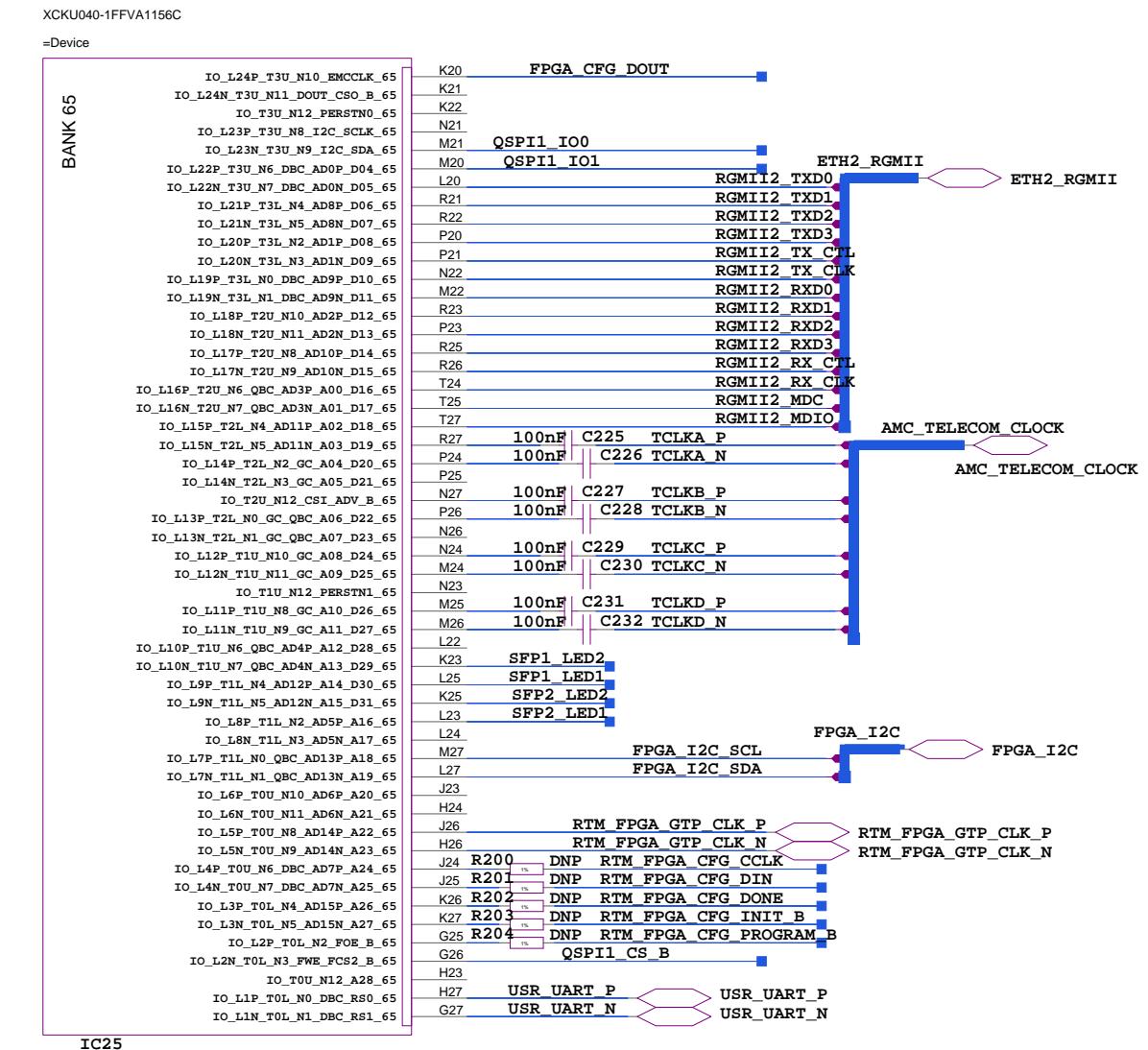
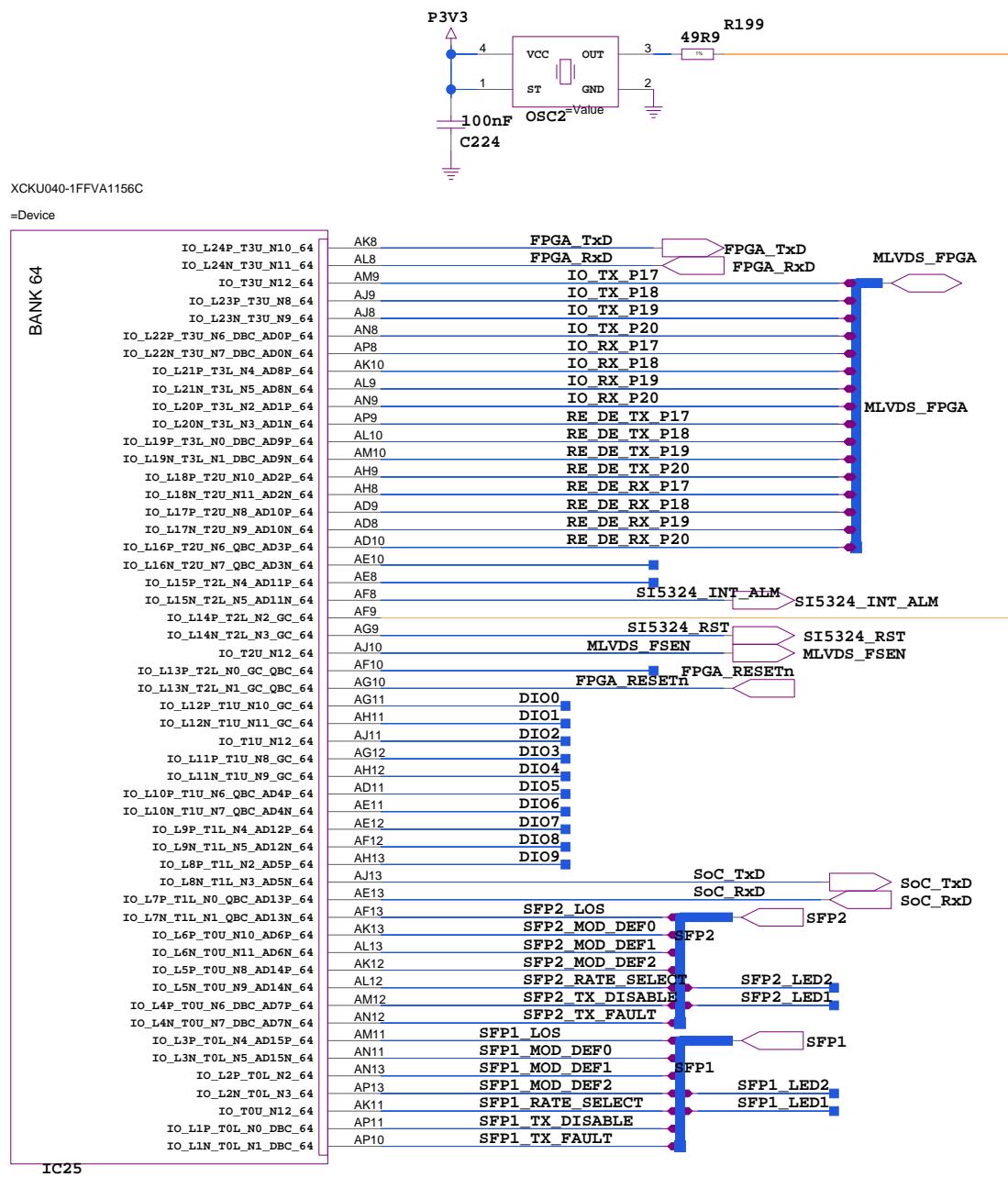
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Bank 64 HR

Bank 65 HE



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FPGA Banks 64 65 HR

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REV

Page 1

G.K.

29

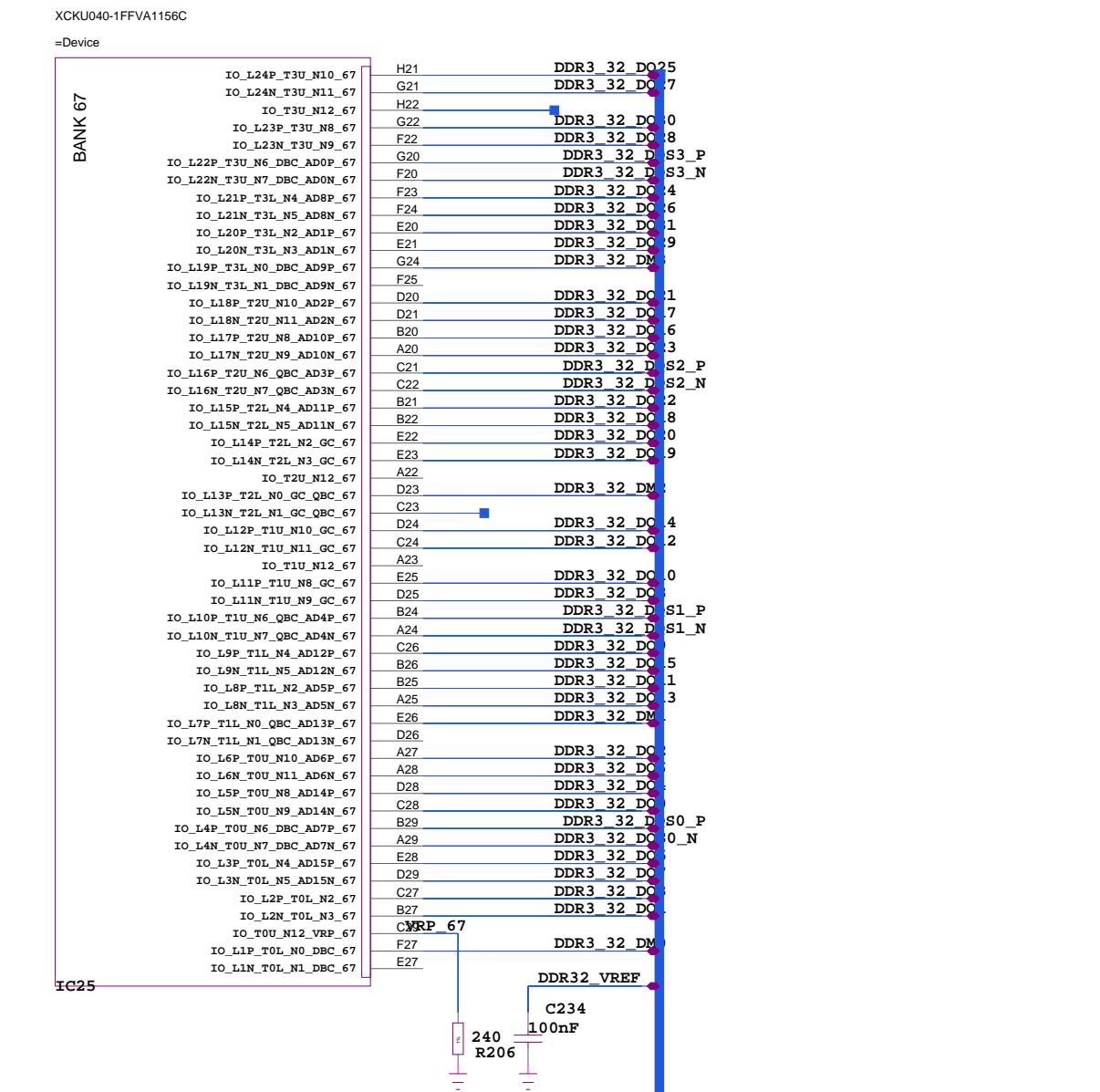
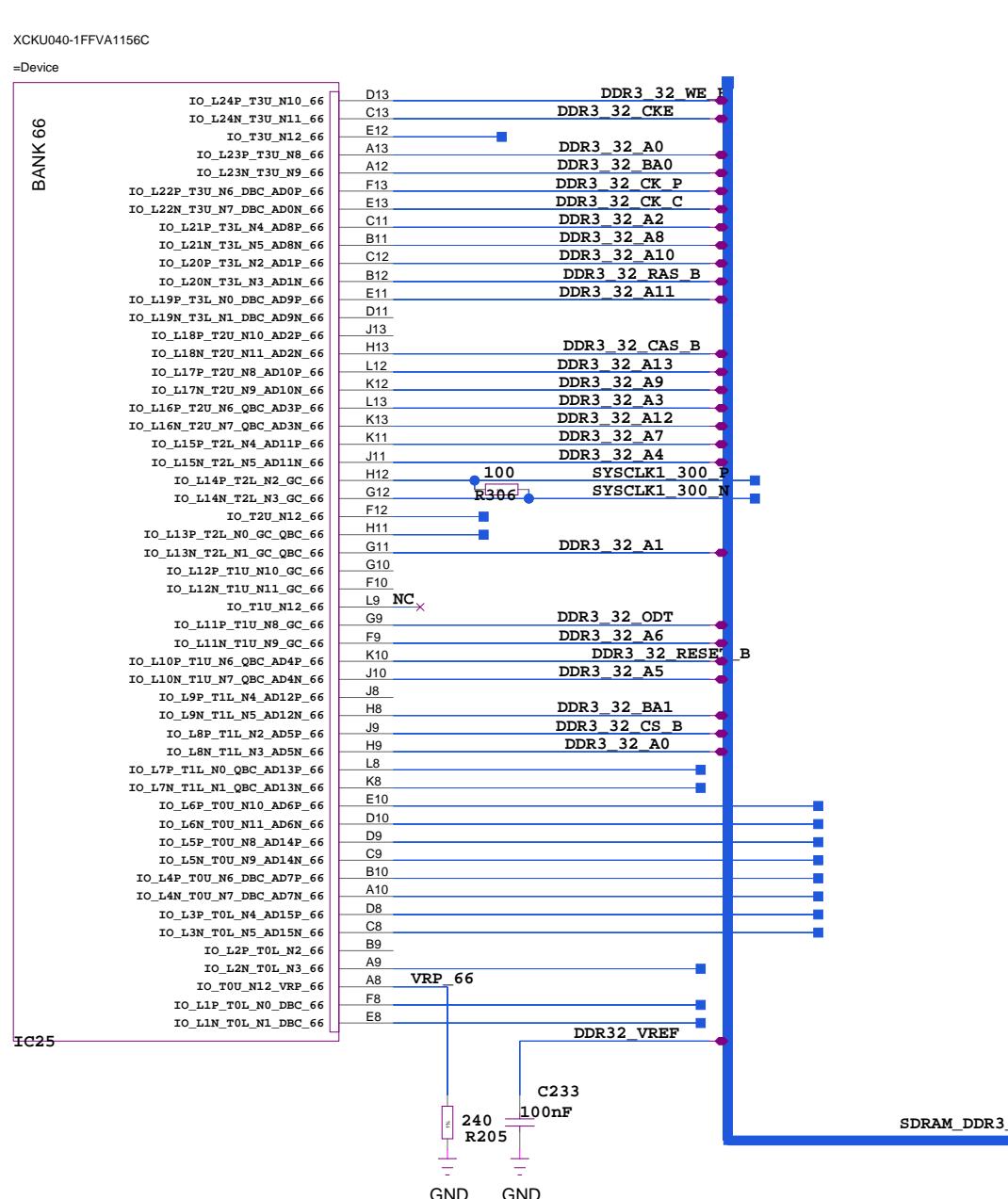
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Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

Bank 66 HP

Bank 67 HE



FPGA Banks 66 67 DDR32



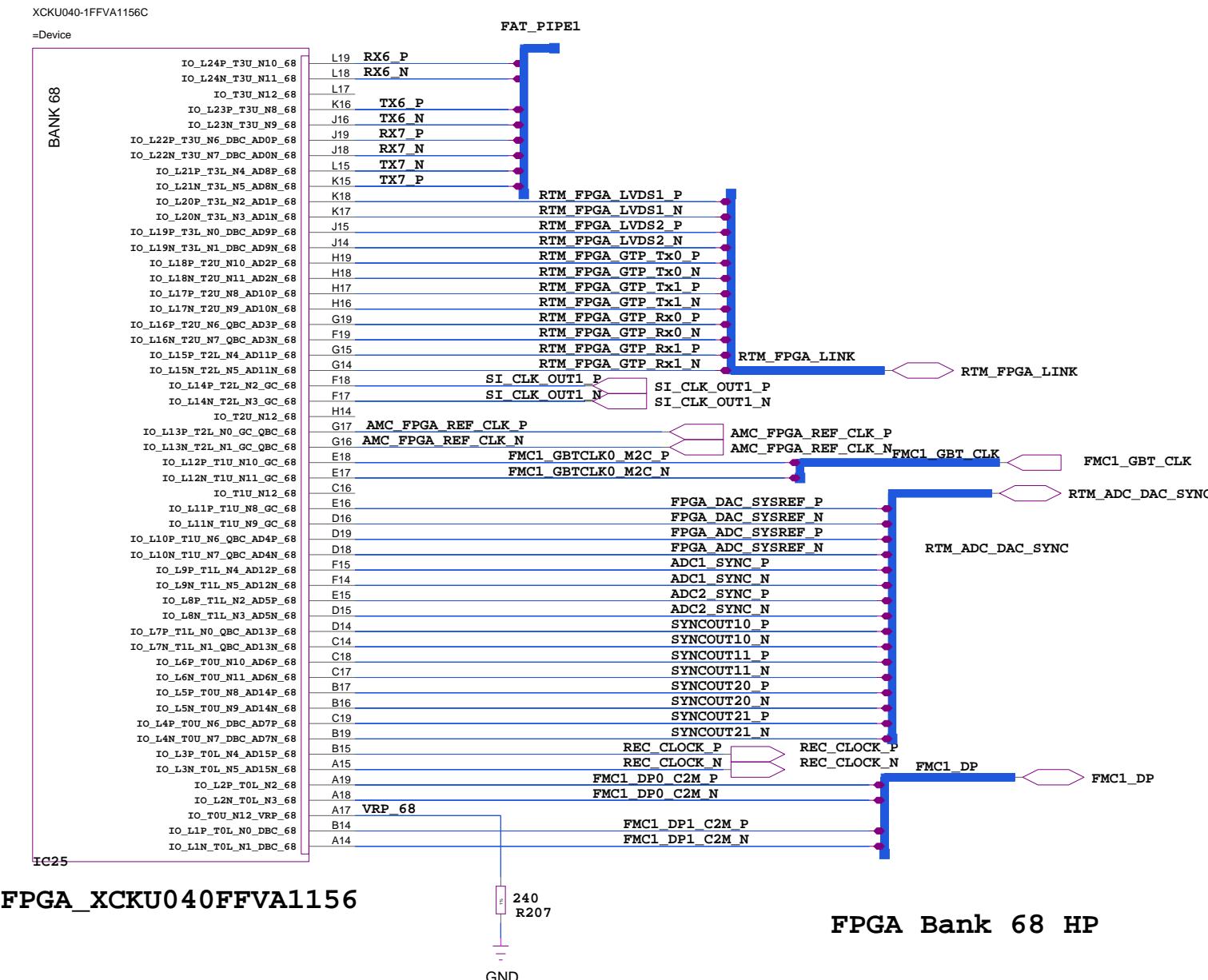
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FPGA Banks 66 67 DDR3 32

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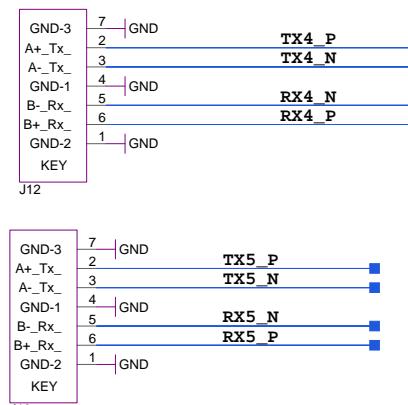
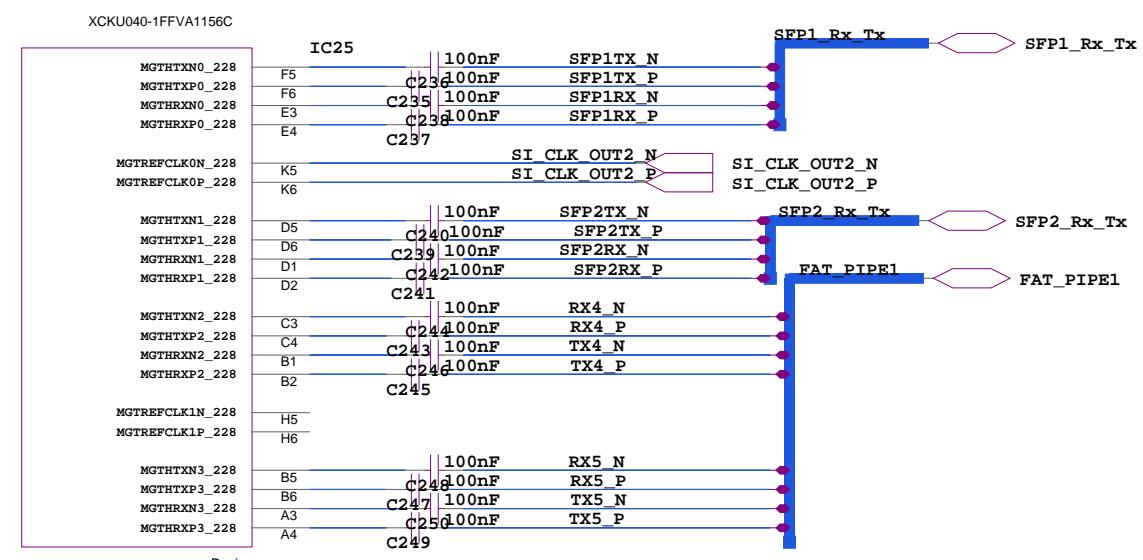
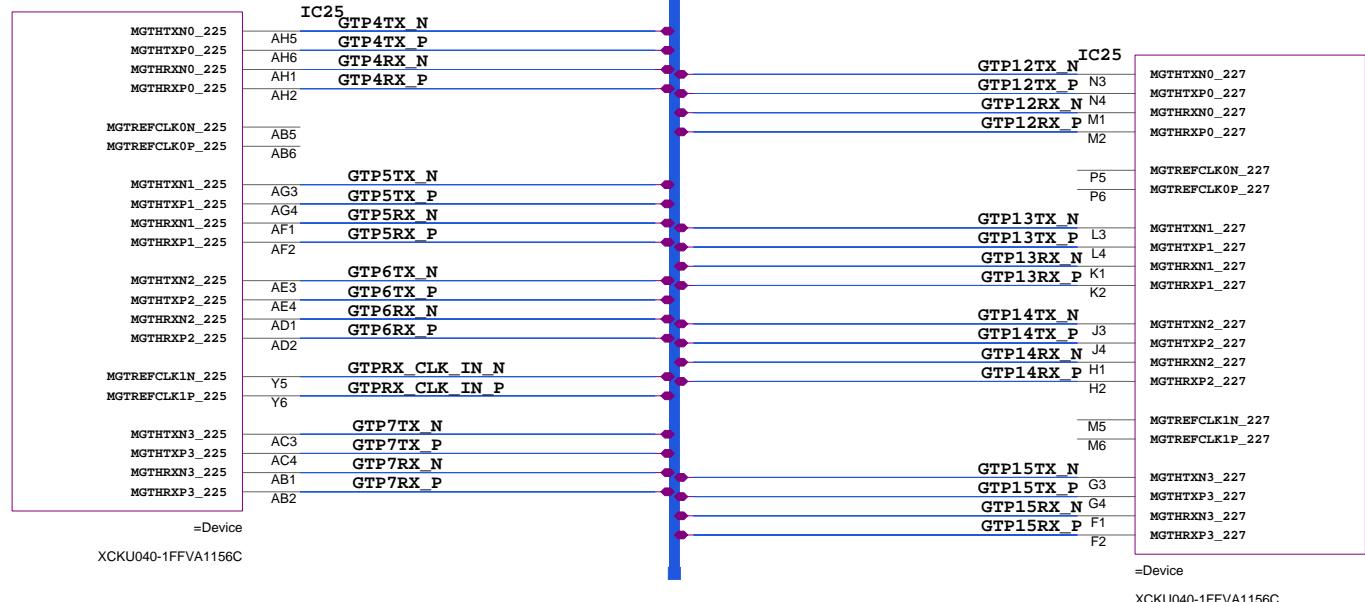
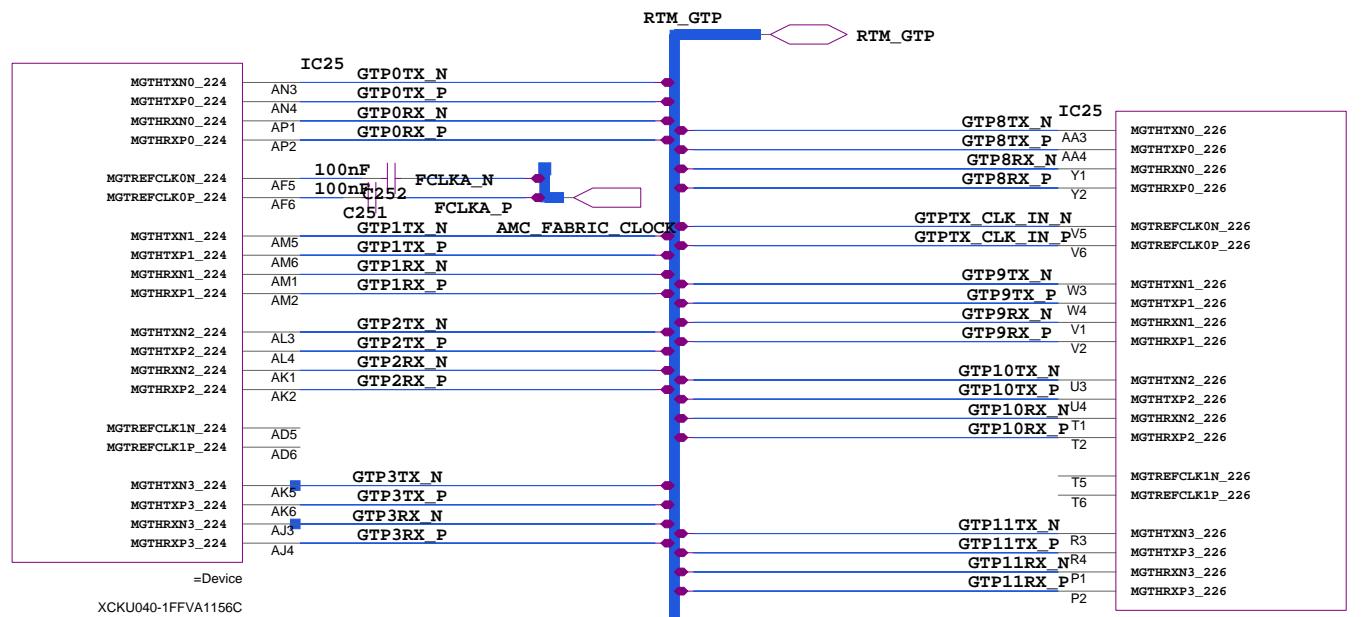
Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

Bank 68 HP



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FPGA Bank 68 HP



FPGA_XCKU040FFVA1156



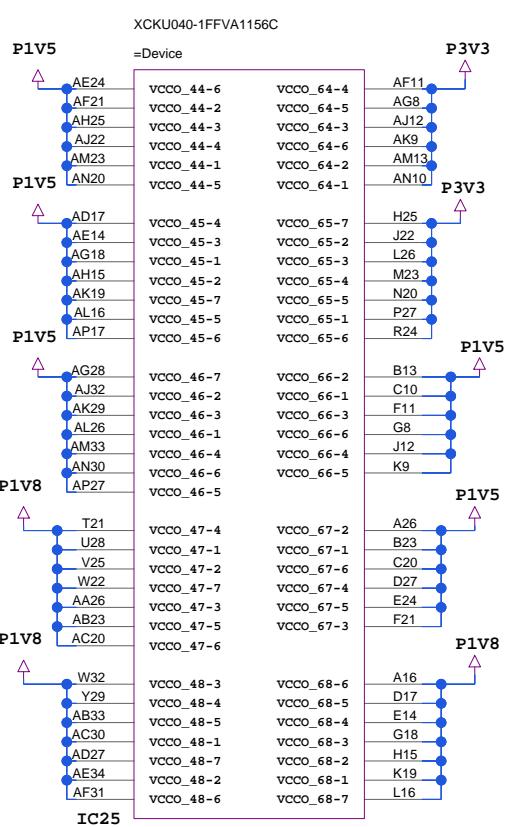
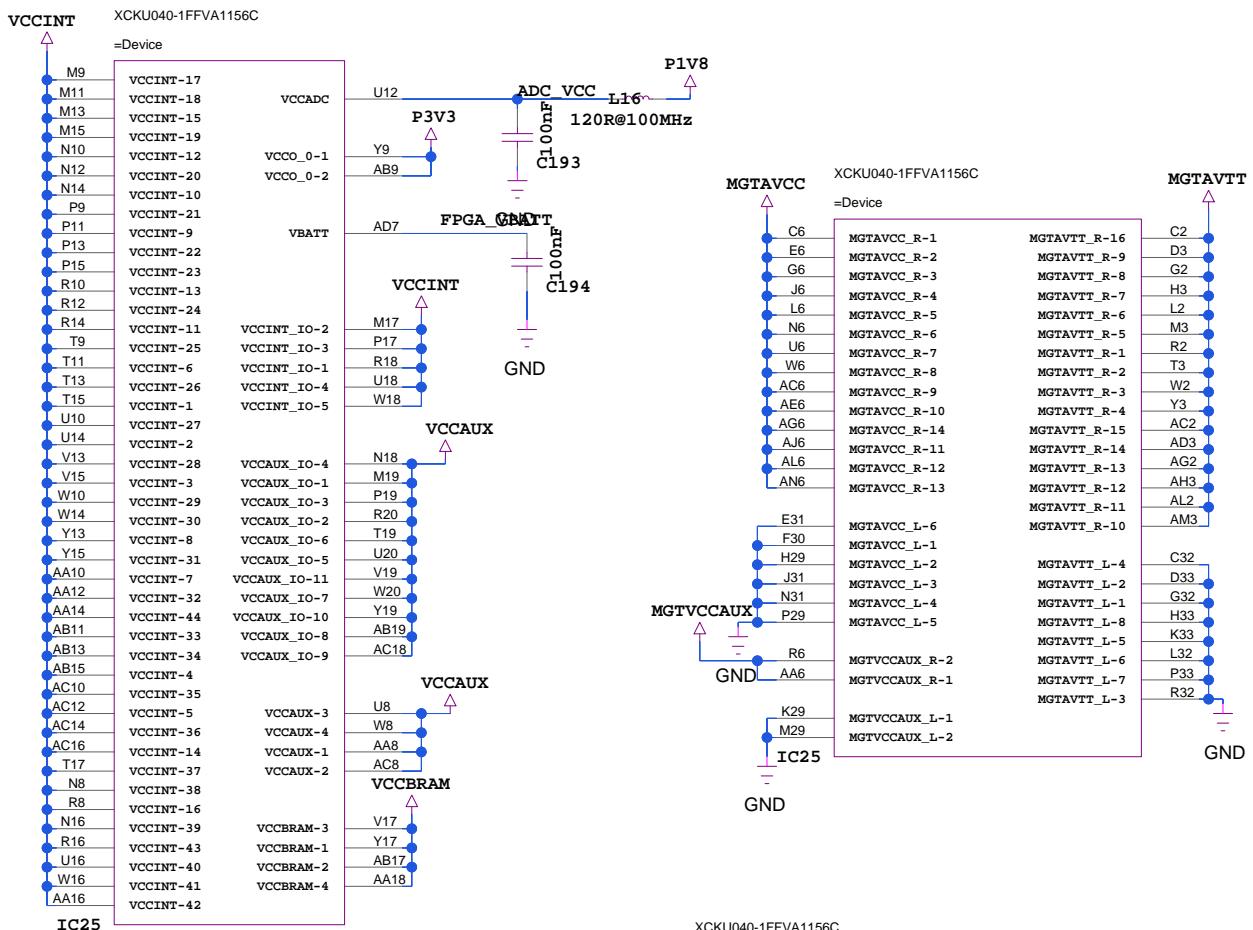
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FPGA Banks 224 225 226 227 228

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Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

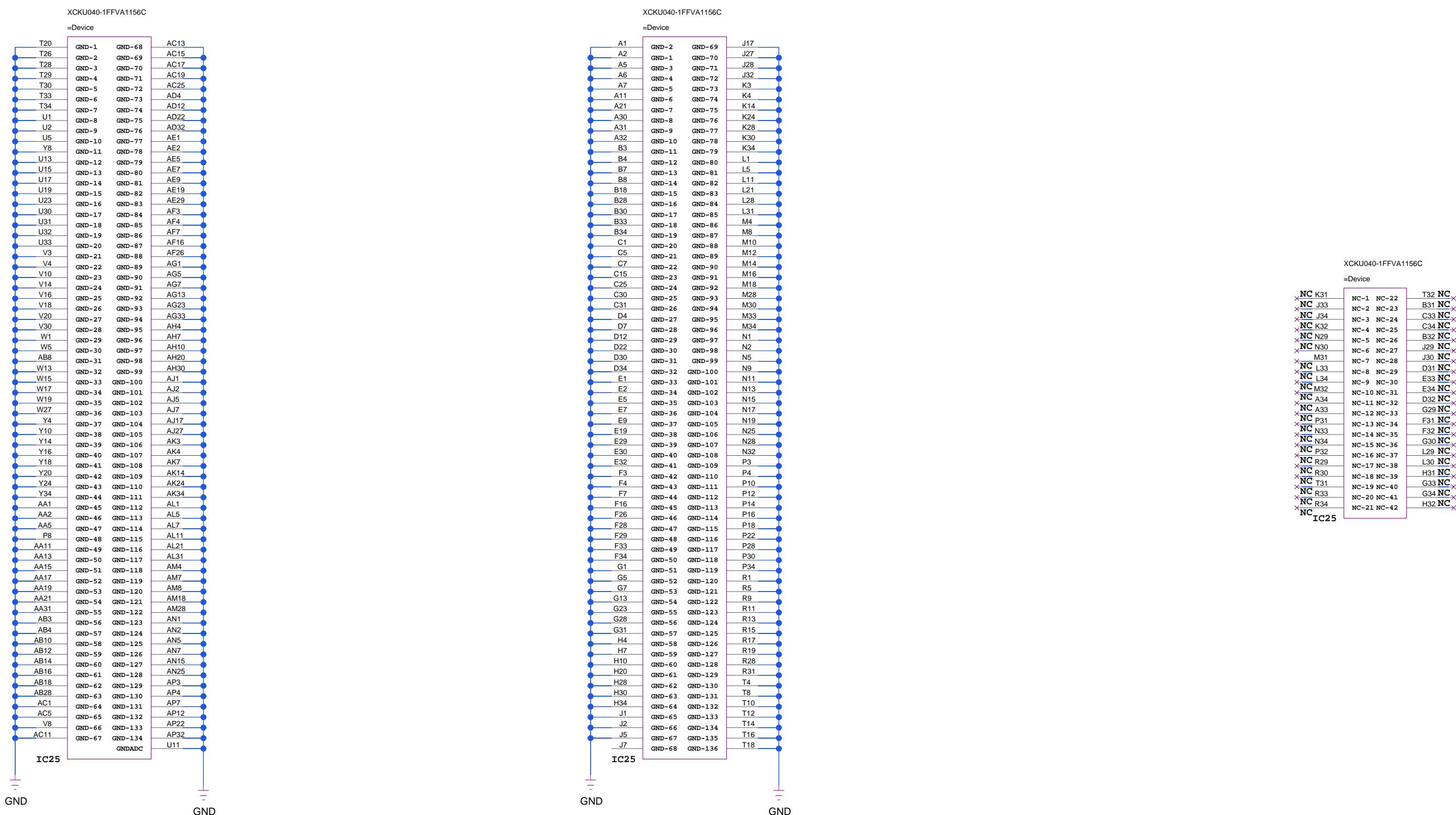
Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V _{CCINT}	Internal supply voltage	0.922	0.950	0.979	V
	For -1L (0.90V) devices: internal supply voltage	0.880	0.900	0.920	V
	For -3 (1.0V only) devices: internal supply voltage	0.970	1.000	1.030	V
V _{CCINT_IO} ⁽³⁾	Internal supply voltage for the I/O banks	0.922	0.950	0.979	V
	For -1L (0.90V) devices: internal supply voltage for the I/O banks	0.880	0.900	0.920	V
	For -3 (1.0V only) devices: internal supply voltage for the I/O banks	0.970	1.000	1.030	V
V _{CCBRAM}	Block RAM supply voltage	0.922	0.950	0.979	V
	For -3 (1.0V only) devices: block RAM supply voltage	0.970	1.000	1.030	V
V _{CCAUX}	Auxiliary supply voltage	1.746	1.800	1.854	V
V _{CCO} ⁽⁴⁾⁽⁵⁾	Supply voltage for HR I/O banks	1.140	-	3.400	V
	Supply voltage for HP I/O banks	0.950	-	1.890	V
V _{CCAUX_IO} ⁽⁶⁾	Auxiliary I/O supply voltage	1.746	1.800	1.854	V
V _{IN} ⁽⁷⁾	I/O input voltage	-0.200	-	V _{CCO} + 0.200	V
	I/O input voltage (when V _{CCO} = 3.3V) for V _{REF} and differential I/O standards except TMDS_33 ⁽⁸⁾ .	-	0.400	2.625	V
I _{IN} ⁽⁹⁾	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	-	-	10.000	mA
V _{BATT} ⁽¹⁰⁾	Battery voltage	1.000	-	1.890	V
GTH and GTY Transceivers					
V _{MGTAVCC} ⁽¹¹⁾	Analog supply voltage for the GTH and GTY transceivers ⁽¹⁰⁾	0.970	1.000	1.030	V
V _{MGTAVTT} ⁽¹¹⁾	Analog supply voltage for the GTH and GTY transmitter and receiver termination circuits	1.170	1.200	1.230	V
V _{MGTVCCAUX} ⁽¹¹⁾	Auxiliary analog QPLL voltage supply for the transceivers	1.750	1.800	1.850	V



FPGA_XCKU040FFVA1156

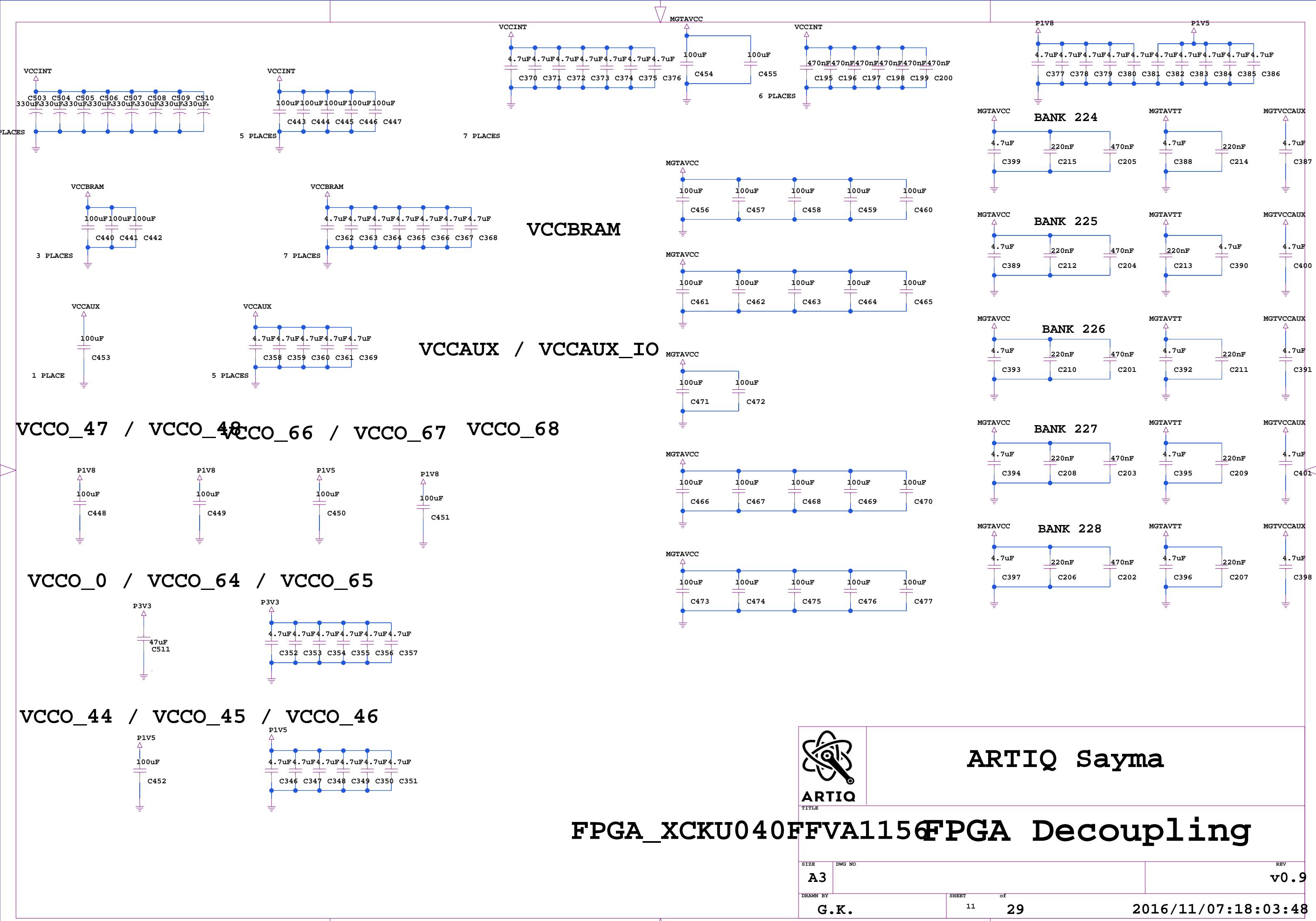
ARTIQ Sayma

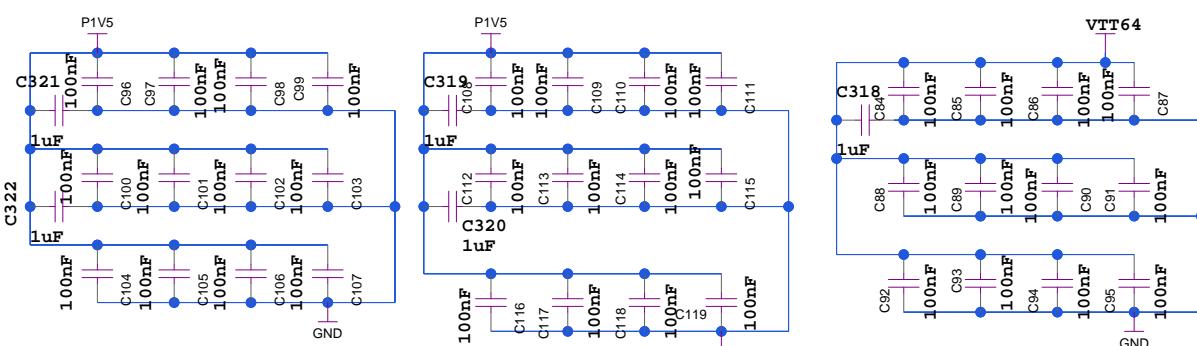
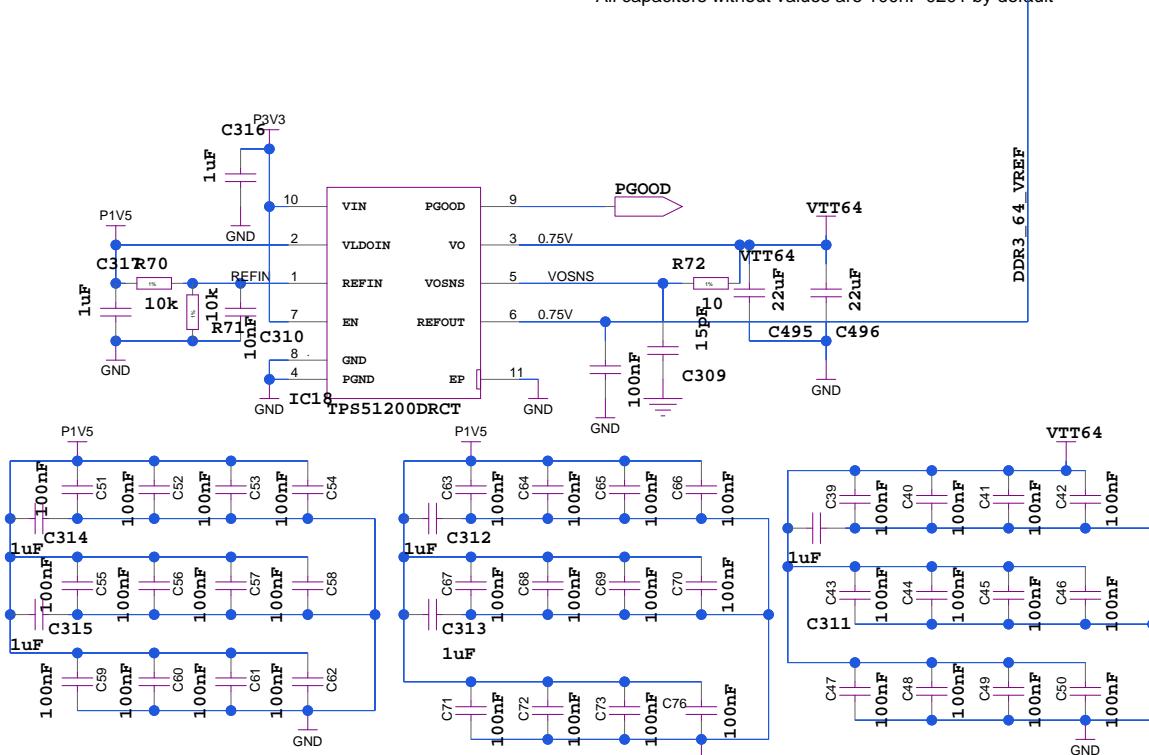
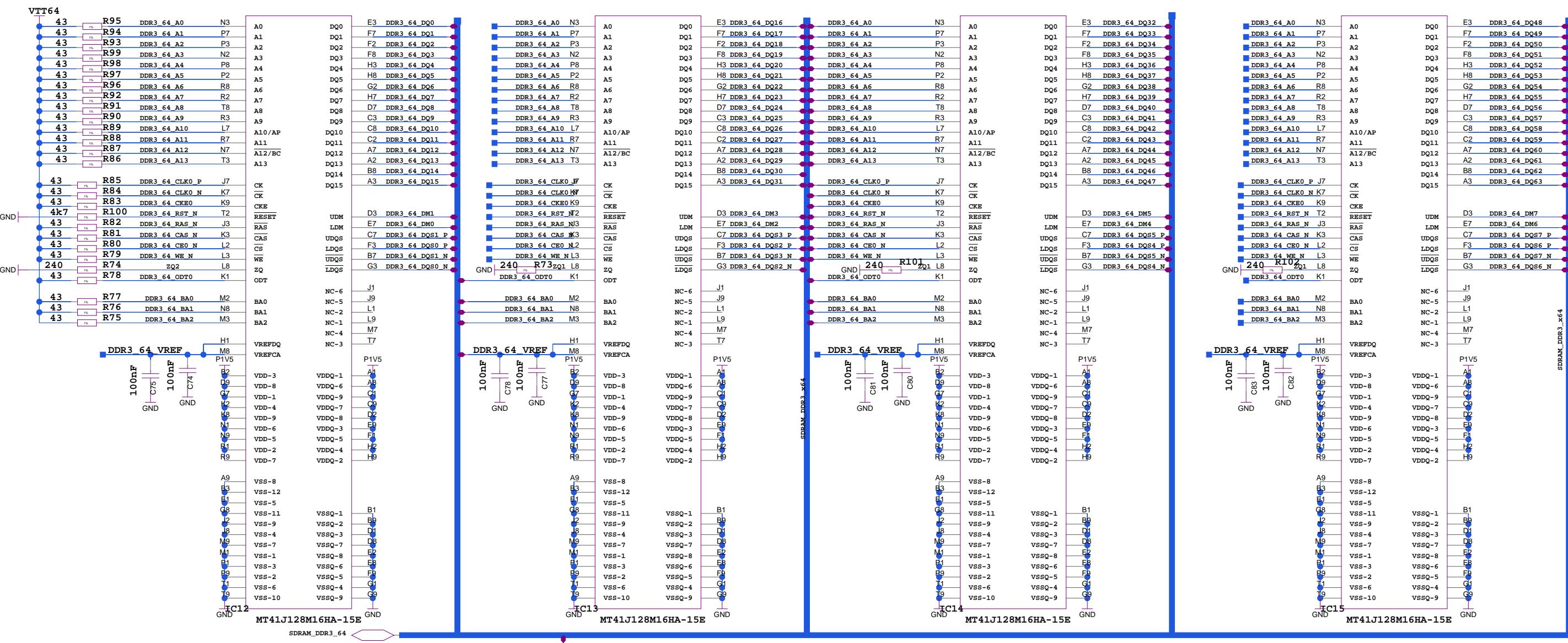
FPGA Power



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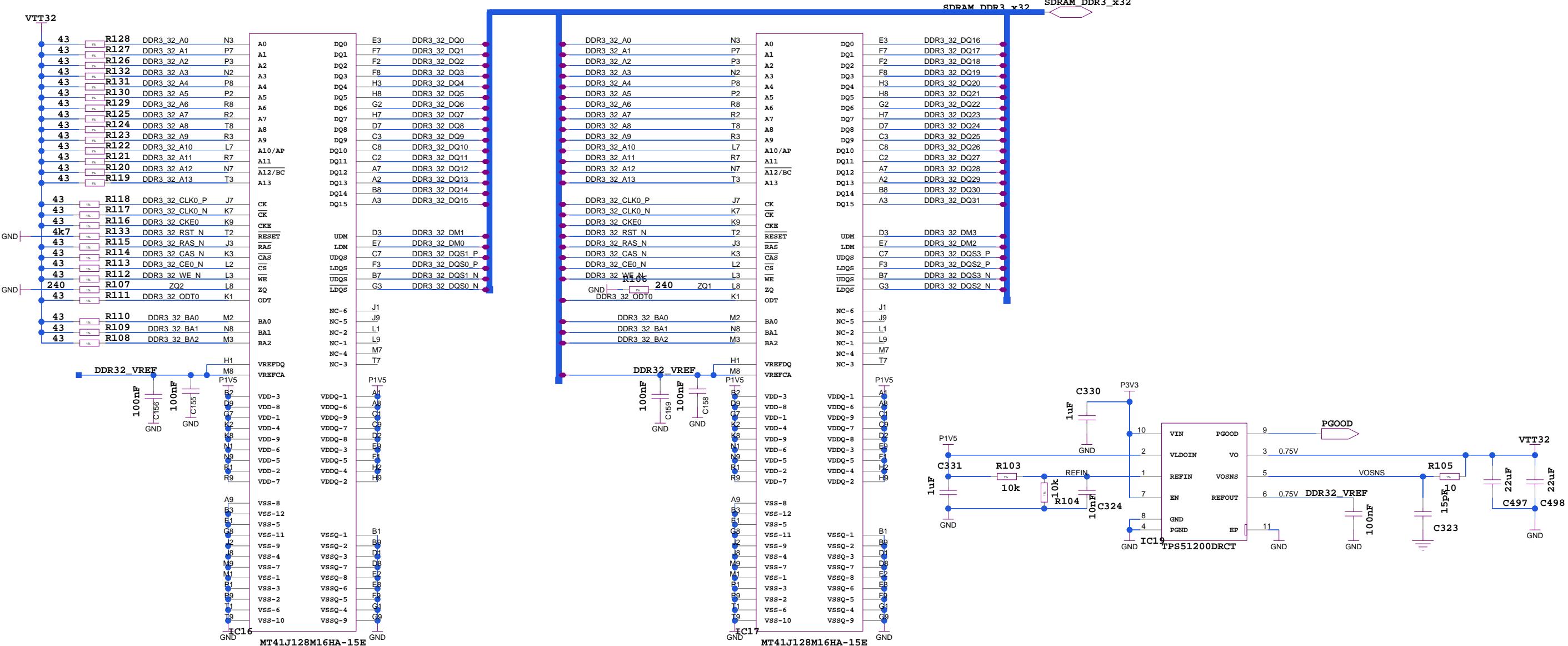
FPGA_XCKU040FFVA1156 FPGA GND NC



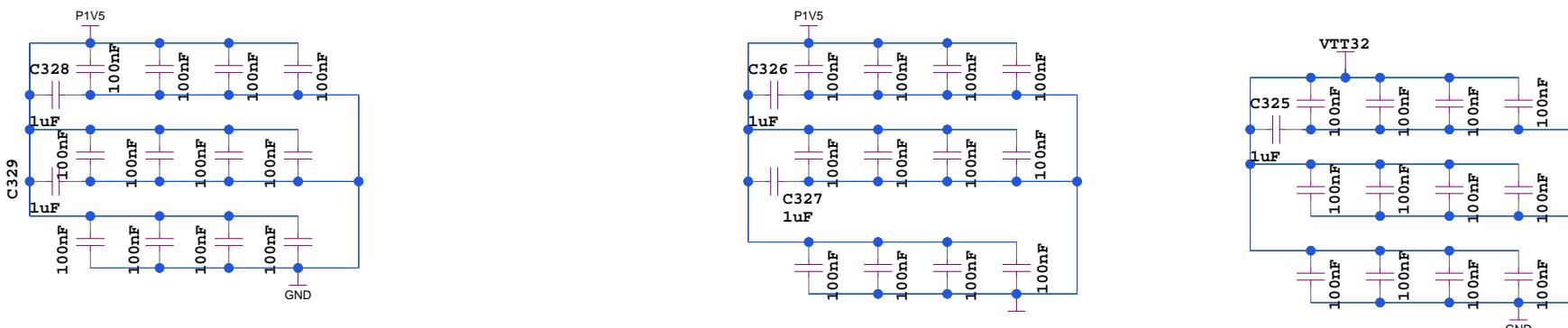


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SDRAM_DDR3_4x16



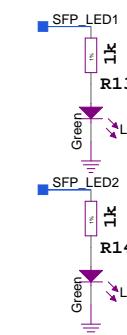
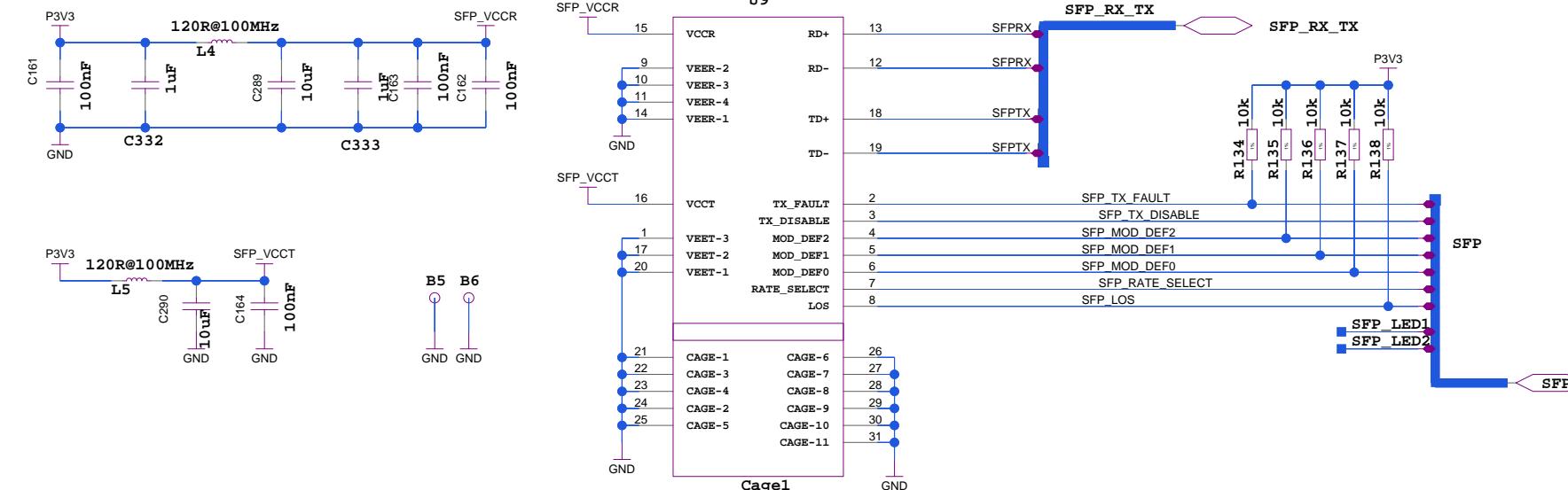
All capacitors without values are 100nF 0201 by default



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SDRAM DDR3 2x16

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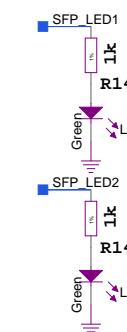
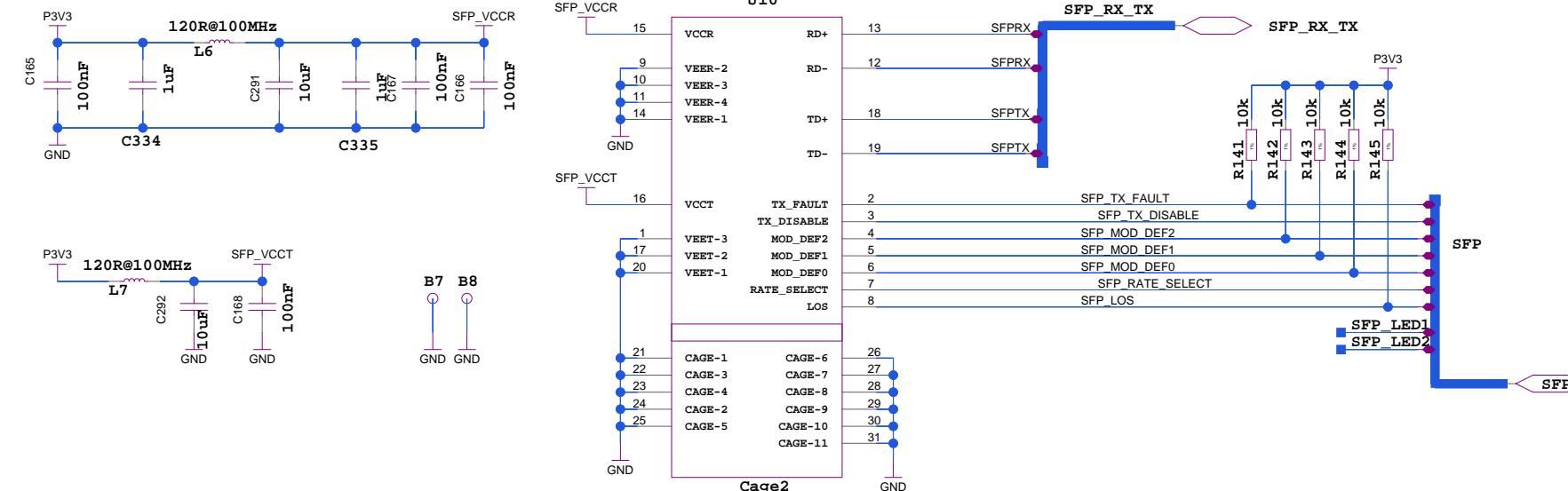


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SFP

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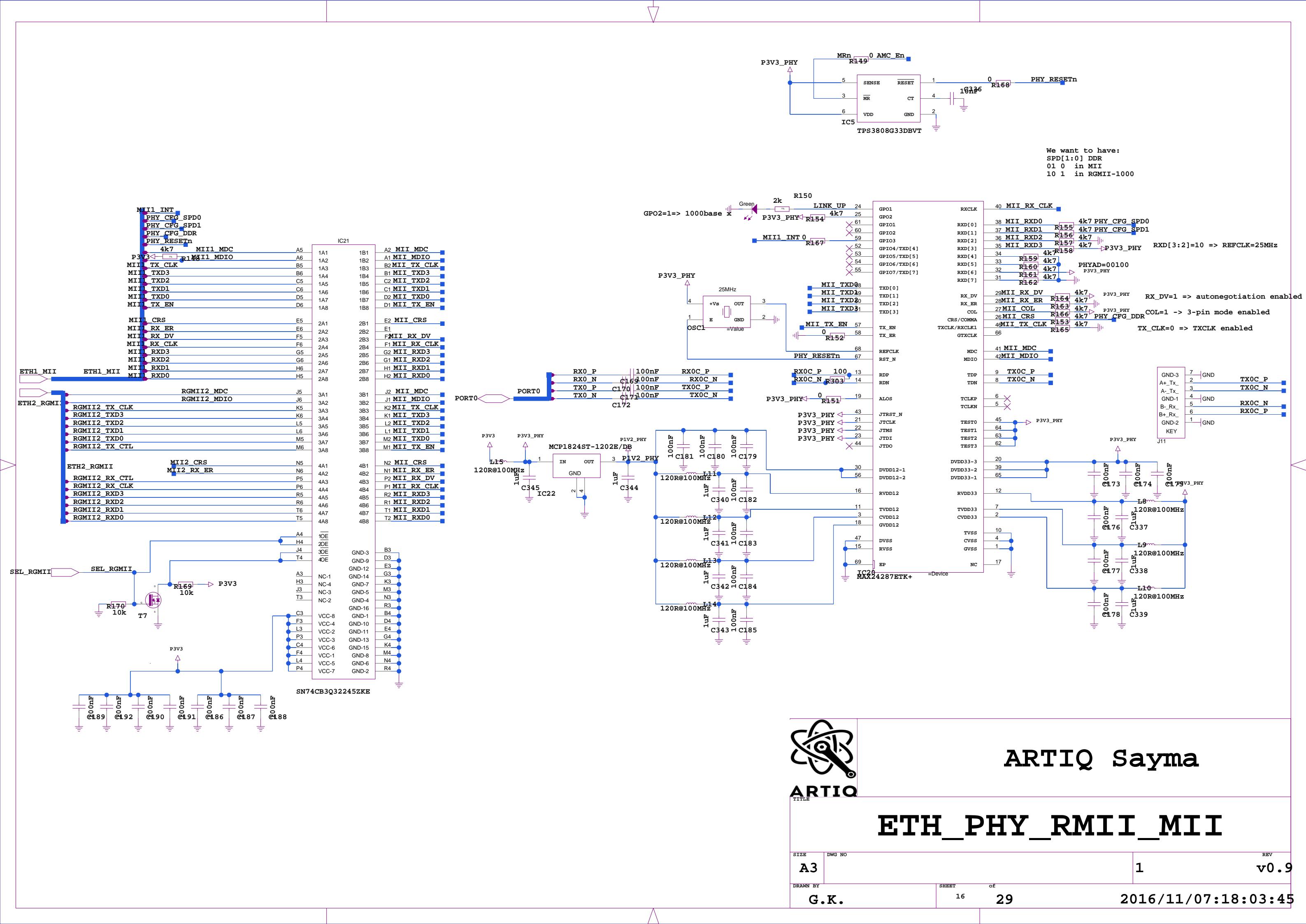
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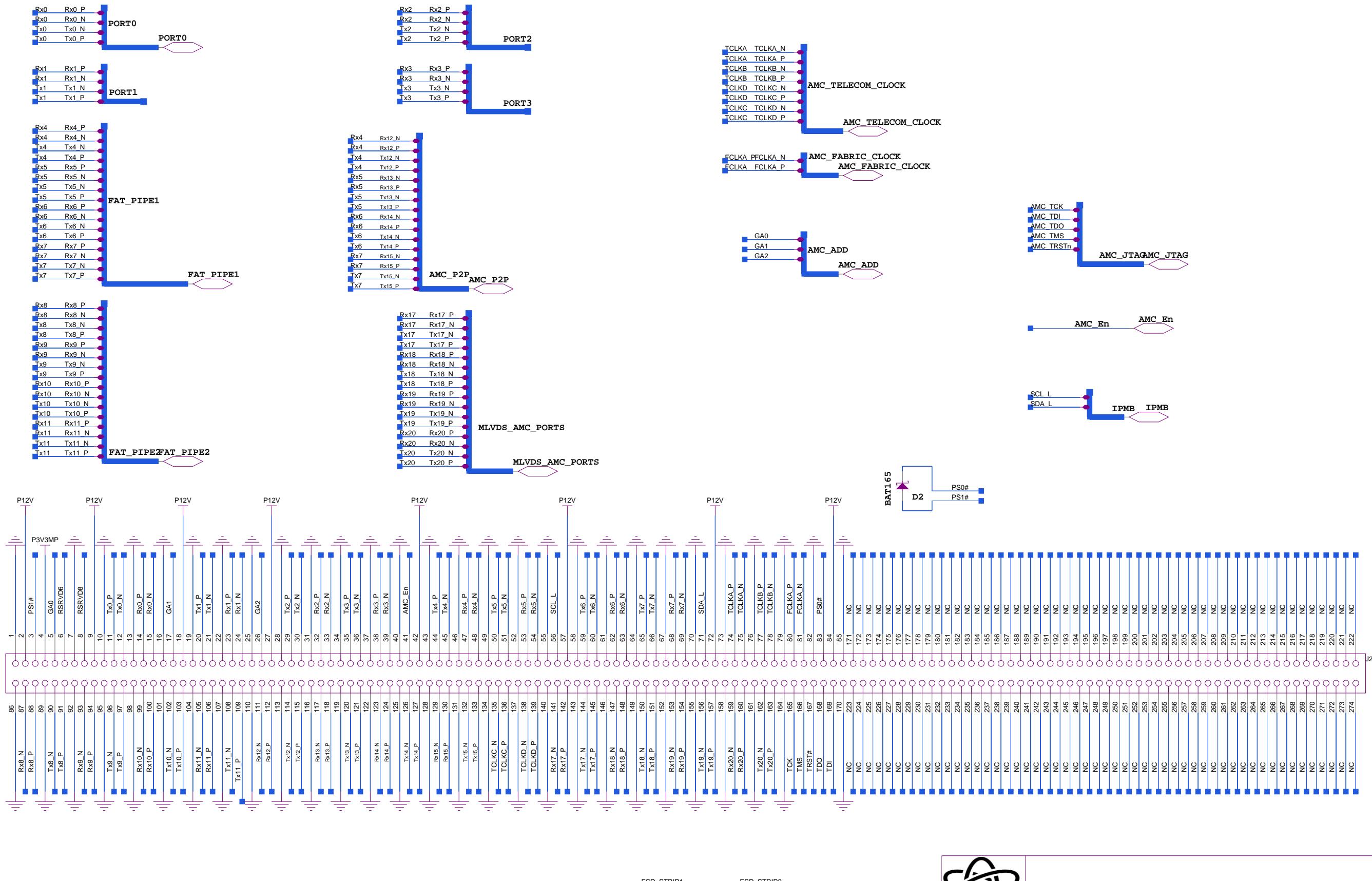


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SFP

SIZE	DWG NO	REV	
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G.K.	15	29	2016/11/07:18:03:56





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AMC_Connector

SIZE	DWG NO	REV
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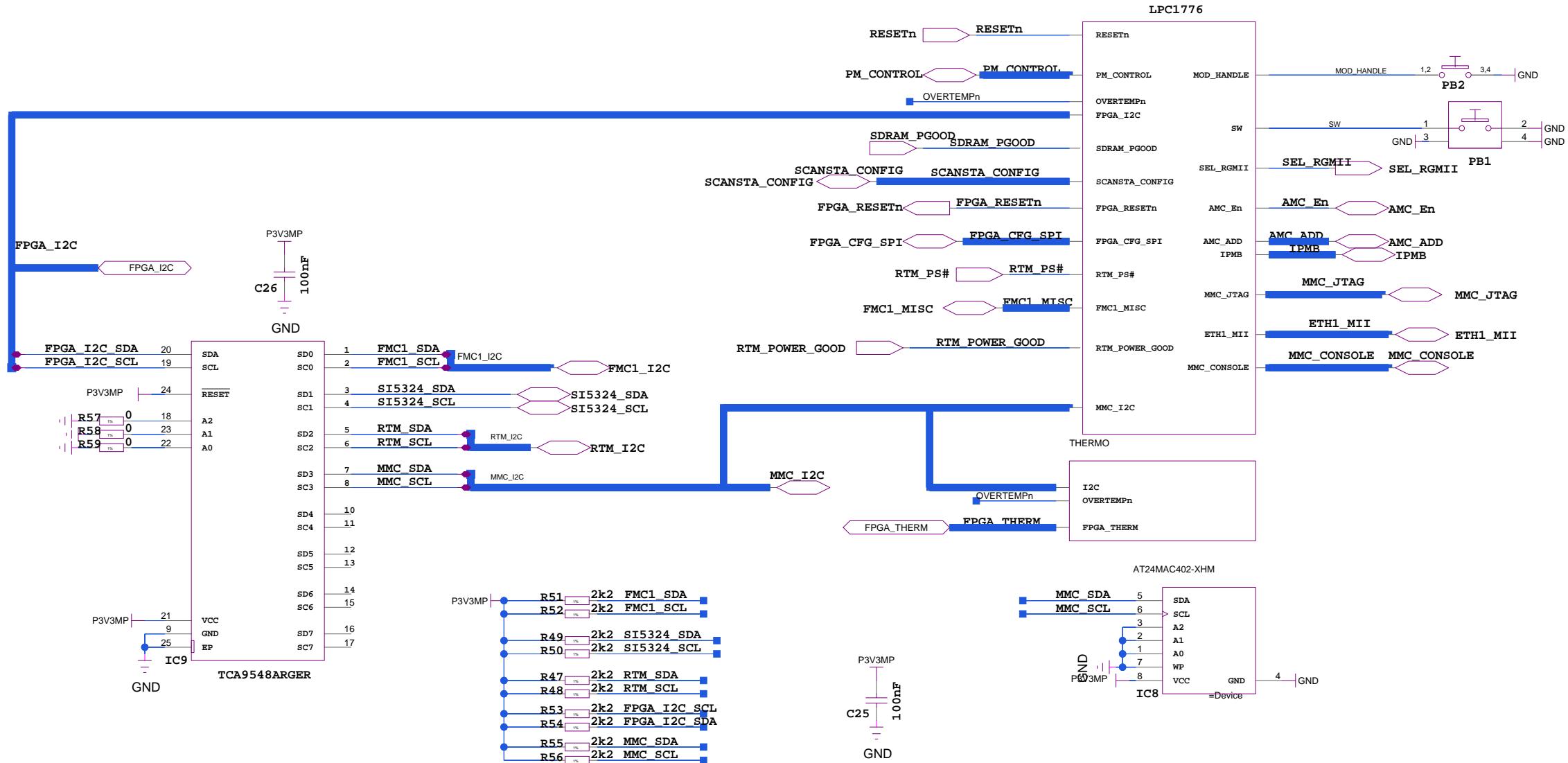
(http://ohwr.org/CERNOHL). The documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

- Dimensions are in MM, nominal values used
- Component height rule derived from AMC Base Specification.PDF, Page 62
- The two corners of outline near the edge-connector are approximated, see AMC Base Specification.PDF, Page 59
- Stackup is not specified in AMC Base Specification.PDF or implemented in this template.

REV

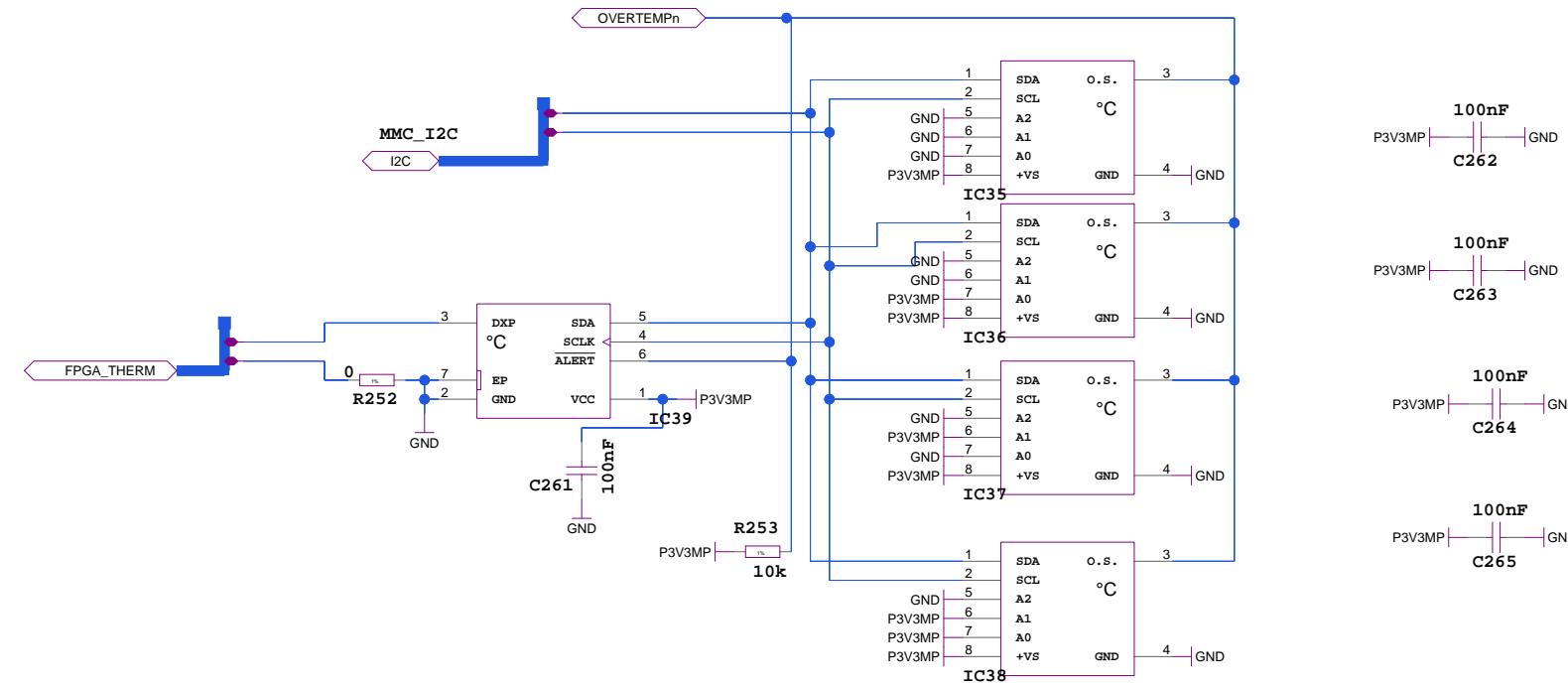
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IPMI



100nF
P3V3MP || GND
C262

100nF
P3V3MP || GND
C263

100nF
P3V3MP || GND
C264

100nF
P3V3MP || GND
C265



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Thermometers

TITLE

ARTIQ

SIZE DWG NO

A3

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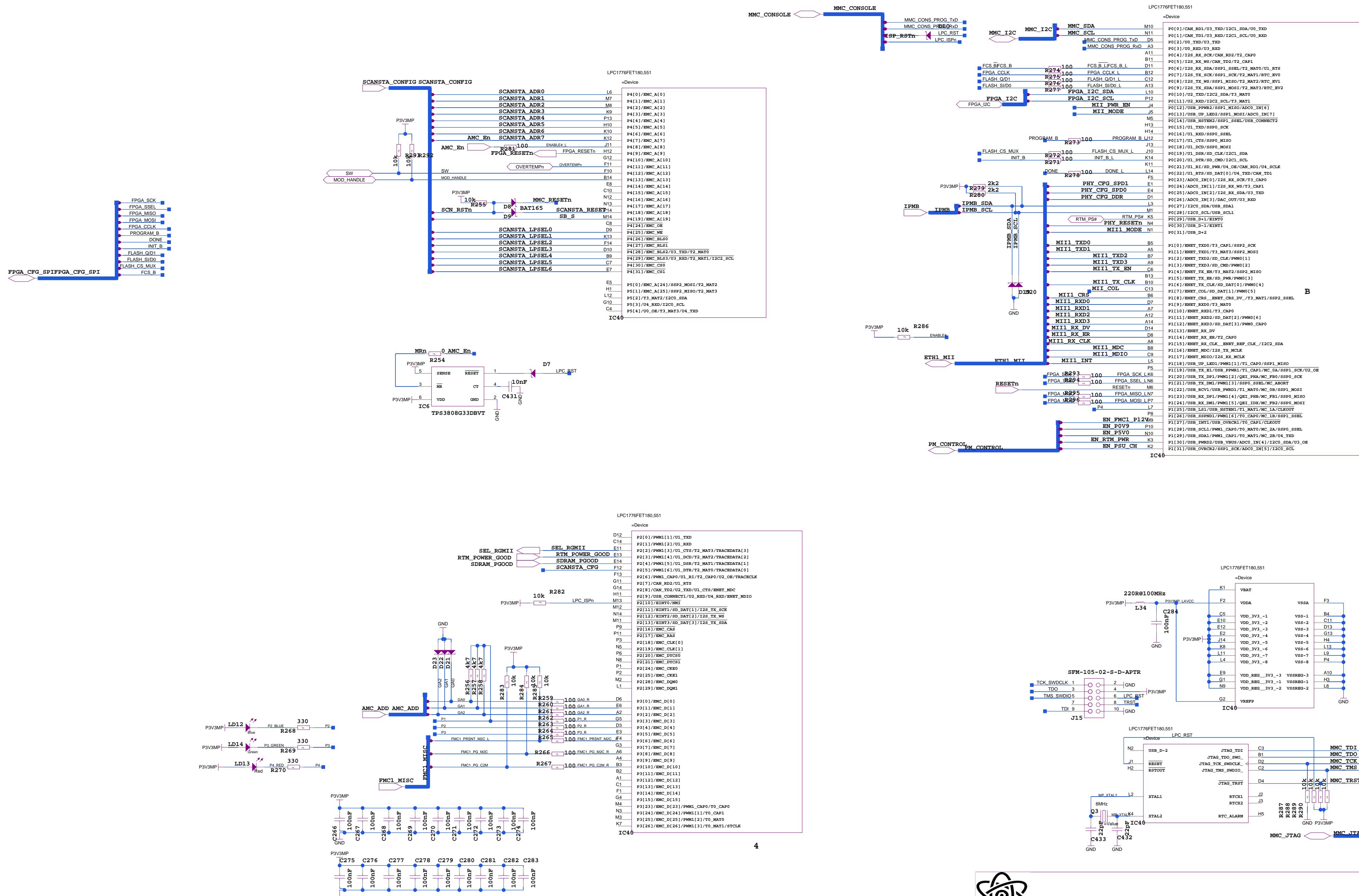
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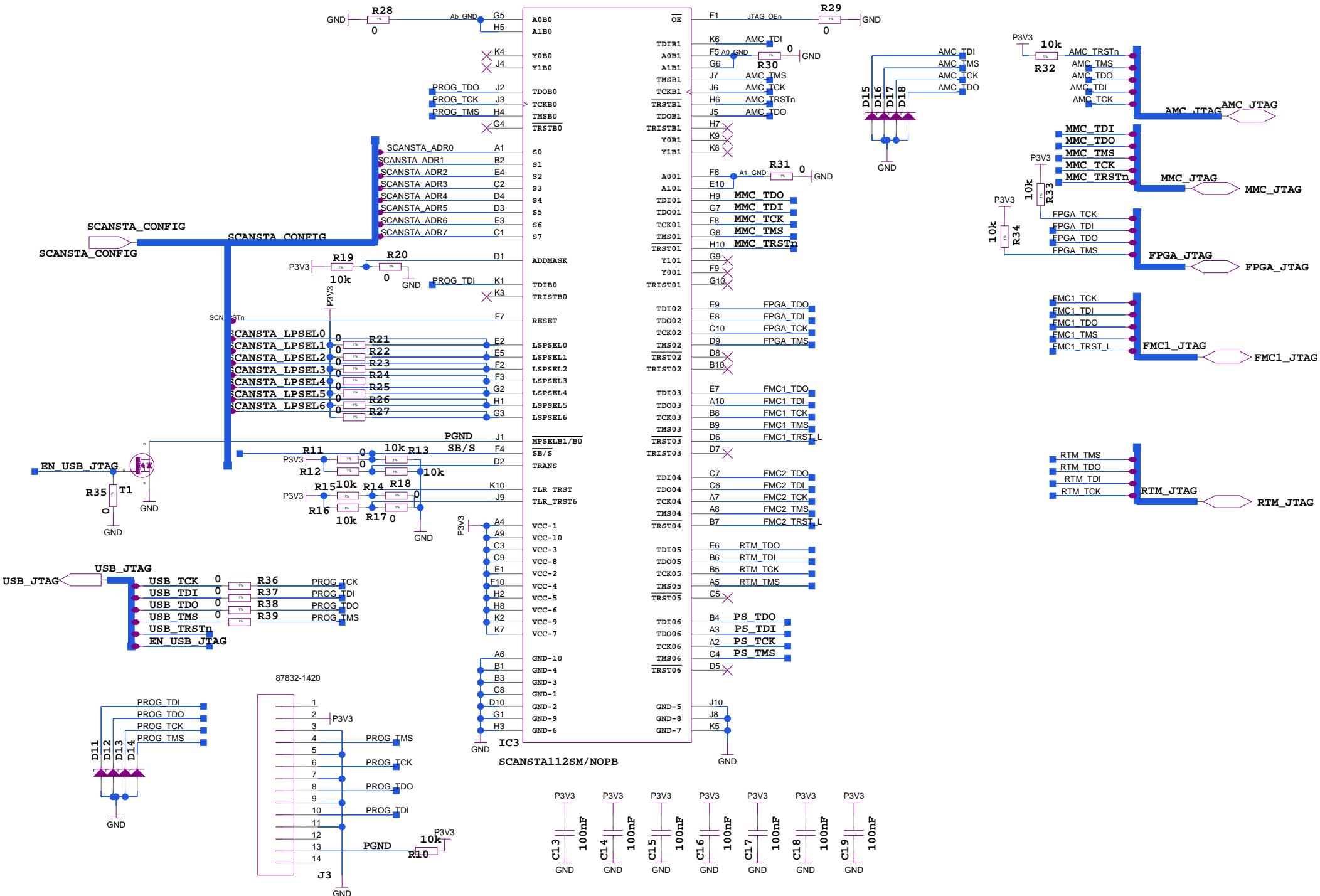
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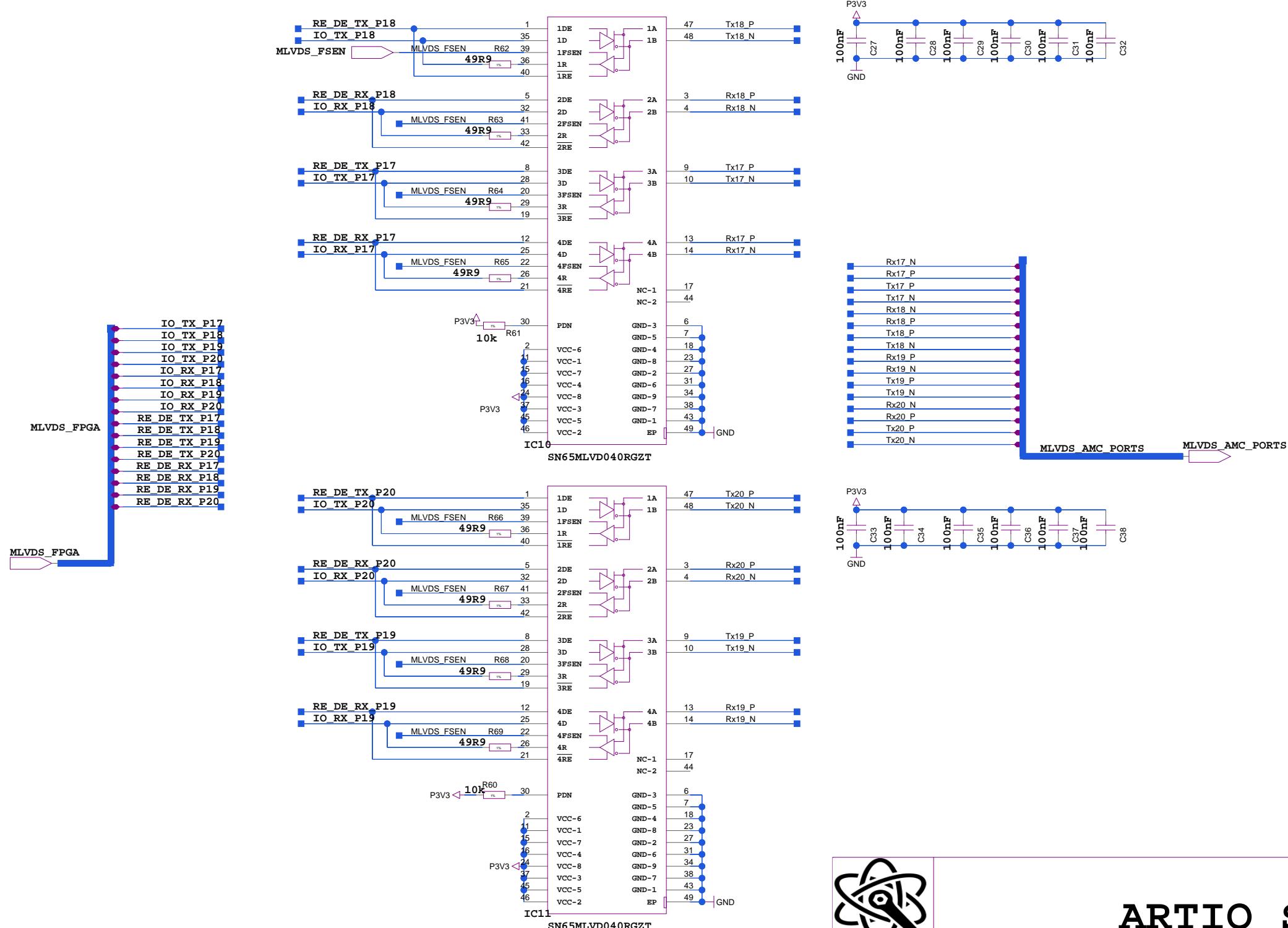
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JTAG_Configuration

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G.K.	21	29



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M-LVDS_PHY

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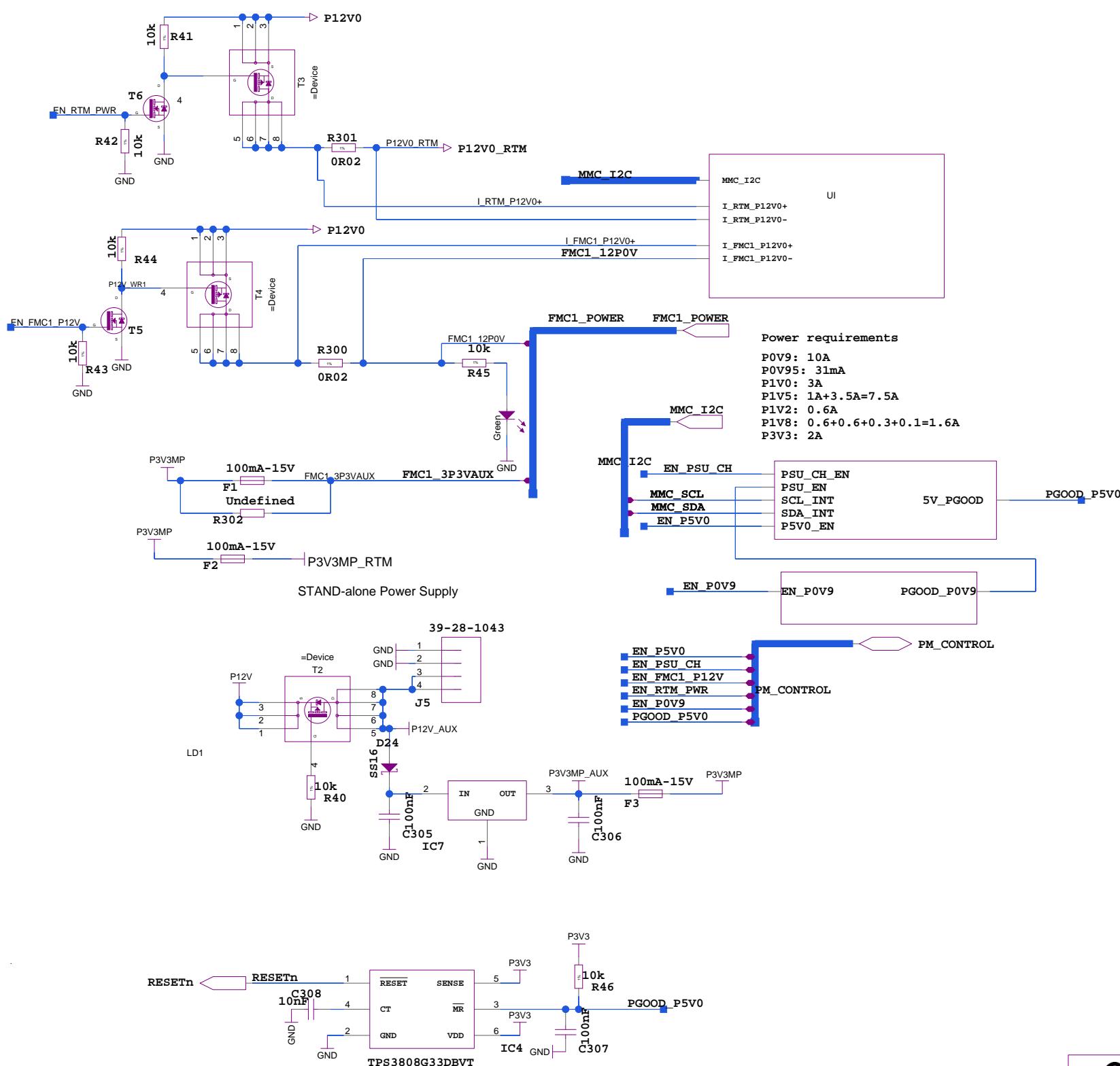


Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V _{CCINT}	Internal supply voltage	0.922	0.950	0.979	V
V _{CCINT}	For -1L (0.90V) devices: internal supply voltage	0.880	0.900	0.920	V
V _{CCINT}	For -3 (1.0V only) devices: internal supply voltage	0.970	1.000	1.030	V
V _{CCBRAM}	Internal supply voltage for the I/O banks	0.922	0.950	0.979	V
V _{CCCAUX}	For -1L (0.90V) devices: internal supply voltage for the I/O banks	0.880	0.900	0.920	V
V _{CCIO} ⁽⁴⁾⁽⁵⁾	Block RAM supply voltage	0.922	0.950	0.979	V
V _{CCIO} ⁽⁴⁾⁽⁵⁾	For -3 (1.0V only) devices: block RAM supply voltage	0.970	1.000	1.030	V
V _{CCIO} ⁽⁶⁾	Auxiliary supply voltage	1.746	1.800	1.854	V
V _{CCIO} ⁽⁶⁾	Supply voltage for HP I/O banks	1.140	-	3.400	V
V _{CCIO} ⁽⁶⁾	Auxiliary I/O supply voltage	0.950	-	1.890	V
V _{IN} ⁽⁷⁾	I/O input voltage	-0.200	-	V _{CCO} + 0.200	V
V _{IN} ⁽⁷⁾	I/O input voltage when V _{CCO} = 3.3V for V _{GEF} and differential I/O standards except TMDS_33 ⁽⁸⁾	-	0.400	2.625	V
I _H ⁽⁹⁾	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	-	-	10.000	mA
V _{BATT} ⁽¹⁰⁾	Battery voltage	1.000	-	1.890	V
GTH and GTY Transceivers					
V _{MGTAVCC} ⁽¹¹⁾	Analog supply voltage for the GTH and GTY transceivers ⁽¹²⁾	0.970	1.000	1.030	V
V _{MGTAVTT} ⁽¹¹⁾	Analog supply voltage for the GTH and GTY transmitter and receiver termination circuits	1.170	1.200	1.230	V
V _{MGTVAUX} ⁽¹¹⁾	Auxiliary analog QPLL voltage supply for the transceivers	1.750	1.800	1.850	V
Symbol Description Min Typ Max Units					
Y_{SYMONCAL} ⁽¹³⁾	Analog supply voltage for the resistor calibration circuit of the GTH and GTY transceiver columns	1.170	1.200	1.230	V
SYMON	SYMON supply relative to GNDADC	1.746	1.800	1.854	V
V _{REF}	Externally supplied reference voltage	1.200	1.250	1.300	V
Temperature					
Junction temperature operating range for commercial (C)	0	-	85	°C	
Junction temperature operating range for extended (E)	0	-	100	°C	
Junction temperature operating range for industrial (I)	-40	-	100	°C	

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}/V_{CCINT}_IO/V_{CCBRAM}/V_{CCAU}/V_{CCAU}_IO and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-state at power-on. The recommended power-down sequence is V_{CCINT}_IO/V_{CCAU}/V_{CCAU}/V_{CCO}. If the I/Os are 3-state at power-on, they can be powered by the same supply and ramped simultaneously. V_{CCINT}_IO must be connected to V_{CCINT}. If V_{CCAU}/V_{CCAU}_IO and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAU} and V_{CCAU}_IO must be connected together. When the current minimums are met, the device powers up after V_{CCINT}/V_{CCINT}_IO/V_{CCBRAM}/V_{CCAU}/V_{CCAU}_IO and V_{CCO} supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied.

V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing recommendations. The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, V_{MGTAVCC}, V_{MGTAVTT} OR V_{MGTAVCC}, V_{CCINT}, V_{MGTAVTT}. There is no recommended sequencing for V_{MGTAVCC}, V_{MGTAVTT} or V_{MGTAVCC}, V_{MGTAVTT}. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from V_{MGTAVTT} can be higher than specifications during power-up and power-down.

Power Supply			
Source	Voltage	Total (A)	
V _{CCINT}	0,900	9,165	
V _{CCINT} _IO	0,900	0,620	
V _{CCBRAM}	0,950	0,031	
V _{CCAU}	1,800	0,660	
V _{CCAU} _IO	1,800	0,546	
V _{CCO} 3.3V	3,300	0,000	
V _{CCO} 2.5V	2,500		
V _{CCO} 1.8V	1,800	0,380	
V _{CCO} 1.5V	1,500	0,936	
V _{CCO} 1.35V	1,350		
V _{CCO} 1.2V	1,200		
V _{CCO} 1.0V	1,000		
MGT _V _{CCAU}	1,800	0,081	
MGT _V _{CC}	1,000	3,038	
MGT _V _{TT}	1,200	0,592	
	-		
V _{CCADC}	1,800	0,014	

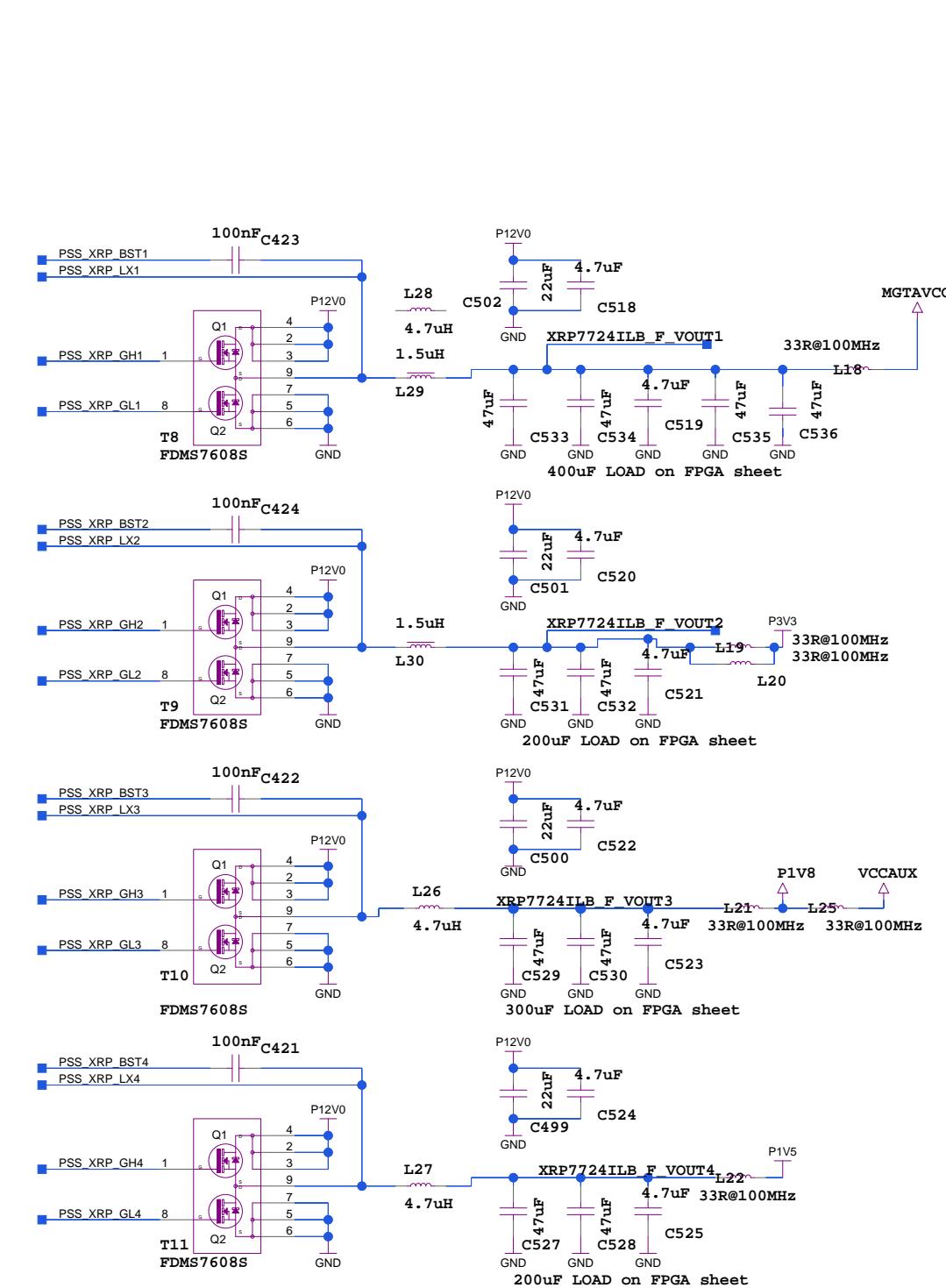
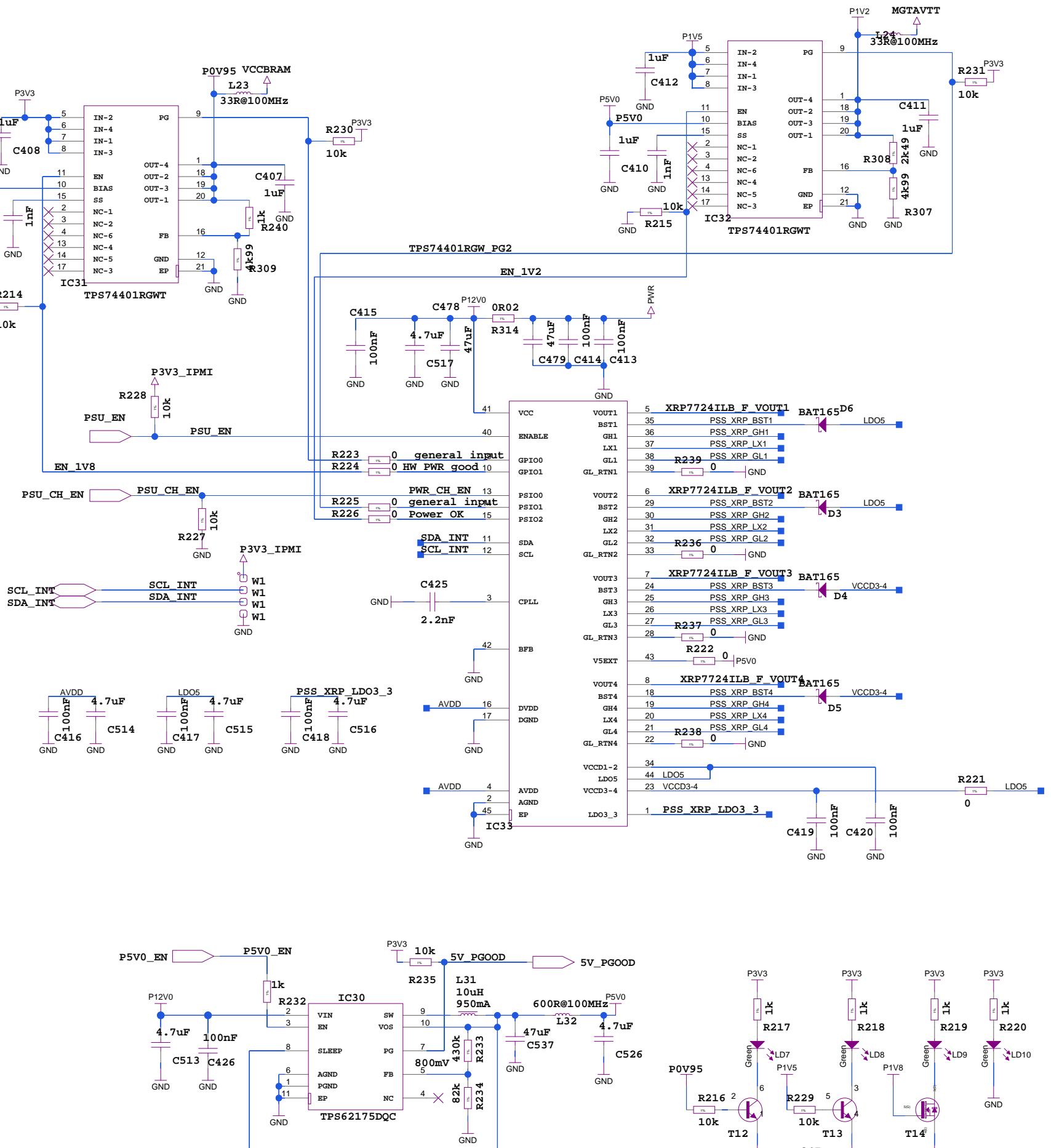


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POWER_Management

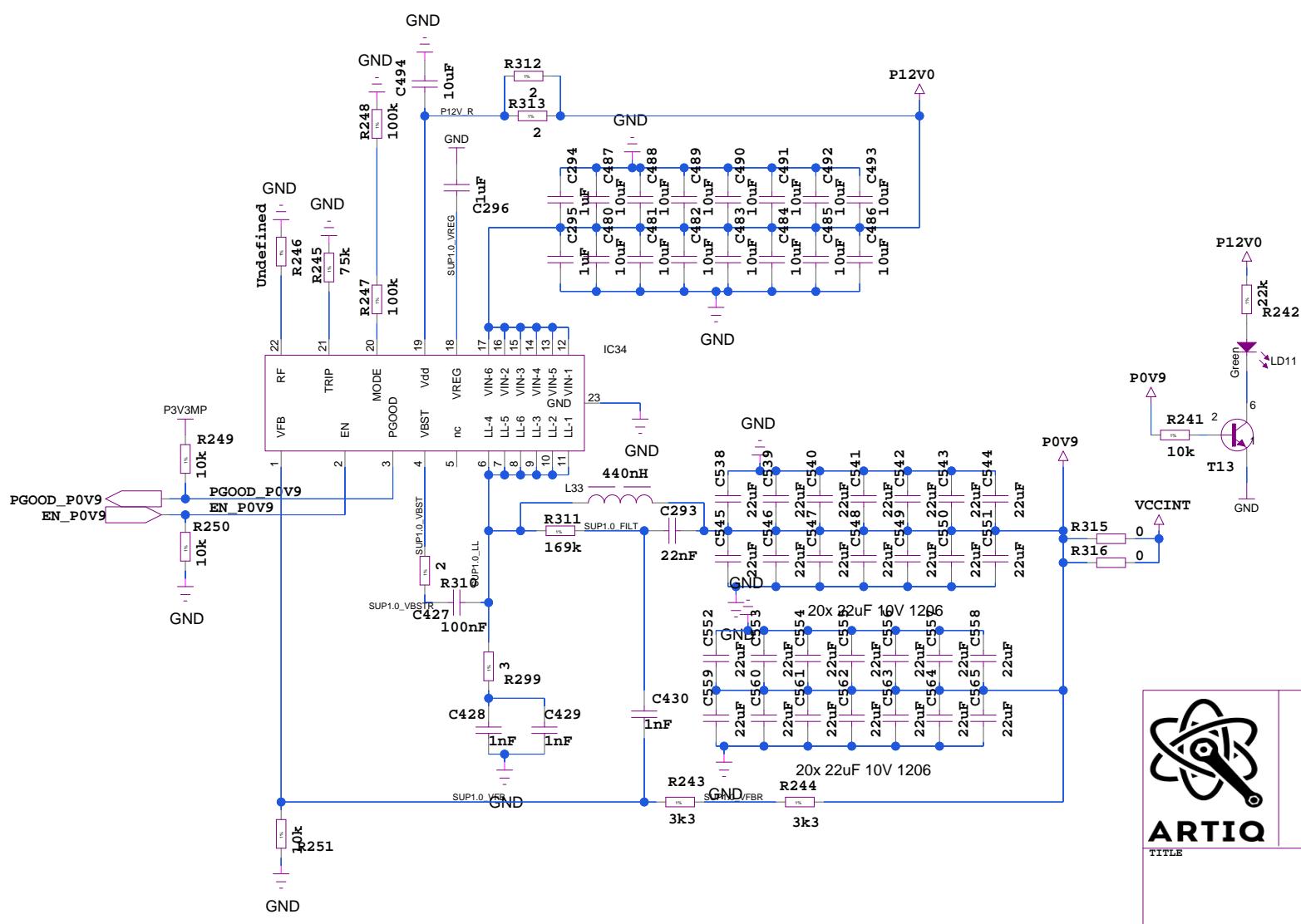
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of			
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PWR_DC_DC_EXAR

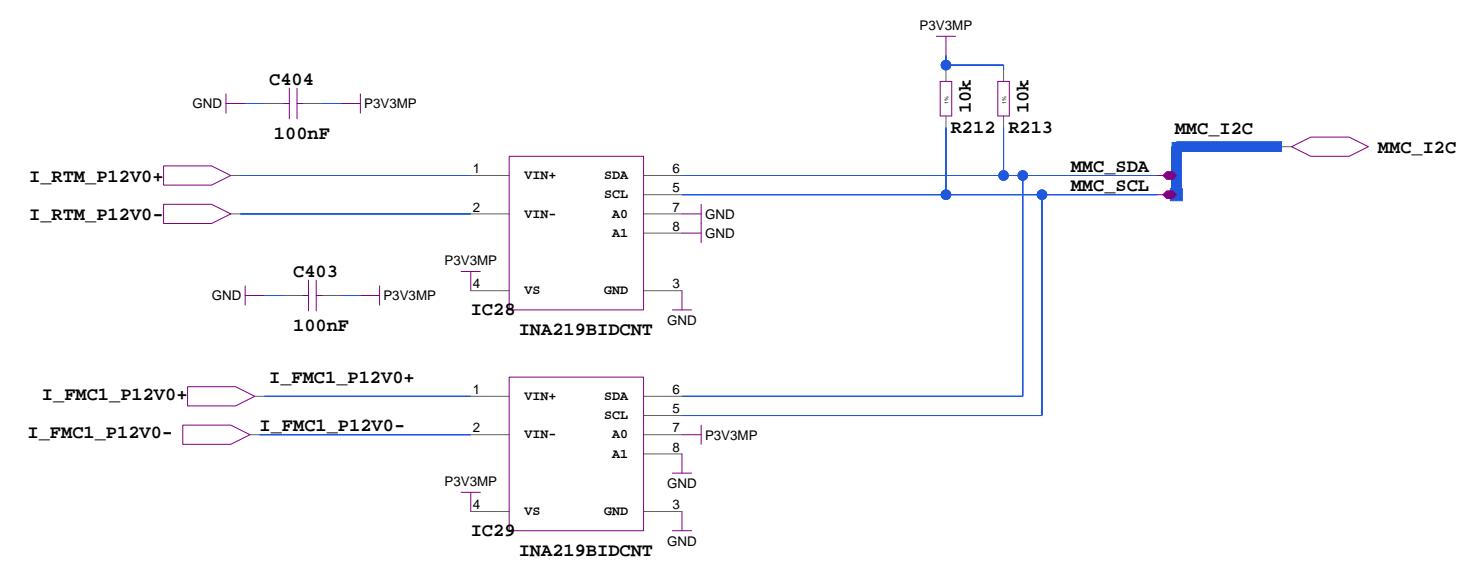
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G.K.	24	29	2016/11/07:18:03:43



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PWR_0V9

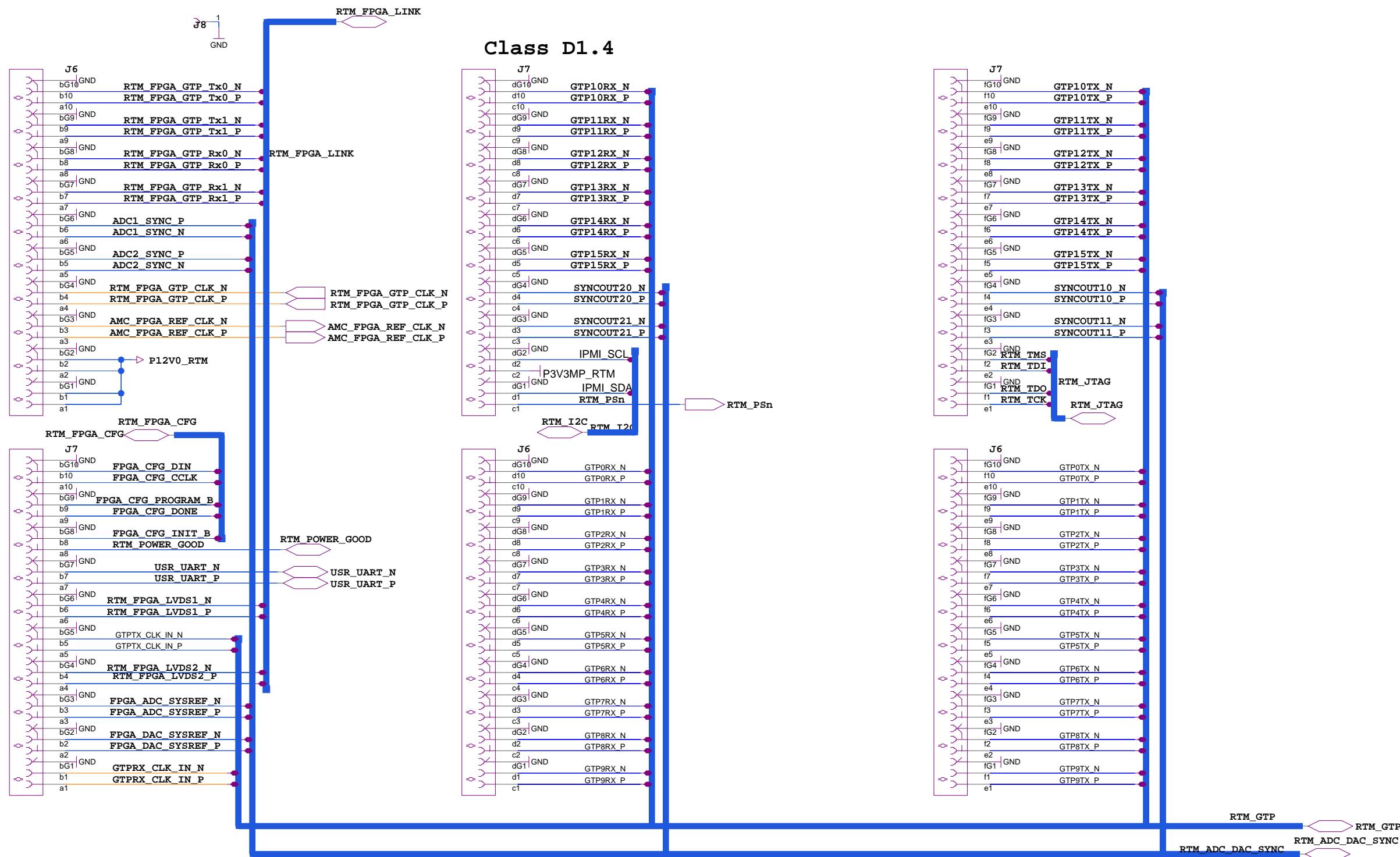
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UI_mon

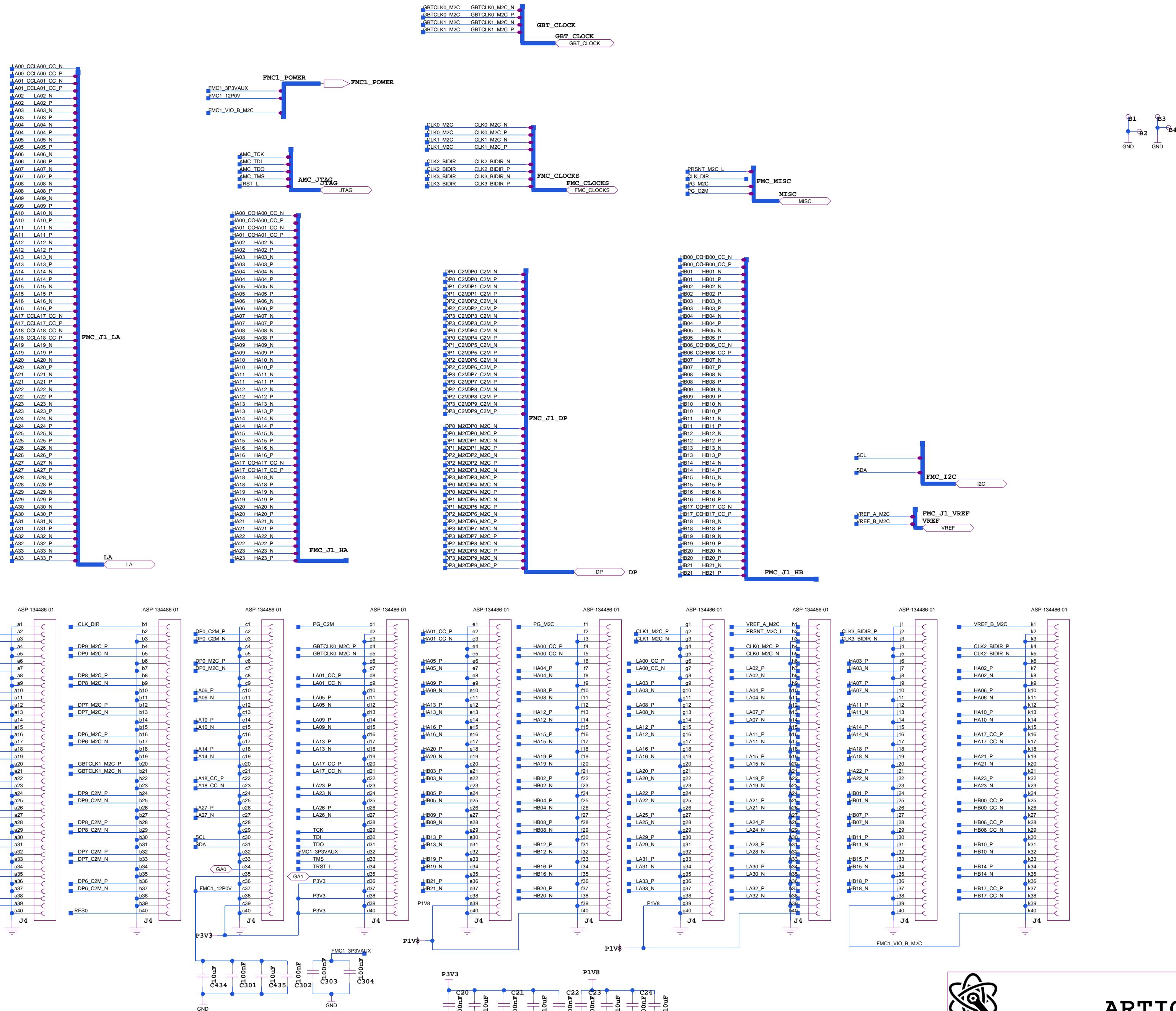
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RTM_CON

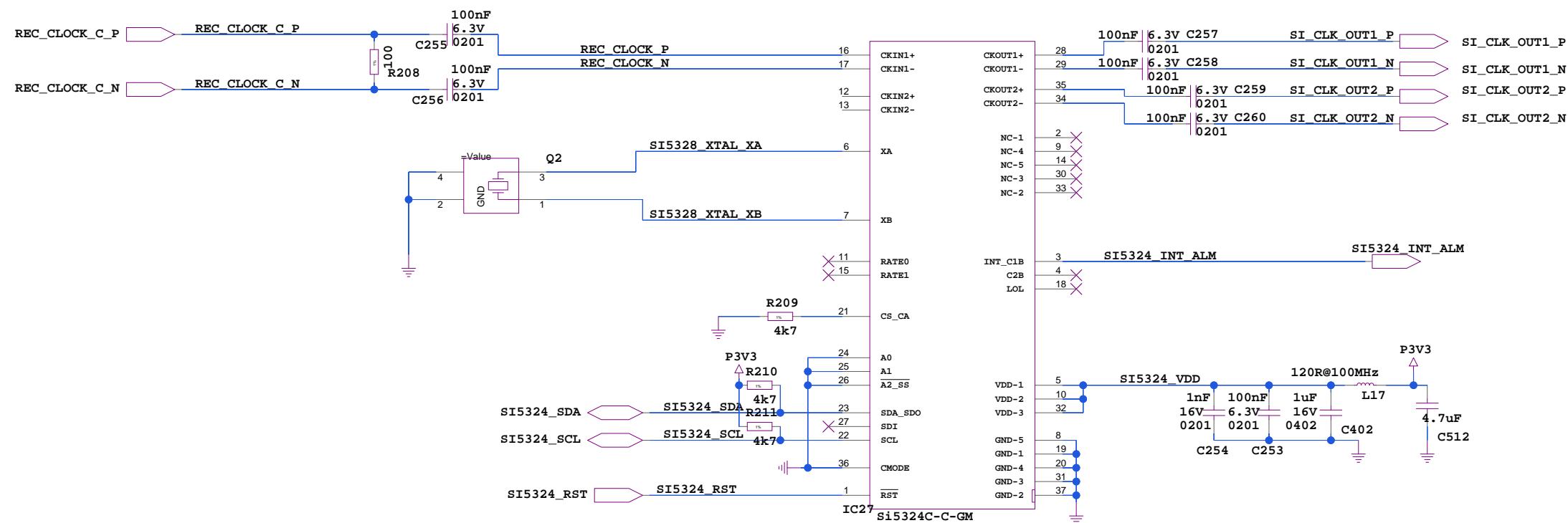
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G.K.	27	29	2016/11/07:18:03:44



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FMC_connector

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TITLE

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SI5324_CLK_RECOVERY

SIZE DWG NO

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1

REV
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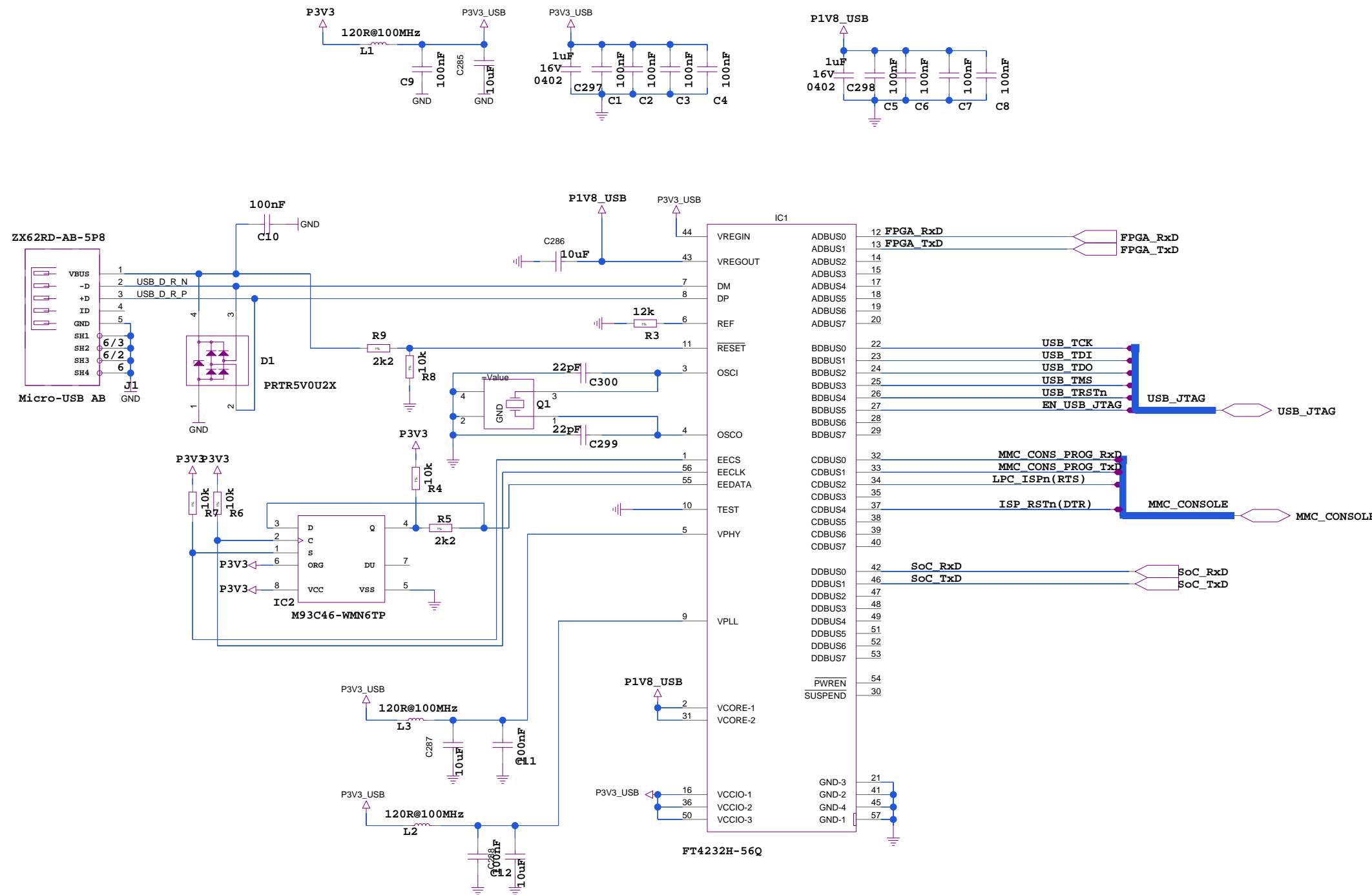
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supply from USB to enable MMC at 3.3V MP



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USB_SERIAL_QUAD