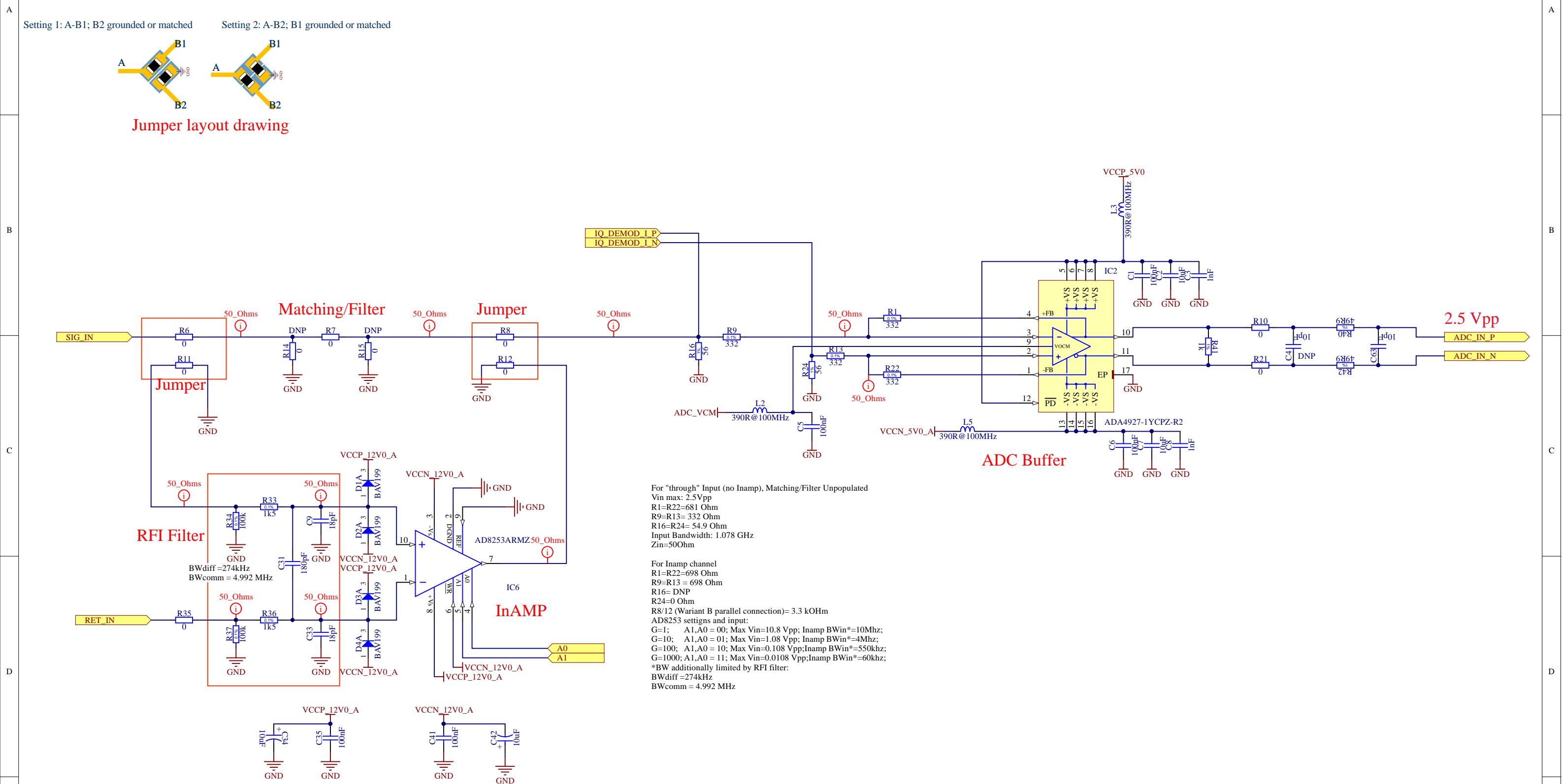
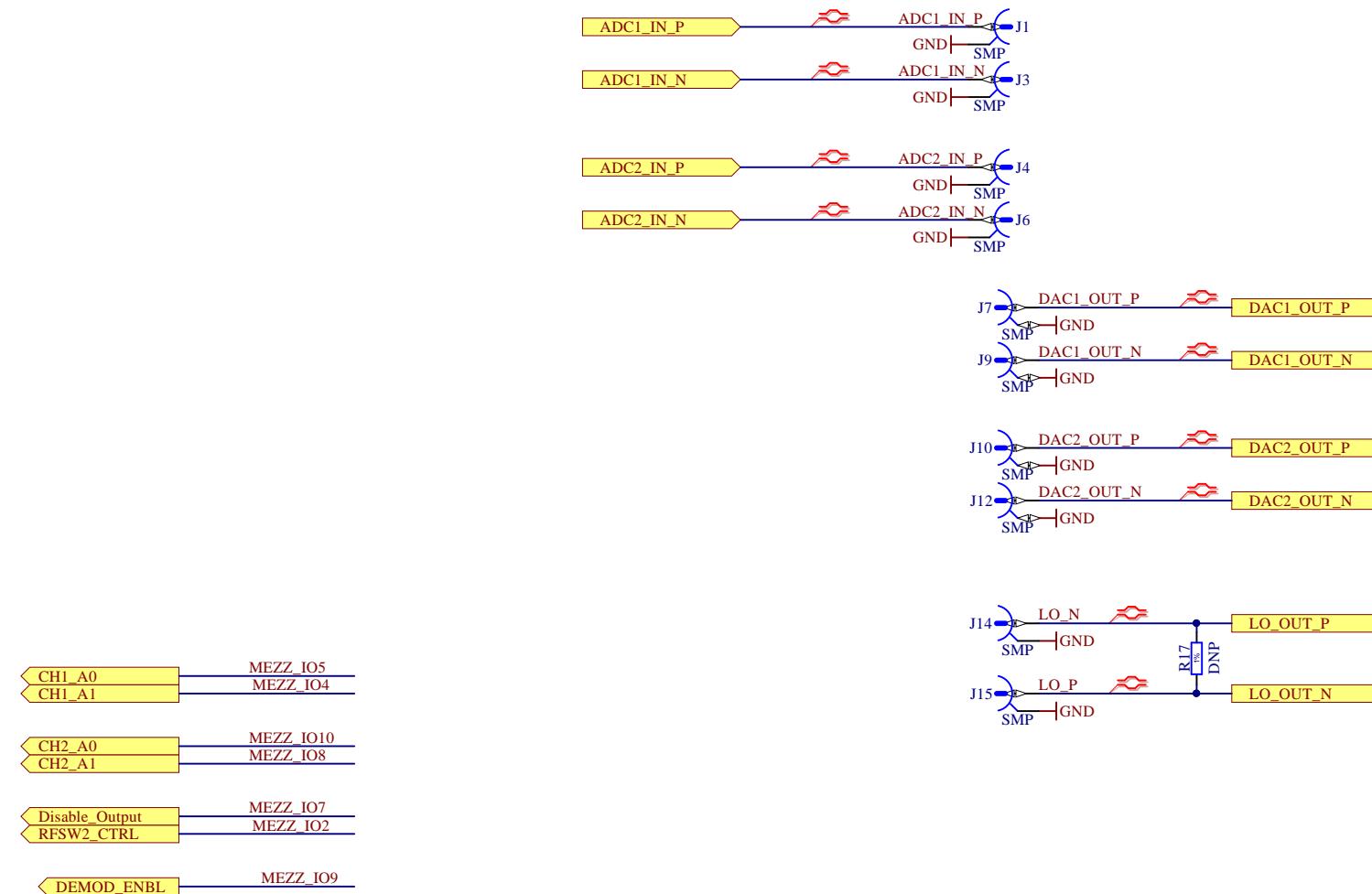


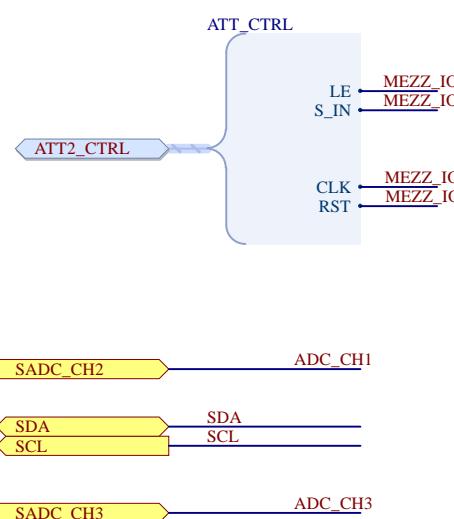
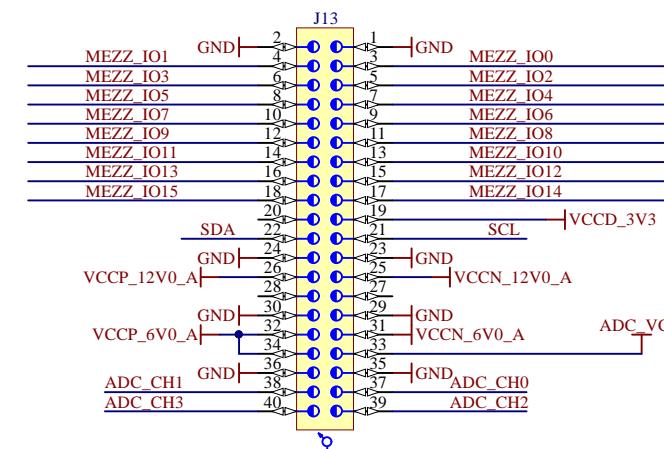
Project/Equipment		ADC/DAC MEZZANINE	
Document		Designer	SBH
		Drawn by	SBH
		Check by	-
		Last Mod.	2017-08-01
		File	nanoga_mezz_top.SchDoc
		Print Date	2017-08-01 16:12:21
		Sheet	1 of 1
Warsaw University of Technology ISE Nowowiejska 15/19		ARTIQ	Size A3 Rev -



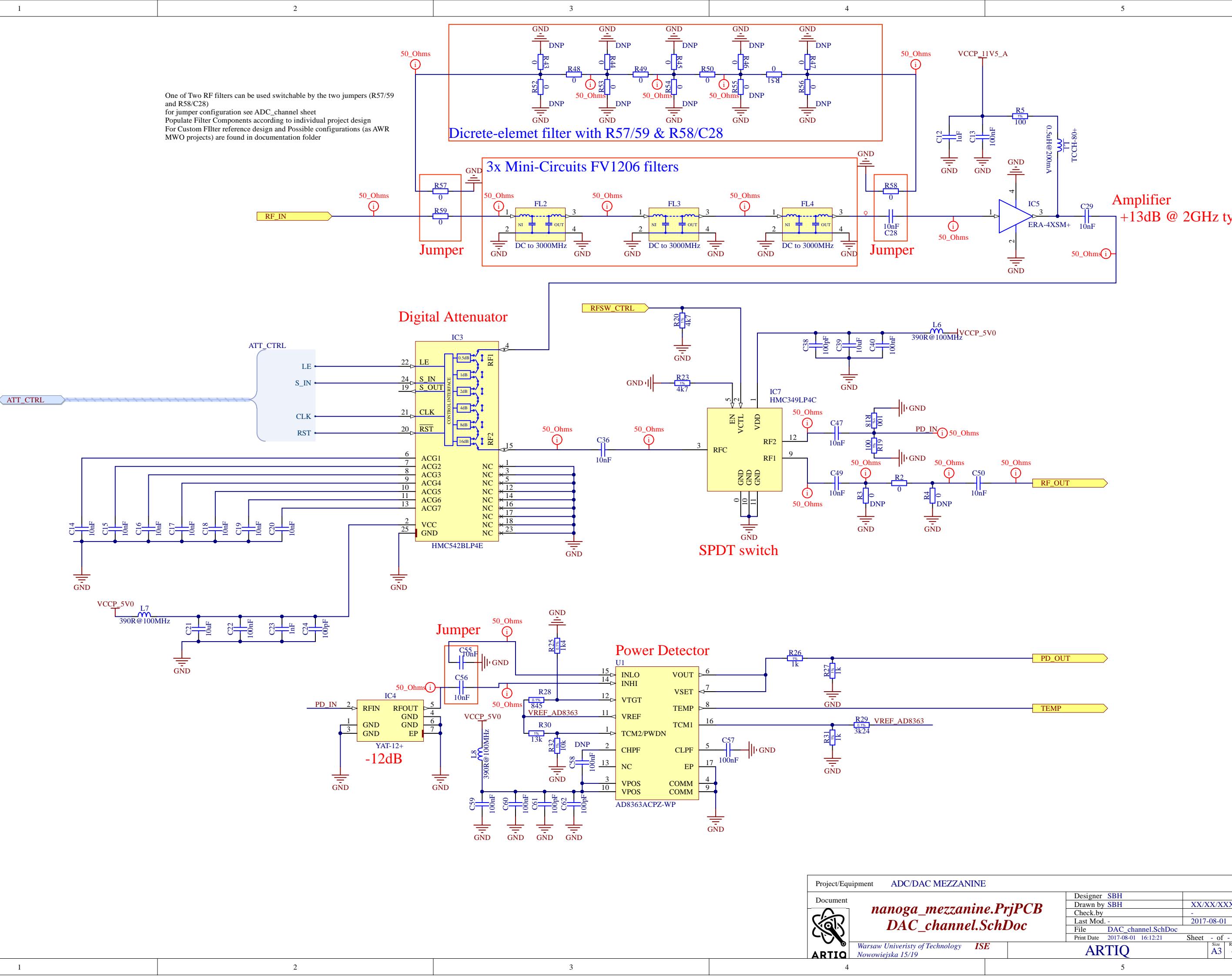
Board-2-Board Analog Connectors



Board-2-Board Digital Connector

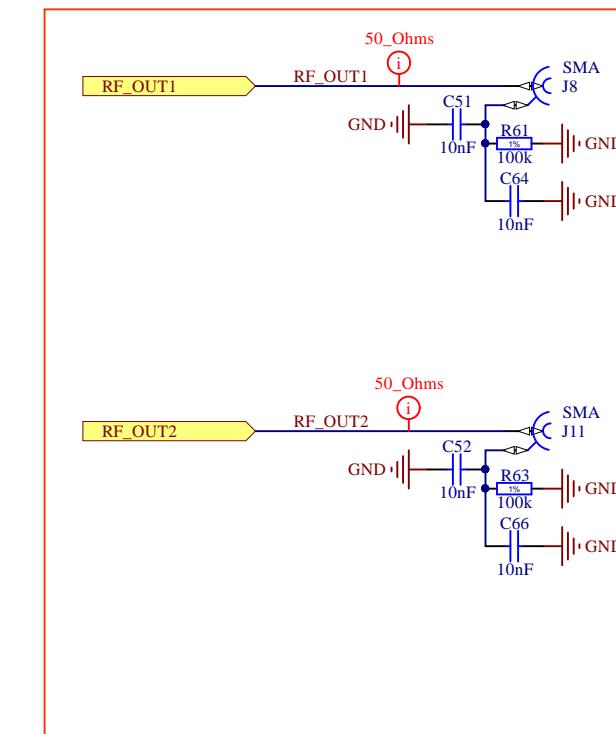
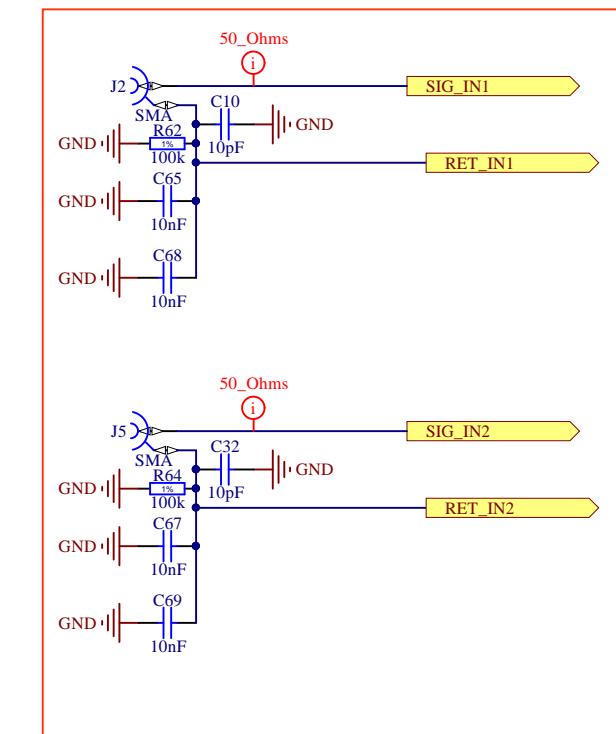


Project/Equipment		ADC/DAC MEZZANINE	
Document		Designer	SBH
		Drawn by	SBH
		Check by	-
		Last Mod.	2017-08-01
		File	B2B_connectors.SchDoc
		Print Date	2017-08-01 16:12:21
		Sheet	of
		Warsaw University of Technology	ISE
		Nowowiejska 15/19	
		ARTIQ	A3



A

A

Output SMAs**Input SMAs**

Input considerations and Variants:
 -> ADC-channel.SchDoc

B

B

C

C

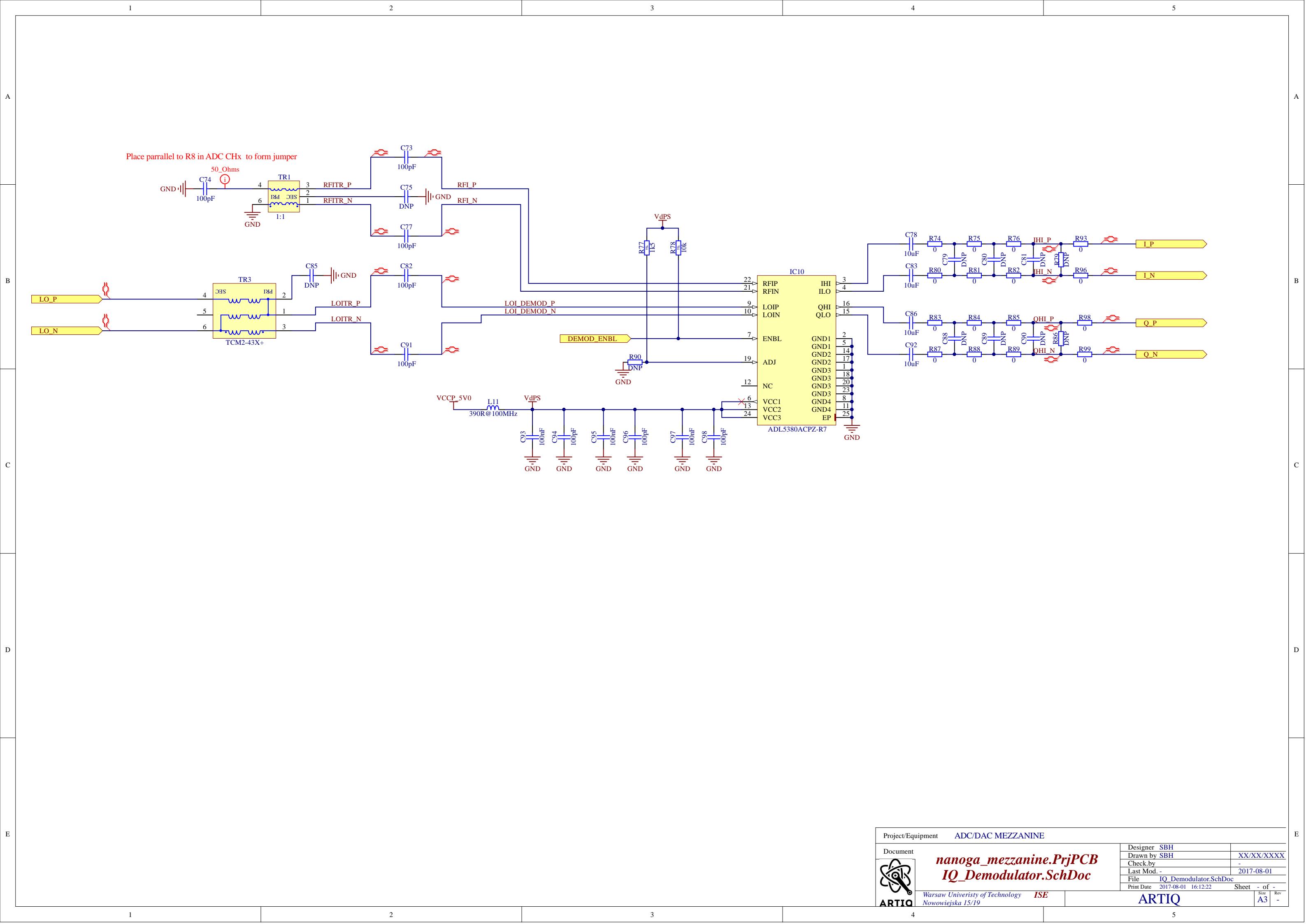
D

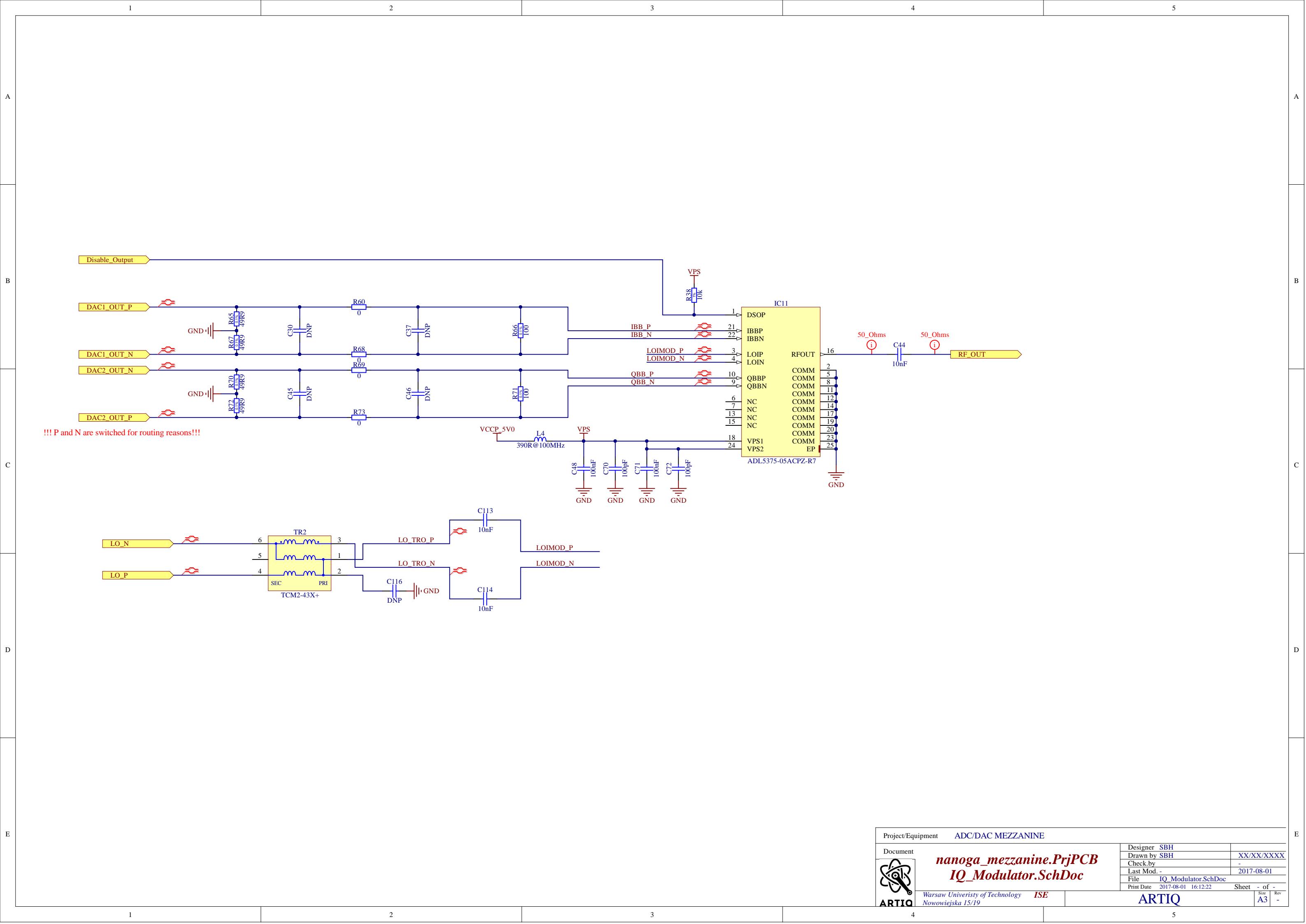
D

E

E

Project/Equipment		ADC/DAC MEZZANINE	
Document	nanoga_mezzanine.PrjPCB FP_connectors.SchDoc	Designer	SBH
		Drawn by	SBH
		Check by	-
		Last Mod.	2017-07-30
		File	FP_connectors.SchDoc
		Print Date	2017-08-01 16:12:22
		Sheet	of





A

A

B

B

C

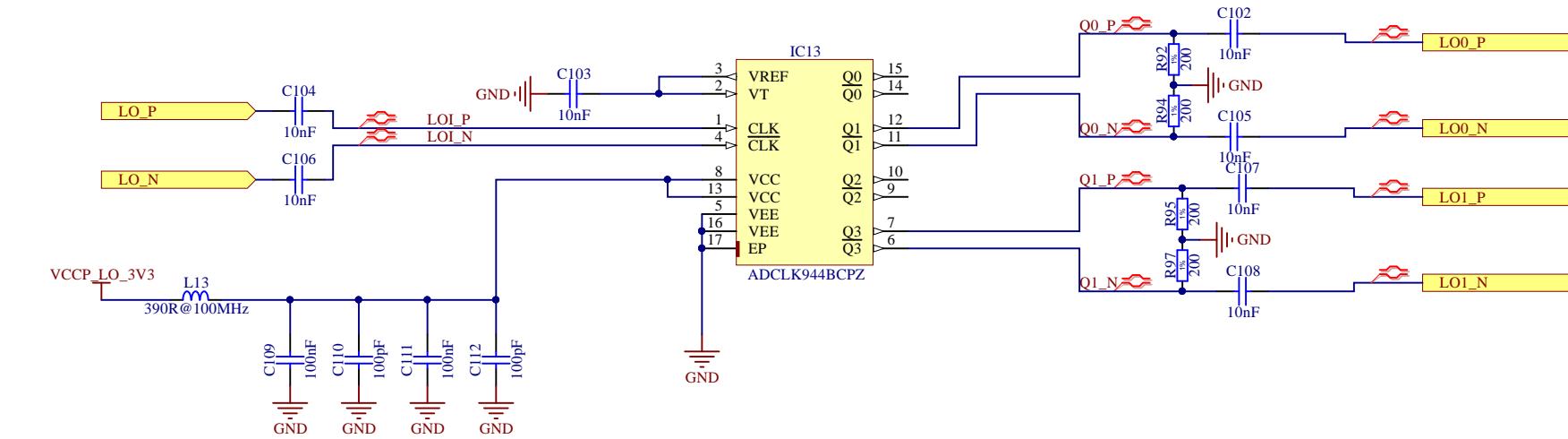
C

D

D

E

E



Project/Equipment	ADC/DAC MEZZANINE		
Document	<i>nanoga_mezzanine.PrjPCB LO_Distribution.SchDoc</i>		
	<i>Warsaw University of Technology ISE Nowowiejska 15/19</i>		
Designer SBH	Drawn by SBH	Check by -	XX/XX/XXXX
Last Mod. -	2017-08-01	File LO_Distribution.SchDoc	Sheet of -
Print Date 2017-08-01 16:12:22	Size A3	Rev -	

A

A

B

B

C

C

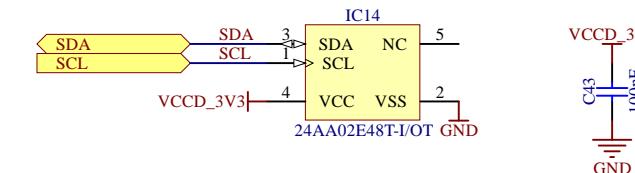
D

D

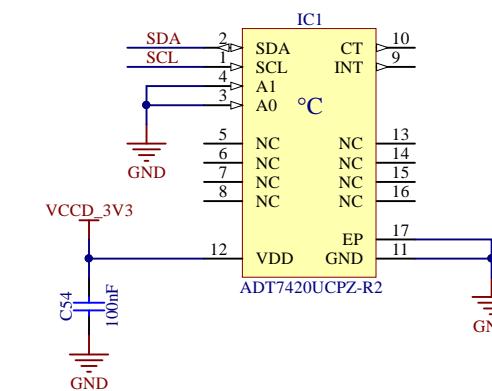
E

E

ID EEPROM



Temperature sensor



Project/Equipment ADC/DAC MEZZANINE

Document



nanoga_mezzanine.PrjPCB
Mgmt.SchDoc

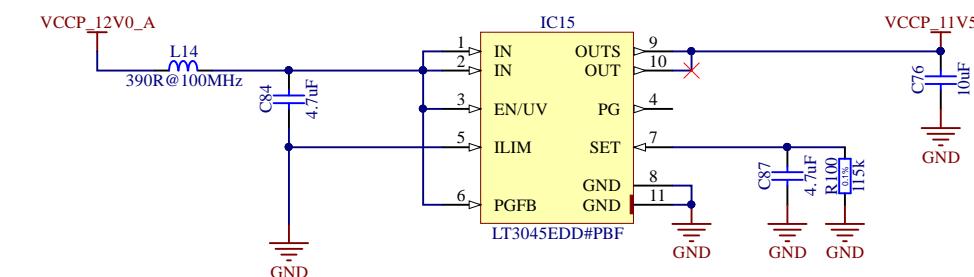
Designer SBH	Drawn by SBH	XX/XX/XXXX
Check by -	-	
Last Mod. -	2017-07-30	
File Mgmt.SchDoc		
Print Date 2017-08-01 16:12:22		Sheet of
		A3 -

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ARTIQ

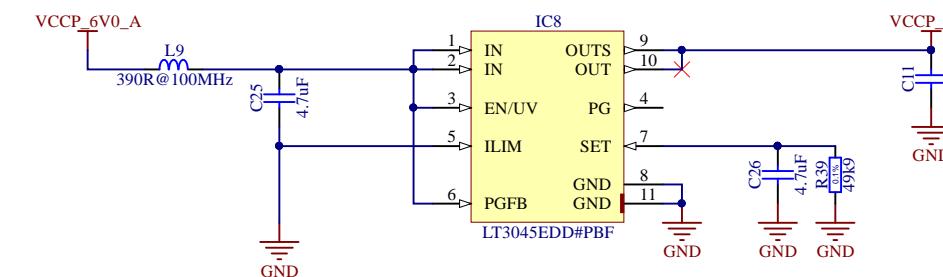
A

A

+11V5

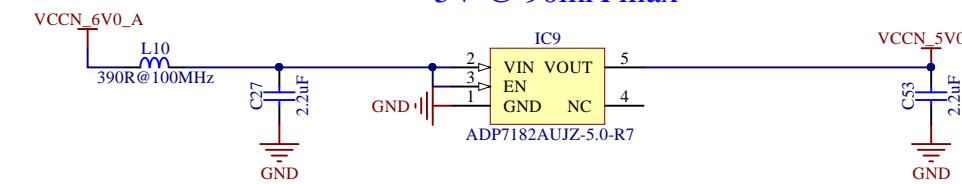
B

B

+5V @ 170mA max

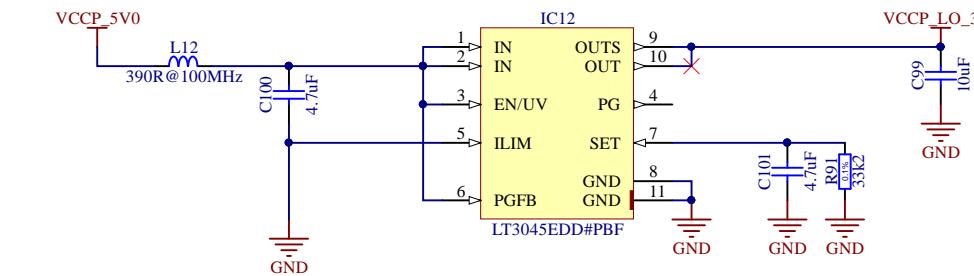
C

C

-5V @ 90mA max

D

D



E

E

Project/Equipment ADC/DAC MEZZANINE

Document

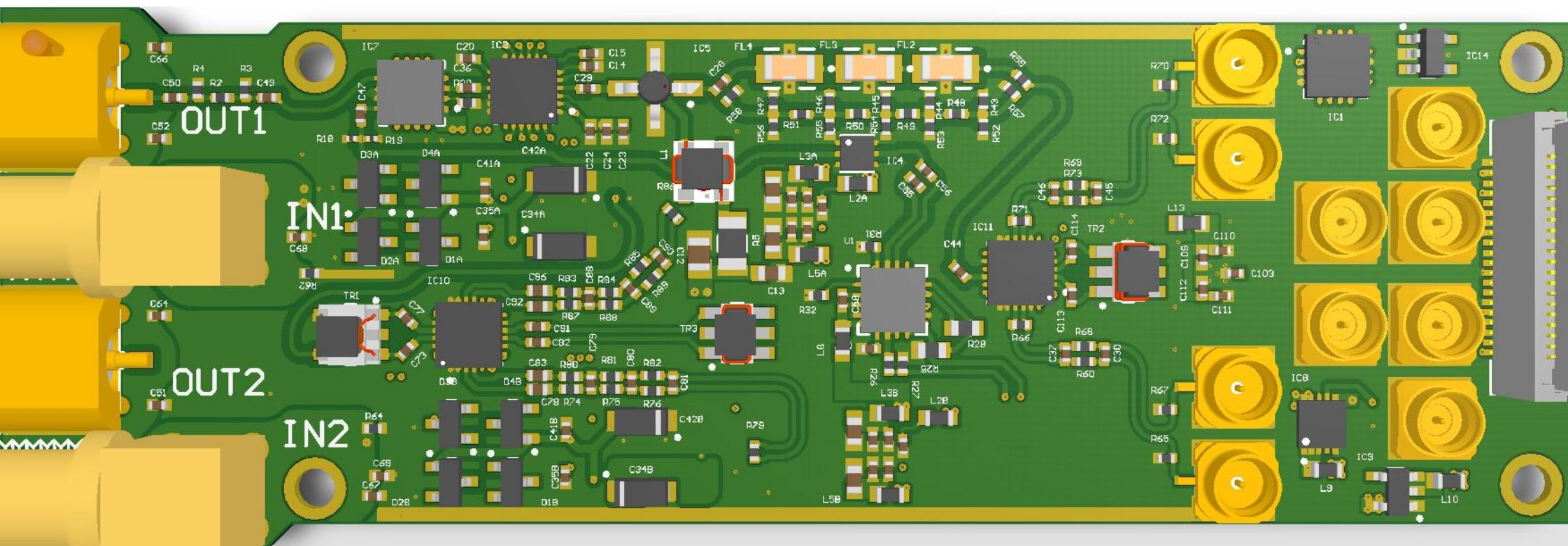


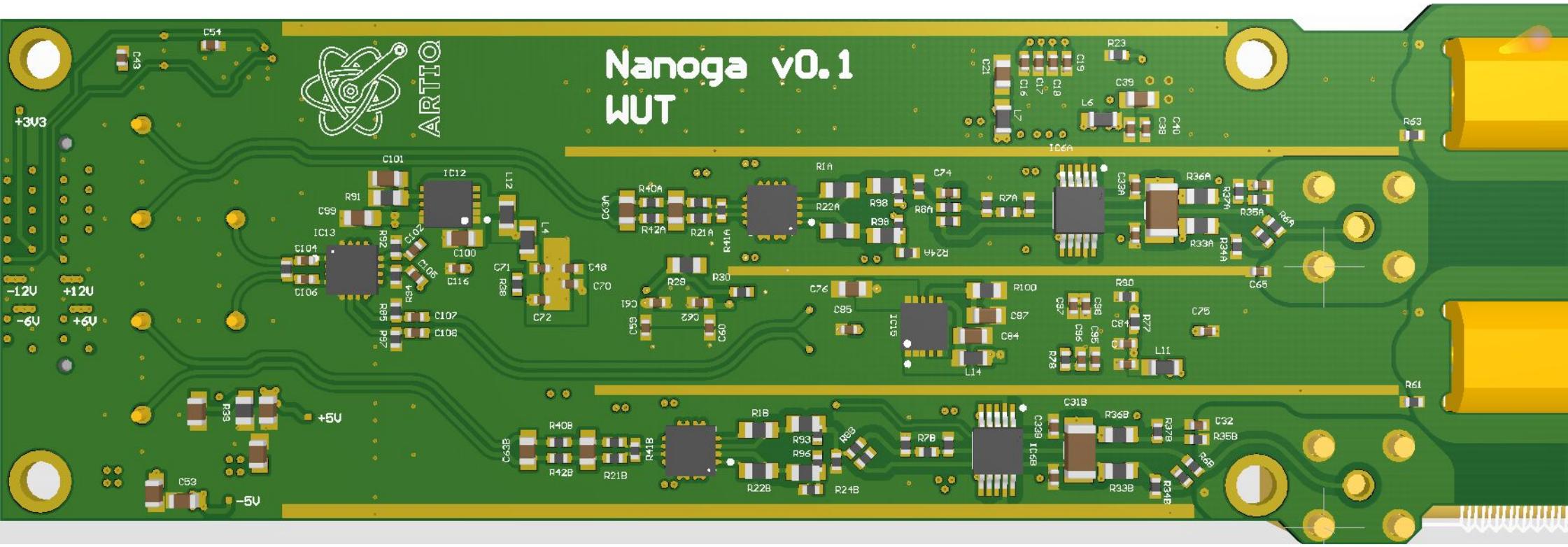
**nanoga_mezzanine.PrjPCB
PowerSupply.SchDoc**

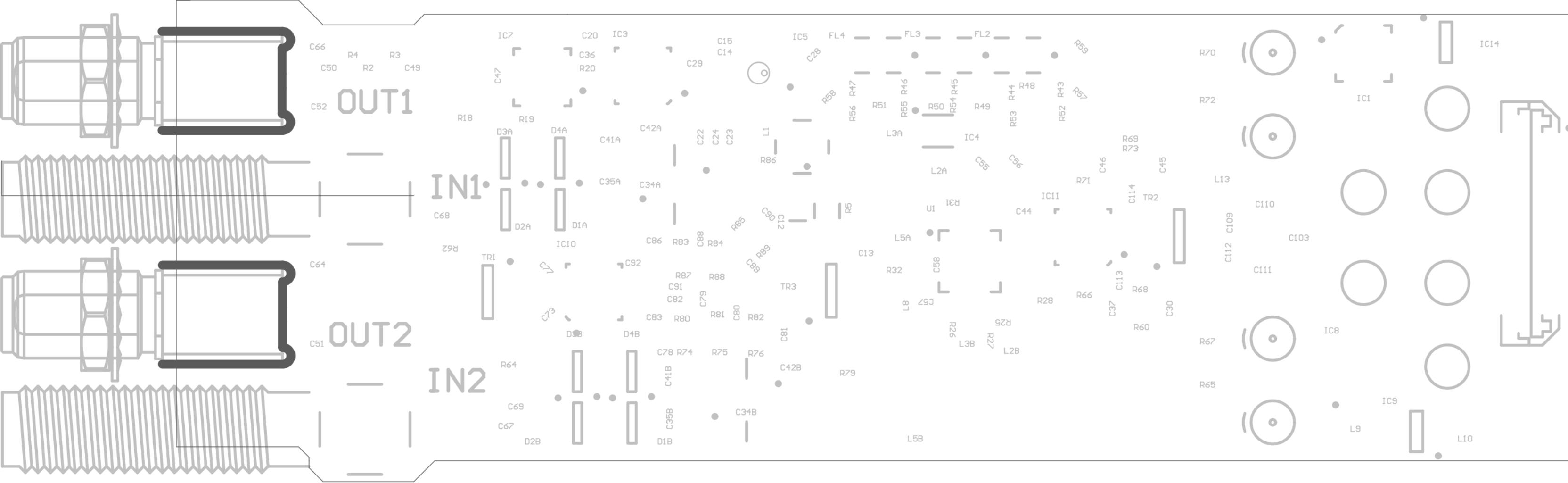
Designer SBH	Drawn by SBH	XX/XX/XXXX
Check by	-	
Last Mod.	-	2017-08-01
File PowerSupply.SchDoc	Print Date 2017-08-01 16:12:22	Sheet of
		A3 -

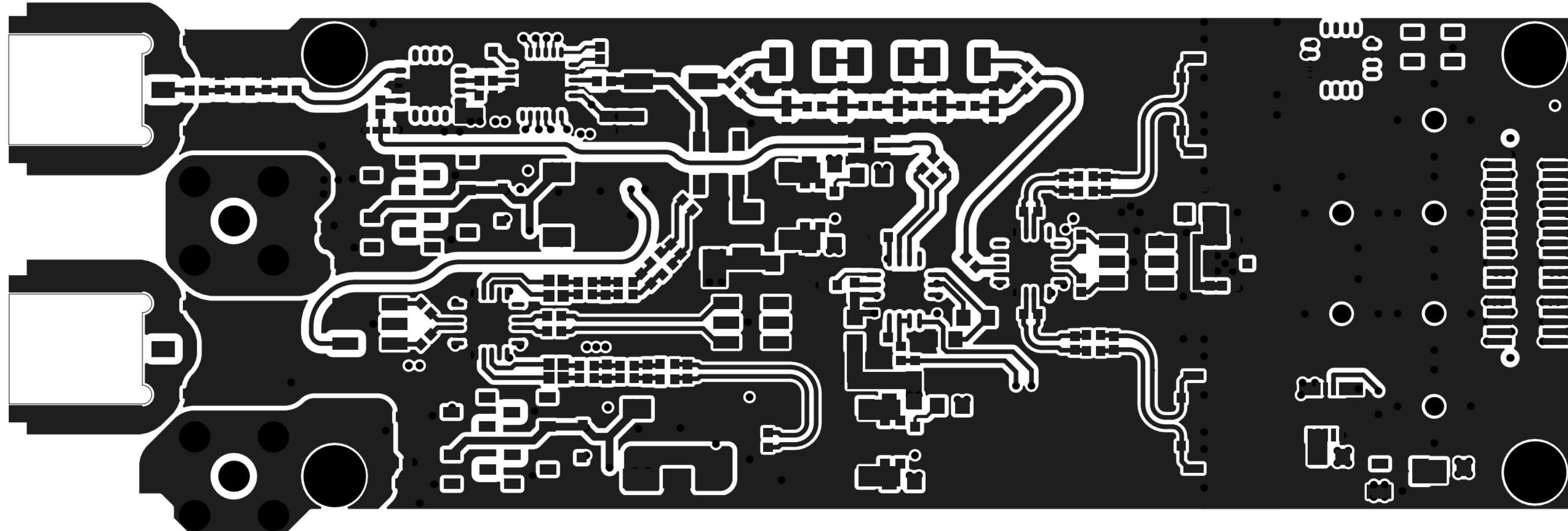
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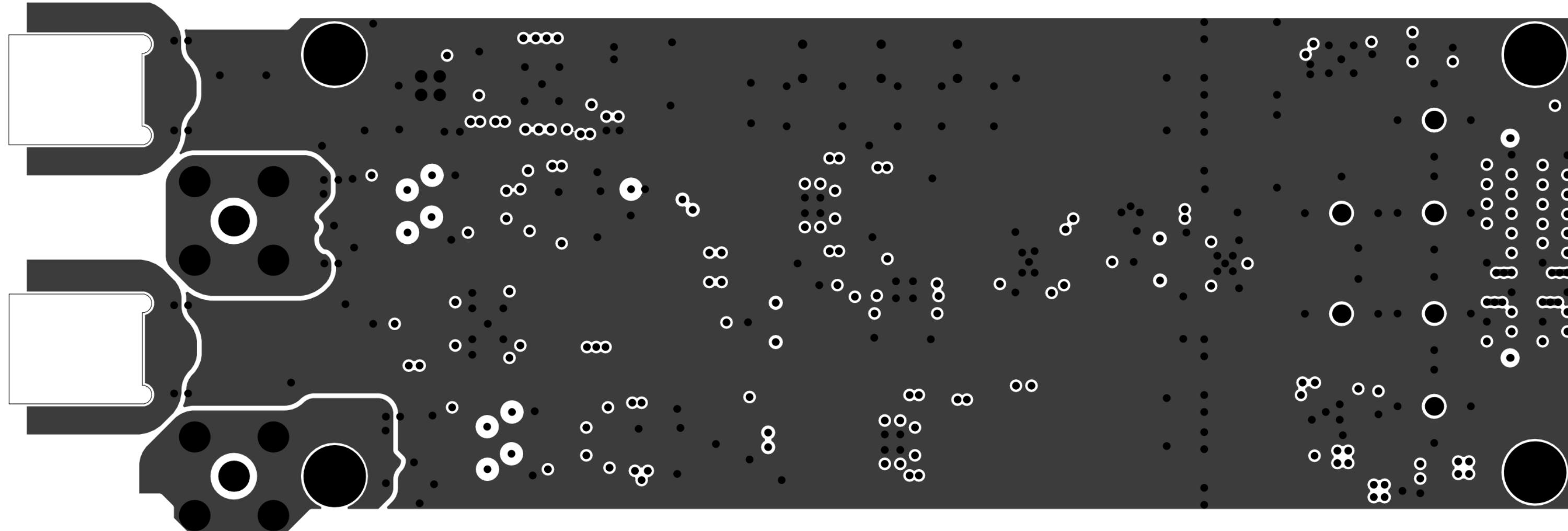
ARTIQ

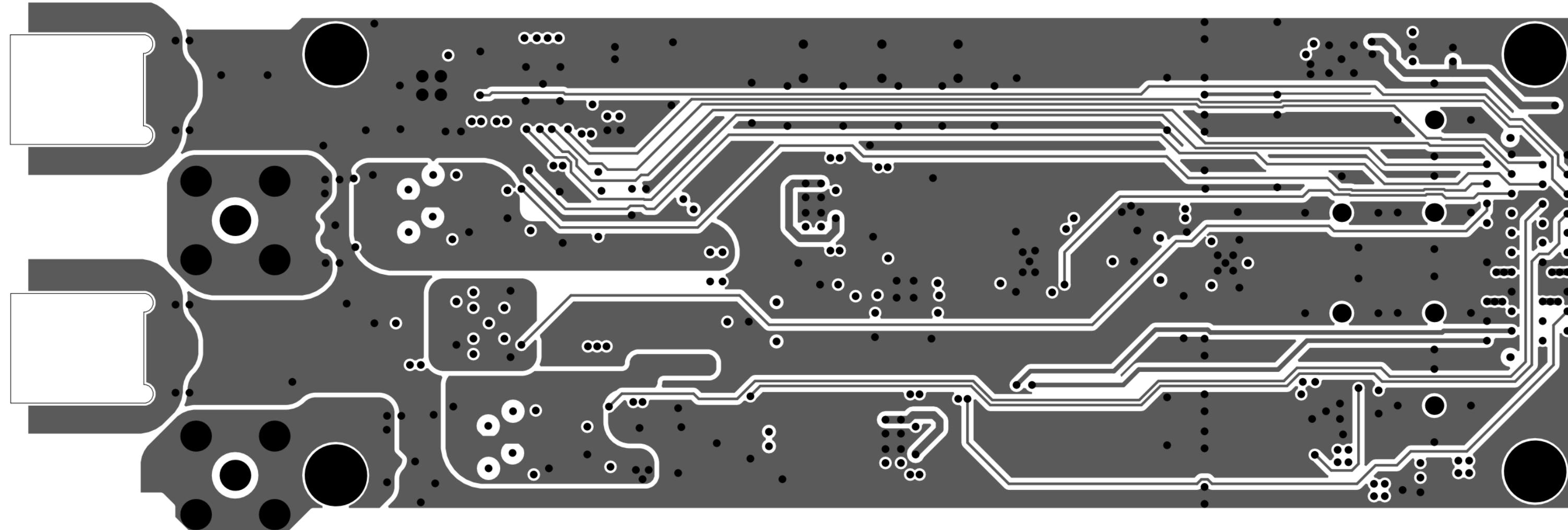


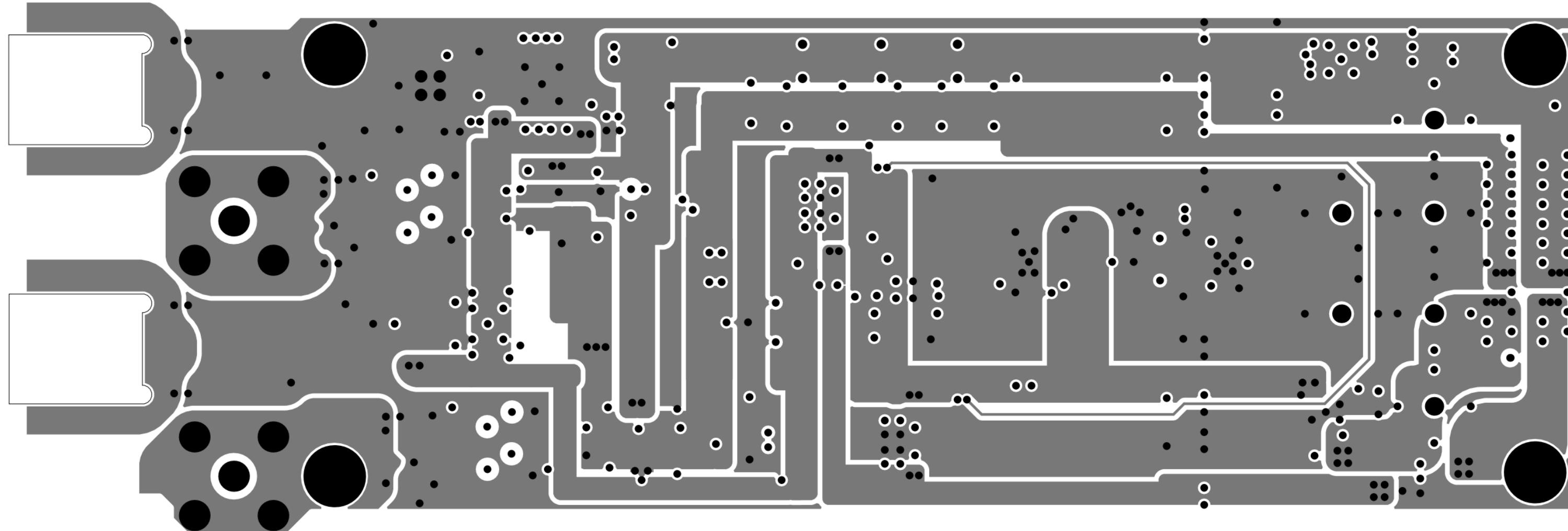




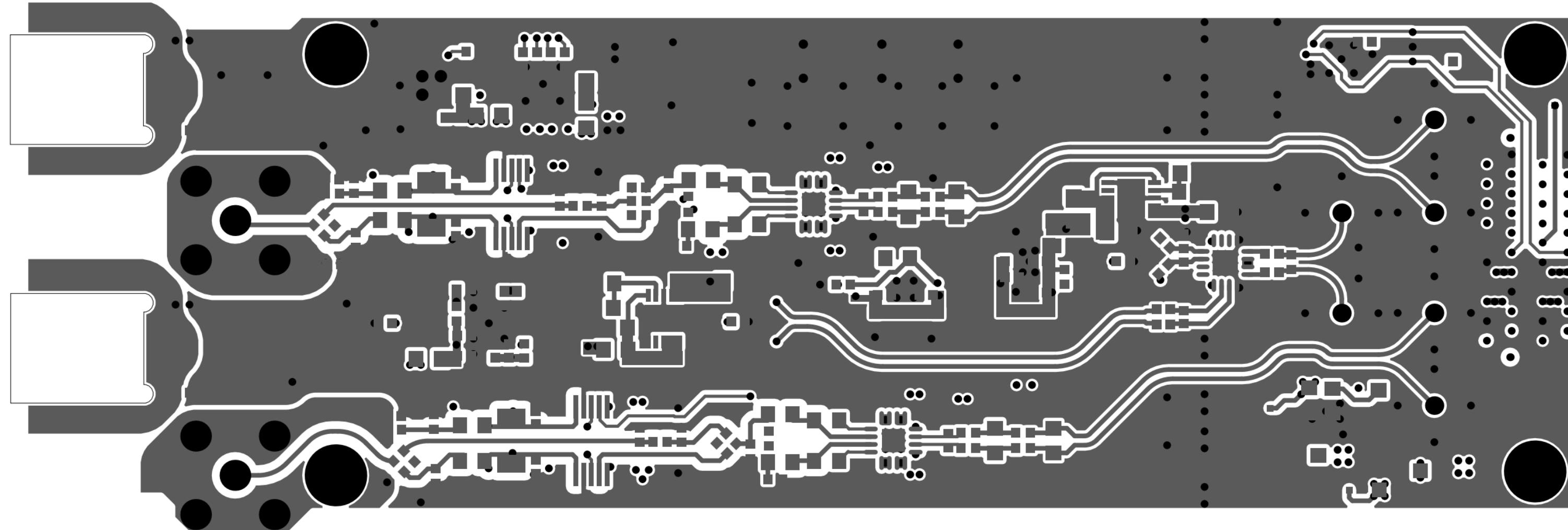












+3U3

-5A +12A

C45

C53

+5A

C54

-5A

C55

+5A

C51



Nanode v0.1

C51

R45B

R52B

R34B

R32B



R45



R45



R45



R45



R45



R45



R45



R45



R45



R45



R45