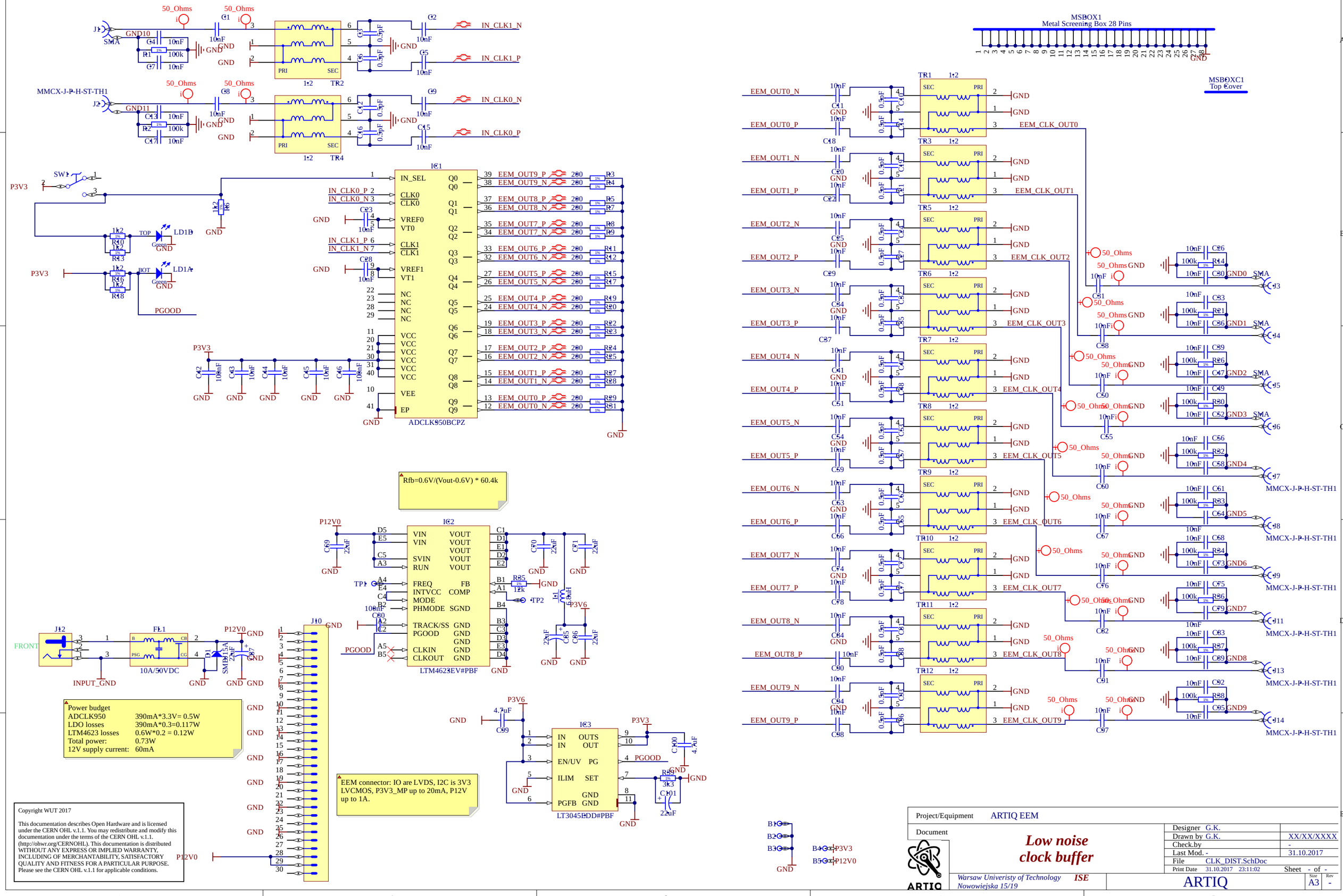
MMCX-J-P-H-ST-TH1
J1
J2
SMA
GND10
GND11
50_Ohms
G1
G2
G8
G9
C1
C2
C8
C9
C3
C4
C5
C6
C13
C14
C15
C16
C17
R1
R2
1:2
TR2
TR4
PRI
SEC
IN_CLK1_N
IN_CLK1_P
IN_CLK0_N
IN_CLK0_P
GND
P3V3
SW1
R6
1k2
TOP
BOT
LD1B
LD1A
Green
R40
R43
R45
R48
PGOOD
IC1
IN_SEL
CLK0
VREF0
VT0
CLK1
VREF1
VT1
NC
VCC
VEE
EP
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
ADCLK950BCPZ
EEM_OUT9_P
EEM_OUT9_N
EEM_OUT8_P
EEM_OUT8_N
EEM_OUT7_P
EEM_OUT7_N
EEM_OUT6_P
EEM_OUT6_N
EEM_OUT5_P
EEM_OUT5_N
EEM_OUT4_P
EEM_OUT4_N
EEM_OUT3_P
EEM_OUT3_N
EEM_OUT2_P
EEM_OUT2_N
EEM_OUT1_P
EEM_OUT1_N
EEM_OUT0_P
EEM_OUT0_N
R3
R4
R5
R7
R8
R9
R41
R42
R45
R47
R49
R50
R52
R53
R54
R55
R57
R58
R59
R60
R61
R62
R63
R64
R65
R66
R67
R68
R69
R70
R71
R72
R73
R74
R75
R76
R77
R78
R79
R80
R81
C42
C43
C44
C45
C46
100nF
10nF
Rfb=0.6V/(Vout-0.6V) * 60.4k
IC2
VIN
SVIN
RUN
FREQ
INTVCC
MODE
PHMODE
TRACK/SS
PGOOD
CLKIN
CLKOUT
VOUT
FB
COMP
SGND
LTM4623EV#PBF
P12V0
P3V6
TP1
TP2
R85
12k
L1
6.8uH
C69
C70
C71
C80
C85
C86
22uF
FRONT
J12
FL1
10A/50VDC
INPUT_GND
D1
SMBJ15A
C87
J10
Power budget
ADCLK950 390mA*3.3V= 0.5W
LDO losses 390mA*0.3=0.117W
LTM4623 losses 0.6W*0.2 = 0.12W
Total power: 0.73W
12V supply current: 60mA
EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A.
IC3
IN
EN/UV
ILIM
PGFB
OUTS
OUT
PG
SET
LT3045EDD#PBF
C99
C100
C101
R89
3k3
4.7uF
MSBOX1
Metal Screening Box 28 Pins
MSBOXC1
Top Cover
TR1
TR3
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
EEM_CLK_OUT0
EEM_CLK_OUT1
EEM_CLK_OUT2
EEM_CLK_OUT3
EEM_CLK_OUT4
EEM_CLK_OUT5
EEM_CLK_OUT6
EEM_CLK_OUT7
EEM_CLK_OUT8
EEM_CLK_OUT9
GND0
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
J3
J4
J5
J6
J7
J8
J9
J11
J13
J14
B1
B2
B3
B4
B5
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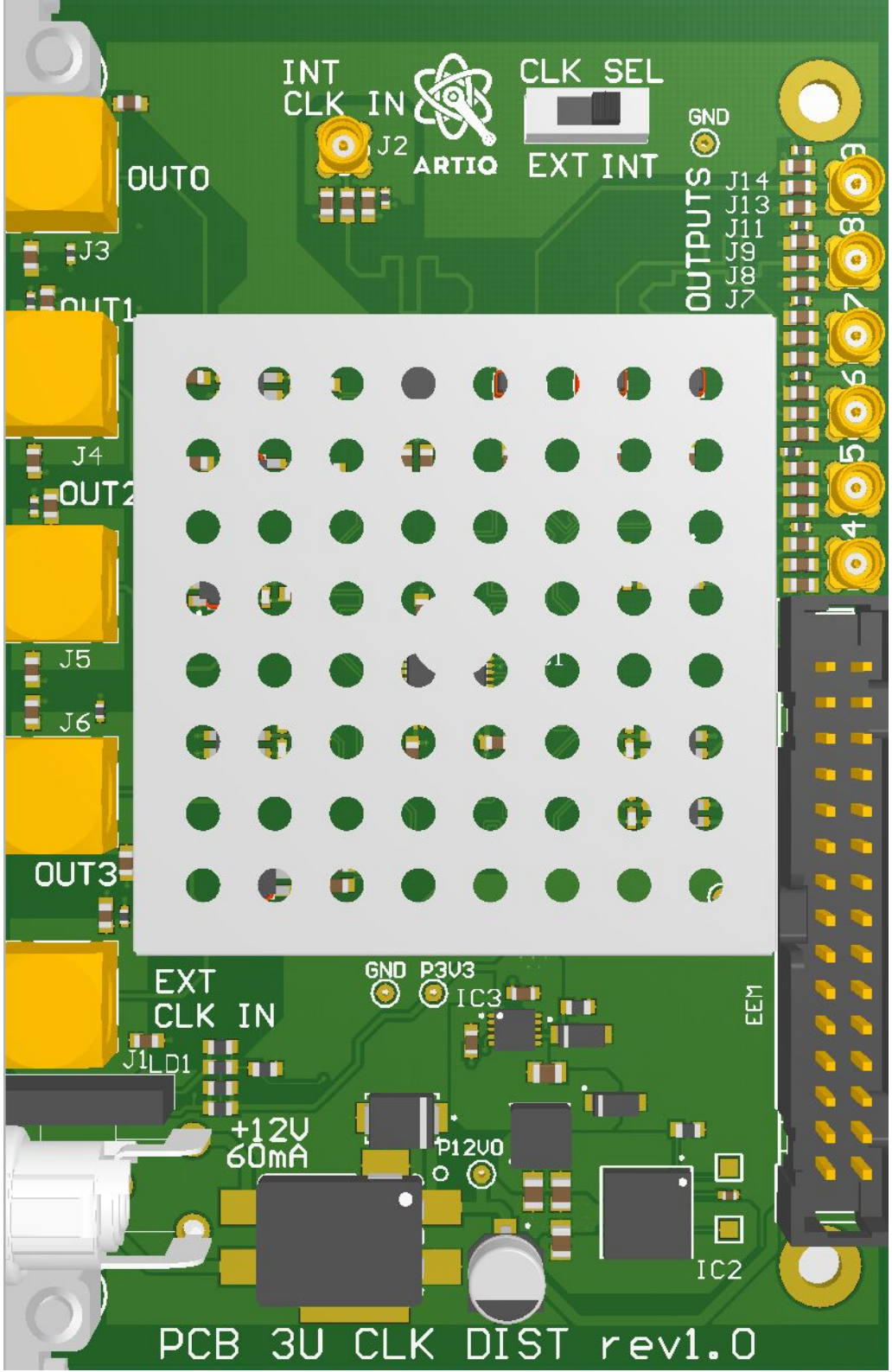
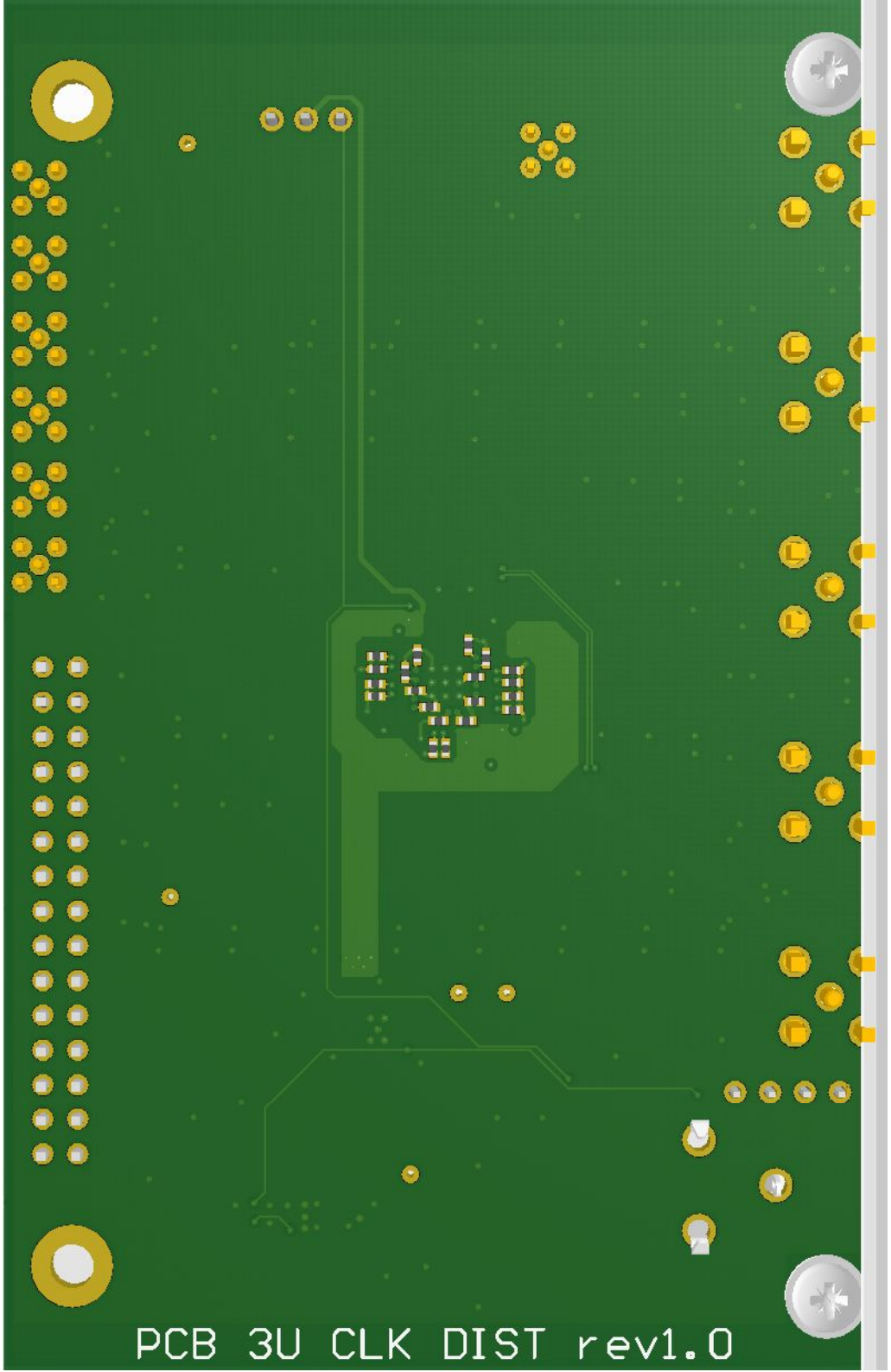
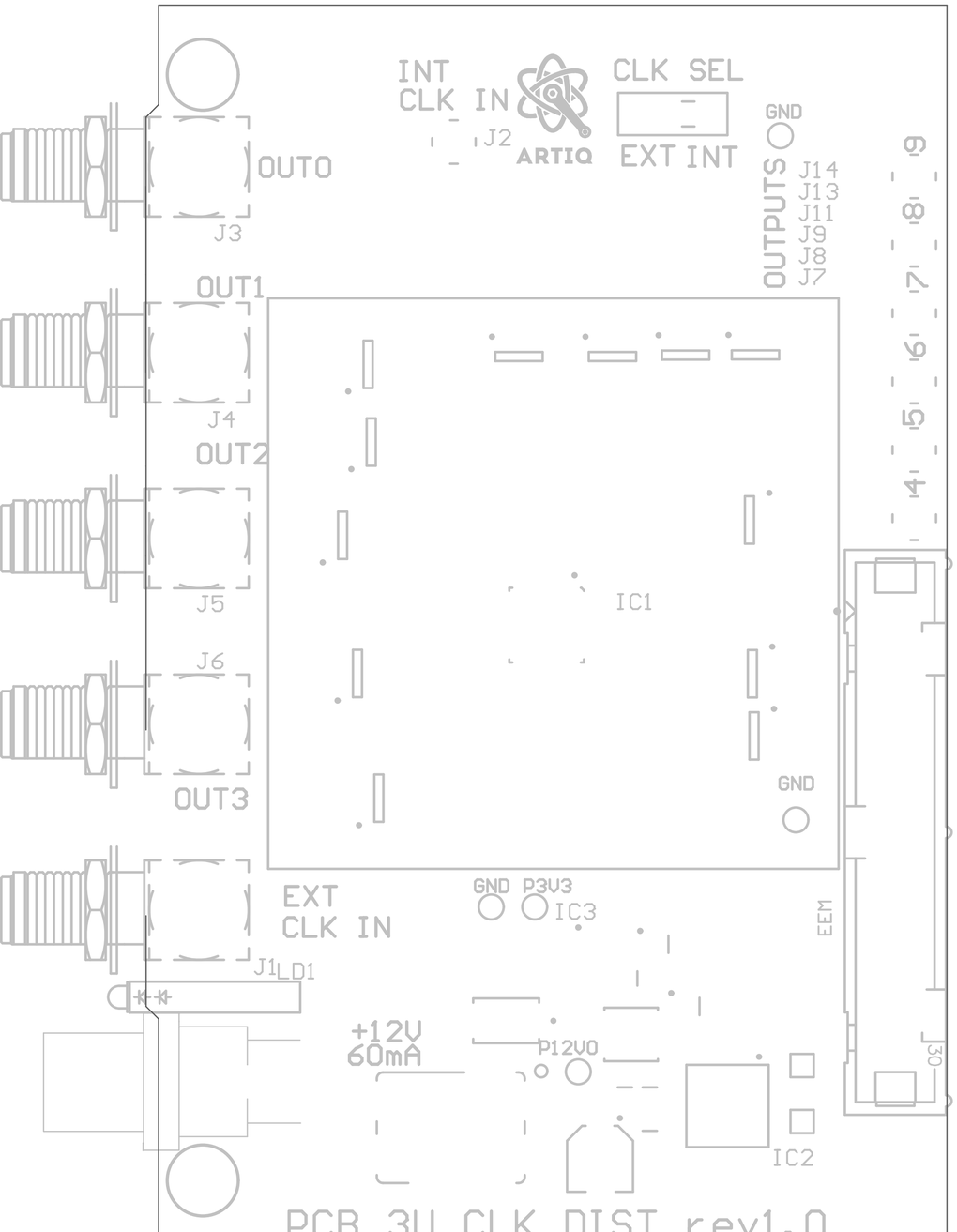
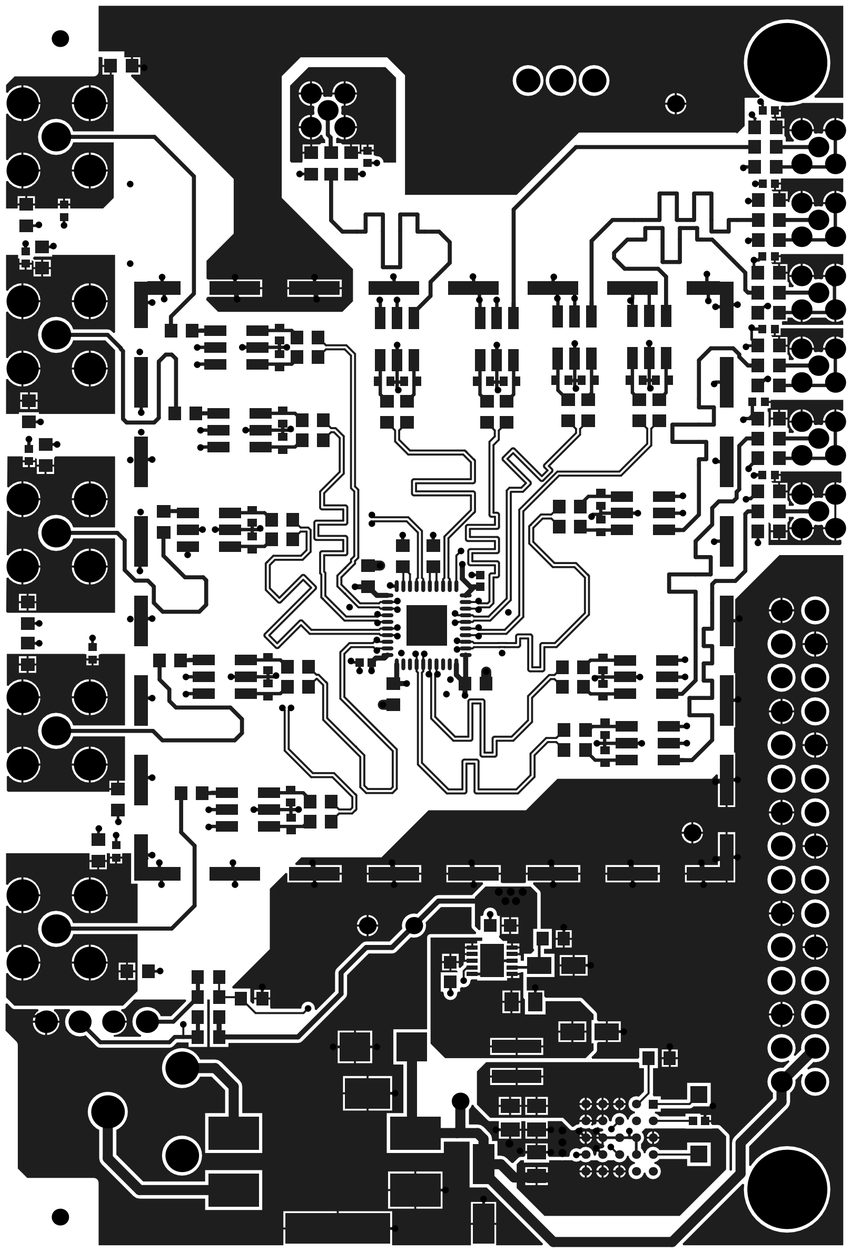
Project/Equipment ARTIQ EEM
Document
Low noise clock buffer
Designer G.K.
Drawn by G.K. XX/XX/XXXX
Check.by -
Last Mod. - 31.10.2017
File CLK_DIST.SchDoc
Print Date 31.10.2017 23:11:02
Sheet - of -
Warsaw Univeristy of Technology ISE
Nowowiejska 15/19
ARTIQ
Size A3
Rev -

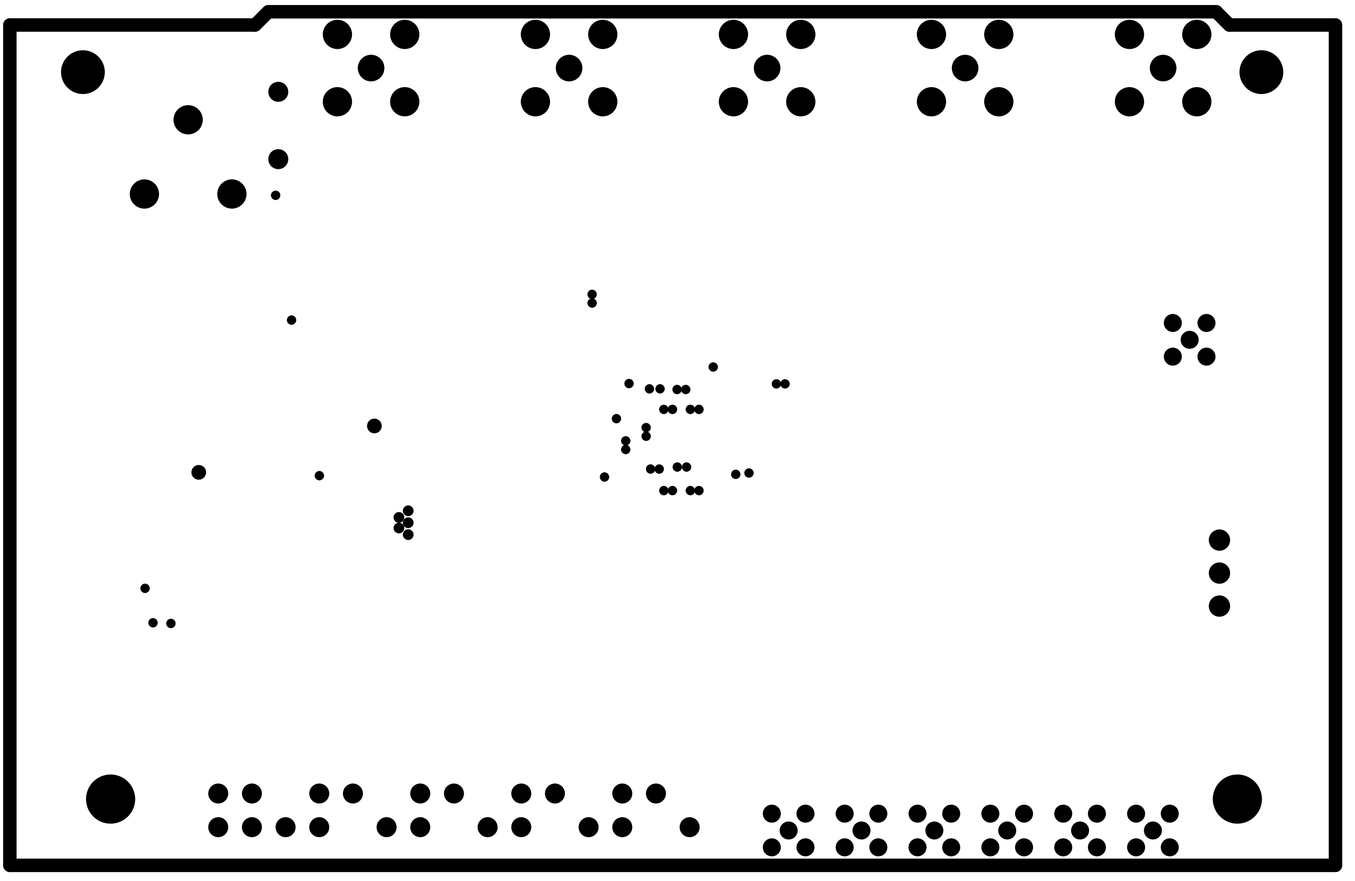

INT
CLK IN
J2
ARTIQ
CLK SEL
EXT INT
GND
OUTPUTS
J14
J13
J11
J9
J8
J7
OUT0
J3
OUT1
J4
OUT2
J5
J6
OUT3
EXT
CLK IN
J1
LD1
GND
P3V3
IC3
EEM
+12V
60mA
P12V0
IC2
PCB 3U CLK DIST rev1.0

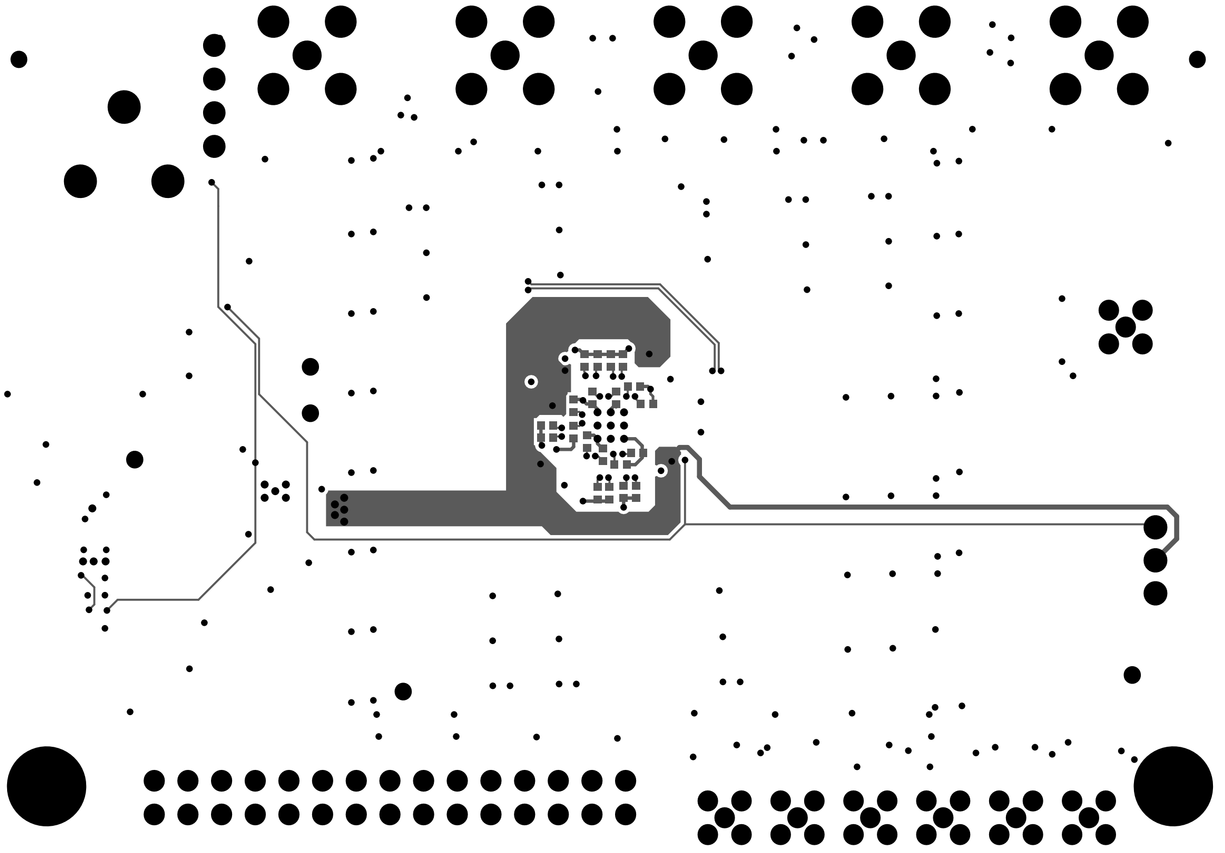

PCB 3U CLK DIST rev1.0


INT
CLK IN
J2
ARTIQ
CLK SEL
EXT INT
GND
OUTPUTS
J14
J13
J11
J9
J8
J7
OUT0
J3
OUT1
J4
OUT2
J5
J6
OUT3
IC1
GND
EXT
CLK IN
GND P3V3
IC3
EEM
J1
LD1
+12V
60mA
P12V0
IC2
PCB 3U CLK DIST rev1.0

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	TopOverlay				
2	TopSolder	Solder Resist	0.010mm	3.5	
3	Top	Copper	0.056mm		
4	Dielectric1	FR-4	0.180mm	4.8	
5	MP(G)	Copper	0.036mm		
6	Dielectric 3		1.080mm	4.2	
7	L3	Copper	0.036mm		
8	Dielectric 4		0.180mm	4.2	
9	Bot	Copper	0.056mm		
10	BottomSolder	Solder Resist	0.010mm	3.5	
11	BottomOverlay				







PCB 3U CLK DIST rev1.0