shield clips

CLIP1 CLIP2 CLIP3 CLIP4 CLIP5
CLIP6 CLIP7 CLIP8 CLIP9 CLIP10 CLIP27
CLIP11 CLIP12 CLIP13 CLIP14 CLIP15 CLIP28
CLIP16 CLIP17 CLIP18 CLIP19 CLIP20 CLIP29
CLIP21 CLIP22 CLIP23 CLIP24 CLIP25 CLIP26
GND

Ext clock input

Clock from Kasli

10nF C37 10nF C42
100k R6
SMA J2
50_Ohms
Coax_1Female_1Shield
IN_SEL
CLK_DIV

U_CLK_INPUT
CLK_INPUT.SchDoc
CK_SMA_IN
IN_SEL
CLK_DIV
INT_CLK_IN
DDS_CLKA0_P DDS_CLKA0_N DDS_CLKA1_P DDS_CLKA1_N DDS_CLKA2_P DDS_CLKA2_N DDS_CLKA3_P DDS_CLKA3_N DDS_CLKB0_P DDS_CLKB0_N DDS_CLKB1_P DDS_CLKB1_N DDS_CLKB2_P DDS_CLKB2_N DDS_CLKB3_P DDS_CLKB3_N

Output SMAs

10nF C41 100k R64 SMA J3 10nF C25 RF_OUT0 50_Ohms
10nF C51 100k R65 SMA J4 10nF C52 RF_OUT1 50_Ohms
10nF C53 100k R74 SMA J5 10nF C54 RF_OUT2 50_Ohms
10nF C55 100k R75 SMA J6 10nF C41 RF_OUT3 50_Ohms

ATT_CLK ATT_LE ATT_RSTn ATT_S_IN ATT_S_OUT

U_DDS_OUT_channel0
DDS_OUT_channel.SchDoc
DAC_OUT_P DAC_OUT_N RF_OUT ATT_CLK RFSW_CTRL ATT_LE ATT_RSTn ATT_S_IN ATT_S_OUT
RFSW_CTRL0

U_DDS_OUT_channel1
DDS_OUT_channel.SchDoc
RFSW_CTRL1

U_DDS_OUT_channel2
DDS_OUT_channel.SchDoc
RFSW_CTRL2

U_DDS_OUT_channel3
DDS_OUT_channel.SchDoc
RFSW_CTRL3

U_CTRL_LOGIC
CTRL_LOGIC.SchDoc
RFSW_CTRL0 RFSW_CTRL1 RFSW_CTRL2 RFSW_CTRL3
DDS_SDO[3..0] DDS_SDI[3..0] DDS_SCKI[3..0] DDS_CSn[3..0] IN_SEL CLK_DIV DDS_UPDATE[3..0] DDS_SYNC_CLK0 DDS_PLL_LOCK[3..0] SYNC_SMP_ERR[3..0] DDS_Profile
DDS_I/O_RESET DDS_RESET LED[7..0] ATT_CLK ATT_LE ATT_RSTn ATT_S_IN ATT_S_OUT
RE_DE[15..0]
IO0_SCKI IO1 IO2 IO3 IO4 IO5 IO6 IO7 IO8_CLK IO9 IO10 IO11 IO12 IO13 IO14 IO15
DDS_SYNC_CLKSEL DDS_SYNC_OUTEN DDS_SYNC_CLK_OUTEN

RE_DE[15..0]
DDS_SYNC_CLKSEL
DDS_SYNC_OUTEN

LVDS_IFC_DDS.SchDoc U_LVDS_IFC
IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7 LVDS0_P LVDS0_N LVDS1_P LVDS1_N LVDS7_P LVDS7_N
I2C_SDA I2C_SCL RE_DE0 RE_DE1 RE_DE2 RE_DE3 RE_DE4 RE_DE5 RE_DE6 RE_DE7
IDC0
RE_DE0 RE_DE1 RE_DE2 RE_DE3 RE_DE4 RE_DE5 RE_DE6 RE_DE7

LVDS_IFC_DDS.SchDoc U_LVDS_IFC
IDC1
RE_DE8 RE_DE9 RE_DE10 RE_DE11 RE_DE12 RE_DE13 RE_DE14 RE_DE15

PLACE IT CLOSE TO LVDS Rx/Tx
DDS_SYNC_CLK0
P3V3_CLK1
IC1 FIN1101K8X
GND

PLACE IT CLOSE TO LVDS Rx/Tx
IC9
DDS0_SYNC_OUT_P DDS0_SYNC_OUT_N
DDS0_SYNC_IN_P DDS0_SYNC_IN_N DDS1_SYNC_IN_P DDS1_SYNC_IN_N DDS2_SYNC_IN_P DDS2_SYNC_IN_N DDS3_SYNC_IN_P DDS3_SYNC_IN_N
IC6 FIN1101K8X
P3V3_CLK1
GND
120R@100MHz
P3V3
Si53304-B-GM
10nF 10nF

When routing please do a reasonable (100ps) length match within each of DDS_SYNC_CLK[3:0], DDS_UPDATE[3:0], RFSW_CTRL[3:0], IO[15:11] (nominally the RFSW_CTRL lines), DDS[3:0]_SYNC_IN, DDS_RESET and a really good one on DDS_CLK[3:0]_[PN].

U_DDS_channel0
DDS_channel.SchDoc
DAC_OUT_P DAC_OUT_N SYNC_OUT_P SYNC_OUT_N SYNC_CLK I/O_RESET RESET SYNC_IN_P SYNC_IN_N
SDO SDI SCKI CSN IO_UPDATE PLL_LOCK SYNC_SMP_ERR DDS_Profile DDS_CLKA_P DDS_CLKA_N DDS_CLKB_P DDS_CLKB_N
DDS_SDO0 DDS_SDI0 DDS_SCKI0 DDS_CSn0 DDS_UPDATE0 DDS_PLL_LOCK0 SYNC_SMP_ERR0 DDS_Profile DDS_CLKA0_P DDS_CLKA0_N DDS_CLKB0_P DDS_CLKB0_N

U_DDS_channel1
DDS_channel.SchDoc
DDS_SDO1 DDS_SDI1 DDS_SCKI1 DDS_CSn1 DDS_UPDATE1 DDS_PLL_LOCK1 SYNC_SMP_ERR1 DDS_Profile DDS_CLKA1_P DDS_CLKA1_N DDS_CLKB1_P DDS_CLKB1_N

U_DDS_channel2
DDS_channel.SchDoc
DDS_SDO2 DDS_SDI2 DDS_SCKI2 DDS_CSn2 DDS_UPDATE2 DDS_PLL_LOCK2 SYNC_SMP_ERR2 DDS_Profile DDS_CLKA2_P DDS_CLKA2_N DDS_CLKB2_P DDS_CLKB2_N

U_DDS_channel3
DDS_channel.SchDoc
DDS_SDO3 DDS_SDI3 DDS_SCKI3 DDS_CSn3 DDS_UPDATE3 DDS_PLL_LOCK3 SYNC_SMP_ERR3 DDS_Profile DDS_CLKA3_P DDS_CLKA3_N DDS_CLKB3_P DDS_CLKB3_N

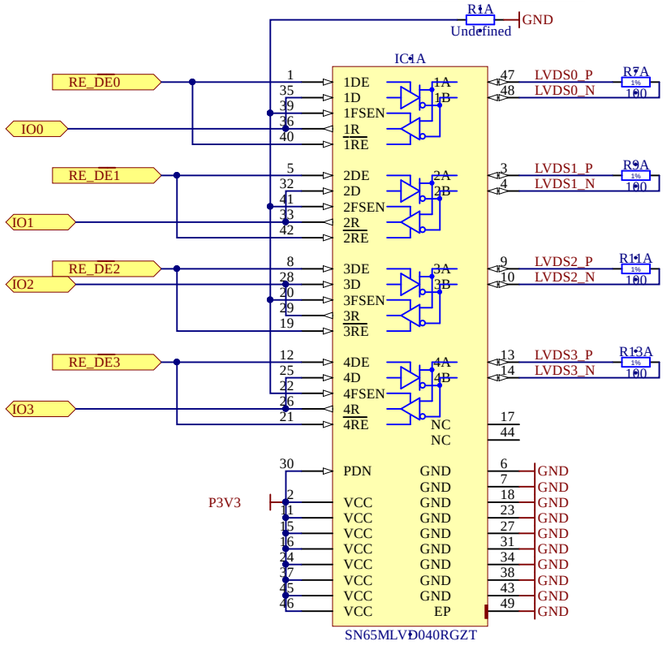
LED0 LED1 LED2 LED3 LED4 LED5 LED6 LED7
R25 R26 R27 R28 R29 R80 R43 R44 470
LD2A LD2B LD5A LD5B LD6A LD6B LD8A LD8B BOT TOP Green
GND

FIG1 FIG2 FIG3 FIG4

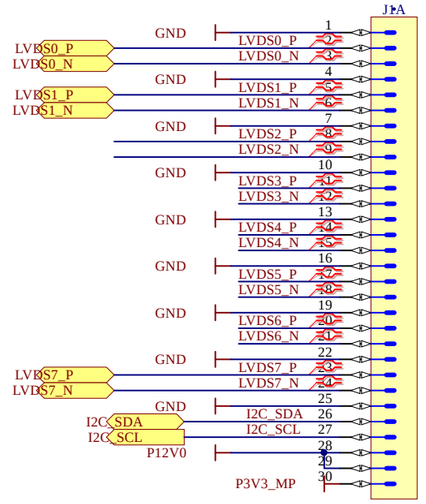
U_Supply_DDS
Supply_DDS.SchDoc

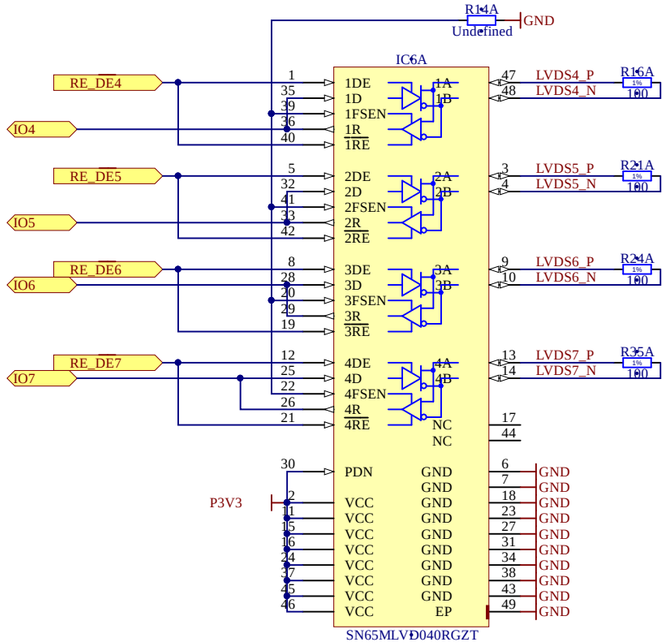
Project/Equipment	ARTIQ/SINARA		
Document	PCB_3U_DDS.PrjPCB PCB_3U_DDS.schdoc	Designer G.K.	
Cannot open file D:\Dropbox\DESIGNS\MTCA projects\SI		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File PCB_3U_DDS.schdoc	
		Print Date 17.09.2017 18:23:26	Sheet 1 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE	ARTIQ	Size A3 / Rev -

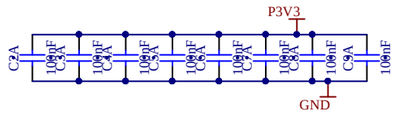
FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output

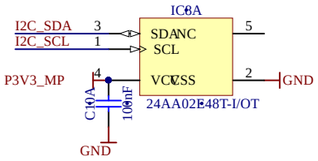


This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVCMOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A









Project/Equipment	ARTIQ/SINARA		
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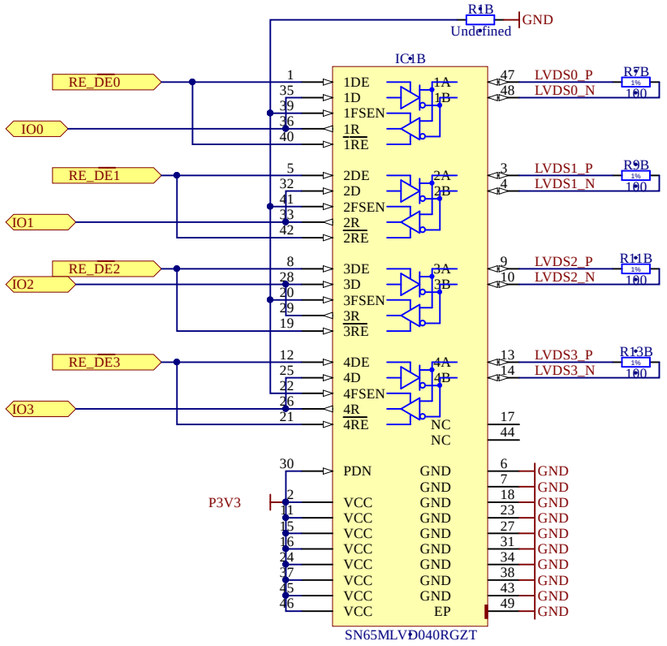
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE	ARTIQ	Size A3 / Rev -

FSEN = 1 -> type 2 receiver with offset; hanging input causes L at the output



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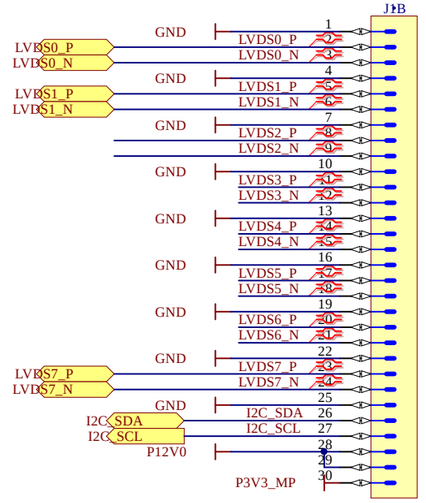

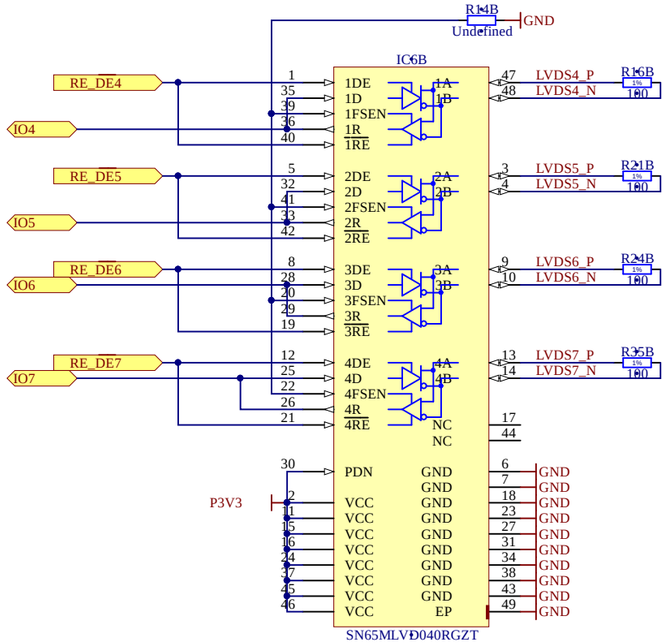

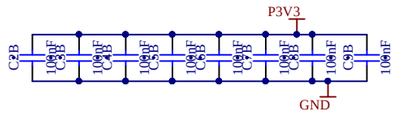

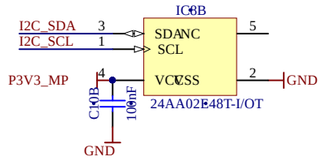

Project/Equipment	ARTIQ/SINARA		
Document	PCB_3U_DDS.PrjPCB LVDS_IFC_DDS.SchDoc	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
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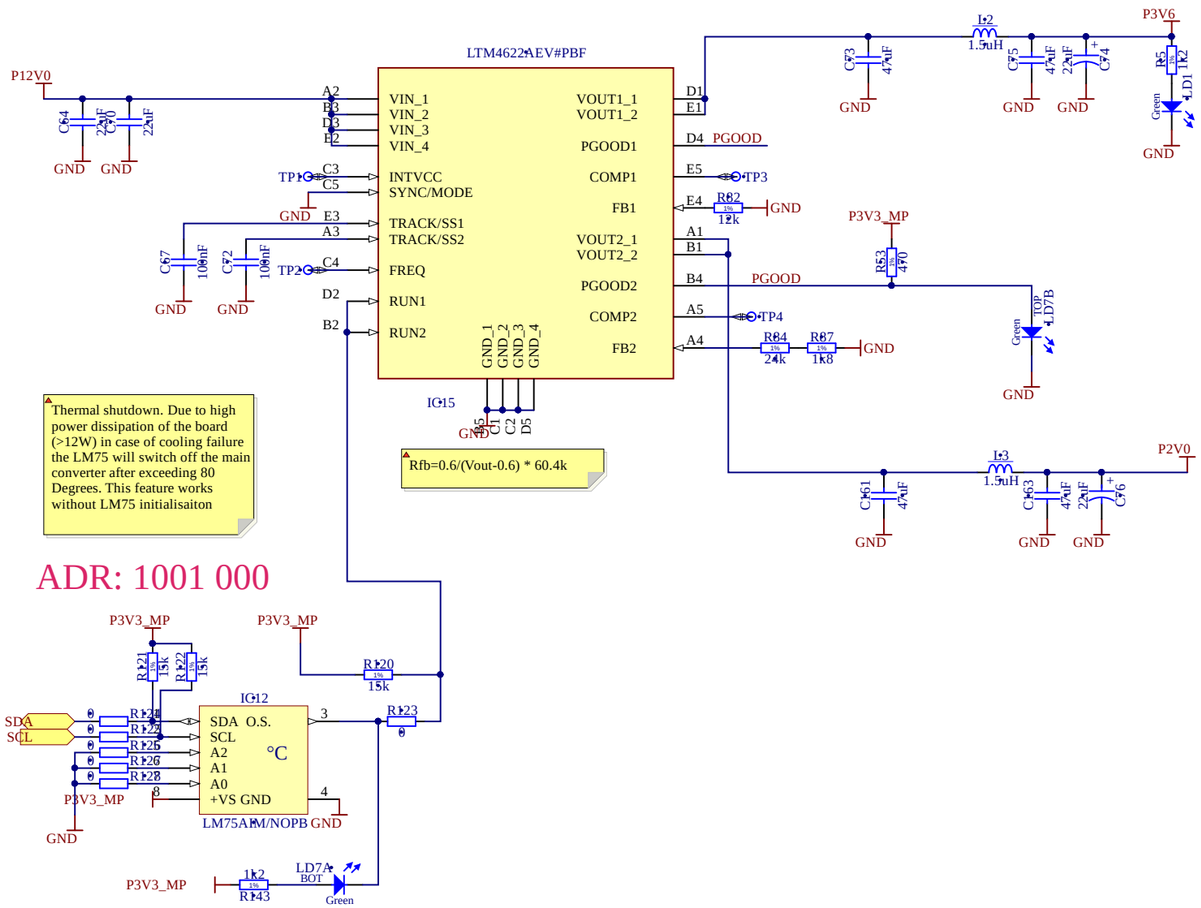
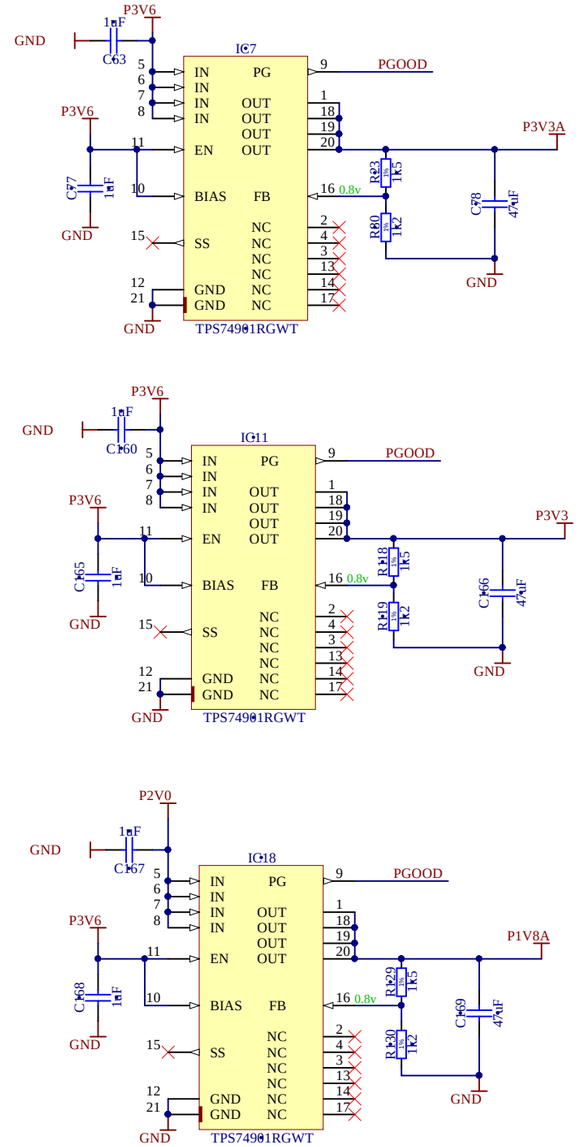
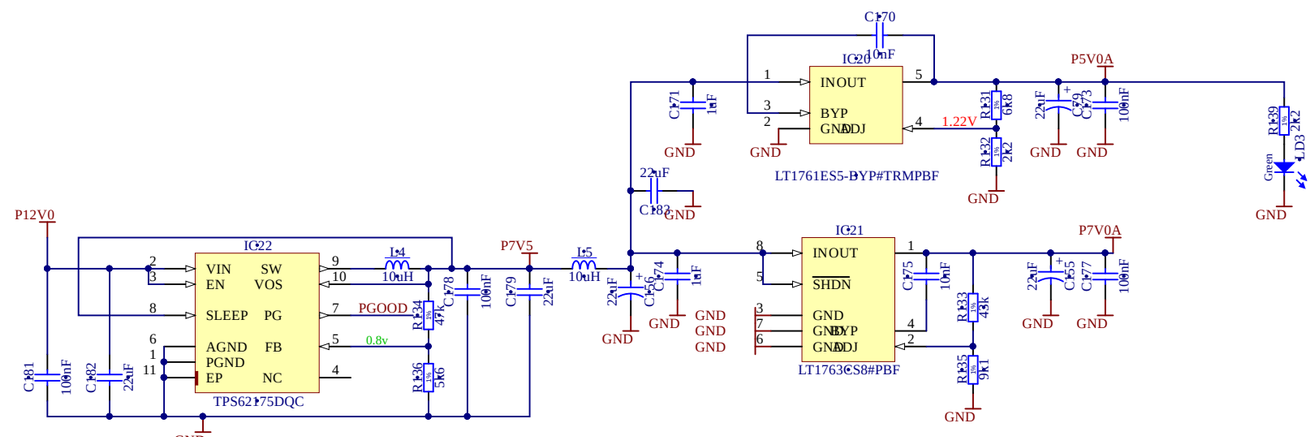
		Print Date 17.09.2017 18:23:26	Sheet 2 of 7
Cannot open file D:\Dropbox\DESIGNS\MTCA projects\SI	Warsaw Univeristy of Technology Nowowiejska 15/19	ISE	ARTIQ
			Size A3 / Rev -





Power budget (max ratings):	AD9912 variant(mA)	AD9910 variant(mA)
P3V3:		
LVDS interface 4x	660	660
LVDS load 4x24mA	96	96
CPLD	100	100
ADCLK948	230	230
DDS AVDD3	4*(9,6+31)=133,6	4*29=116
DDS DVDDIO	4*3=12	4*11=44
TOTAL P3V3	1121	1146
TOTAL POWER	3.7	3.7
P1V8:		
DDS AVDD	4*(48+136)=736	4*110=440
DDS DVDD	4*246=984	4*222=888
TOTAL P1V8	1720	1328
TOTAL POWER	3,096	2.39
P5V0		
HMC542BLP4E	4*2.9=11.6	4*2.9=11.6
HMC349LP4C	4*3.5=14	4*3.5=14
TOTAL 5V0	25.6	25.6
TOTAL POWER	0,125	0,125
P7V0		
ERA-3XSM+	4*35=150	4*35=150
TOTAL POWER	1.05	1.05
DC/DC converter losses		
TPS62175 eff .95	0,05*(.27+0,026)*7,5=0.11	0,05*(.27+0,026)*7,5=0.11
LTM:3.6V eff .9	0.1*1,321*3,6=0,47	0,1*1,346*3,6=0,48
LTM:2V eff .87	0.13*1,721*2=0,44	0.13*1.328*2=0.34
LDO losses		
2V->1.8V	0.34	0,26
3.6V->3.3V	0.396	0.4
7.5V->7V	0,135	0,135
7.5V->5V	0,064	0,064
Total power from 12V	9.95W	9.05
Total current from 12V	0.83A	0.75A



Project/Equipment	ARTIQ/SINARA		
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		Last Mod. -	06.09.2017
		File Supply_DDS.SchDoc	
		Print Date 17.09.2017 18:23:26	Sheet 3 of 7
Cannot open file D:\Dropbox\DESIGNS\MTCA projects\SI	Warsaw Univeristy of Technology Nowowiejska 15/19 ISE	ARTIQ	Size A3 / Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

Jumper

Jumper

Digital Attenuator

F clk max = 30MHz

HMC542BLP4E

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R5 power = 65mA^2*39 = 0.16W

SPDT switch

HMC349ALP4CE

Amplifier
~23 dB gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA		
Document	PCB_3U_DDS.PrjPCB DDS_OUT_channel.SchDoc	Designer G.K.	
Cannot open file D:\Dropbox\DESIGNS\MTCA projects\SI		Drawn by G.K.	XX/XX/XXXX
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Warsaw Univeristy of Technology ISE Nowowiejska 15/19	ARTIQ	Size A3	Rev -

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Jumper

Jumper

Digital Attenuator

F clk max = 30MHz

HMC542BLP4E

SPDT switch

HMC349ALP4CE

With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

R5 power = 65mA^2*39 = 0.16W

Amplifier
~23 dB gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA		
Document	PCB_3U_DDS.PrjPCB DDS_OUT_channel.SchDoc	Designer G.K.	
Cannot open file D:\Dropbox\DESIGNS\MTCA projects\SI		Drawn by G.K.	XX/XX/XXXX
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		Last Mod. -	17.09.2017
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		Print Date 17.09.2017 18:23:27	Sheet 4 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19 ISE	ARTIQ	Size A3	Rev -

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R5 power = 65mA^2*39 = 0.16W

SPDT switch

HMC349ALP4CE

Amplifier
~23 dB gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA
Document	PCB_3U_DDS.PrjPCB DDS_OUT_channel.SchDoc
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Drawn by	G.K. XX/XX/XXXX
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Last Mod.	- 17.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	17.09.2017 18:23:27 Sheet 4 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
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Populate Filter Components according to individual project design
For Custom FIlter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

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Jumper

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F clk max = 30MHz

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With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.

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SPDT switch

HMC349ALP4CE

Amplifier
~23 dB gain and 13 dBm P1dB

Project/Equipment	ARTIQ/SINARA
Document	PCB_3U_DDS.PrjPCB DDS_OUT_channel.SchDoc
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Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_OUT_channel.SchDoc
Print Date	17.09.2017 18:23:28 Sheet 4 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

NOT MOUNTED BY DEFAULT

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

Clock must be AC coupled

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

IC13A

AD9912ABCPZ

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

IC2A

AD9910BSVZ

Project/Equipment	ARTIQ/SINARA
Document	PCB_3U_DDS.PrjPCB DDS_channel.SchDoc
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_channel.SchDoc
Print Date	17.09.2017 18:23:28 Sheet 5 of 7
Cannot open file D:\Dropbox\DESIGNS\MTCA projects\SI	Warsaw Univeristy of Technology Nowowiejska 15/19 ISE
	ARTIQ Size A3 Rev -

NOT MOUNTED BY DEFAULT

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

Clock must be AC coupled

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

IC13B

AD9912ABCPZ

IC2B

AD9910BSVZ

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Project/Equipment	ARTIQ/SINARA
Document	PCB_3U_DDS.PrjPCB DDS_channel.SchDoc
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
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Print Date	17.09.2017 18:23:29 Sheet 5 of 7
Cannot open file D:\Dropbox\DESIGNS\MTCA projects\SI	Warsaw Univeristy of Technology Nowowiejska 15/19 ISE
	ARTIQ Size A3 Rev -

NOT MOUNTED BY DEFAULT

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

Clock must be AC coupled

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

IC13C

AD9912ABCPZ

Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

IC12C

AD9910BSVZ

Project/Equipment	ARTIQ/SINARA
Document	PCB_3U_DDS.PrjPCB DDS_channel.SchDoc
Cannot open file D:\Dropbox\DESIGNS\MTCA projects\SI	
Designer	G.K.
Drawn by	G.K. XX/XX/XXXX
Check.by	-
Last Mod.	- 17.09.2017
File	DDS_channel.SchDoc
Print Date	17.09.2017 18:23:29 Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE
ARTIQ	Size A3 Rev -

NOT MOUNTED BY DEFAULT

Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source.

Clock must be AC coupled

System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed

Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power down state. This pin has an internal 50 kΩ pull-down resistor.

PIN37 is not used but must be powered 1.8 or 3.3

IC13D

AD9912ABCPZ

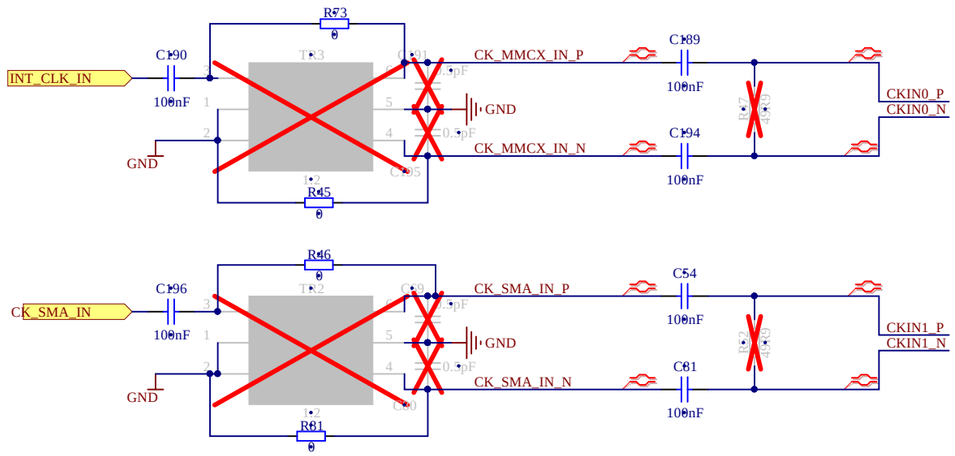
Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

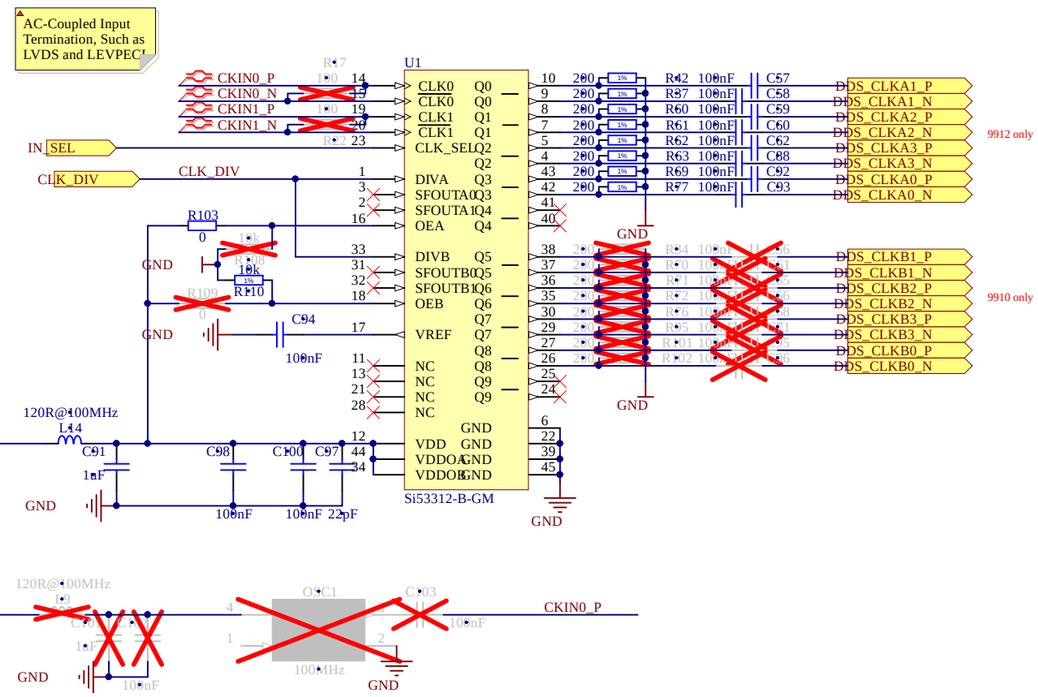
Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

IC2D

AD9910BSVZ

Project/Equipment	ARTIQ/SINARA		
Document	PCB_3U_DDS.PrjPCB DDS_channel.SchDoc	Designer G.K.	
Cannot open file D:\Dropbox\DESIGNS\MTCA projects\SI		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	17.09.2017
		File DDS_channel.SchDoc	
		Print Date 17.09.2017 18:23:30	Sheet 5 of 7
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE	ARTIQ	Size A3 / Rev -





Project/Equipment: ARTIQ/SINARA

Document: Cannot open file D:\Dropbox\DESIGNS\MTCA projects\SI

PCB_3U_DDS.PrjPCB
CLK_INPUT.SchDoc

Designer	G.K.	
Drawn by	G.K.	XX/XX/XXXX
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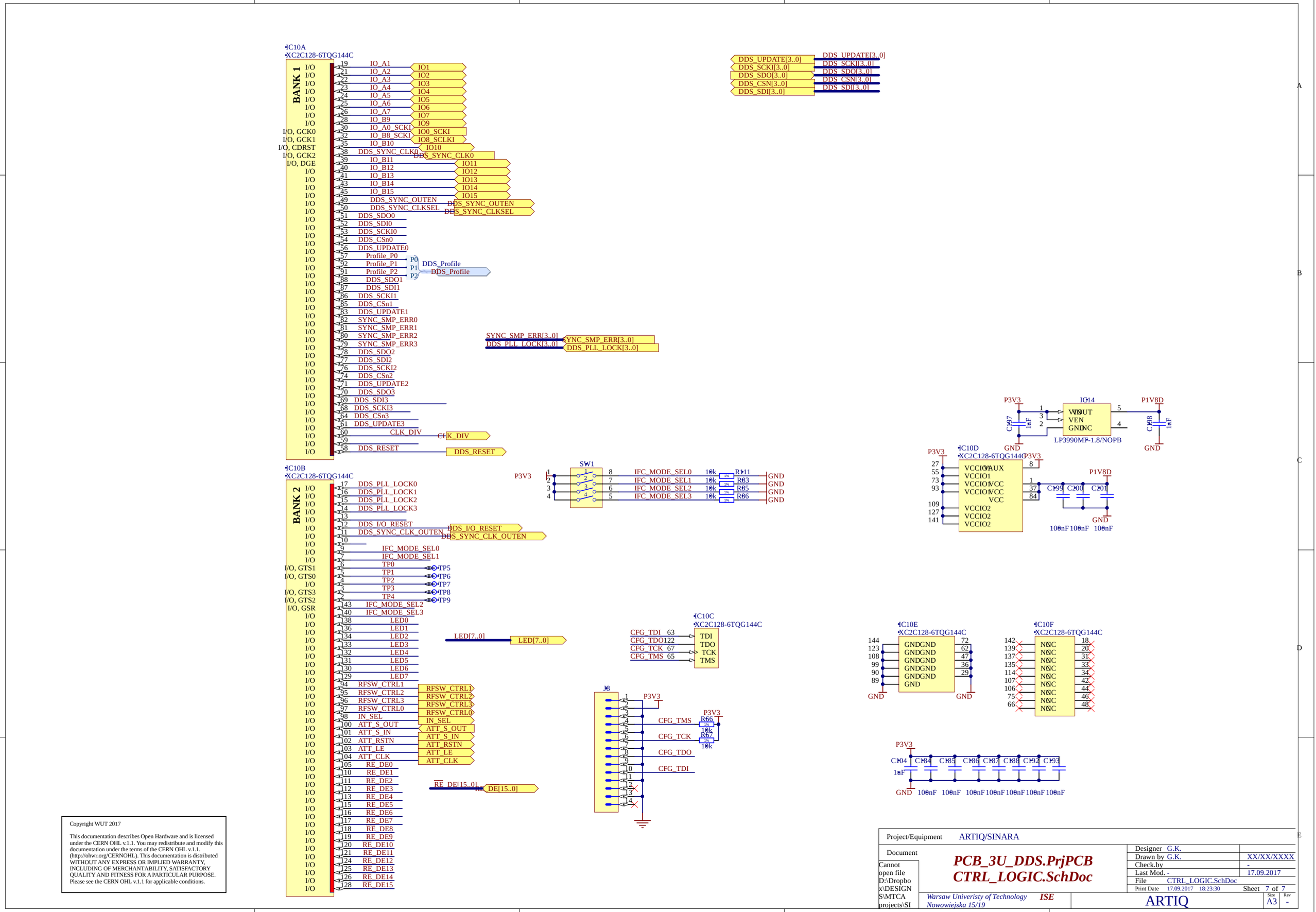
File	CLK_INPUT.SchDoc	
Print Date	17.09.2017 18:23:30	Sheet 6 of 7

Warsaw Univeristy of Technology *ISE*
Nowowiejska 15/19

ARTIQ

Size A3 | Rev -



Project/Equipment	ARTIQ/SINARA		
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		Print Date 17.09.2017 18:23:30	Sheet 7 of 7
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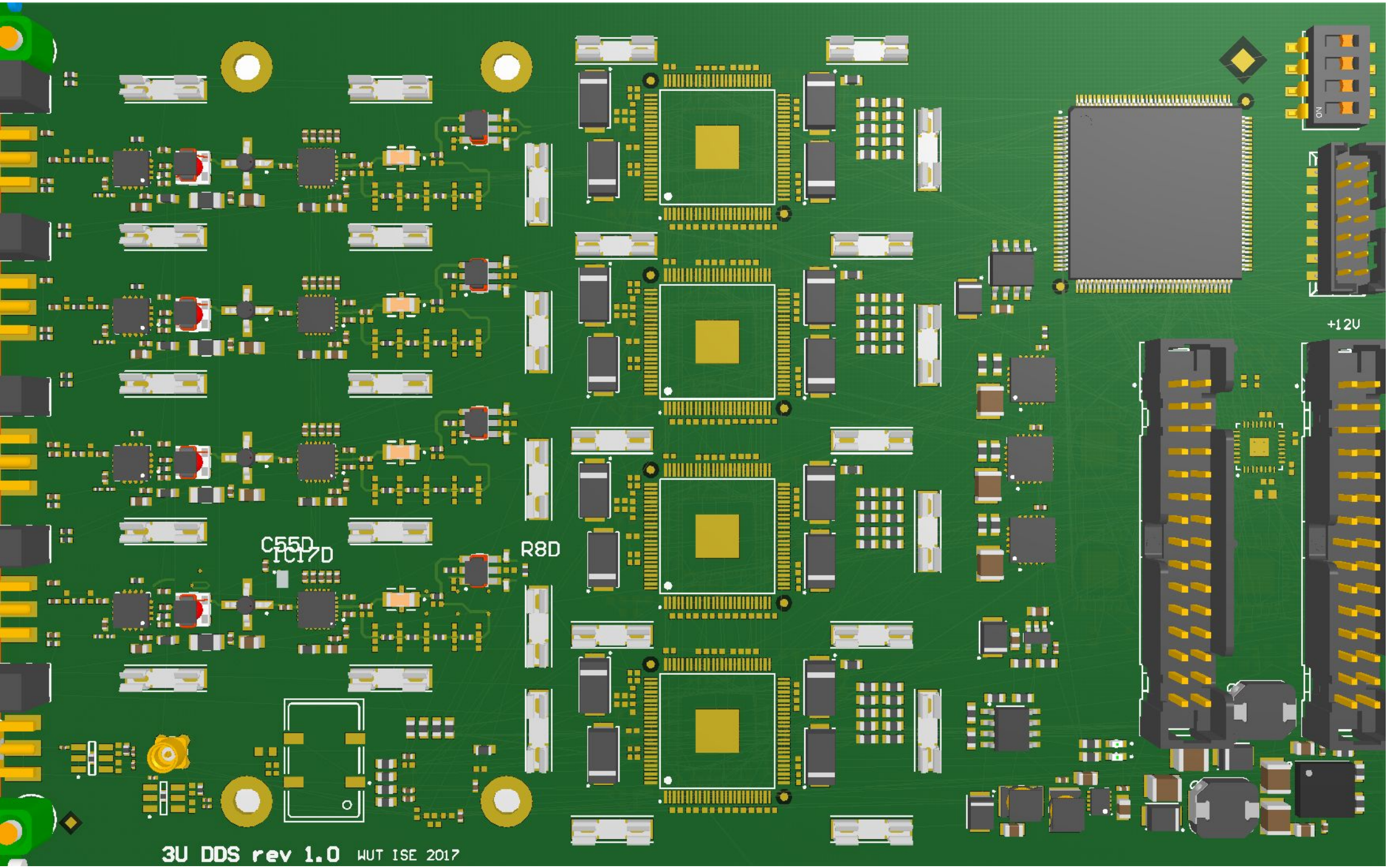
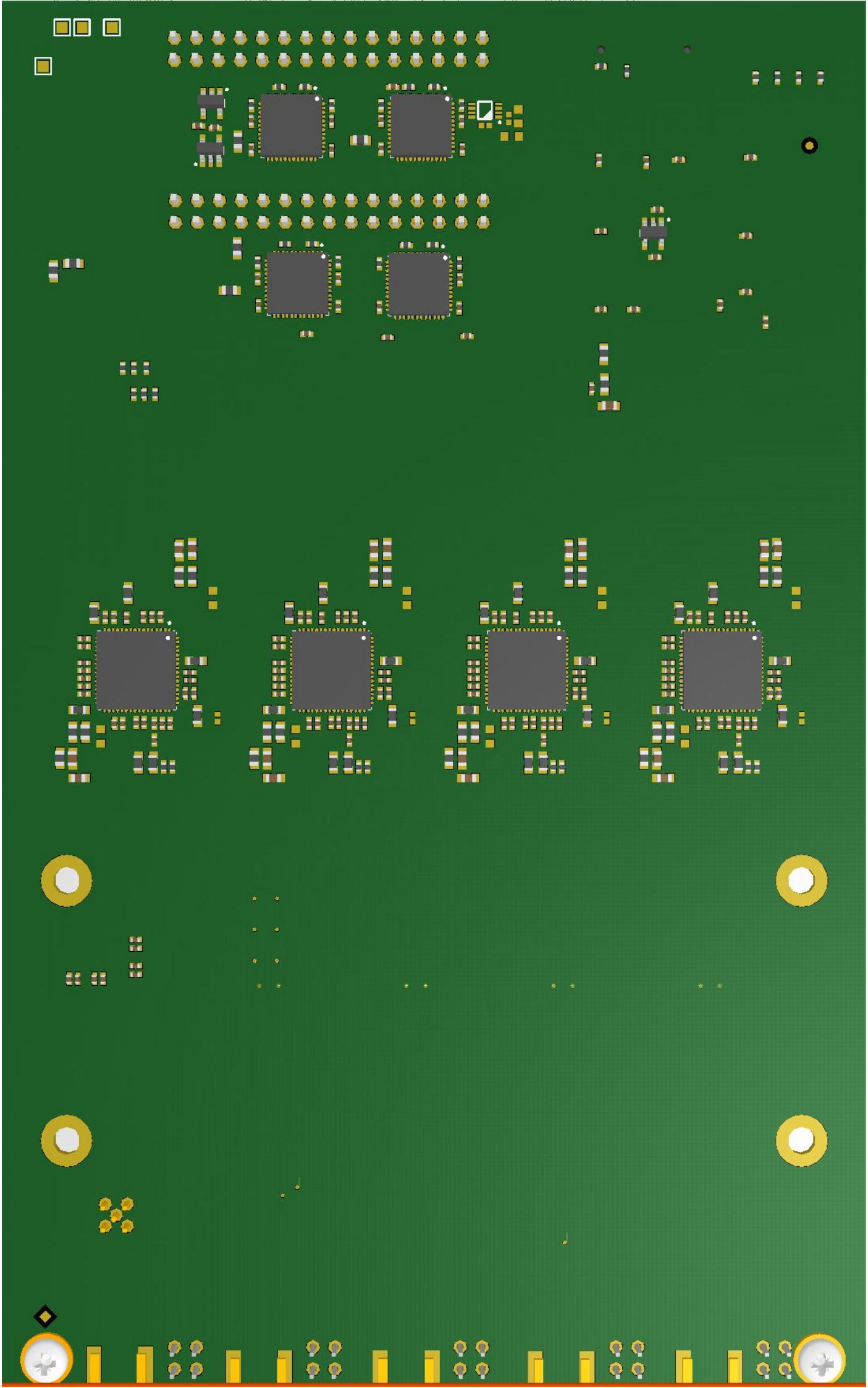
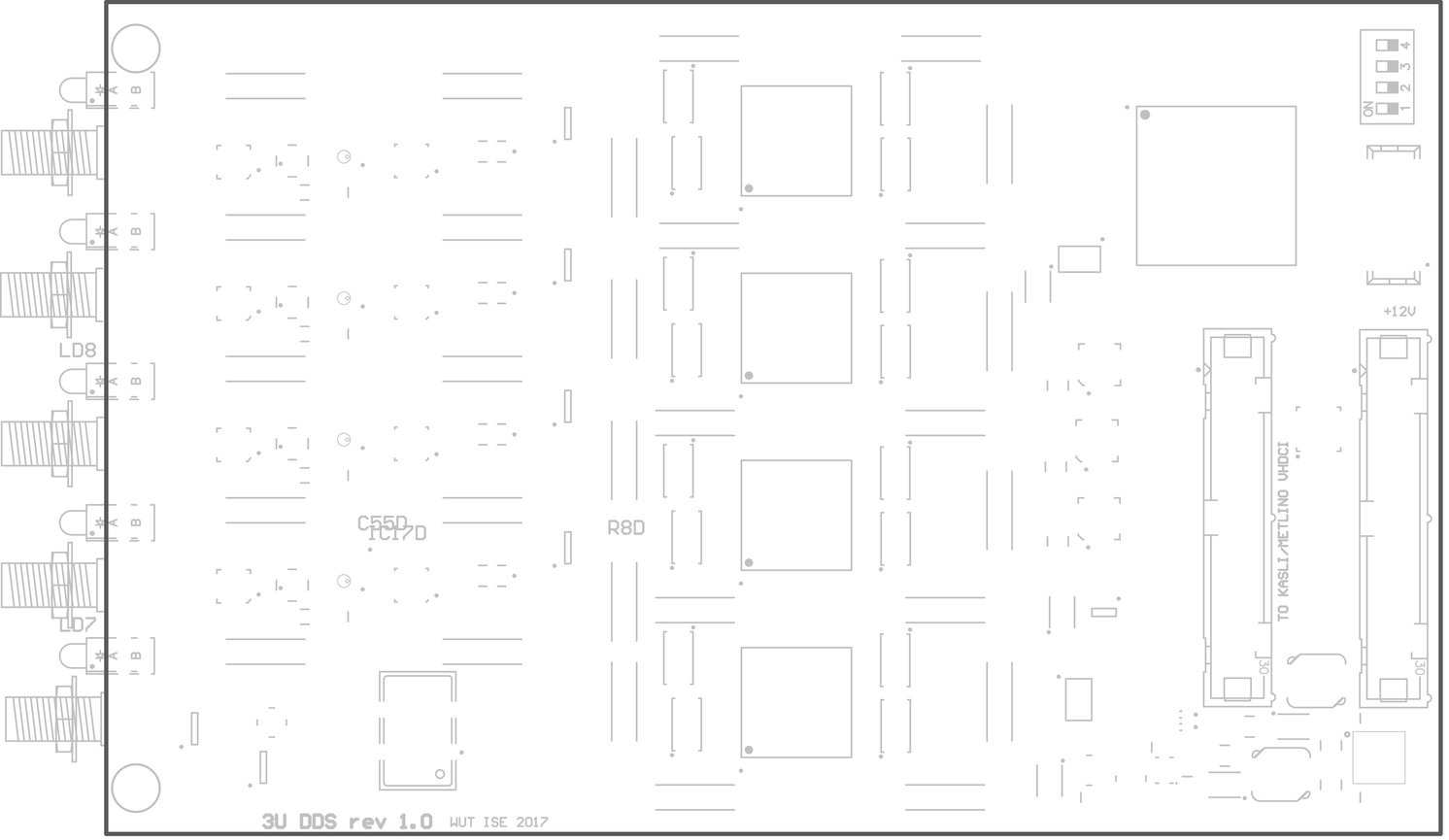

C55D
IC17D
R8D
+12V
3U DDS rev 1.0 WUT ISE 2017





C55C IC17C R8C

C55B IC17B R8B

C55A IC17A R8A

R15D R12D

R15C R12C R10C

R15B R12B R10B

R15A R12A R10A

TP9 TP8 TP7 TP6 TP5

R102 R101 R95 C71 R76 C68 R72 C66 R109 R110 R71 C65 R70 R108 R34 C56 R103 R22 U1 R17

C46 IC16 R6 C37 C42