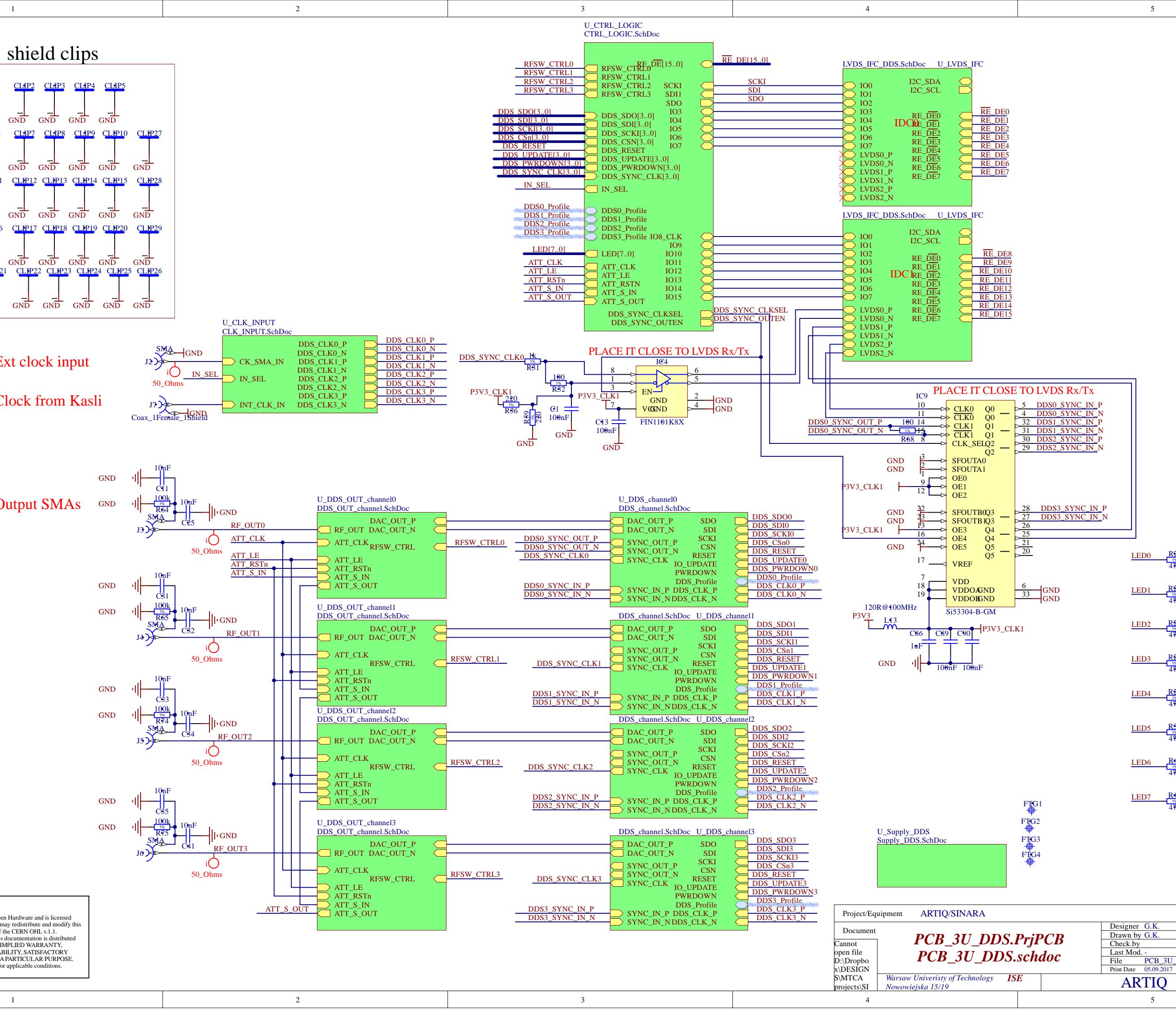
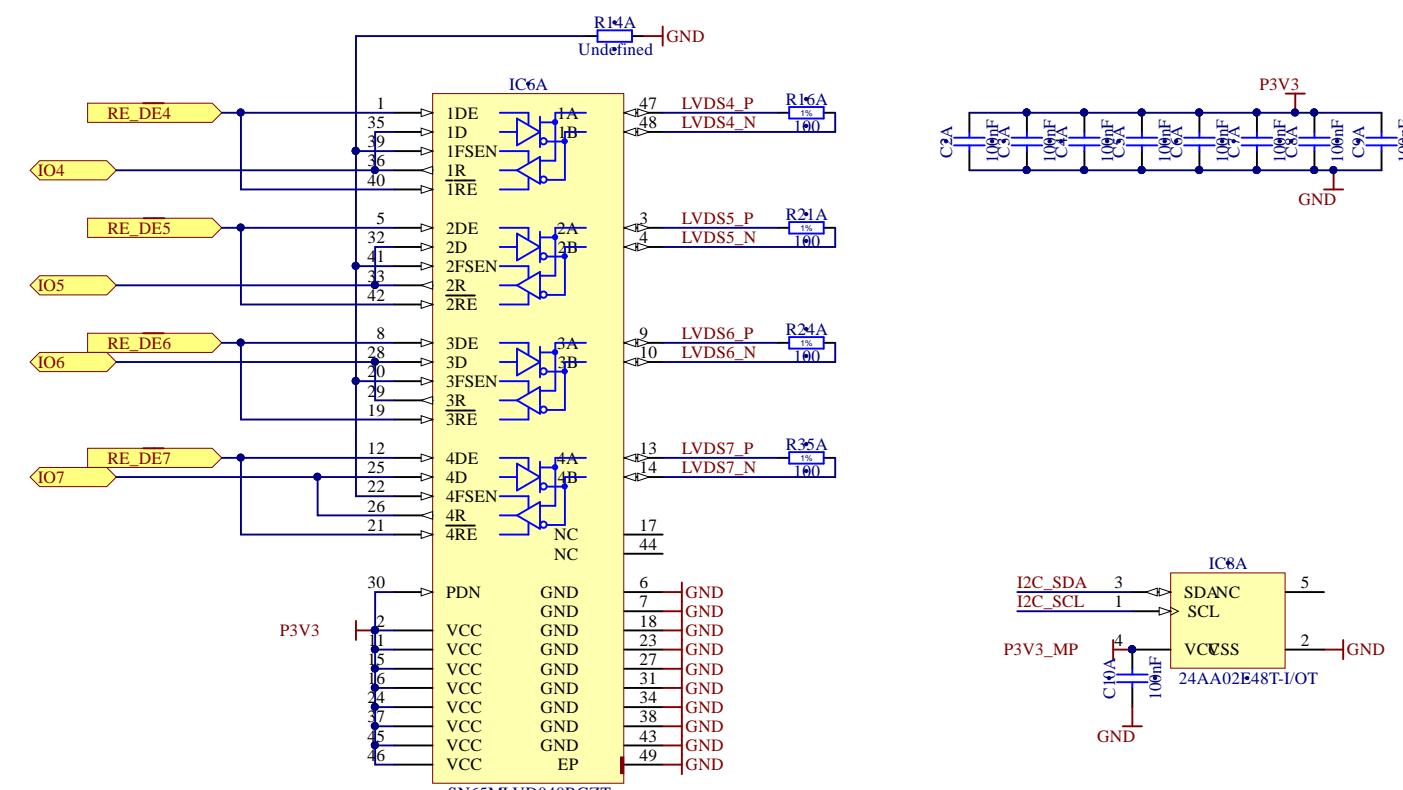
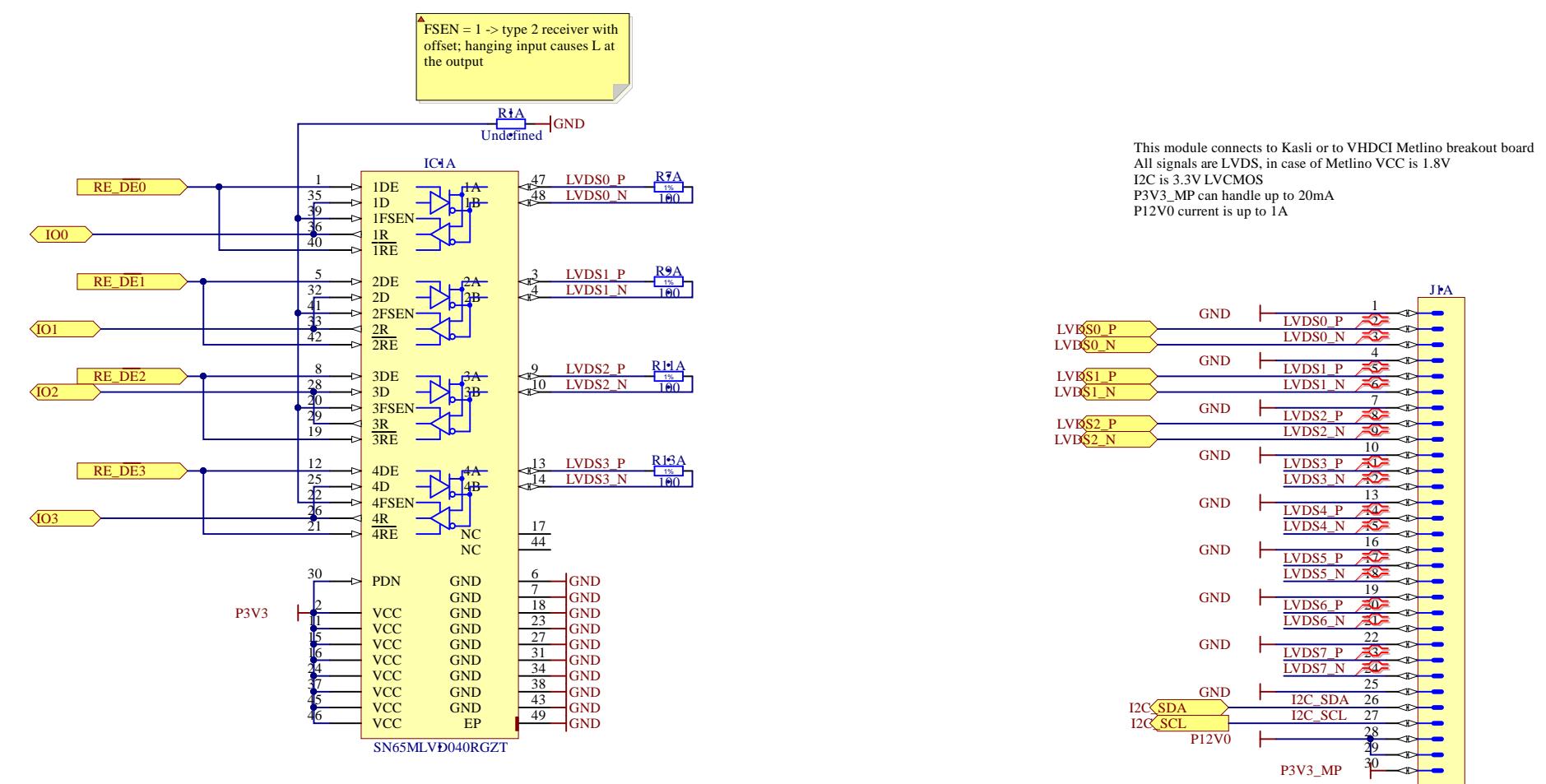
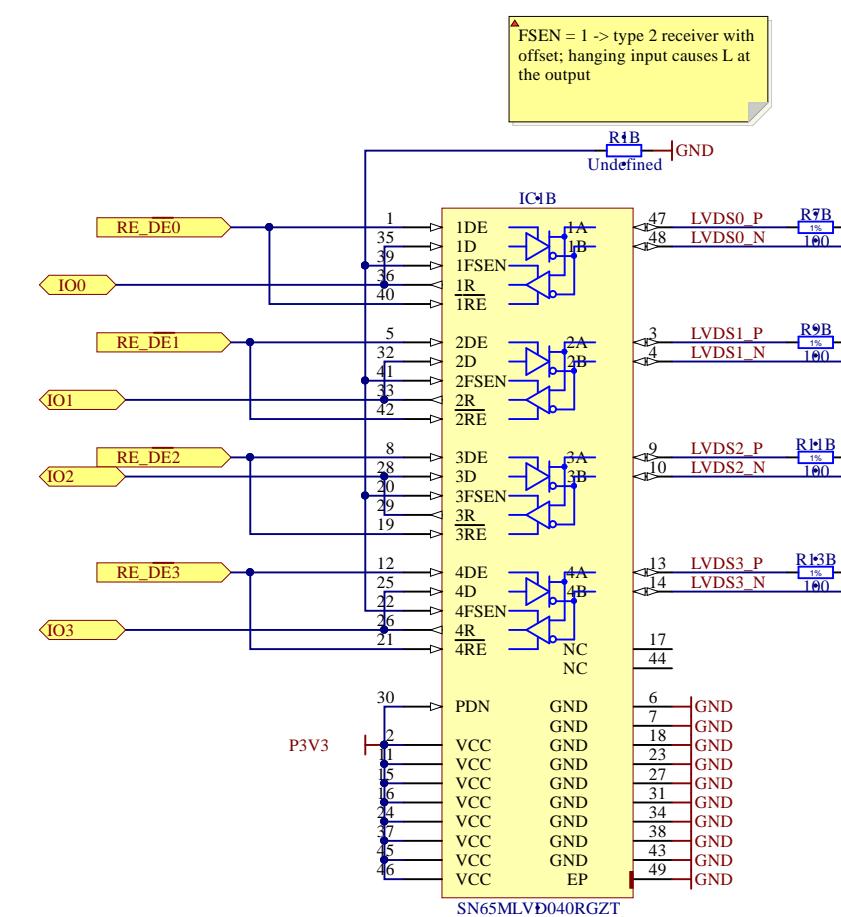


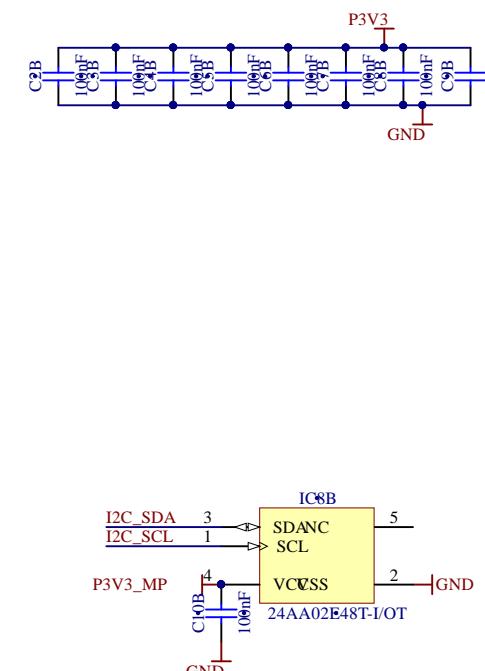
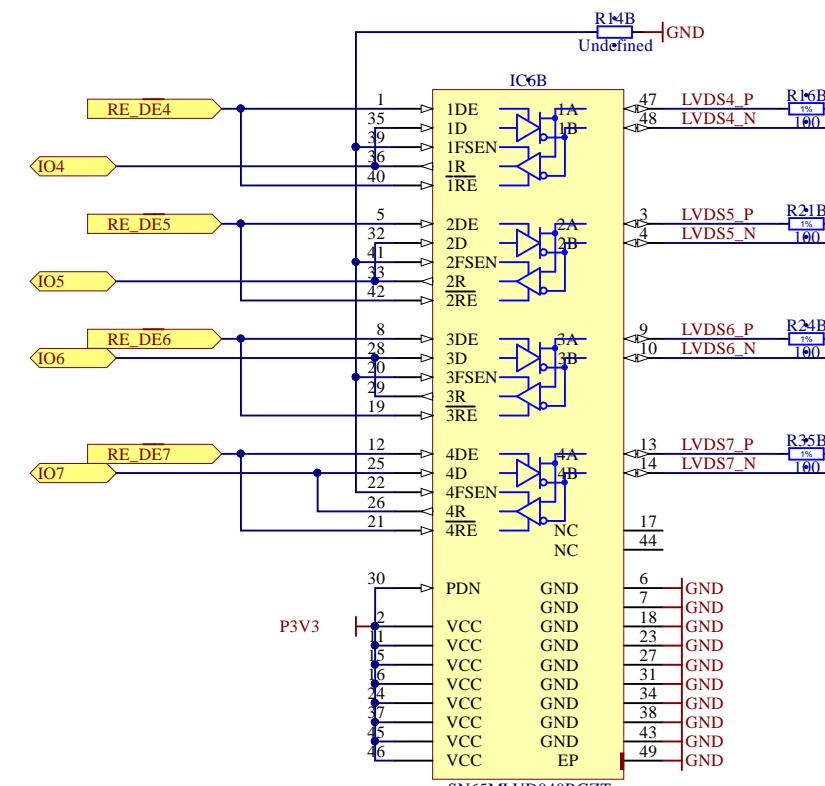
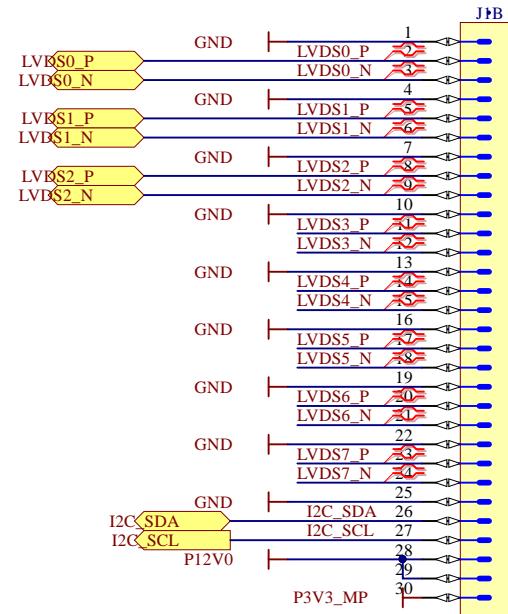
3U DDS rev 1.0 WUT ISE 2017







This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVC MOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



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Project/Equipment ARTIQ/SINARA

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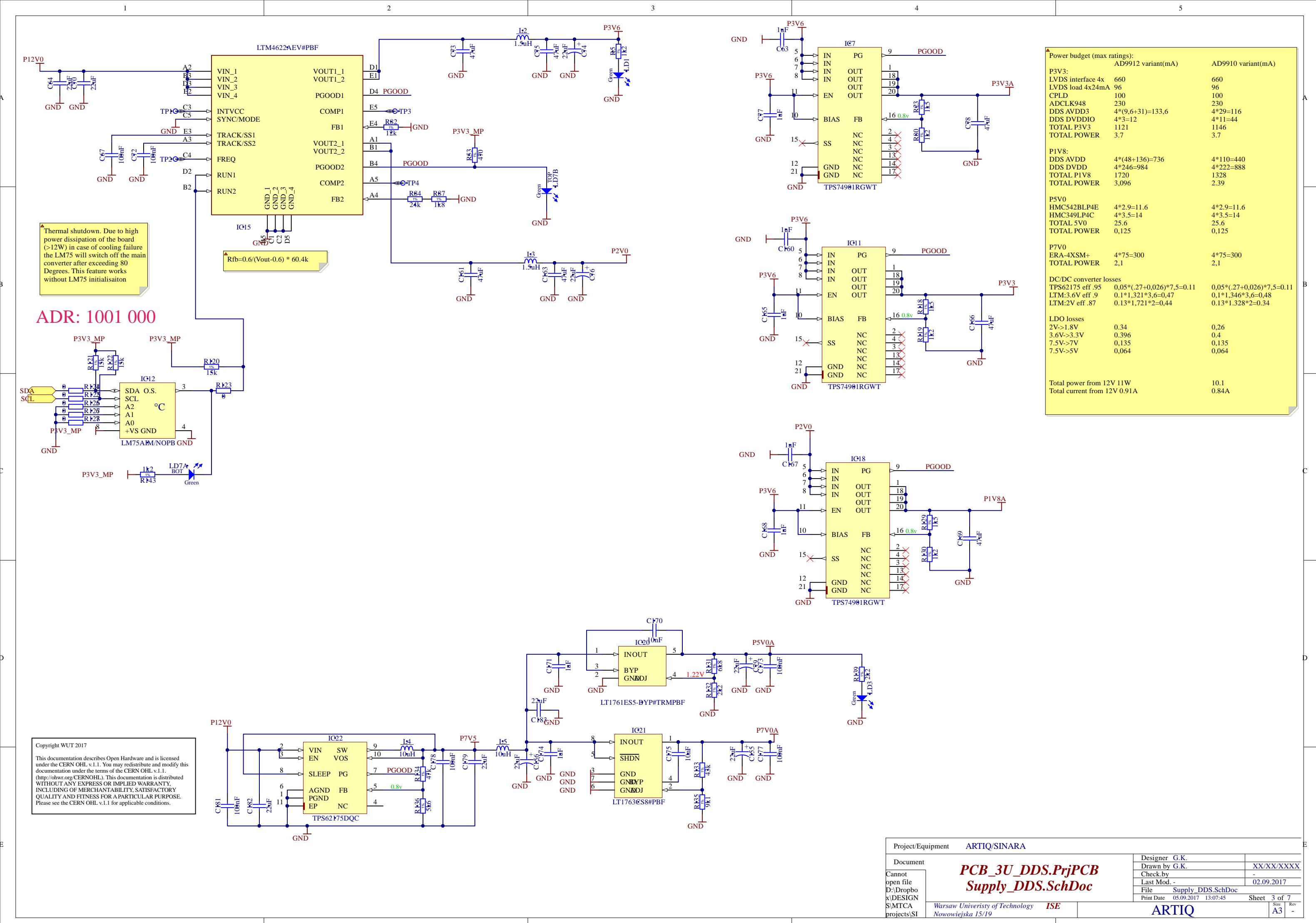
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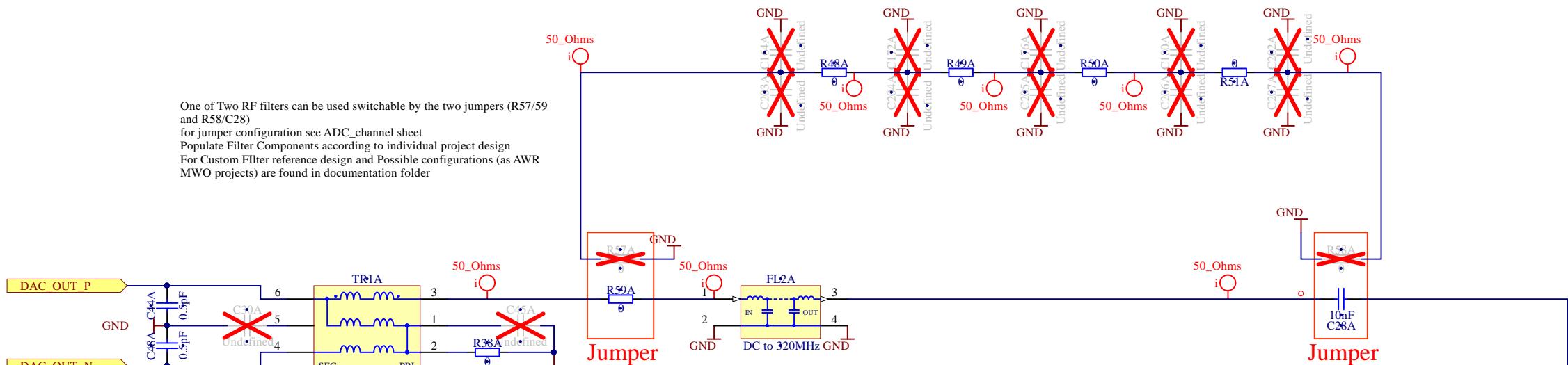
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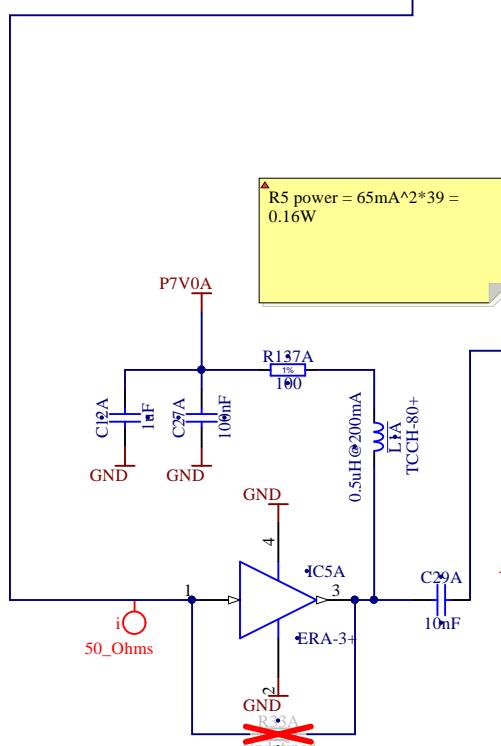
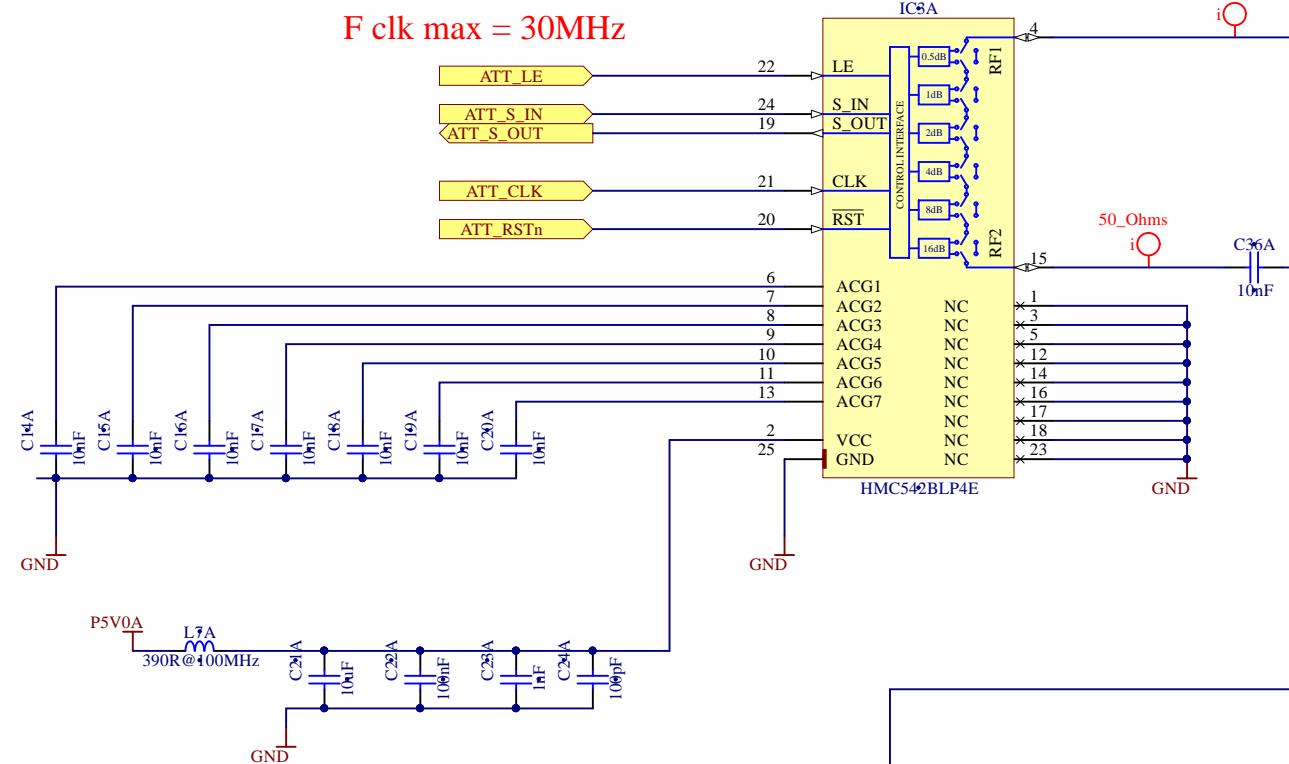
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A A

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom Filter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

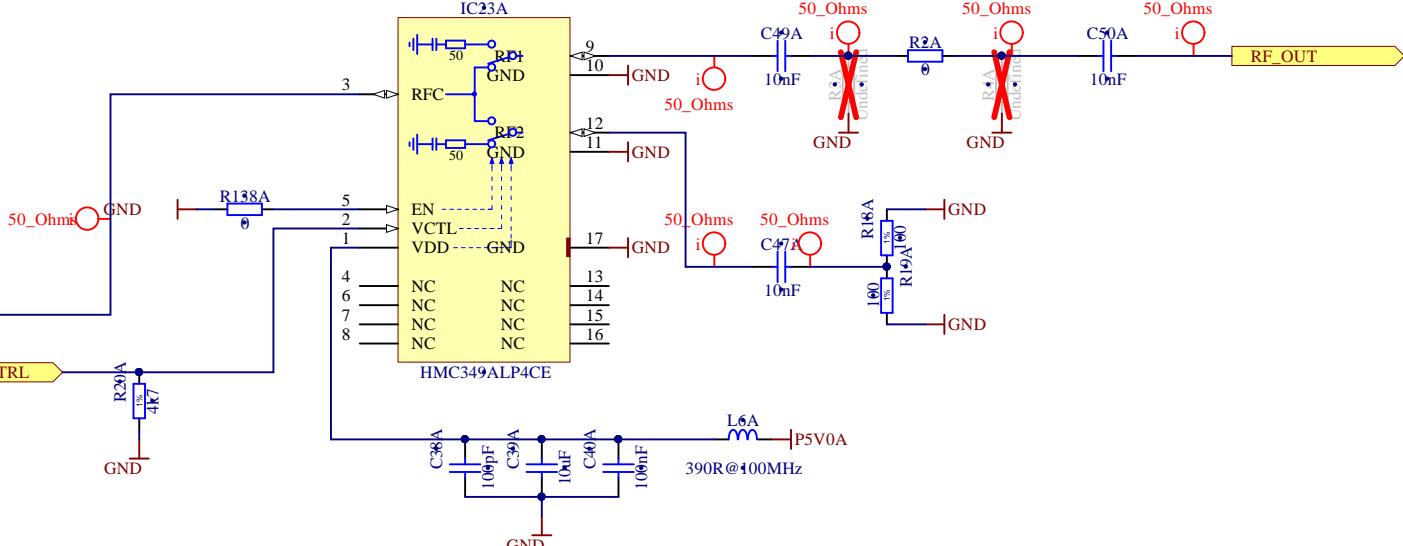


Digital Attenuator



Amplifier
+13dB @ 2GHz typ.

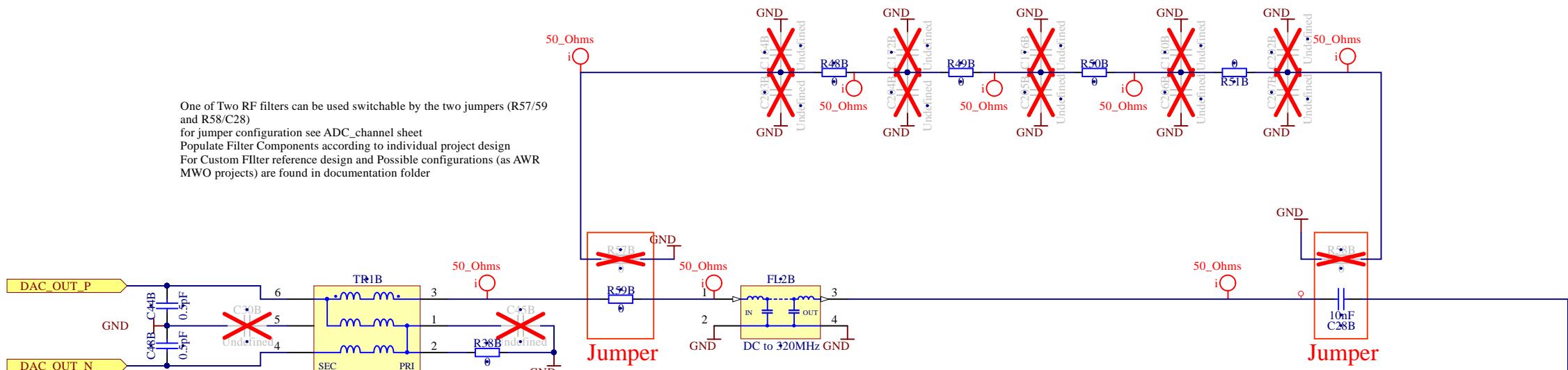
SPDT switch



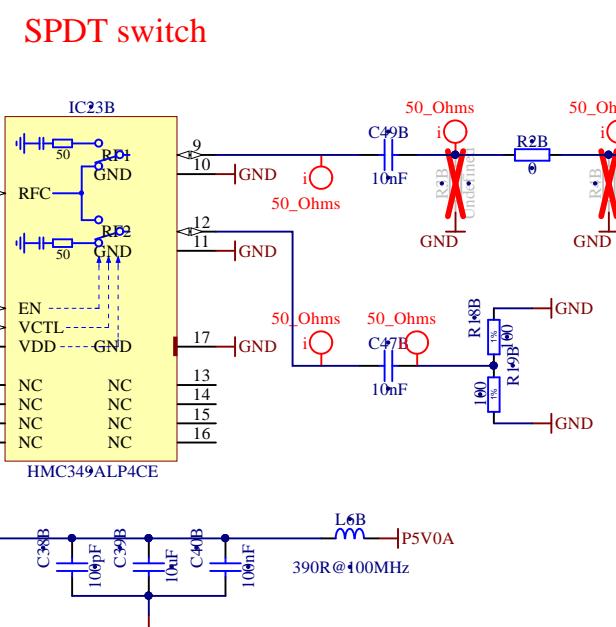
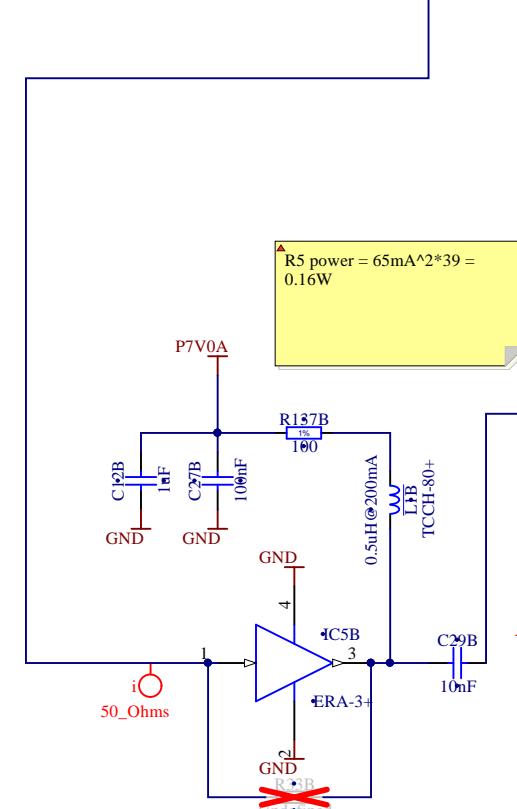
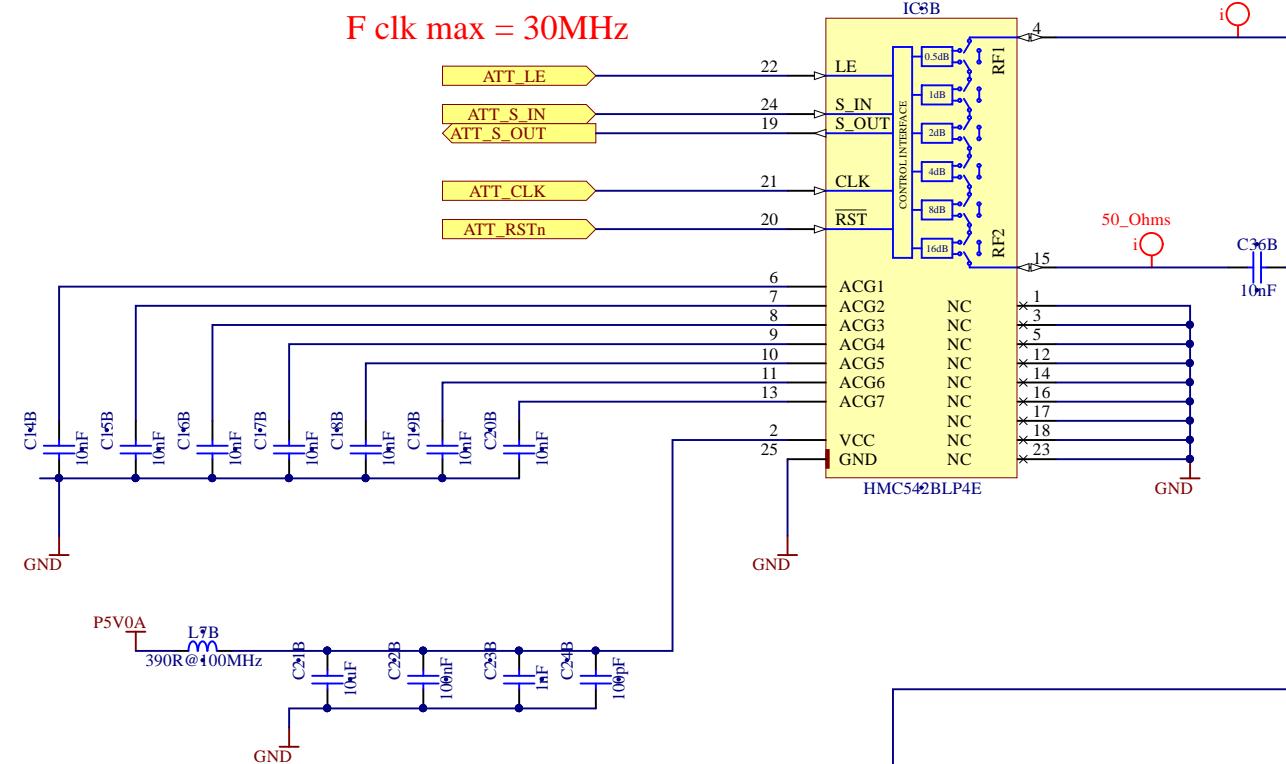
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for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
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Digital Attenuator



Amplifier +13dB @ 2GHz typ.

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ARTIQ

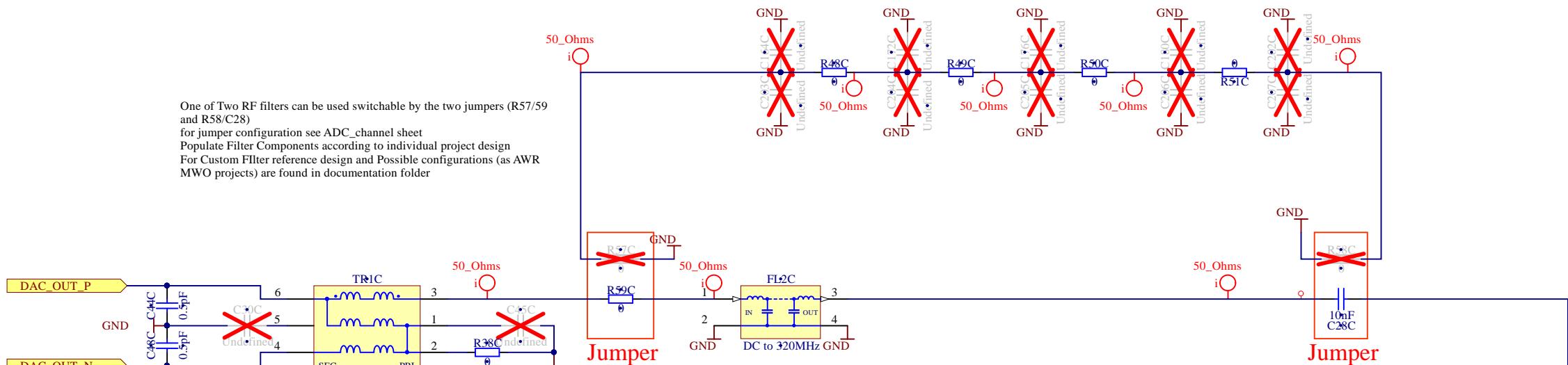
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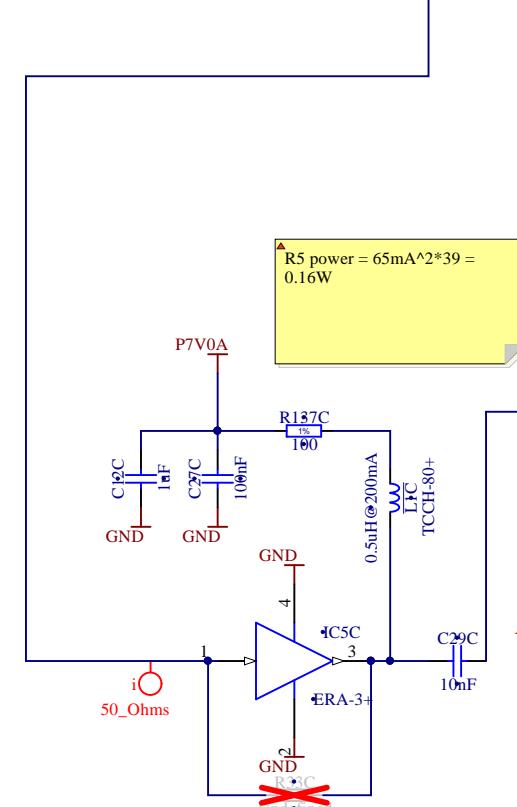
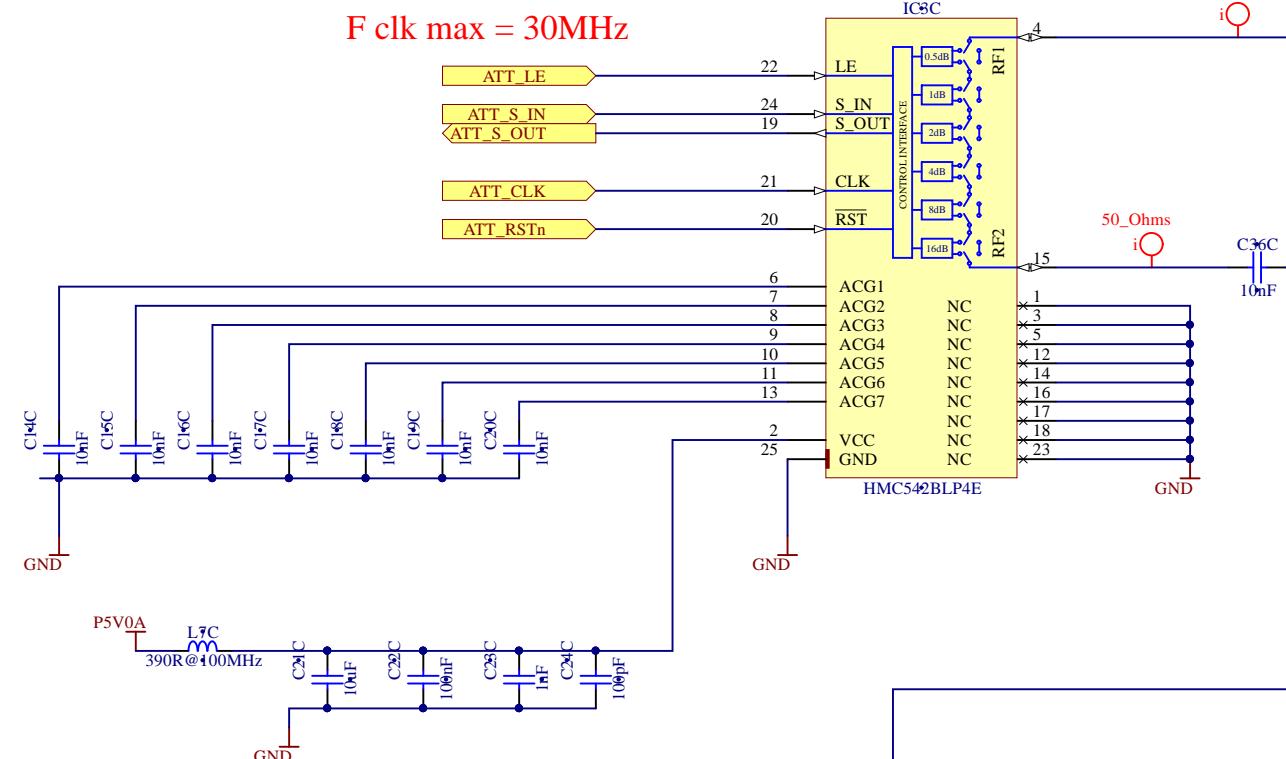
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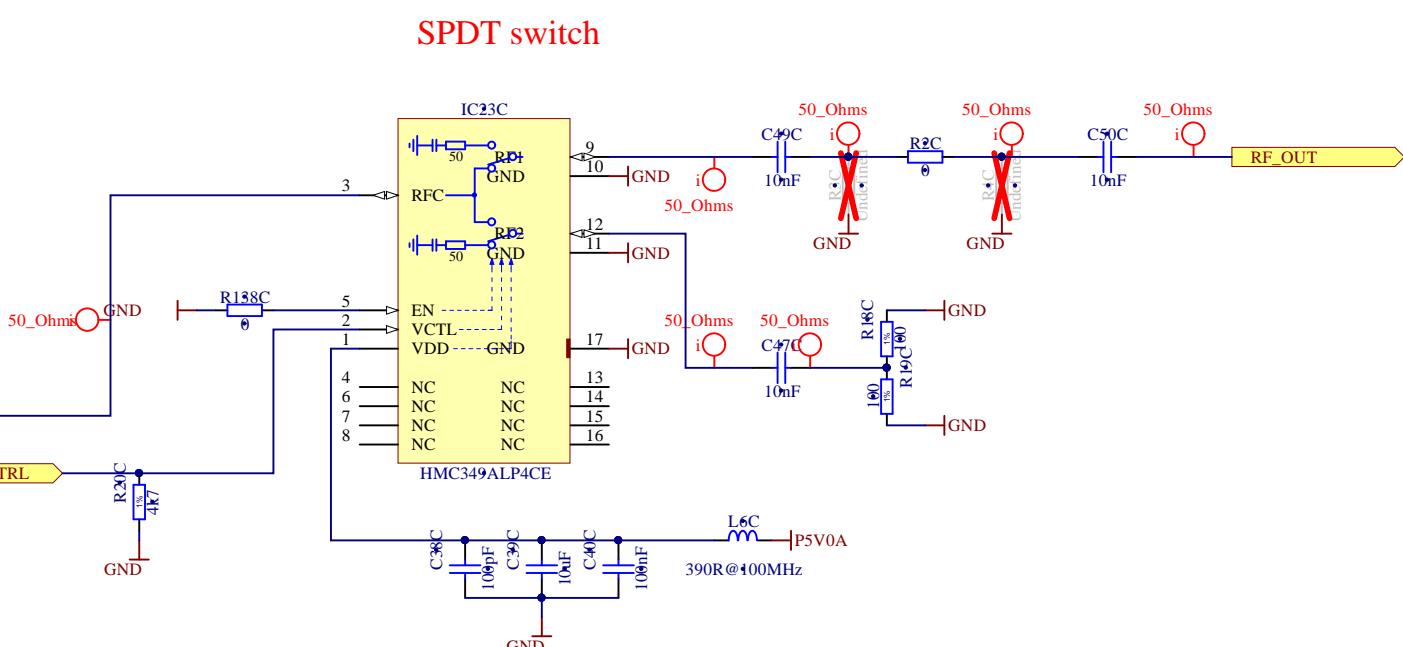
One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
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Populate Filter Components according to individual project design
For Custom Filter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder



Digital Attenuator



Amplifier
+13dB @ 2GHz typ.



Project/Equipment ARTIQ/SINARA
PCB_3U_DDS.PrjPCB
DDS_OUT_channel.SchDoc

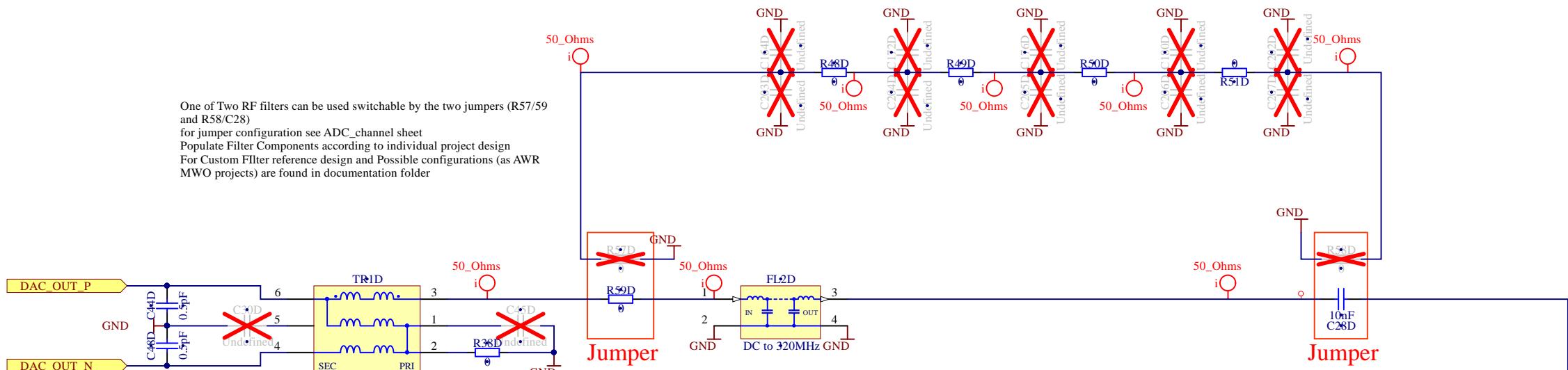
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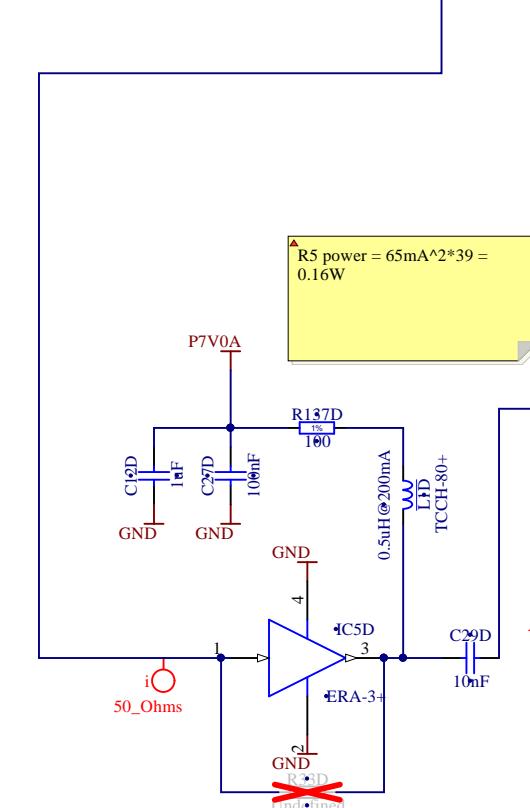
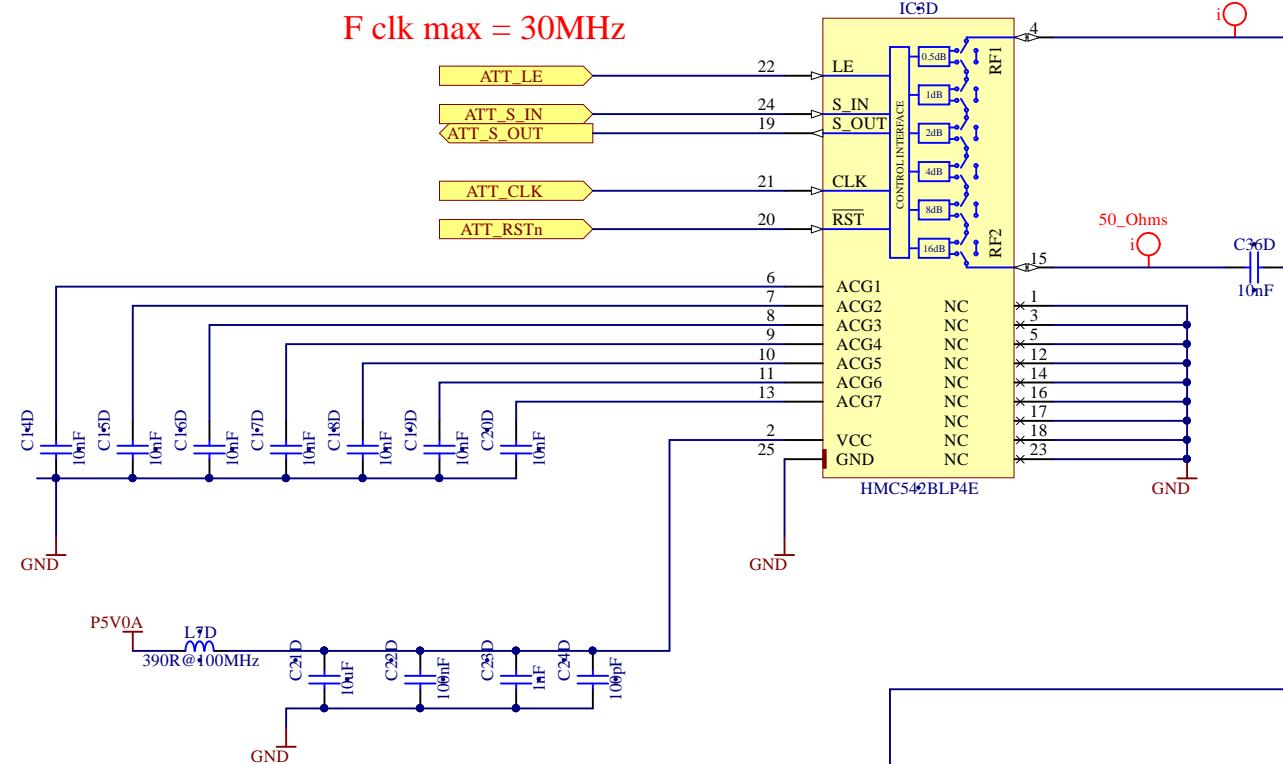
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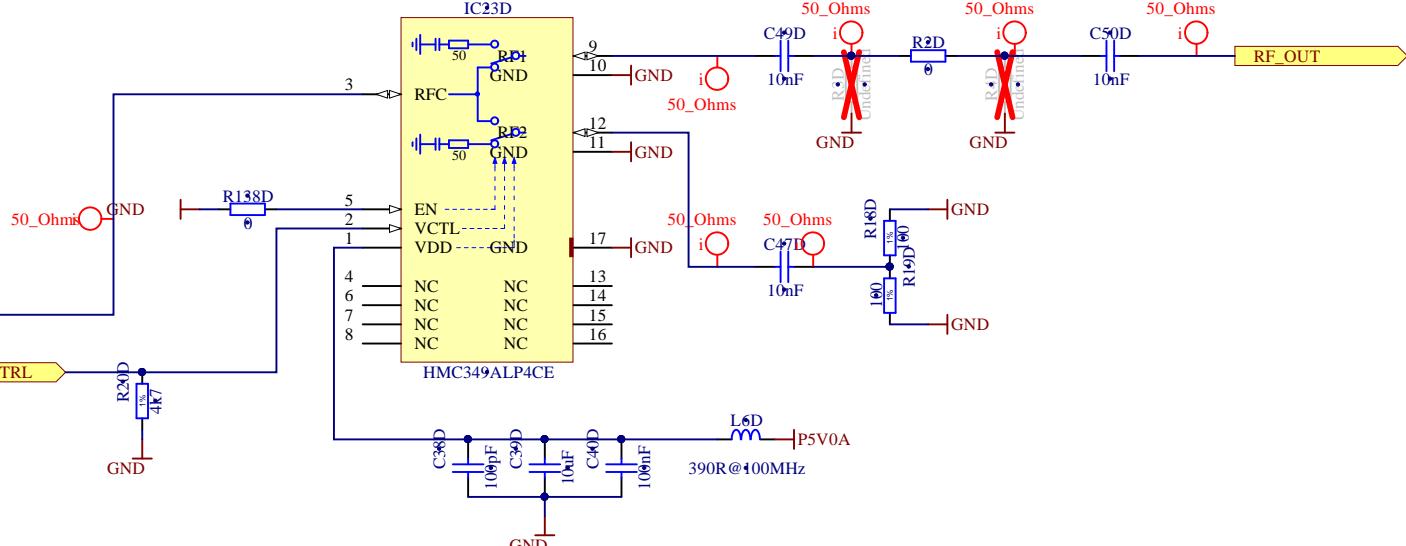
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Populate Filter Components according to individual project design
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Digital Attenuator



SPDT switch



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Project/Equipment ARTIQ/SINARA

**PCB_3U_DDS.PrjPCB
DDS_OUT_channel.SchDoc**

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Nowowiejska 15/19

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ARTIQ

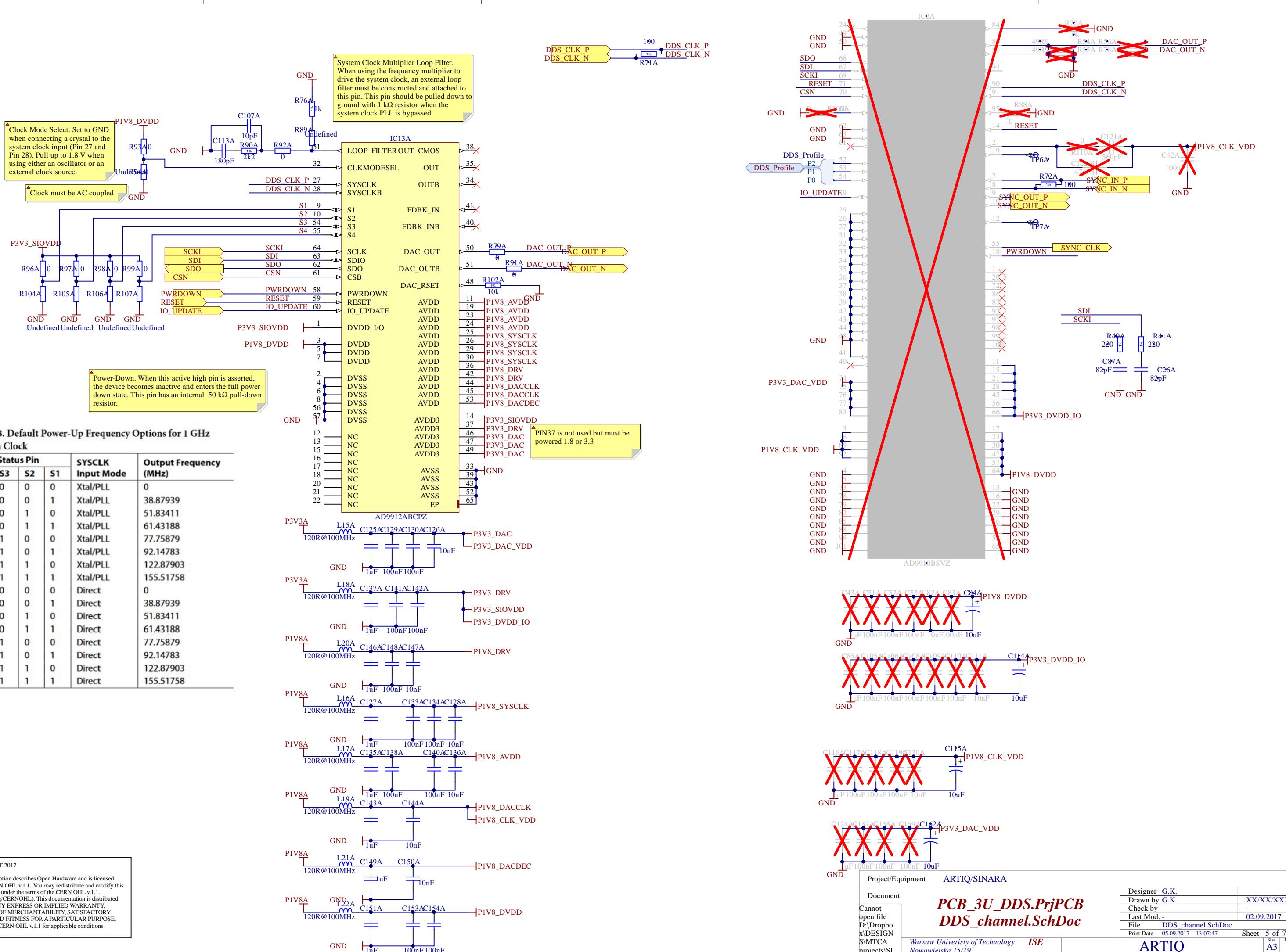
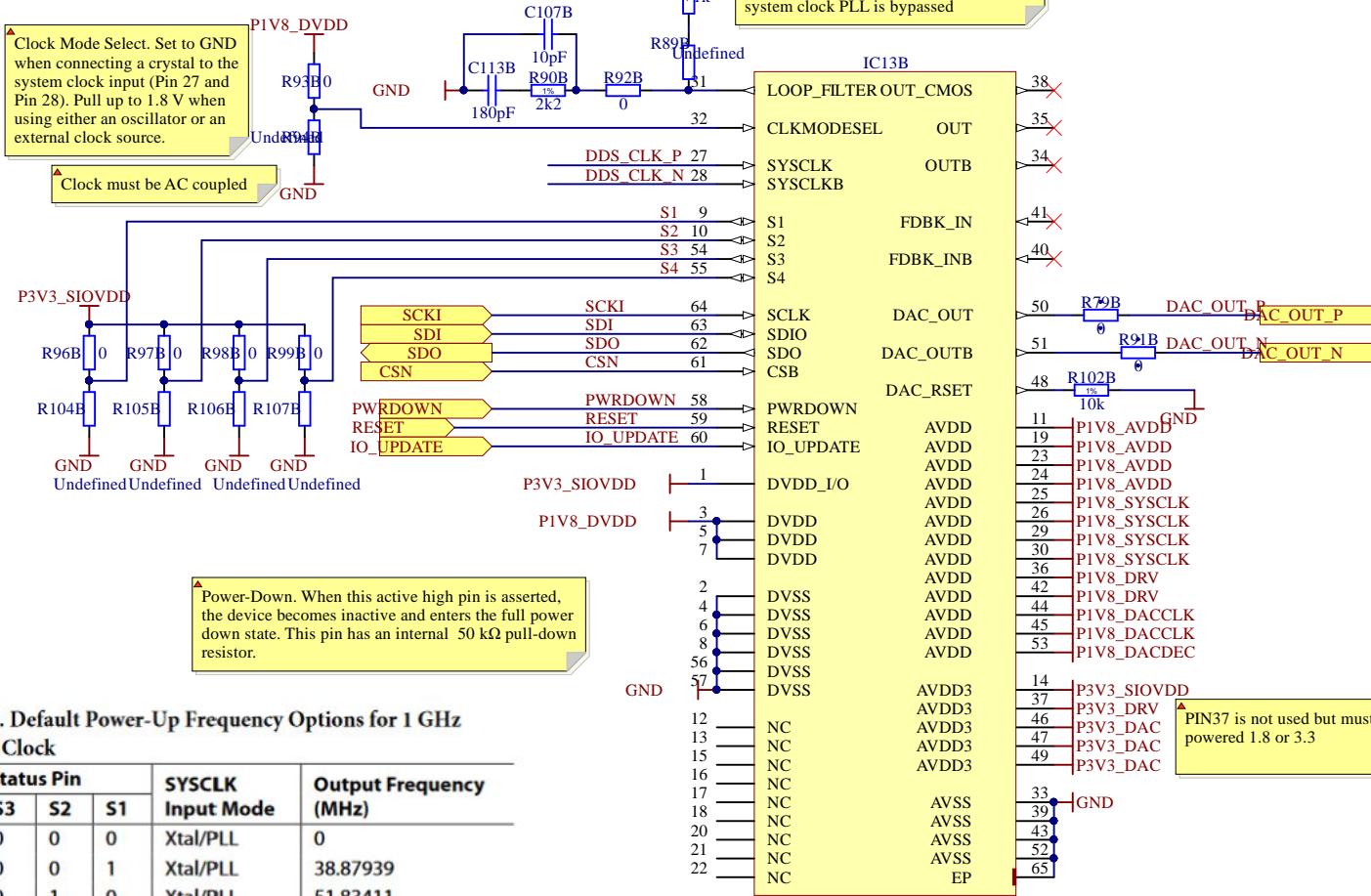


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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AD9912ABCPZ

P3V3A L15B C125BC129BC130BC126B 120R@100MHz P3V3_DAC 10nF

GND 1uF 100nF 100nF P3V3_DAC_VDD

P3V3A L18B C137B C141BC142B 120R@100MHz P3V3_DRV 10nF

GND 1uF 100nF 100nF P3V3_SIOVDD

P1V8A L20B C146BC148BC147B 120R@100MHz P1V8_DRV 10nF

GND 1uF 100nF 100nF P1V8_DVDD_IO

P1V8A L16B C127B C133BC134BC128B 120R@100MHz P1V8_SYSCLK 10nF

GND 1uF 100nF 100nF P1V8_AVDD

P1V8A L17B C135BC138B C140BC136B 120R@100MHz P1V8_DACCLK 10nF

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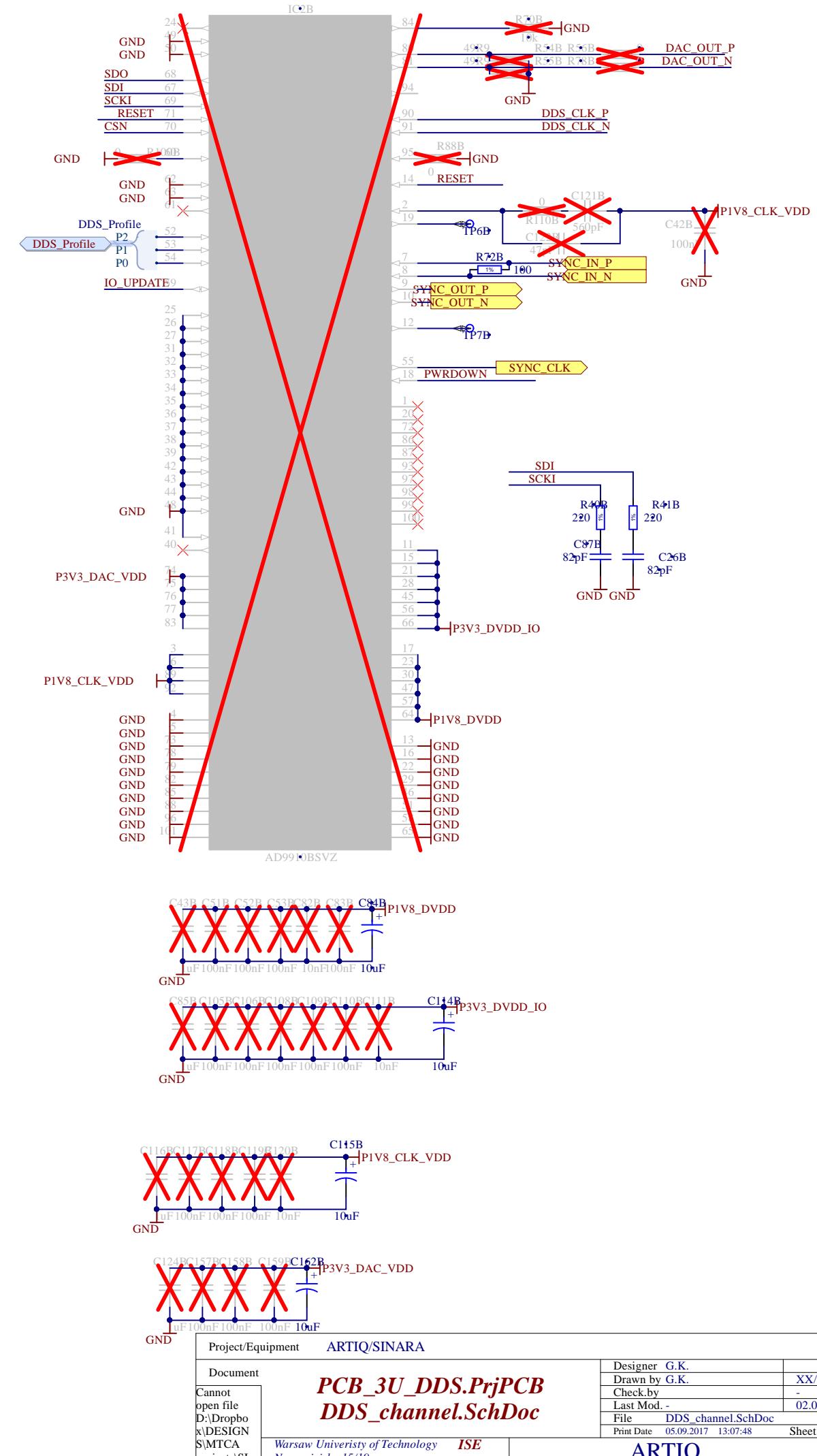
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GND 1uF 100nF 100nF P1V8_CLK_VDD

P1V8A L22B C151B C153BC154B 120R@100MHz P1V8_DVDD 10nF

GND 1uF 100nF 100nF P1V8_CLK_VDD



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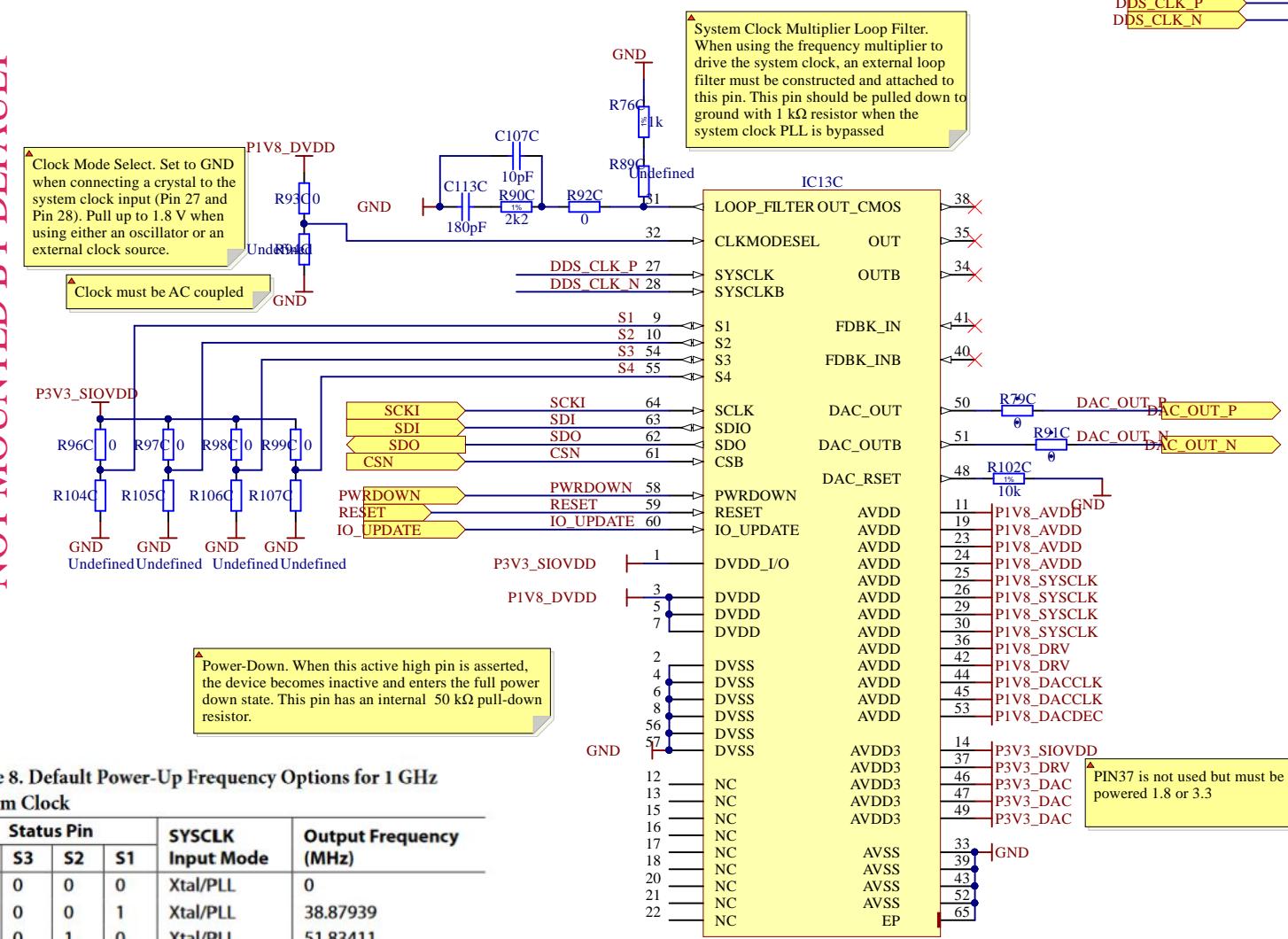
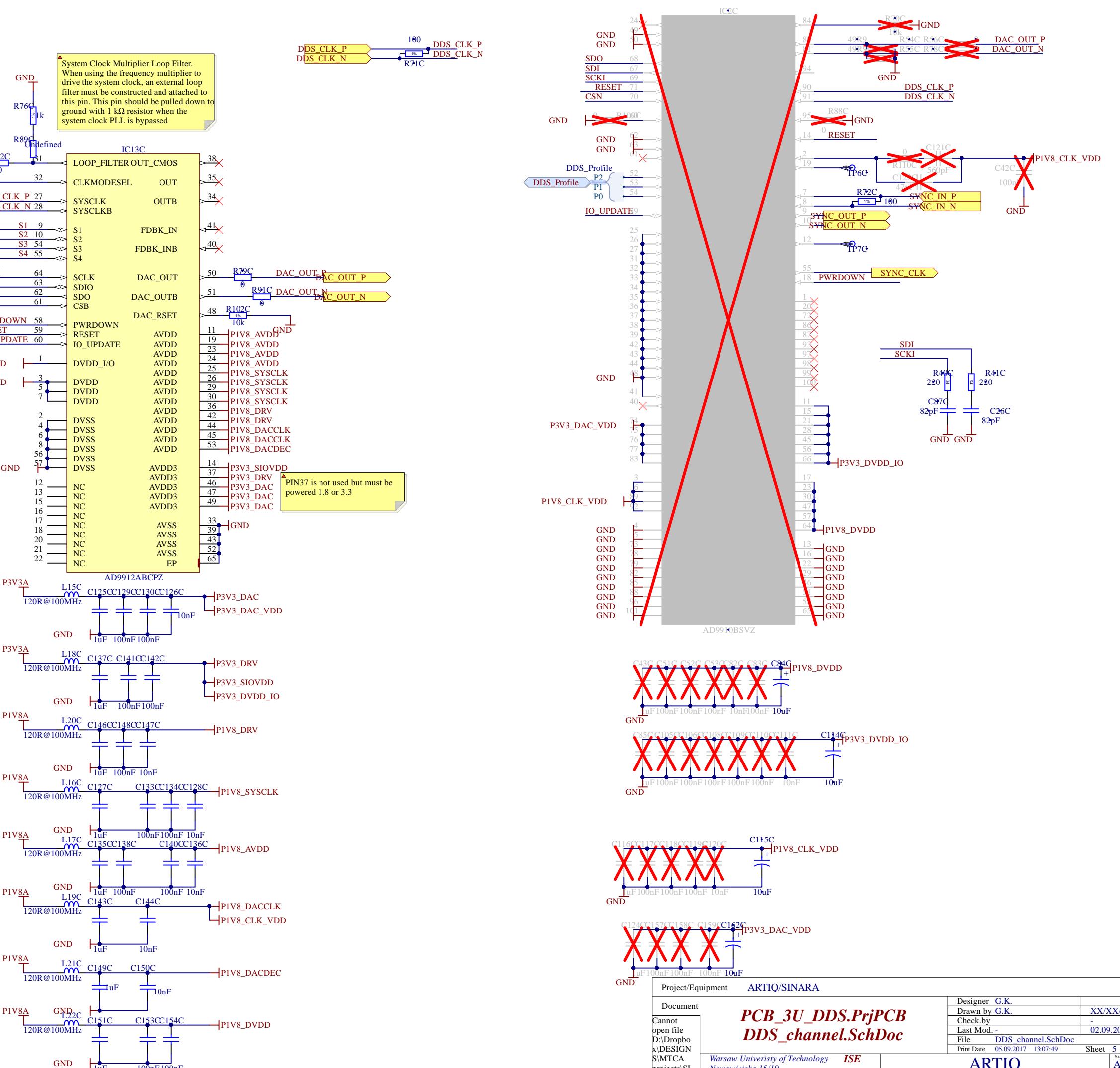


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

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0	1	1	1	Xtal/PLL	155.51758
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1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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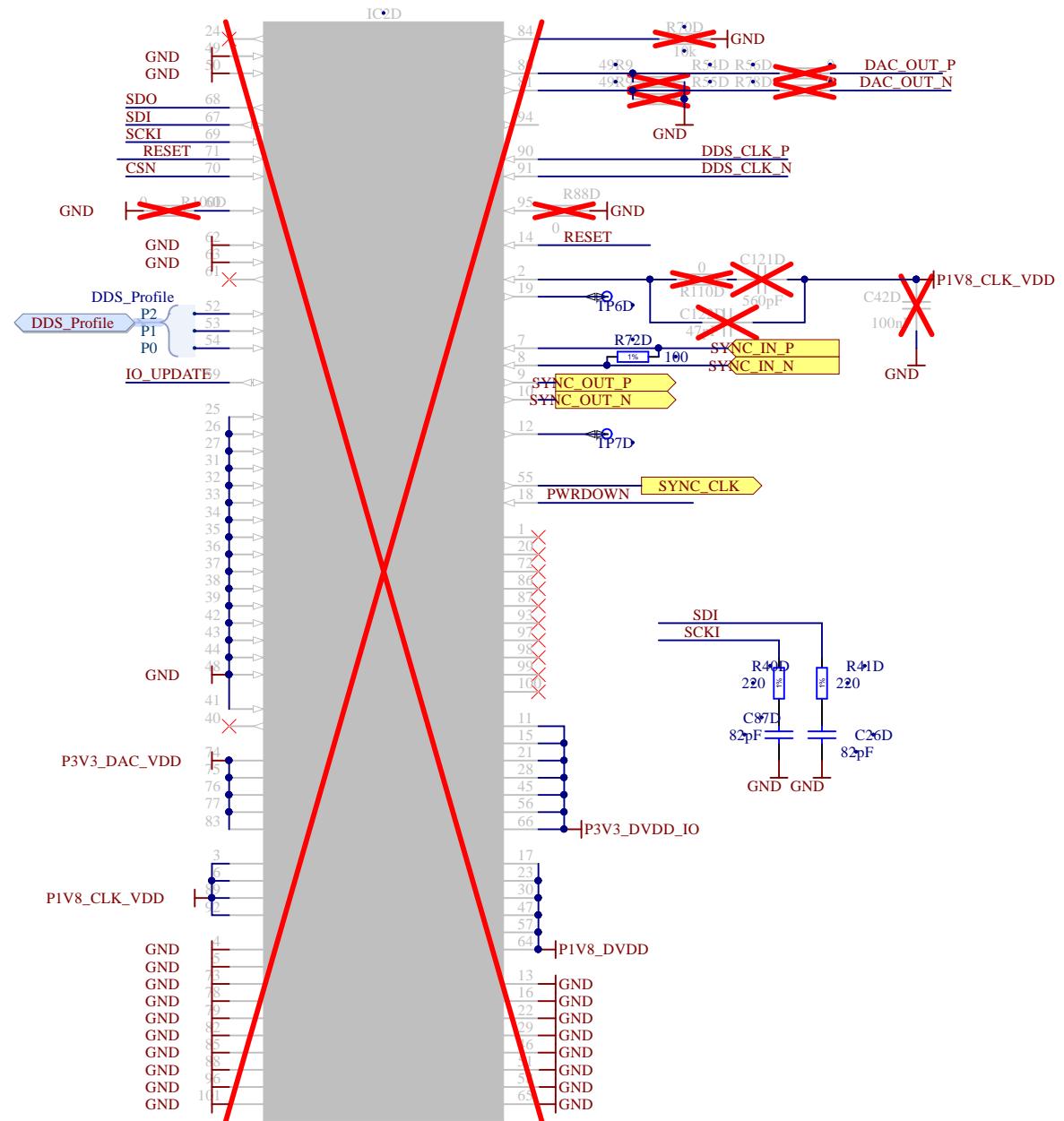
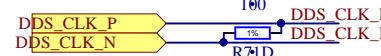
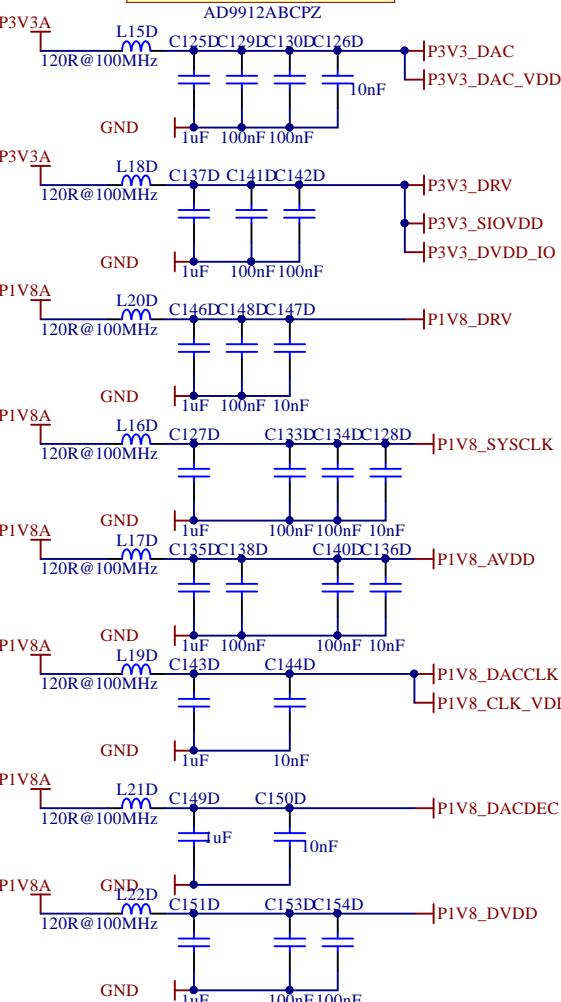
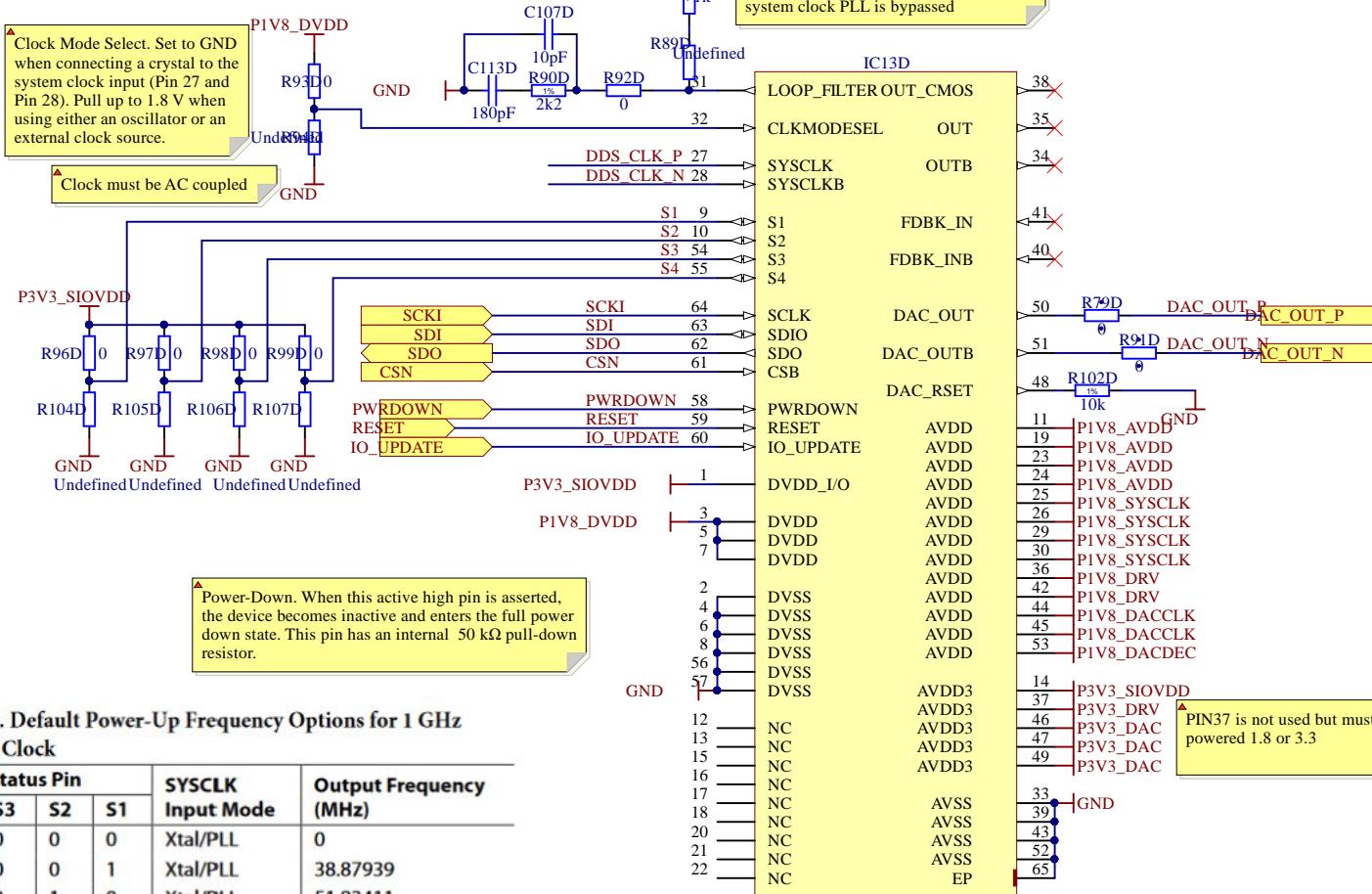
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Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

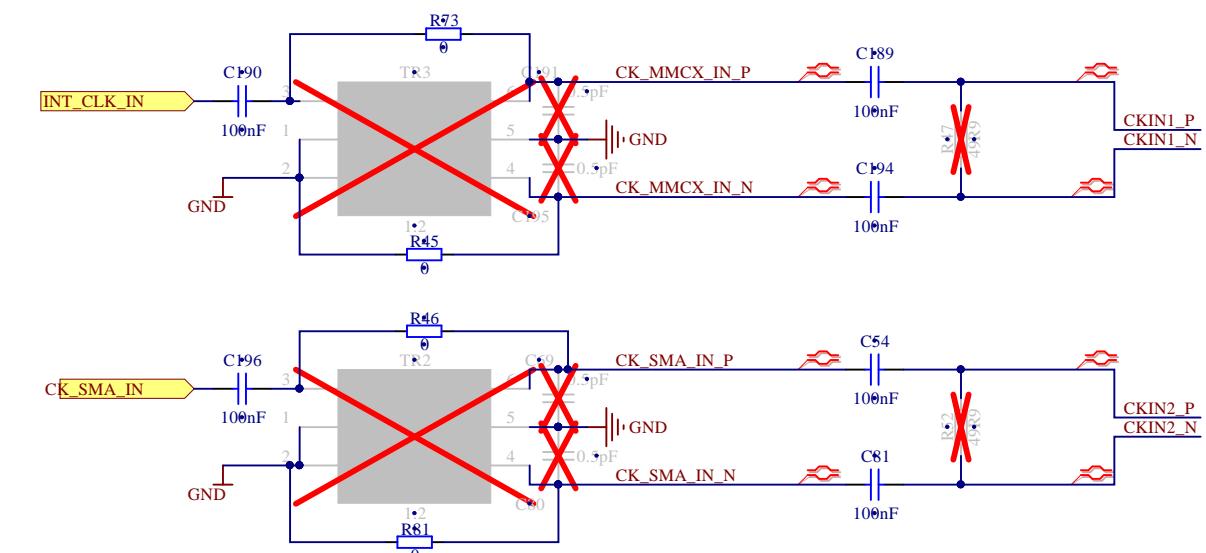
Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
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0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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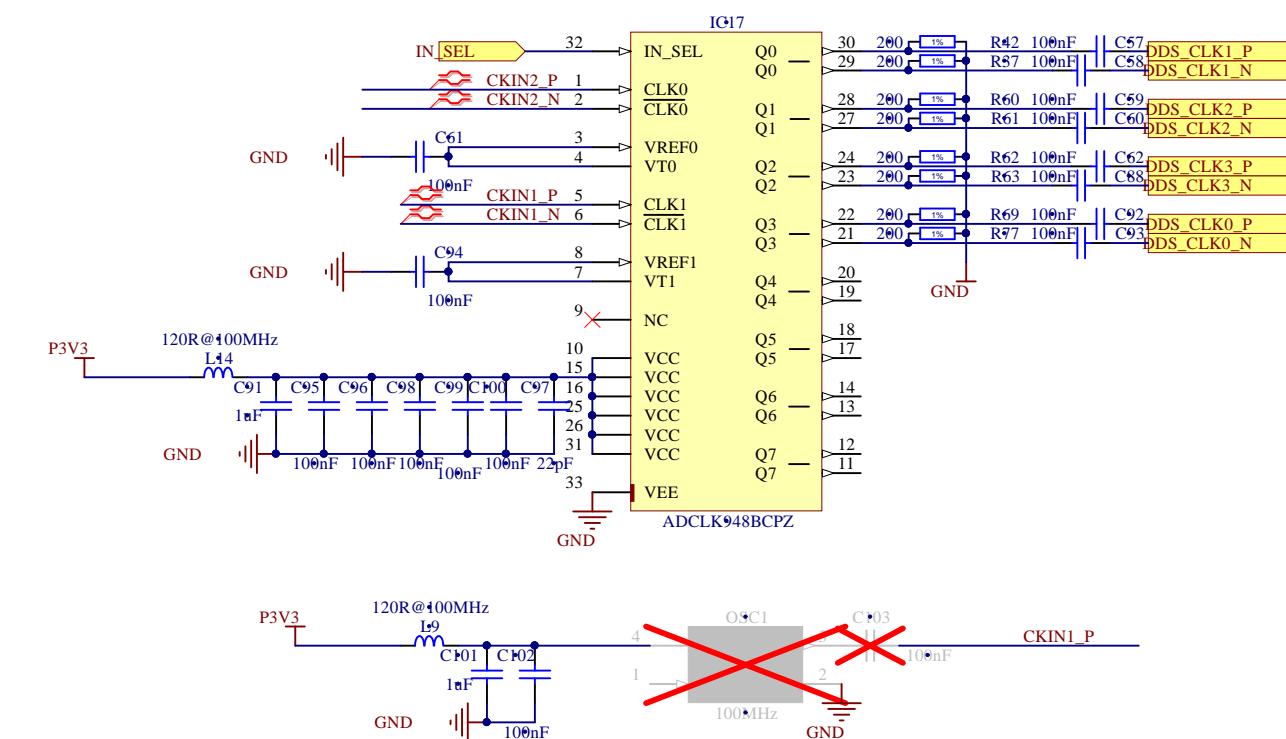


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Sheet 5 of 7		



AC-Coupled Input
Termination, Such as
LVDS and LEVPEC

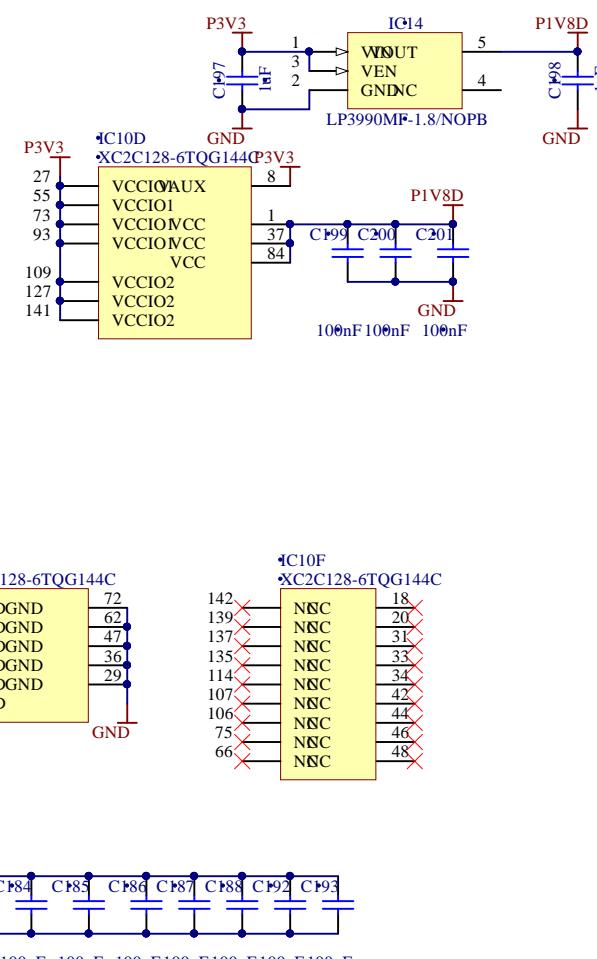
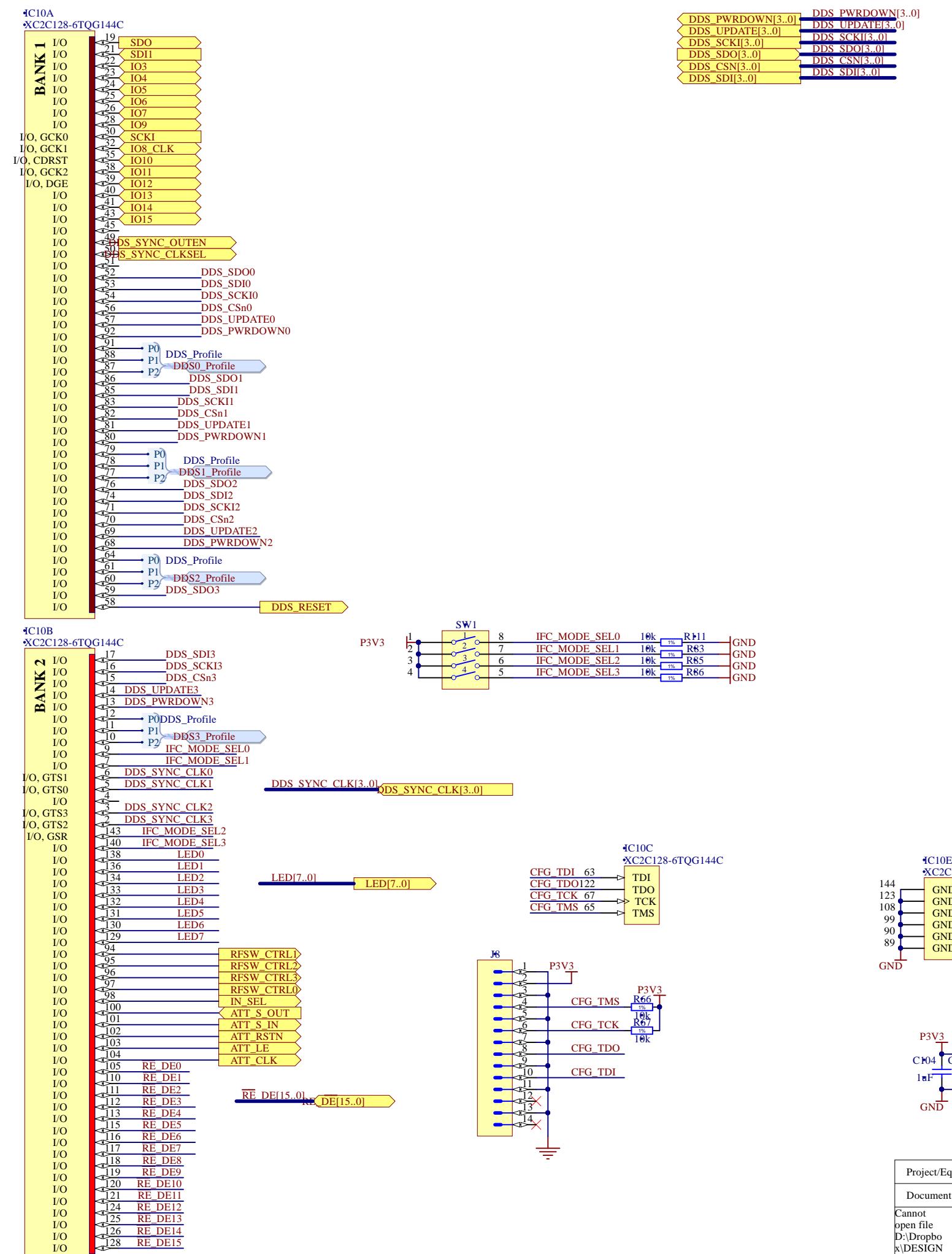


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PCB_3U_DDS.PrjPCB CLK_INPUT.SchDoc

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