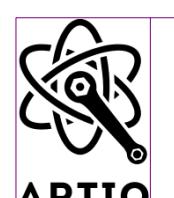
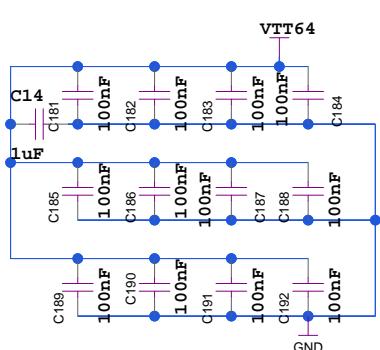
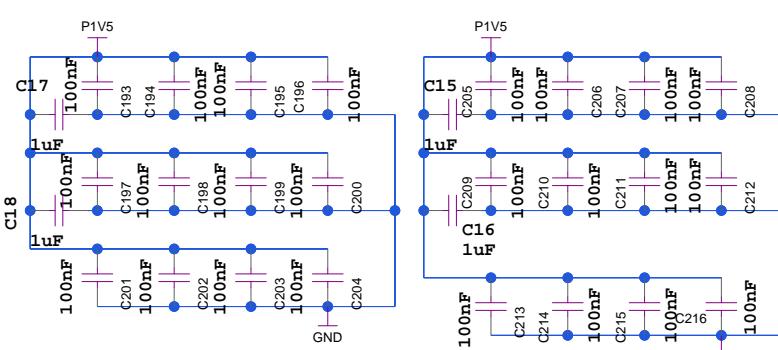
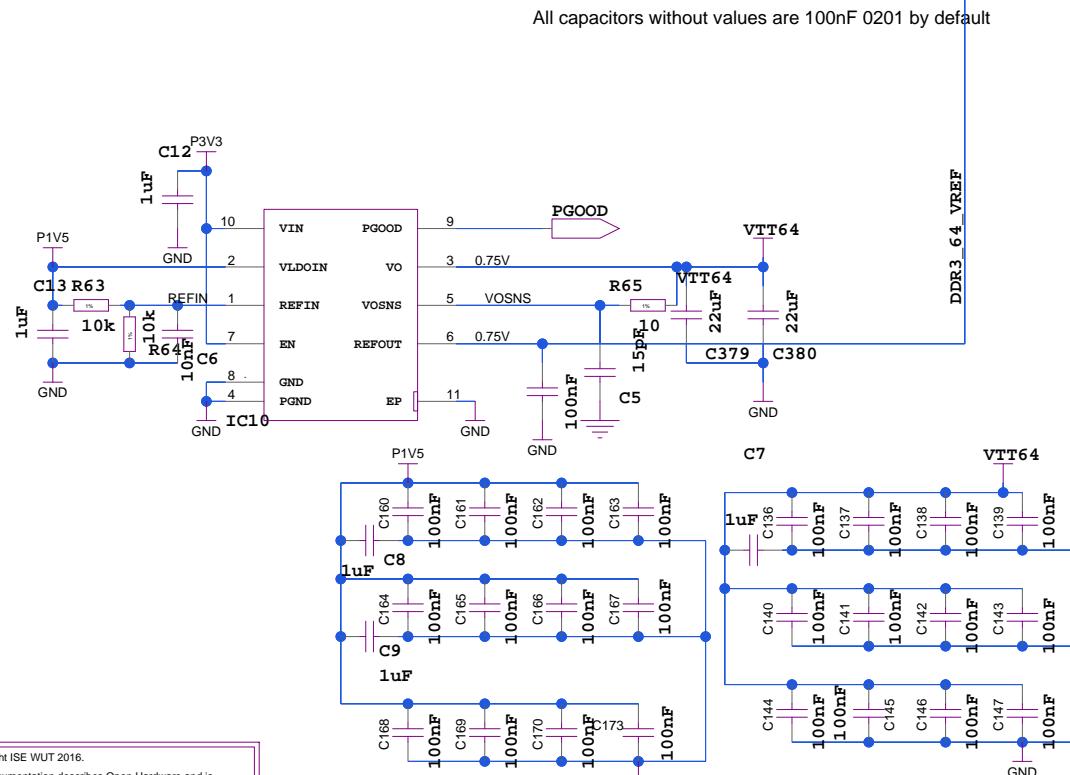
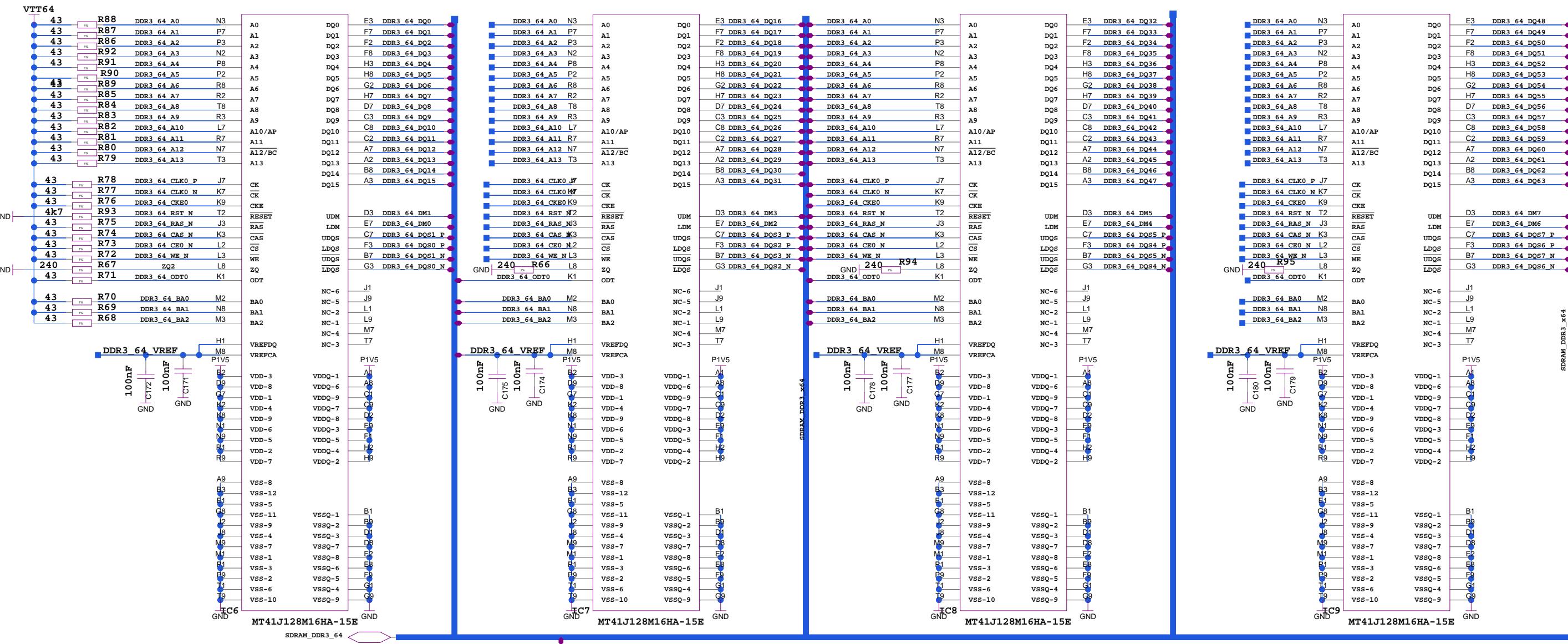


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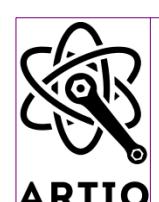
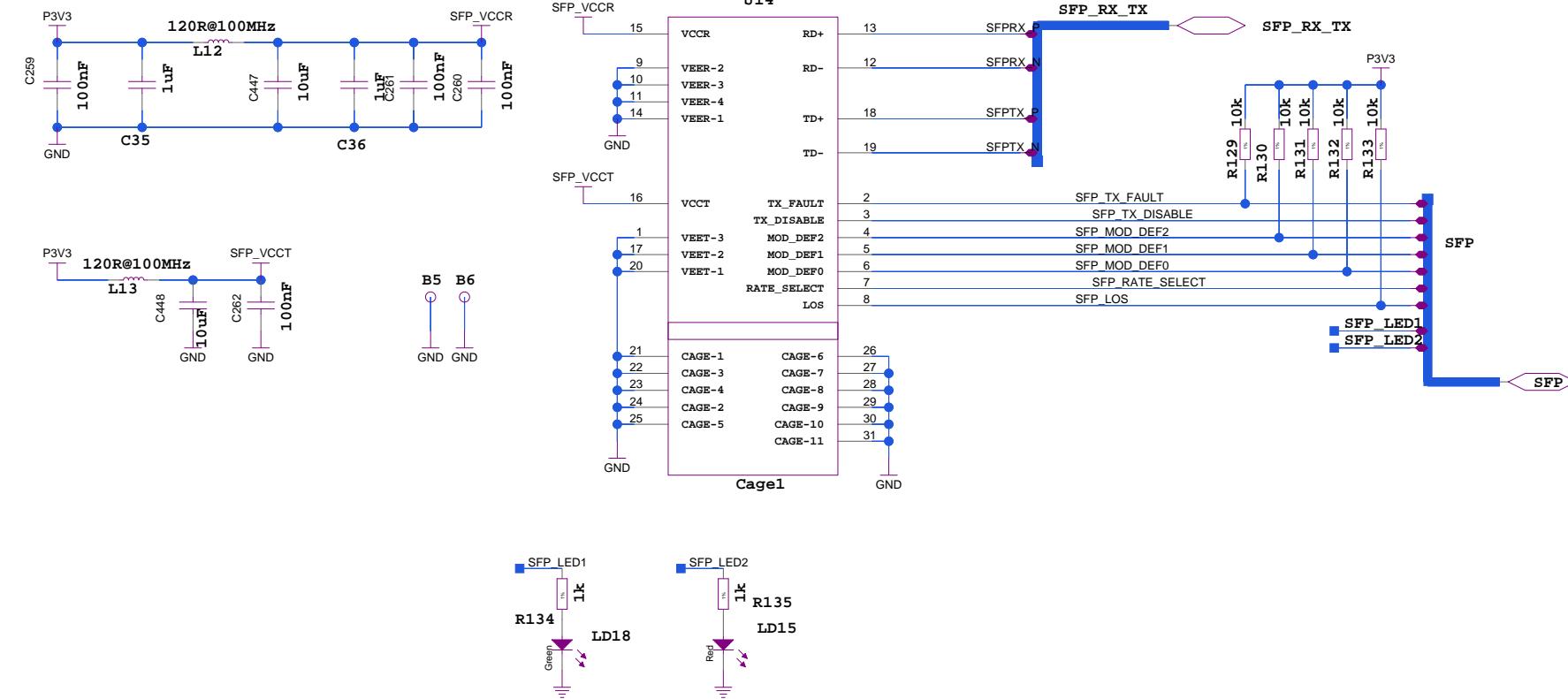
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SDRAM DDR3 4x16

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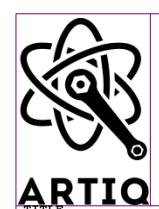
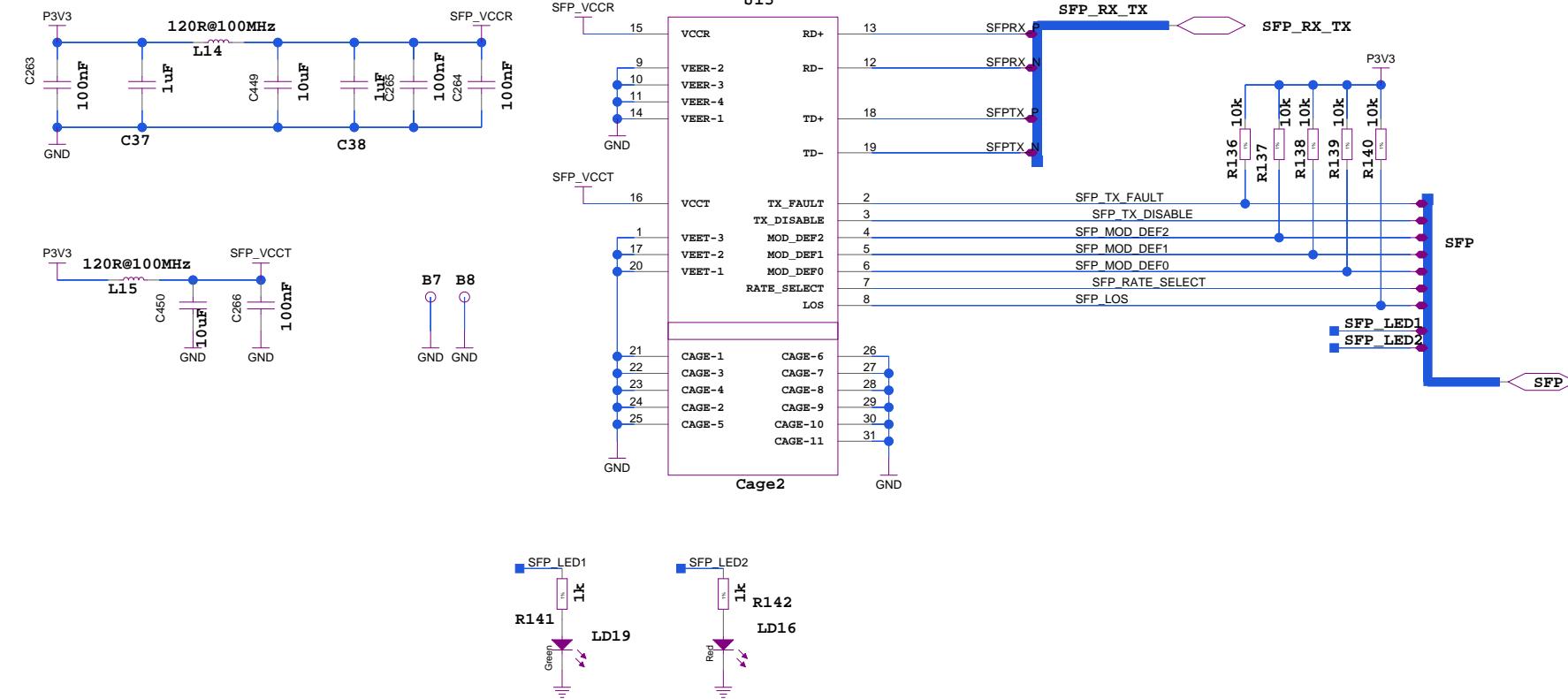
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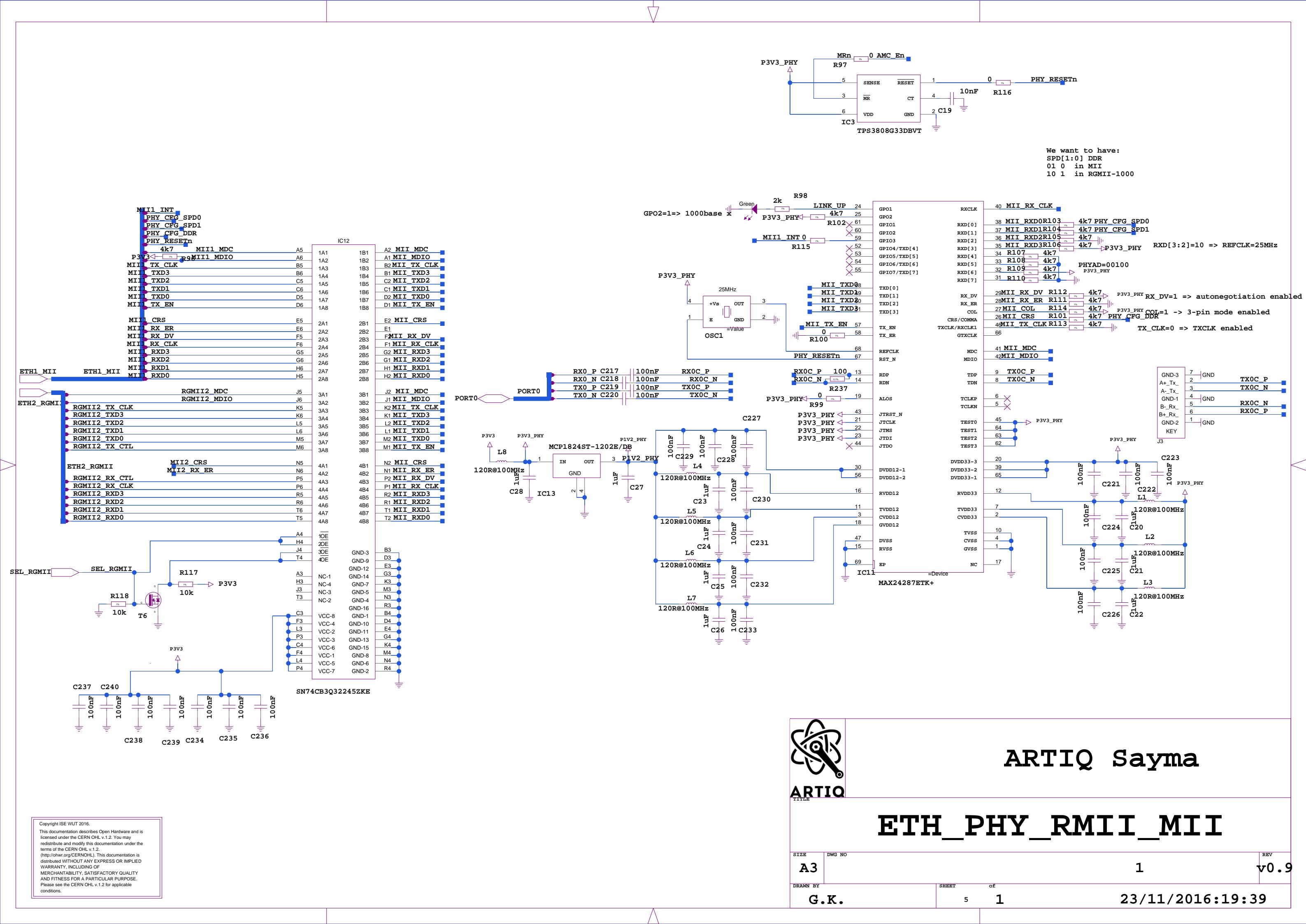
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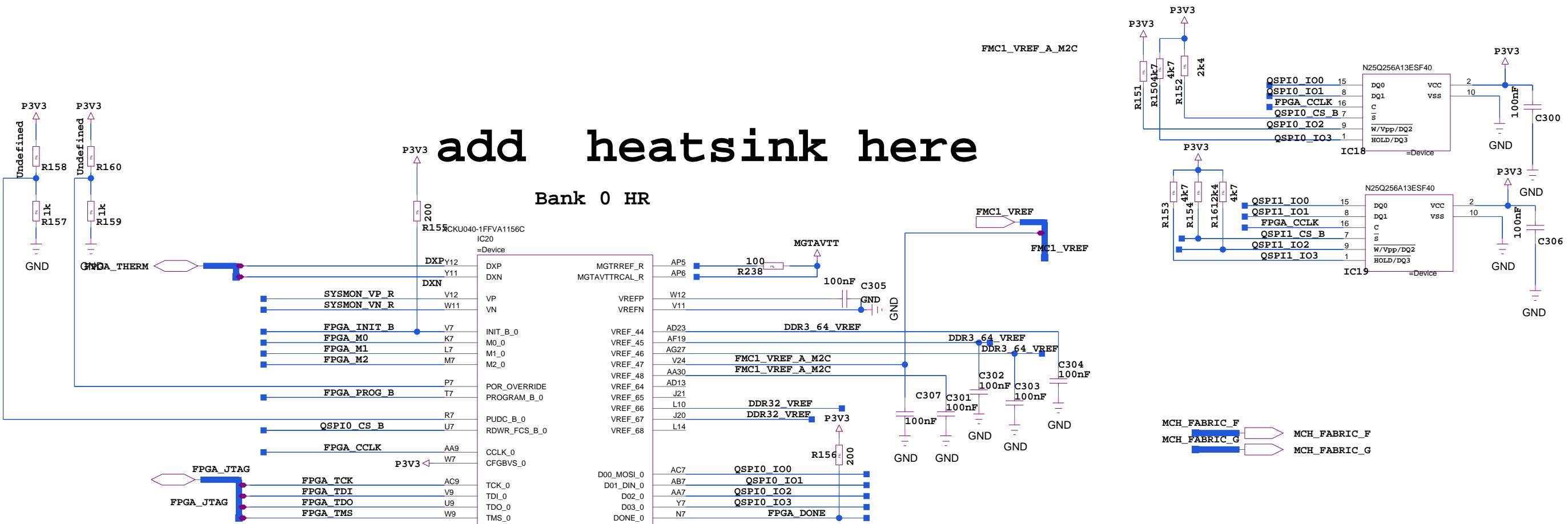
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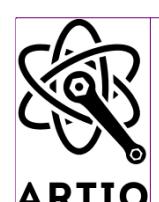
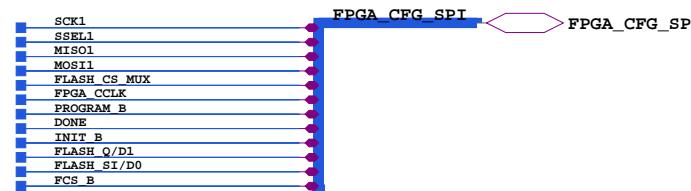
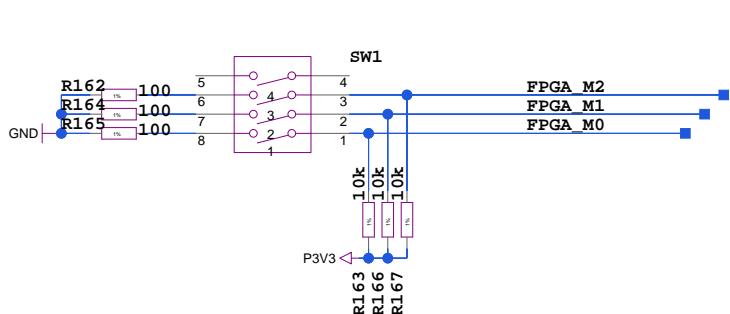
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Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via



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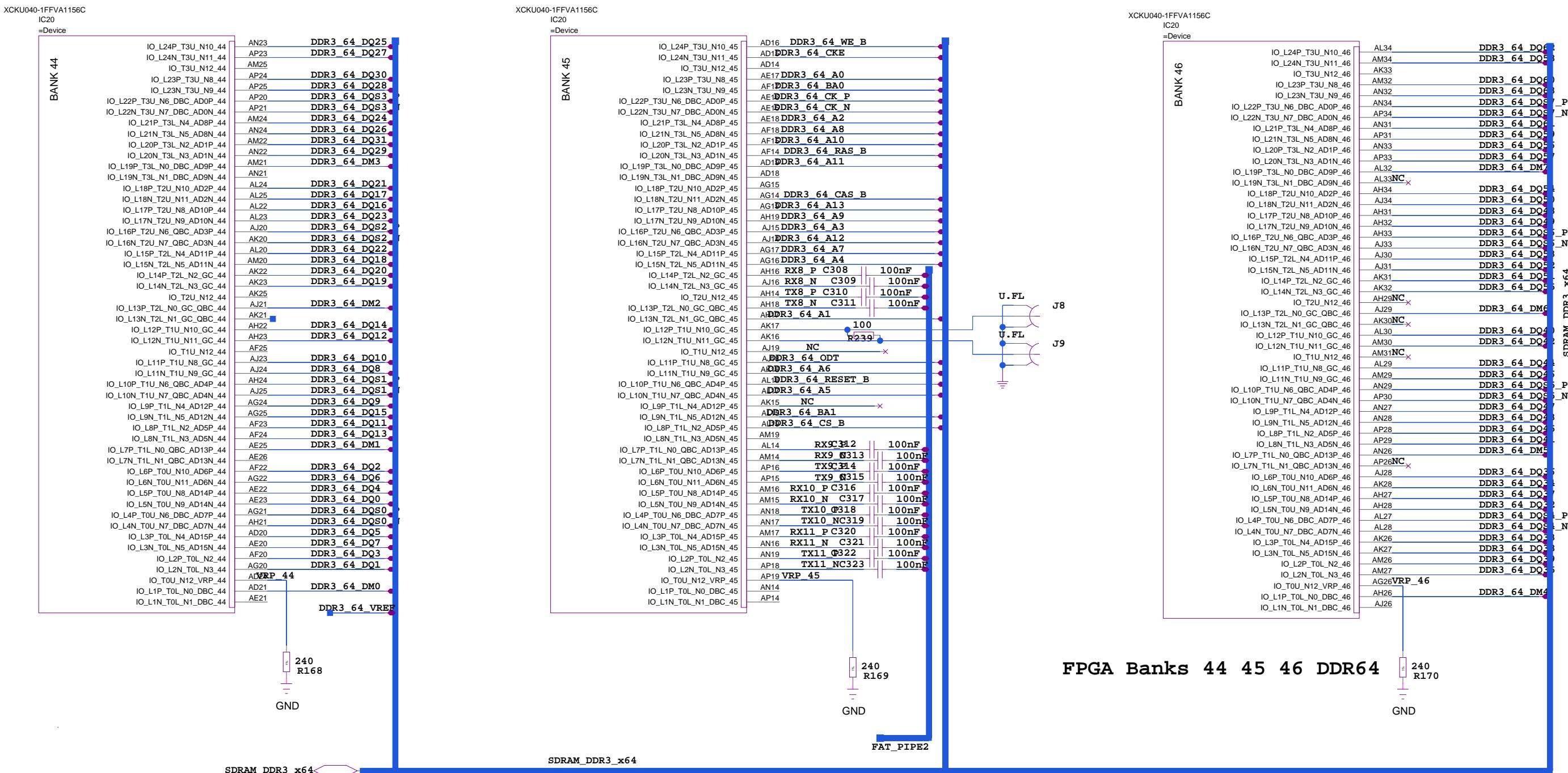
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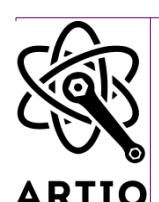
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Bank 46 HP



FPGA Banks 44 45 46 DDR64

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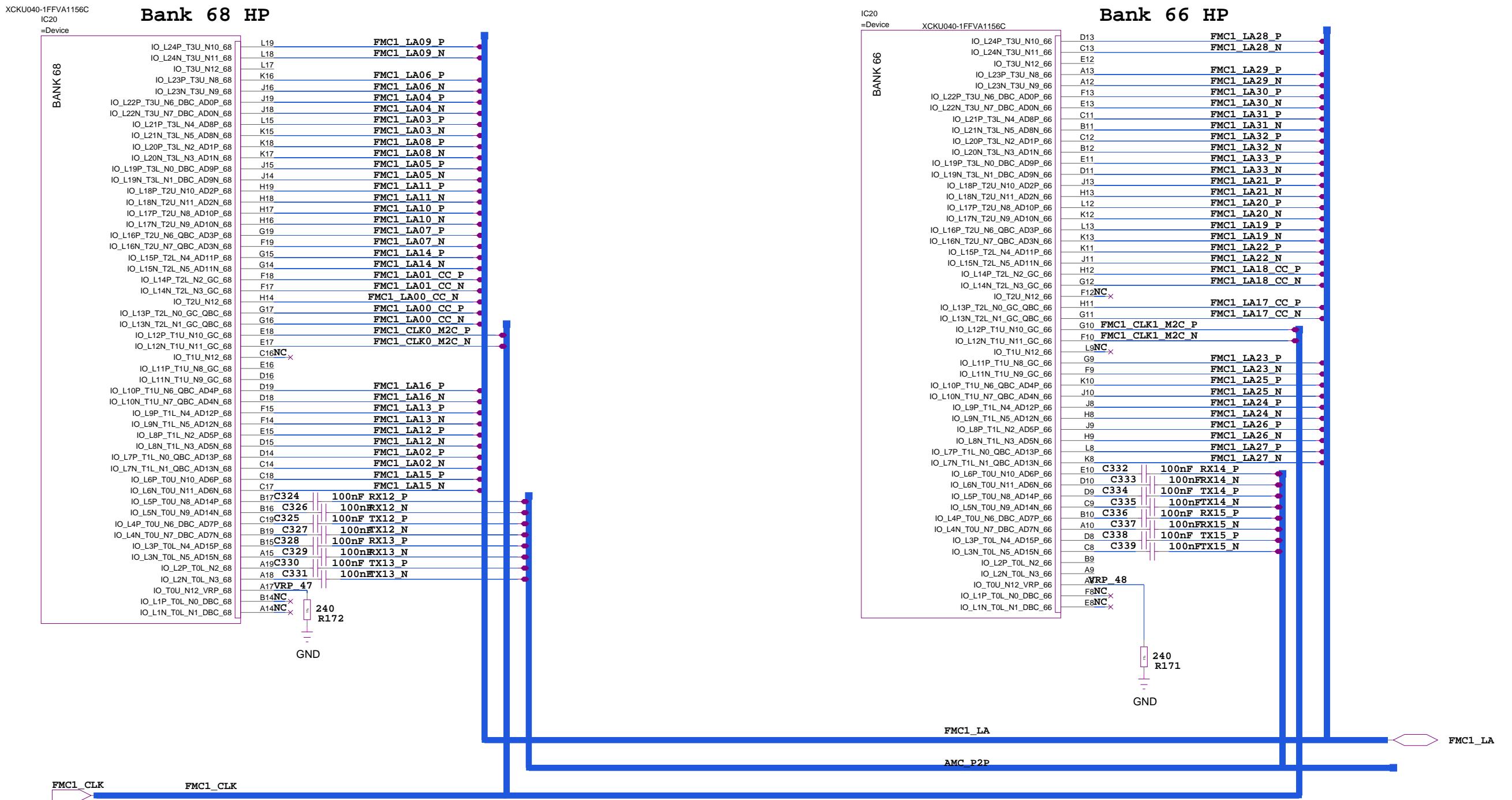
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FPGA Banks 44 45 46 DDR64

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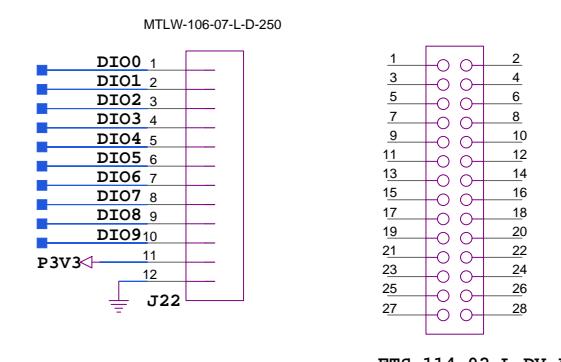
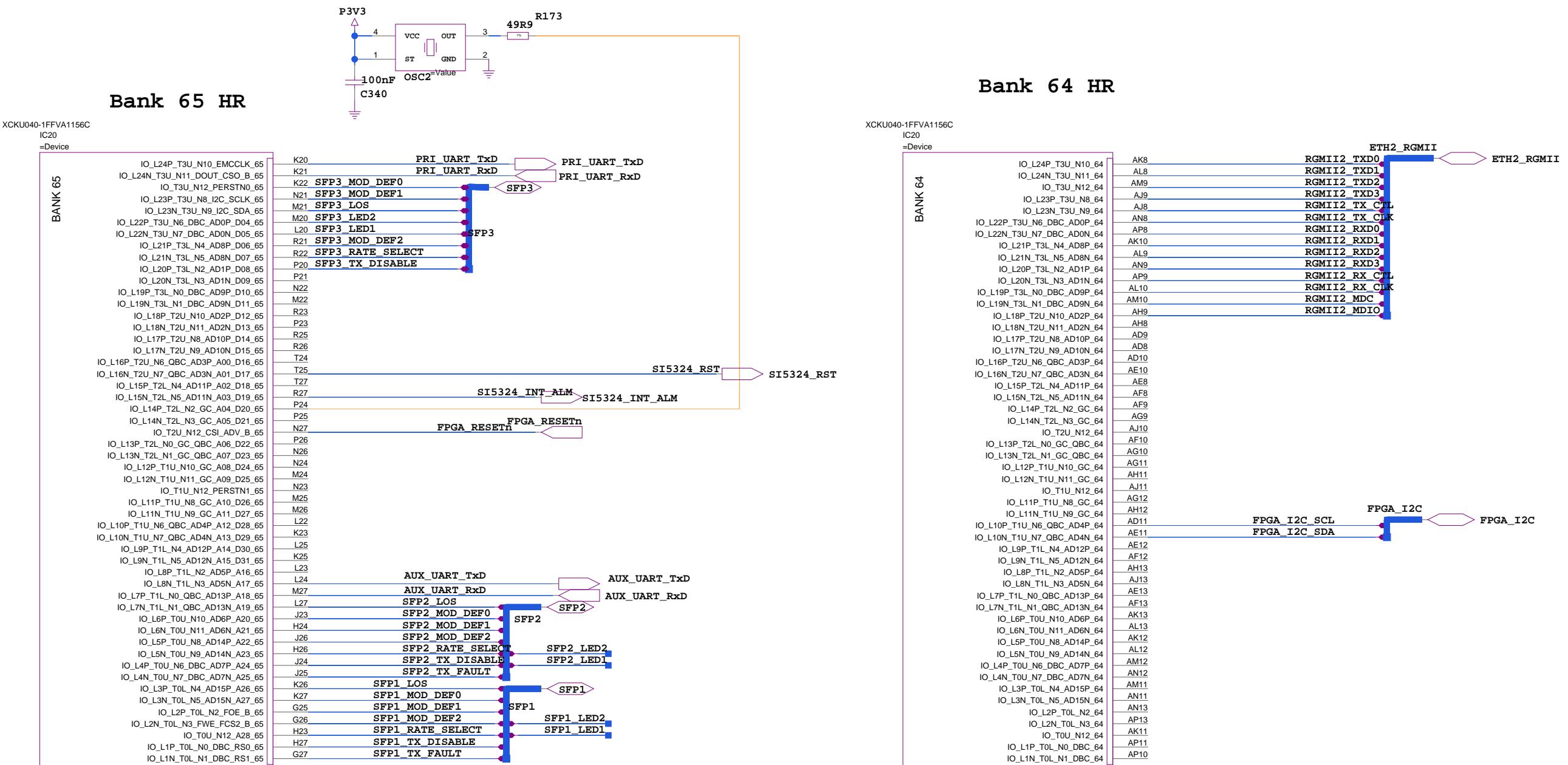
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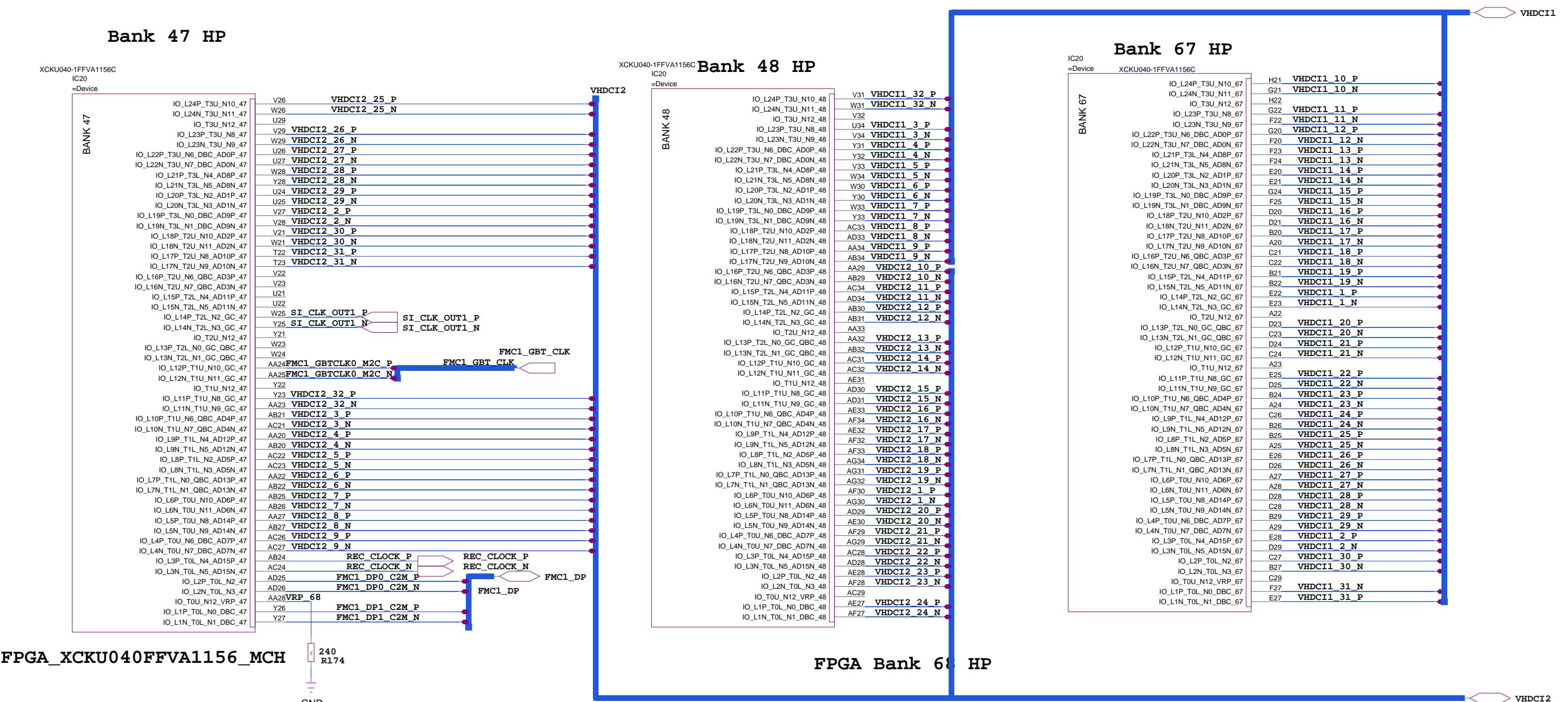
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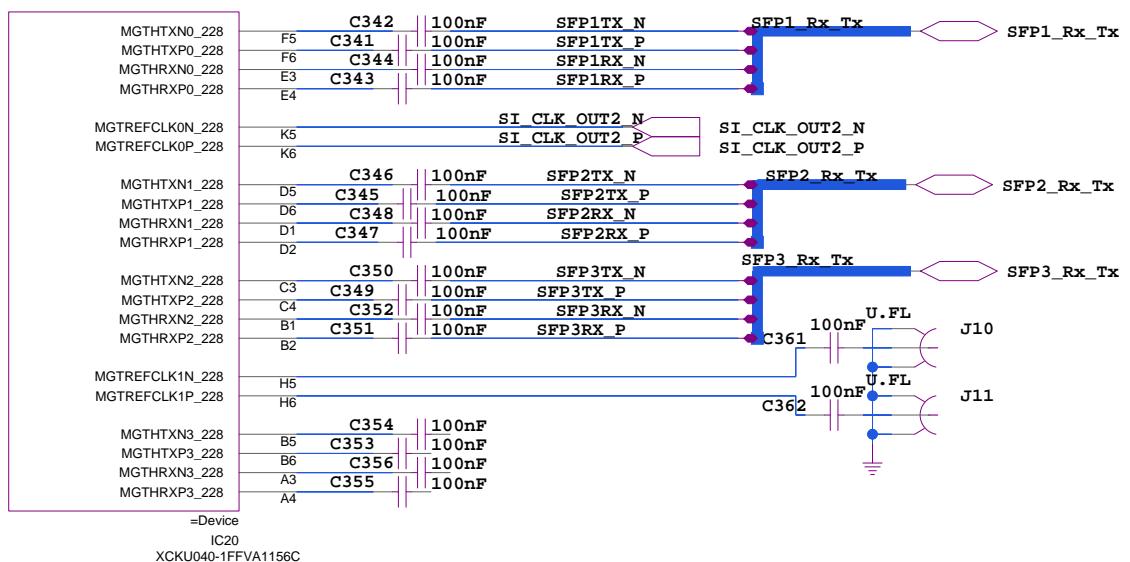
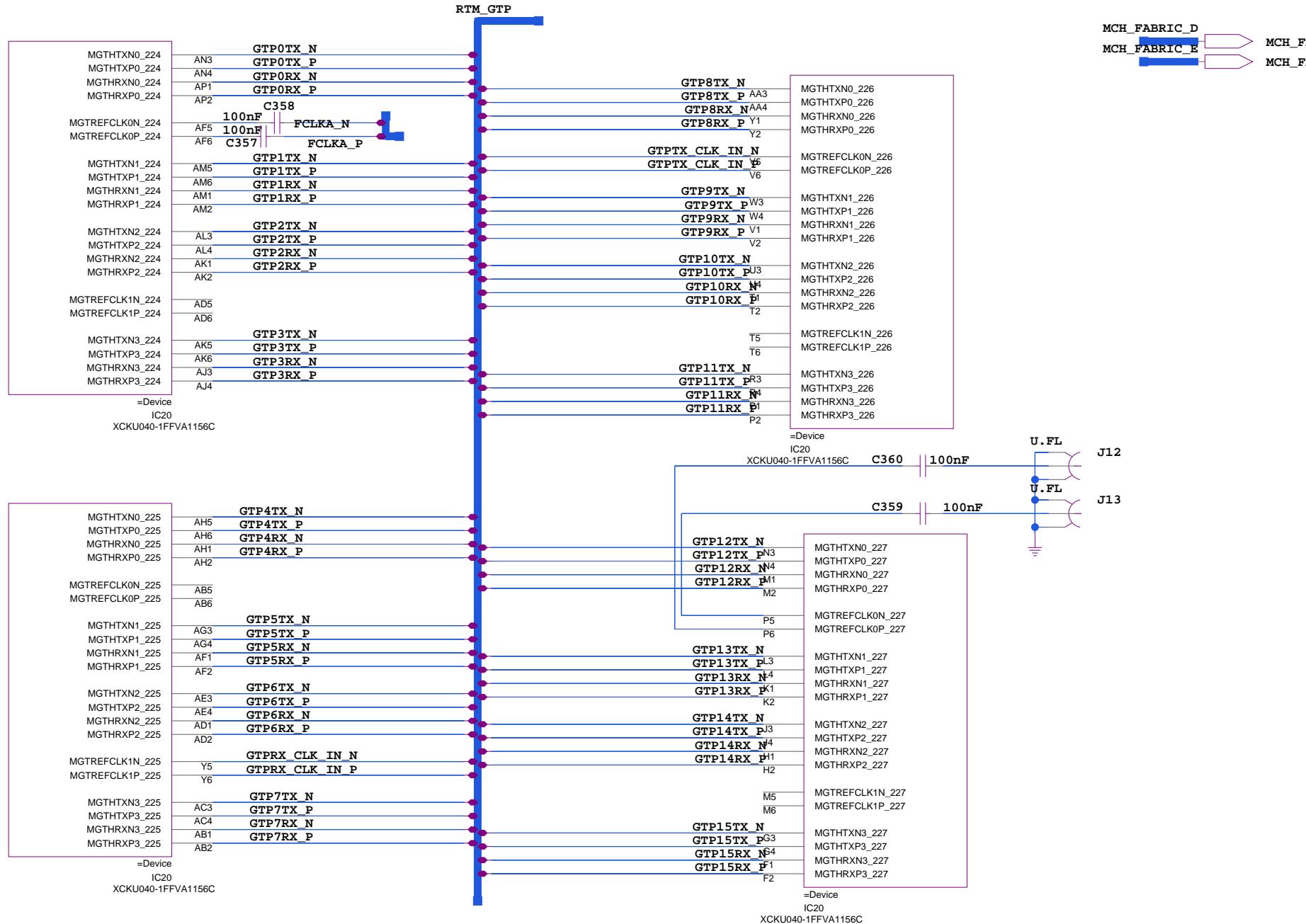
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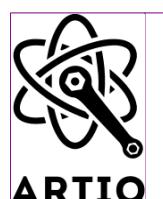
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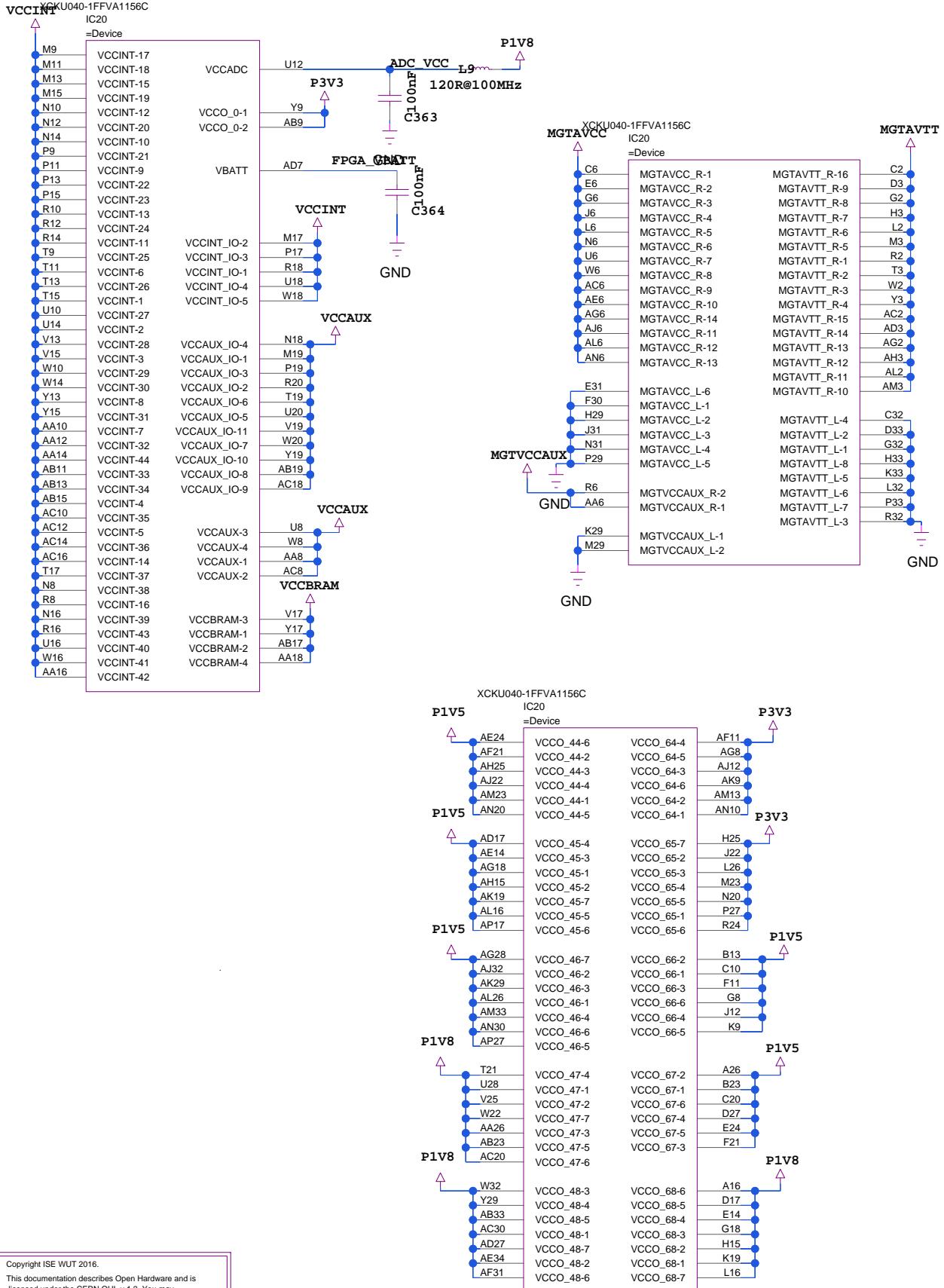
FPGA XCKU040FFVA1156



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FPGA Banks 224 225 226 227 228

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FPGA Power

FPGA_XCKU040FFVA1156

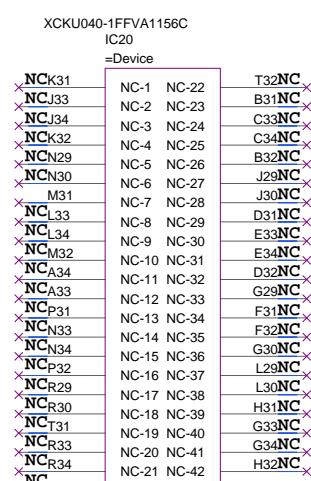
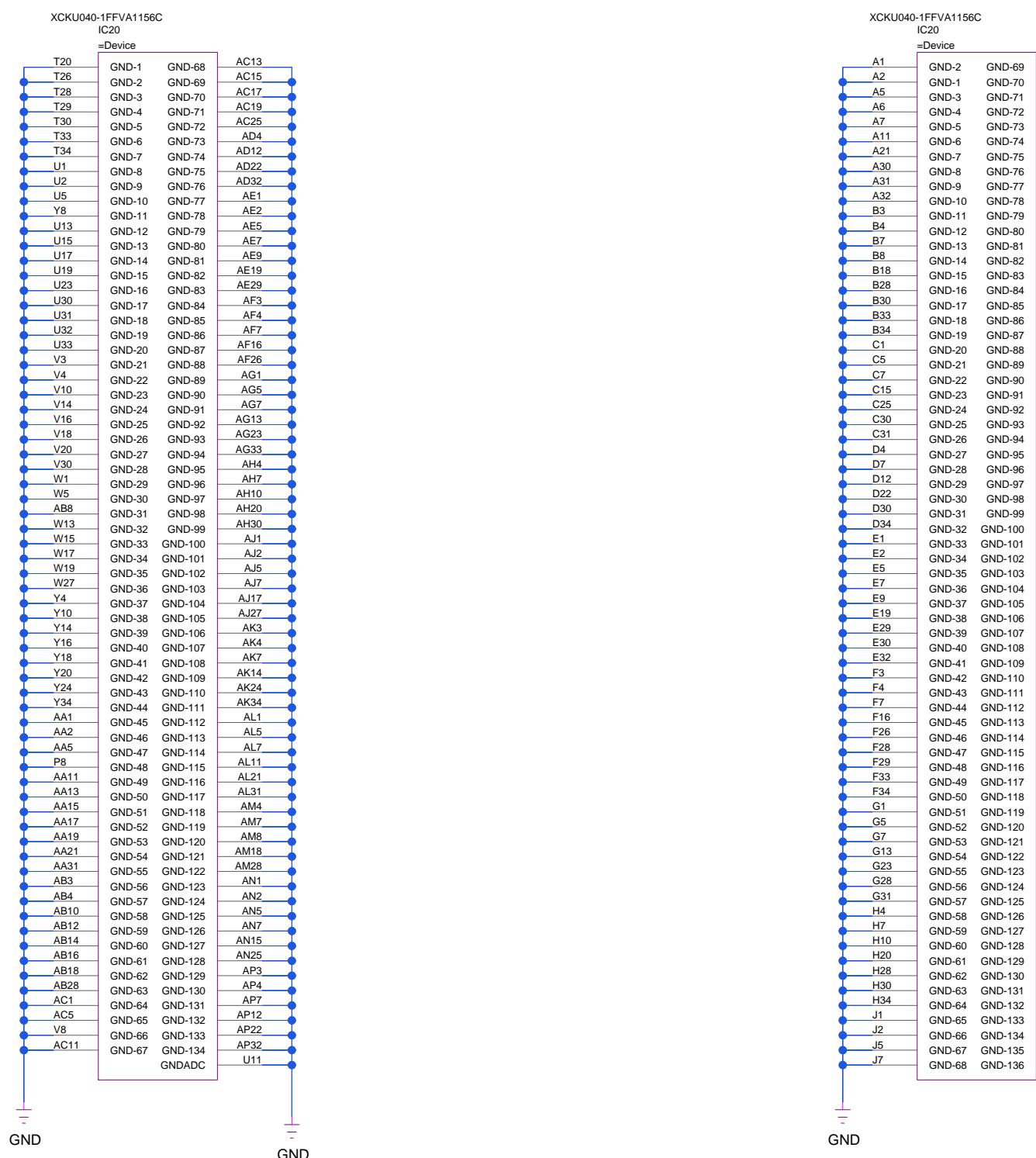


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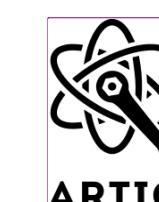
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FPGA GND NC

Figure 1. A schematic diagram of the experimental setup.

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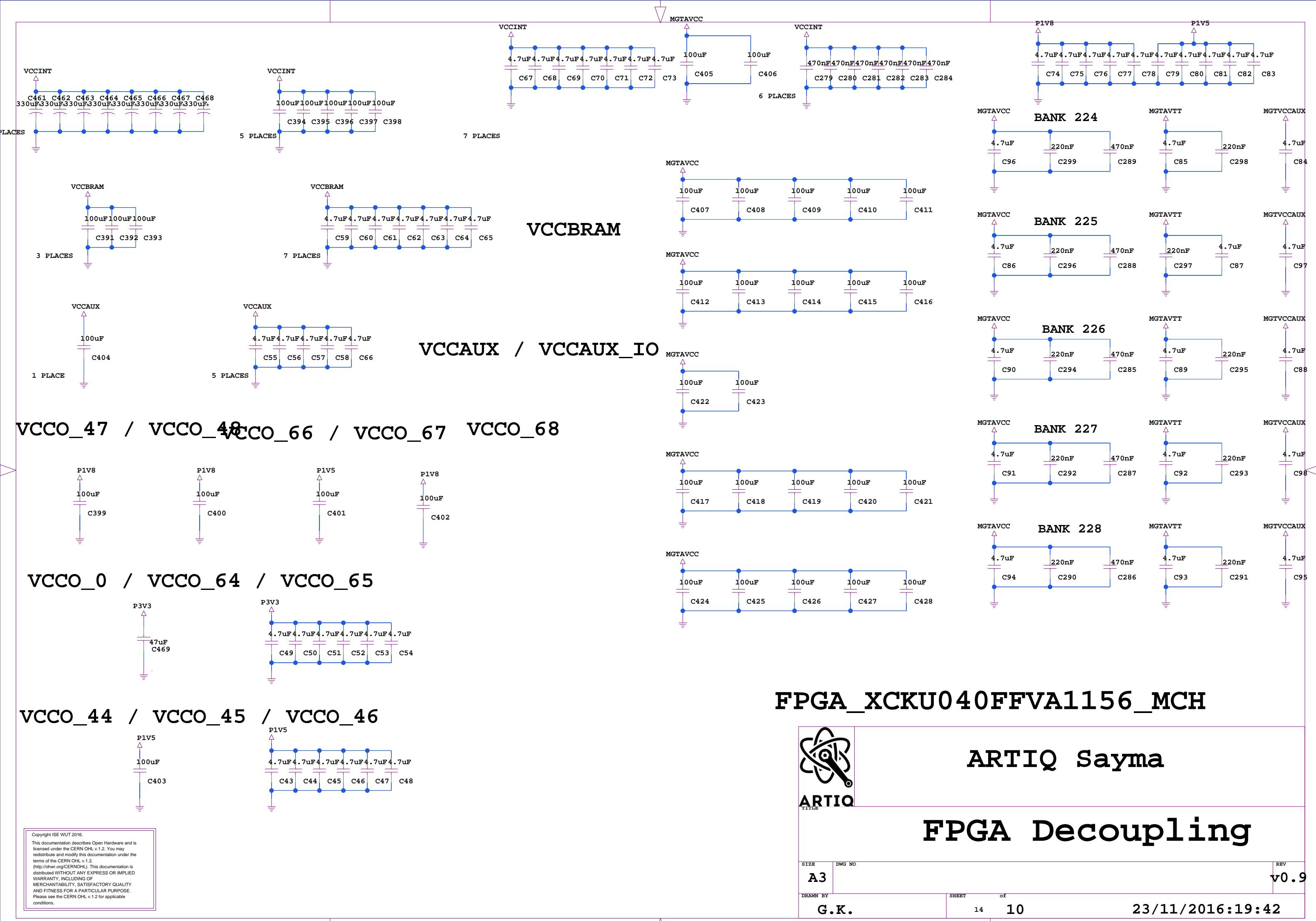
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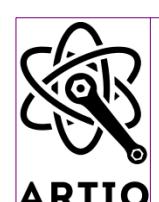
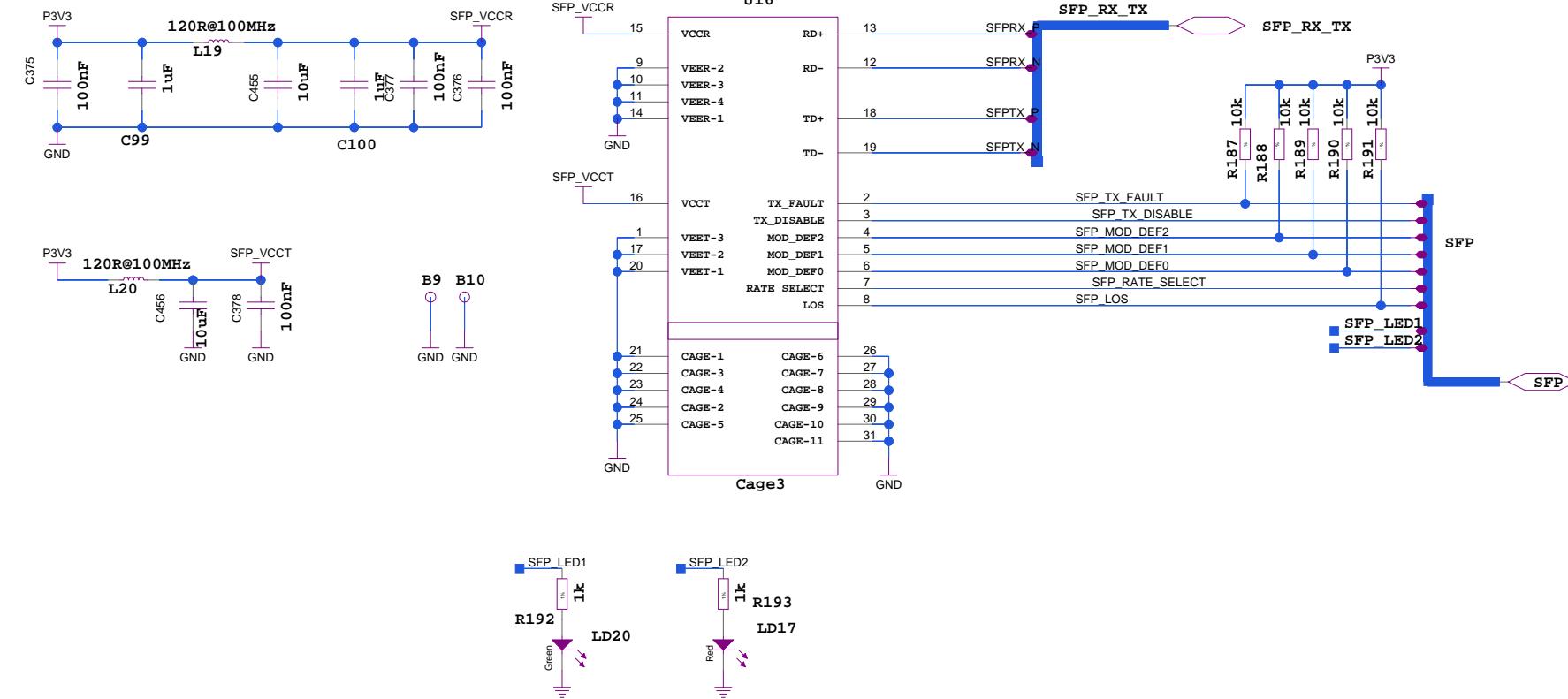
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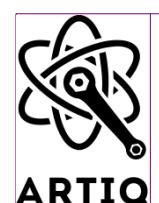
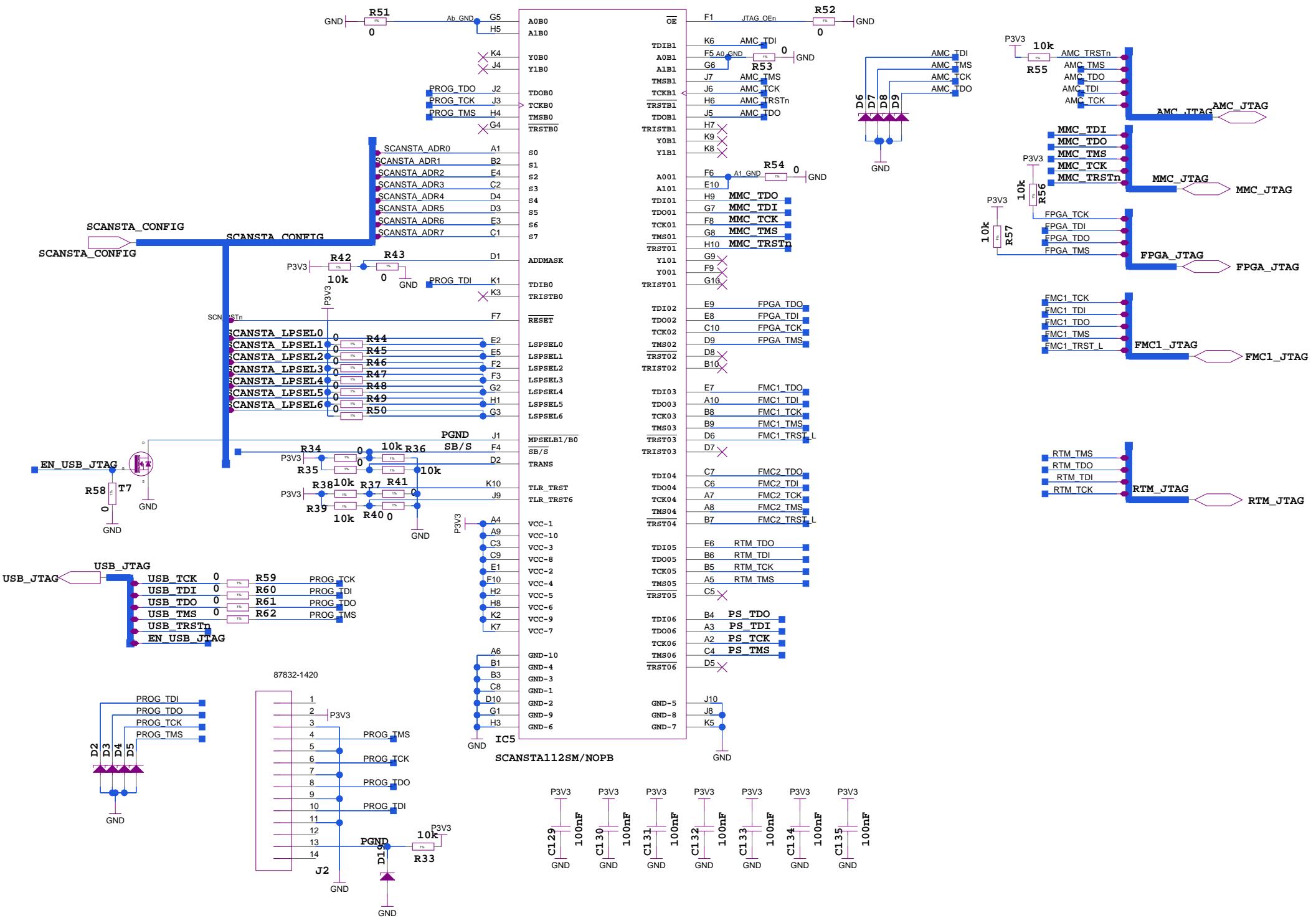
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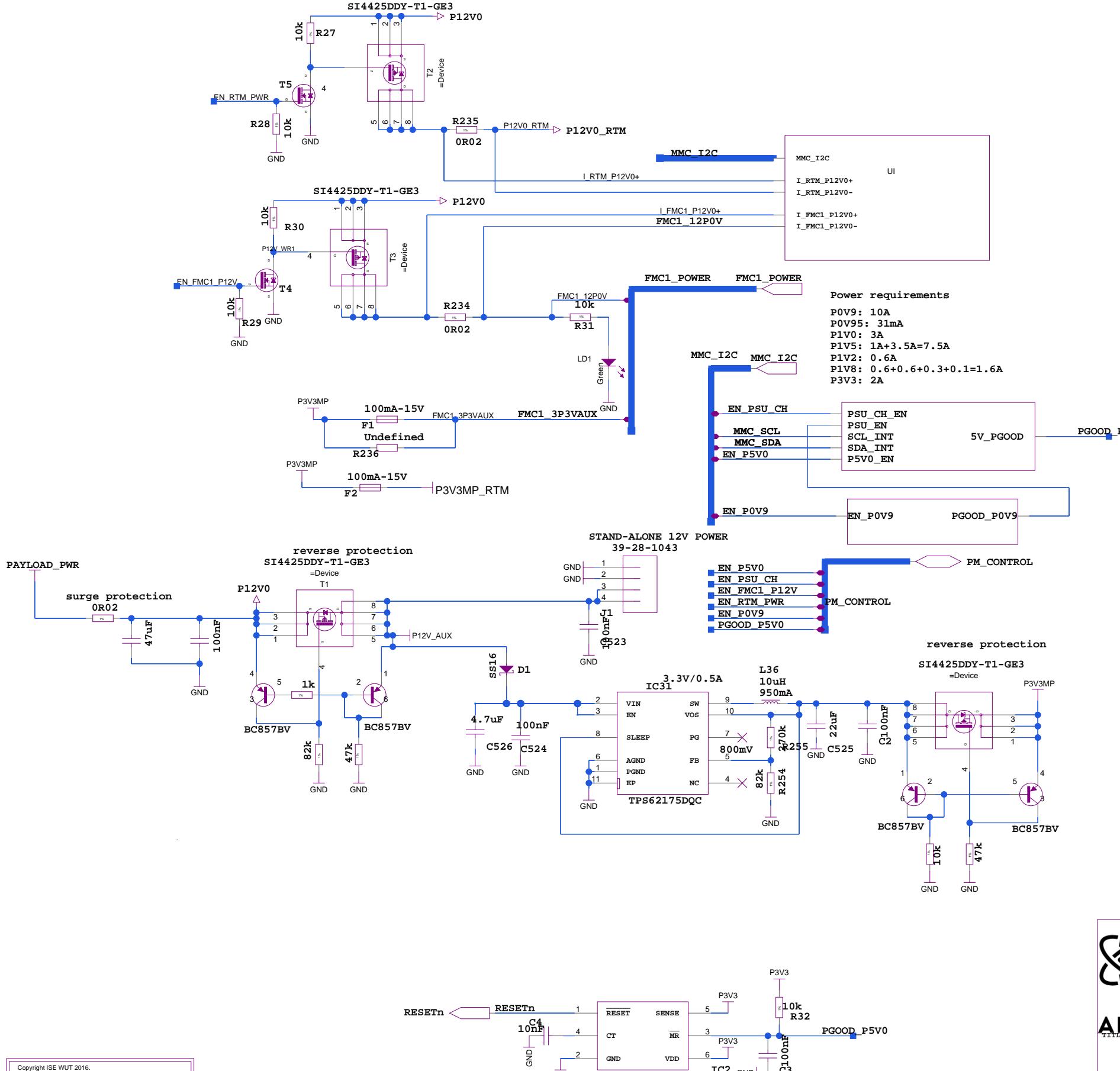
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JTAG_Configuration

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Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V _{CCINT}	Internal supply voltage	0.922	0.950	0.979	V
V _{CCINT}	For -1 (0.90V) devices: internal supply voltage	0.880	0.900	0.920	V
V _{CCINT}	For -3 (1.0V only) devices: internal supply voltage	0.970	1.000	1.030	V
V _{CCINT}	Internal supply voltage for the I/O banks	0.922	0.950	0.979	V
V _{CCINT}	For -1 (0.90V) devices: internal supply voltage for the I/O banks	0.880	0.900	0.920	V
V _{CCRAM}	Block RAM supply voltage	0.970	1.000	1.030	V
V _{CCRAM}	For -3 (1.0V only) devices: block RAM supply voltage	0.970	1.000	1.030	V
V _{CCAUX}	Auxiliary supply voltage	1.746	1.800	1.854	V
V _{CCO}	Supply voltage for HP I/O banks	1.140	-	3.400	V
V _{CCO}	Supply voltage for HP I/O banks	0.950	-	1.890	V
V _{CCO}	Auxiliary I/O supply voltage	1.746	1.800	1.854	V
V _{IN}	I/O input voltage	-0.200	-	V _{CCO} + 0.200	V
V _{IN}	I/O input voltage when V _{CCO} = 3.3V for V _{CCF} and differential I/O standards except TMDS, 33 ¹⁰	-	0.400	2.625	V
I _H	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	-	-	10.000	mA
V _{BATT}	Battery voltage	1.000	-	1.890	V
GTH and GTY Transceivers					
V _{MGTAVCC}	Analog supply voltage for the GTH and GTY transceivers ¹⁰	0.970	1.000	1.030	V
V _{MGTAVTT}	Analog supply voltage for the GTH and GTY transmitter and receiver termination circuits	1.170	1.200	1.230	V
V _{MGTVAUX}	Auxiliary analog QPLL voltage supply for the transceivers	1.750	1.800	1.850	V
Temperature					
V _{CCMON}	Analog supply voltage for the resistor calibration circuit of the GTH and GTY transceiver columns	1.170	1.200	1.230	V
V _{CCMON}	SYSMON supply relative to GNDADC	1.746	1.800	1.854	V
V _{REFP}	Externally supplied reference voltage	1.200	1.250	1.300	V
T _J	junction temperature operating range for commercial (C)	0	-	85	°C
T _J	junction temperature operating range for extended (E) temperature devices	0	-	100	°C
T _J	junction temperature operating range for industrial (I)	-40	-	100	°C

Power-On/Off Power Supply Sequencing

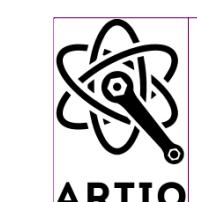
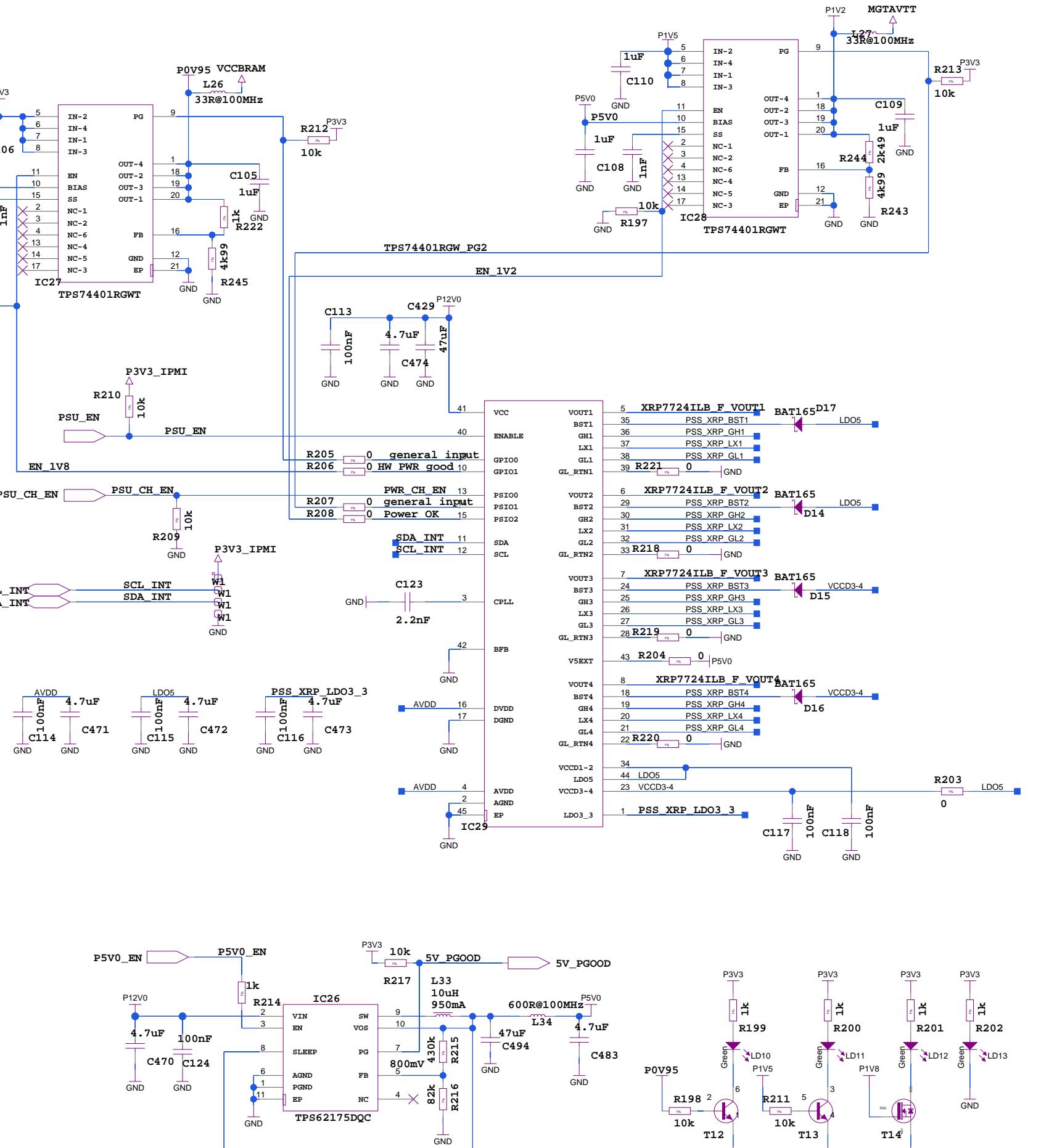
The recommended power on sequence is V_{CCINT}/V_{CCINT}_IO/V_{CCRAM}/V_{CCAUX}/V_{CCAO} to achieve minimum current draw and ensure that the I/Os are 3-state at power-on. The recommended power down sequence is V_{CCINT}/V_{CCINT}_IO/V_{CCRAM}/V_{CCAUX}/V_{CCAO}. If the I/Os are 3-state at power-down, the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT}_IO must be connected to V_{CCINT}. If V_{CCAU}/V_{CCAUX}_IO and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAU} and V_{CCAUX} must be connected together. When the current minimums are met, the device powers up after the V_{CCINT}/V_{CCINT}_IO/V_{CCRAM}/V_{CCAUX}/V_{CCAO} supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied.

V_{CCADC} and V_{CCF} can be powered at any time and have no power-up sequencing recommendations. The recommended power on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}/V_{MGTAVCC}/V_{MGTAVTT} OR V_{MGTAVCC}/V_{CCINT}/V_{MGTAVTT}. There is no recommended sequencing for V_{MGTAVCC}, V_{MGTAVTT} and V_{CCINT}. The recommended power off sequence is the reverse of the power on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from V_{MGTAVTT} can be higher than specifications during power-up and power-down.

Power Supply			
Source	Voltage	Total (A)	
V _{CCINT}	0,900	9,165	
V _{CCINT} _IO	0,900	0,620	
V _{CCRAM}	0,950	0,031	
V _{CCAUX}	1,800	0,660	
V _{CCAUX} _IO	1,800	0,546	
V _{CCO} 3.3V	3,300	0,000	
V _{CCO} 2.5V	2,500		
V _{CCO} 1.8V	1,800	0,380	
V _{CCO} 1.5V	1,500	0,936	
V _{CCO} 1.35V	1,350		
V _{CCO} 1.2V	1,200		
V _{CCO} 1.0V	1,000		
MGT _V CAUX	1,800	0,081	
MGT _V CC	1,000	3,038	
MGT _V TT	1,200	0,592	
	-		
V _{CCADC}	1,800	0,014	

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POWER Management

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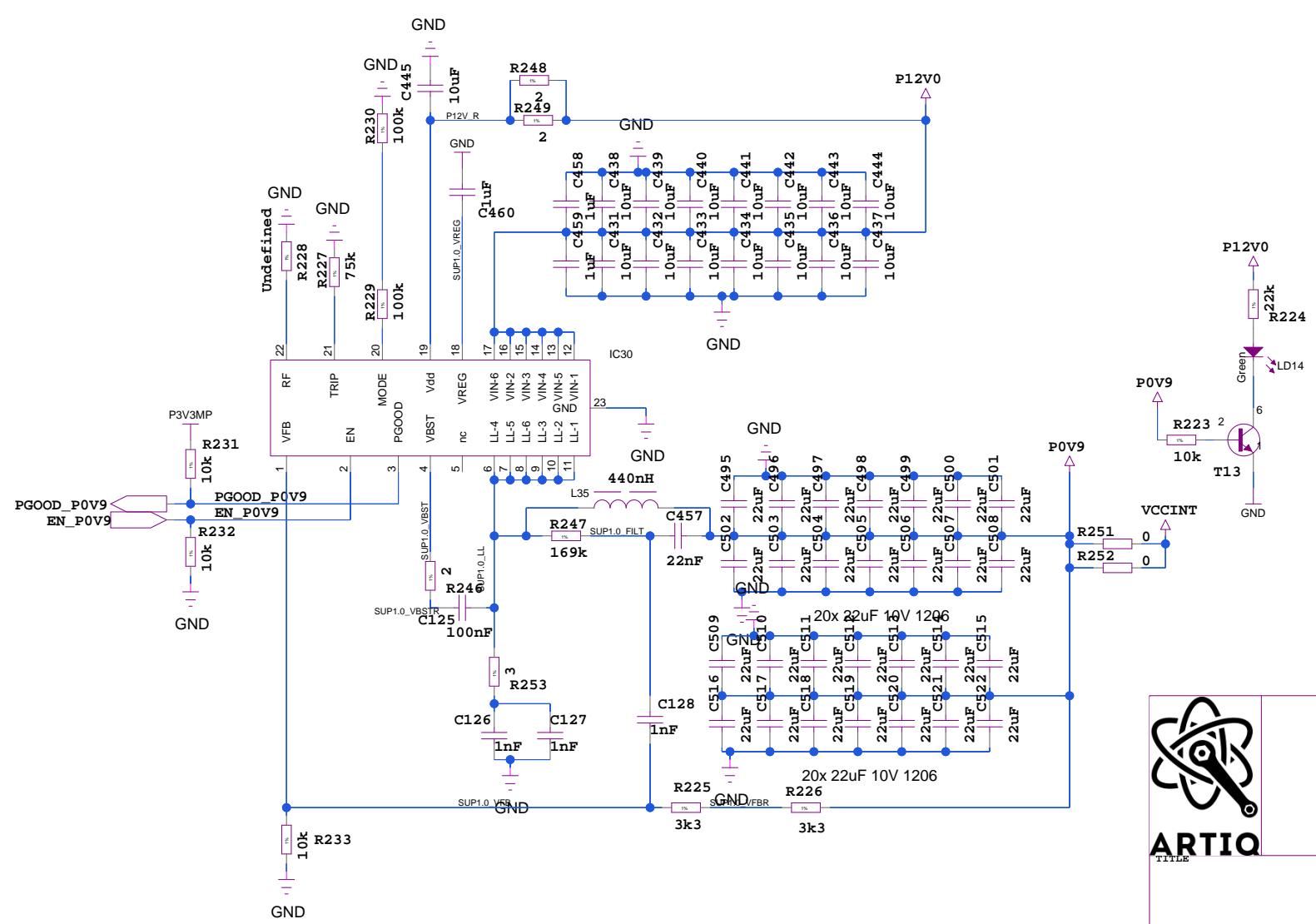


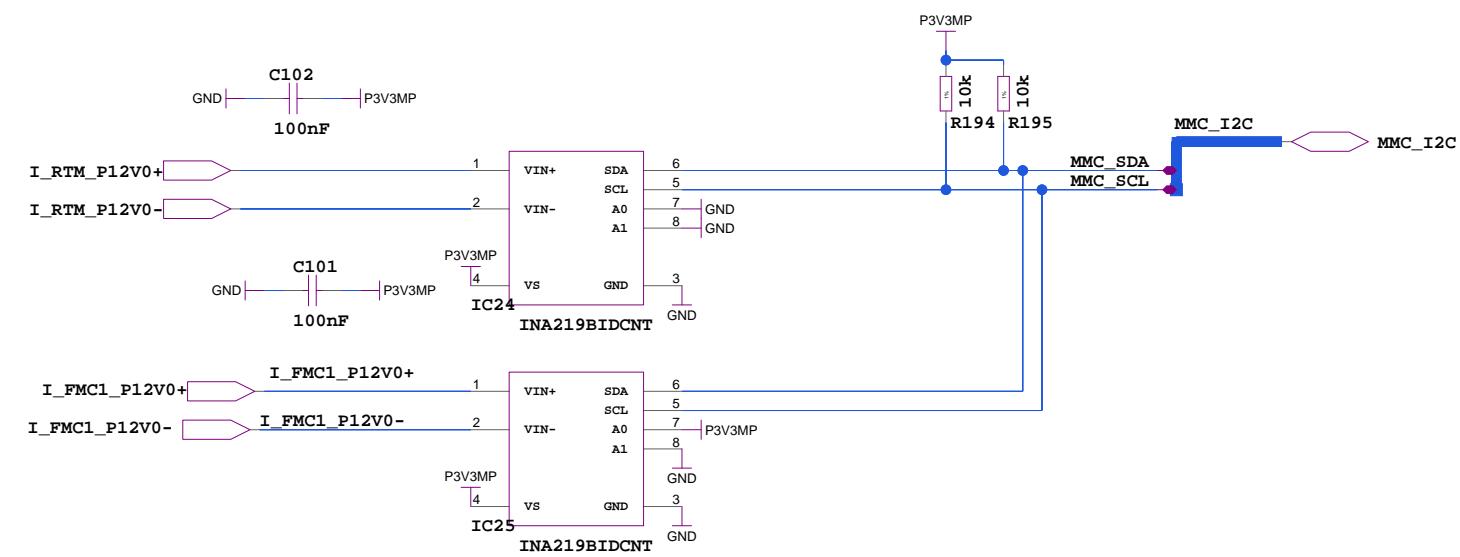
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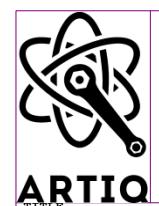
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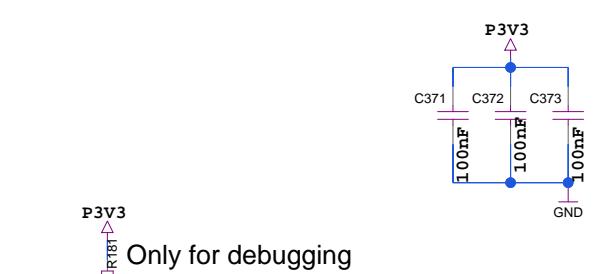
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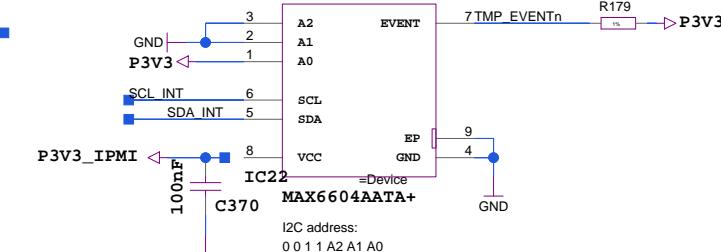
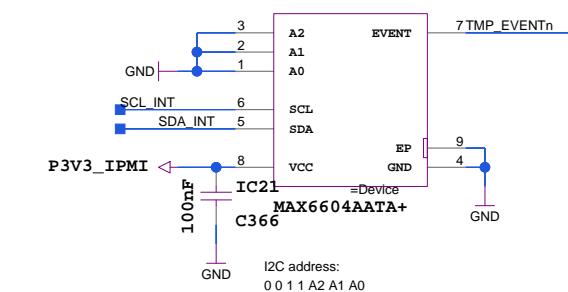
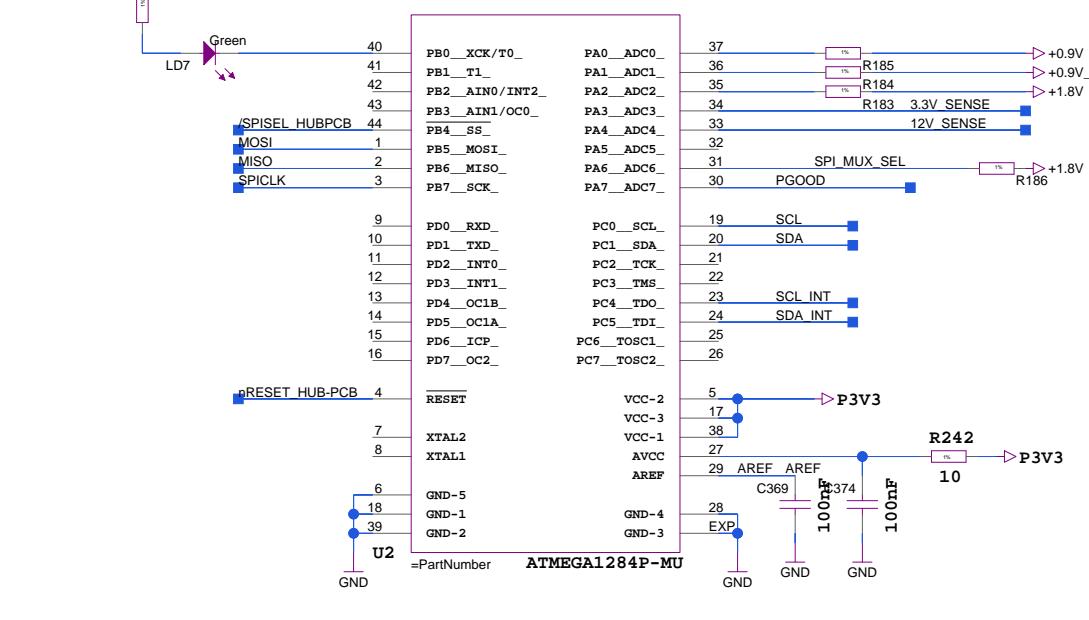
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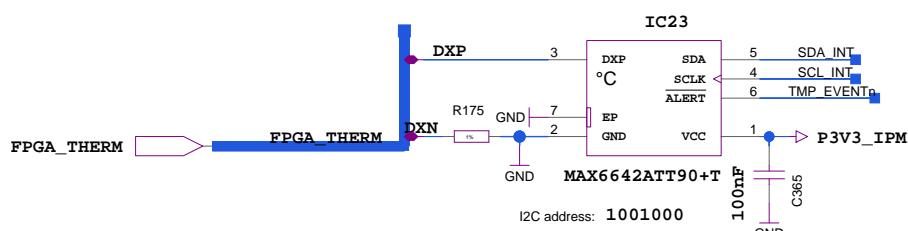
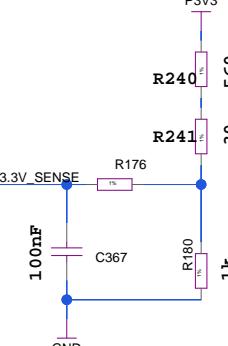
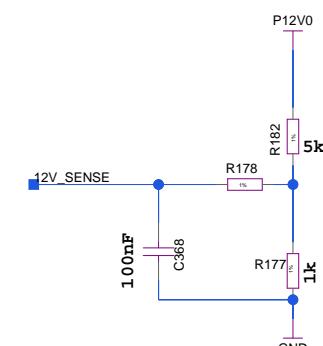
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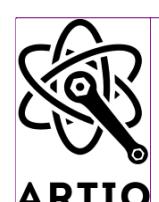
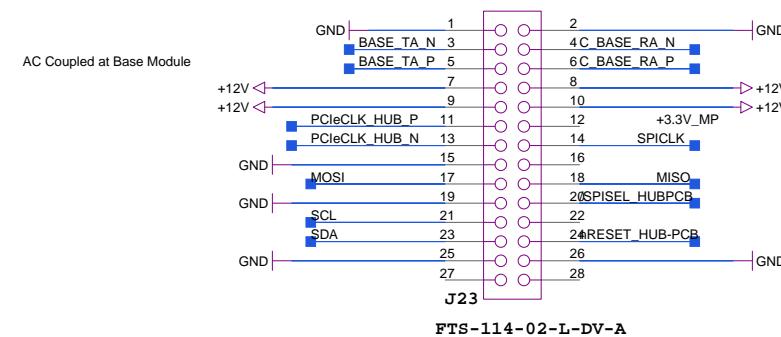
Voltage at MC pin has to be below 2.5V



MMC_MOTION_CONSOLE
PM_CONTROL

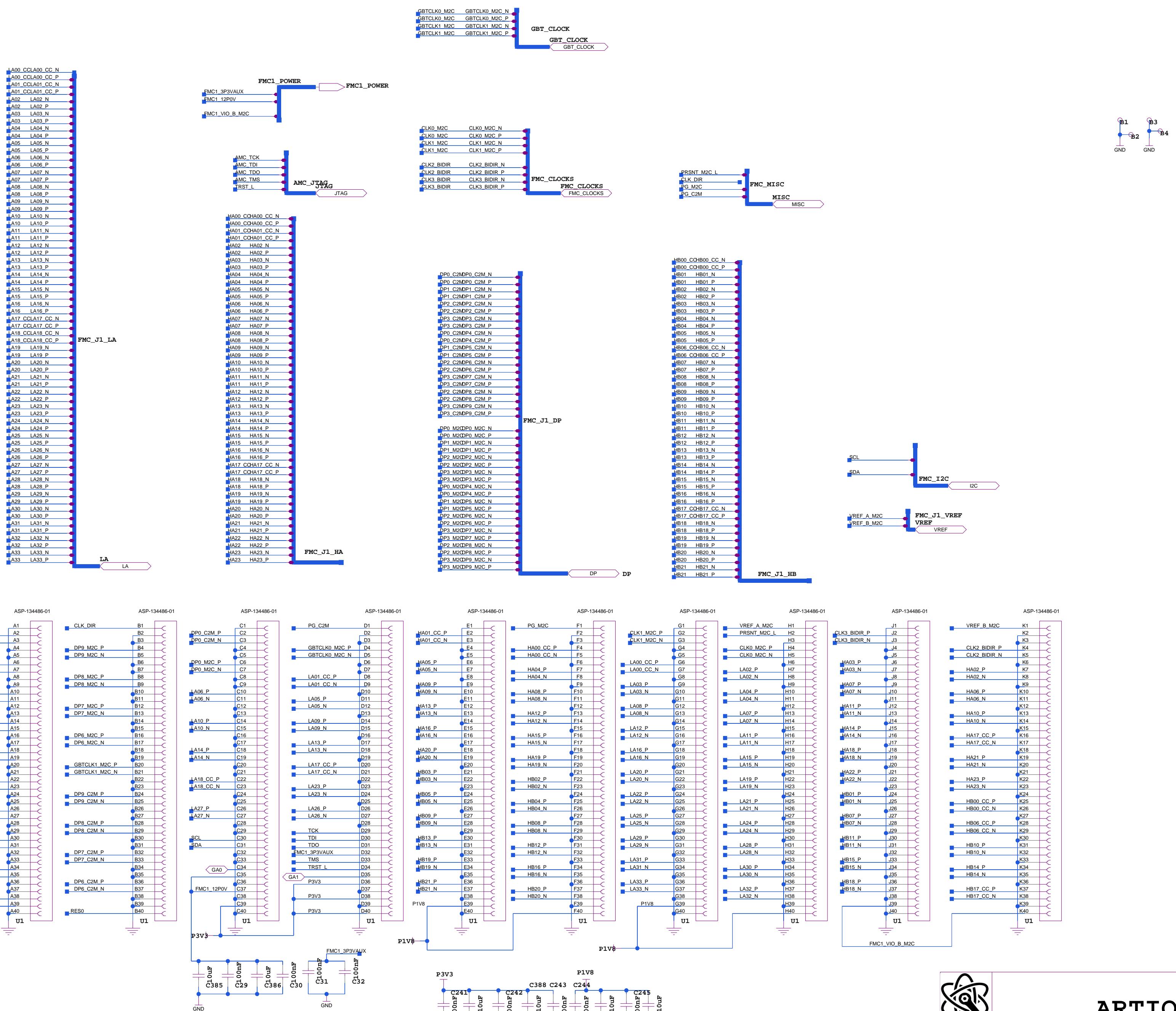


Connector to 1st or 2nd PCB



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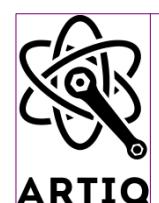
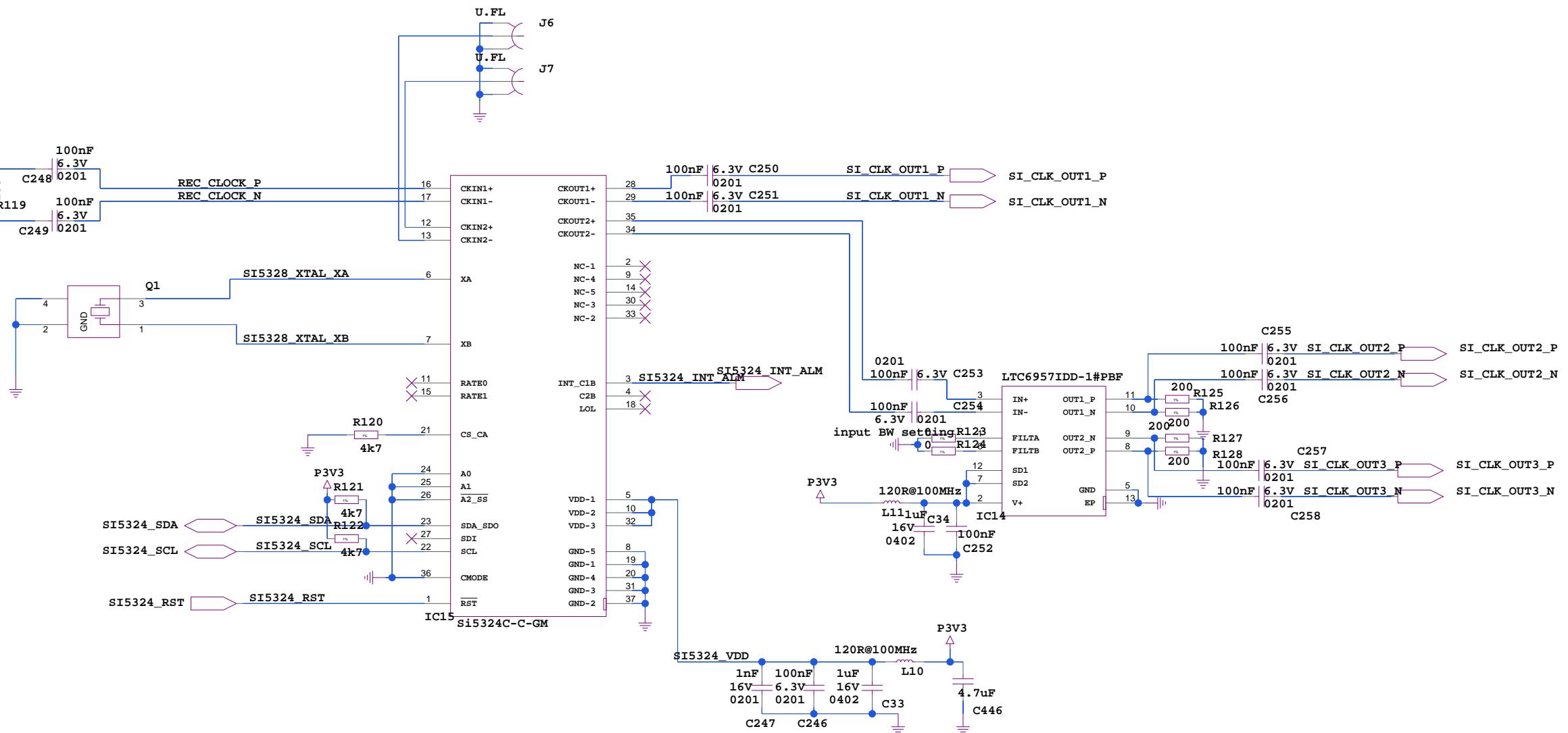
SIZE	DWG NO	REV
A3	CON_Tongue3_IPMI 1	v0.9
DRAWN BY	G.K.	
SHEET	21	27



ARTIQ Sayma

FMC_connector

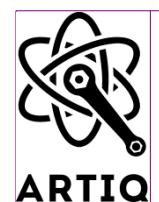
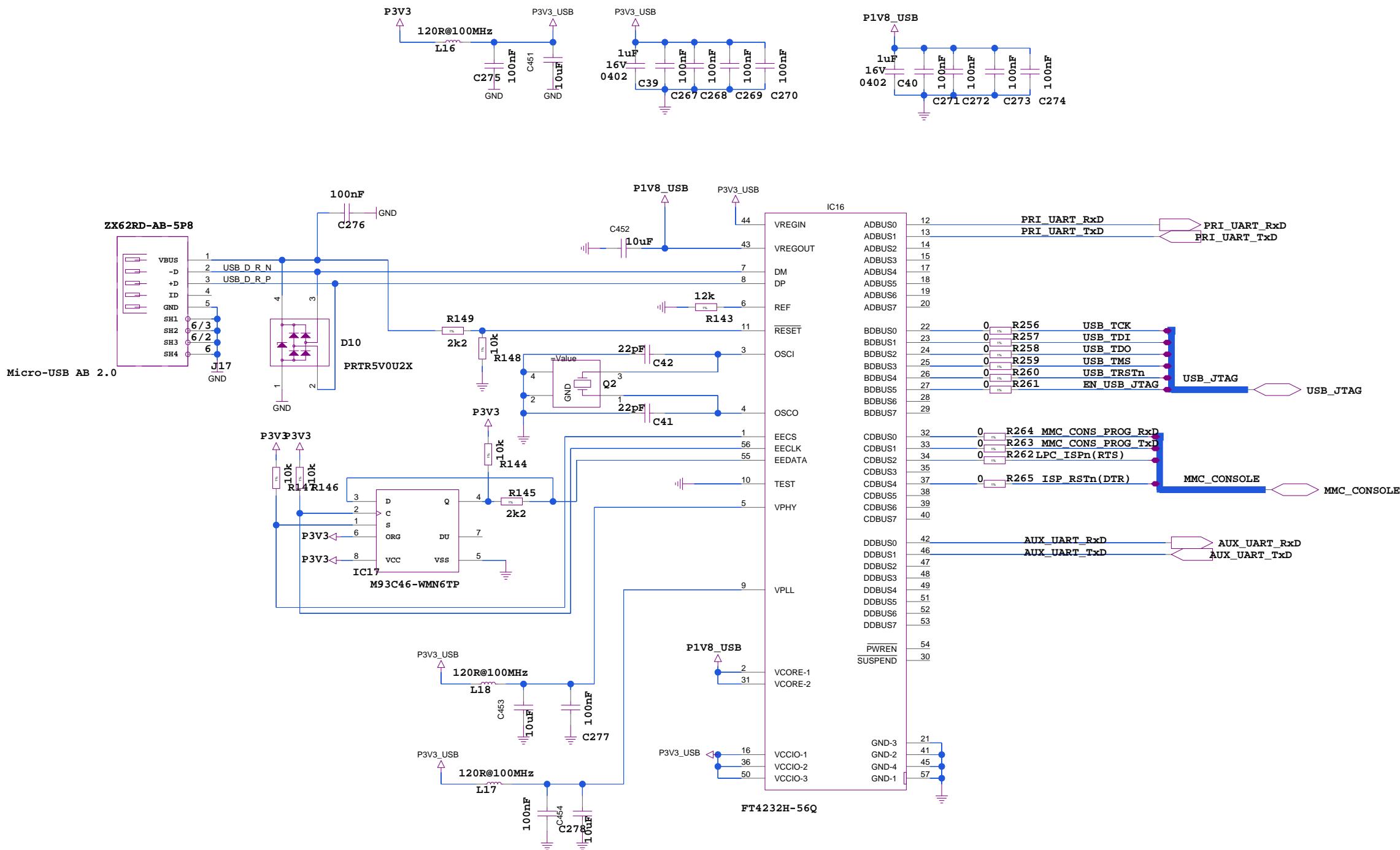
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SI5324_CLK_RECOVERY

SIZE	DWG NO	REV
A3		v0.9
DRAWN BY	SHEET of	
G.K.	24	1



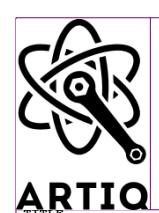
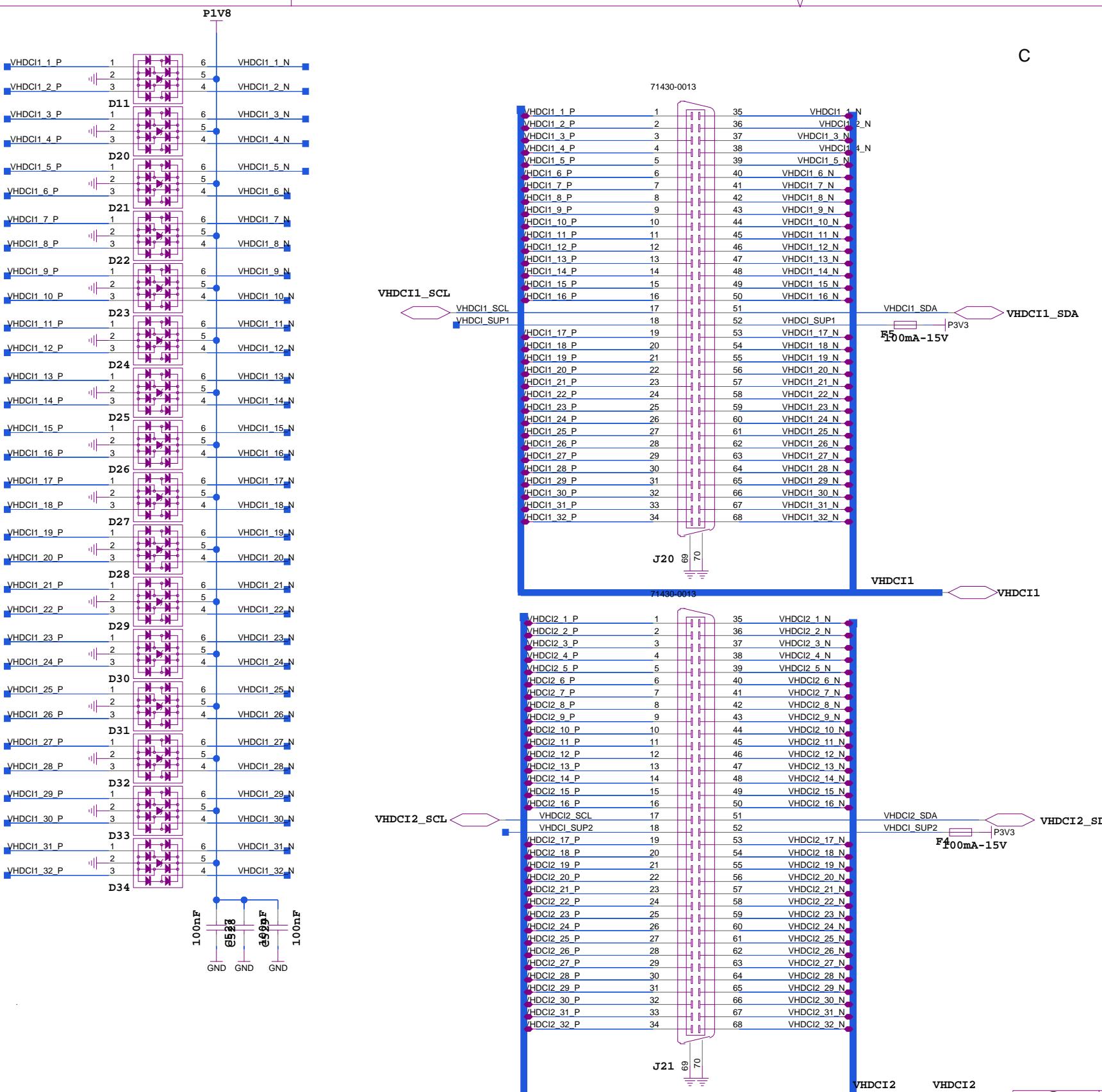
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USB_SERIAL_QUAD

SIZE	DWG NO	REV
A3		v0.9
DRAWN BY	SHEET of	
G.K.	25	1

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C



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SIZE	DWG NO	REV
A3		v0.9
DRAWN BY	SHEET OF	
G.K.	26	27