

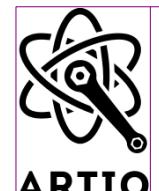
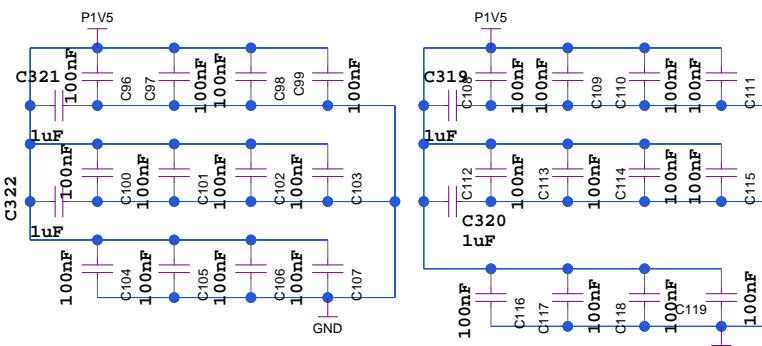
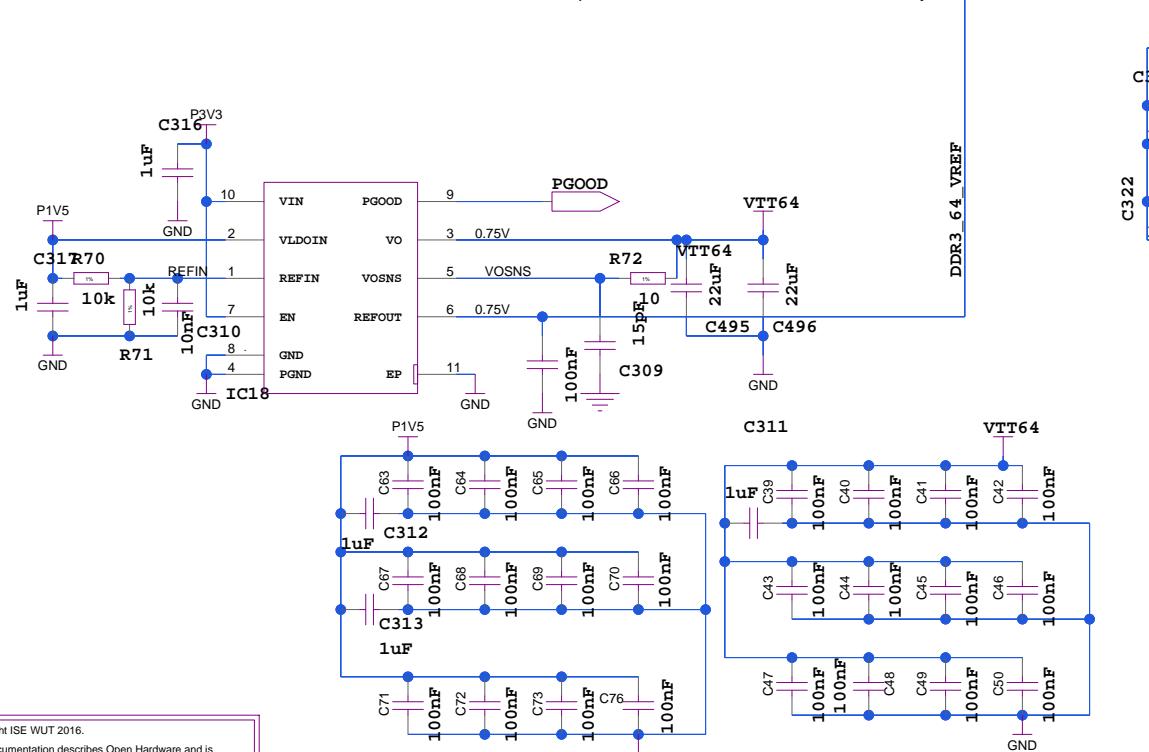
ARTIQ Sinara

Sayma_AMC

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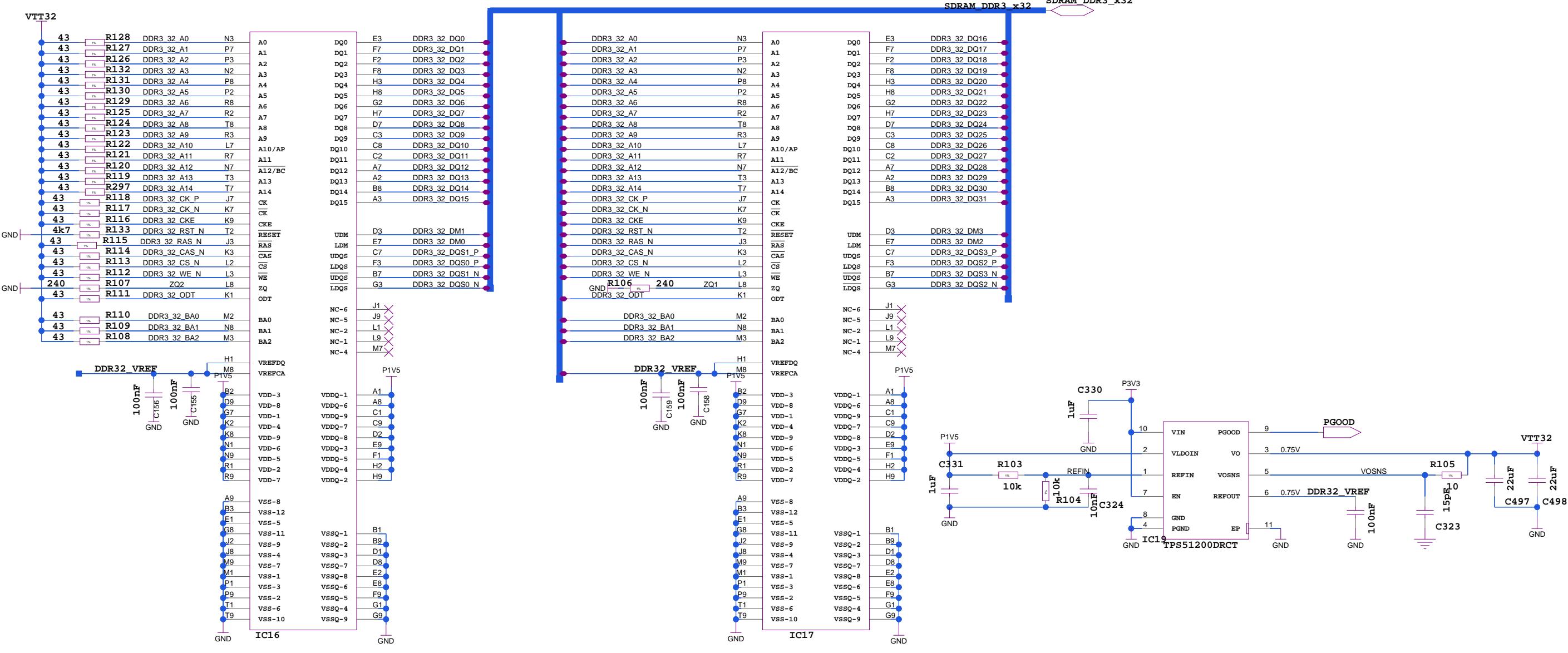
All capacitors without values are 100nF 0201 by default



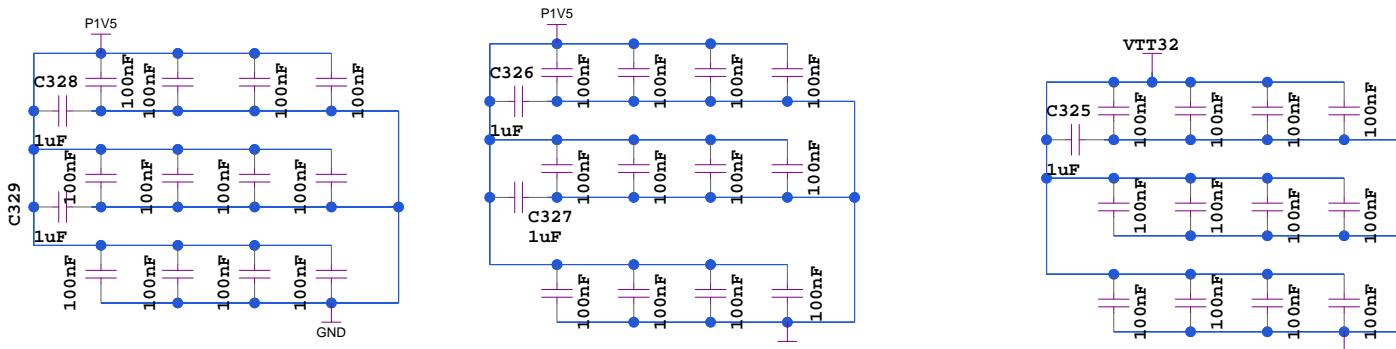
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SDRAM DDR3_4x16

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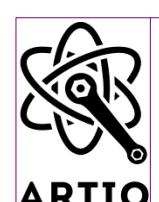
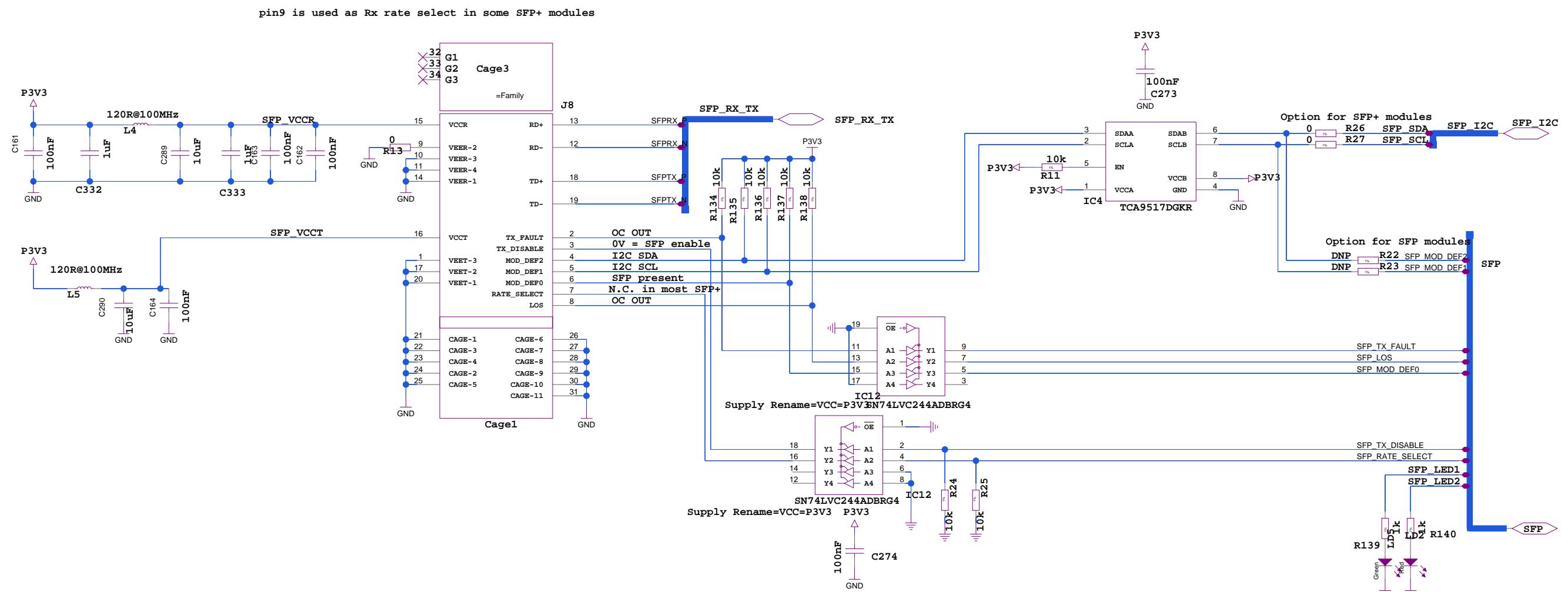
All capacitors without values are 100nF 0201 by default



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SDRAM DDR3 2x16

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SFP

SIZE DWG NO

A3

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G.K.

SHEET

of

4

31

REV
v0.97

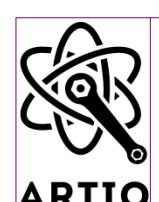
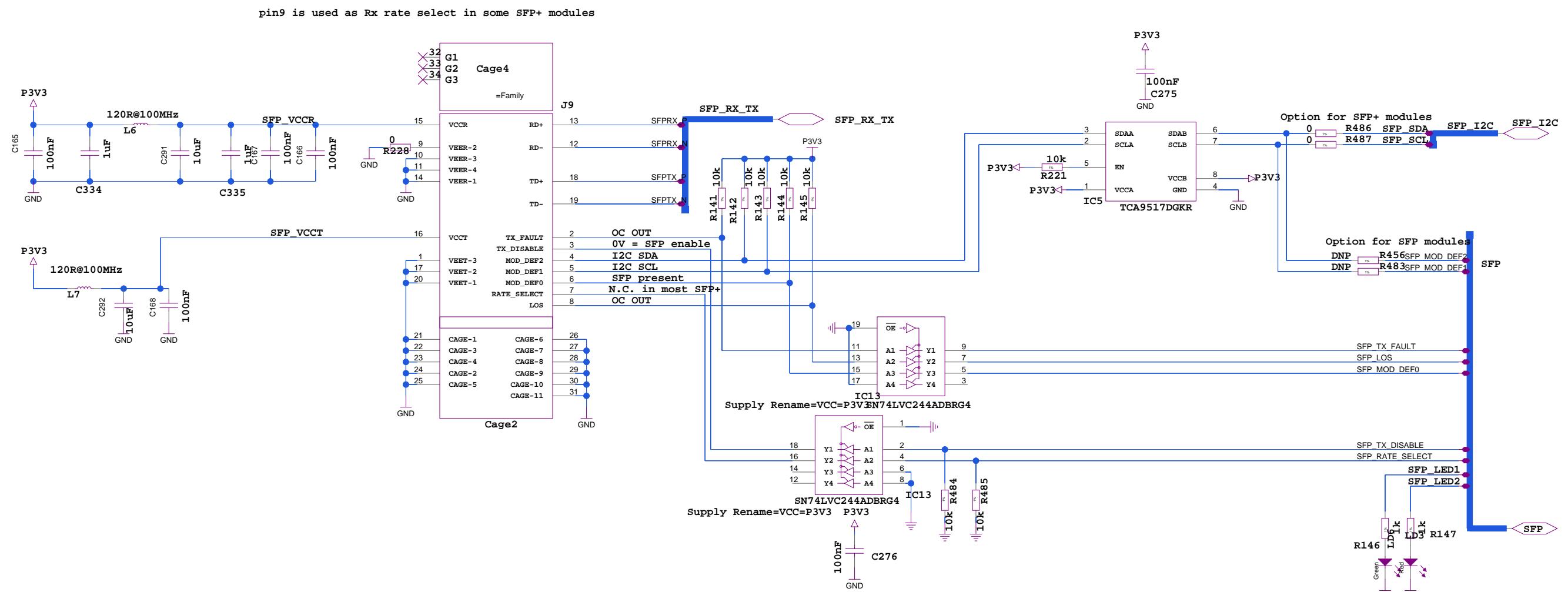
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REV
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SFP

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10/02/2017:01:06



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SFP

SIZE DWG NO

A3

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G.K.

SHEET

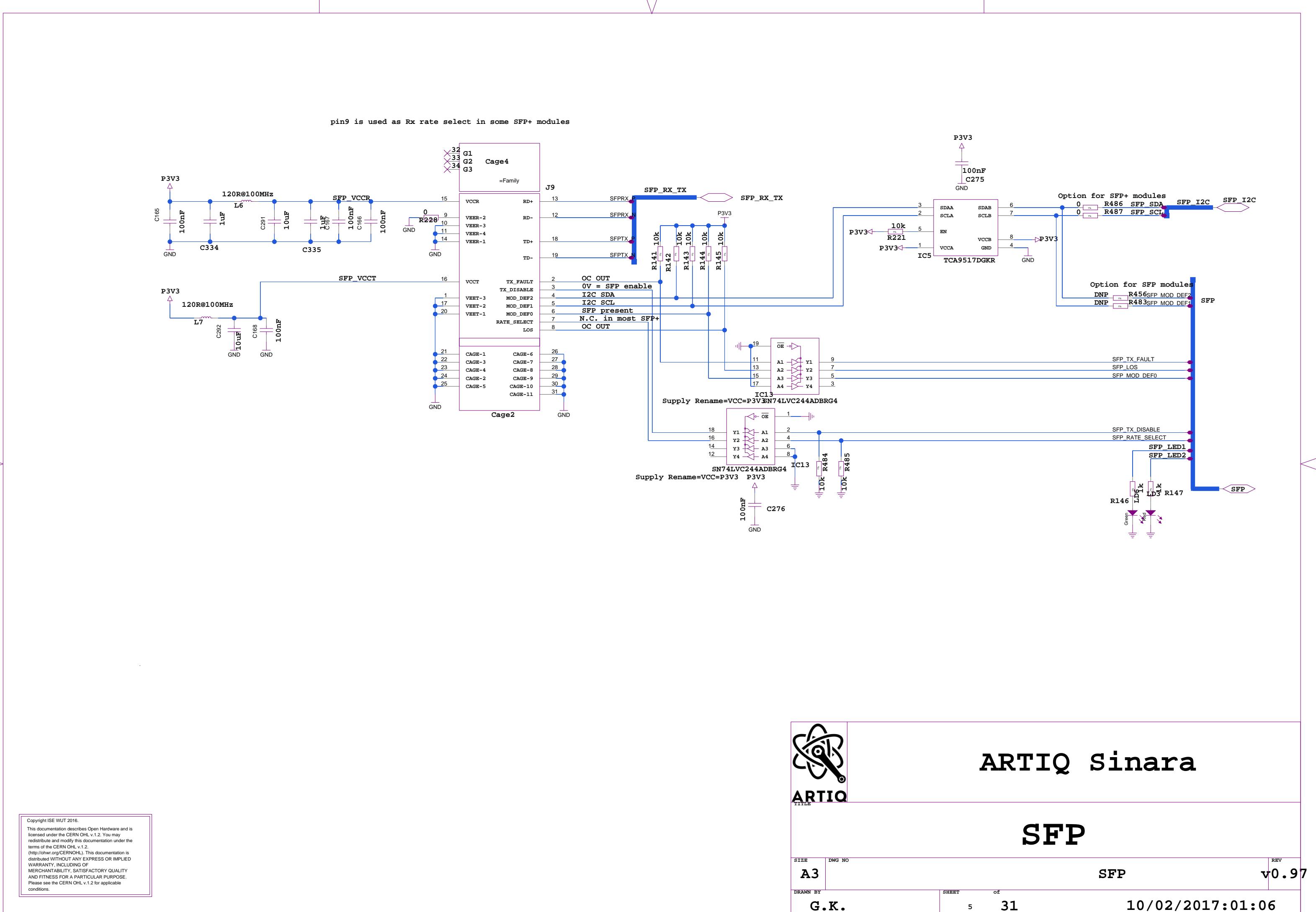
of

5

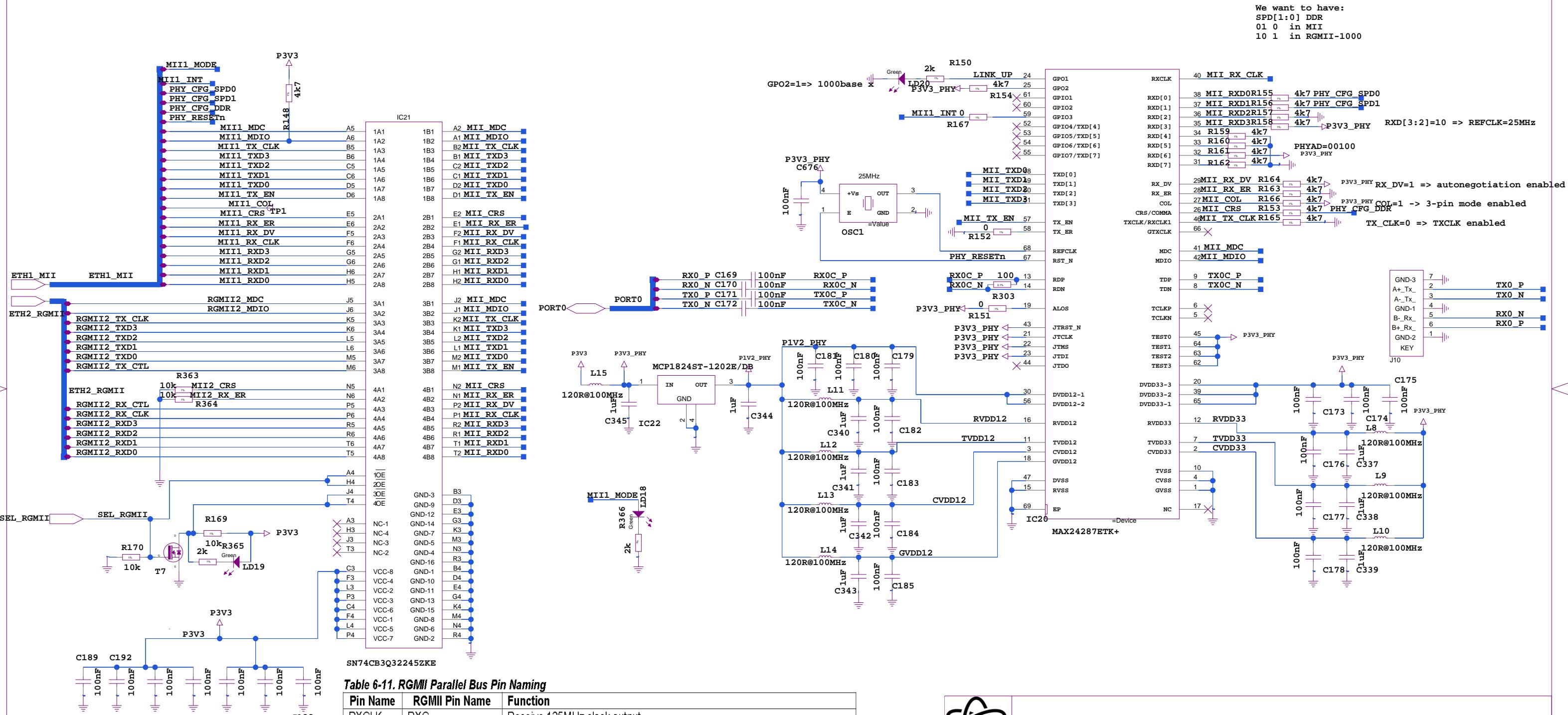
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REV
v0.97

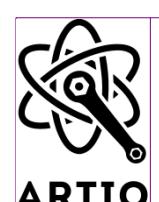
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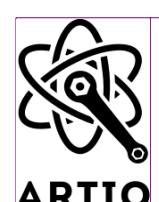
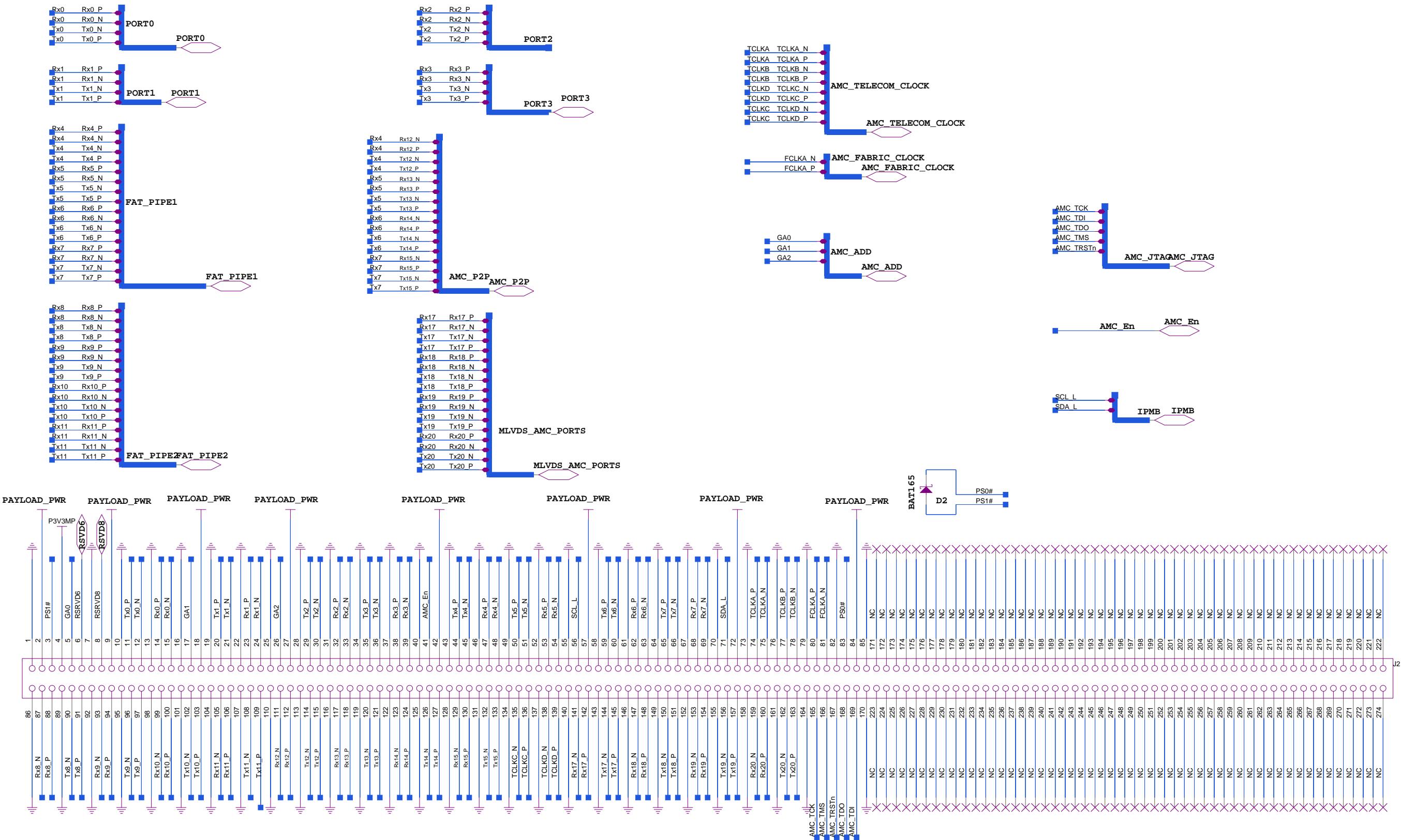


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ETH_PHY_RMII_MII



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AMC_Connector

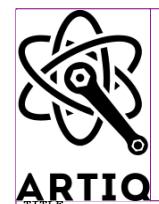
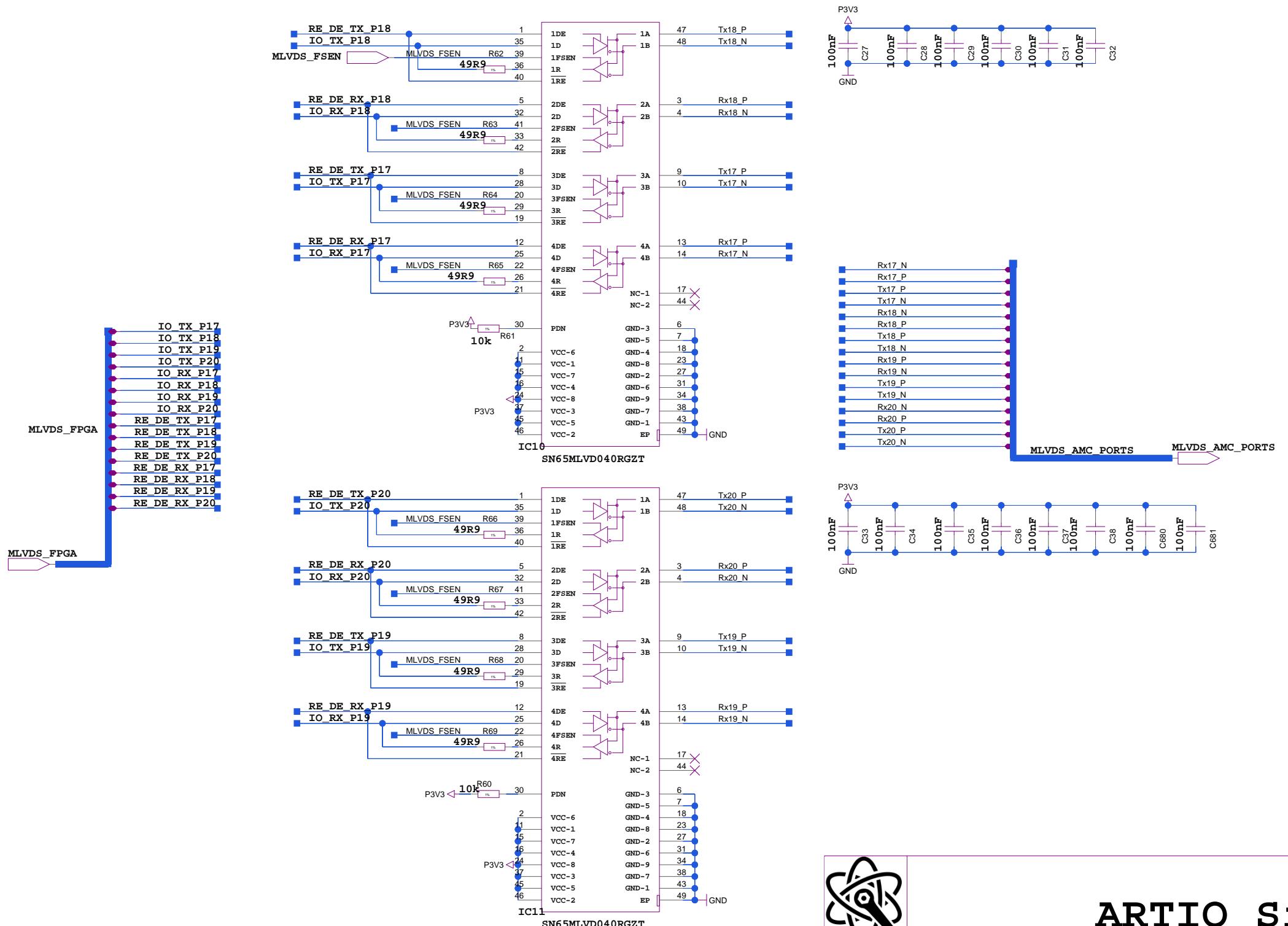
SIZE	DWG NO	REV
A3		v0.97
DRAWN BY		1
G.K.	7	31

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- Dimensions are in MM, nominal values used
- Component height rule derived from AMC Base Specification.PDF, Page 62
- The two corners of outline near the edge-connector are approximated, see AMC Base Specification.PDF, Page 59
- Stackup is not specified in AMC Base Specification.PDF or implemented in this template.

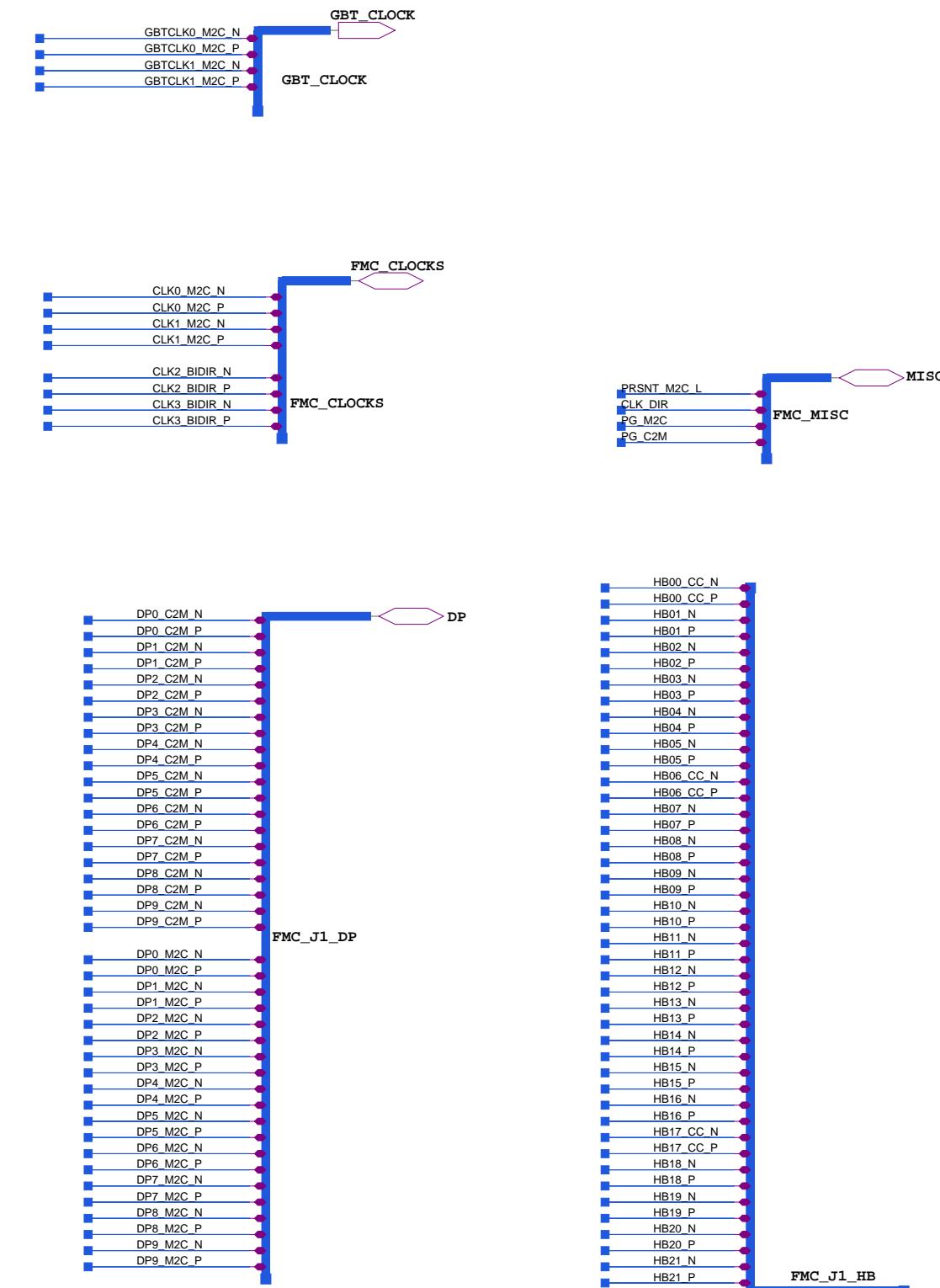
14/02/2017:17:27



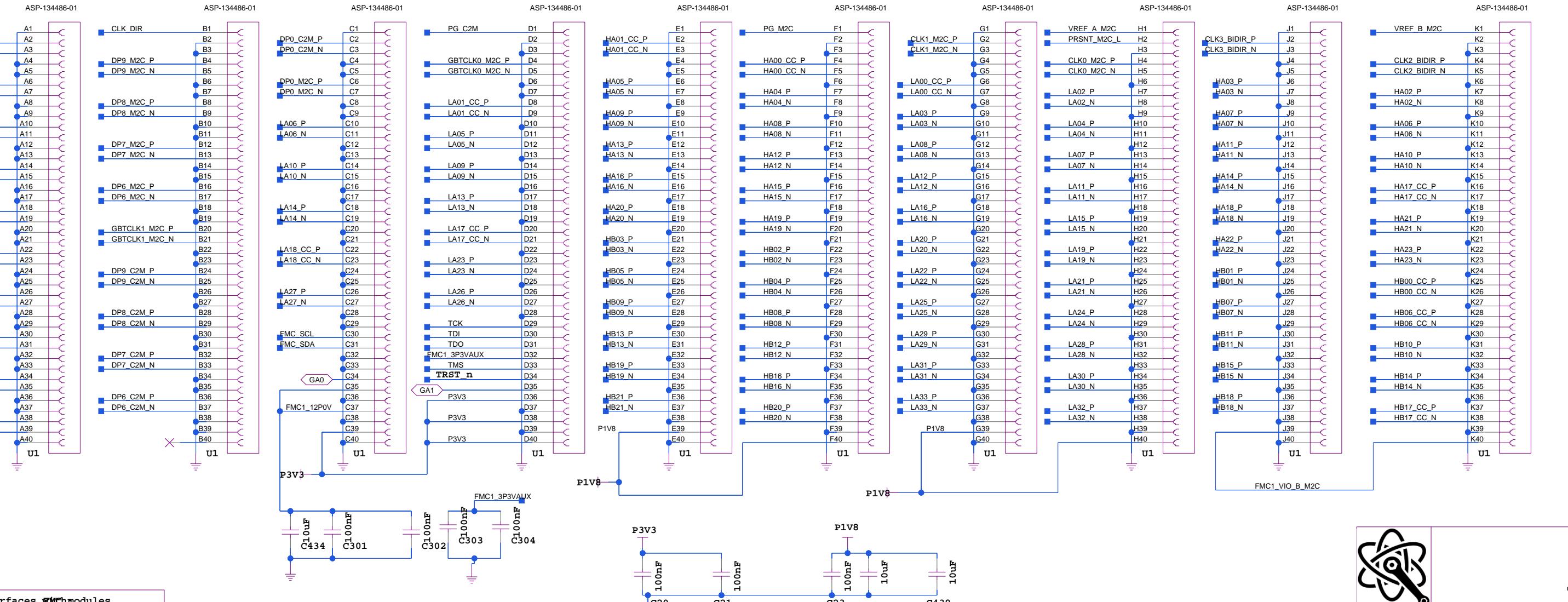
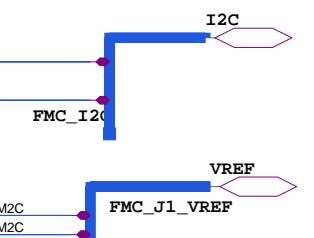
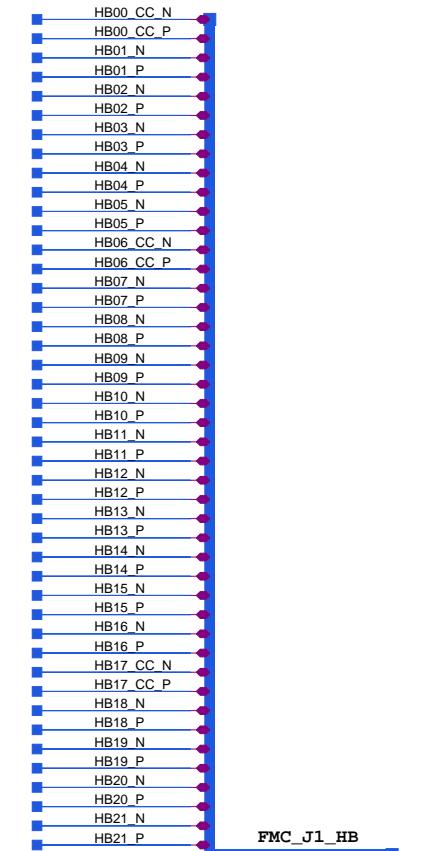
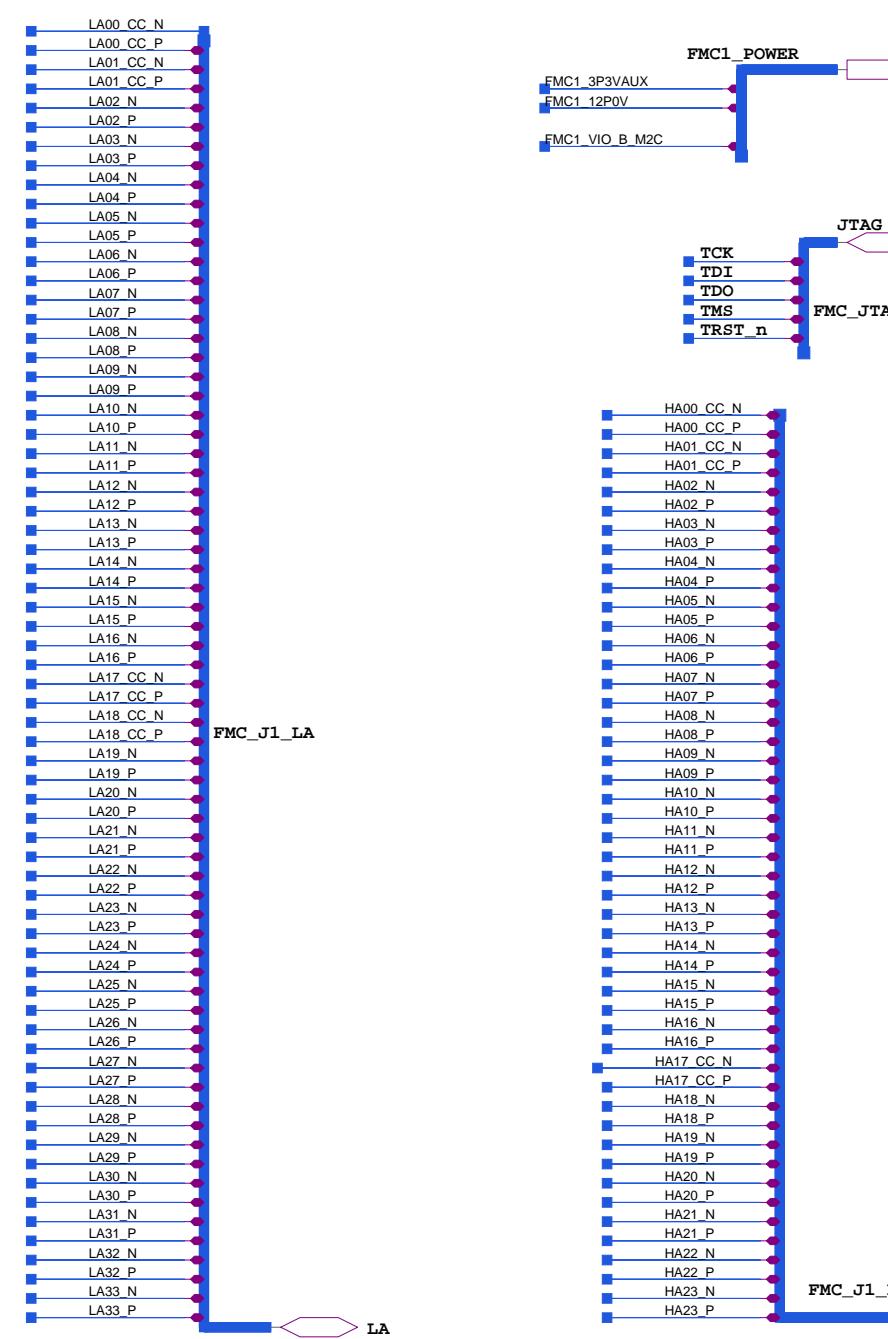
ARTIQ Sinara

M-LVDS PHY

SIZE	DWG NO		REV
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G.K.	8	31	24/01/2017:23:15



B1
B2
B3
B4



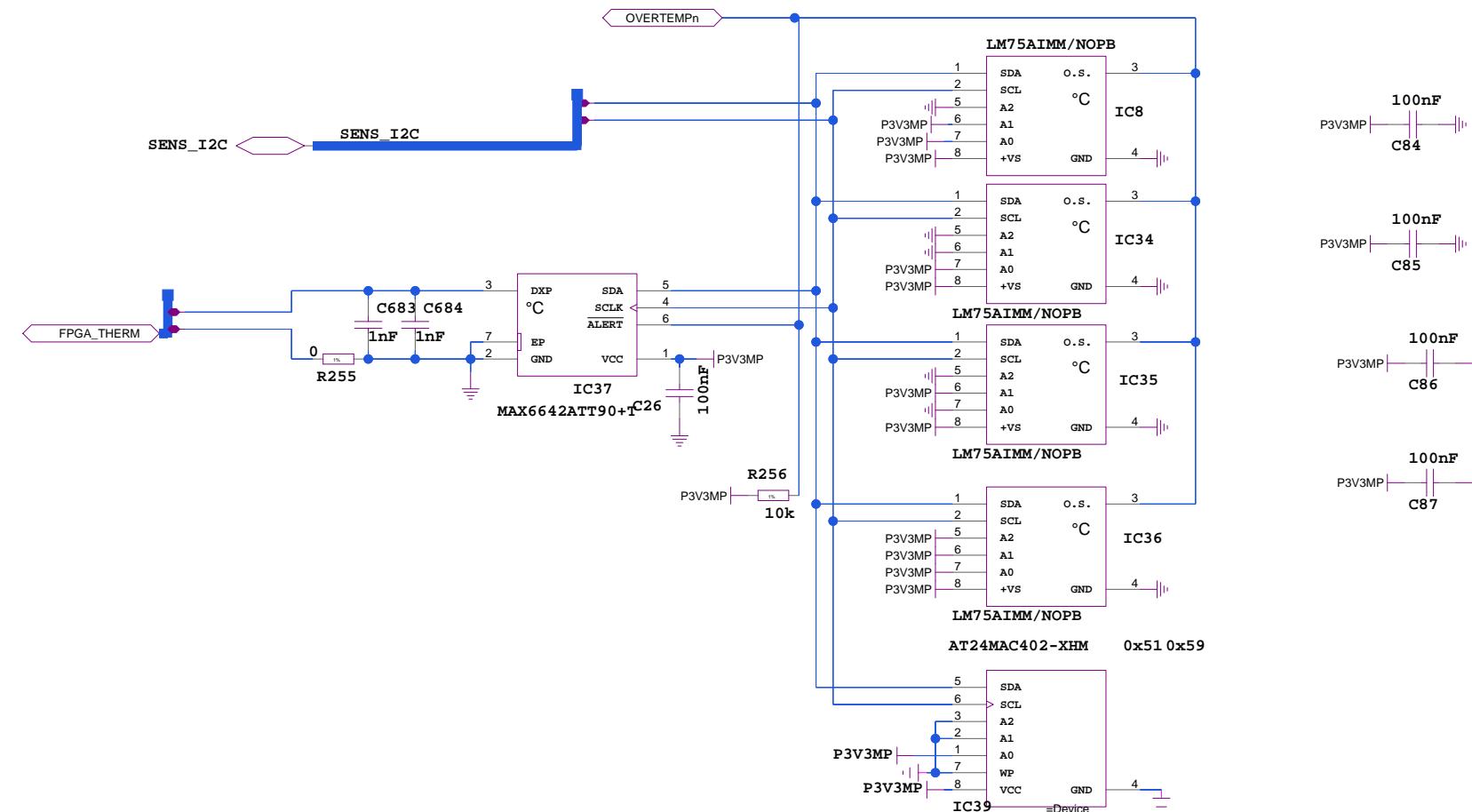
Interfaces with modules
Impedance: 100Ω diff
diff lines: LVDS 2.5V
control signals: 3.3V LVC MOS

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FMC_connector



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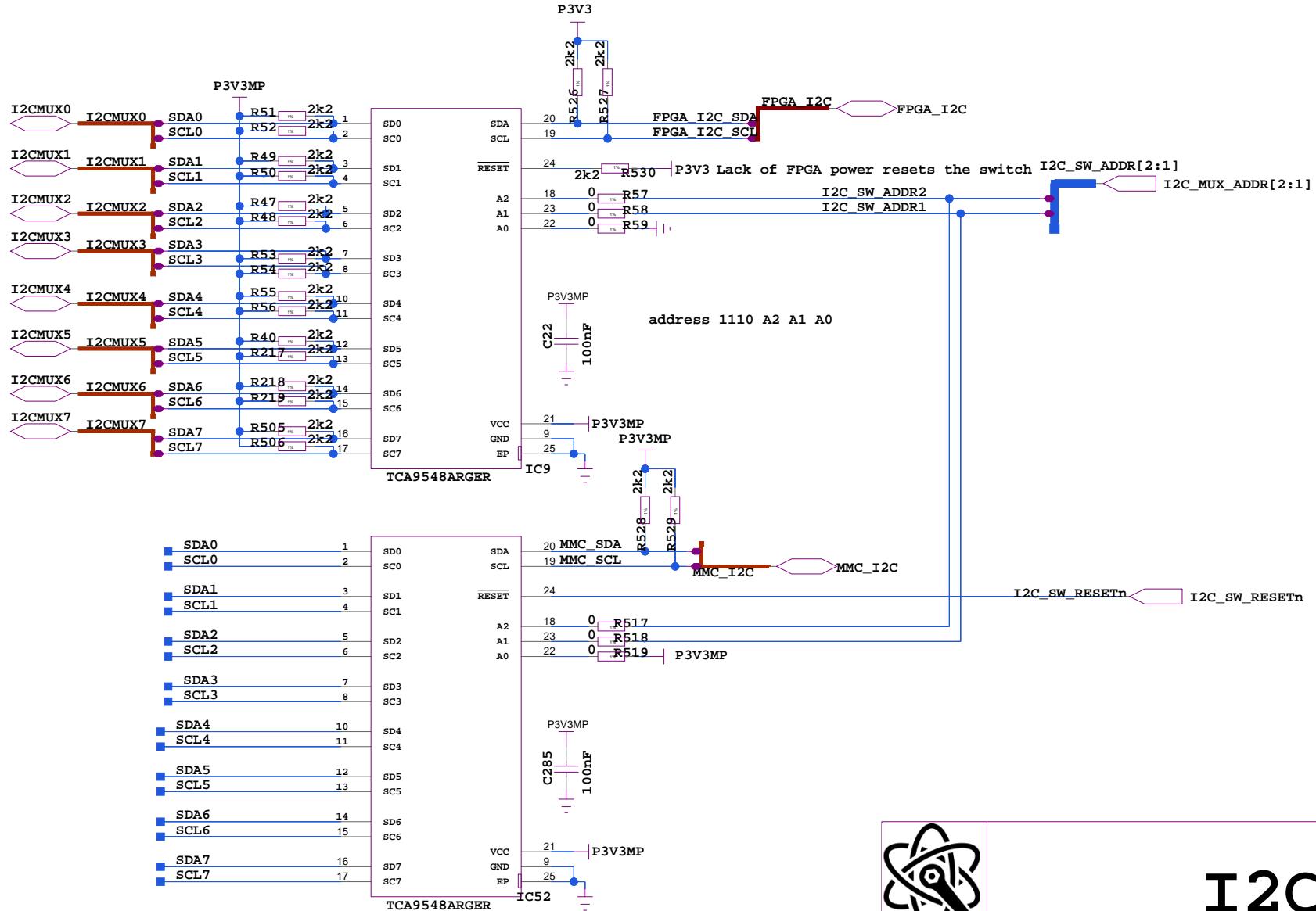
Thermometers

SIZE	DWG NO	REV
A3		v0.97
DRAWN BY	SHEET of	
G.K.	11	31

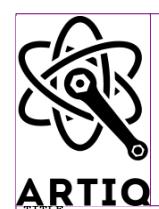
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13/02/2017:18:45

I2C switch footprint is compatible with MAX7358 which has interesting anti-lock capabilities



I2C_MUX



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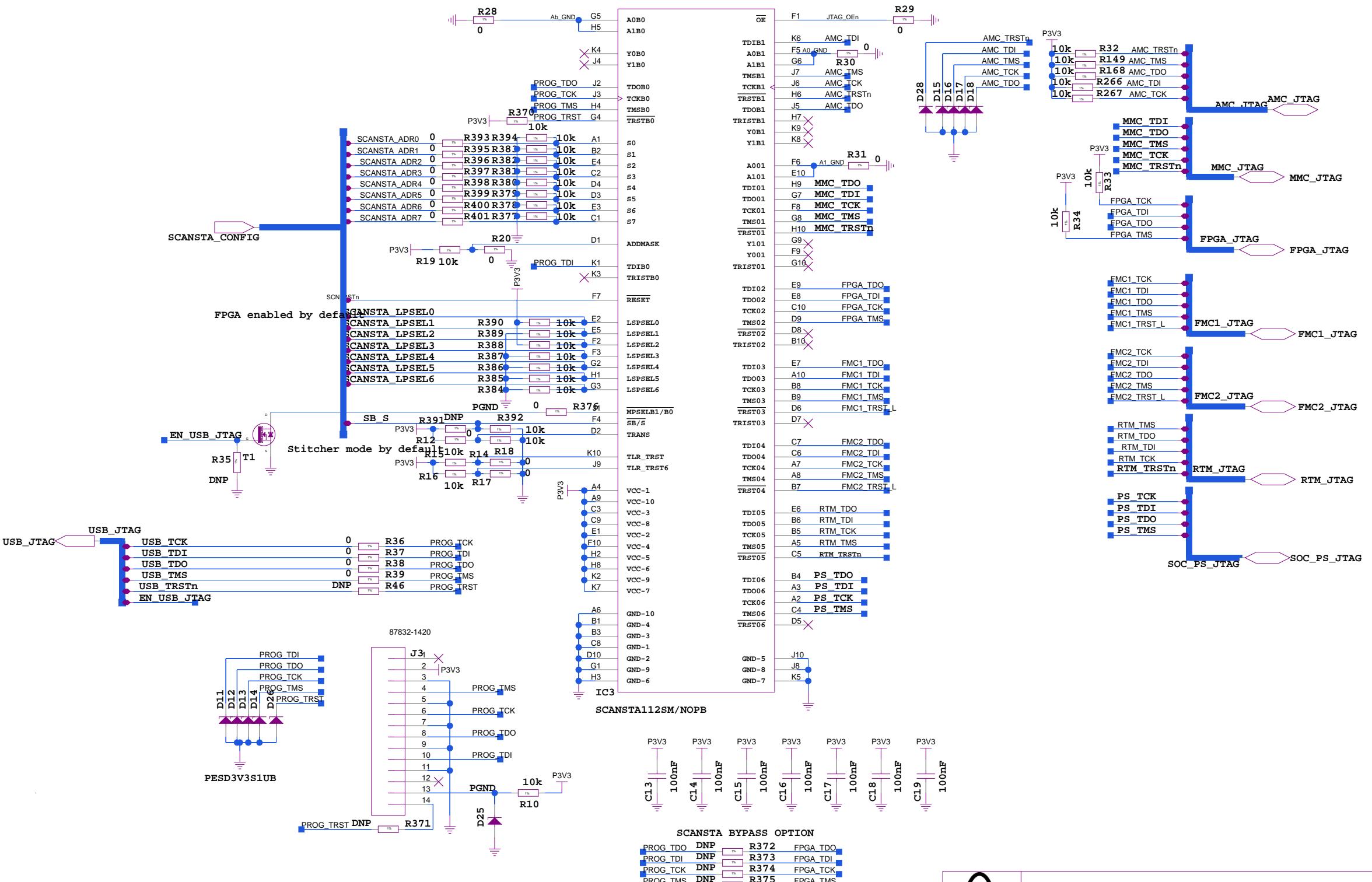
REV
v0.97

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SHEET of

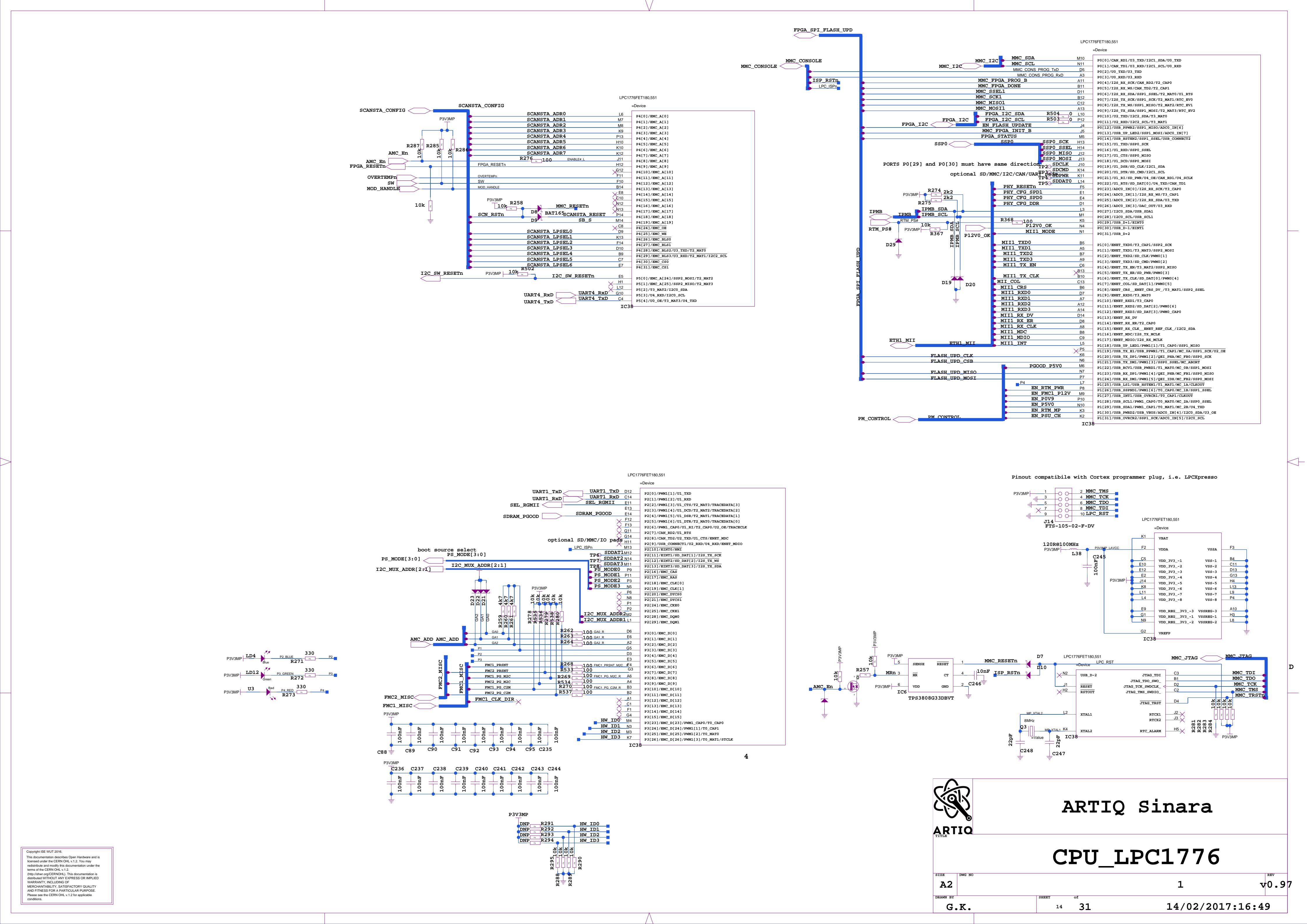
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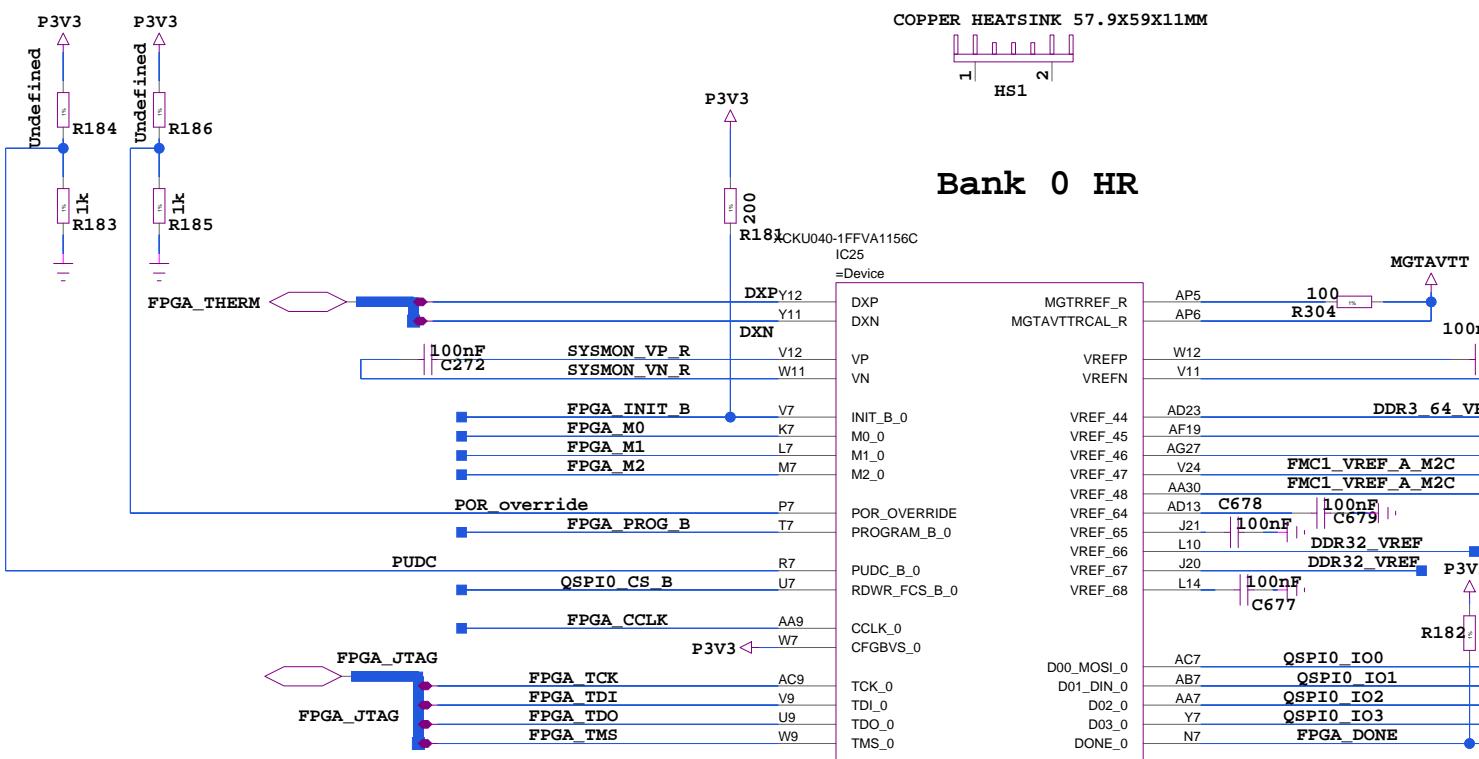


ARTIQ Sinara

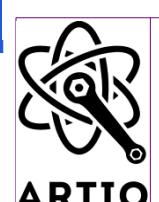
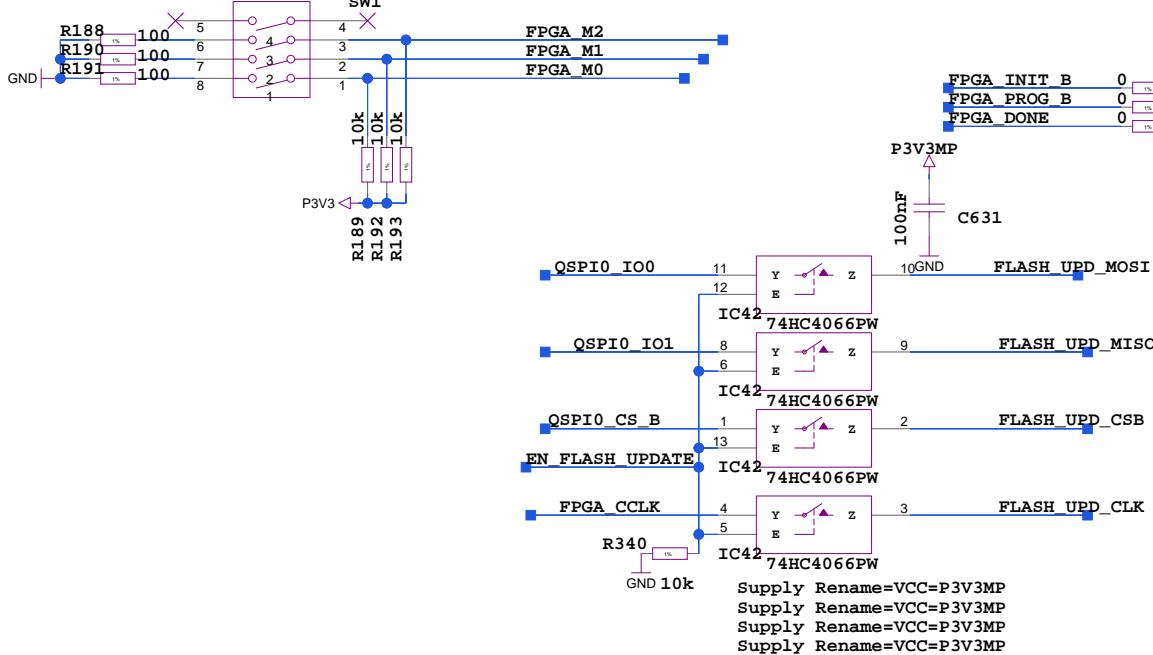
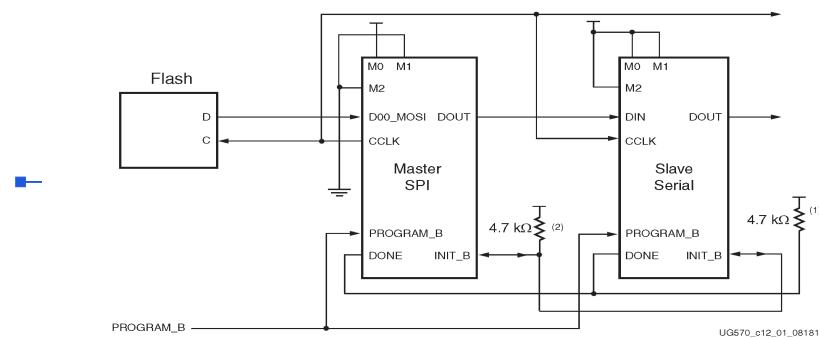
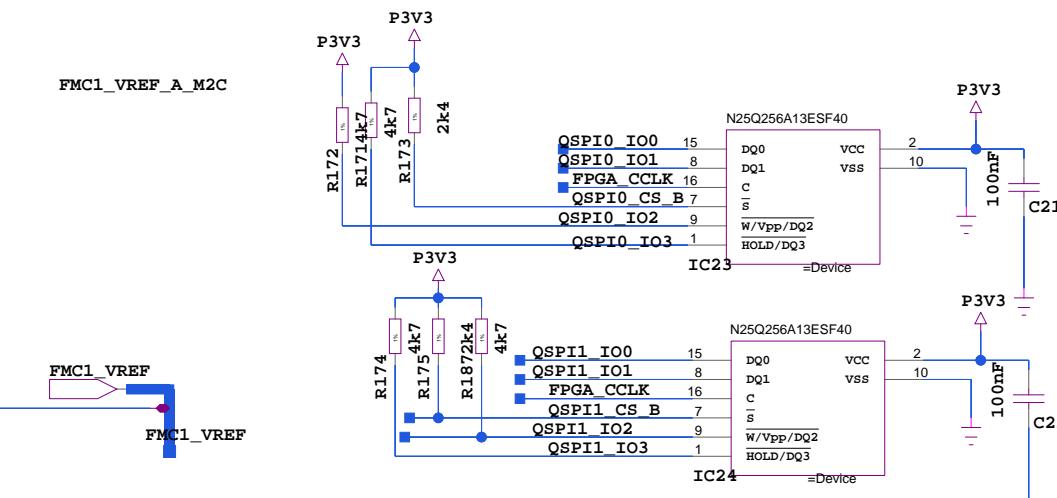
JTAG_Configuration

SIZE	DWG NO	REV
A3		v0.97
DRAWN BY	SHEET of	1
G.K.	13	31





Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via



FPGA_XCKU040FFVA1156

ARTIQ Sinara

FPGA Bank 0 CFG

A3

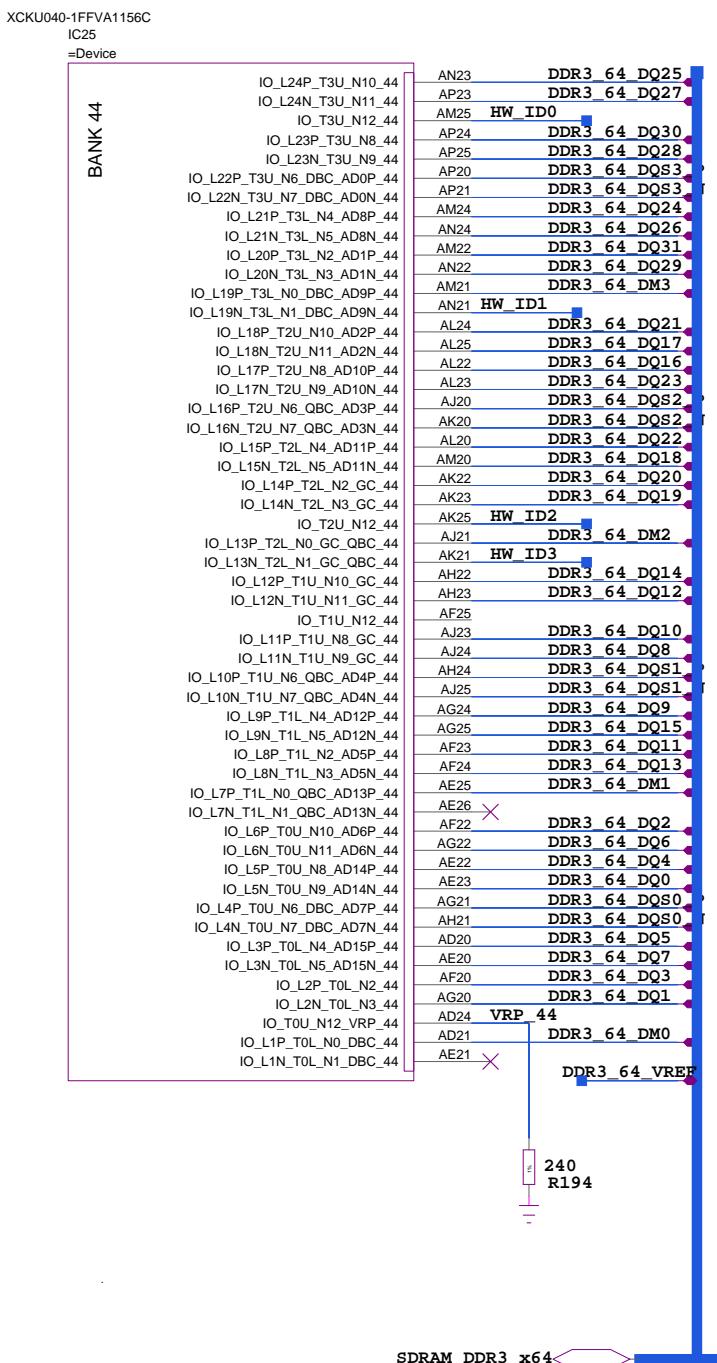
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15 31

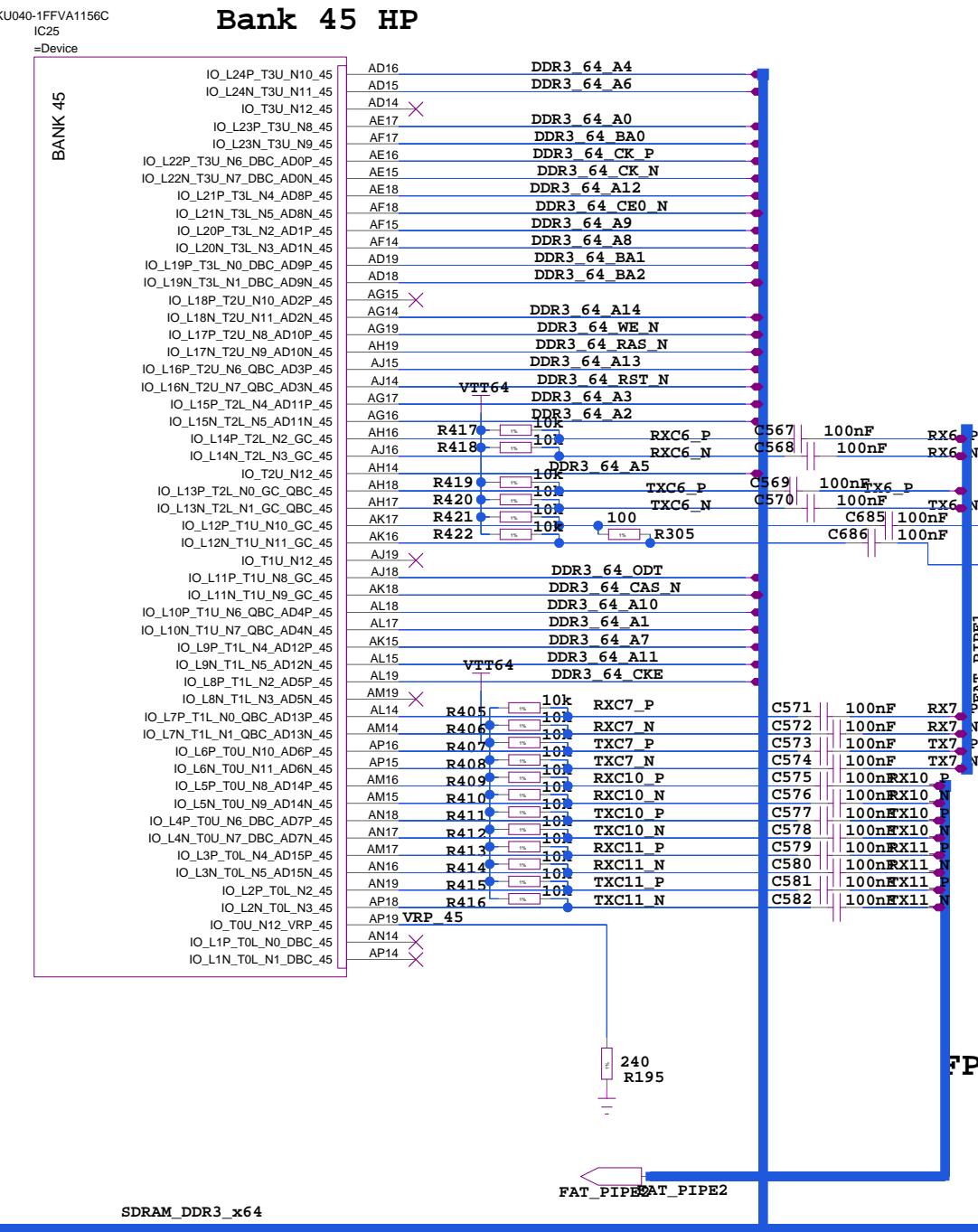
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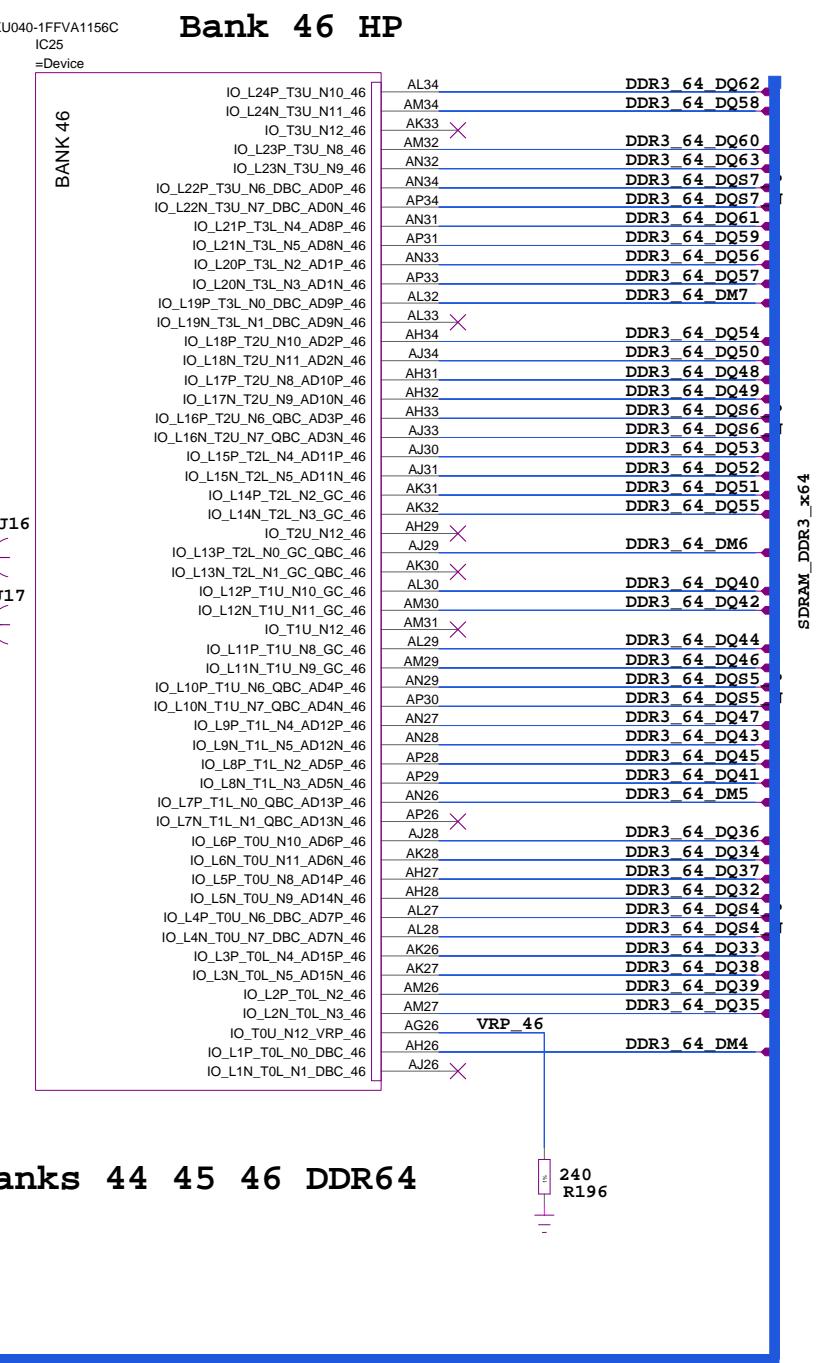
Bank 44 HP



Bank 45 HP

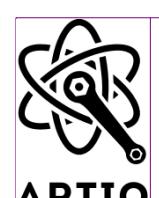


Bank 46 HP



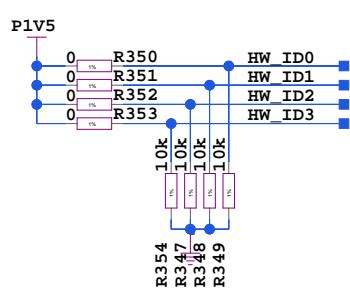
FPGA Banks 44 45 46 DDR64

FPGA_XCKU040FFVA1156



ARTIQ Sinara

SIZE DWG NO
A3
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SHEET 1 OF 1
REV v0.97



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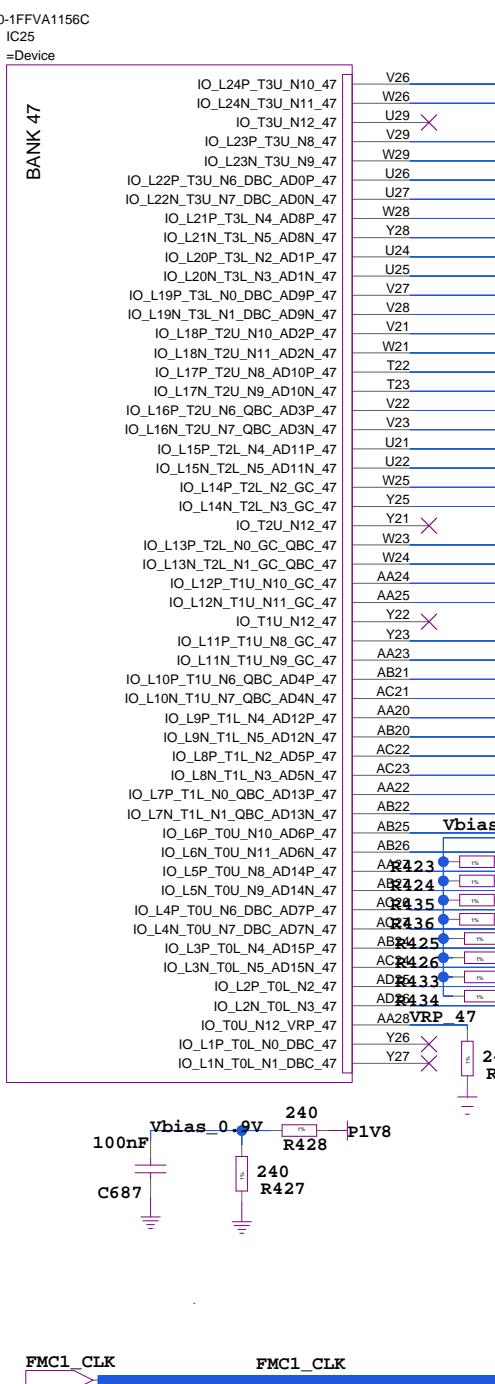
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16

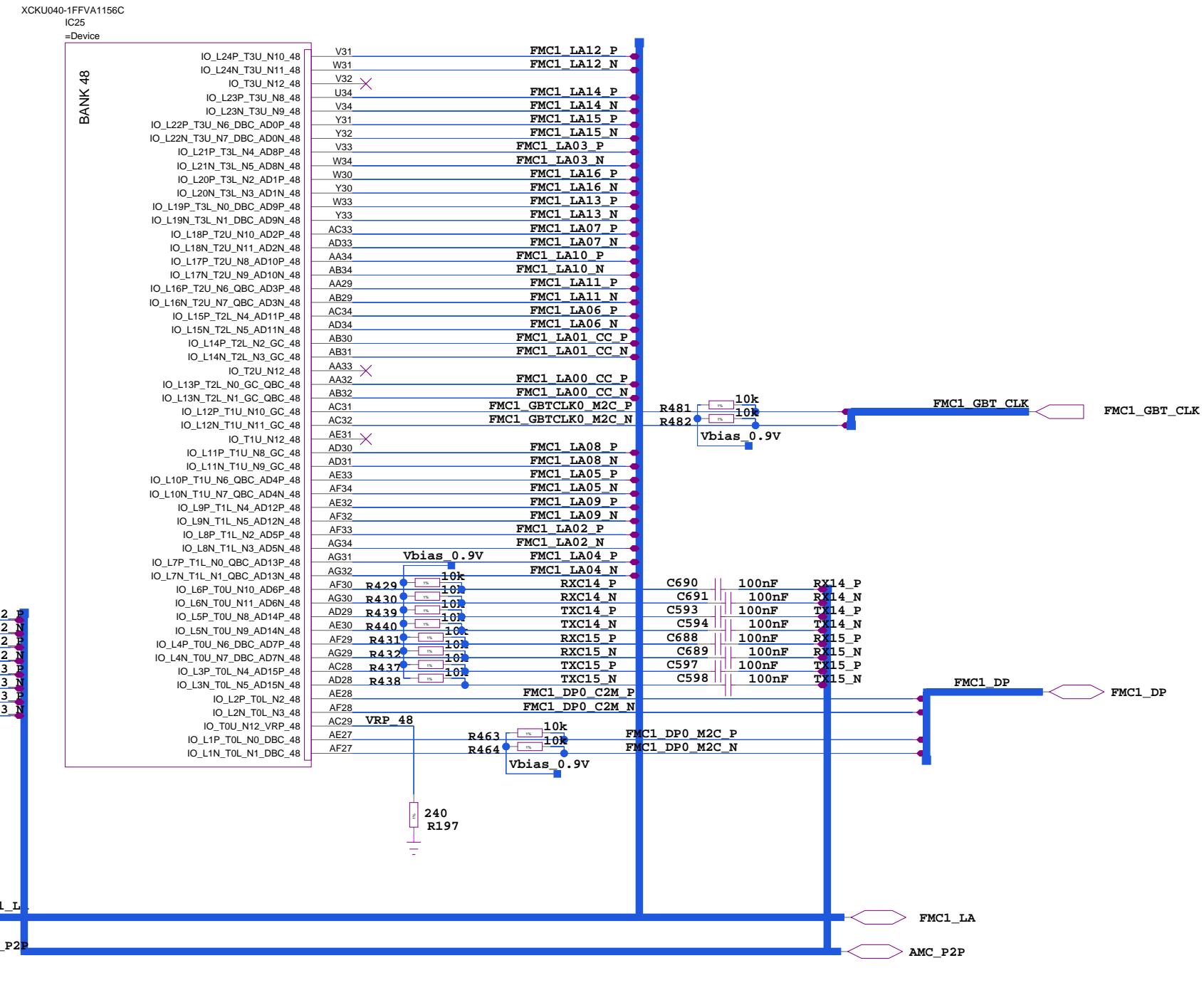
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24/01/2017:23:12

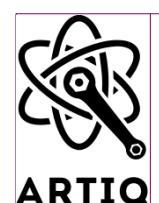
Bank 47 HP



Bank 48 HP



FPGA_XCKU040FFVA1156



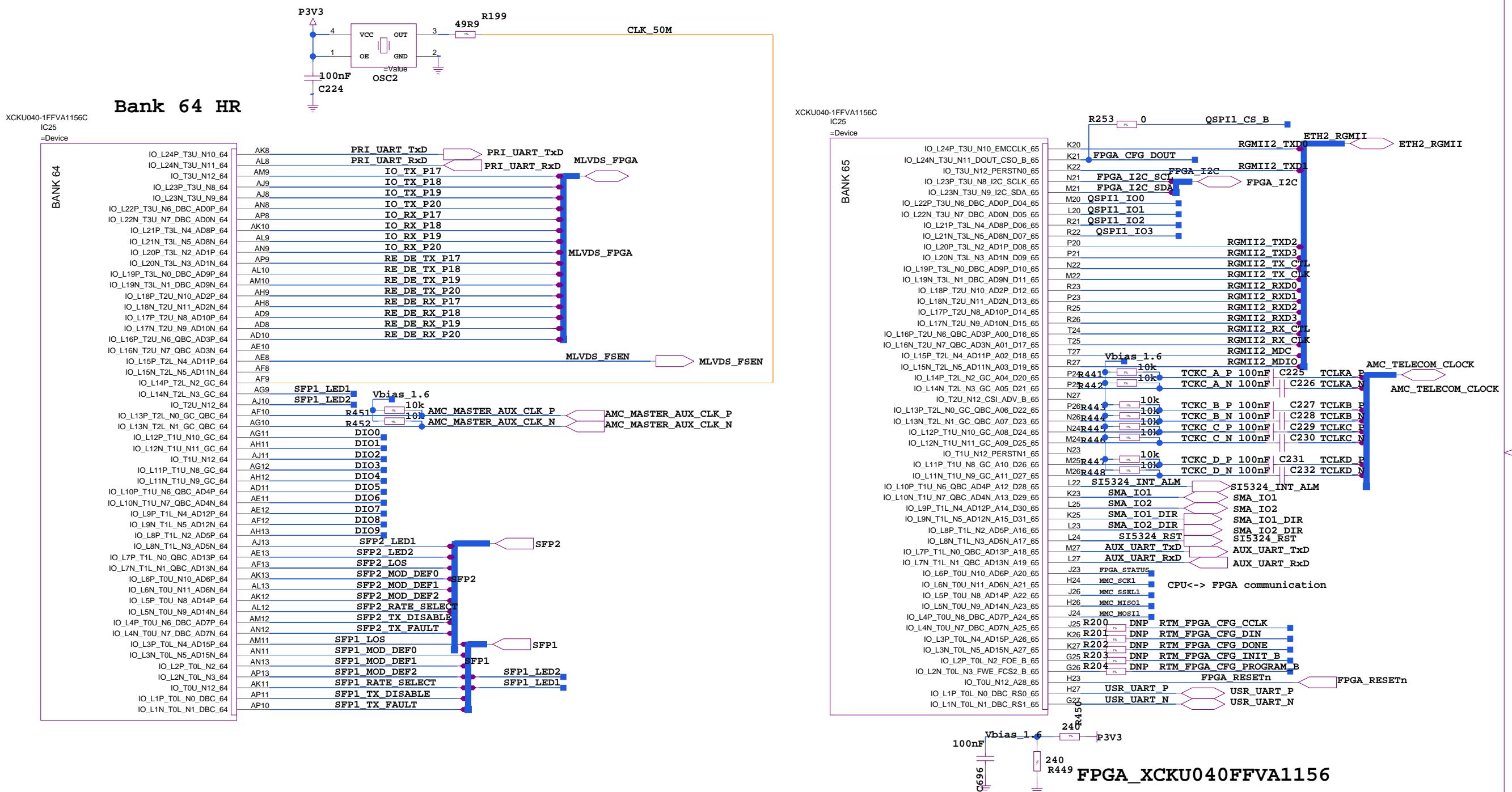
ARTIQ Sinara

FPGA Banks 47 48 HP FM

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SIZE DWG NO
A3
DRAWN BY G.K. SHEET 17 of 31
REV v0.97
14/02/2017:01:16

Bank 65 HR

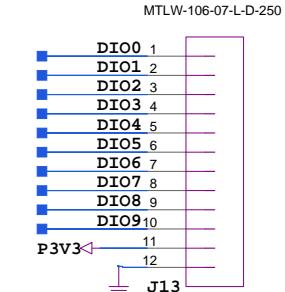


ARTIQ Sinara

FPGA Banks 64 65 HR

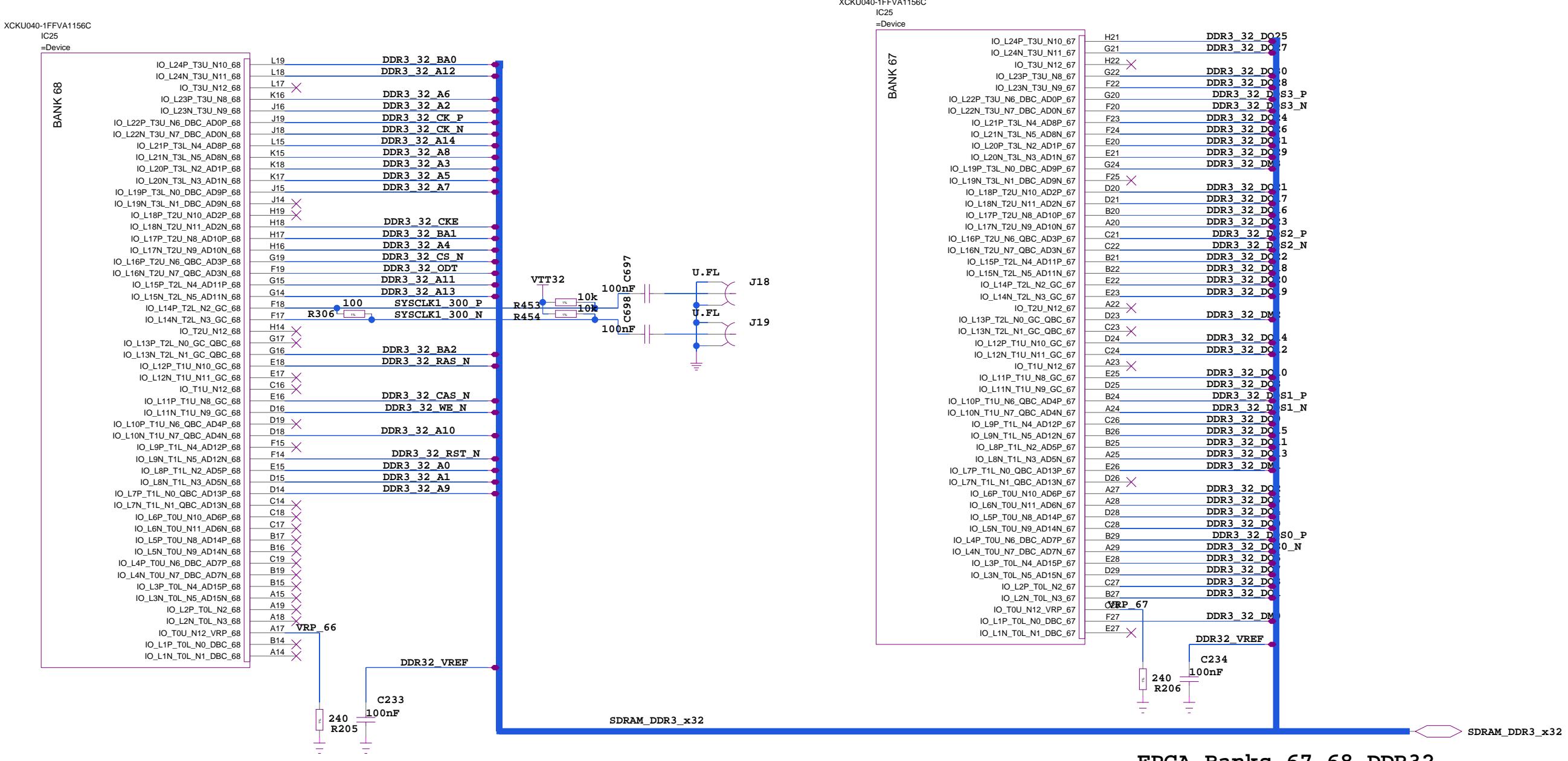
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A3		v0.97
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G.K.	18	31

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Bank 68 HP Underneath the FPGA via array right next to the via

Bank 67 HE



FPGA XCKU040FFVA1156

APRETO *sin*

ARTIQ Sinara

FPGA Banks 67 68 DDR3

WG NO

1

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31

REV
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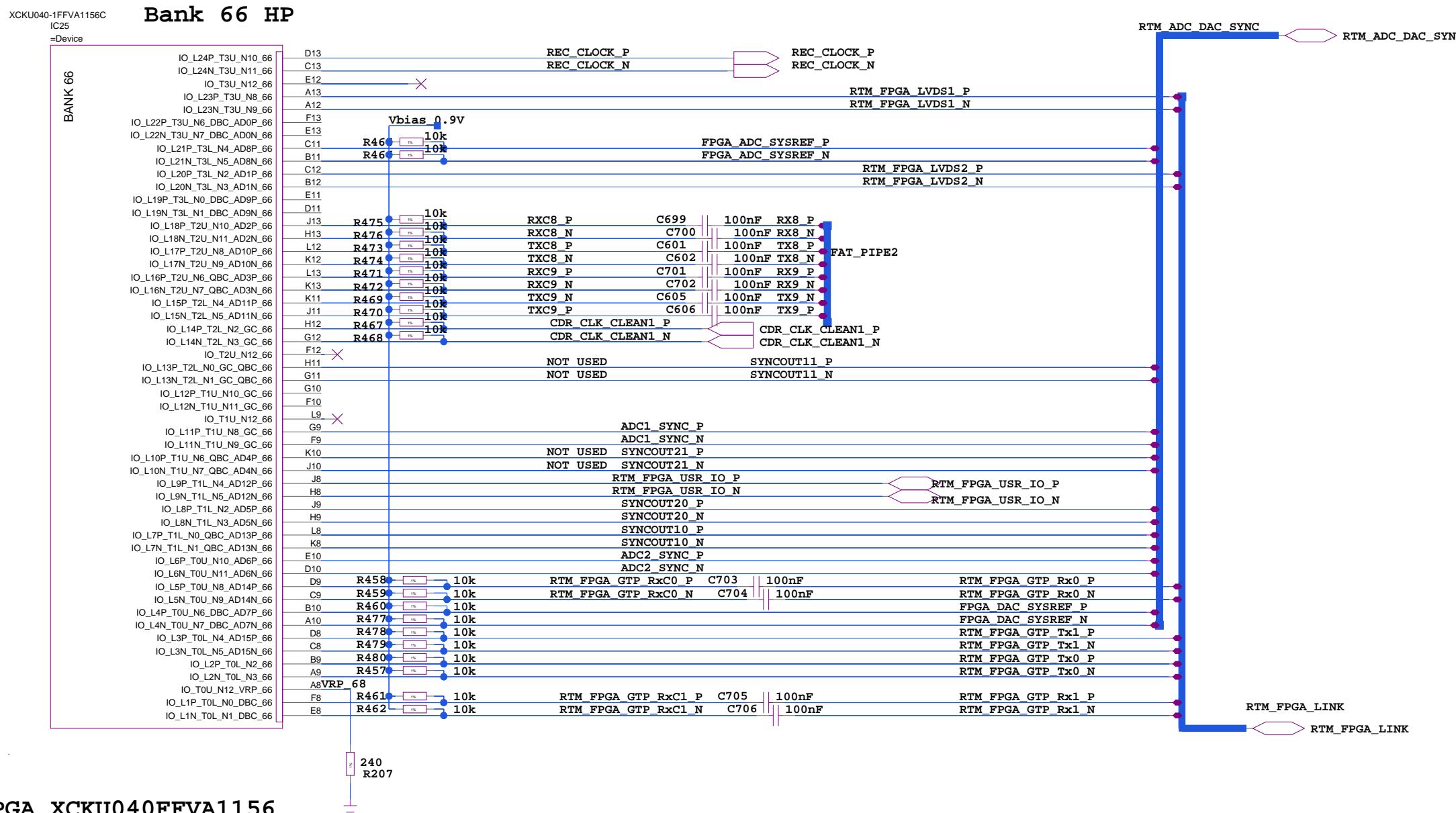
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Layout: Place resistor and capacitor for VREF

Vbias_0.9V

Underneath the FPGA via array
right next to the via



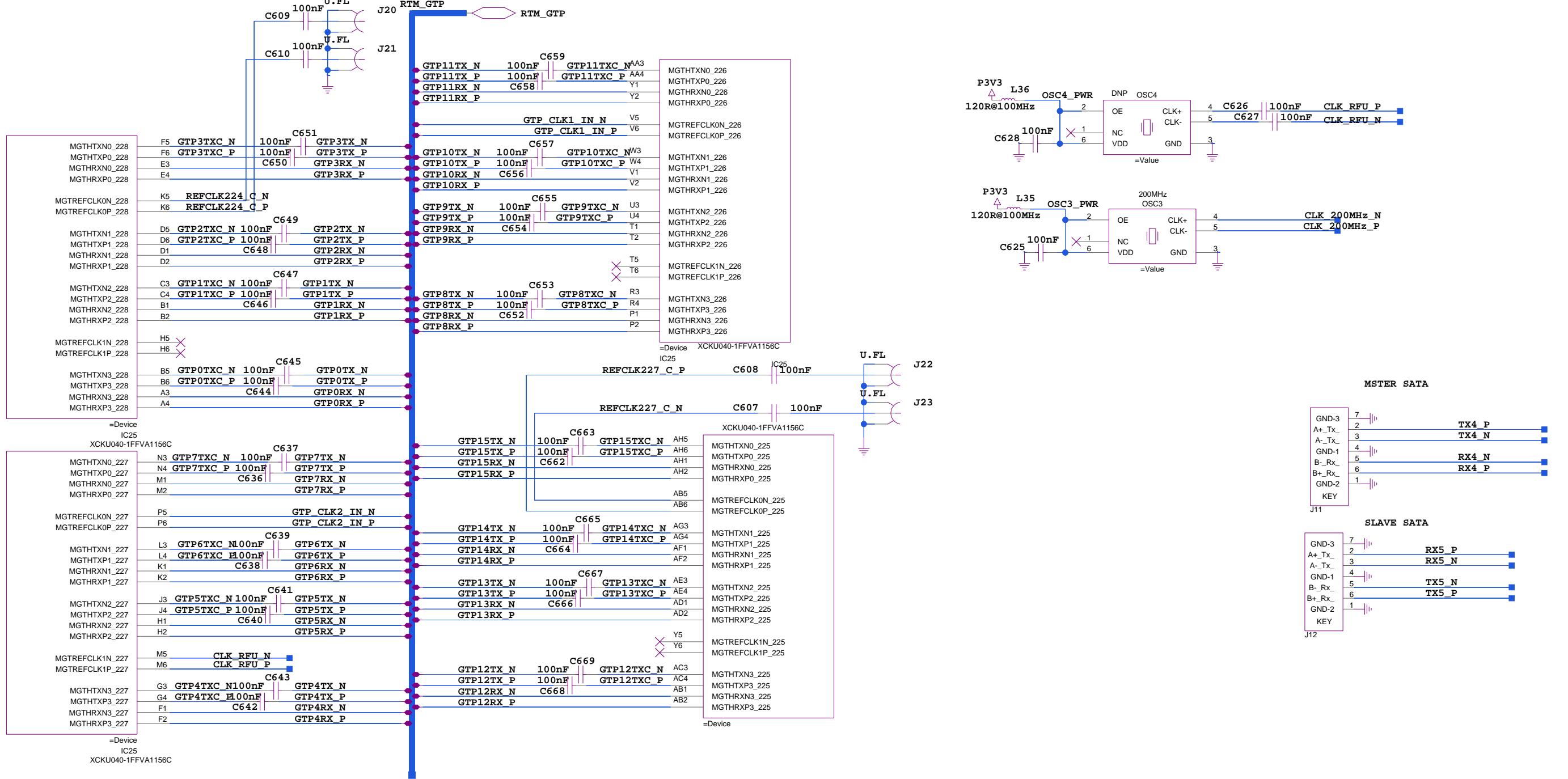
FPGA_XCKU040FFVA1156

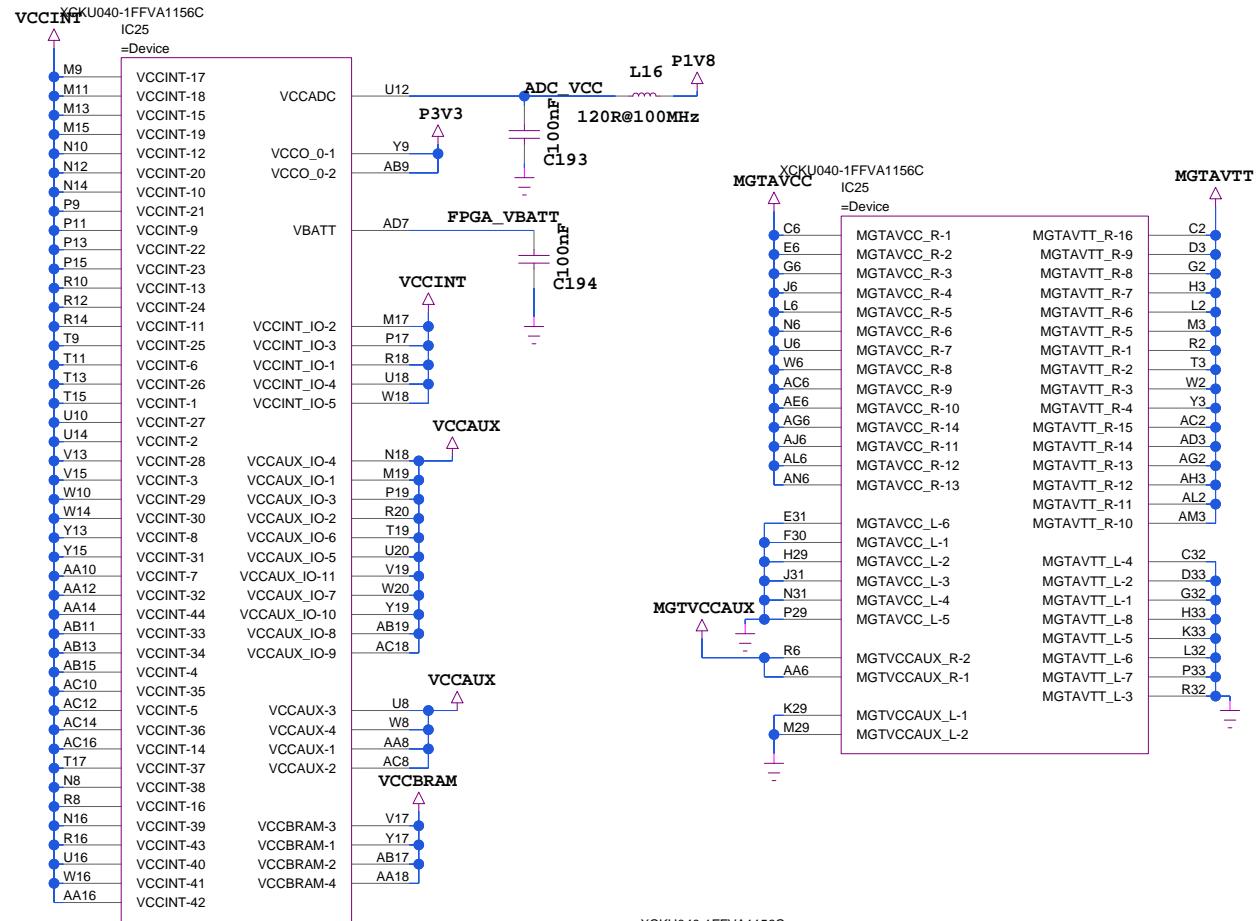
FPGA Bank 66 HF

ARTIQ Sinara

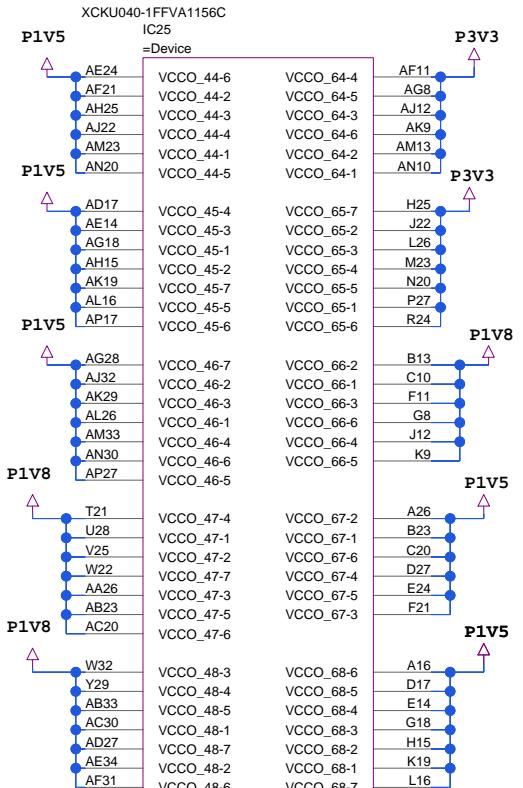
FPGA Bank 66 HP

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Power Supply		
Source	Voltage	Total (A)
V _{CCINT}	0.900	9.165
V _{CCINT_IO}	0.900	0.620
V _{CCBRAM}	0.950	0.031
V _{CCAUX}	1.800	0.660
V _{CCAUX_IO}	1.800	0.546
V _{CCO 3.3V}	3.300	0.000
V _{CCO 2.5V}	2.500	
V _{CCO 1.8V}	1.800	0.380
V _{CCO 1.5V}	1.500	0.936
V _{CCO 1.35V}	1.350	
V _{CCO 1.2V}	1.200	
V _{CCO 1.0V}	1.000	
MGTVC _{CAUX}	1.800	0.081
MGTAV _{CC}	1.000	3.038
MGTAV _{TT}	1.200	0.592
V _{CCADC}	1.800	0.014



FPGA Power

FPGA_XCKU040FFVA1156

ARTIQ Sinara

FPGA Power

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TITLE

SIZE DWG NO

A3

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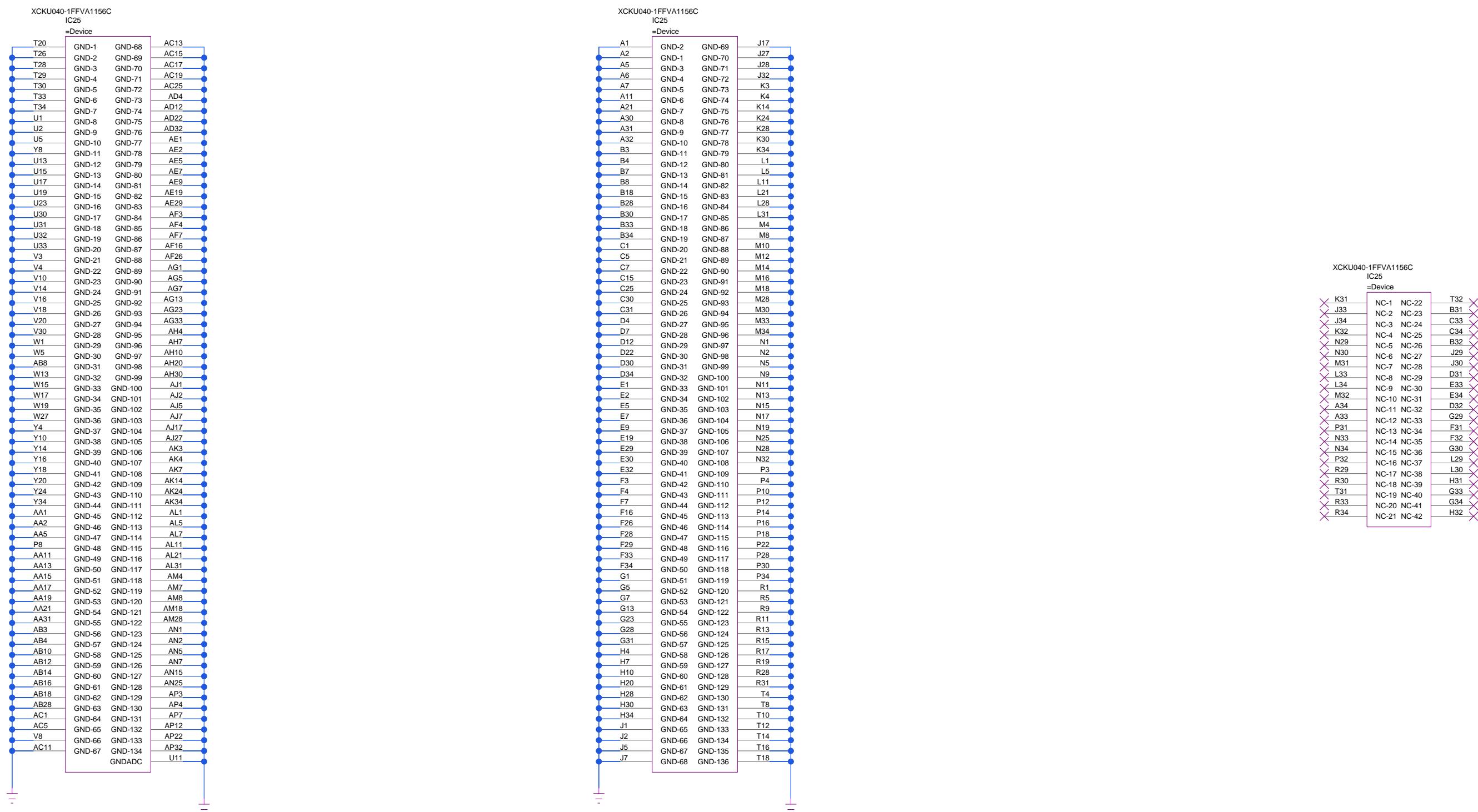
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v0.97

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FPGA_XCKU040FARMAQ1s6ara
ARTIQ

FPGA GND NC

SIZE DWG NO

A3

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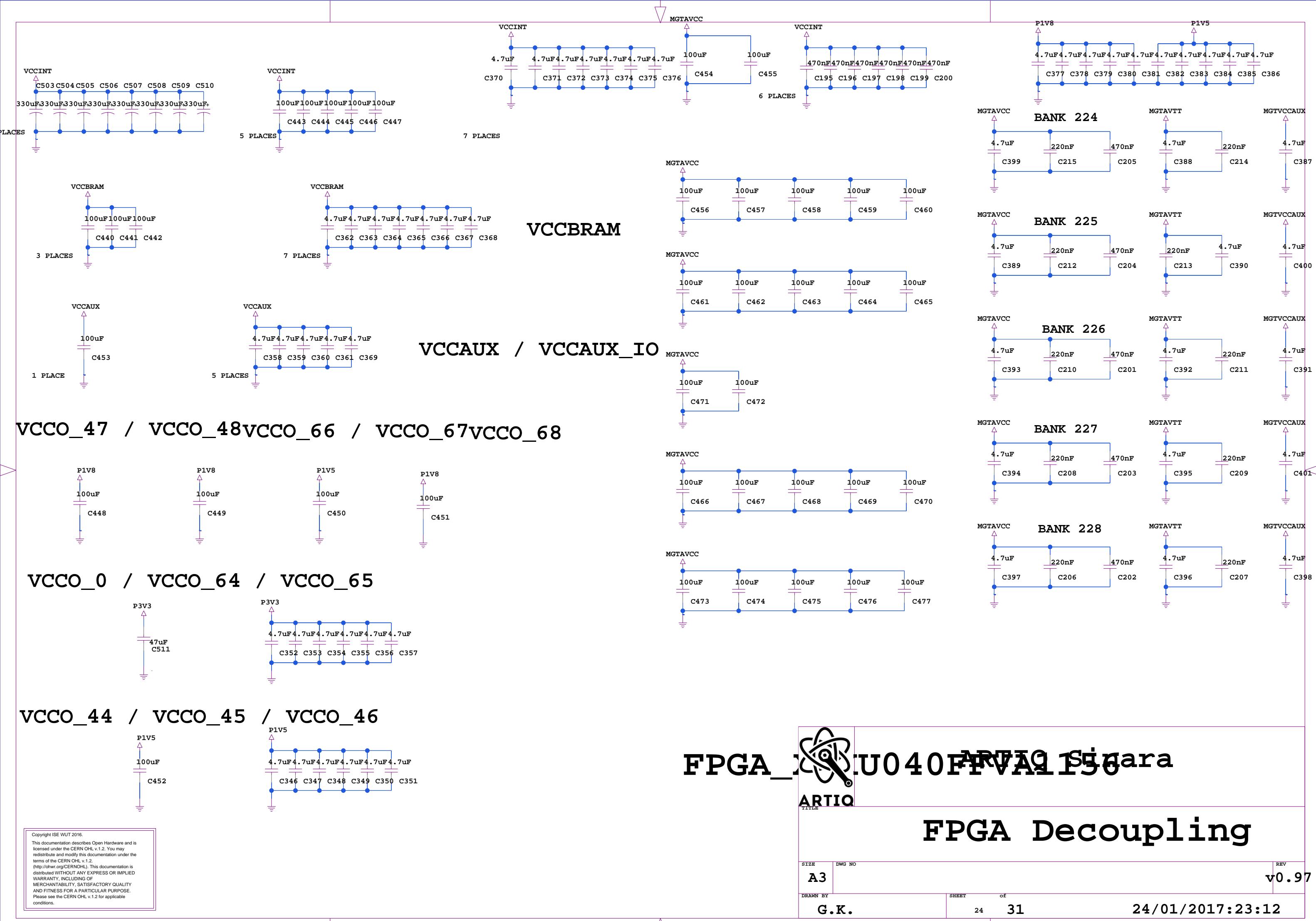
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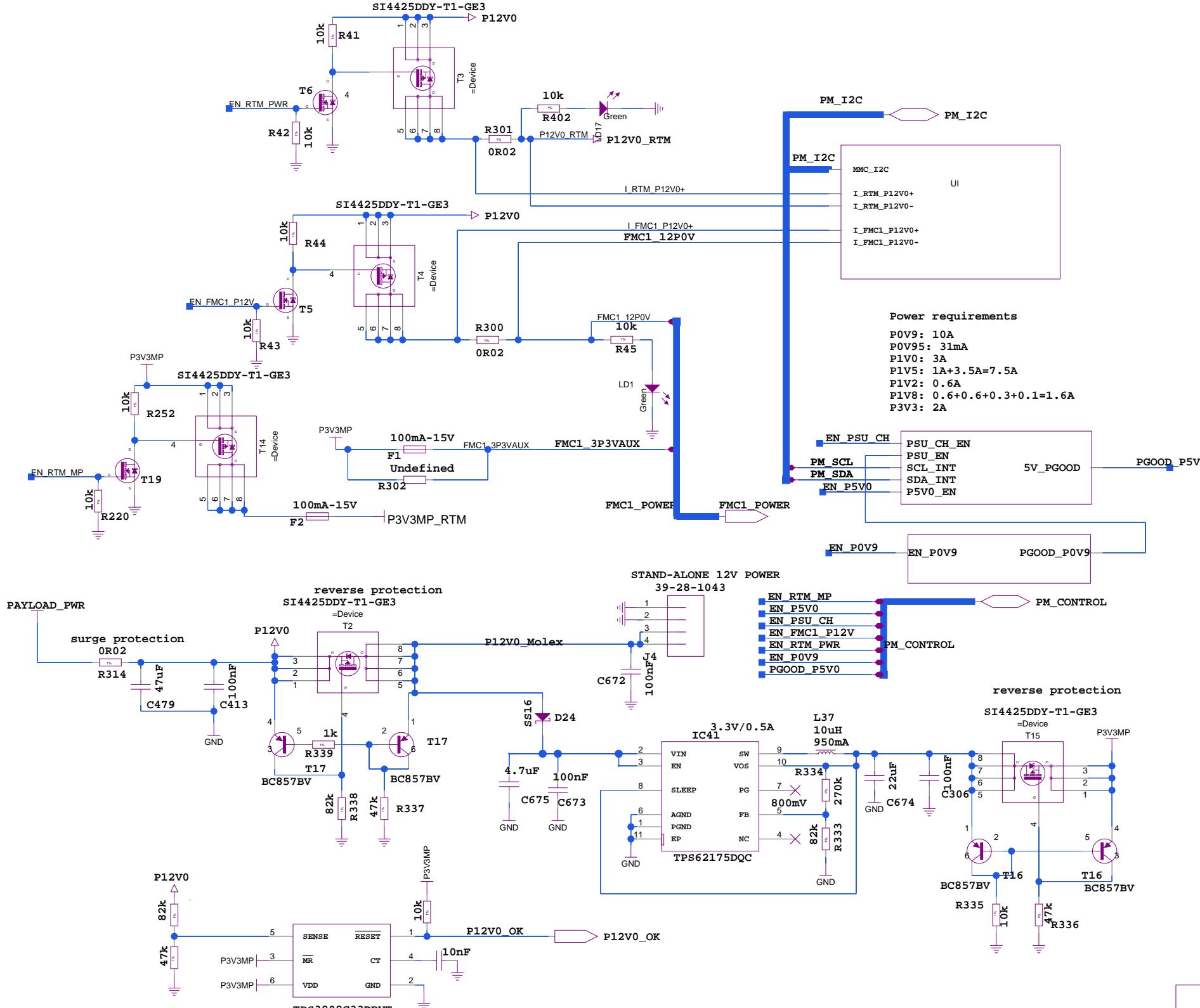
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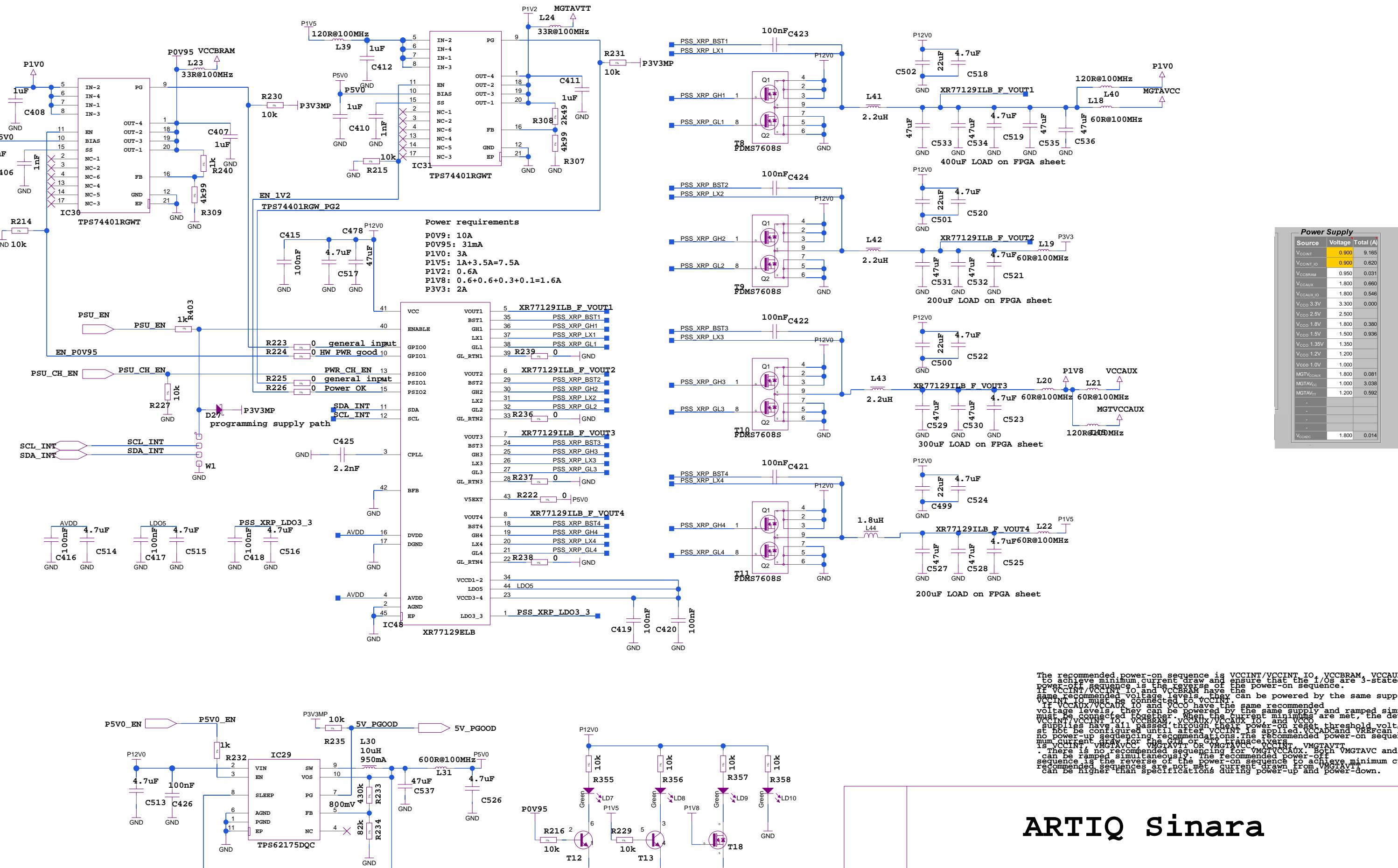


Power Supply		
Source	Voltage	Total (A)
V _{CCINT}	0.900	9.165
V _{CCINT_IO}	0.900	0.620
V _{CCBRAM}	0.950	0.031
V _{CCAUX}	1.800	0.660
V _{CCAUX_IO}	1.800	0.546
V _{CCO 3.3V}	3.300	0.000
V _{CCO 2.5V}	2.500	
V _{CCO 1.8V}	1.800	0.380
V _{CCO 1.5V}	1.500	0.936
V _{CCO 1.35V}	1.350	
V _{CCO 1.2V}	1.200	
V _{CCO 1.0V}	1.000	
MGTAV _{CCAUX}	1.800	0.081
MGTAV _{CC}	1.000	3.038
MGTAV _{TT}	1.200	0.592
-	-	
-	-	
V _{CCADC}	1.800	0.014

The recommended power-on sequence is VCCINT/VCCINT_IO, VCCBRAM, VCCAUX/VCCAUX_IO, and VCCO to achieve minimum current draw and ensure that the 1/0s are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCINT/VCCINT_IO and VCCBRAM have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. If VCCAUX/VCCAUX_IO and VCCO have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. VCCAUX and VCCO must be connected together. When the current minimums are met, the device powers on after the VCCINT/VCCINT_IO, VCCBRAM, VCCAUX/VCCAUX_IO, and VCCO supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after VCCINT is applied. VCCADC and VREF can be powered at any time and have no power-up sequencing recommendations. The recommended power-on sequence to achieve minimum current draw for the GTH or GTx transceivers is VCCINT, VMGTAVCC, VMGTAVTT, OR VMGTAVCC, VCCINT, VMGTAVTT. There is no recommended sequencing for VMGTAVCC. Both VMGTAVCC and VCCINT can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from VMGTAVTT can be higher than specifications during power-up and power-down.

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POWER_Management

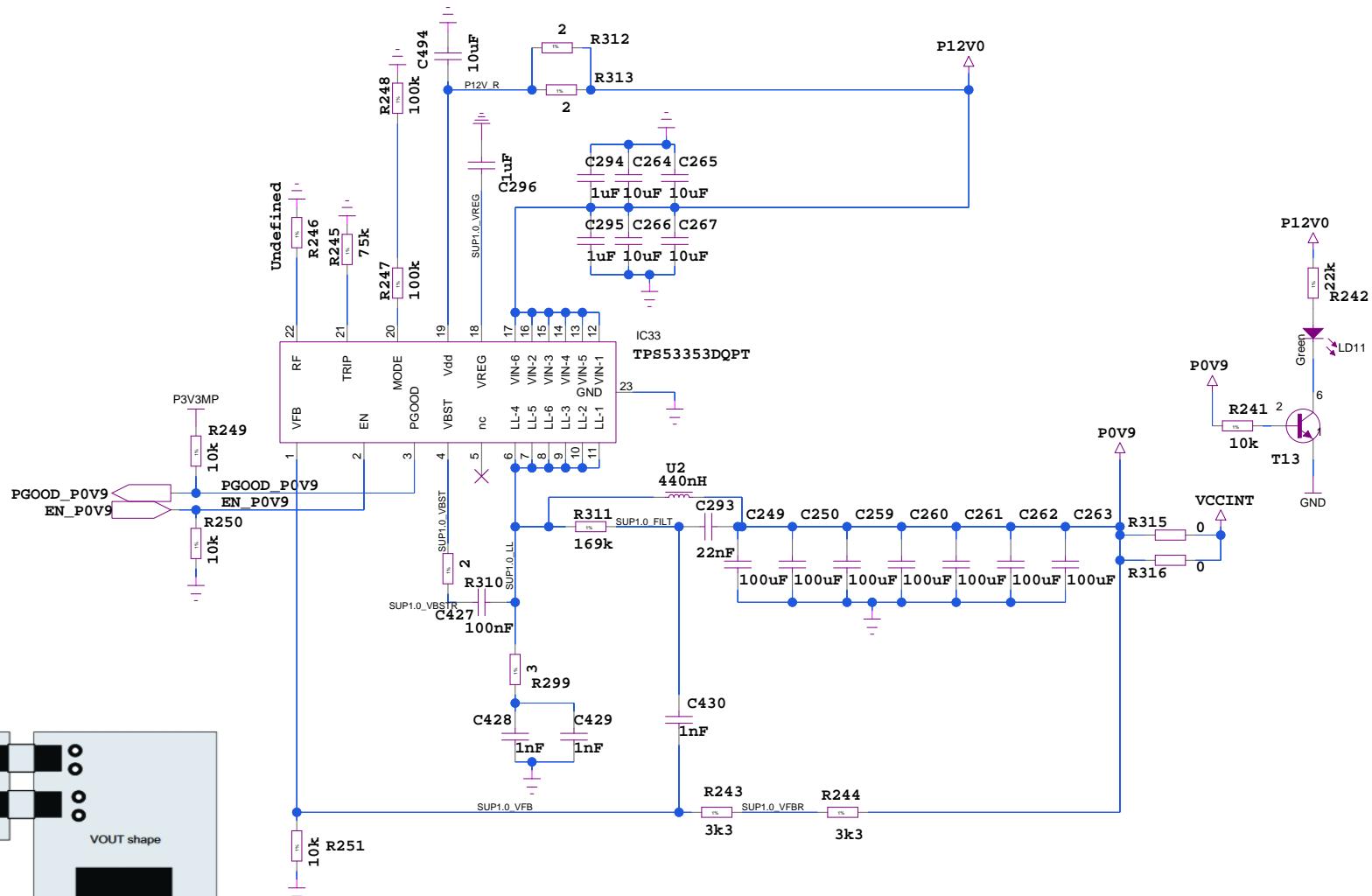
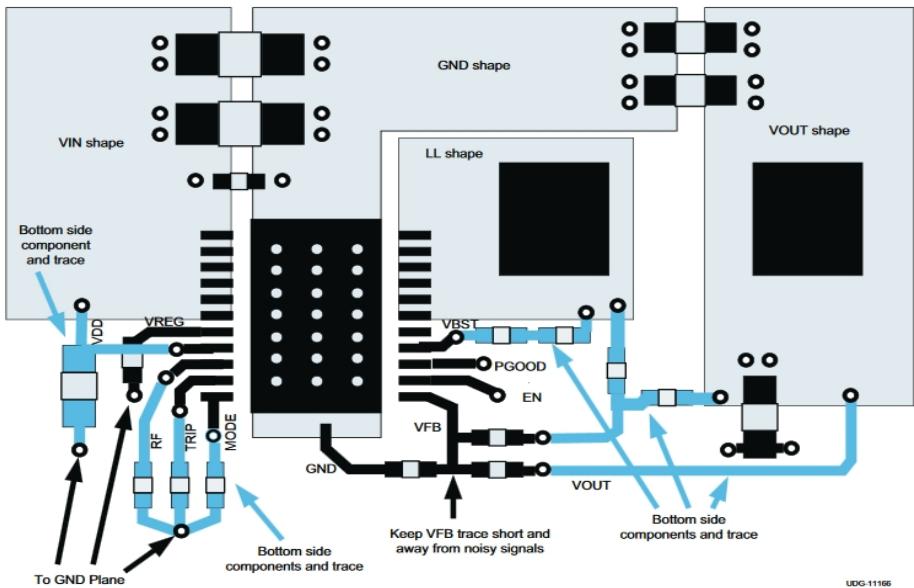


The recommended power-on sequence is VCCINT/VCCINT IO, VCCBRAM, VCCAUX/VCCAUX IO, and VCCREF. The recommended power-down sequence is the reverse of the power-on sequence. Both VMGTAUC and VCCINT have the same recommended voltage levels which can be powered by the same supply and VCCINTIO must be connected to VCCINT. VCCAUXIO and VCCIO have the same recommended voltage levels which can be powered by the same supply and ramped simultaneously. When the current minimums are met, the device must be connected to VCCBRAM, VCCAUX/VCCAUX IO, and VCCIO. The recommended sequencing for VMGTAUC and VCCINT is not required until after VCCINT is applied. VCCREF can be powered without sequencing recommendations. The recommended power-on sequence for VMGTAUC transceivers is VMGTAUC, VCCAUX, VMGTAUT, VMGTAVT. There is no recommended sequencing for VMGTAUC. Both VMGTAUC and VCCINT can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. Recommended sequencing for minimum power-down draw is VMGTAUC, VCCAUX, VMGTAUT, VMGTAVT.

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PWR DC DC EXAR

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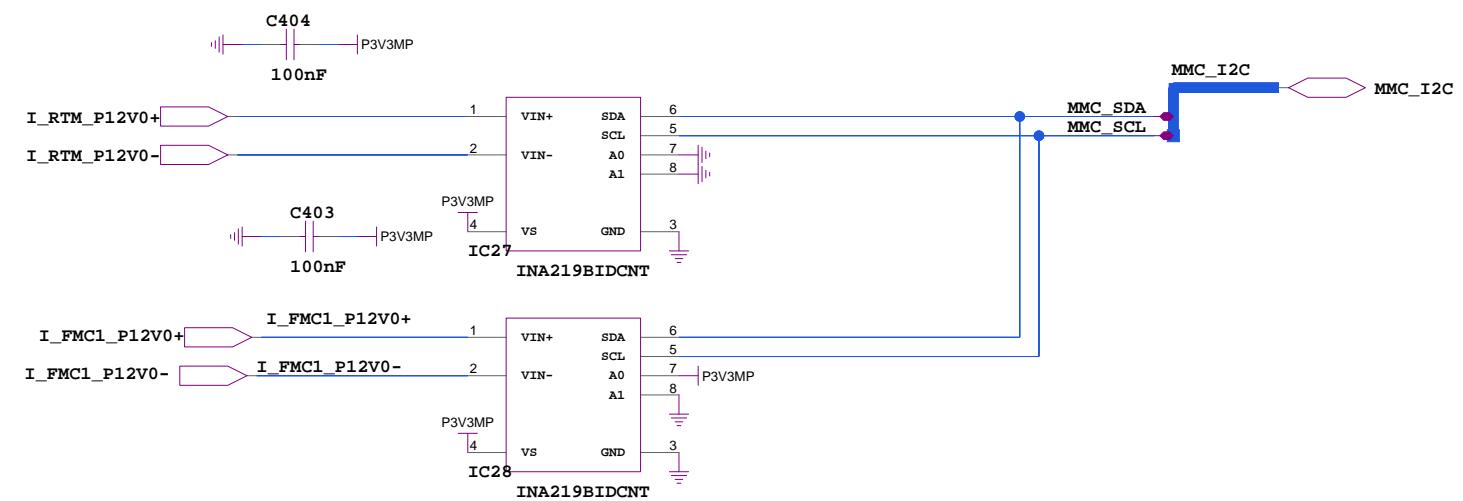
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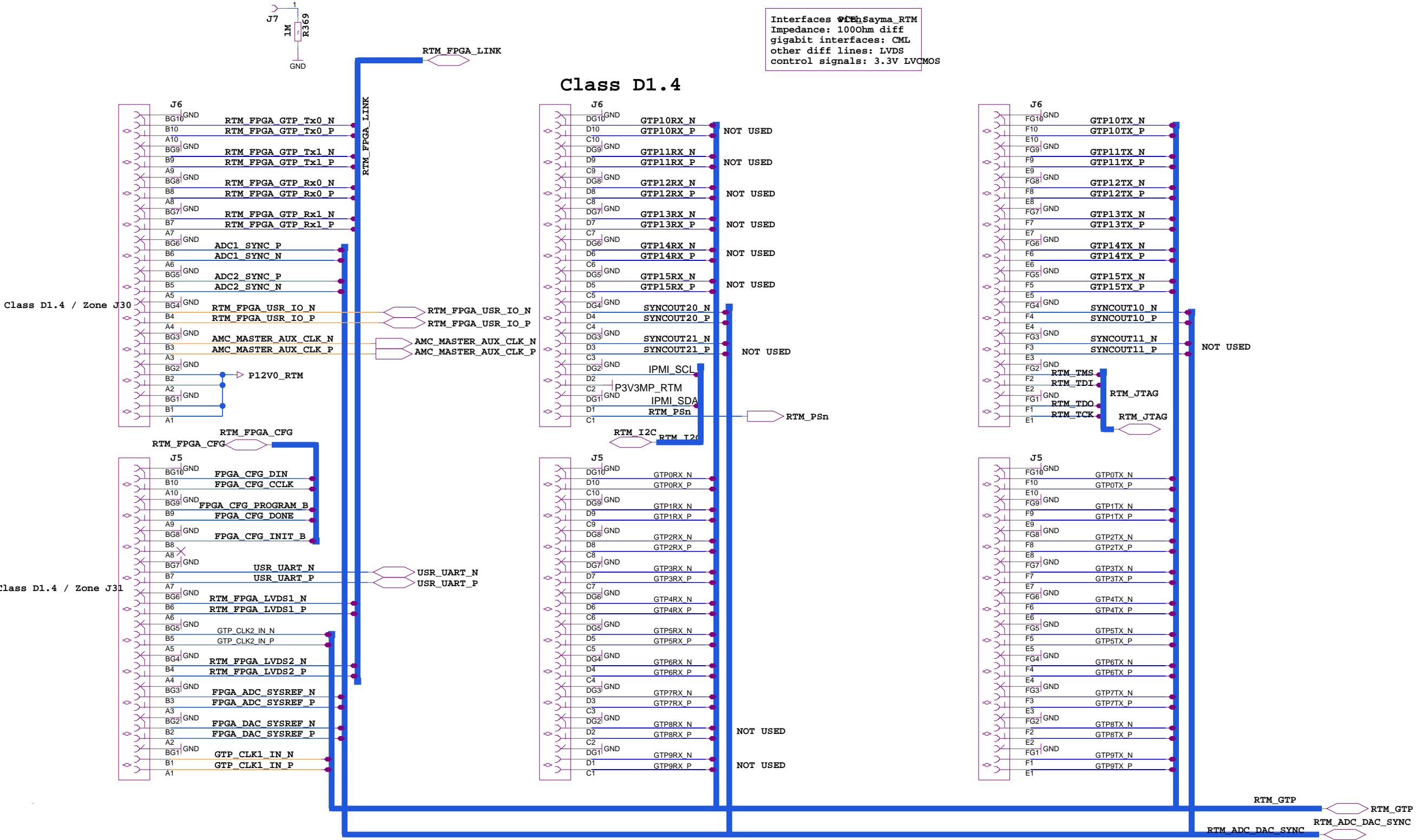
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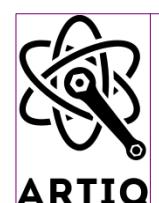
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UI_mon

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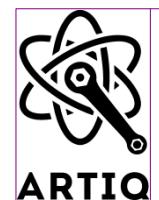
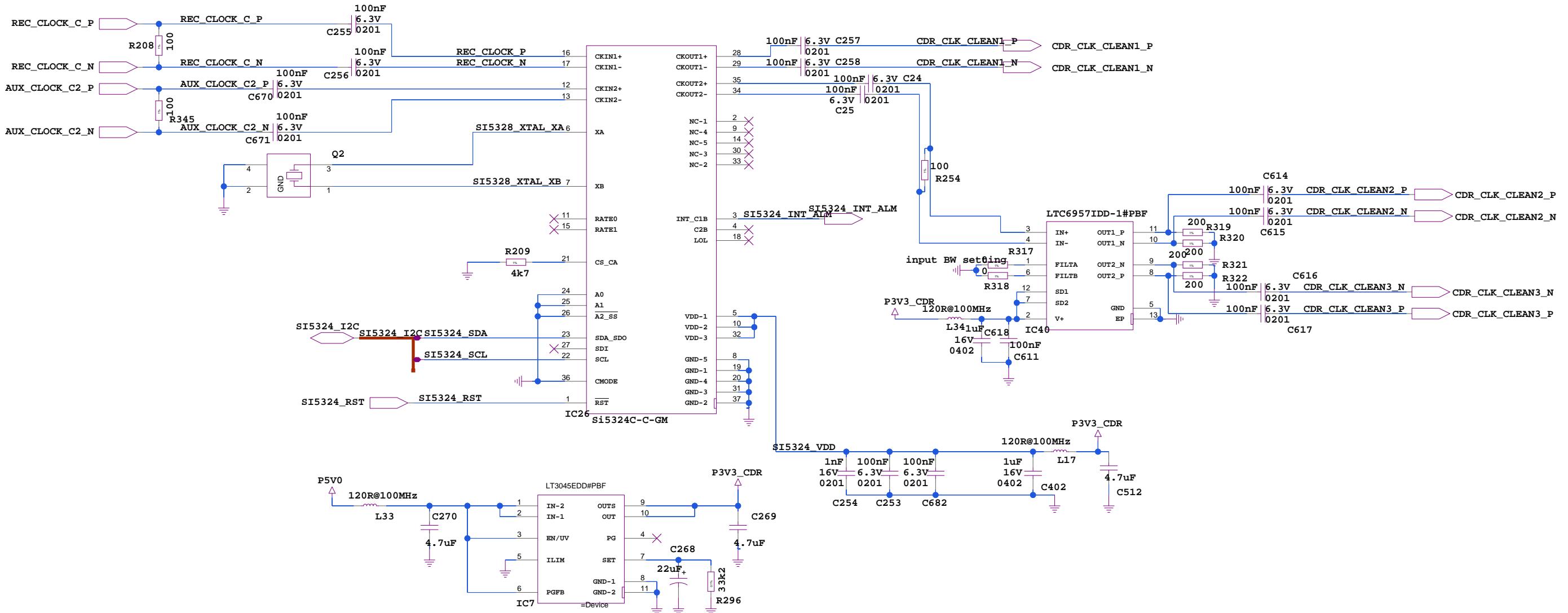
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MTCA.4 management	1 PWR A1	PWR B1	PS#	SDA	TCK	TDO
Digital clocks fixed IO	2 PWR A2	PWR B2	MP	SCL	TDI	TMS
	3 AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
	4 AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
Standard Gbit-Links	5 P30_IO+ / CC*	P30_IO+ / CC*	GTP15_RX+	GTP15_RX+	GTP15_TX+	GTP15_TX-
	6 P30_IO+ / CC*	P30_IO+ / CC*	GTP14_RX+	GTP14_RX+	GTP14_TX+	GTP14_TX-
	7 GTP12-15_CLK_IN+	GTP12-15_CLK_IN+	GTP12_RX+	GTP12_RX+	GTP13_RX+	GTP13_TX-
	8 GTP12-15_CLK_OUT+	GTP12-15_CLK_OUT+	GTP12_RX+	GTP12_RX+	GTP12_TX+	GTP12_TX-
	9 P30_IO+ / CC*	P30_IO+ / CC*	GTP11_RX+	GTP11_RX+	GTP11_TX+	GTP11_TX-
	10 P30_IO+ / CC*	P30_IO+ / CC*	GTP10_RX+	GTP10_RX+	GTP10_TX+	GTP10_TX-
Standard Gbit-Links	1 GTP8-11_CLK_IN+	GTP8-11_CLK_IN-	GTP9_RX+	GTP9_RX-	GTP9_TX+	GTP9_TX-
	2 GTP8-11_CLK_OUT+	GTP8-11_CLK_OUT-	GTP8_RX+	GTP8_RX-	GTP8_TX+	GTP8_TX-
	3 P31_IO+ / CC	P31_IO+ / CC	GTP7_RX+	GTP7_RX-	GTP7_TX+	GTP7_TX-
	4 P31_IO+ / CC	P31_IO+ / CC	GTP8_RX+	GTP8_RX-	GTP6_TX+	GTP6_TX-
	5 GTP4-7_CLK_IN+	GTP4-7_CLK_IN+	GTP5_RX+	GTP5_RX-	GTP5_TX+	GTP5_TX-
	6 GTP4-7_CLK_OUT+	GTP4-7_CLK_OUT+	GTP4_RX+	GTP4_RX-	GTP4_TX+	GTP4_TX-
	7 P31_IO+ / CC*	P31_IO+ / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
	8 P31_IO+ / CC*	P31_IO+ / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
	9 GTP0-3_CLK_IN+	GTP0-3_CLK_IN+	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
	10 GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT+	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-



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RTM_CON

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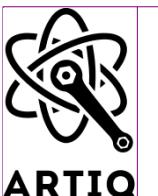
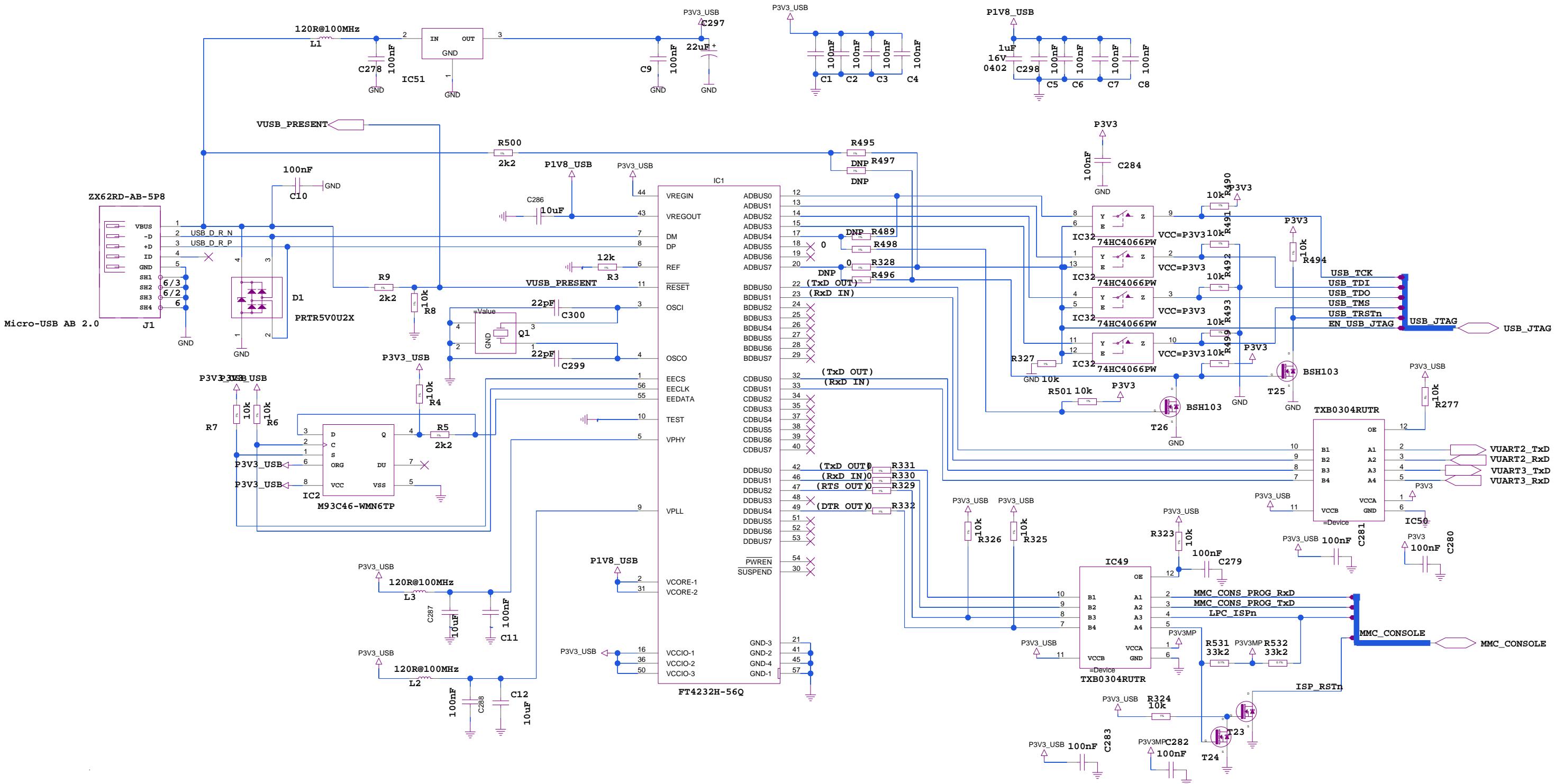


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SI5324_CLK_RECOVERY

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G.K.	30	31



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USB_SERIAL_QUAD

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