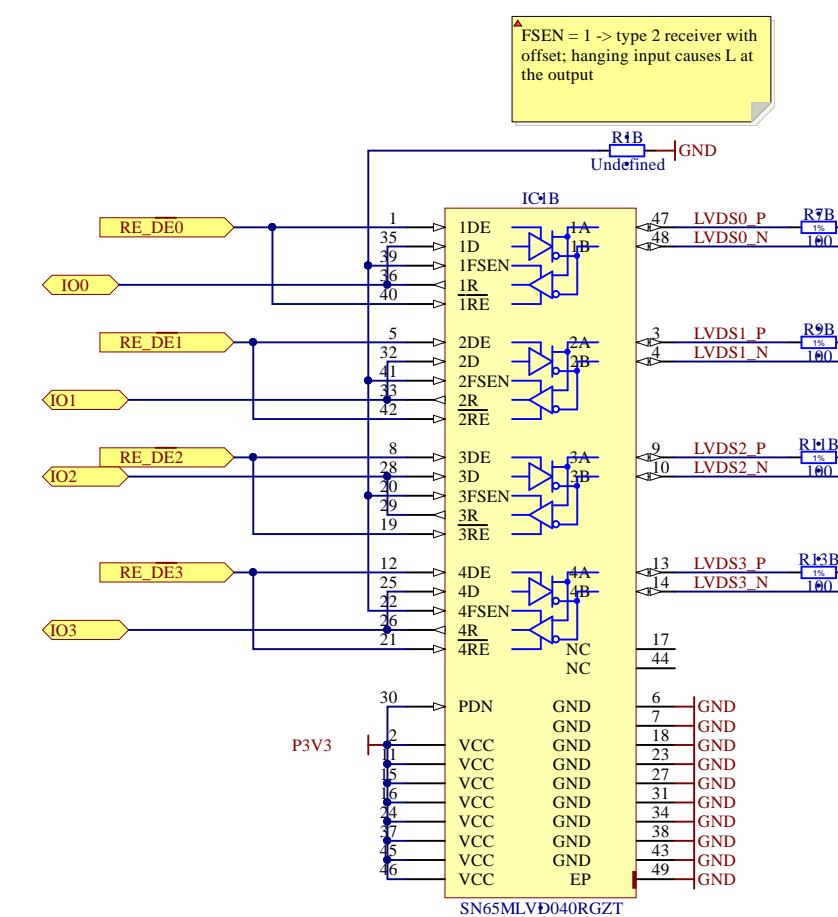


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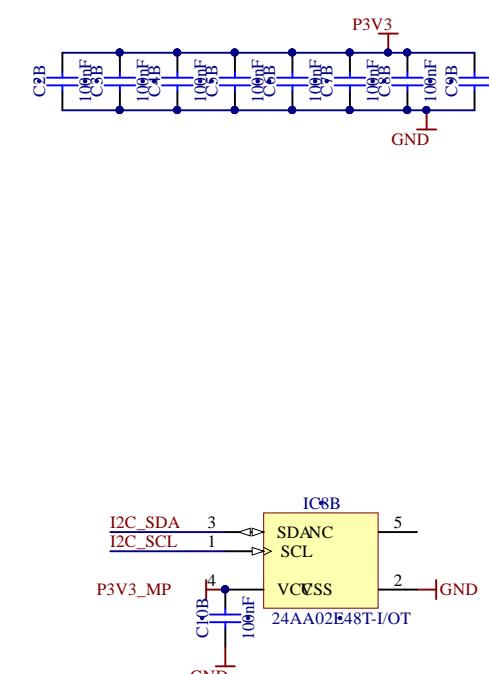
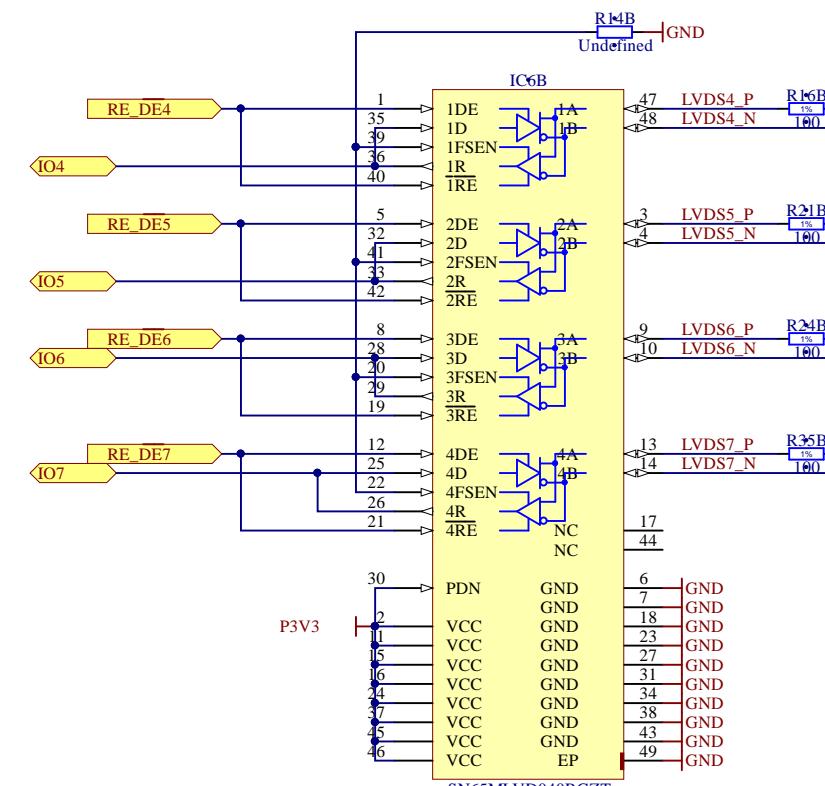
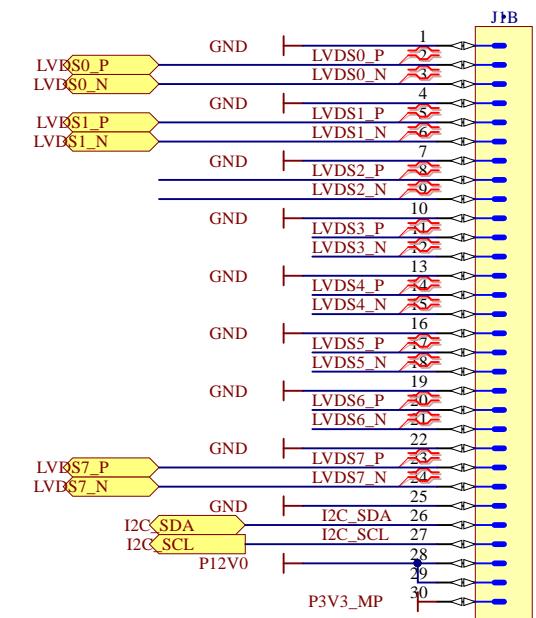
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ARTIQ



This module connects to Kasli or to VHDCI Metlino breakout board
All signals are LVDS, in case of Metlino VCC is 1.8V
I2C is 3.3V LVC MOS
P3V3_MP can handle up to 20mA
P12V0 current is up to 1A



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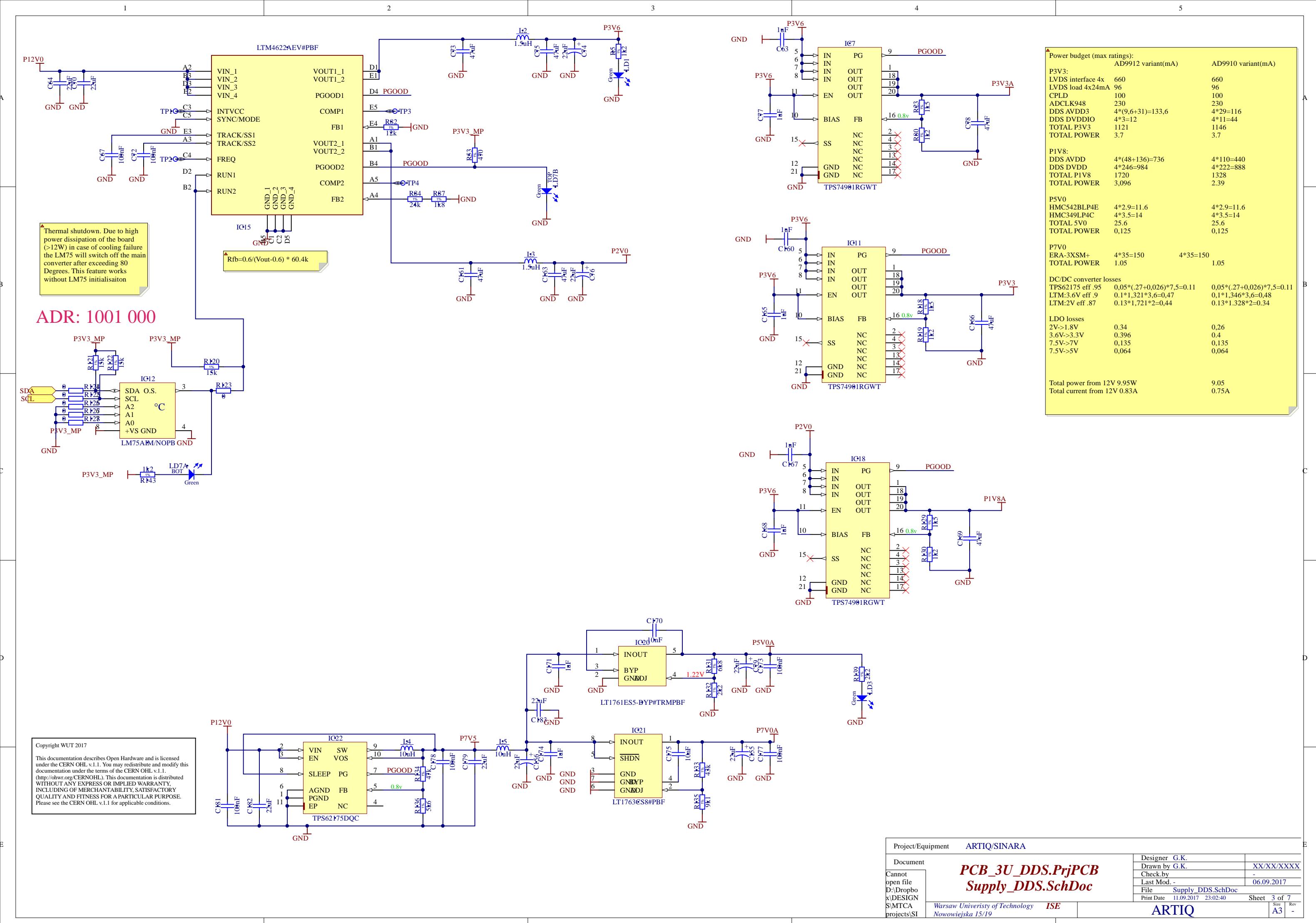
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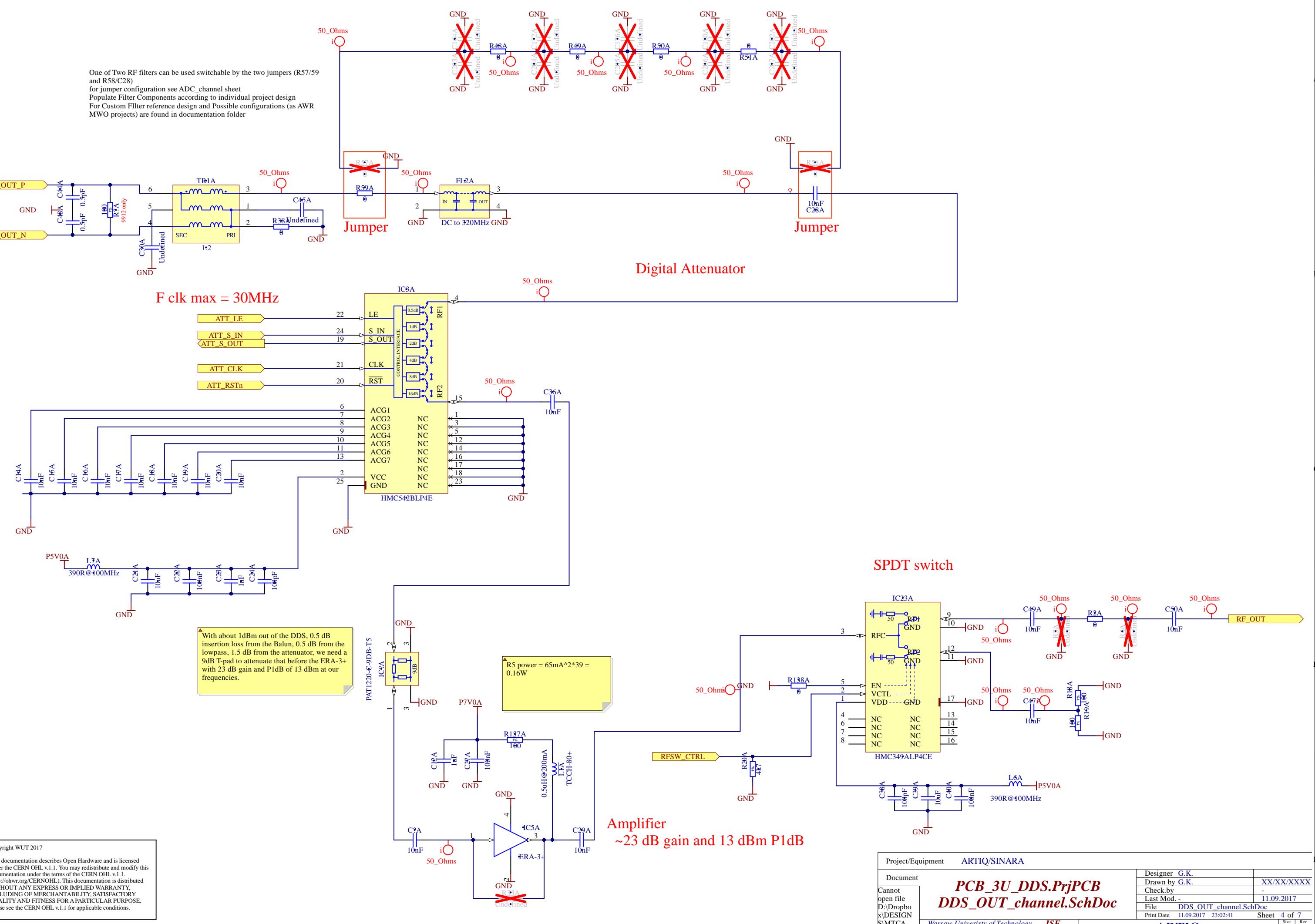
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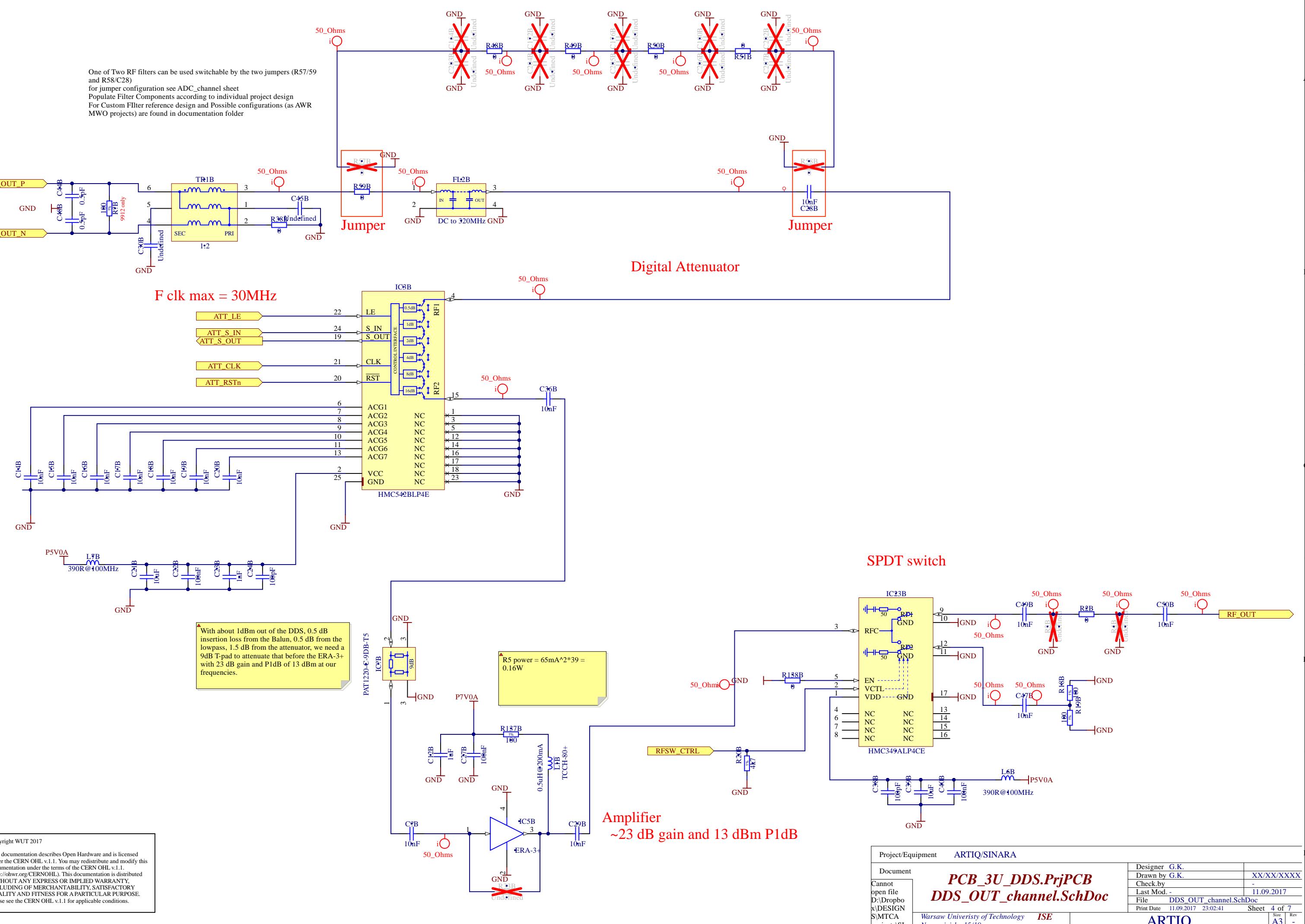
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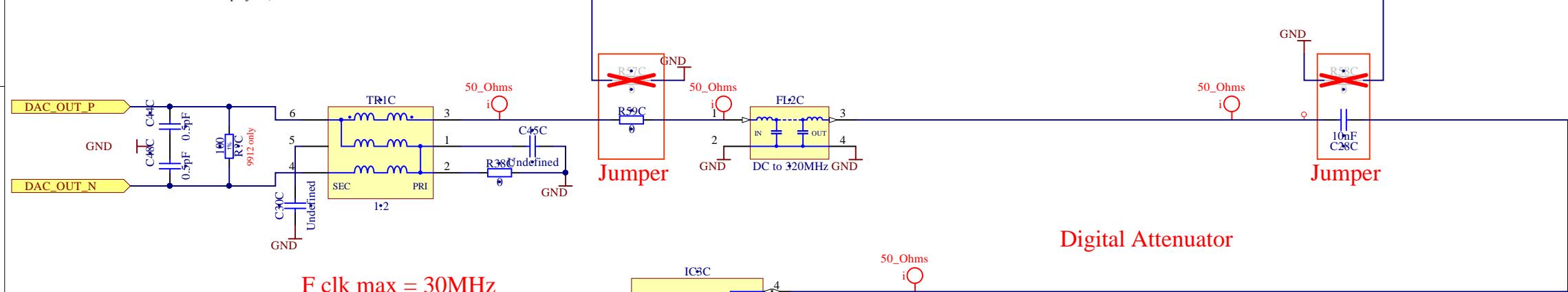




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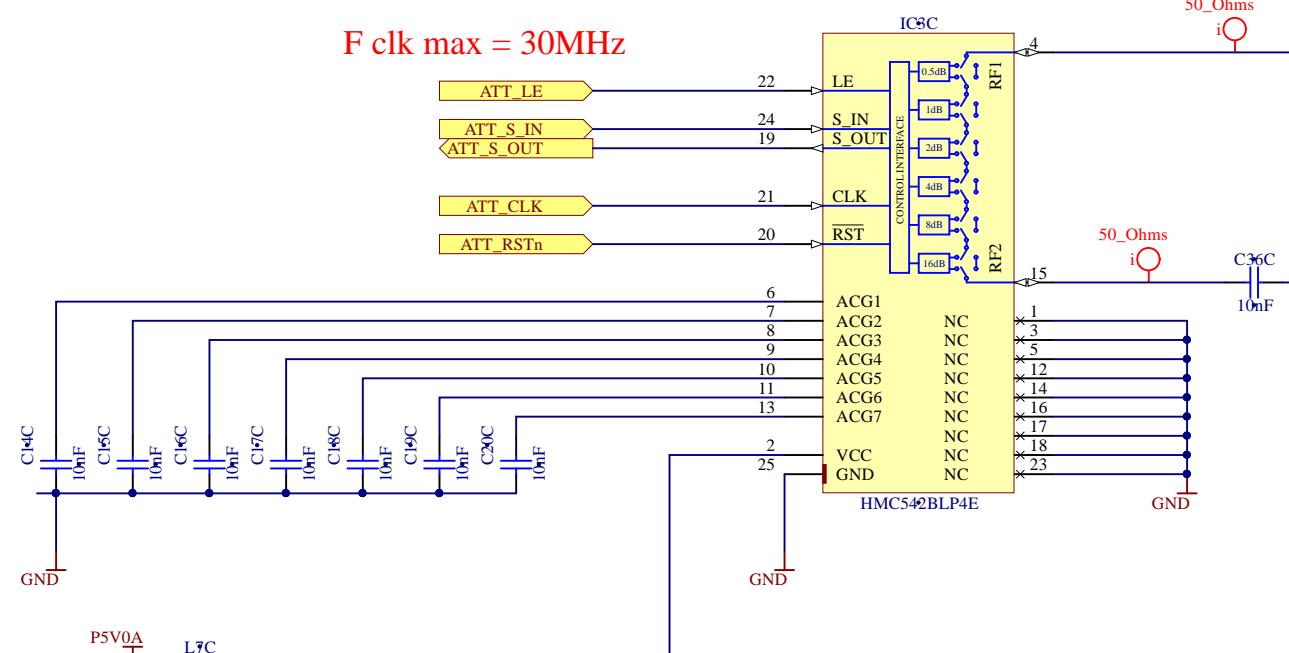
A A

One of Two RF filters can be used switchable by the two jumpers (R57/59 and R58/C28)
for jumper configuration see ADC_channel sheet
Populate Filter Components according to individual project design
For Custom Filter reference design and Possible configurations (as AWR MWO projects) are found in documentation folder

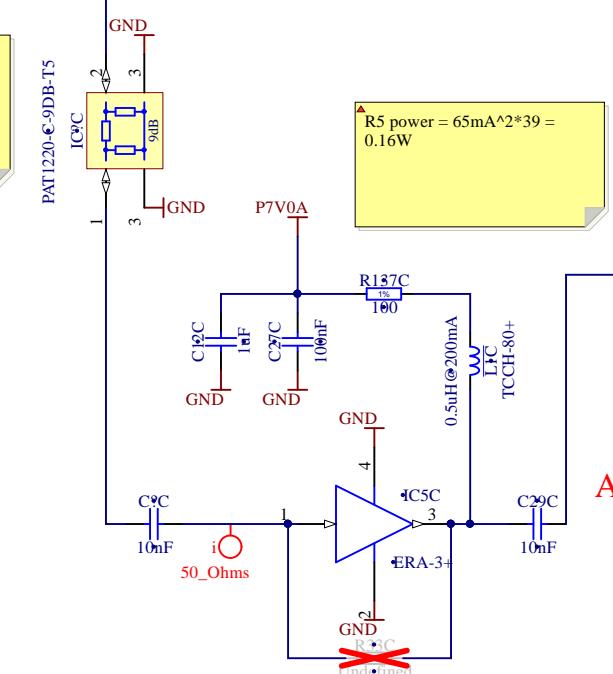


Digital Attenuator

F clk max = 30MHz

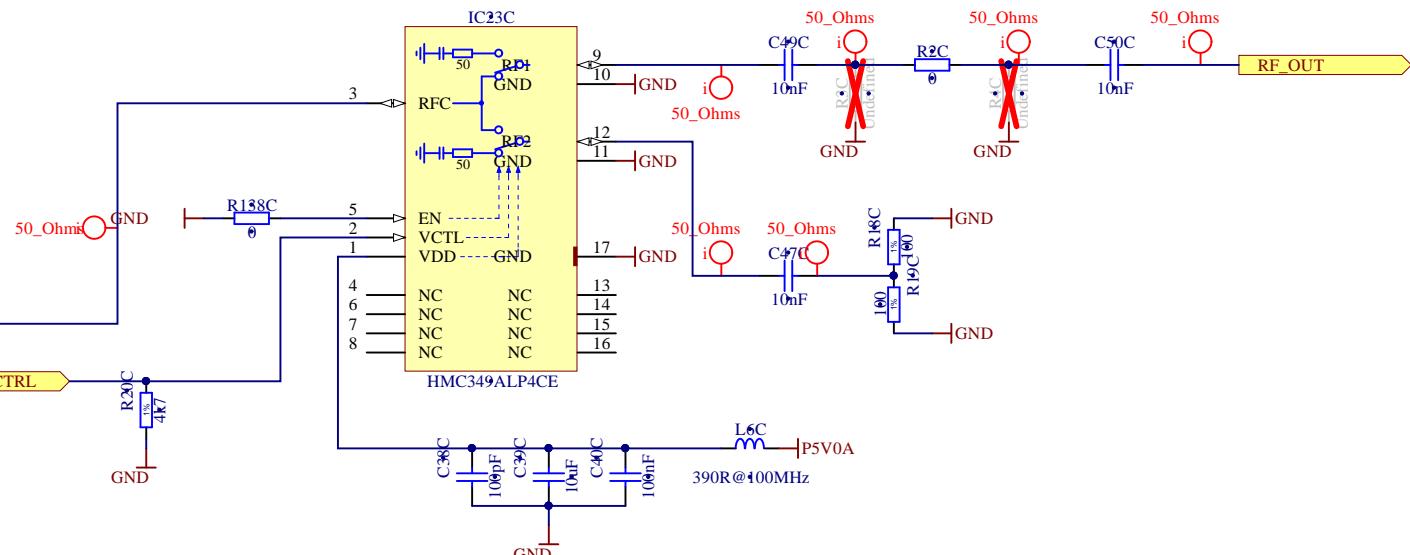


With about 1dBm out of the DDS, 0.5 dB insertion loss from the Balun, 0.5 dB from the lowpass, 1.5 dB from the attenuator, we need a 9dB T-pad to attenuate that before the ERA-3+ with 23 dB gain and P1dB of 13 dBm at our frequencies.



Amplifier
~23 dB gain and 13 dBm P1dB

SPDT switch



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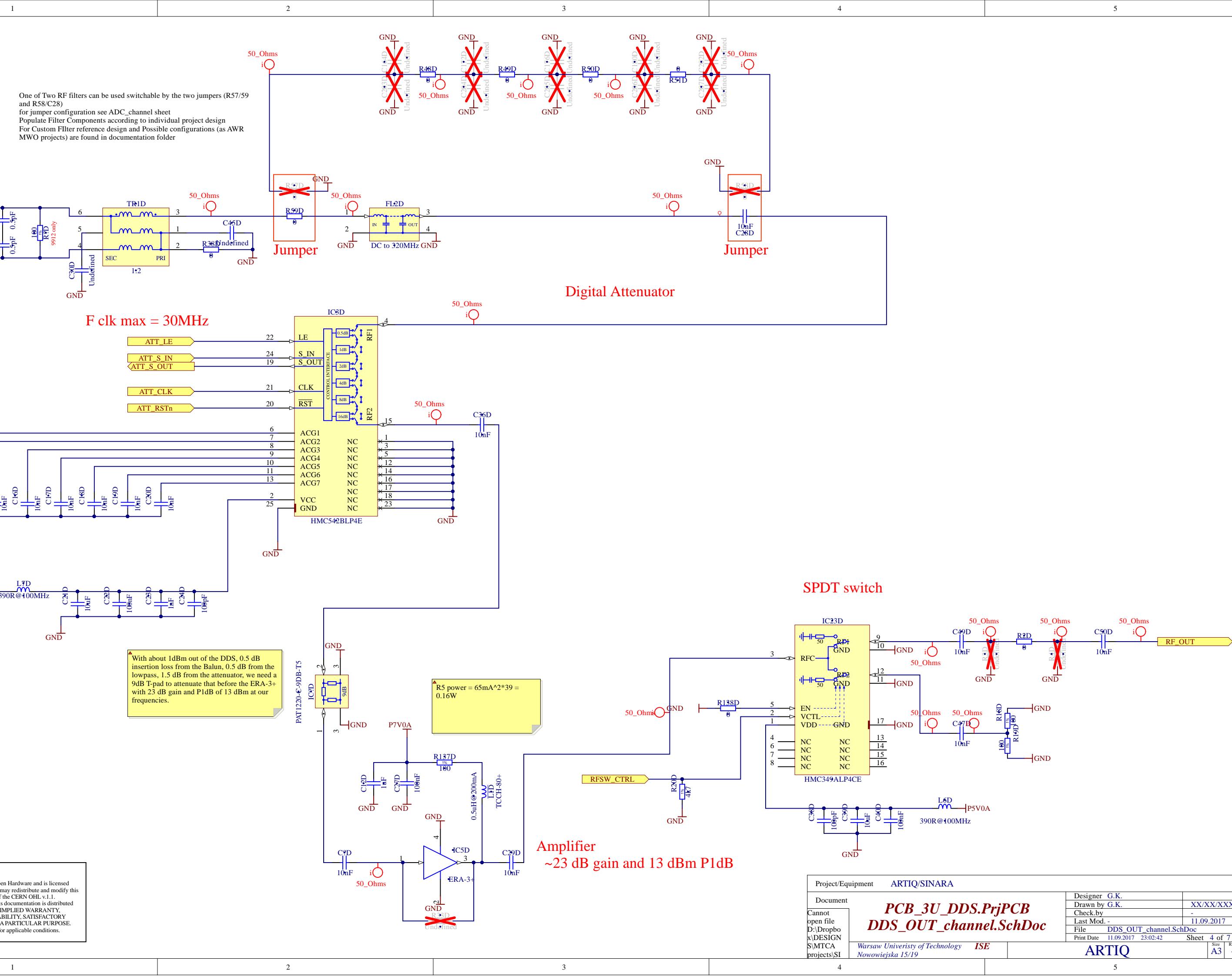
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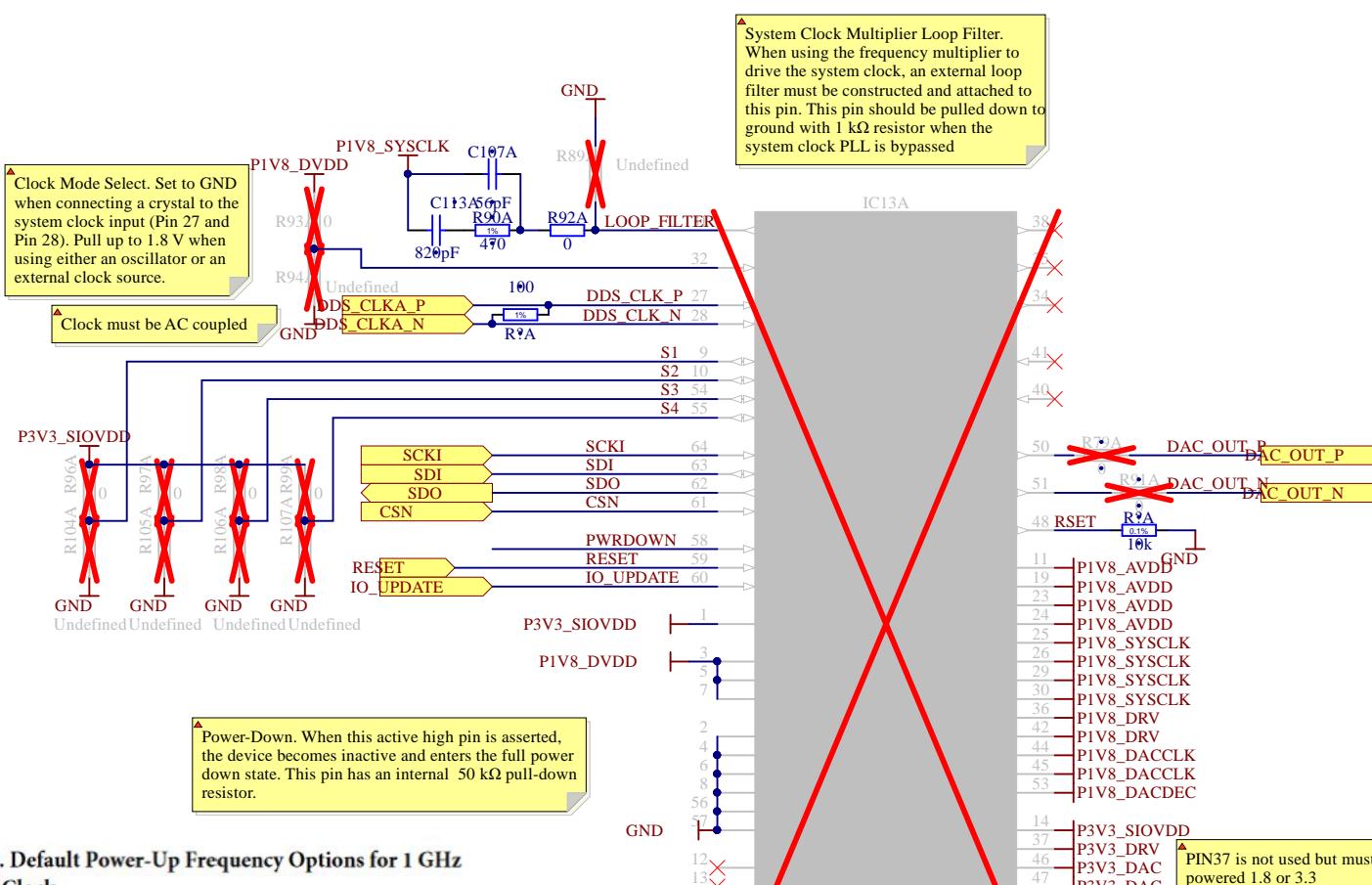
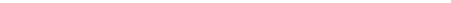
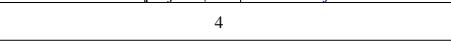
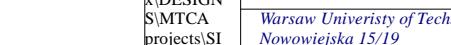
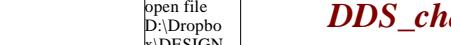
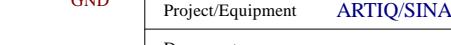
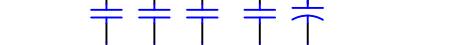
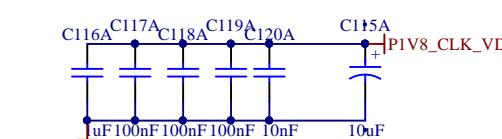
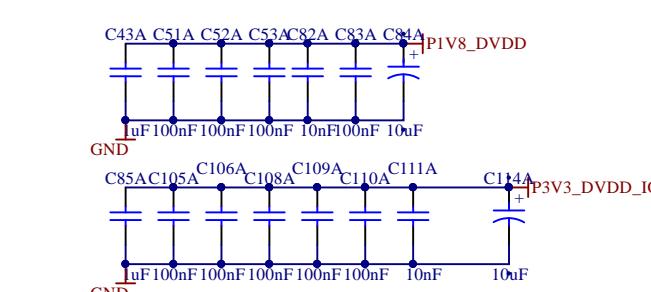
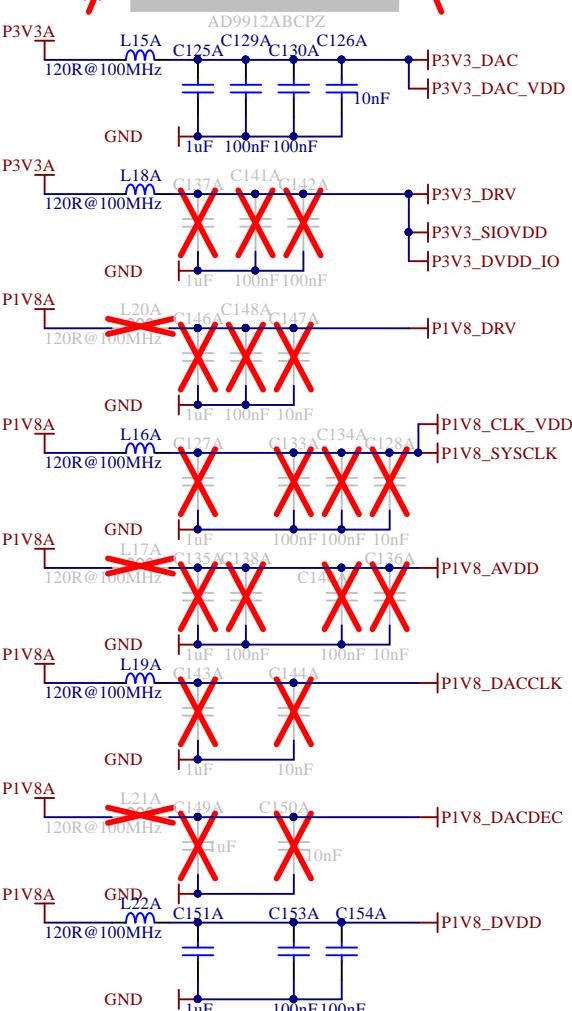
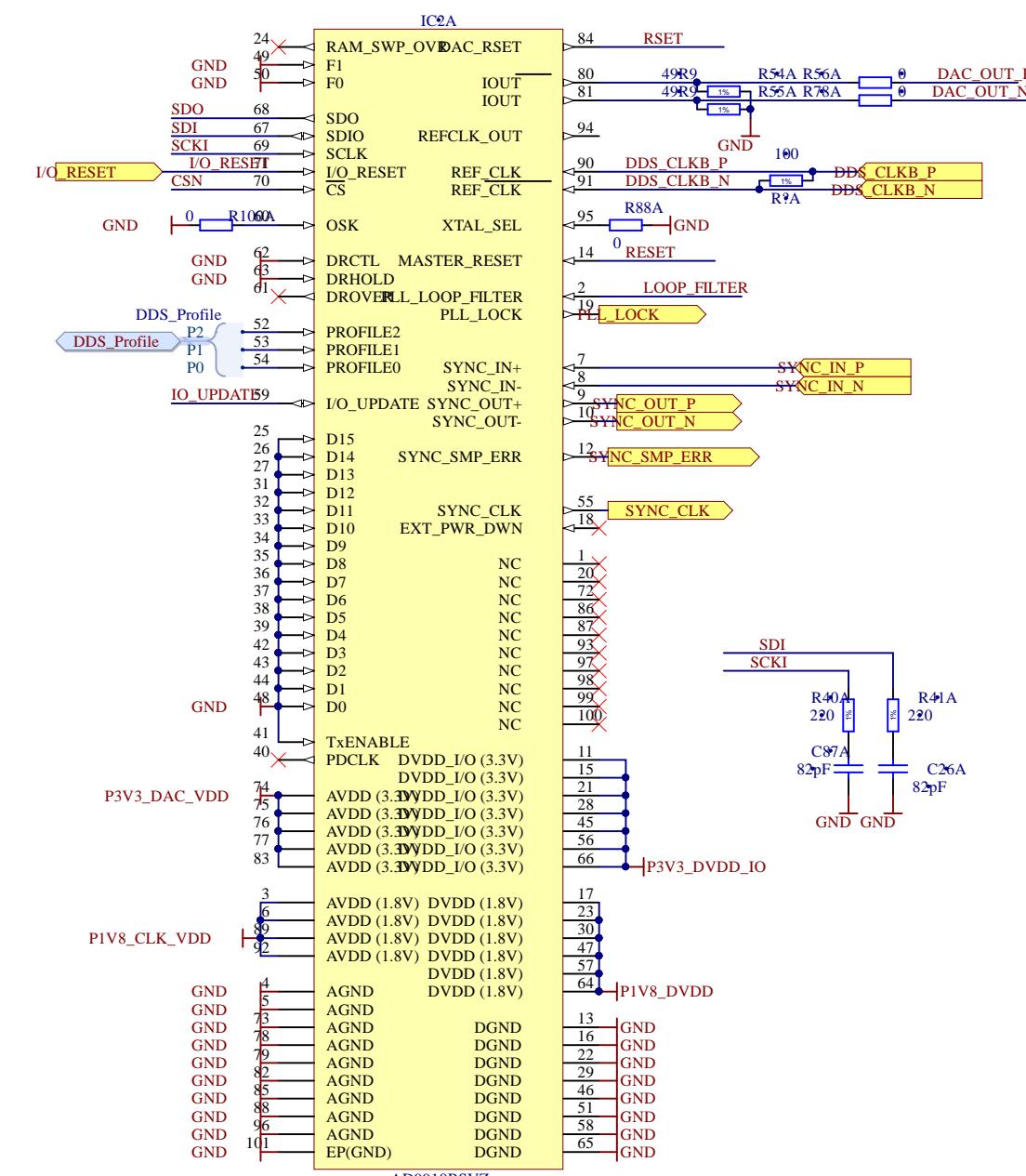


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal/PLL	38.87939
0	0	1	0	Xtal/PLL	51.83411
0	0	1	1	Xtal/PLL	61.43188
0	1	0	0	Xtal/PLL	77.5879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.5879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

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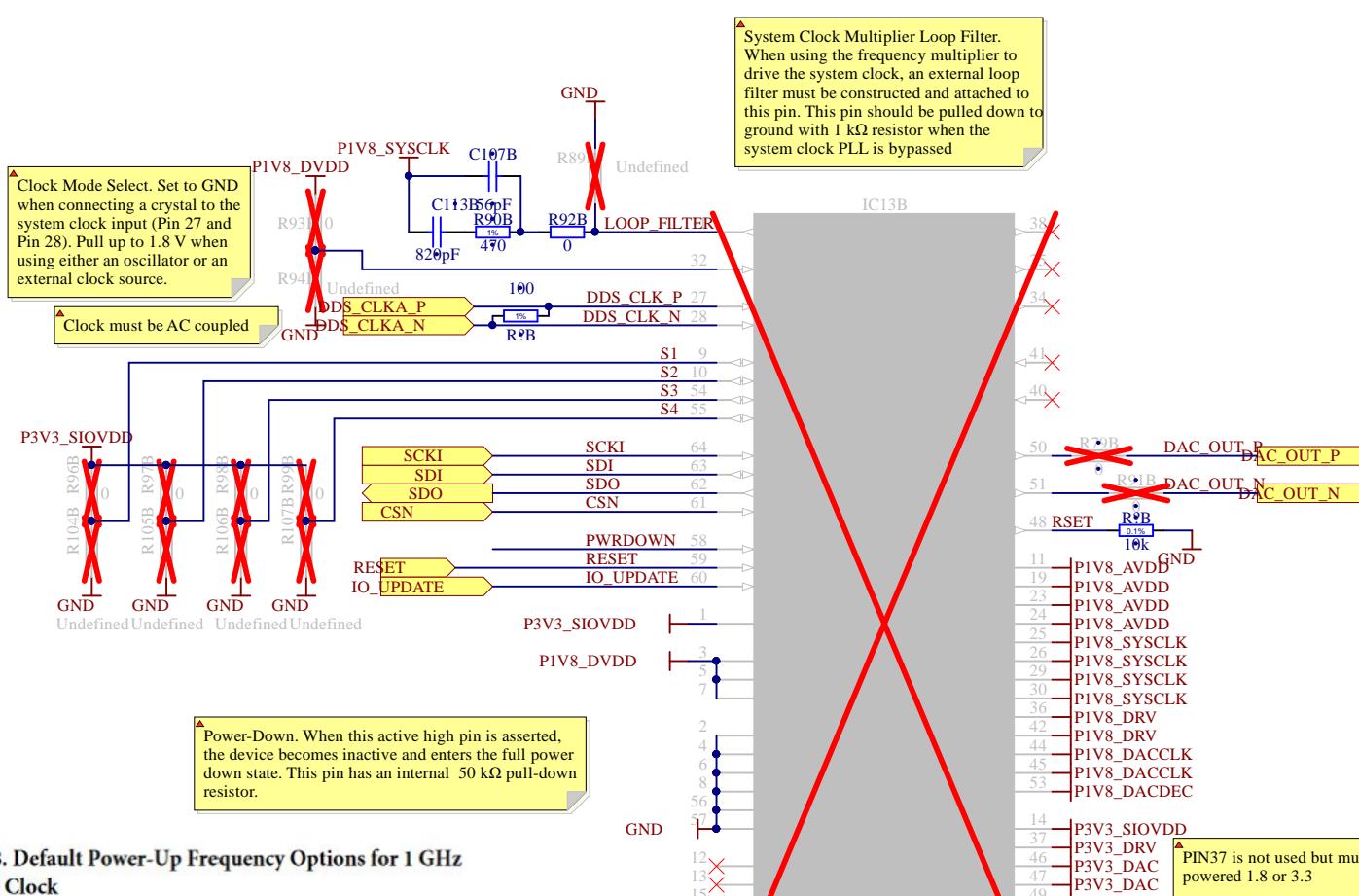
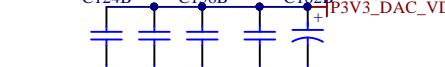
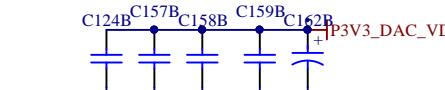
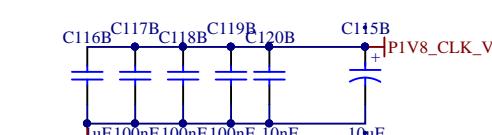
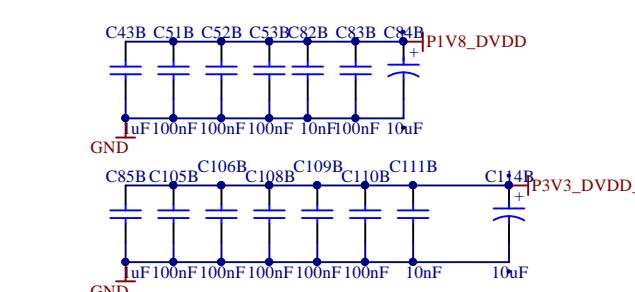
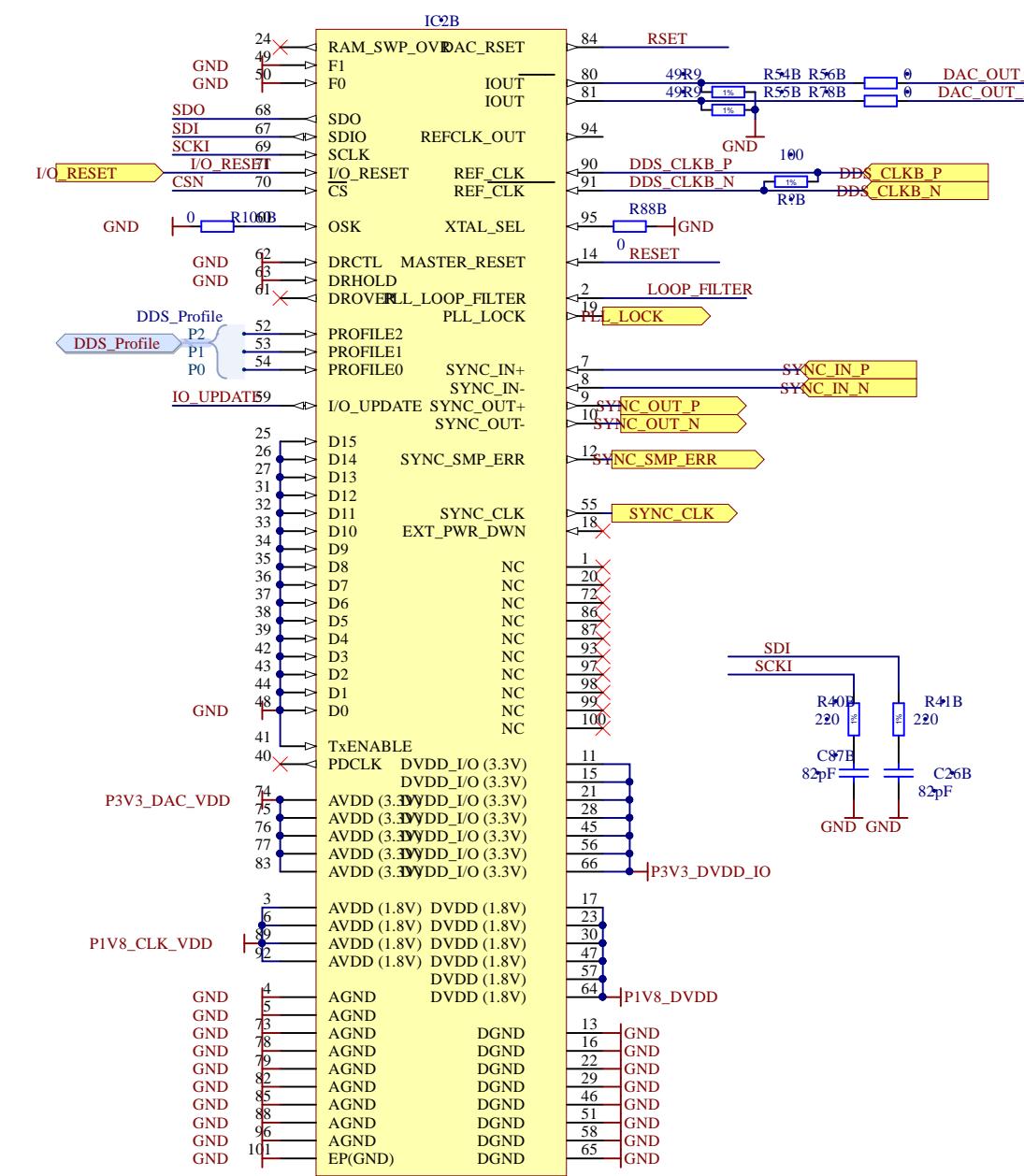
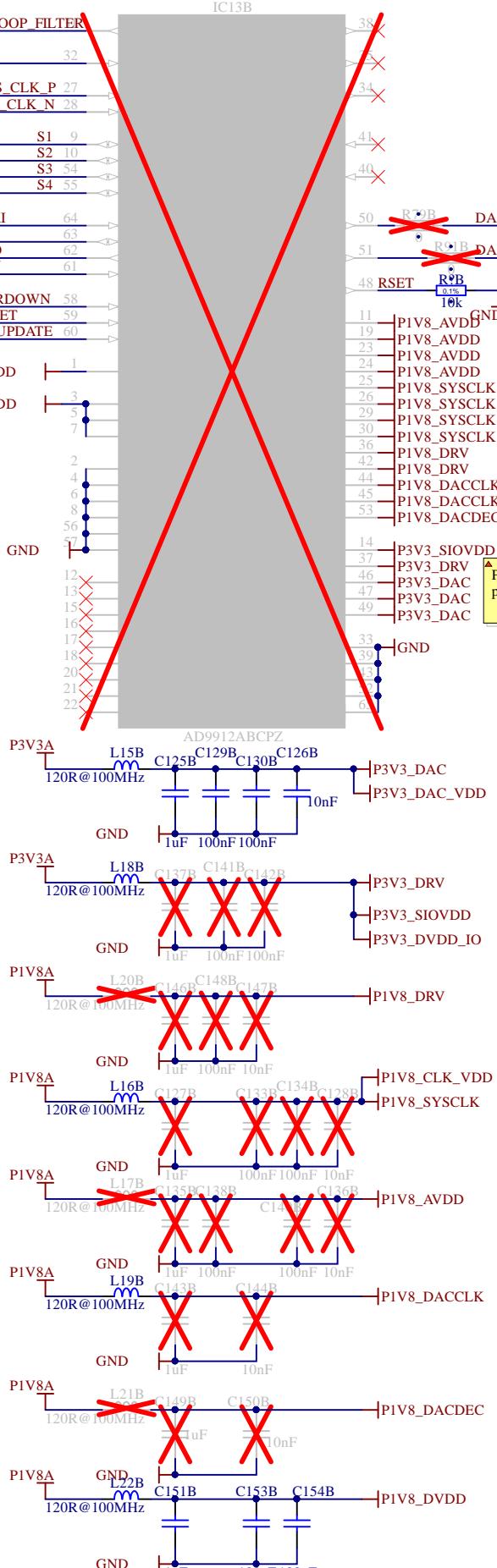


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
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0	1	0	0	Xtal/PLL	77.75879
0	1	0	1	Xtal/PLL	92.14783
0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758



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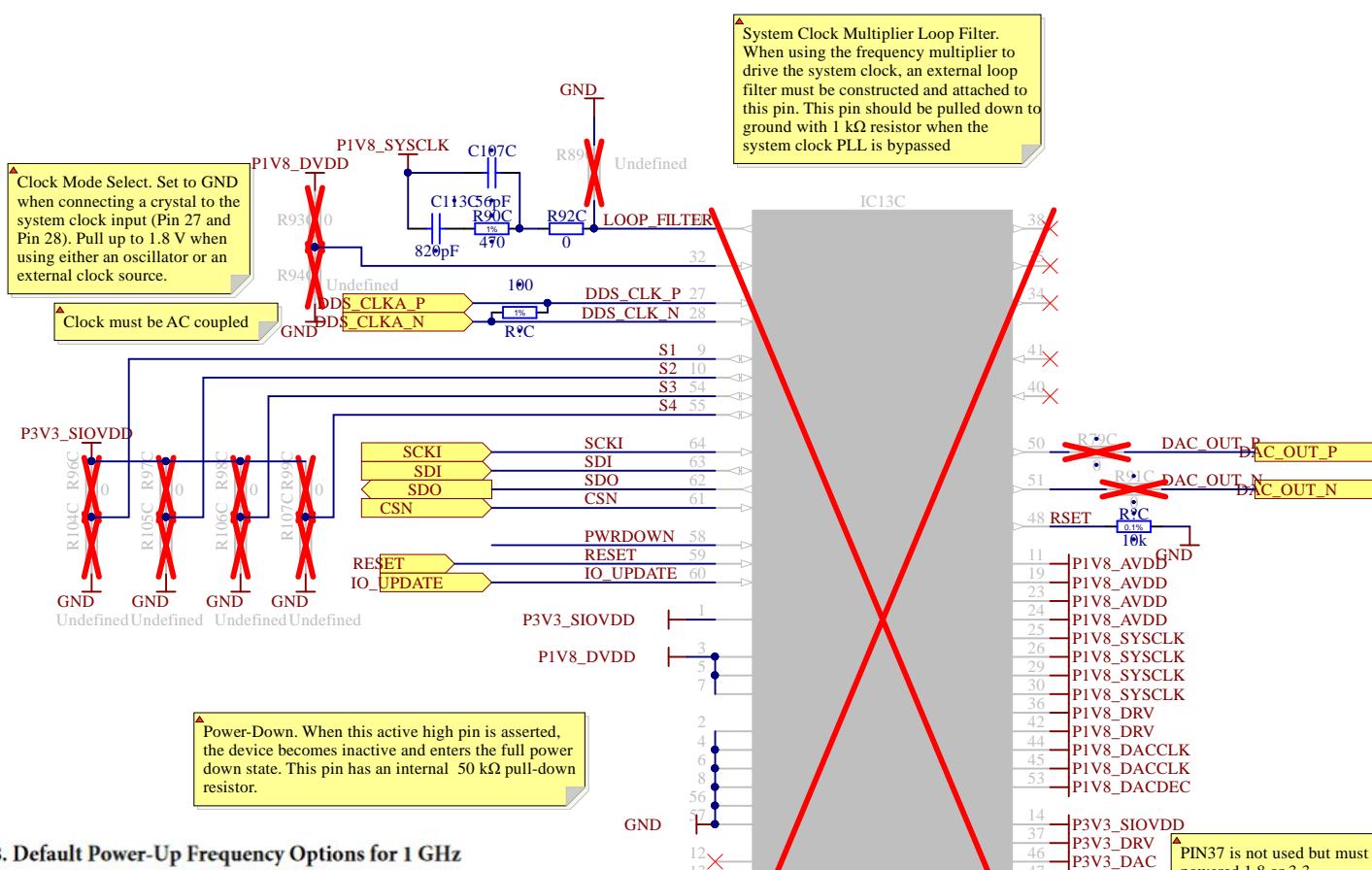
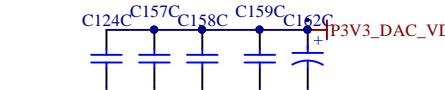
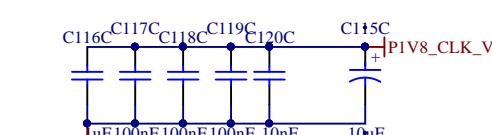
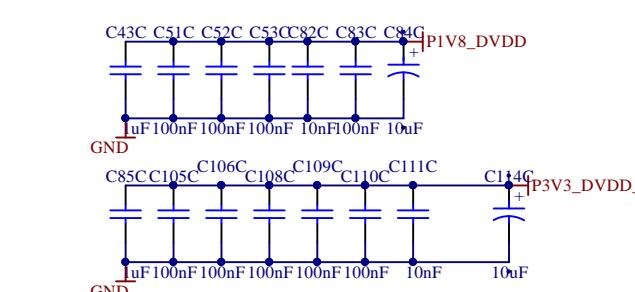
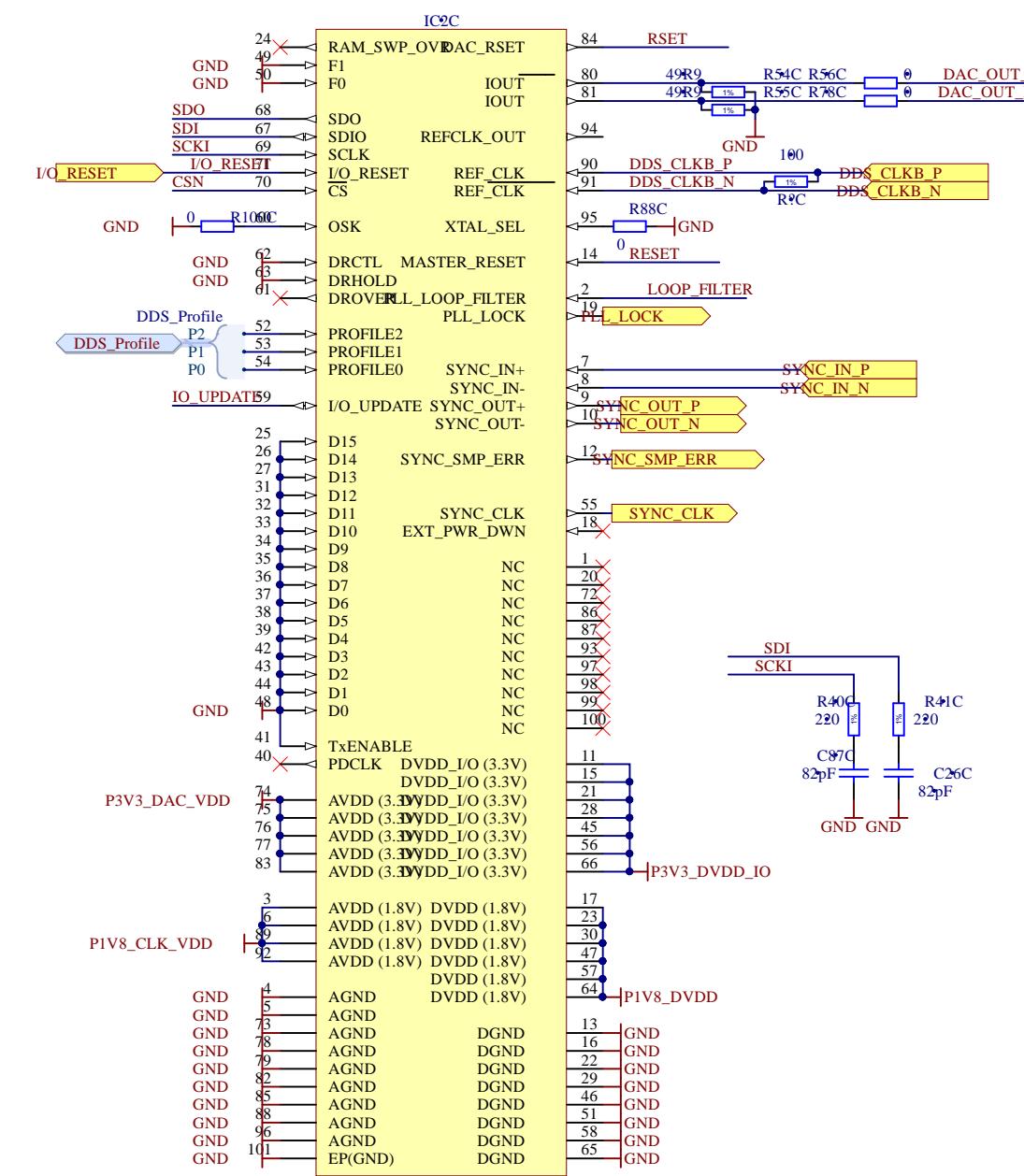
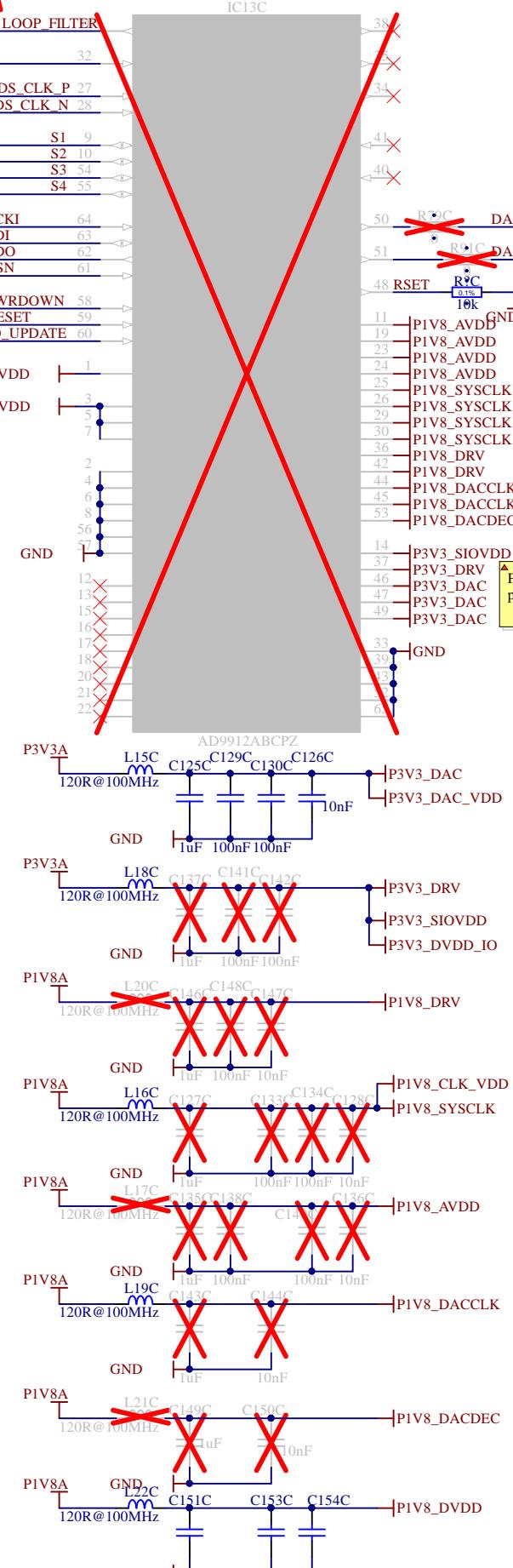


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
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0	1	0	0	Xtal/PLL	77.75879
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0	1	1	0	Xtal/PLL	122.87903
0	1	1	1	Xtal/PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758



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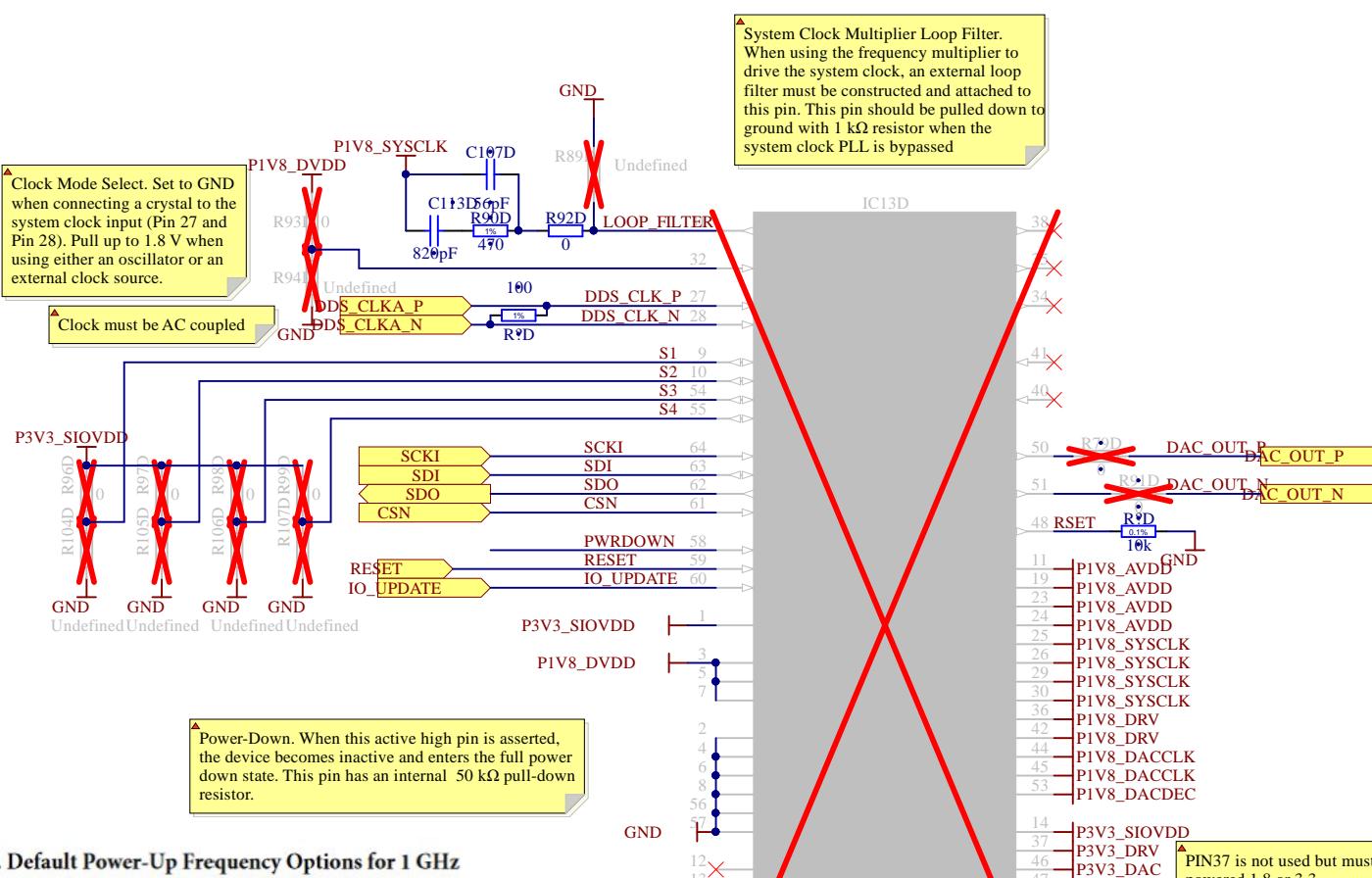
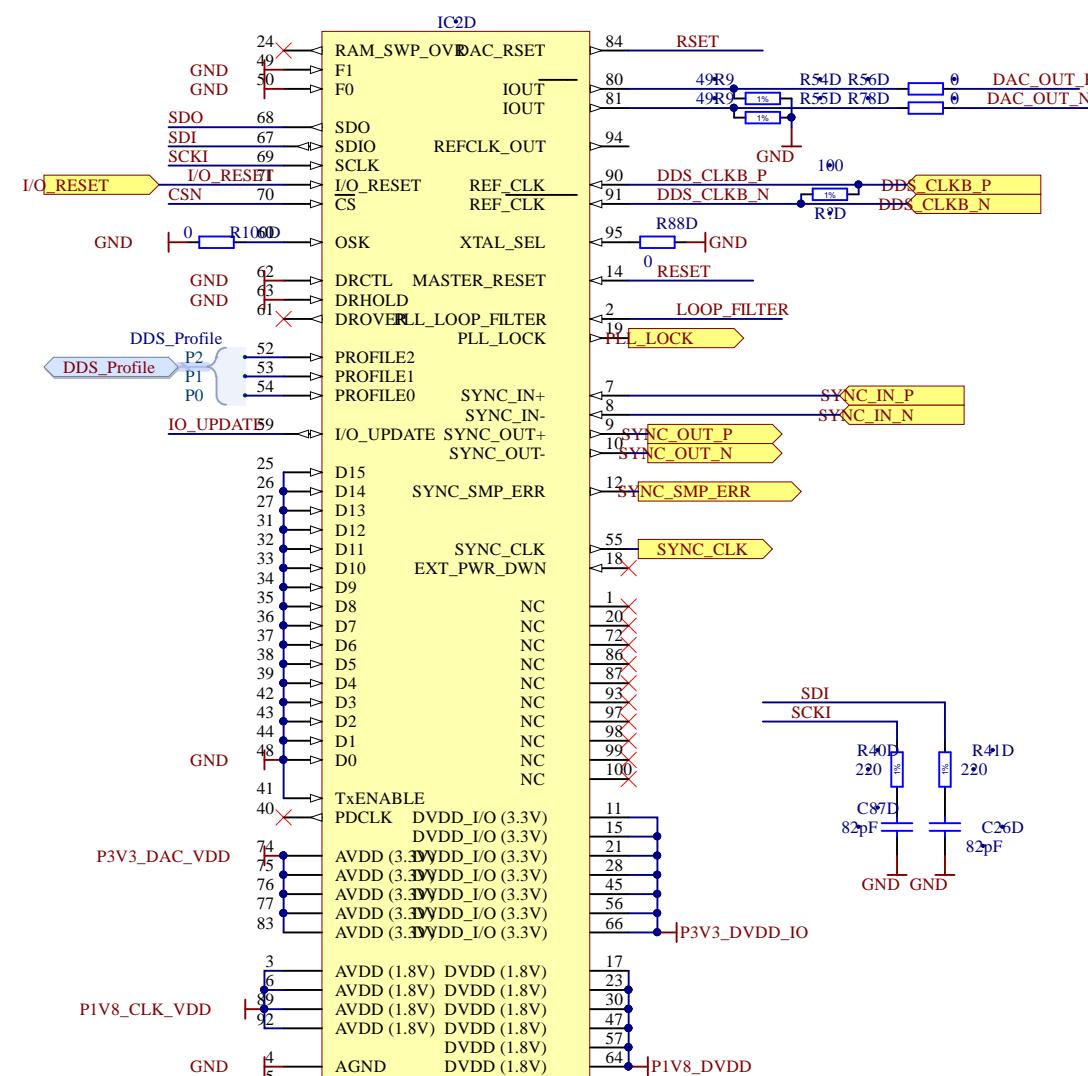


Table 8. Default Power-Up Frequency Options for 1 GHz System Clock

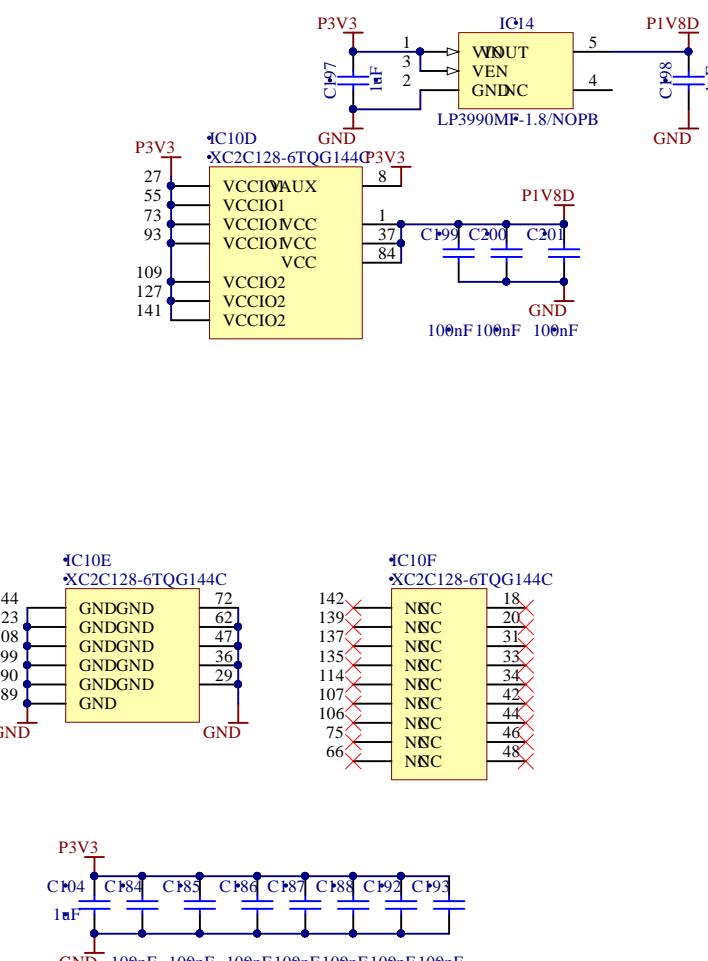
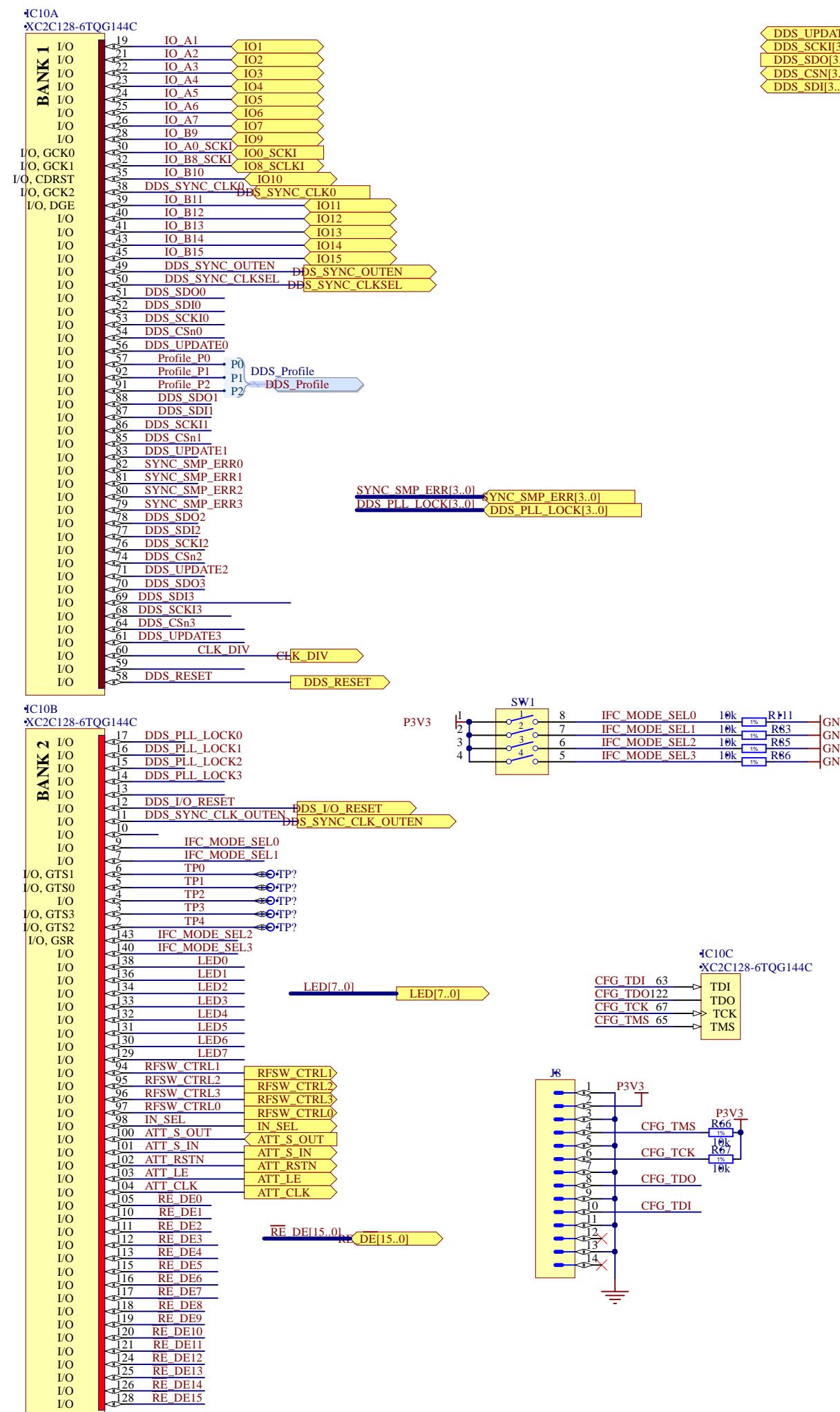
Status Pin		SYSCLK Input Mode	Output Frequency (MHz)	
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0	0	1	0	Xtal/PLL
0	0	1	1	Xtal/PLL
0	1	0	0	Xtal/PLL
0	1	0	1	Xtal/PLL
0	1	1	0	Xtal/PLL
0	1	1	1	Xtal/PLL
1	0	0	0	Direct
1	0	0	1	38.87939
1	0	1	0	51.83411
1	0	1	1	61.43188
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1	1	1	0	122.87903
1	1	1	1	155.51758

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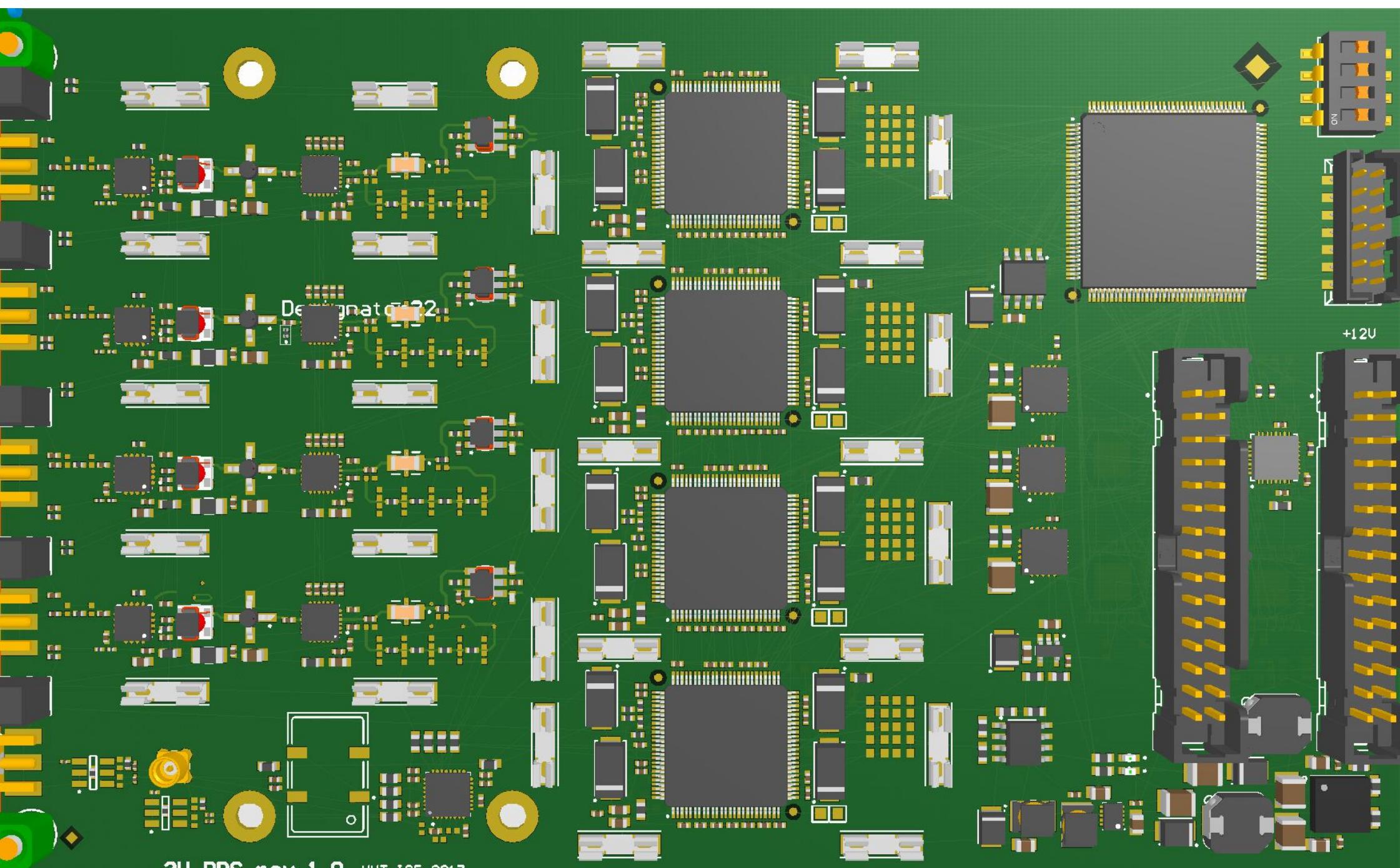
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