

SUMMARY

2.5+ Years of experience as Standard cell layout engineer

6 months as physical design trainee at Jagruthi Educational and Welfare society

Description

Standard Cell Layout Engineer - 1

Nov '18 - Present

KA, IN

- Currently Working as Standard Cell Layout Engineer - 1 in Microchip Technology India PVT Ltd.
- Job role includes generation of Open Access views ,Generation of Layout, DRC LVS, Layout Extraction, LEF MW views generation . Schematic views generation using StarVisionPro , netlist generation
- Robust Audit procedures which validates all the above views generated
- Validate Standard cells library collaterals sailing through various PNR stages
- Validates standard cells through various stages like manual Netlist stitch ~> Synthesis ~> PNR stage ~> DRC/LVS
- Worked on many nodes starting from 500nm to 28nm
- Involved in various other job activities like Density report generations , Contact improvement in the cells , library packaging testing of the new development scripts
- I am given the Ownership to organize and schedule Knowledge Sharing sessions across the team which is a Hit.
- Trained at Jagruthi Educational and Welfare society in Physical Design
- Having Hands on Knowledge in shell , Python, TCL and Skill scripts
- Looking for on opportunity to work as implementation engineer or standard cell domain

Work Experience

Microchip Technology Ind PVT Ltd.

Nov '18 - Present

Standard cell Layout Engineer - 1

KA, IN

Jagruthi Educational and Welfare society

May '18 - Oct '18

Physical design trainee

TS, IN

Education

Mtech in Microelectronics

Jan '21 - Present

BITS WILP

Pilani

Pursuing Mtech in Micro electronics at BITS pilani WILP

Btech

May '18

CVR College of Engineering

Hyderabad

Graduated in Electrical and Electronics with **76.5 %**

11th- 12th

Apr '14

Sri chaitanya junior Kalasala

Hyderabad

Completed 12th standard with **94.6 %**

10th

Apr '12

P Obul Reddy Public School

Hyderabad

Completed 10th Standard with **8.8 CGPA**

KEY SKILLS

OPEN ACESS views

LEF MW views generation

Extraction

DRC/LVS

LAYOUT

Calibre

aucdl netlisting

Automation

Layout QA

TECHNICAL SKILLS

- **Languages:** Shell, Python, Skill script , TCL
- **EDA Tools :** Cadence Innovus , Virtuoso
- **Platforms :** Linux/Windows