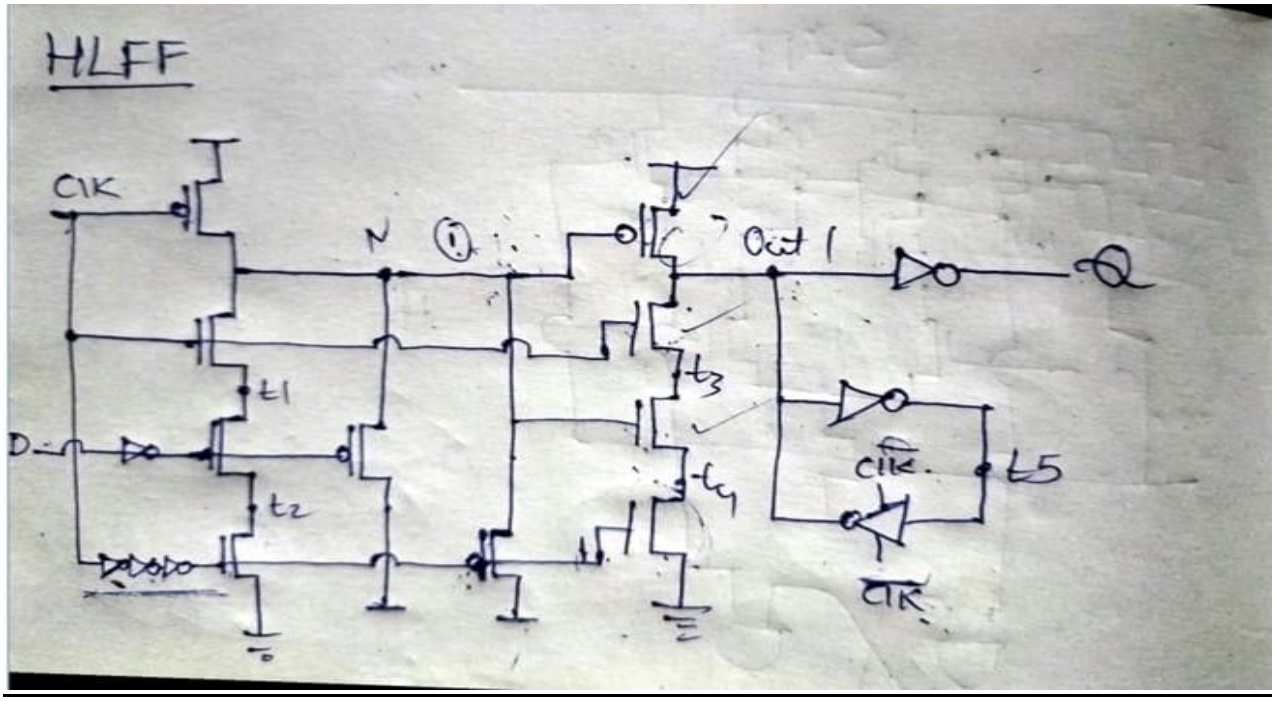
HLFF(Hybrid Latch Flip Flop)

Circuit diagram



Code

```
**********project2
.include "C:\Users\sindu\Downloads\ngspice-44.2_64\Spice64\bin\tri.sp"
.include "C:\Users\sindu\Downloads\ngspice-44.2_64\Spice64\examples\soi\bsim4soi\nmos4p0.mod"
.include "C:\Users\sindu\Downloads\ngspice-44.2_64\Spice64\examples\soi\bsim4soi\pmos4p0.mod"
.include "C:\Users\sindu\Downloads\ngspice-44.2_64\Spice64\bin\invr.sp"

Vpower vdd 0 1
Vgnd vss 0 0
vclk clk 0 PULSE(0 1 0.5n 50p 50p 0.5n 1n)
vd d 0  PULSE(0 1 0.4n 50p 50p 1n 2n)
*vclk clk 0 1
*vd d 0 1
.param wid = 6.1u
mp0 x clk vdd vdd P1 w='2*wid' l=0.18u
mn1 x clk n2 vss N1 w='1*wid' l=0.18u
mn2 n2 in n3 vss N1 w='1*wid' l=0.18u
mn3 n3 clkb vss vss N1 w='1*wid' l=0.18u
mp1 n4 x vdd vdd P1 w='3*wid' l=0.18u
mn4 n4 clk n5 vss N1 w='1.5*wid' l=0.18u
mn5 n5 x n6 vss N1 w='1.5*wid' l=0.18u
mn6 n6 clkb vss vss N1 w='1.5*wid' l=0.18u
mp2 x in vdd vdd P1 w='1*wid' l=0.18u
mp3 x clkb vdd vdd P1 w='1*wid' l=0.18u
x1 n4 o vdd vss invr
x2 o n4 clk clkb vdd vss tri
```

```
****inverterout
mn7 q n4 vss vss N1 w='3*wid' l=0.18u
mp5 q n4 vdd vdd P1 w='3*wid' l=0.18u
***inverterin
mn8 in d vss vss N1 w='1*wid' l=0.18u
mp6 in d vdd vdd P1 w='2*wid' l=0.18u
x3 clk o1 vdd vss invr
x4 o1 o2 vdd vss invr
*x5 o2 o3 vdd vss invr
*x6 o3 o4 vdd vss invr
*x7 o4 o5 vdd vss invr
*x8 o5 o6 vdd vss invr
*x9 o6 o7 vdd vss invr
*x10 o7 o8 vdd vss invr
x11 o2 clkb vdd vss invr
C q 0 5f
.tran 0.01n 10n
.control
run
meas tran ptotal AVG i(Vpower) FROM=0n TO=10n
meas tran clkq TRIG v(clk) VAL=0.5 RISE=6 TARG v(q) VAL=0.5 fall=1
meas tran dq TRIG v(d) VAL=0.5 fall=1 TARG v(q) VAL=0.5 fall=1
meas tran dclk TRIG v(d) VAL=0.5 fall=1 TARG v(clk) VAL=0.5 RISE=6
meas tran pulse_width TRIG v(clk) VAL=0.5 RISE=1 TARG v(clkb) VAL=0.5 fall=1
*meas tran clkq TRIG v(clk) VAL=0.5 RISE=2 TARG v(q) VAL=0.5 RISE=1
*meas tran dq TRIG v(d) VAL=0.5 rise=1 TARG v(q) VAL=0.5 rise=1
*meas tran dclk TRIG v(d) VAL=0.5 RISE=1 TARG v(clk) VAL=0.5 RISE=2
*plot v(clk) v(clkb)
plot  v(d) v(clk) v(q)
.endc
.end
```

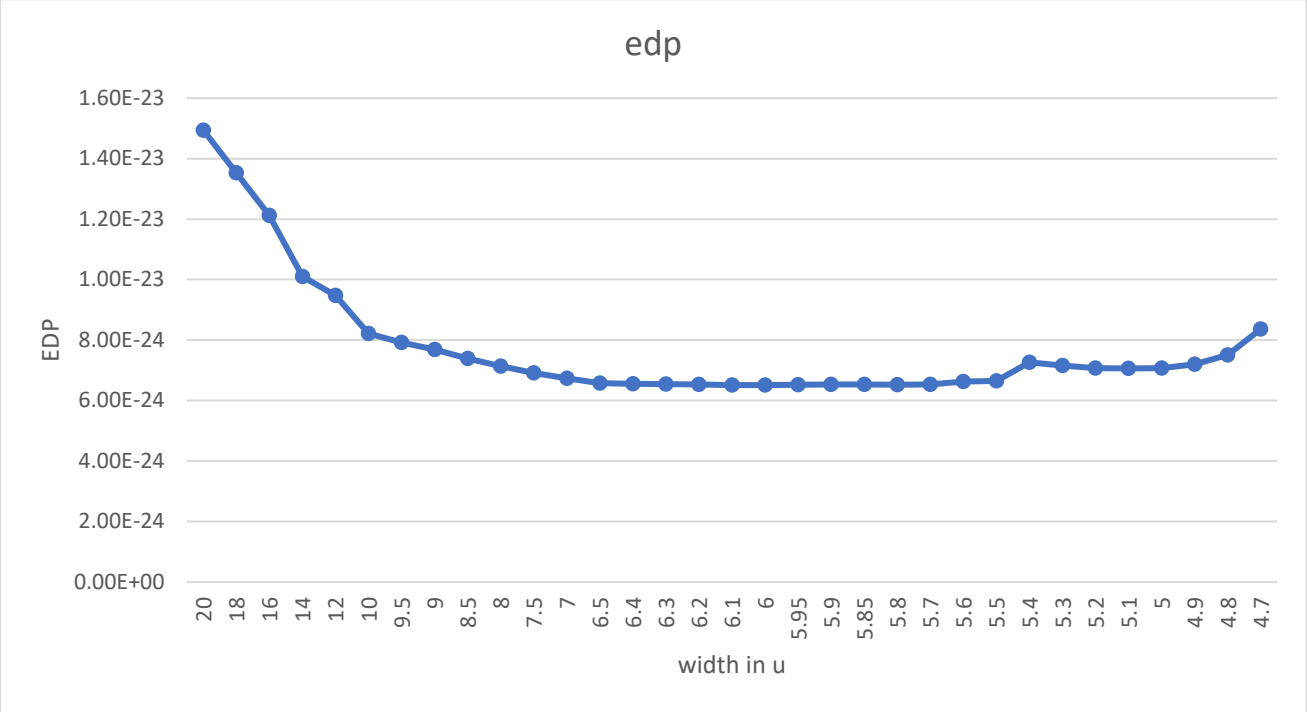
Subcircuit code

```
*inverter*
.SUBCKT invr in out vdd vss
.include "C:\Users\sindu\Downloads\ngspice-44.2_64\Spice64\examples\soi\bsim4soi\nmos4p0.mod"
.include "C:\Users\sindu\Downloads\ngspice-44.2_64\Spice64\examples\soi\bsim4soi\pmos4p0.mod"

mn out in vss vss N1 w=12u l=0.18u
mp out in vdd vdd P1 w=12u l=0.18u
.ENDS invr


.SUBCKT tri in out clk clkb vdd vss
.include "C:\Users\sindu\Downloads\ngspice-44.2_64\Spice64\examples\soi\bsim4soi\nmos4p0.mod"
.include "C:\Users\sindu\Downloads\ngspice-44.2_64\Spice64\examples\soi\bsim4soi\pmos4p0.mod"

mp0 net1 clk vdd vdd P1 w=2u l=0.18u
mp1 out in net1 vdd P1 w=2u l=0.18u
mn0 out in net2 vss N1 w=1u l=0.18u
mn1 net2 clkb vss vss N1 w=1u l=0.18u
.ENDS tri
```

Efficient HLFF for falling

width	ptotal	clk-q	d-q	d-clk	energy	edp
20	5.34E-04	1.45E-10	1.67E-10	2.20E-11	8.93E-14	1.49E-23
18	4.85E-04	1.45E-10	1.67E-10	2.20E-11	8.10E-14	1.35E-23
16	4.36E-04	1.46E-10	1.67E-10	2.10E-11	7.27E-14	1.21E-23
14	3.61E-04	1.46E-10	1.67E-10	2.10E-11	6.04E-14	1.01E-23
12	3.36E-04	1.46E-10	1.68E-10	2.15E-11	5.64E-14	9.47E-24
10	2.86E-04	1.48E-10	1.69E-10	2.15E-11	4.85E-14	8.21E-24
9.5	2.74E-04	1.48E-10	1.70E-10	2.15E-11	4.66E-14	7.92E-24
9	2.62E-04	1.48E-10	1.71E-10	2.35E-11	4.49E-14	7.68E-24
8.5	2.50E-04	1.48E-10	1.72E-10	2.39E-11	4.30E-14	7.39E-24
8	2.38E-04	1.49E-10	1.73E-10	2.42E-11	4.12E-14	7.13E-24
7.5	2.26E-04	1.49E-10	1.75E-10	2.55E-11	3.96E-14	6.91E-24
7	2.15E-04	1.50E-10	1.77E-10	2.70E-11	3.81E-14	6.74E-24
6.5	2.04E-04	1.50E-10	1.79E-10	2.90E-11	3.67E-14	6.57E-24
6.4	2.03E-04	1.51E-10	1.80E-10	2.90E-11	3.64E-14	6.56E-24
6.3	2.01E-04	1.52E-10	1.81E-10	2.90E-11	3.62E-14	6.54E-24
6.2	1.99E-04	1.52E-10	1.81E-10	2.90E-11	3.61E-14	6.53E-24
6.1	1.97E-04	1.52E-10	1.82E-10	3.01E-11	3.58E-14	6.51E-24
6	0.00019534	1.52633E-10	1.82633E-10	3E-11	3.57E-14	6.52E-24
5.95	0.0001946	1.52948E-10	1.83048E-10	3.01E-11	3.56E-14	6.52E-24
5.9	0.00019391	1.53278E-10	1.83478E-10	3.02E-11	3.56E-14	6.53E-24
5.85	0.00019297	1.53251E-10	1.83951E-10	3.07E-11	3.55E-14	6.53E-24
5.8	1.92E-04	1.53E-10	1.84E-10	3.16E-11	3.54E-14	6.53E-24
5.7	1.91E-04	1.53E-10	1.85E-10	3.20E-11	3.53E-14	6.53E-24
5.6	0.00019041	1.54418E-10	1.86618E-10	3.22E-11	3.55E-14	6.63E-24
5.5	0.00018831	1.53836E-10	1.87836E-10	3.4E-11	3.54E-14	6.64E-24
5.4	0.00020291	1.55183E-10	1.89183E-10	3.4E-11	3.84E-14	7.26E-24
5.3	0.000197	1.56184E-10	1.90584E-10	3.44E-11	3.75E-14	7.16E-24
5.2	0.00019213	1.56696E-10	1.91896E-10	3.52E-11	3.69E-14	7.07E-24
5.1	1.88E-04	1.57E-10	1.94E-10	3.63E-11	3.64E-14	7.06E-24
5	1.85E-04	1.58E-10	1.96E-10	3.73E-11	3.61E-14	7.07E-24
4.9	1.79E-04	1.50E-10	2.00E-10	5.00E-11	3.59E-14	7.20E-24
4.8	1.77E-04	1.50E-10	2.06E-10	5.60E-11	3.65E-14	7.50E-24
4.7	1.81E-04	1.49E-10	2.15E-10	6.61E-11	3.89E-14	8.36E-24

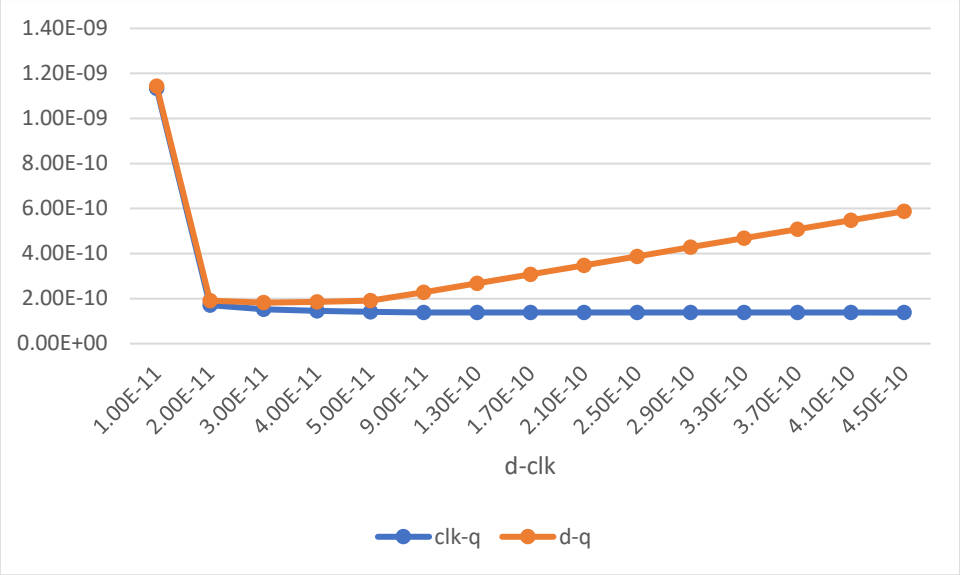
EDP:



Minimum EDP=6.51E-24

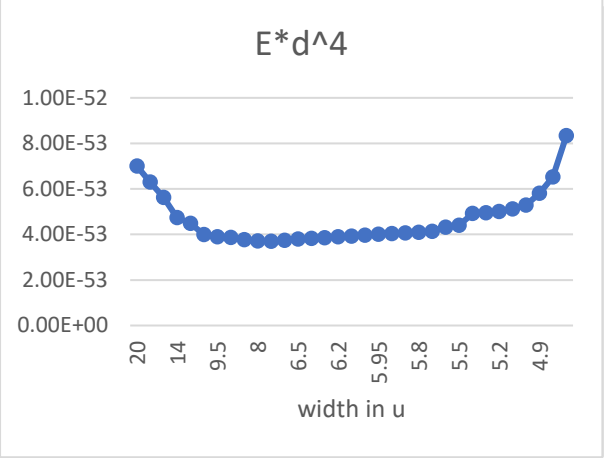
Setup time characterization for efficient circuit :

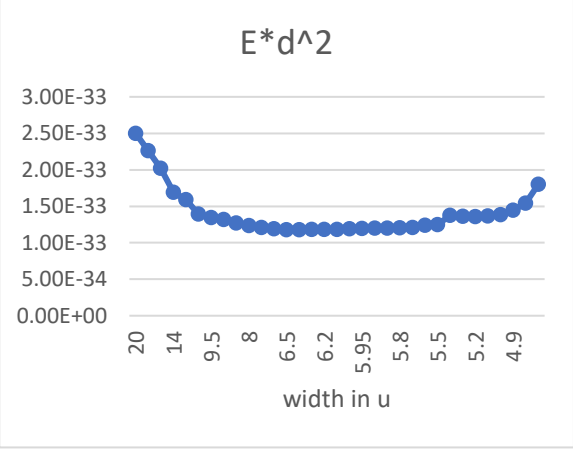
data	clk-q	d-q	d-clk
1	1.38E-10	5.88E-10	4.50E-10
1.04	1.38E-10	5.48E-10	4.10E-10
1.08	1.38E-10	5.08E-10	3.70E-10
1.12	1.38E-10	4.68E-10	3.30E-10
1.16	1.38E-10	4.28E-10	2.90E-10
1.2	1.38E-10	3.88E-10	2.50E-10
1.24	1.38E-10	3.48E-10	2.10E-10
1.28	1.38E-10	3.08E-10	1.70E-10
1.32	1.38E-10	2.68E-10	1.30E-10
1.36	1.38E-10	2.28E-10	9.00E-11
1.4	1.42E-10	1.92E-10	5.00E-11
1.41	1.45E-10	1.85E-10	4.00E-11
1.42	**1.52E-10**	1.82E-10	3.00E-11
1.43	1.71E-10	1.91E-10	2.00E-11
1.4	1.13E-09	1.14E-09	1.00E-11

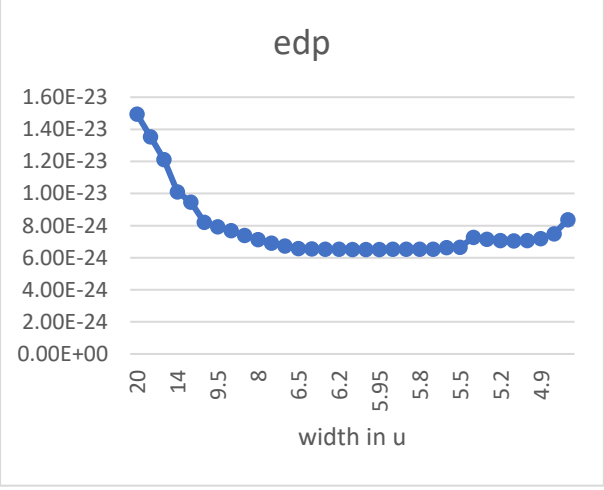


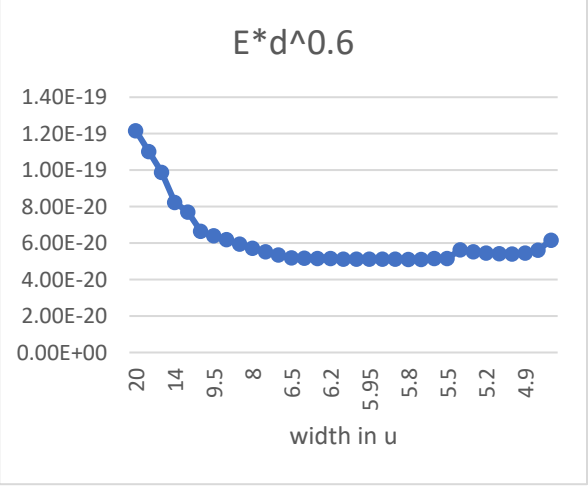
Setup time=1.52E-10

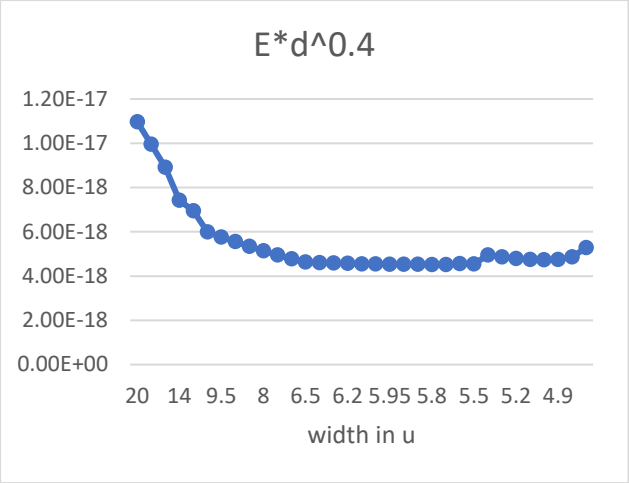
EDP plots

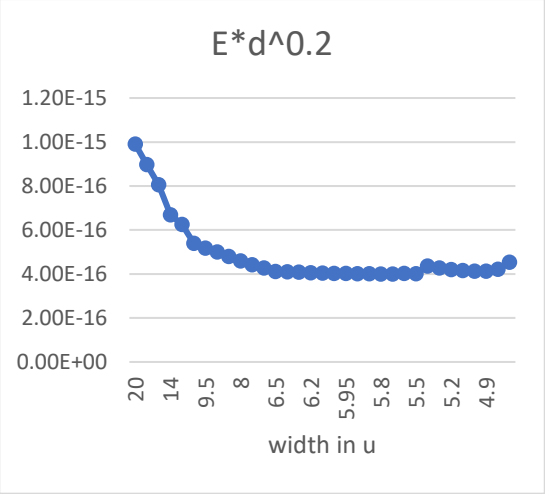






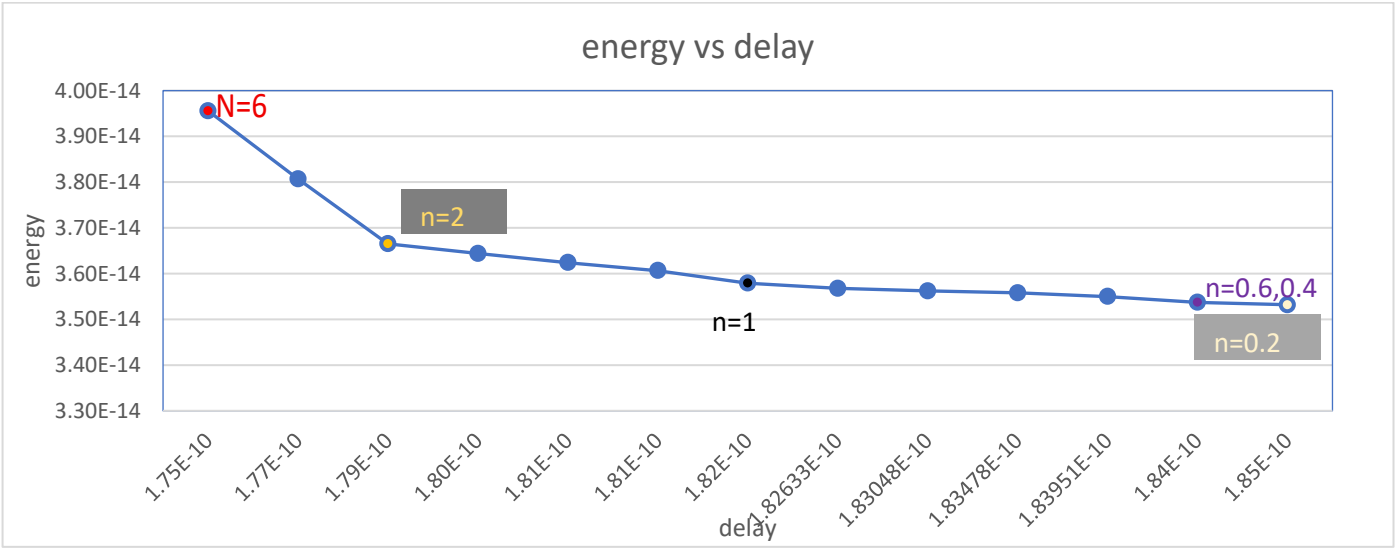






Energy vs delay:

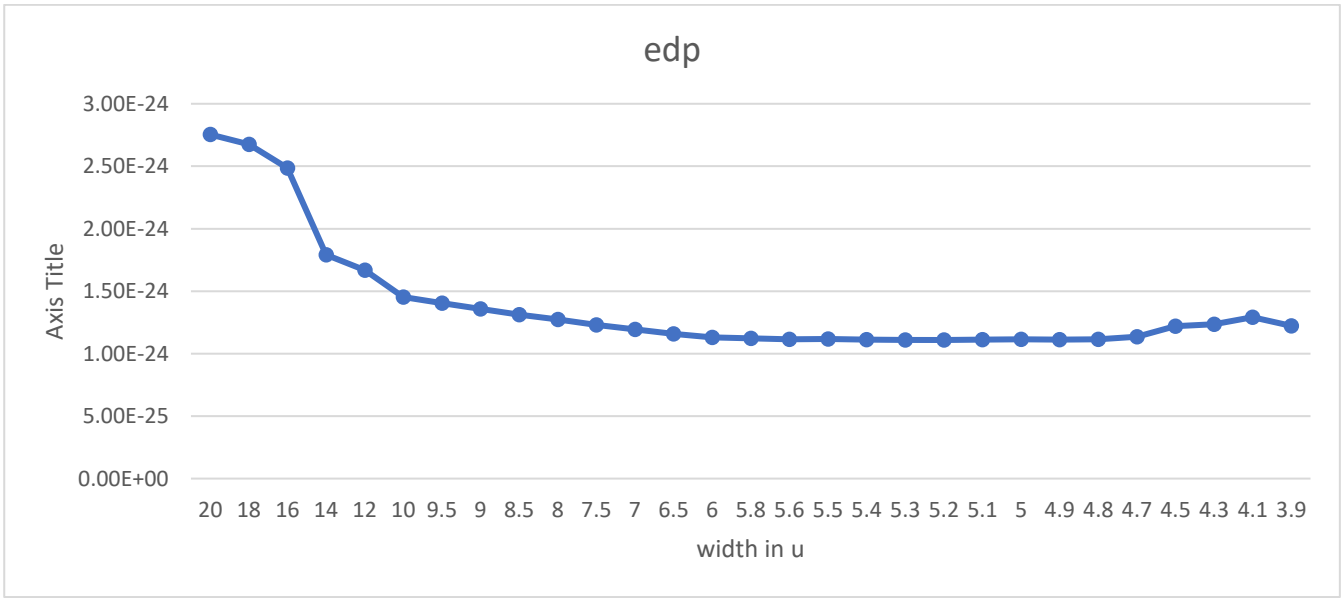
width	ptotal	d-q	energy	edp	E*d^4	E*d^2	E*d^0.6	E*d^0.4	E*d^0.2
7.5	2.26E-04	1.75E-10	3.96E-14	6.91E-24	**3.69E-53**	1.21E-33	5.53E-20	4.95E-18	4.42E-16
7	2.15E-04	1.77E-10	3.81E-14	6.74E-24	3.73E-53	1.19E-33	5.36E-20	4.78E-18	4.27E-16
6.5	2.04E-04	1.79E-10	3.67E-14	6.57E-24	3.79E-53	**1.18E-33**	5.20E-20	4.63E-18	4.12E-16
6.4	2.03E-04	1.80E-10	3.64E-14	6.56E-24	3.82E-53	1.18E-33	5.18E-20	4.61E-18	4.10E-16
6.3	2.01E-04	1.81E-10	3.62E-14	6.54E-24	3.85E-53	1.18E-33	5.17E-20	4.59E-18	4.08E-16
6.2	1.99E-04	1.81E-10	3.61E-14	6.53E-24	3.89E-53	1.18E-33	5.15E-20	4.57E-18	4.06E-16
6.1	1.97E-04	1.82E-10	3.58E-14	6.51E-24	3.92E-53	1.18E-33	5.12E-20	4.55E-18	4.03E-16
6	0.00019534	1.82633E-10	3.57E-14	6.52E-24	3.97E-53	1.19E-33	5.12E-20	4.54E-18	4.02E-16
5.95	0.0001946	1.83048E-10	3.56E-14	6.52E-24	4.00E-53	1.19E-33	5.12E-20	4.54E-18	4.02E-16
5.9	0.00019391	1.83478E-10	3.56E-14	6.53E-24	4.03E-53	1.20E-33	5.12E-20	4.54E-18	4.02E-16
5.85	0.00019297	1.83951E-10	3.55E-14	6.53E-24	4.06E-53	1.20E-33	5.12E-20	4.53E-18	4.01E-16
5.8	1.92E-04	1.84E-10	3.54E-14	6.53E-24	4.10E-53	1.20E-33	**5.11E-20**	**4.52E-18**	4.00E-16
5.7	1.91E-04	1.85E-10	3.53E-14	6.53E-24	4.14E-53	1.21E-33	5.11E-20	4.52E-18	**3.99E-16**
5.6	0.00019041	1.86618E-10	3.55E-14	6.63E-24	4.31E-53	1.24E-33	5.17E-20	4.56E-18	4.03E-16



Rising EDP

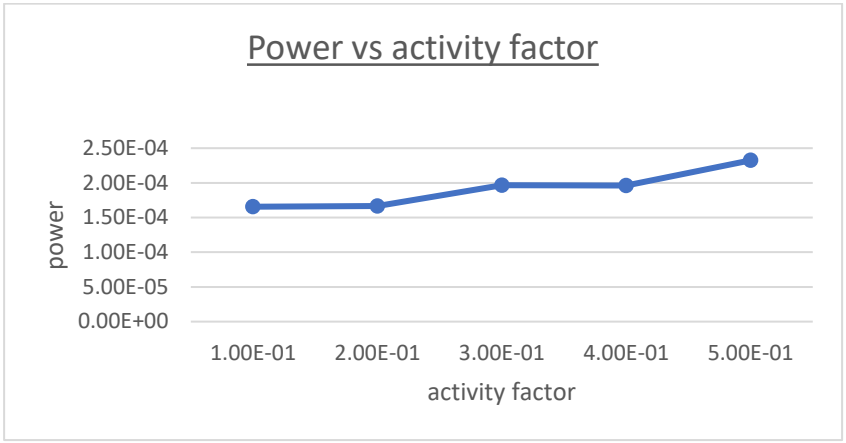
width	ptotal	clk-q	d-q	d-clk	energy	edp
20	5.57E-04	8.33E-11	7.03E-11	-1.30E-11	3.92E-14	2.75E-24
18	5.43E-04	8.32E-11	7.02E-11	-1.30E-11	3.81E-14	2.67E-24
16	5.04E-04	8.33E-11	7.03E-11	-1.30E-11	3.54E-14	2.49E-24
14	3.56E-04	8.39E-11	7.09E-11	-1.30E-11	2.53E-14	1.79E-24
12	3.29E-04	8.43E-11	7.13E-11	-1.30E-11	2.34E-14	1.67E-24
10	2.77E-04	8.55E-11	7.25E-11	-1.30E-11	2.01E-14	1.45E-24
9.5	2.64E-04	8.59E-11	7.29E-11	-1.30E-11	1.93E-14	1.40E-24
9	2.52E-04	8.64E-11	7.34E-11	-1.30E-11	1.85E-14	1.36E-24
8.5	2.40E-04	8.70E-11	7.40E-11	-1.30E-11	1.77E-14	1.31E-24
8	2.28E-04	8.73E-11	7.48E-11	-1.25E-11	1.70E-14	1.27E-24
7.5	2.16E-04	8.82E-11	7.54E-11	-1.28E-11	1.63E-14	1.23E-24
7	2.05E-04	8.91E-11	7.63E-11	-1.28E-11	1.56E-14	1.19E-24
6.5	1.93E-04	9.01E-11	7.74E-11	-1.27E-11	1.50E-14	1.16E-24
6	1.83E-04	9.14E-11	7.87E-11	-1.27E-11	1.44E-14	1.13E-24
5.8	1.79E-04	9.18E-11	7.93E-11	-1.25E-11	1.42E-14	1.12E-24
5.6	1.75E-04	9.24E-11	7.99E-11	-1.25E-11	1.39E-14	1.11E-24
5.5	1.73E-04	9.25E-11	8.04E-11	-1.21E-11	1.39E-14	1.12E-24
5.4	1.71E-04	9.28E-11	8.07E-11	-1.21E-11	1.38E-14	1.11E-24
5.3	1.69E-04	9.32E-11	8.11E-11	-1.21E-11	1.37E-14	1.11E-24
5.2	1.67E-04	9.35E-11	8.14E-11	-1.21E-11	1.36E-14	1.11E-24
5.1	1.66E-04	9.37E-11	8.20E-11	-1.17E-11	1.36E-14	1.11E-24
5	1.64E-04	9.41E-11	8.24E-11	-1.17E-11	1.35E-14	1.11E-24
4.9	0.000162858	9.46507E-11	8.26507E-11	-1.2E-11	1.35E-14	1.11E-24
4.8	1.65E-04	1.04E-10	8.22E-11	-2.20E-11	1.36E-14	1.12E-24
4.7	1.62E-04	9.53E-11	8.38E-11	-1.15E-11	1.36E-14	1.14E-24
4.5	1.70E-04	9.62E-11	8.47E-11	-1.15E-11	1.44E-14	1.22E-24
4.3	1.67E-04	9.71E-11	8.61E-11	-1.10E-11	1.44E-14	1.24E-24
4.1	1.69E-04	9.84E-11	8.74E-11	-1.10E-11	1.48E-14	1.29E-24
3.9	1.55E-04	9.98E-11	8.88E-11	-1.10E-11	1.38E-14	1.22E-24

Minimum EDP=1.11E-24

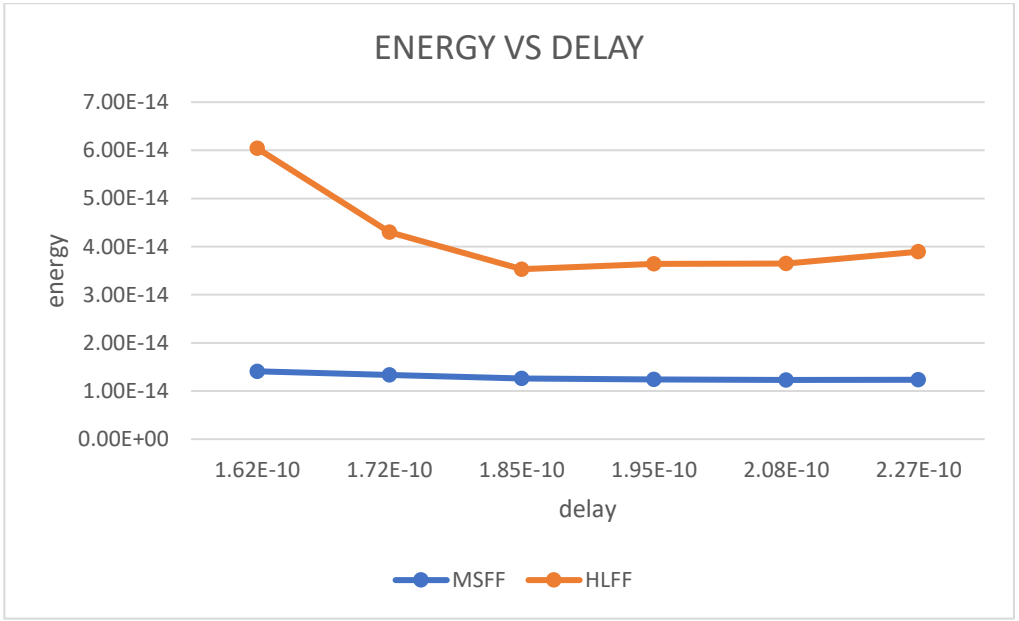


Power vs activity factor

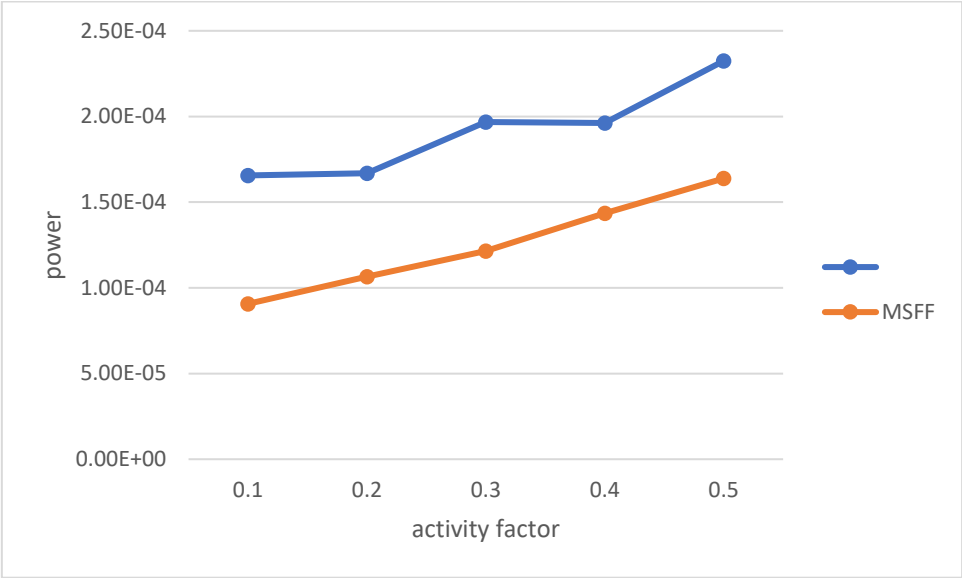
activity factor	power
1.00E-01	1.66E-04
2.00E-01	1.67E-04
3.00E-01	1.97E-04
4.00E-01	1.96E-04
5.00E-01	2.32E-04



Energy of HLFF and MSFF for different delays :



Power vs activity factor of MSFF AND HLFF:



Power of HLFF

total power=	2.32E-04

clk, data	static power
0,0	2.77E-07
0,1	2.90E-07
1,0	5.34E-08
1,1	6.31E-08
avg=	1.71E-07

data	clk power
0	2.29E-04
1	7.89E-05
avg=	1.54E-04

clk	data switching power
0	2.10E-05
1	1.48E-05
avg=	1.79E-05

Detailed Conclusion and Insights:

The HLFF (Half-Latch Flip-Flop) design demonstrates superior energy efficiency, especially in falling transitions where the Energy Delay Product (EDP) is minimized compared to rising

transitions. The worst-case scenario occurs in falling edges, but even then, HLFF outperforms traditional flip-flop (MSFF) designs in power-delay trade-offs.

Setup time characterization reveals a setup time of approximately 117 ps, indicating the time window required before the clock edge to reliably capture data. This is a critical timing parameter for high-frequency circuit design.

The power consumption scales linearly with the activity factor (switching activity), with measured power increasing from 1.16E-04 W at 0.1 activity factor to 1.64E-04 W at 0.5. This shows predictable power behavior under varying input switching conditions.

Static (leakage) power is also characterized, with values in the range of 10^-7 W, which although low, contributes to overall power in inactive or low activity states.

Comparisons between HLFF and the standard MSFF indicate that HLFF has higher power under low activity factors but exhibits better energy efficiency as delays decrease, implying better suitability for timing-critical low-power designs.

Multiple plots representing EDP versus width and energy versus delay highlight how HLFF can be tuned by transistor sizing (width) for optimal performance depending on workload demands.

Drawbacks and Challenges:

Despite the efficiency gains, the HLFF's setup time and delay sensitivity to transistor sizing and transitions require careful optimization, potentially complicating physical design and timing closure.

The higher power consumption at certain activity levels compared to MSFF may restrict its use in ultra-low power domains without further enhancements.

The trade-off in performance between rising and falling transitions may lead to non-uniform behavior dependent on input signal characteristics, requiring more complex adaptive control in some applications.

The report implies a need to balance the energy-delay trade-off carefully, which may limit the generality of the HLFF design in some integrated circuit environments.

Potential area overhead or increased design complexity compared to simpler flip-flops has not been explicitly detailed but could be a concern based on additional circuitry required for the efficient operation in falling transitions.

Additional Observations:

Total switching power includes contributions from both data and clock signals; HLFF shows a lower average clock switching power compared to data.

HLFF's slope in power vs activity is lower (1.19E-04) than MSFF's slope (1.52E-04), indicating a slightly more controlled increase in power consumption as switching activity increases.

This design can be particularly beneficial for circuits where energy-delay product optimization is critical such as in portable or battery-operated devices.