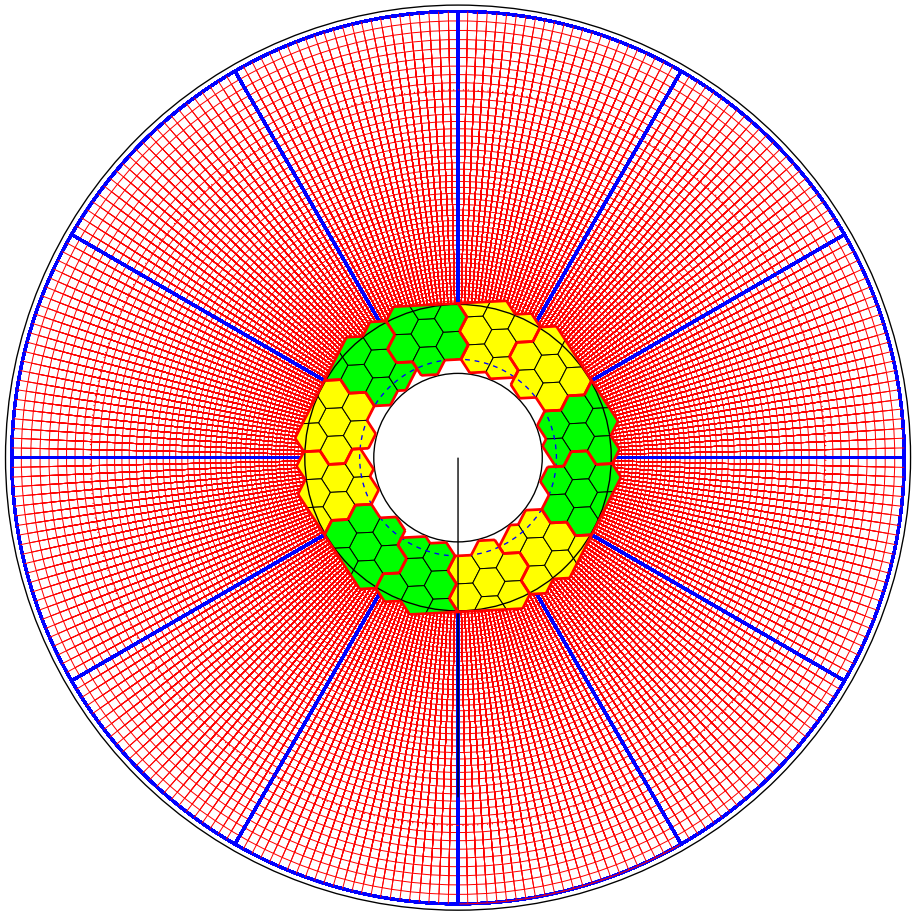

Figure 2.13: Layout of wafers and tiles in a layer where both are present: the 22$^{\text{nd}}$ layer of CE-H.

cast and machined or injection-moulded, as individual tiles or multiple tile units (megatiles). In addition, the reflective coating with paint or foil is still subject to optimisation by prototyping. Both approaches build on experience: painted megatiles are used in the CMS HCAL, and foil-wrapped individual tiles have been developed in the CALICE framework. The final choice, to be made in 2019, will be driven by cost, performance, and ease of assembly considerations, e.g. the amount of light yield loss and noise increase due to irradiation, and by thermal-mechanical considerations. The thermal expansion coefficient of plastic scintillator is $78 \times 10^{-6}\,\mathrm{K}^{-1}$ and thus 5 times larger than that of the copper cooling plate and the PCB. For a temperature difference of 70 K (assembly at 30 °C and operation at −40 °C) this leads to millimeter-size mismatches and in practice limits the maximum size of megatiles to about 20 cm. In the inner parts with small cells, such a size still represents a significant reduction in the number of parts to be handled. On the other hand individual tiles are better suited for assembly using standard pick-and-place tools.

The tileboard holds the SiPMs, the front-end electronics, LEDs and associated driving circuitry, low voltage regulators and the connectivity to the motherboard that is situated at the outer periphery of the cassette.