Sid Singh

ELEC2210 W 3-4:50pm

Final Design Project Report

This design project requires application of the knowledge learned throughout this course in order to construct a basic finite state machine. The aforementioned system takes a certain sequence of inputs and translates them into a corresponding output based on given constraints. Specifically, a 4-digit code must be entered as an input for a security system. Whilst there is a lack of 4 consecutive inputs, an LED must blink at a rate of 2 blinks/second (standby mode). When 4 digits are entered, the LED stops and a comparison is made to a provided code sequence to determine if the input matches. If the comparison results in a 1 (perfect match), the LED must come on at a steady state and a motor must be turned on (fan motor). Alternatively, if the sequence does not match the provided one, the LED must turn off and an alarm should come off operating in a frequency detectable by the human ear.

This report is separated into three sections outlining the fundamental process of creating the system. The first part involves the construction of the mechanism which enables the LED to blink at a rate of 2/second. The second part describes the system used to enable the fan motor when a correct sequence is entered. Finally, the third part outlines the implementation of a binary counter to ensure the functionality of the alarm system.

An LED may blink in the presence of a square wave function input as long as the turn on voltage supersedes a portion of the wave voltage. To regulate the period at which the LED blinks, the wave is centered at an average value of 0V with a Vpp of 5V (0V offset). In order for the 2 blinks/second rate to be accurate, calculations were made leading to the determination of a wave frequency of 2Hz. This wave is supplied by an external function generator connected through the breadboard's FGEN terminal. In order to enable the LED to leave standby mode (stop blinking), a shift register is connected to the DIO0-2 IO ports. A

sequence of logic gates is utilized to return an active high signal when the 4 inputs match the code provided by the TA during the lab. These 4 predetermined inputs are entered into digital writer ports connected to DIO7-4. These DIO ports are connected to XOR gates in tandem with corresponding outputs of the shift register. When the corresponding input digit (1^{st},2^{nd}, 3^{rd}, 4^{th}) matches the predetermined digit, the gate returns 0 as shown in Table 1. This output is then inverted to 1 using a double input technique into a NAND gate. The output of this NAND gate is then compared to the outputs of NAND gates associated with other digits using an AND gate. The signals are then put through additional AND comparisons until a single high or low value is outputted. This value is 1 when the codes match and 0 otherwise. This final signal is routed to an OR gate with the input from FGEN. However, in order to maintain functionality of the clear bit (DIO0), the FGEN input is routed through an AND gate with DIO0 as an additional input. This means that the wave will only enter the LED if DIO0 is set to a high value (Figure 2, LOW=CLR).

Input Digit	Correct Digit	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

Table 1: Crucial XOR Logic

FGEN+DIO0(CLR)	Matching Logic Output	LED (AND)
0	0	0
0	1	0
Square Wave	0	0
Square Wave	1	Square Wave (Blink)

Table 2: Final LED Input Logic

The fan motor must come on only when there are 4 digits entered and they match the value and order of the predetermined code. This segment of logic was previously explained and completed in the previous part. Due to the signal becoming weak from logical conversion, a BJT is used for amplification in tandem with a 5V source and 500 ohm resistor. The setup is depicted below in Figure 1.

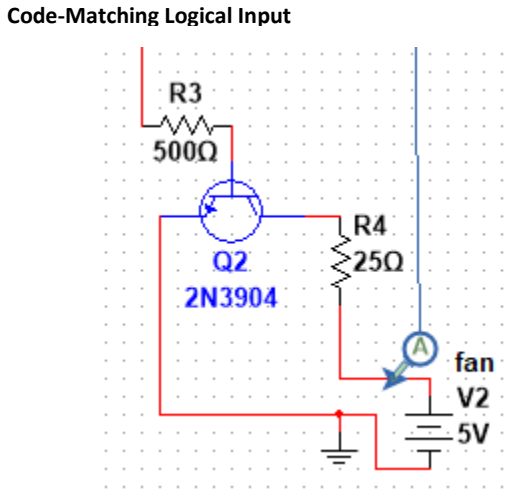

Figure 1: Setup for Fan

The operation of the alarm proves to be a more tedious task. The alarm must only sound when 4 digits have been entered. Otherwise, it may constantly sound due to a low input from the code-matching logical output. To combat this issue, a binary counter is utilized to ensure that 4 inputs have been entered. The clock and clr inputs (DIO2 and DIO0) previously attached to the shift register is routed to the counter. All counter inputs (A-D) are grounded to ensure the clock is the only factor affecting output. Decimal 4 is 100 in binary thus output QD is irrelevant. A high value must be returned when the counter outputs 100 in the order QC, QB, and QA. Therefore, QA and QB must be 0. These outputs are both inverted using NAND gate techniques and then routed as inputs to an AND gate. When both of these values are 0, their inverted values are 1 so consequently the AND gate will return 1. Then, this output is routed to an additional AND gate with QC as another input. Thus, when QCQBQA = 100, the logic system will return 1. This logic system is outlined in Table 3. The counter logic output is inputted

into an AND gate with the same signal that leads to the fan. However, the fan signal is inverted using a NAND gate before this. This logic is shown in Table 4. The reason behind this inversion is that the code-matching logic will output 0 (low) when the codes don't match, but a signal from the function generator is required to power the alarm speaker. Similar to the previous part, a BJT is required to amplify the signal in order to produce a current which powers the fan. This setup is shown below in Figure 2.

QA NAND QA = (X)	QB NAND QB = (Y)	X AND Y = (Z)	Z AND QC
0	0	0	0
0	1	0	1
1	0	0	‘’
1	1	1	‘’

Table 3: Counter Logic Output

Counter Logic	Inverted Code-Match Logic	BJT Input Signal (AND)
0	0	0
0	1	0
1	0	0
1	1	1

Table 4: Speaker BJT Input Logic

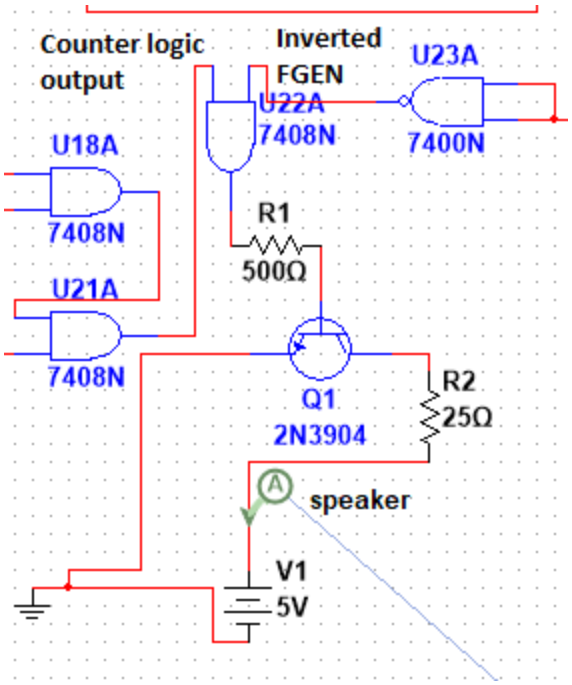

Figure 2: Speaker Setup with Logic Labels

The project was planned and simulated in Multisim. Shown in Figure 3, the LED is in the blinking stage and both fan and speaker modules (represented by probes) show active low values due to a lack of inputs. Figure 4 shows the system when a correct code is entered. The LED remains on and the magnitude of the fan voltage is increased. Figure 5 shows when an incorrect code is entered. The fan voltage is active low and the magnitude of the speaker voltage is increased. Figure 6 depicts a function-block diagram which makes the complete system more easily understandable.

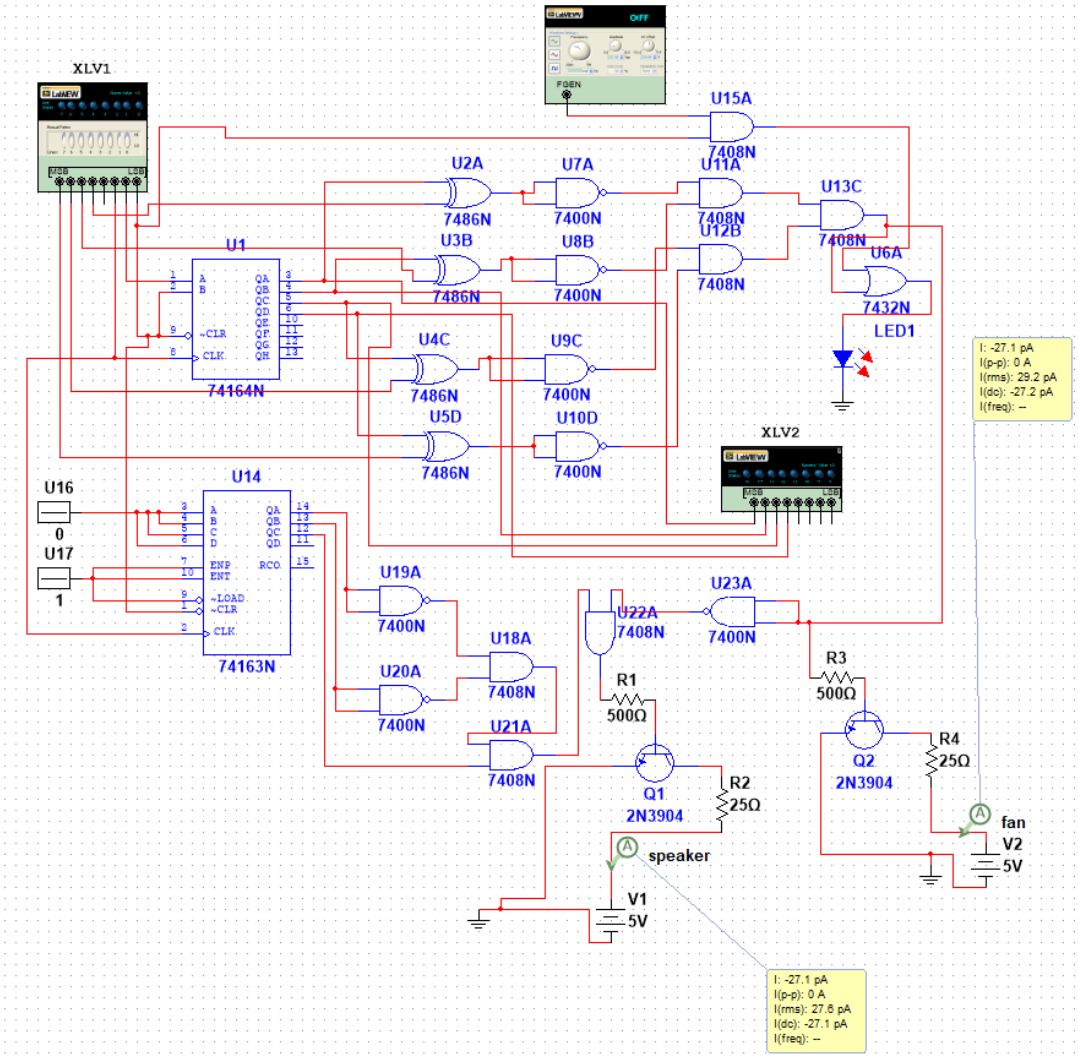

Figure 3: Standby State

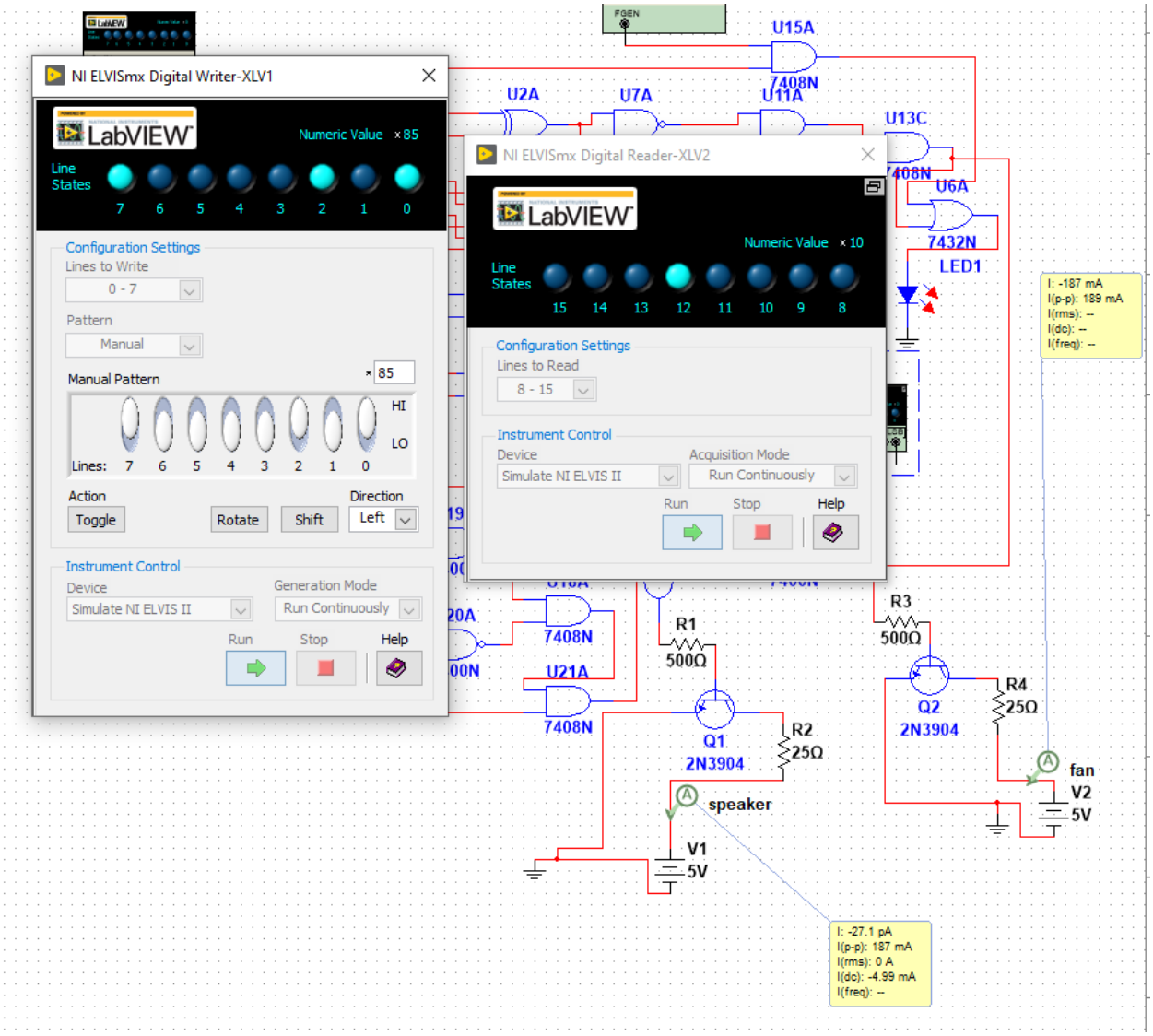

Figure 4: Correct Code State

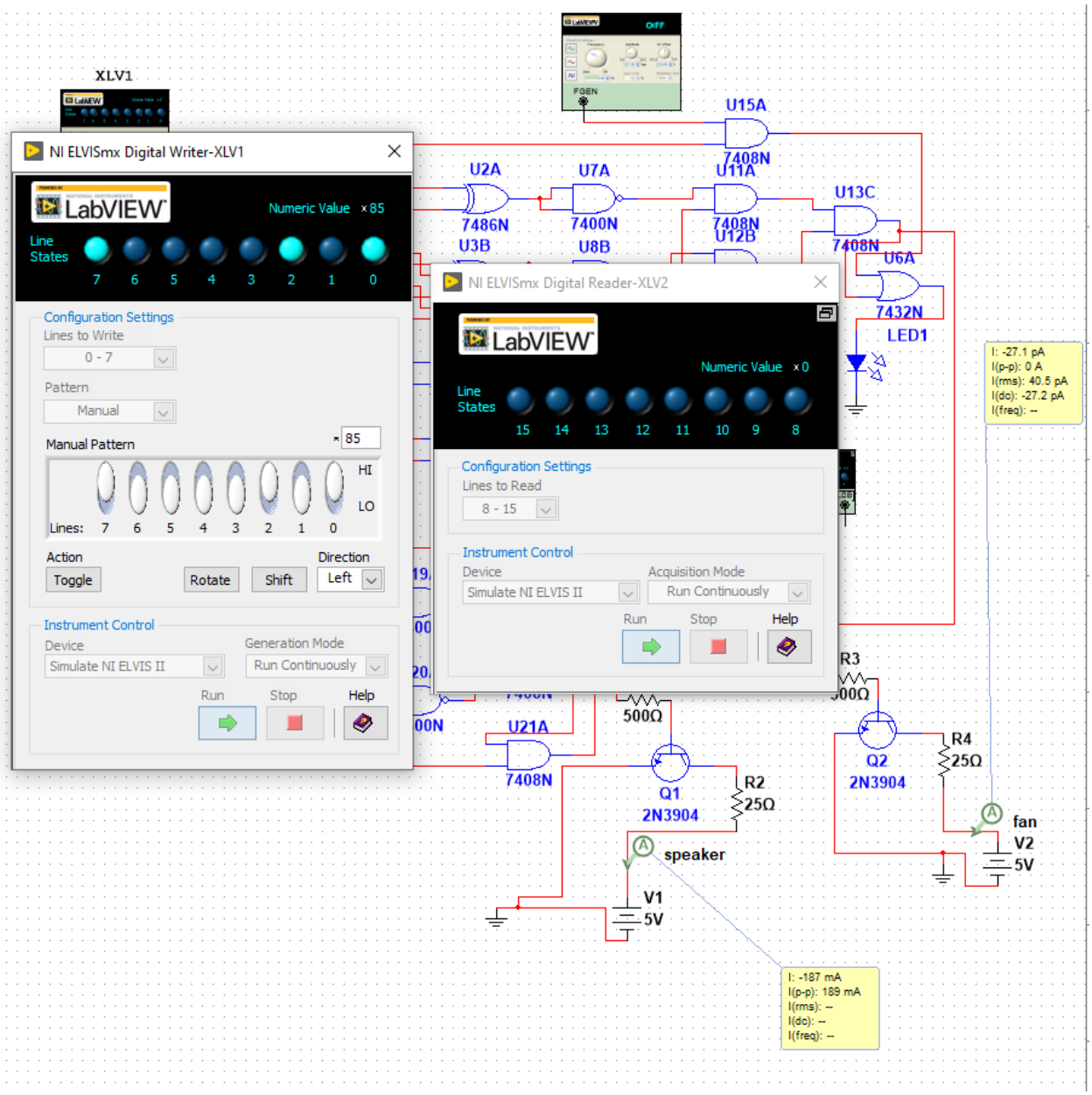

Figure 5: Incorrect Code State

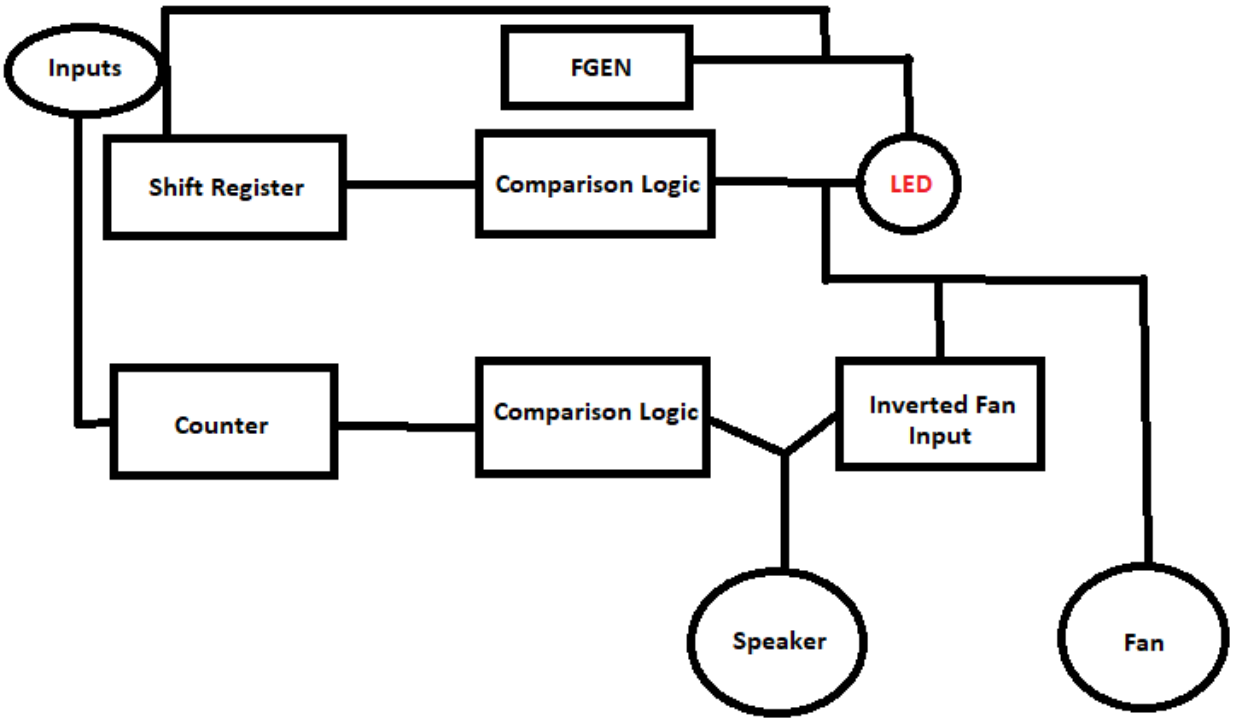

Figure 6: FSM Function-Block Diagram

In conclusion, this was an extremely fun project to work through. It required a significant amount of knowledge learned throughout the course to implement. The design proved useful in reaffirming the practices learned in-lab throughout the course.

Bibliography

ELEC 2210 – Final Design Project. Online Lab Manual. (Rep.). (n.d.). Auburn University.