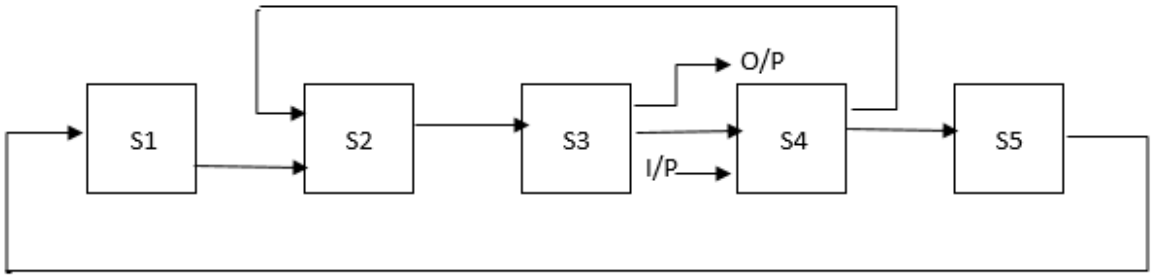
ASSIGNMENT II

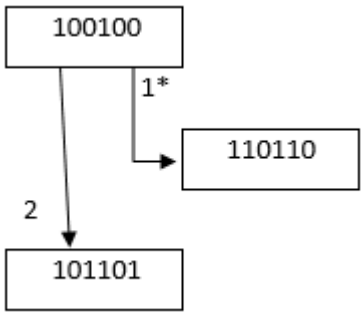
1. Consider a pipelined processor with 5 stages. It has a total evaluation time of 6 clock cycles. All successor stages must be used after each clock cycle. Draw the state transition diagram showing all possible transitions.



2. Consider the following reservation table. Find the all the greedy cycles and show all the steps clearly.

	1	2	3	4	5	6	7
A	X			X			X
B			X				
C		X			X		
D		X				X	

3. Complete the state transition diagram and find all simple cycles, latency cycles and greedy cycles.



4. Consider the following pipeline reservation table. What will the maximum throughput of this pipeline if τ=30 ns.

	1	2	3	4	5	6
A	X					X
B		X			X	
C			X			
D				X		
E		X				X

5. Three functional pipelines are characterized by the following reservation tables. Using these three pipelines a composite pipeline is formed. Each task going through this composite pipeline in the following order: f1 first, f2 and f3 next, f1 again and then the output is obtained. Draw the reservation table for the composite pipeline and determine the MAL associated with the shortest greedy cycle.

	1	2	3	4
S1	X			
S2		X		
S3			X	X

	1	2	3	4
T1	X			X
T2		X		
T3			X	

	1	2	3	4
U1	X		X	
U2				X
U3		X		

6. Find the sum of the numbers given below using an array of 16 PEs. Write the algorithm and the masking scheme for the same.

12 23 21 43 21 13 15 4 6 10