Assignment -1

1A.Explain the working of Indirect Cycle and Execute cycle with a neat diagram

1B. An instruction is 2byte wide and there are 32 such instructions. How many clock cycles does it take to execute it on

i) WSBS system
ii) WSBP [1, 8]
iii) WPBS[32, 1]
iv) WPBP[32, 8]

Explain each step in detail.

2A. Give Space Time Diagram for Instruction Pipelining, for 6 instructions across 4 stages.

2B. Describe average parallelism and processor utilization using Feng's Classification.

3A.Explain the concept of General pipeline with neat diagram

3B. With a neat diagram, explain the system of 16 PDP-11 minicomputers of a word length of 16 bits with respect to MISD and MIMD modes as per Handlers classifications.

4A. Explain pipeline classification schemes based on pipeline configuration and control strategies?

4B. Consider the execution of a program of 20000 instructions by a linear pipelining processor. The clock rate of the pipelining is 25MHz. Pipeline has five stages and one instruction is issued per clock cycle. Neglect penalties due to branch instructions and out of sequence execution. Calculate (i) Speedup (ii) Efficiency (iii) Throughput

5A.Define the following terminologies:

a) Pipeline efficiency
b) Static Pipeline
c) Multifunctional Pipeline

5B. Prove that a k-stage linear pipeline can be atmost k times faster than that of a non-pipelined serial processor?