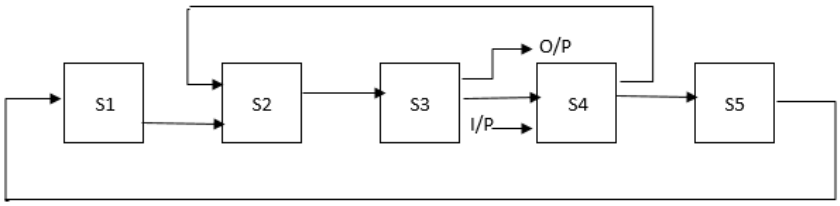
ASSIGNMENT II- Solutions

1. Consider a pipelined processor with 5 stages. It has a total evaluation time of 6 clock cycles. All successor stages must be used after each clock cycle. Draw the state transition diagram showing all possible transitions.

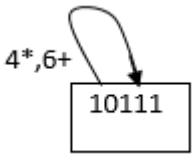


Ans: Reservation Table:

	1	2	3	4	5	6
S1			X			X
S2		X		X	X	
S3			X		X	X
S4	X			X		X
S5		X			X	

Forbidden Latencies: 5, 3, 2, 1 Permissible Latencies: 6, 4 Initial collision vector: 10111

State transition diagram:



Node A:

C4: 00001
10111

10111

C6: 00000
10111

10111

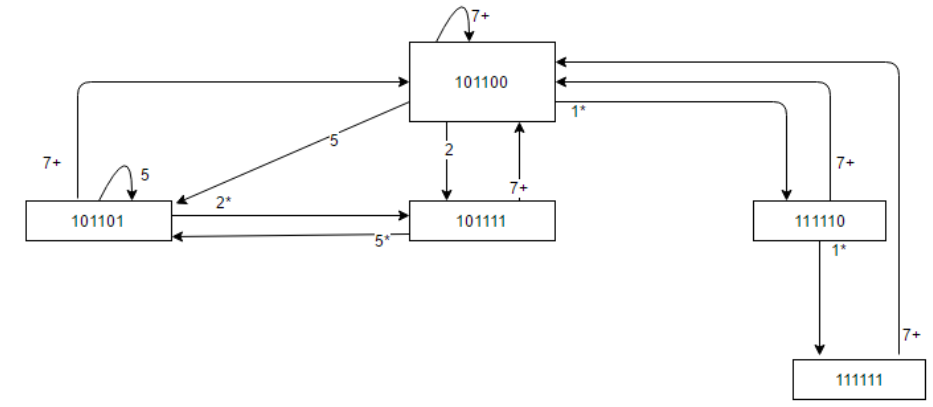
2. Consider the following reservation table. Find the all the greedy cycles and show all the steps clearly.

	1	2	3	4	5	6	7
A	X			X			X
B			X				
C		X			X		
D		X				X	

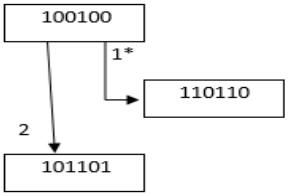
Ans:

Forbidden Latencies: 6, 4, 3 Permissible Latencies: 7, 5, 2, 1 Initial collision vector: 101100

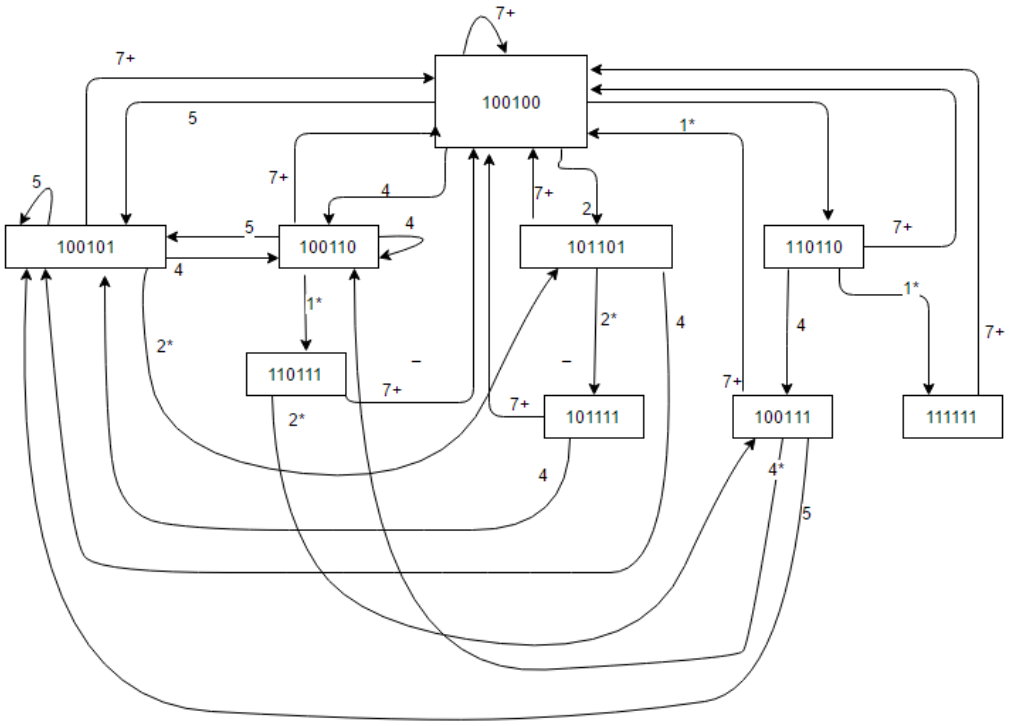
Node A: C1: 010110 101100 --- 111110 C2: 001011 101100 --- 101111 C5: 000001 101100 --- 101101	C7: 000000 101100 --- 101100 **Node B:** C5: 011111 101100 --- 111111 C7: 000000 101100 --- 101100	**Node C:** C5: 000001 101100 --- 101100 C7: 000000 101100 --- 101100 **Node D:** C2: 001011 101100 --- 101100	C5: 000001 101100 --- 101101 C7: 000000 101100 --- 101100 **Node E:** C7: 000000 101100 --- 101100	Greedy Cycle (2*, 5*) (1*,1*,7*)	



3. Complete the state transition diagram and find all simple cycles, latency cycles and greedy cycles.

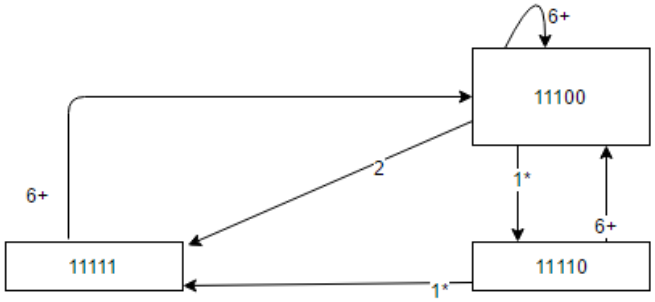


Node A:	**Node B:**	**Node D:**	**Node E:**	**Node F:**	**Node H:**
C1: 010010 100100 ---------- 110110 (B) C2: 001001 100100 ---------- 101101 (C) C4: 000010 100100 ---------- 100110 (D) C5: 000001 100100 ---------- 100101 (E) C7: 000000 100100 ---------- 100100	C1: 011011 100100 ---------- 111111 (F) C4: 000011 100100 ---------- 100111 (G) C7: 000000 100100 ---------- 100100 **Node C:** C2: 001011 100100 ---------- 101111 (H) C5: 000001 100100 ---------- 100101 C7: 000000 100100 ---------- 100100	C1: 010011 100100 ---------- 110111 (I) C4: 000010 100100 ---------- 100110 C7: 000001 100100 ---------- 100101 C7: 000000 100100 ---------- 100100	C2: 001001 100100 ---------- 101101 C4: 000010 100100 ---------- 100110 C5: 000001 100100 ---------- 100101 C7: 000000 100100 ---------- 100100	C7: 000000 100100 ---------- 100100 **Node G:** C4: 000010 100100 ---------- 100110 C5: 000001 100100 ---------- 100101 C7: 000000 100100 ---------- 100100	C5: 000001 100100 ---------- 100101 C7: 000000 100100 ---------- 100100 **Node I:** C4: 000011 100100 ---------- 100111 C7: 000000 100100 ---------- 100100
Simple Cycles: write all the cycles Latency Cycles: write all the cycles Greedy Cycles: write all the cycles					



4. Consider the following pipeline reservation table. What will the maximum throughput of this pipeline if τ=30 ns.

	1	2	3	4	5	6
A	X					X
B		X			X	
C			X			
D				X		
E		X				X



Node A:	**Node B:**	Greedy Cycle:
C1: 01110 11100 ---------- 11110 C2: 00111 11100 ---------- 11111 C6: 00000 11100 ---------- 11100	C1:01111 11100 ---------- 11111 C6: 00000 11100 ---------- 11100 **Node C:** C6: 00000 11100 ---------- 11100	(1,1,6) = 2.667-> MAL Maximum Throughput: $\frac{1}{\tau} \times \frac{1}{MAL} = \frac{1}{30 \times 10^{-9}} \times \frac{1}{2.667}$ = 12.49 MIPS

5. Three functional pipelines are characterized by the following reservation tables. Using these three pipelines a composite pipeline is formed. Each task going through this composite pipeline in the following order: f1 first, f2 and f3 next, f1 again and then the output is obtained. Draw the reservation table for the composite pipeline and determine the MAL associated with the shortest greedy cycle.

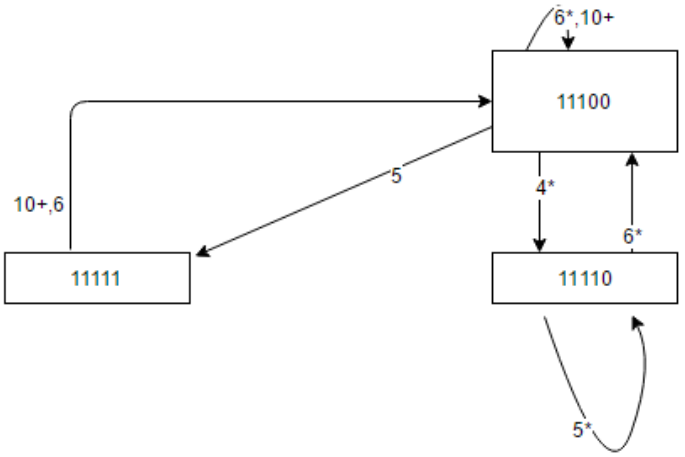
	1	2	3	4
S1	X			
S2		X		
S3			X	X

	1	2	3	4
T1	X			X
T2		X		
T3			X	

	1	2	3	4
U1	X		X	
U2				X
U3		X		

	1	2	3	4	5	6	7	8	9	10	11	12
S1	X								X			
S2		X								X		
S3			X	X							X	X
T1					X			X				
T2						X						
T3							X					
U1					X		X					
U2								X				
U3						X						

FL = 9,8,7,3,2,1 PL = 6,5,4 ICV=111000111



Node A: C4: 000011100 111000111 ---------- 111011111 C5: 000001110 111000111 ---------- 111001111 C6: 000000111 111000111 ---------- 111000111 C10: 00000000 111000111 ---------- 111000111	**Node B:** C6: 000000111 111000111 ---------- 111000111 C10: 000000000 111000111 ---------- 111000111 **Node C:** C5: 000001110 111000111 ---------- 111001111 C6: 000000111 111000111 ---------- 111000111	C10: 000000000 111000111 ---------- 111000111	Greedy Cycle (4*, 6*) = 5 (5*) = 5 MAL associated with shortest greedy cycle is 5

6. Find the sum of the numbers given below using an array of 16 PEs. Write the algorithm and the masking scheme for the same.

12 23 21 43 21 13 15 4 6 10

Since n=10, it requires $\lceil \log_2 10 \rceil$ steps i.e., 4 steps to find the sum

PE0	12	12	12	12	12
PE1	23	23+12=35	35	35	35
PE2	21	21+23=44	44+12=56	56	56
PE3	43	43+21=64	64+35=99	99	99
PE4	21	21+43=64	64+44=108	108+12=120	120
PE5	13	13+21=34	34+64=98	98+35=133	133
PE6	15	15+13=28	28+64=92	92+56=148	148
PE7	4	4+15=19	19+34=53	53+99=152	152
PE8	6	6+4=10	10+28=38	38+108=146	146+12=158
PE9	10	10+6=16	16+19=35	35+98=133	133+35=**168**
PE10					
PE11					
PE12					
PE13					
PE14					
PE15					
		Step1	Step2	Step3	Step4

Algorithm with masking scheme:

Step 1:	Step 2:	Step 3:	Step 4:
Ai→Ri i=0..8 Ri→Ri+1 i=0..8 Ai+Ri→Ai i=1..9	Ai→Ri i=0..7 Ri→Ri+2 i=0..7 Ai+Ri→Ai i=2..9	Ai→Ri i=0..5 Ri→Ri+1 i=0..5 Ai+Ri→Ai i=4..9	Ai→Ri i=0..1 Ri→Ri+1 i=0..1 Ai+Ri→Ai i=8..9

Masking Scheme:

During Data Routing:	**During Addition:**
Step 1: PE9, PE10, PE11, PE12, PE13, PE14, PE15	Step 1: PE0, PE10, PE11, PE12, PE13, PE14, PE15
Step 2: PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15	Step 2: PE0, PE1, PE10, PE11, PE12, PE13, PE14, PE15
Step 3: PE6, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15	Step 3: PE0, PE1, PE2, PE3, PE10, PE11, PE12, PE13, PE14, PE15
Step 4: PE2, PE3, PE4, PE5, PE6, PE7, PE 8, PE9, PE10, PE11, PE12, PE13, PE14, PE15	Step 4:PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7, PE10, PE11, PE12, PE13, PE14, PE15