Trinity College Dublin
Coláiste na Tríonóide, Baile Átha Cliath
The University of Dublin

Declaration concerning plagiarism

I have read and I understand the plagiarism provisions in the General Regulations of the *University Calendar* for the current year, found at http://www.tcd.ie/calendar

I have completed the Online Tutorial in avoiding plagiarism 'Ready, Steady, Write', located at http://tcd-ie.libguides.com/plagiarism/ready-steady-write

STUDENT NUMBER: 21355131

SIGNED:.....

DATE: 04.12.2021

ASSIGNMENT-2
Digital System Design

Prachi Singhroha
Student Number: 21355131

Introduction:

This lab uses codes from Lab F and G. The assignment has following modules:

- display: it takes output from counter and displays on the board
- counter: takes signal from fsm, add 1 to the counter and convert into 4 digit decimal number
- fsm: reads bitstream from LFSR and uses Moore machine to detect the given pattern.
- LFSR
- clock: takes signal from pin W5 and then divide it by clkscale to get the required value of clock
- top (which instantiates the above modules)
- testebenches for fsm, LFSR and top

Labelled Waveforms and screen grabs

- LFSR

Given:

-> LFSR width = 20

-> LFSR seed = 10011001101000100000

The output waveform looks like following:

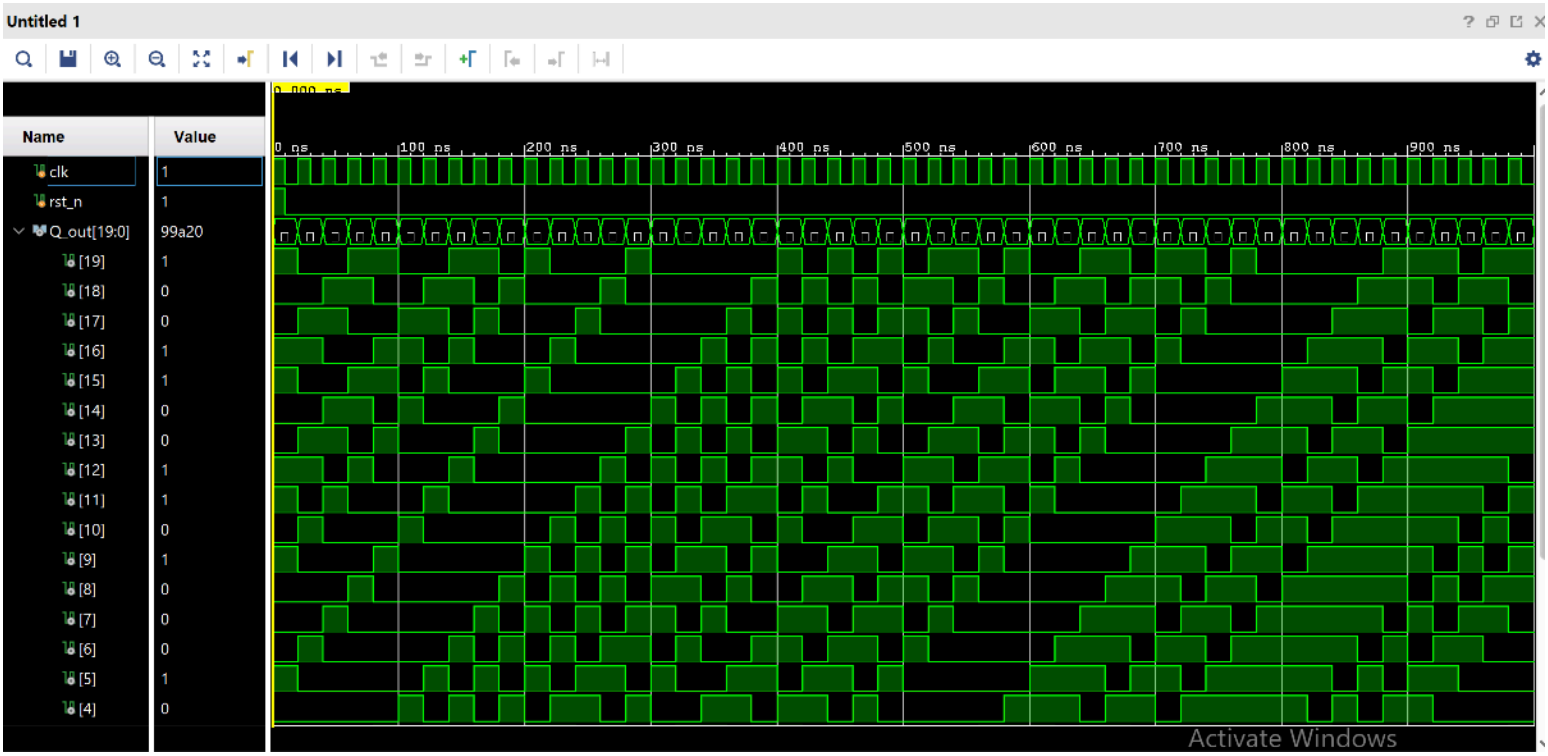

Figure 2.1

To get the above waveform:

- start new project
- Add LFSR.v and testbench.v from the zip file
- Run simulation and you'll get the above waveform

- FSM

The output waveform looks like following:

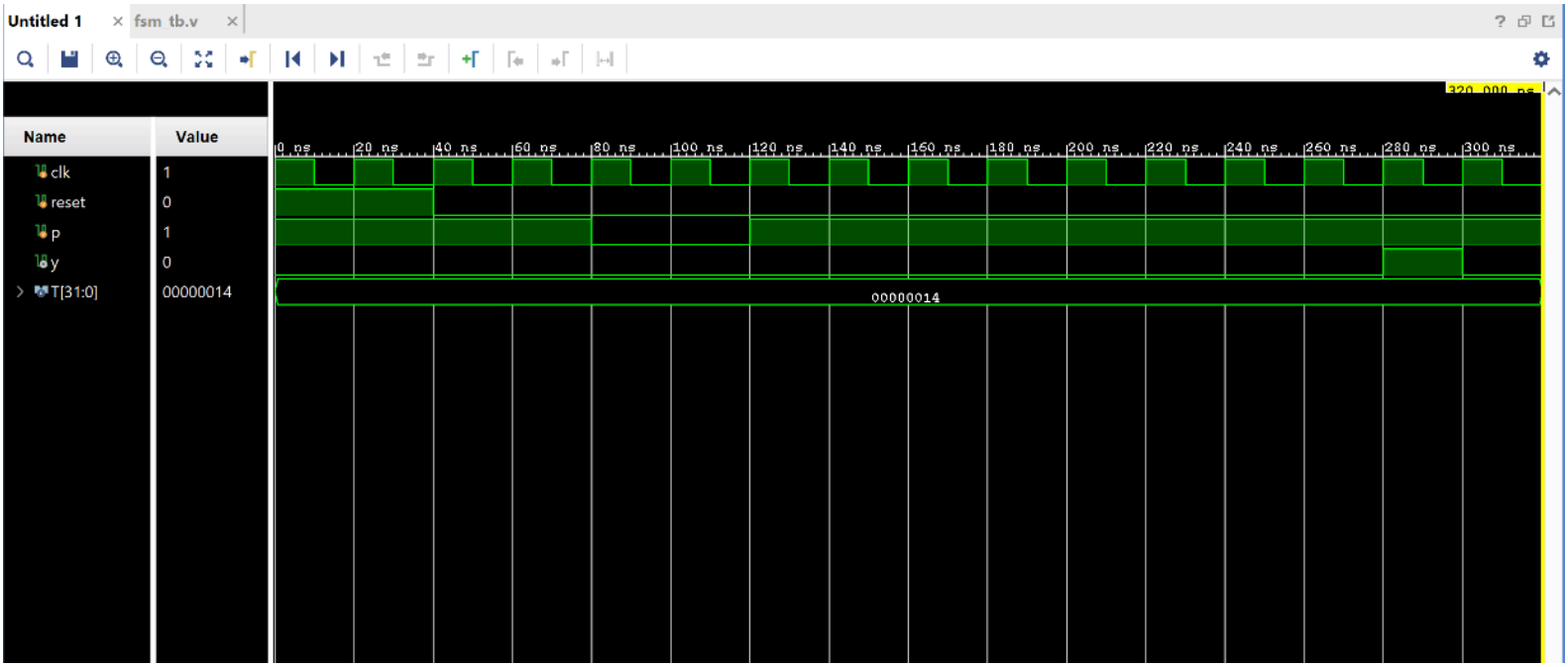

Figure 2.2

To get the above waveform:

- start new project
- Add fsm.v and fsm_tb.v from the zip file
- Run simulation and you'll get the above waveform

- Sequence detector

The output waveform looks like following:

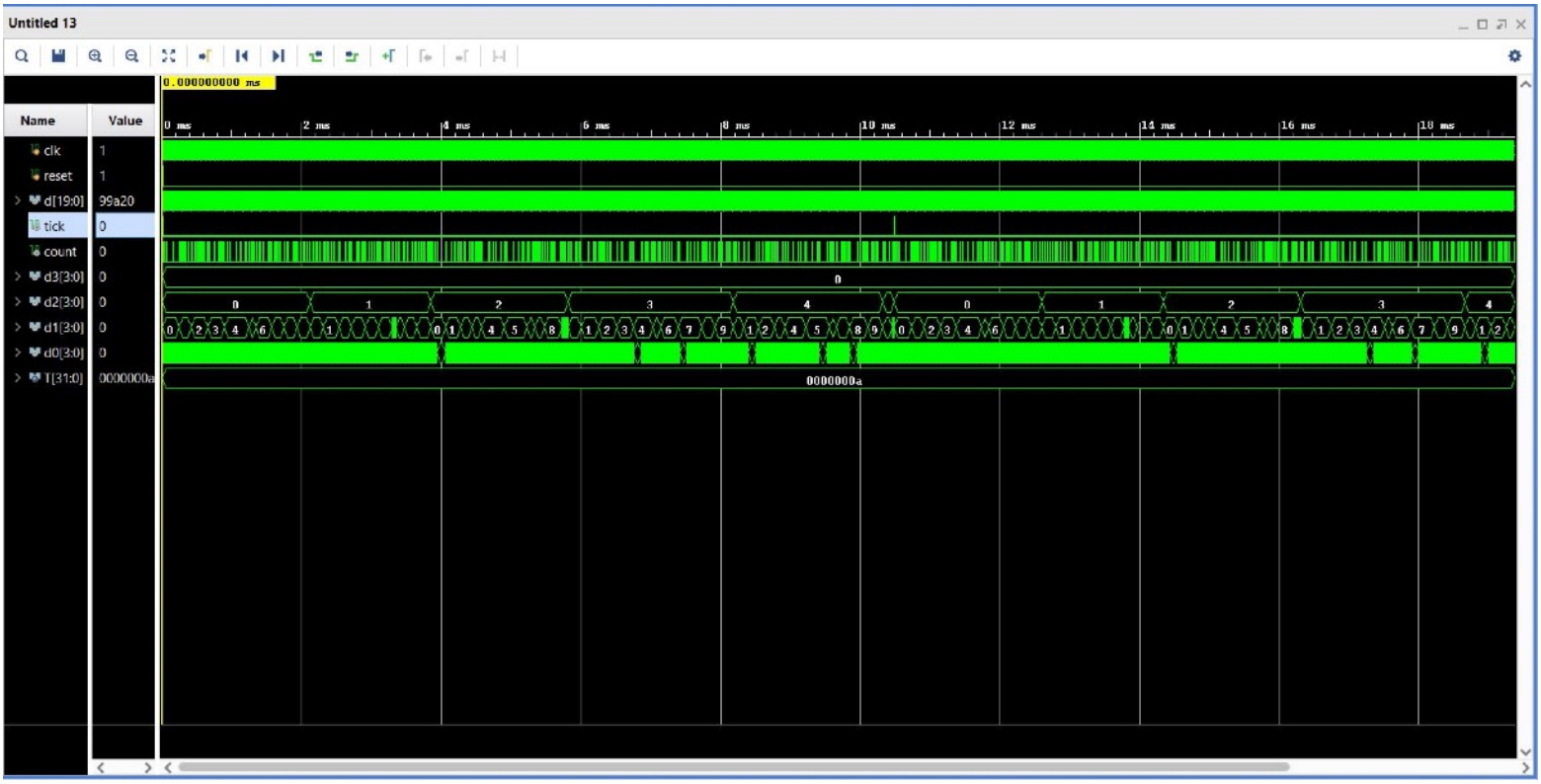

Figure 2.2

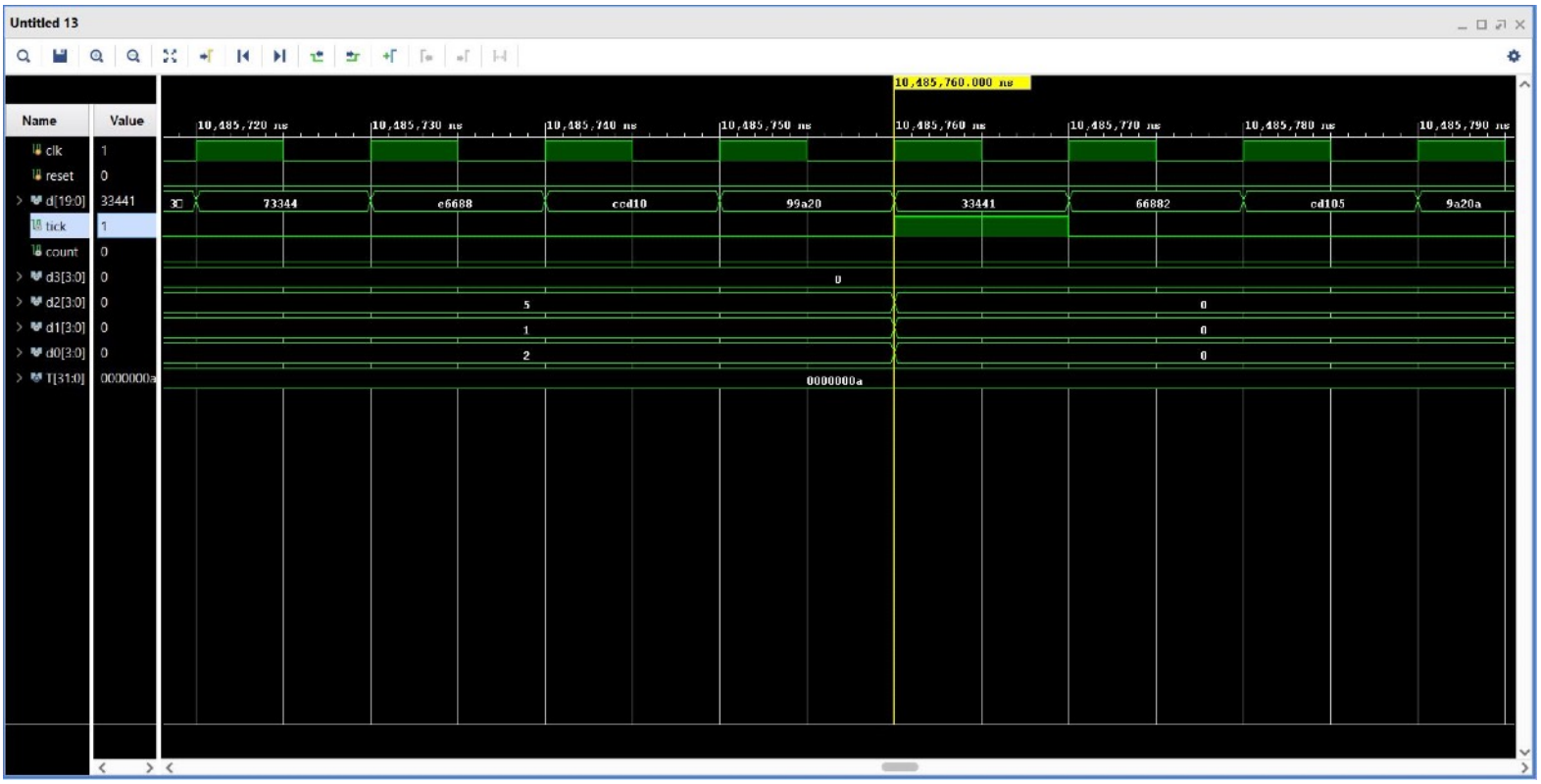

Figure 2.3 (From above waveform we can see that the value of max_tick is 512 i.e. pattern repeats itself every 512 times)

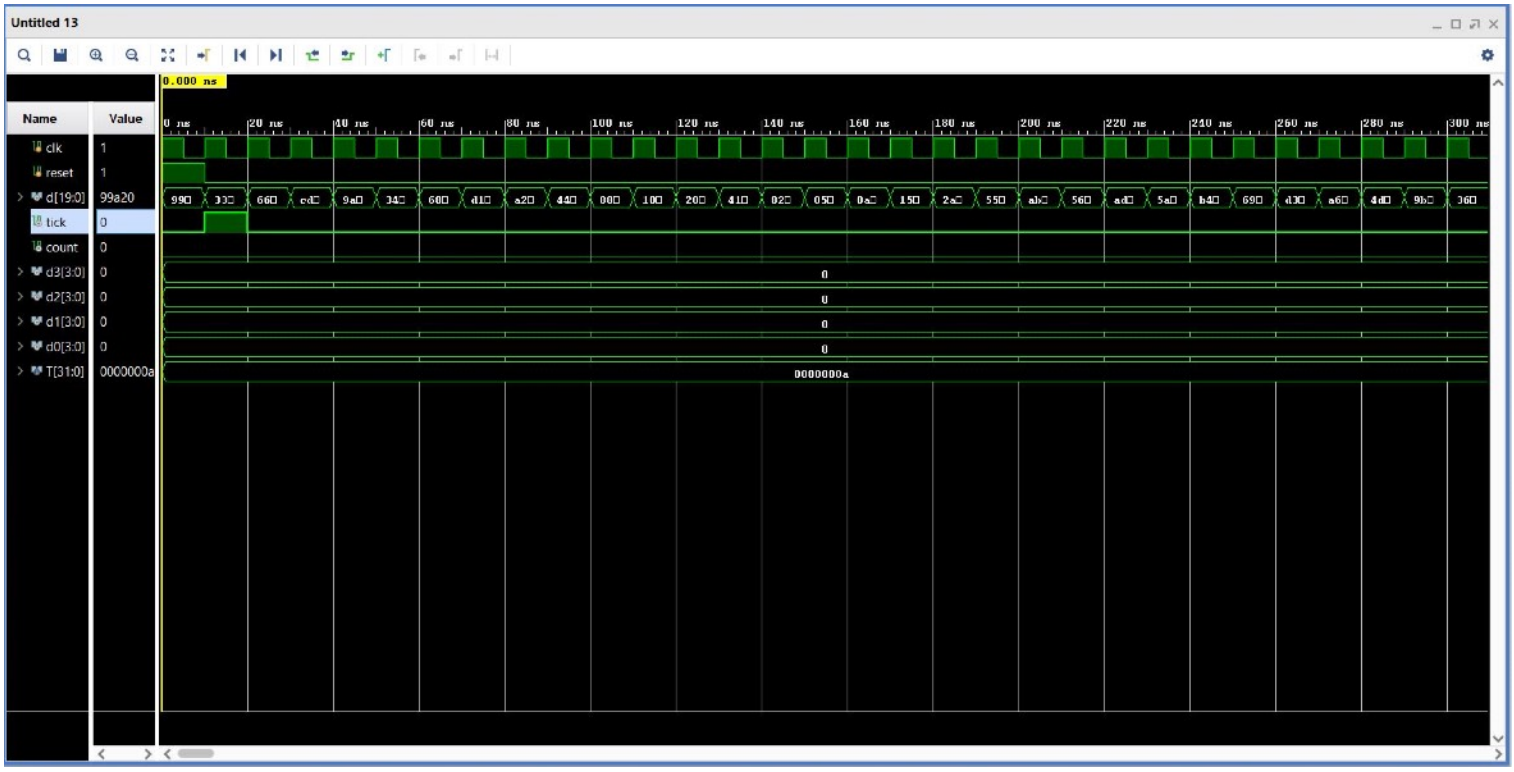

Figure 2.4

To get the above waveform:

- start new project named ‘Assignment2’
- Add the following files:
    - clock.v
    - LFSR.v
    - fsm.v
    - display.v
    - counter.v
    - tb.v
    - tb_.v
- Run simulation and you’ll get the above waveforms

Demo

Following are some pictures of how my board looks like after programming the board:

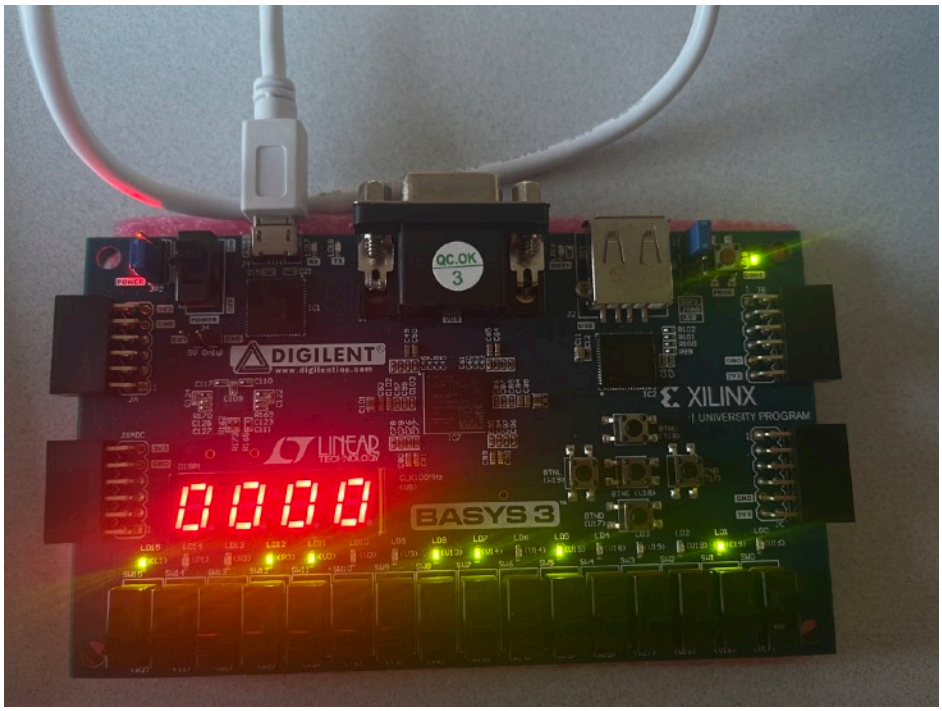

Figure 2.5

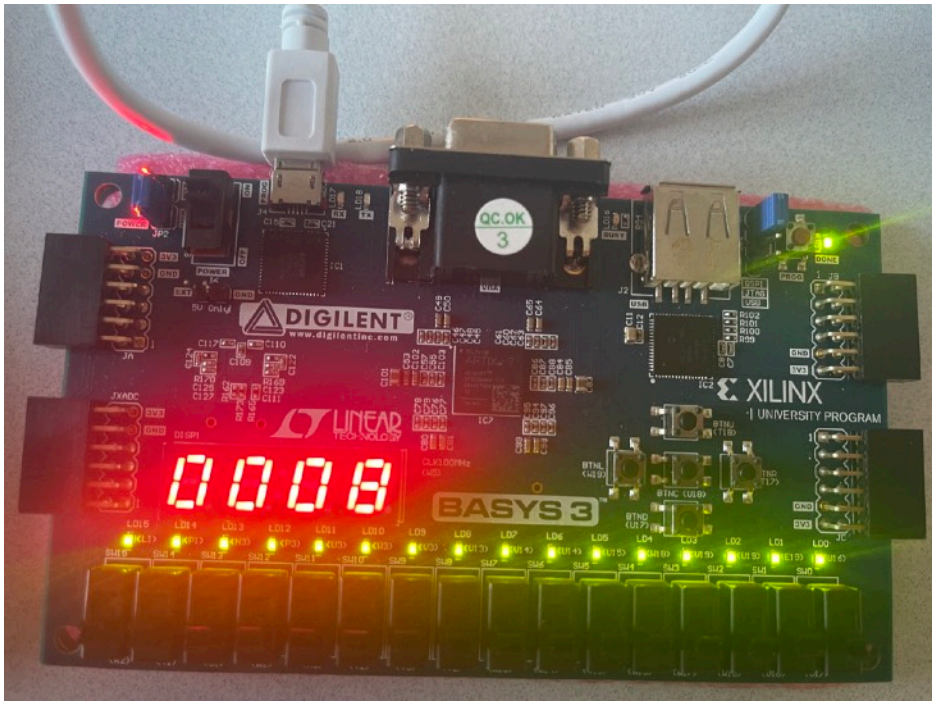

Figure 2.6

Following are hyperlinks of videos showing my working on the board:

1. *Video1*: the output on the LED runs till 512 hits the display and then resets to zero as it has hit 2^N-1 cycles.
2. *Video 2*: it shows that the value on led resets itself when you switch ON the clock on the board which set at pin U16 in my code.

To get the above output on the board:

- In the above created project 'Assignment2' and change the codes as directed in the comments.
- Add FINAL.xdc from the Assign2_singhrohap_codes.zip file
- Now synthesize and implement the design by clicking on Run Synthesis and Run Implementation button in Flow Navigator panel.
- Next Click on Generate Bitstream process located in Flow Navigator panel and choose testbench.bit file located in the same .zip file.
- Now choose Open Hardware Manager and program the device.
- You'll be able to see the above output on the board.

Functional diagram:

41 Cells 34 I/O Ports 78 Nets

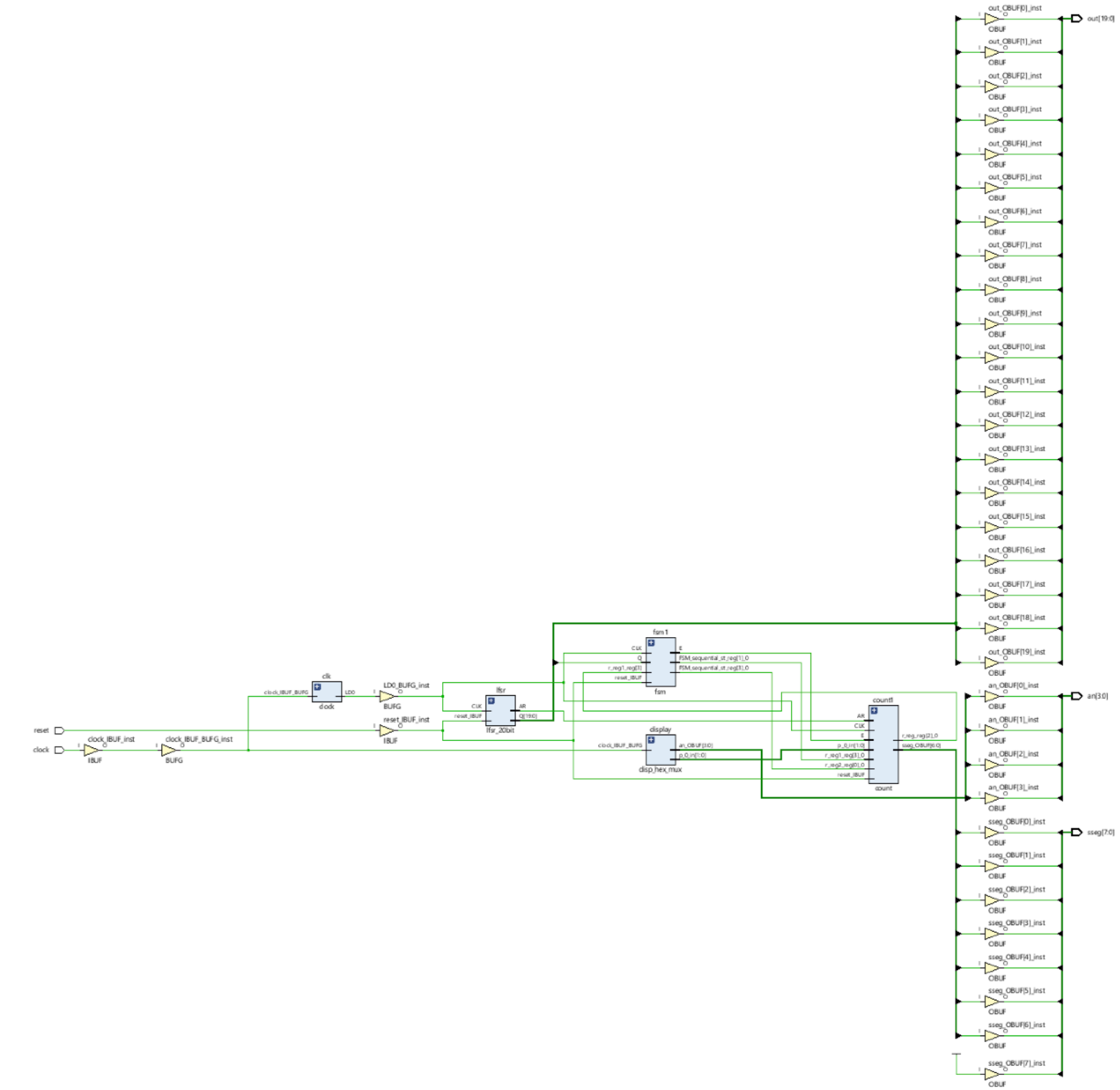

Figure 2.7

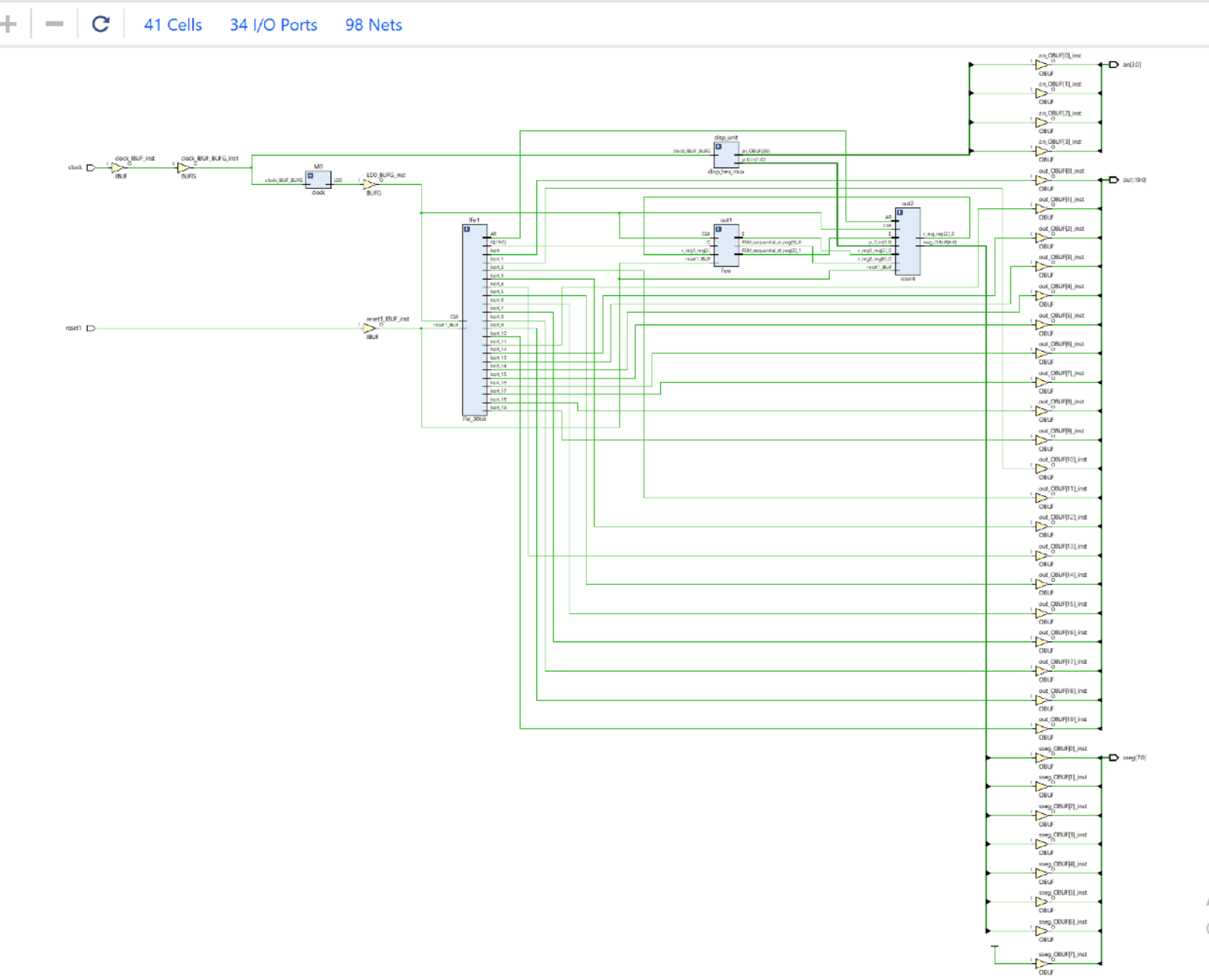

Figure 2.8

FSM design using Moore Model:

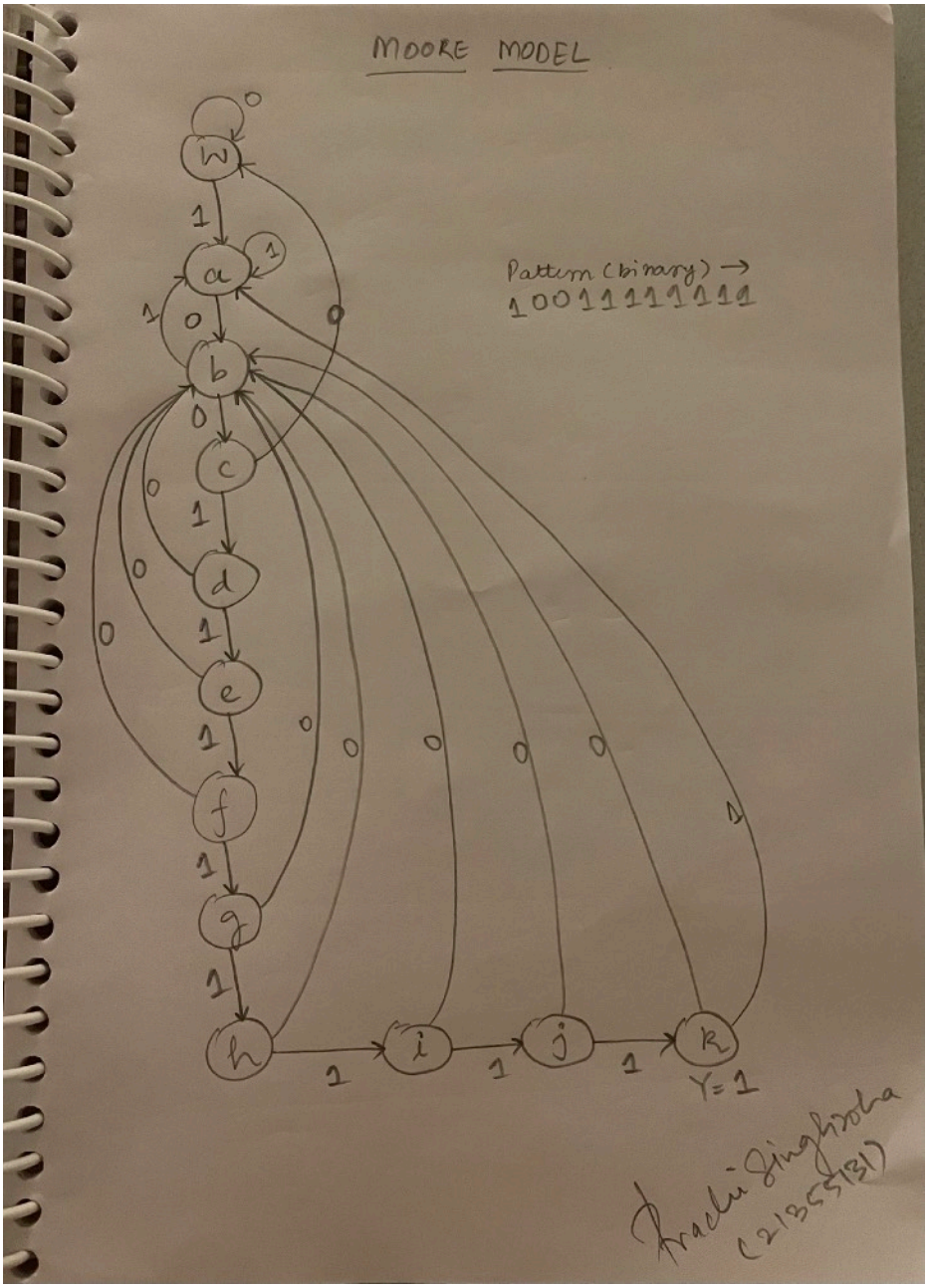

Figure 2.9

Hierarchy of files:

- To get the waveform

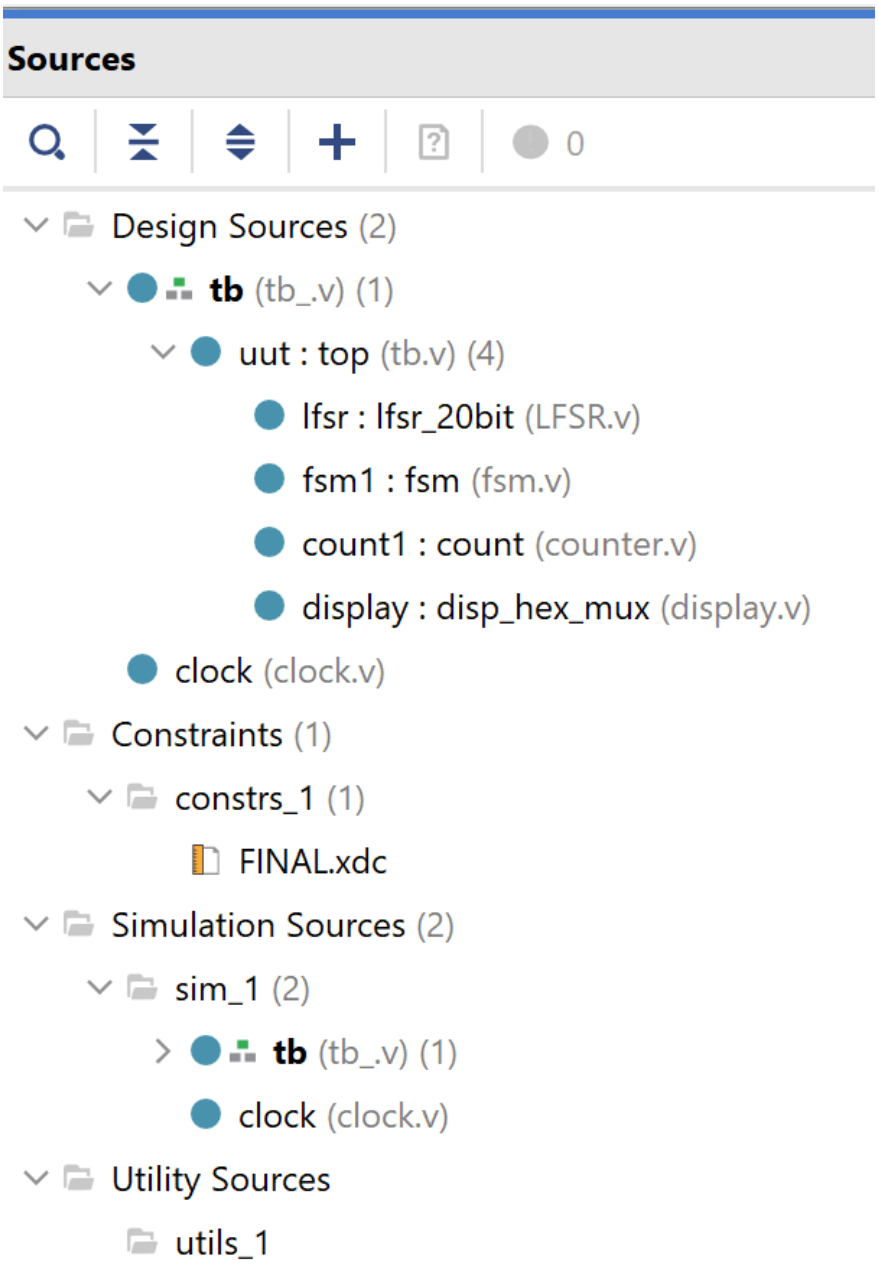

Figure 2.10

- To get run on the board

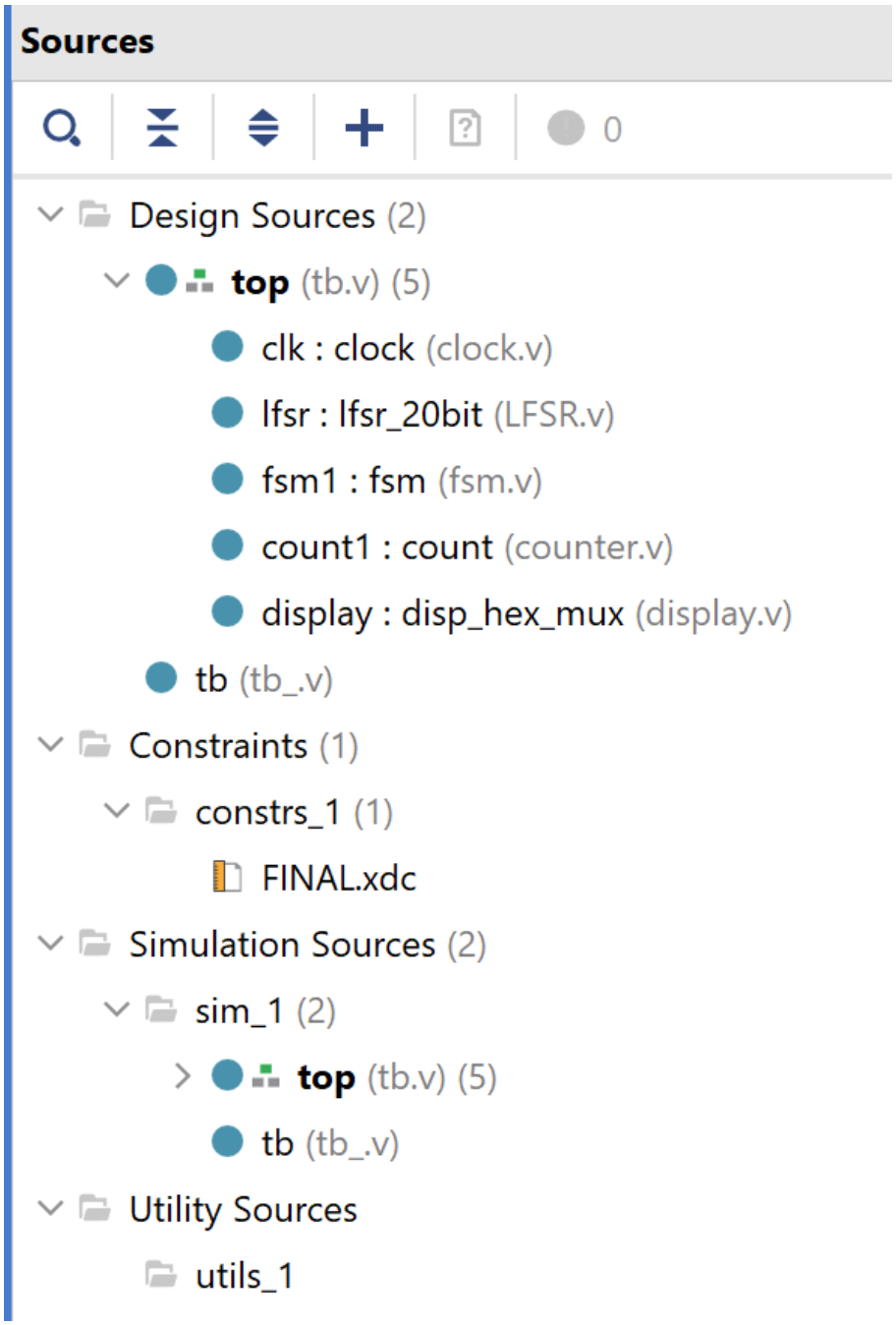

Figure 2.11

Utilisation Report

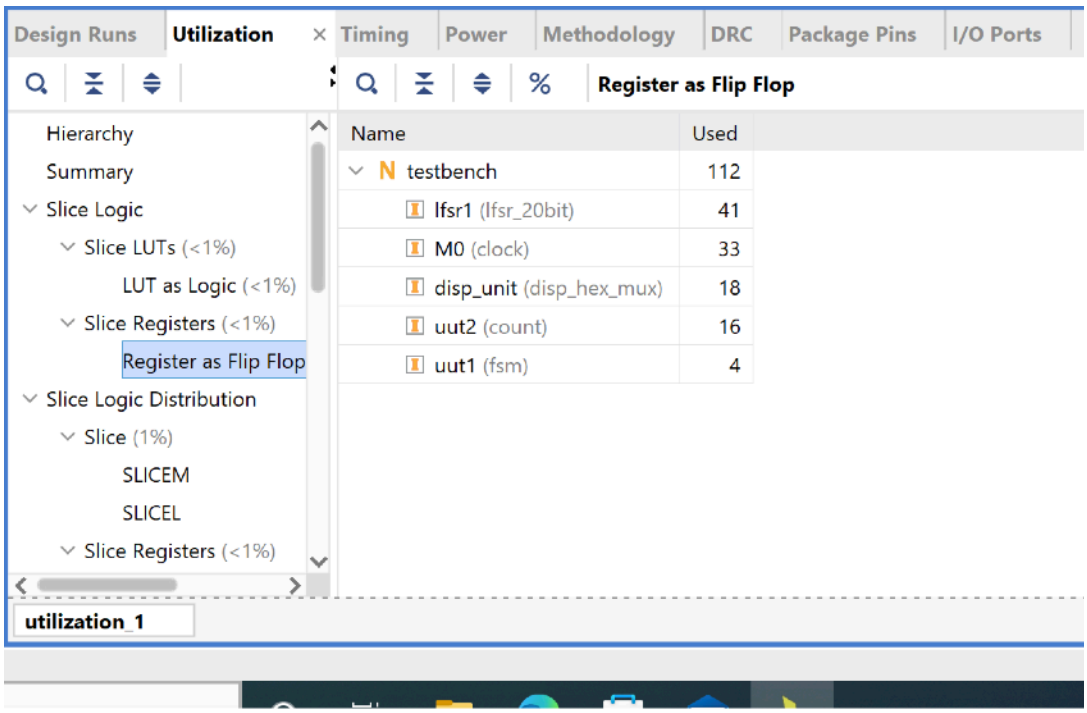

Figure 2.12

Clock Declaration:

```
set_property IOSTANDARD LVCMOS33 [get_ports clock]
set_property IOSTANDARD LVCMOS33 [get_ports reset1]
set_property PACKAGE_PIN V17 [get_ports reset1]
set_property PACKAGE_PIN W5 [get_ports clock]
```

Figure 2.13

References

1. Lecture 6 and 7 slides
2. .zip files given for Lab F and G
3. Chu book