Thapar Institute of Engineering and Technology, Patiala
Department of Electronics & Communication Engineering
Department of Computer Science Engineering
B.E. (2nd Year) (IV-Semester) (Jan-June, 2021)
Course: Engineering Design Project II (UTA014)

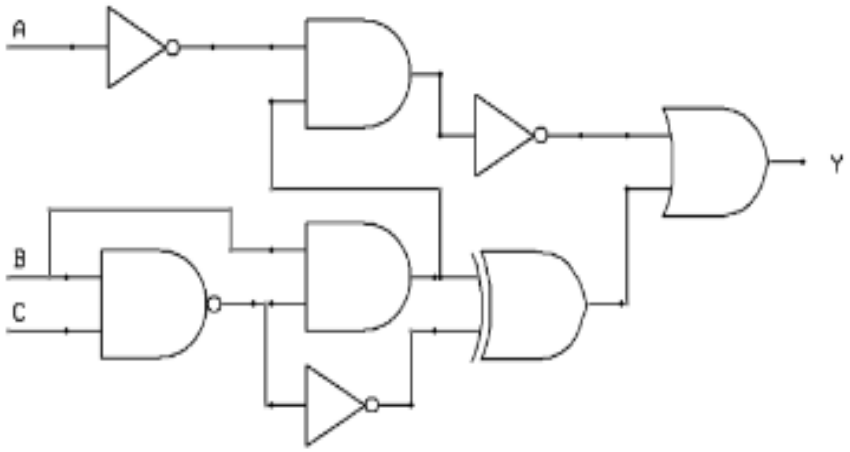
Submission guidelines of assignment-3B (CSED)

- Assignment must be submitted by each student individually. You are restricted to submit assignment on Google form only once.
- The last date of submission is **June 10, 2021.**
- A maximum weightage of this assignment is of **10 marks** (Weightage to overall evaluation will be decided later).
- Assignment must be **typed form** with neat diagram (**3-4 pages preferably**) and the student is required to submit a scan copy (**pdf, up to 1 MB**) of his assignment.
- Marks will be deducted if submitted after the due date of submission.
- Assignment copied from other students will be treated as the case of plagiarism and marks will be deducted from the entire copied version (s).

Assignment-3B (CSED)

Write program for **Any One** of the following questions: (10 marks)

Q1. Write an optimized arduino program to implement following logic circuit using truth table entries and all input values must be provided through serial monitor.



Q2. Write an arduino program to perform the XOR and X-NOR logic gates with 3 inputs using truth table entries and all input values must be provided through serial monitor.

The soft copy of individual **report MUST** include:

- Student Name, Roll No., Batch
- Experiment Number and Name
- Programming Code and,
- Others relevant information about experiment.

Assignment submission Link: https://forms.gle/b8vow6ZsSV5bULHs7