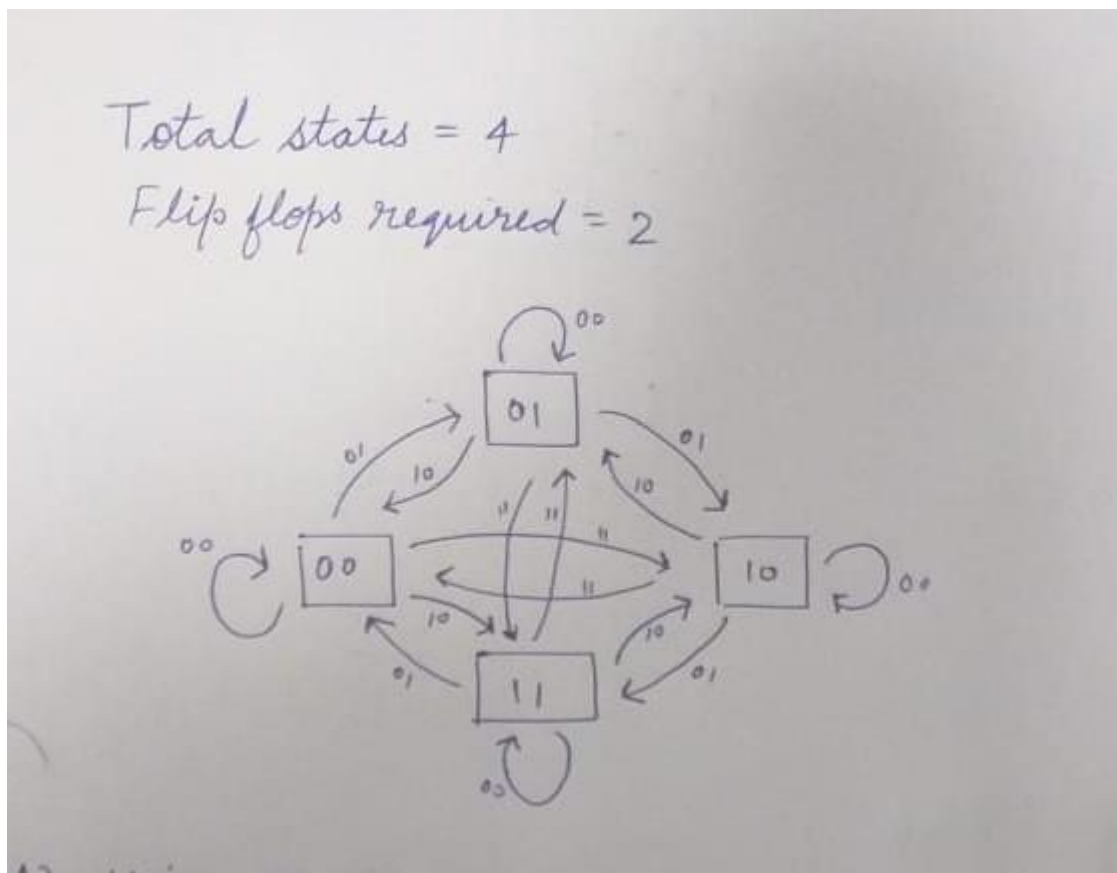


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LAB-10

Q1)



a) Using T Flip Flop

(A) Using T flip flop

C_0	C_1	Q_1	Q_0	Q_1^*	Q_0^*	T_1	T_0
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0
0	0	1	1	1	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	1	0	1	1
0	1	1	0	1	1	0	1
0	1	1	1	0	0	1	1
1	0	0	0	1	1	1	1
1	0	0	1	0	0	0	1
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	1
1	1	0	0	1	0	1	0
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	0
1	1	1	1	0	1	1	0

$Q_1 Q_0$

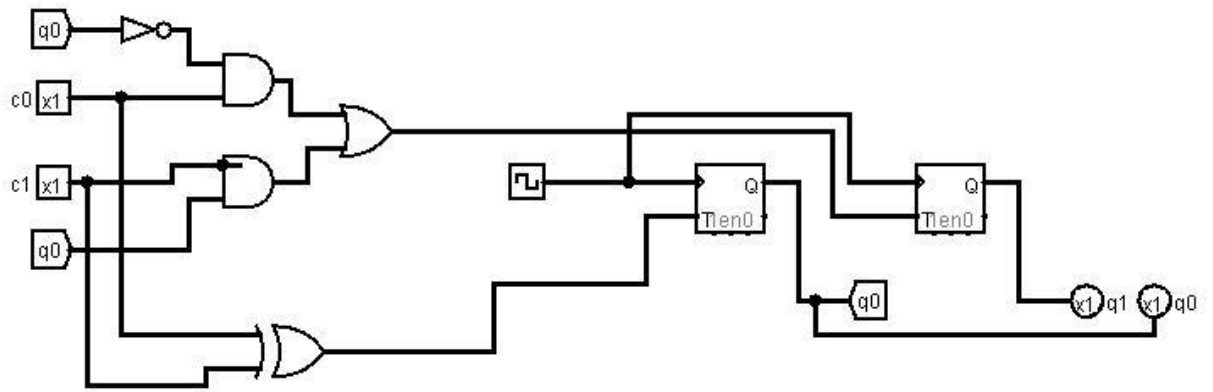
$C_0 C_1$	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	1	1	1	1
10	1	0	0	1

$$T_1 = \overline{C_0} Q_1 + C_1 Q_0 + C_0 \overline{Q_0}$$

$Q_1 Q_0$

$C_0 C_1$	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

$$T_0 = C_0 \oplus C_1$$



b) Using D flip flop

B) Using D flip flop.

C_0	C_1	S_1	S_0	N_1	N_0	D_1	D_0
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0
0	0	1	1	1	1	1	1
0	1	0	0	0	1	0	1
0	1	0	1	1	0	1	0
0	1	1	0	1	1	1	1
0	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1
1	0	0	1	0	0	0	0
1	0	1	0	0	1	0	1
1	0	1	1	1	0	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	1	1	1
1	1	1	0	0	0	0	0
1	1	1	1	0	1	0	1

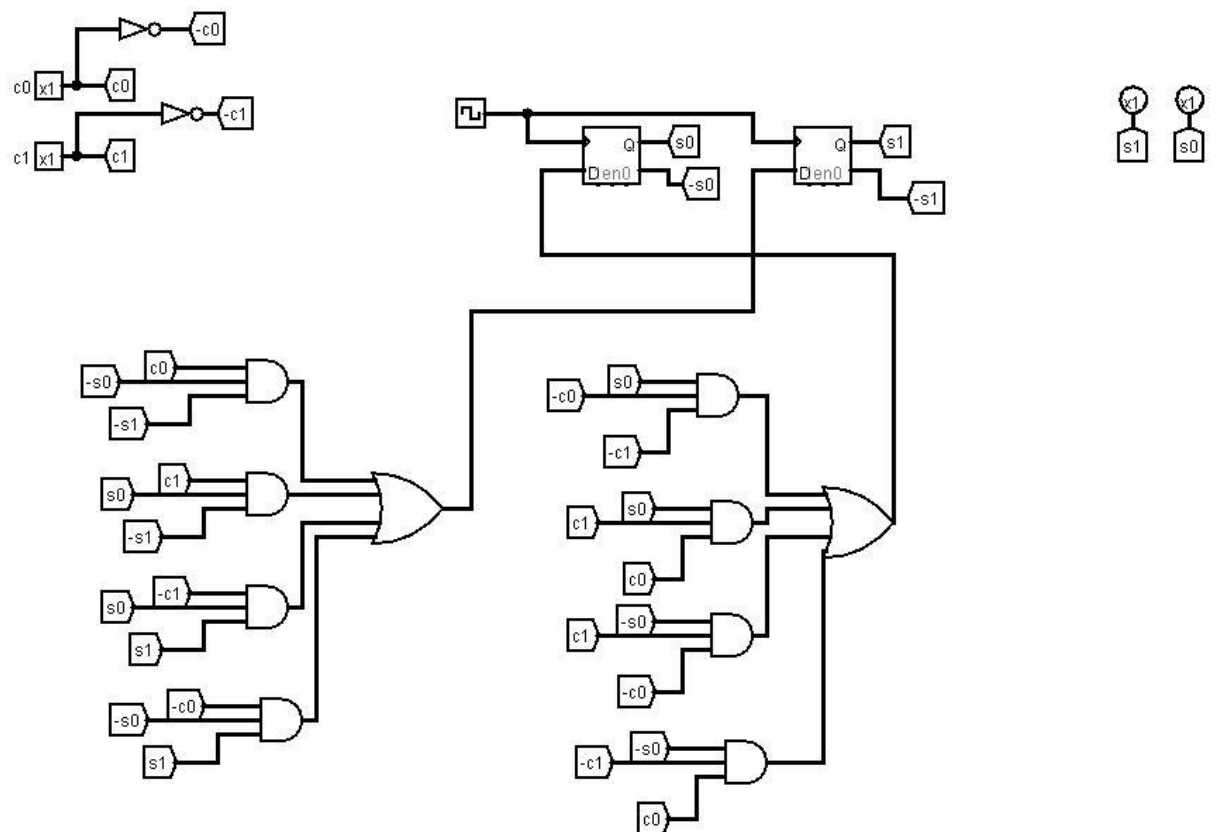
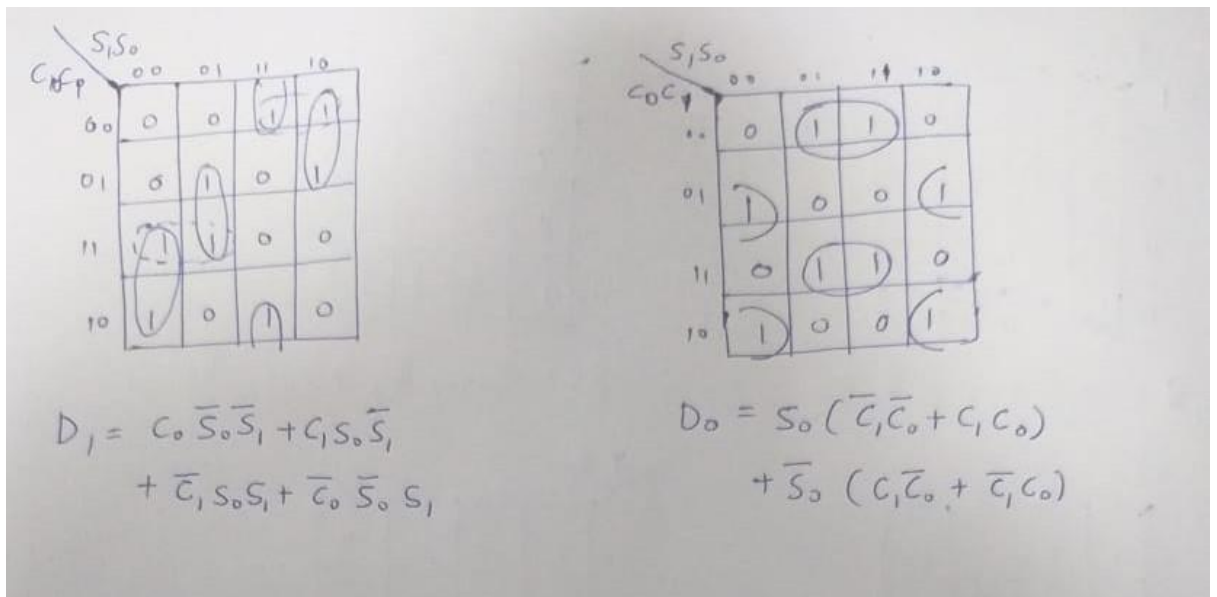


Fig.2 used d flip flop

c) Using SR Flip flop

(C) Using S-R Flip flop.

C_0	C_1	Q_1	Q_0	Q_1^*	Q_0^*	S_1	R_1	S_0	R_0
0	0	0	0	0	0	0	X	0	X
0	0	0	1	0	1	0	X	X	0
0	0	1	0	1	0	X	0	0	X
0	0	0	0	1	1	X	0	X	0
0	1	0	0	0	1	0	X	1	0
0	1	0	1	1	0	1	0	0	1
0	1	1	0	1	1	X	0	1	0
0	1	1	1	0	0	0	1	0	1
1	0	0	0	1	1	1	0	1	0
1	0	0	1	0	0	0	X	0	1
1	0	1	0	0	1	0	1	1	0
1	0	1	1	1	0	X	0	0	1
1	1	0	0	1	0	1	0	0	X
1	1	0	1	1	1	1	0	X	0
1	1	1	0	0	0	0	1	0	X
1	1	1	1	0	1	0	1	X	0

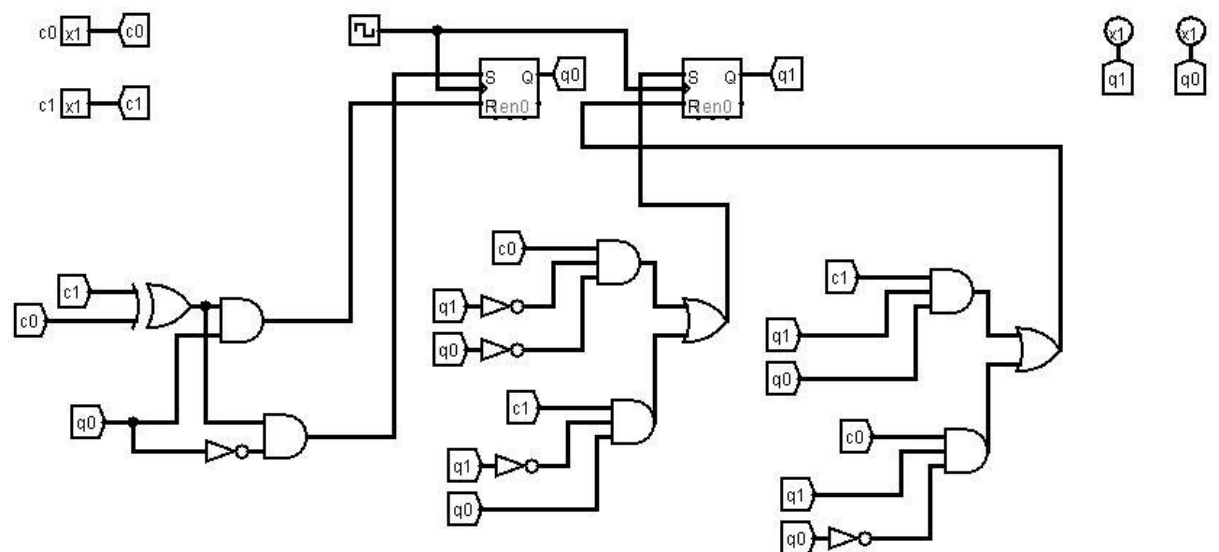
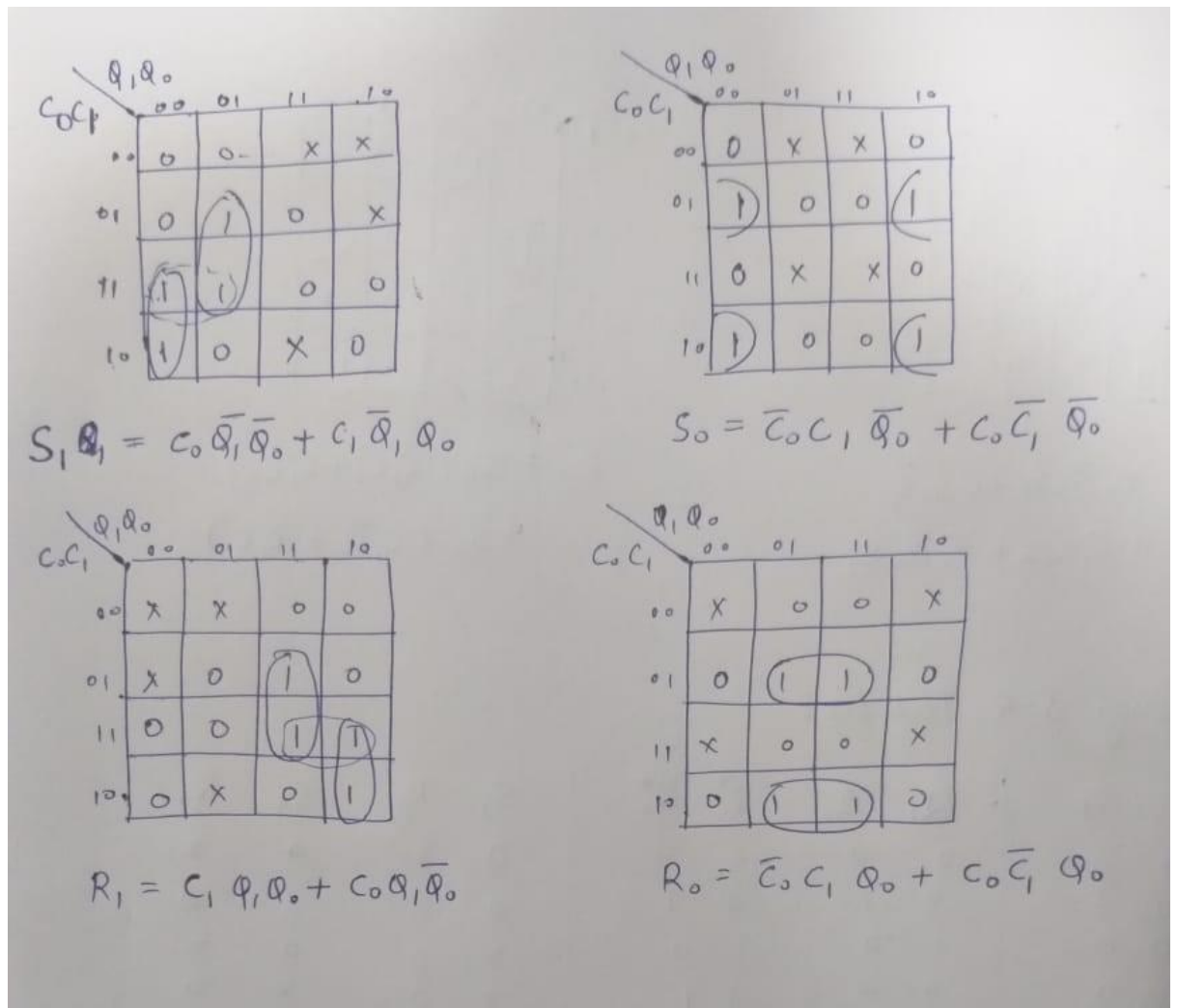


Fig.3 used SR flip flop

d) Using JK Flip Flop

(D) Using J-K flip flop.

C_0	C_1	Q_1	Q_0	Q_1^*	Q_0^*	J_1	K_1	J_0	K_0
0	0	0	0	0	0	0	x	0	x
0	0	0	1	0	1	0	x	x	0
0	0	1	0	1	0	x	0	0	x
0	0	1	1	1	1	x	0	x	0
0	1	0	0	0	1	0	x	1	x
0	1	0	1	1	0	1	x	x	1
0	1	1	0	1	1	x	0	1	x
0	1	1	1	0	0	x	1	x	1
1	0	0	0	1	1	1	x	1	x
1	0	0	1	0	0	0	x	x	1
1	0	1	0	0	1	x	1	1	x
1	0	1	1	1	0	x	0	x	1
1	1	0	0	1	0	1	x	0	x
1	1	0	1	1	1	1	x	x	0
1	1	1	0	0	0	x	1	0	x
1	1	1	1	0	1	x	1	x	0

$C_0 C_1$	$Q_1 Q_0$	00	01	11	10
00		0	0	x	x
01		0	1	x	x
11		1	1	x	x
10		1	0	x	x

$$J_1 = C_0 \bar{Q}_0 + C_1 Q_0$$

$C_0 C_1$	$Q_1 Q_0$	00	01	11	10
00		0	x	x	0
01		1	x	x	1
11		0	x	x	0
10		1	x	x	1

$$J_0 = \bar{C}_0 C_1 + C_0 \bar{C}_1$$

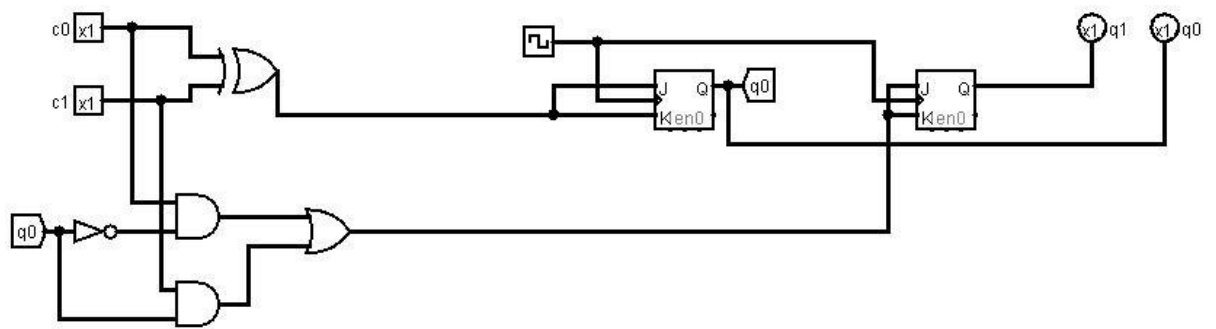
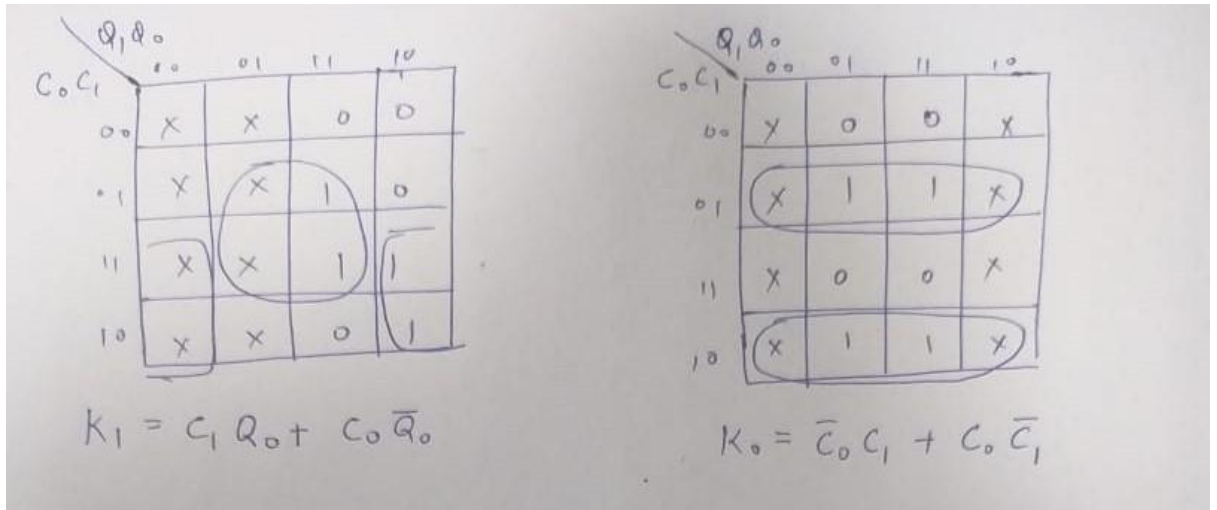
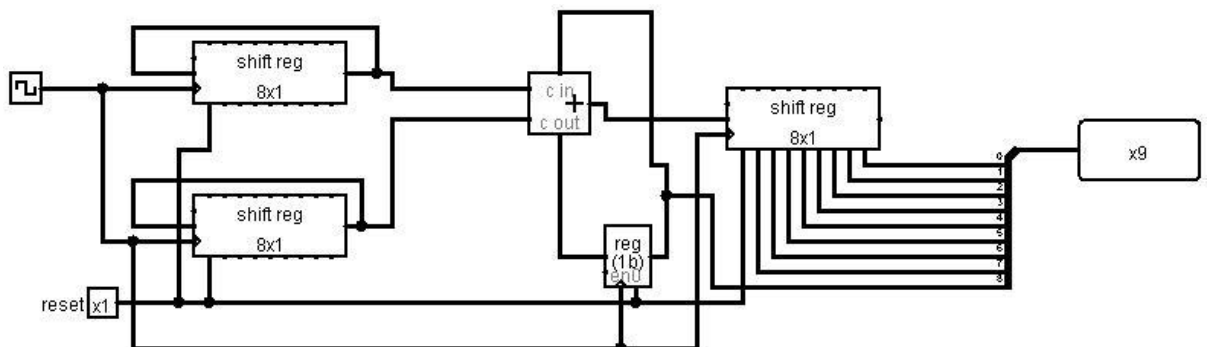


Fig.4 used JK flip flop

Q2) 8-bit adder using shift registers and a full adder.



In above circuit it will require 8 clock pulses for complete addition $Y = A + B$

If we use a FA which is capable of adding more no. of bits then consequently no. of clock pulses required will reduce proportionally

Q3) 4-bit counter using two 2-bit counters.

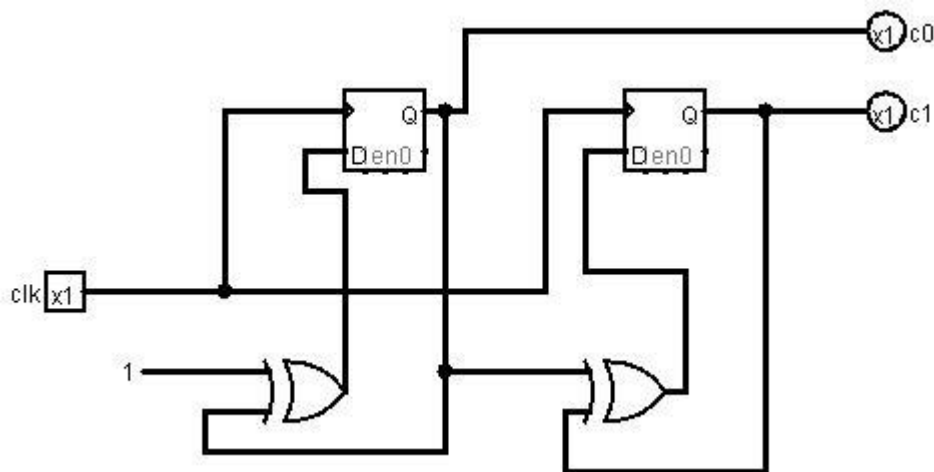


Fig 2bit counter using d flip flop

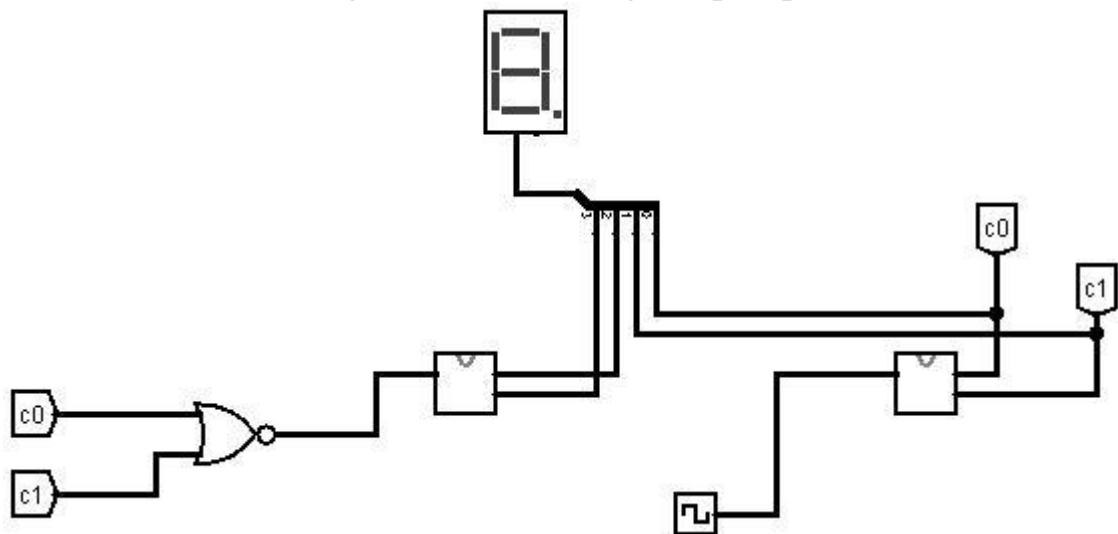


Fig 4 bit counter using two 2 bit counters

Just for the counter representing Most significant bits we have to reduce frequency to $\frac{1}{4}$ of the other.

This can be done if clock for the MSB counter is made by taking a NOR of two LSBs.