EE663: Frequency Synthesizers, Clock and Data Recovery circuits

Course Project

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Entry No: 2023EEM1026

April 5, 2024

Objective:Design a phase-locked loop (PLL) that meets the given criteria, including all sub-blocks (phase frequency detector, voltage-controlled oscillator, loop filters, and divider) using Verilog models and transistor level in Cadence design suit.

1 Introduction

A phase-locked loop (PLL) is a circuit designed to align the output signal of an oscillator with a reference or input signal, ensuring synchronization in both frequency and phase within a given system. In the synchronized or locked state, the phase error between the output signal of the oscillator and the reference signal is either zero or remains constant. If a phase error accumulates, a control mechanism intervenes to minimize the phase error by acting on the oscillator. In this control system, the phase of the output signal becomes locked to the phase of the reference signal, hence the term "phase-locked loop." The project aims to develop a square-wave output frequency generator, primarily utilizing the PLL as a frequency multiplier, achieved by multiplying the frequency of the reference oscillator

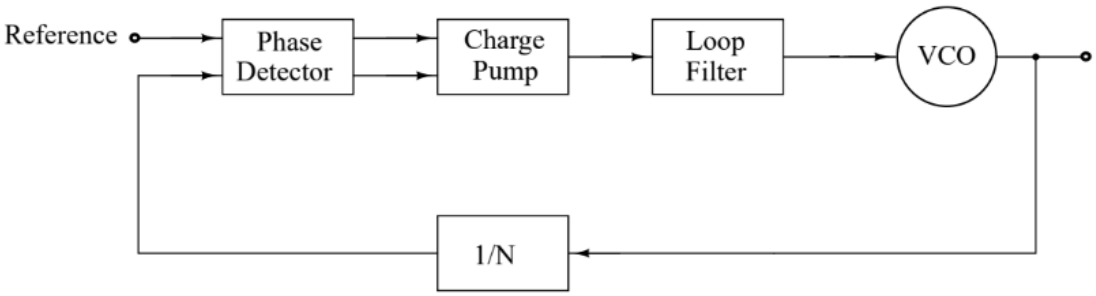

Figure 1: block diagram of PLL

2 Design of Phase Frequency Detector (PFD)

In a PLL, the phase-frequency detector serves the crucial function of comparing the phases of the reference signal and the feedback signal. This detector transforms the phase difference into a voltage (or current), which is subsequently processed through a Low-Pass Filter (LPF) before being converted into the phase for the Voltage-Controlled Oscillator (VCO).

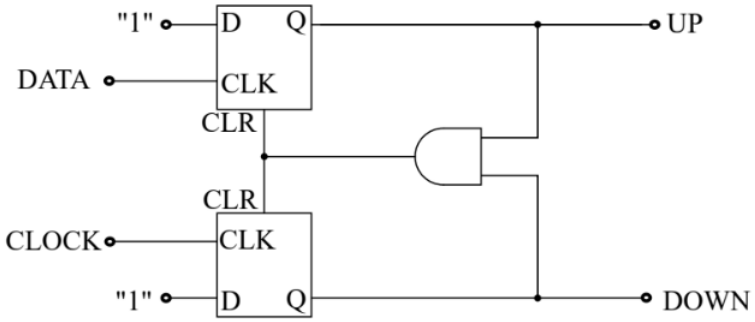

Figure 2: Circuit for phase frequency detector

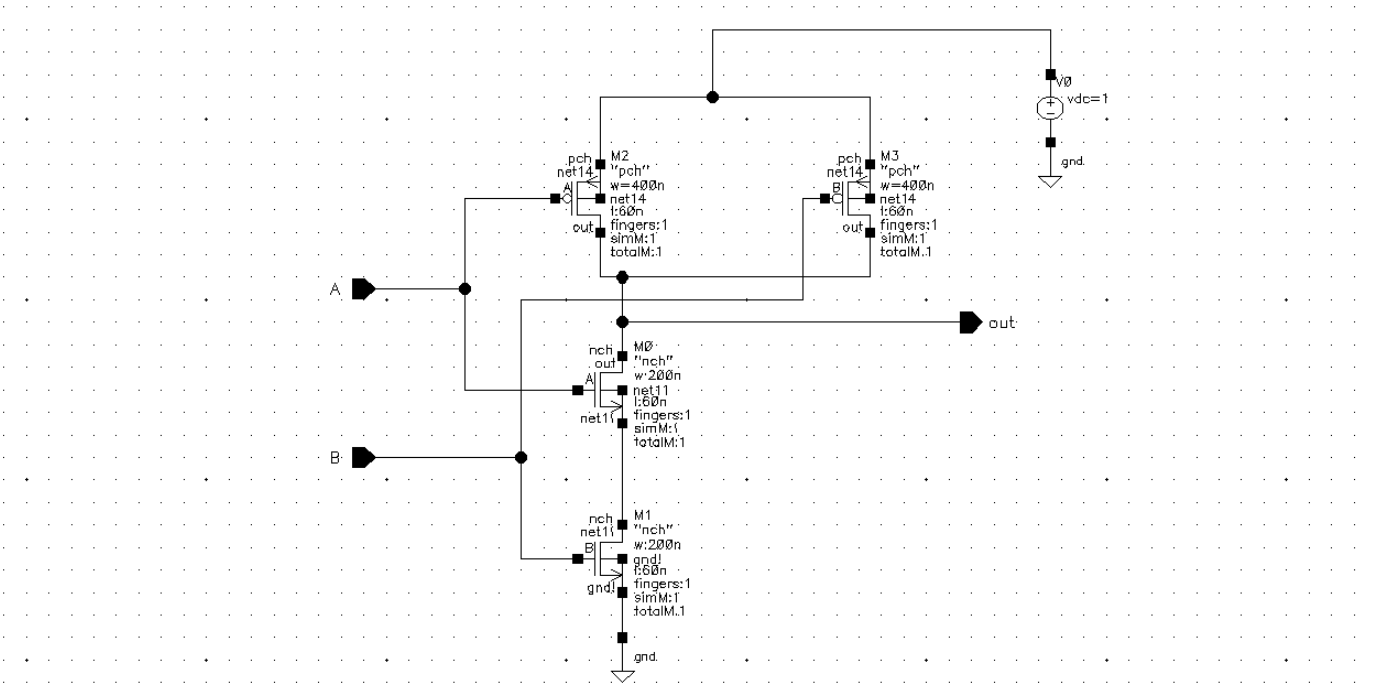

Figure 3: Schematic of 2input NAND gate

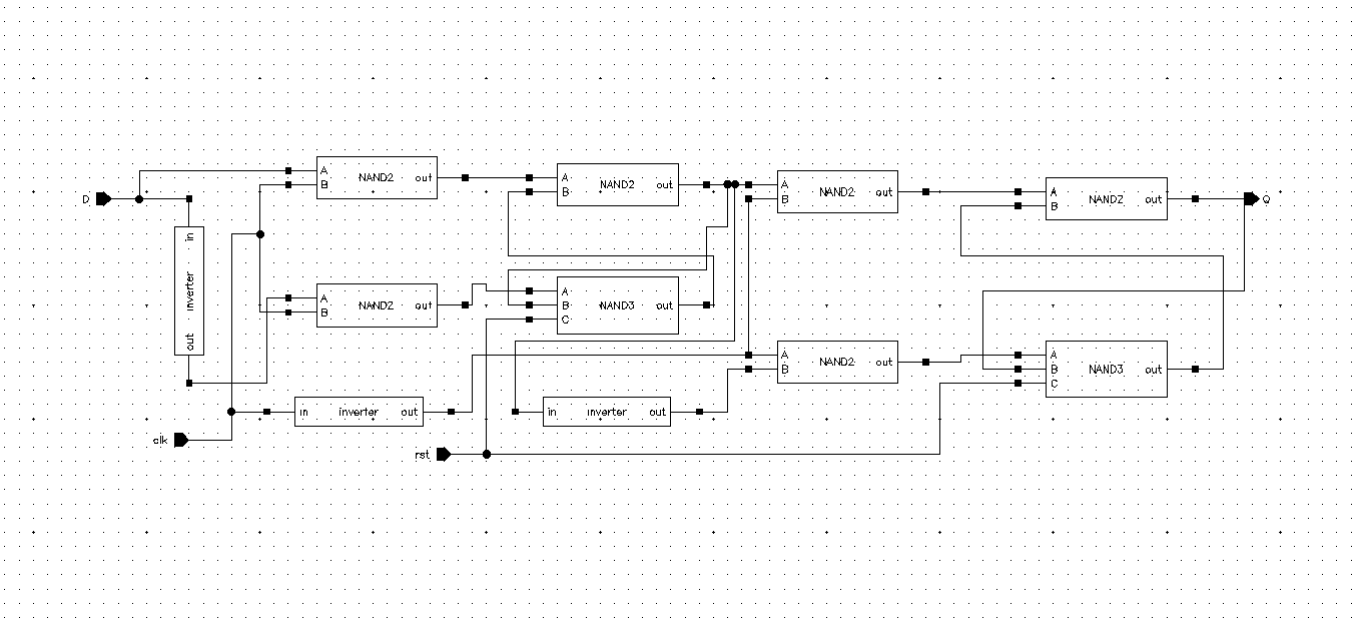

Figure 4: Schematic of D flip-flop used in PFD

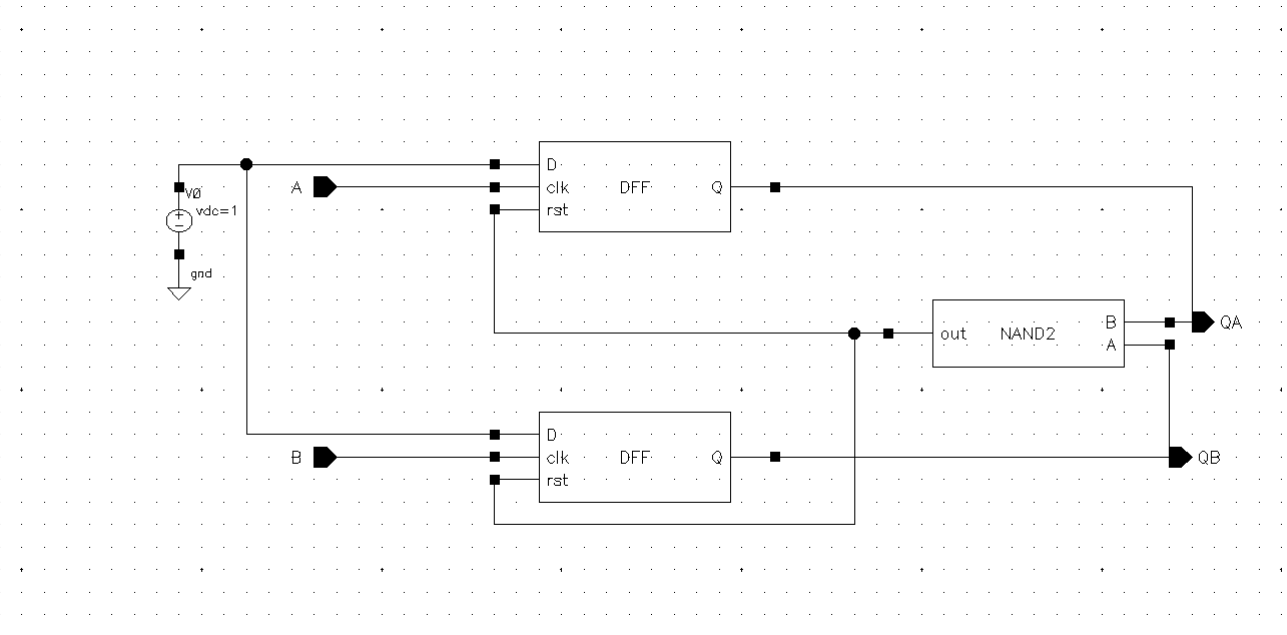

Figure 5: Schematic of PFD

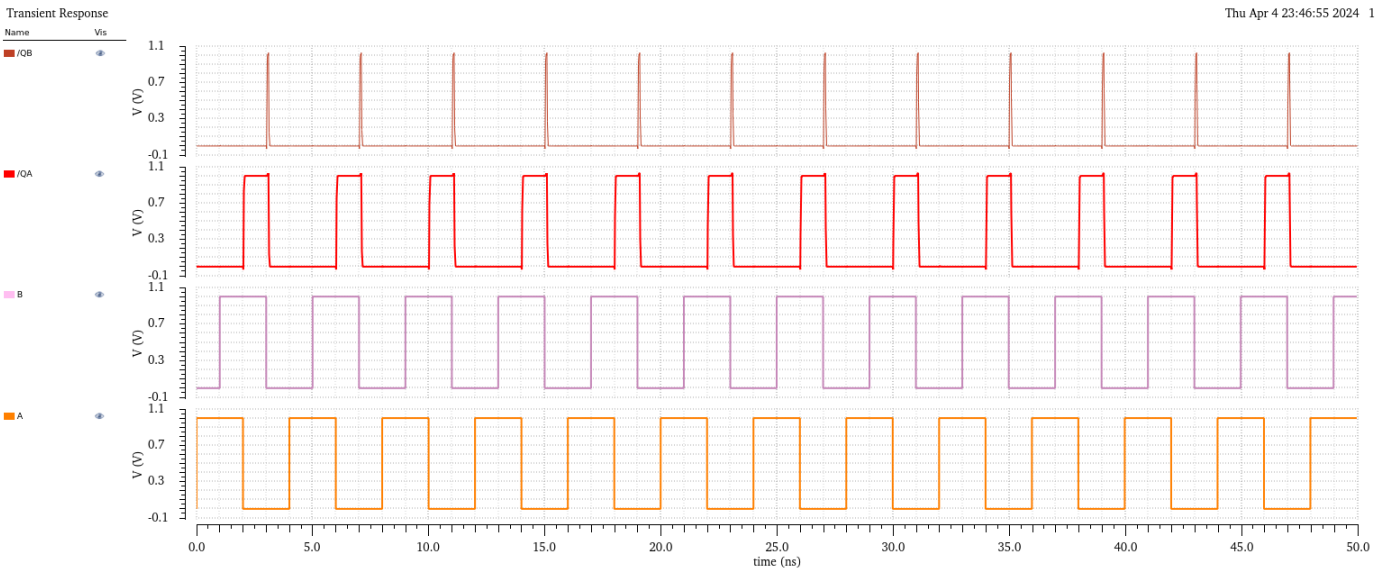

Figure 6: Output of PFD

3 Design of the Charge Pump and Loop Filter

The charge pump consists of two switches equipped with two symmetrical current sources. One current source is linked to a positive power supply, while the other is connected to a negative one. The switches alter their states based on the UP and DN signals. The output of the low-pass filter (LPF), determined by the UP and DN signals, is the Voltage-Controlled Oscillator (VCO) control signal.

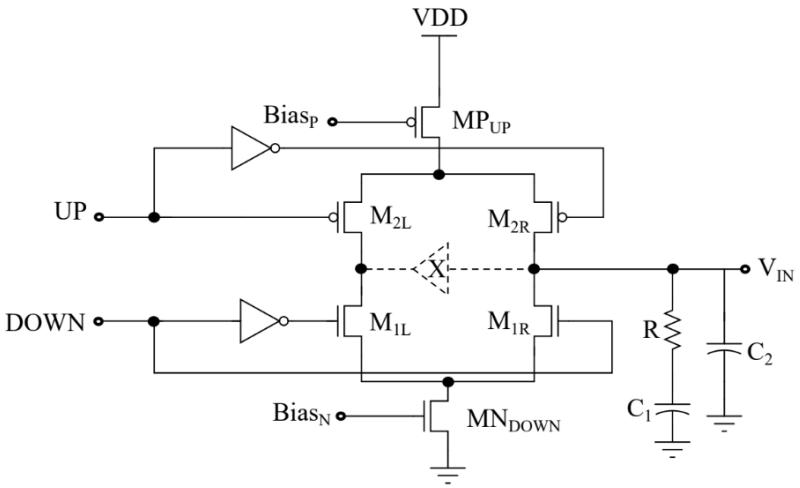

Figure 7: Circuit for charge pump and loop filter

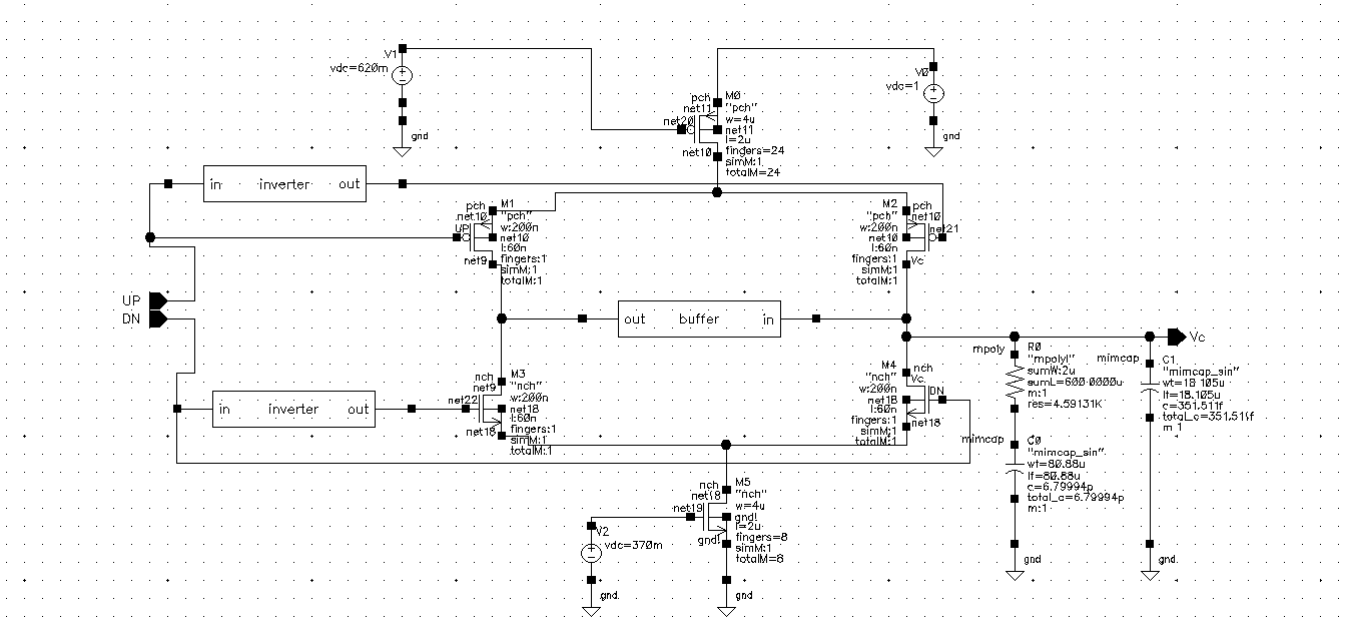

Figure 8: Schematic of Charge Pump with loop filter

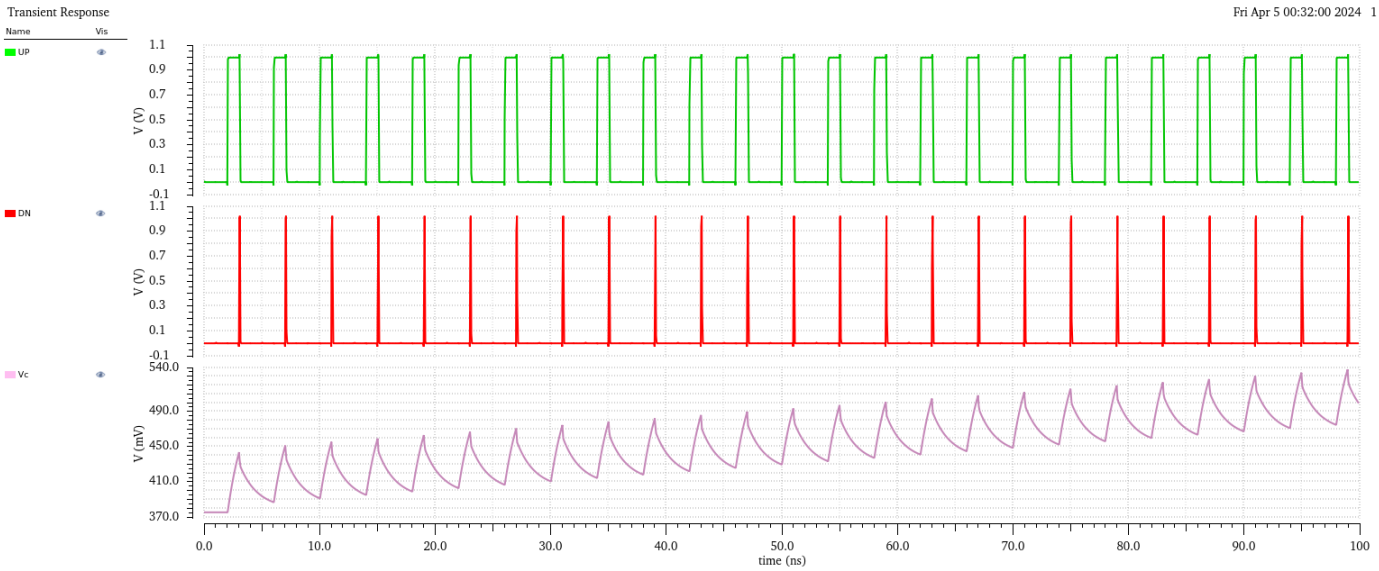

Figure 9: Output of Charge Pump

4 Design of Voltage Controlled Oscillator (VCO)

VCOs play a pivotal role in the architecture of a PLL. The fundamental concept behind a VCO is to generate a clock signal while adhering to the Barkhausen criteria for oscillation. According to the Barkhausen criteria, the magnitude of the VCO's transfer function at the oscillation frequency is unity, and the phase is at -180 degrees.

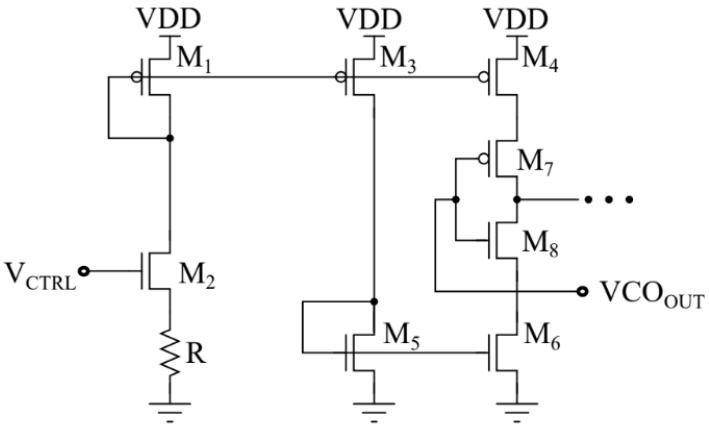

Figure 10: Circuit for VCO

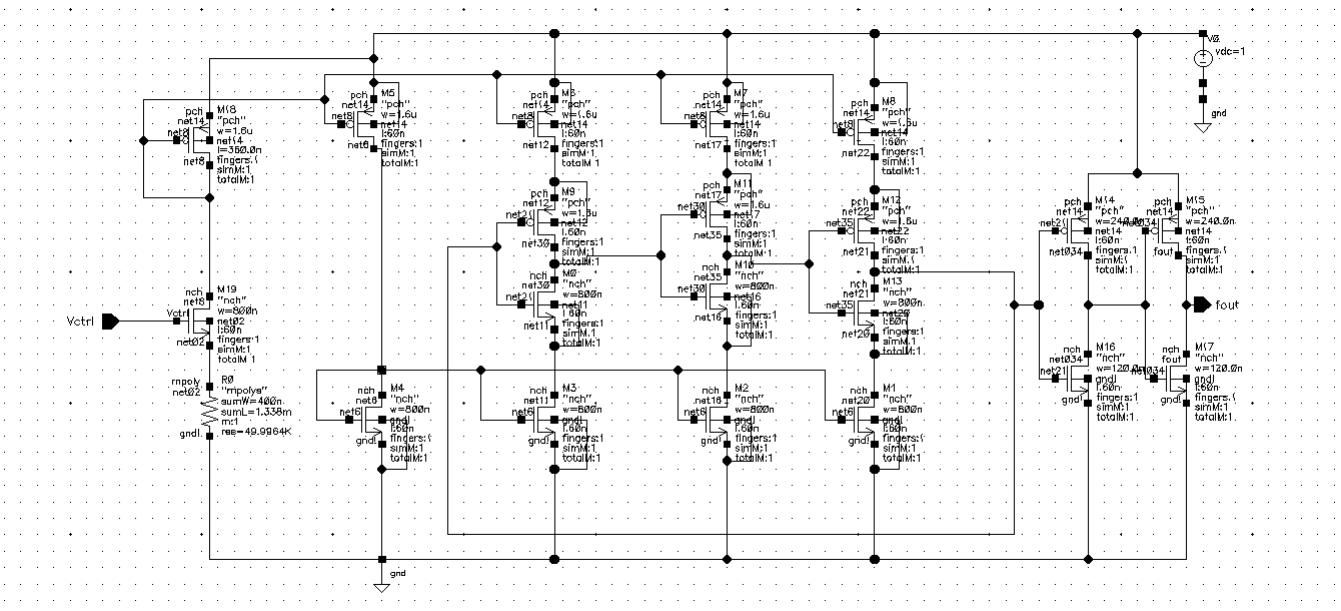

Figure 11: Schematic of VCO

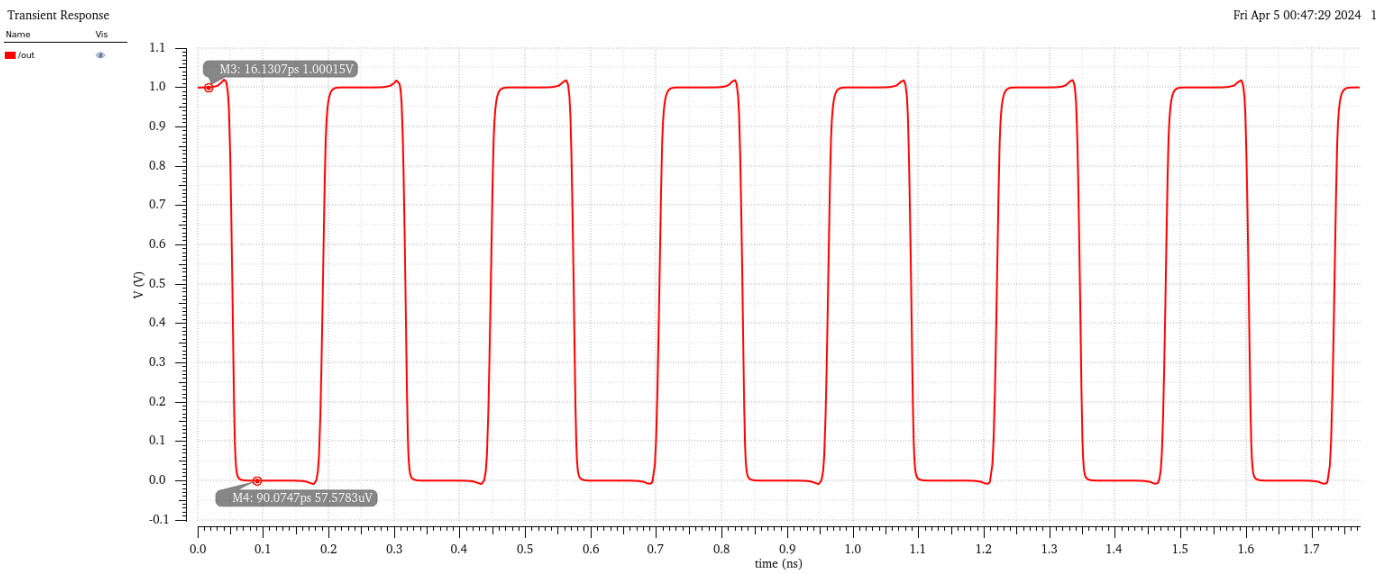

Figure 12: Transient response of VCO

This is the output of VCO when we have applied a dc voltage of 1 V to the VCO.The swing of the VCO can be verified from the graph.

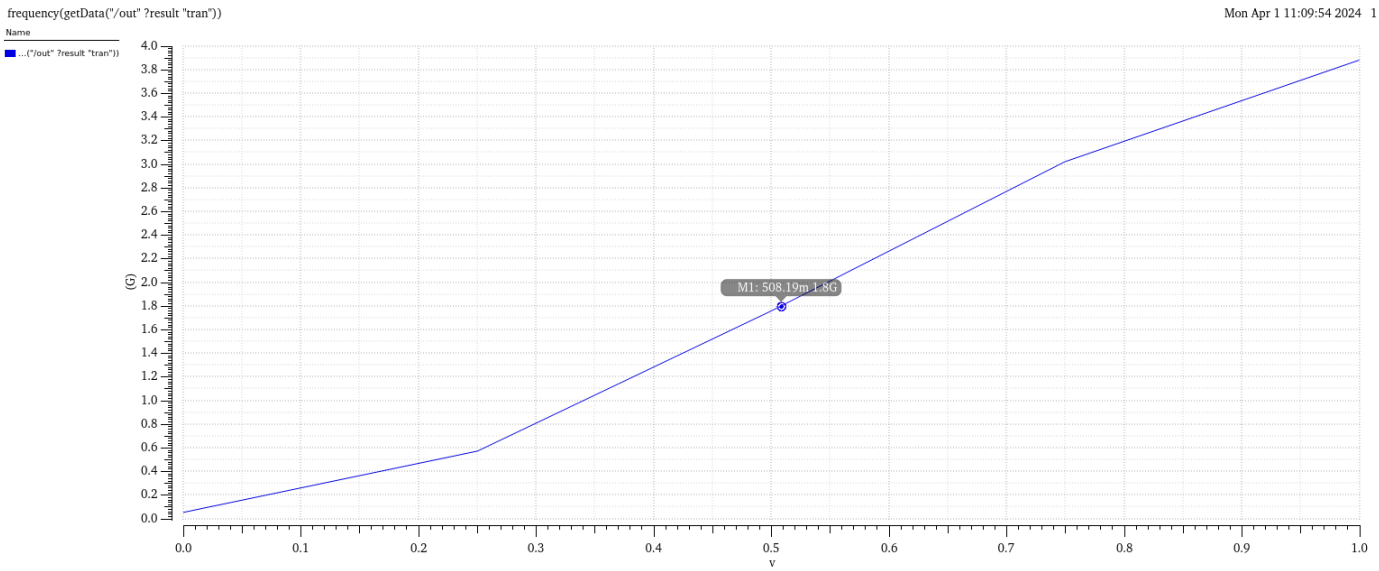

Figure 13: plot of frequency Vs Vctrl

This is the plot of frequency versus the control voltage.As our output frequency is 1.8 GHz, the voltage corresponding to this frequency is marked in the plot which is Vc=508.19 mV.

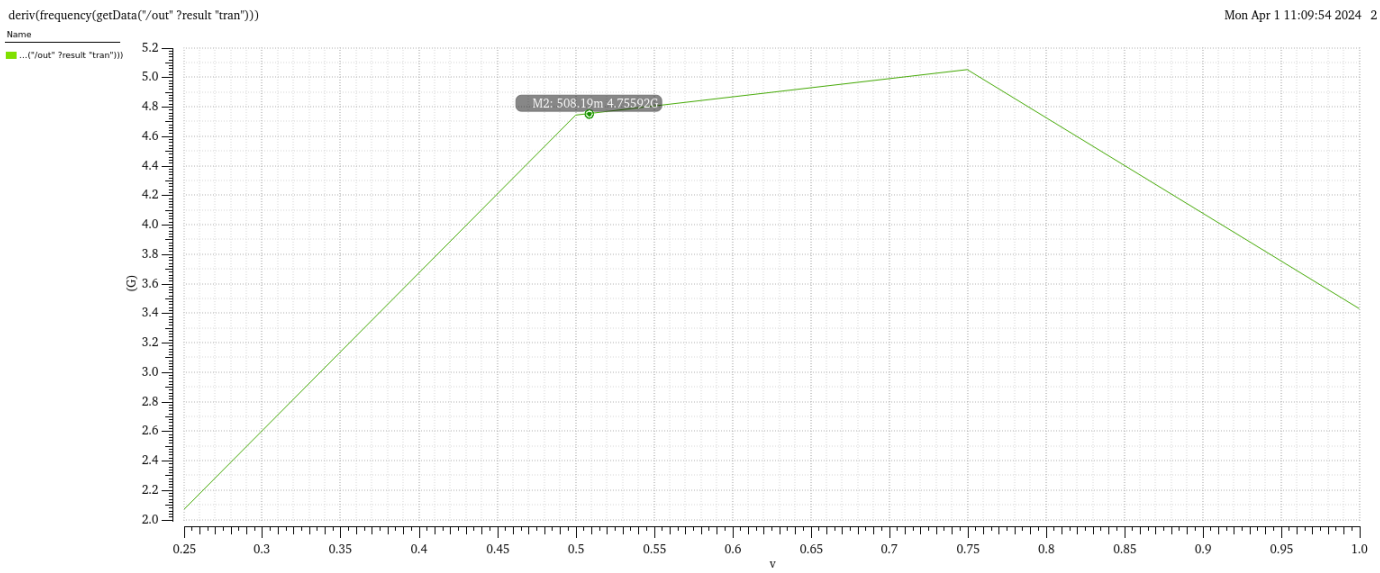

Figure 14: plot showing slope of frequency Vs Vc

To find the value of K_{VCO}, we have plotted the derivative of freq. Vs Vc curve and marked the value corresponding to Vc=508.19 mV and this value comes out to be 4.75 GHz/V.

5 Design Of Divider:

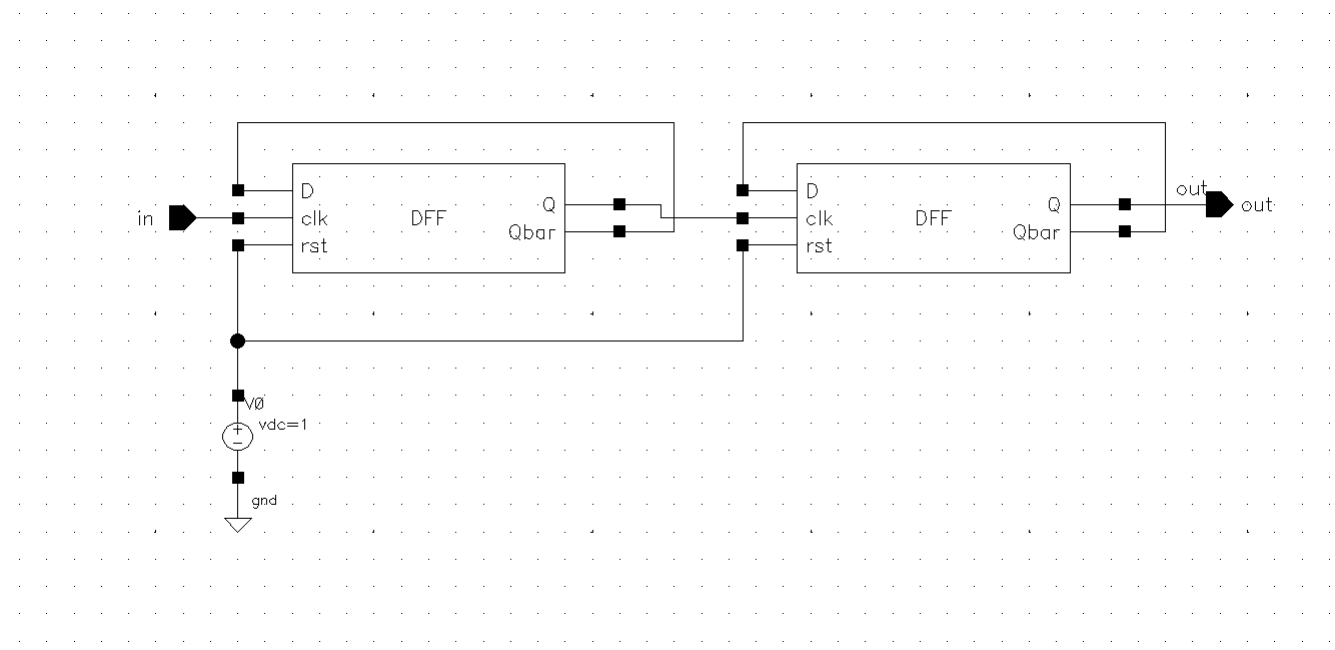

Figure 15: Schematic of divider

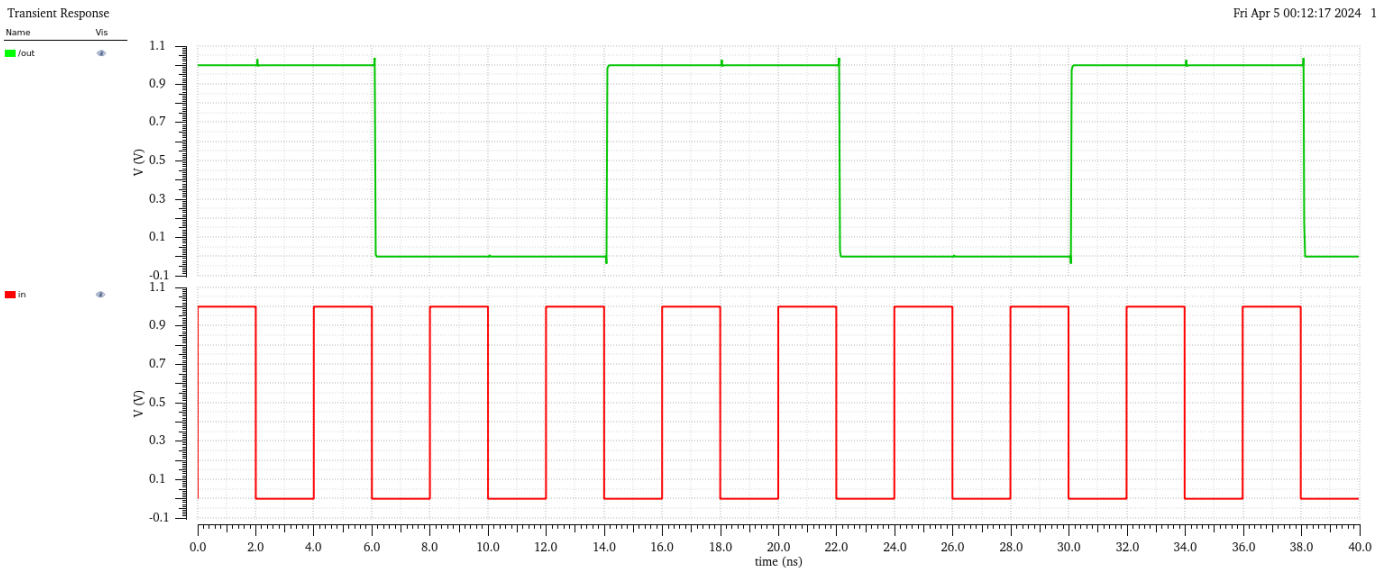

Figure 16: Transient response showing divider output

This is output of divider as our value of N=4, hence we require two D-flipflops in cascade.From the plot we can verify that the time period of the output pulse is four times the input pulse which means that the frequency is being divided by 4.

6 PLL Design:

Calculations:

Given reference frequency, f_{ref}=4.50 $\times$ 10^8 Hz
output frequency, f_{out}=1.8 $\times$ 10^9 Hz, Divider N=4

From the simulation of VCO we have find the value of K_{VCO}=4.75 GHz/V
Here we have assumed phase margin, $\phi_m = 65°$
From the value of phase margin we can find the value of b using the equation:

$$b = 2(tan^2\phi_m + tan\phi_m\sqrt{1 + tan^2\phi_m}) \tag{1}$$

On solving the above equation we get the value of b=19.346
From Gardener's Constraint we know that:

$$(\omega_u)_{loop} = \frac{\omega_{ref}}{20} = 1.4137 \times 10^8 rad/s \tag{2}$$

$$(\omega_u)_{loop} = (\sqrt{b+1})\omega_z \tag{3}$$

$$\omega_z = 0.3129 \times 10^8 rad/s \tag{4}$$

Now from the equation:

$$\frac{K_{VCO} \times I_o}{N} = \frac{(b+1)^{1.5}}{b} \times C_1 \times \omega_z^2 \tag{5}$$

putting the values of K_{VCO},b,ω_z,N we get the relation:

$$I_o = 3.91 \times 10^6 C_1 \tag{6}$$

Taking the value of charge pump current I_o=35 μA, we will get c_1 = 8.95 pF

From the equation:

$$b = \frac{C_1}{C_2} \tag{7}$$

we get $C_2 = 0.46$ pF

$$\omega_z = \frac{1}{R_1 C_1} \tag{8}$$

we get $R_1 = 3.57k\Omega$

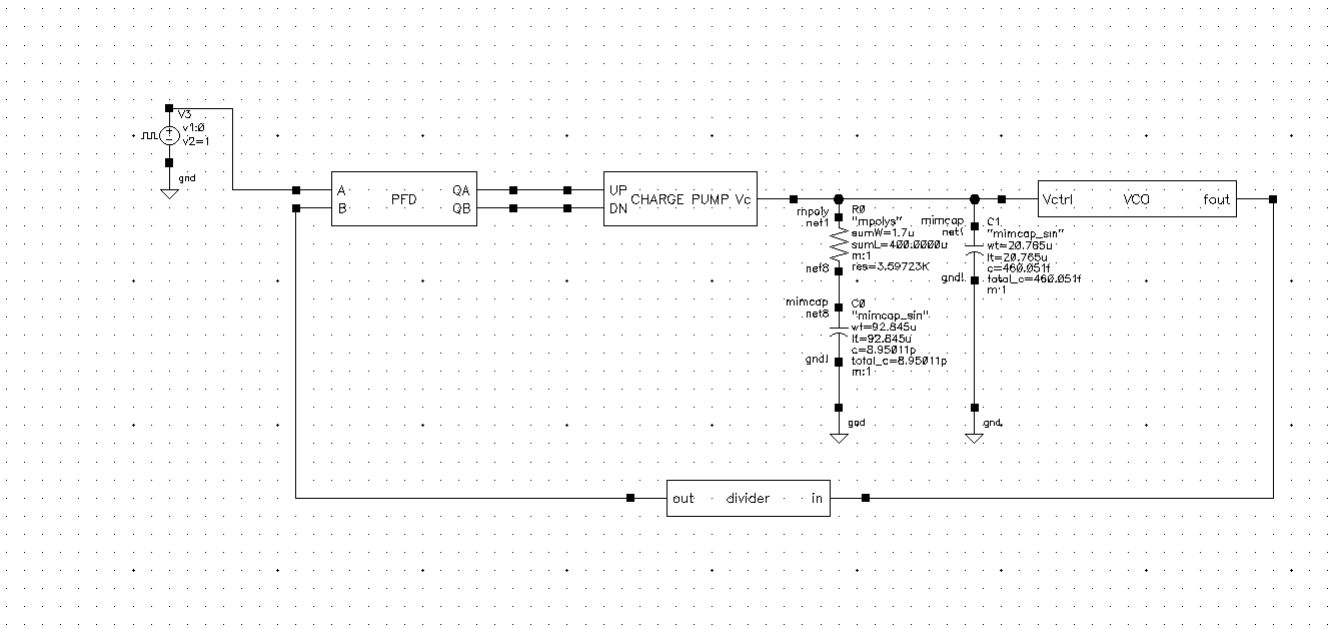

Figure 17: Schematic of PLL

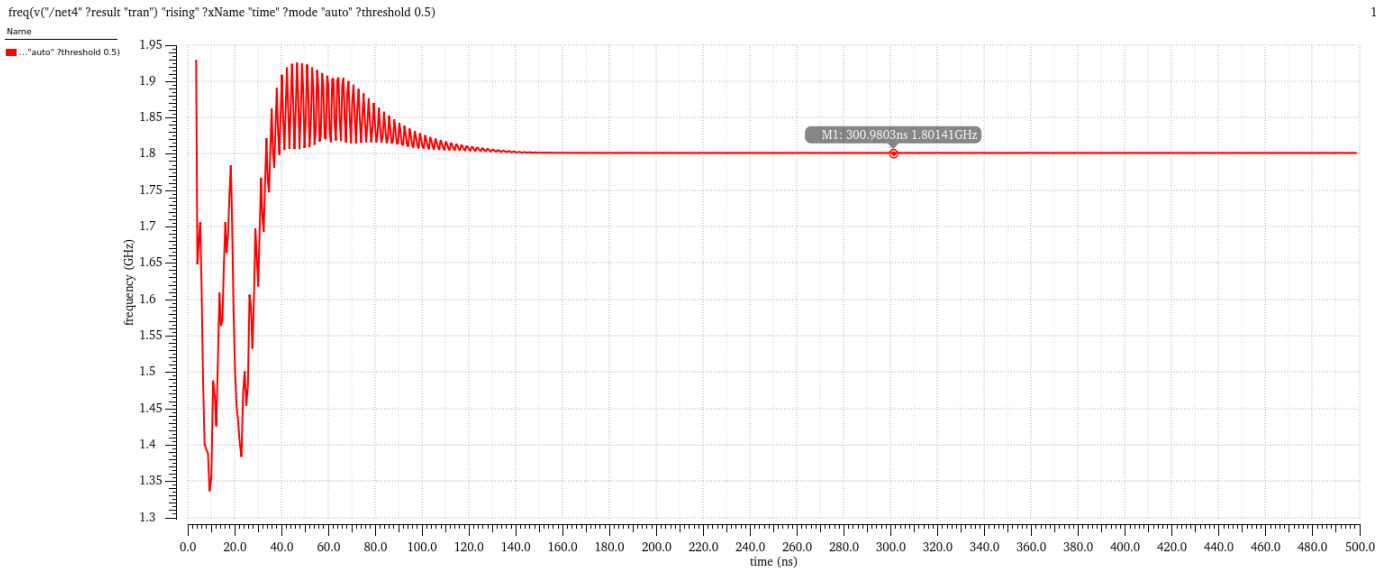

Figure 18: Output of PLL

From this plot we verify that our PLL is working fine and locking the output frequency at 1.8 GHz.

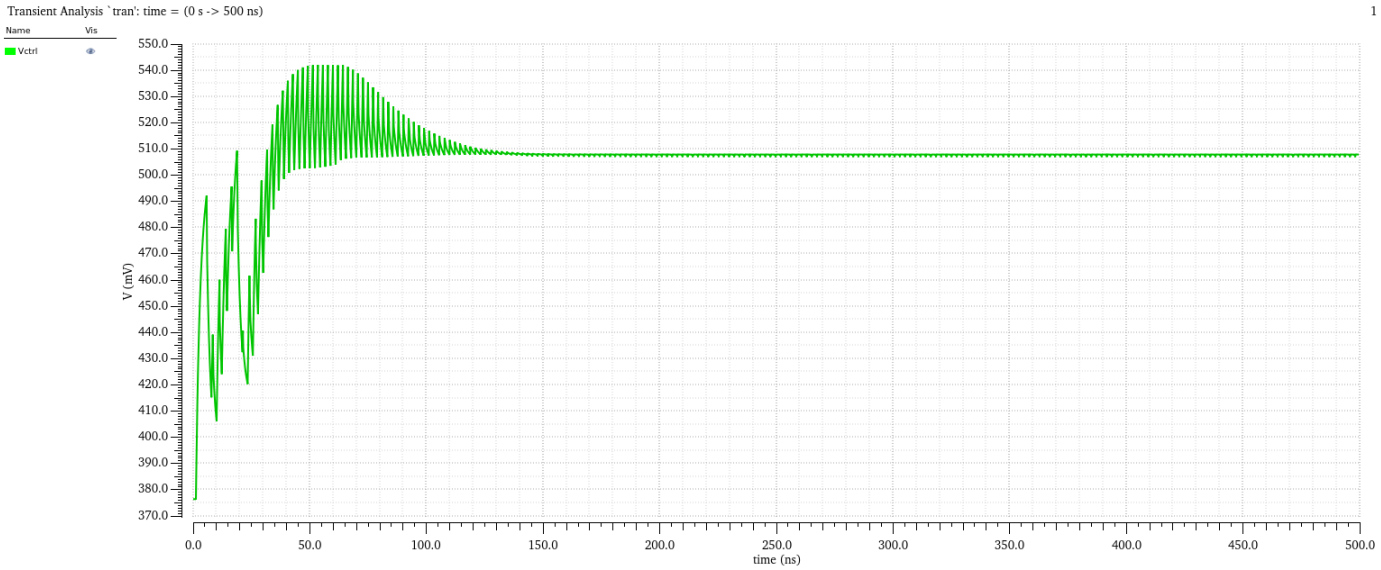

Figure 19: plot of Vc

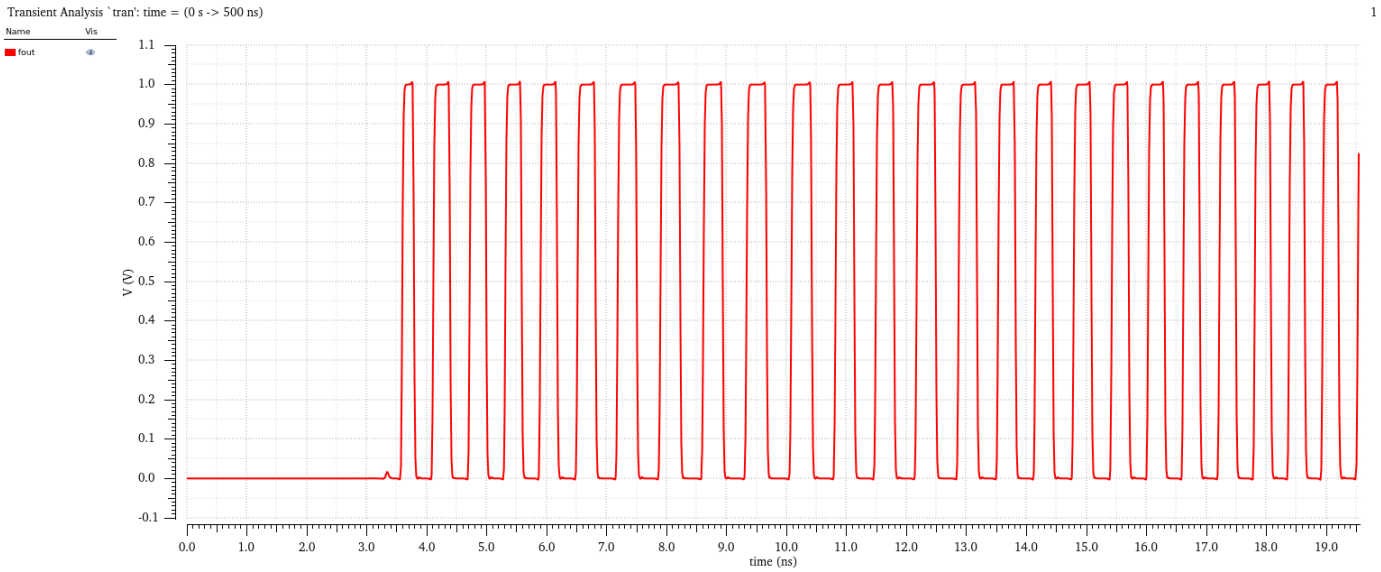

Figure 20: Transient response of PLL

7 Conclusion

Here in this project we have designed a phase-locked loop with a given reference frequency and output frequency and with divider, N=4.Here we have done transistor level implementation of PLL in 65nm TSMC tech node using cadence design suit.The required specifications have been achieved such as total capacitance used equal to 9.41 pF which is less than 25 pF and the charge pump current is $35\mu A$ which is less than $100\mu A$.

8 References

1.) Behzad Razavi, “Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level” , Cambridge University Press, 2020.

2.) P. K. Hanumolu, M. Brownlee, K. Mayaram and Un-Ku Moon, “Analysis of charge-pump phase- locked loops,” in IEEE Trans. on Circuits and Syst. I: Regular Papers, vol. 51, no. 9, pp. 1665-1674, Sept. 2004.

3.) H. R. Rategh, H. Samavati and T. H. Lee, “A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless LAN receiver,” in IEEE J. of Solid-State Circuits,vol. 35, no. 5, pp. 780-787, May 2000.